A 1.5-to-5.0GHz Input-Matched +2dBm P_{1dB} All-Passive Switched-Capacitor Beamforming Receiver Front-End in 65nm CMOS

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Phased arrays in CMOS for consumer communication bands aim to enhance receiver performance by exploiting beamforming with antenna arrays. Sensitivity increases with the number of antenna elements through array gain and interferers can be cancelled through the spatial filtering of the beam pattern [1]. For the latter, the linearity of the receiver before the beamforming summing point becomes a bottleneck as interferers are not cancelled yet. Phase shifting in the LO domain reduces the complexity in the signal path and enables the use of linear signal blocks, but has high requirements on the multi-phase LO generation [2]. On the other hand, a switched-capacitor phase shifter can be very linear, but is limited by the linearity of the necessary input matching and element summing gm-stages [3]. This paper proposes a fully passive phased array receiver front-end which implements impedance matching, phase shifting and element summing with only switched-capacitor stages for a high linearity.

The principle of a vector modulator phase shifter is illustrated in Fig. 1. (top left). A phase shift φ between 0° and 90° can be accomplished by adding two orthogonal signal phases weighted by respectively the sine and cosine of φ. For a full 360° phase shift range, four signal phases are required. These phases can be accurately generated for a wide RF frequency band by performing downconversion with the 25% duty cycle clocked passive quadrature mixer in Fig. 1. (top right).

In order to obtain RF input matching the mixer is loaded with baseband resistors R_{BB} [4]. Fig. 1. (bottom) illustrates conceptually how these resistors can be replaced by a charge redistribution switched-capacitor network that preserves the input matching, while also generating the cos*(φ)* and sin*(φ)* weighted voltages necessary for vector modulation similar to [3]. In the first step, the resistor can be simulated by charging a unit capacitor to the input voltage and then dumping the charge to ground. In the second step, this switched-capacitor circuit can be split in two according to the fraction α, without affecting the input impedance. Finally, as the capacitor charges are dumped anyway, they can first be redistributed across empty 3/4 capacitors to yield a voltage transfer function of *α / (α+¾)* and *(1-α) / (1-α+¾)* respectively. These transfer functions are adequate approximations of the sine and cosine, so that *uniform* steps in *α* correspond to *uniform* steps in phase shift *φ* [3]. The resulting circuit slice is implemented with NMOS switches and 5-metal fringe capacitors (Fig.2). As the *α* and *(1-α)* capacitor are complementary, they can be implemented by a single binary capacitor bank. Two additional 1/16 capacitors provide a fixed 1/2b phase offset to prevent phase points from overlapping on the X and Y axis in the phasor diagram in Fig. 1. (top left).

With the passive mixer loaded by four sine/cosine approximation slices instead of resistors, the 8 weighted components of the phasor diagram are available and 2 of them have to be summed to form the phase shifted vector modulator output. By shifting the clocking of each slice so that they are trailing their respective mixer switch, each slice produces a valid output at a different clock phase. By connecting the 2 desired outputs together, the voltages will be combined in a time-interleaved manner, which can be interpreted after lowpass filtering as averaging in the time

domain. Because of the 25% duty cycle clock, 2 slices will only produce an output half of the time, so each mixer output needs an additional slice with clocking shifted by half a period. Combined, the mixer and 8 slices form an antenna element in the 4-element phased array receiver front-end shown in Fig. 3. The unused slice outputs are not wasted, but are formed into three additional phase shifted signals to provide a differential In-phase and Quadrature baseband output for image rejection. With the element outputs available on switched capacitors, it is natural to do the summing for beamforming in the *charge* domain instead of the conventional *current* domain by simply connecting the elements together. When the right-most switch in a slice closes, the associated 3/4 capacitors in each element see each other and the *summed* charge is redistributed, resulting in a common voltage which is an *average* of the elements.

To provide the 25% duty-cycle 4-phase LO, first an external clock at twice the frequency is divided-by-two with fast Current Mode Logic (CML) blocks and then the duty-cycle is reduced from 50% to 25% with AND gates. The supply power consumption is mostly dynamic from the charging and discharging of switches and CMOS clock gates, with a small static contribution of the CML stage. All switched-capacitors are biased to 0V, so that the clock inverter drivers can directly drive the switches with a full supply voltage overdrive for low switch-on resistance and high linearity. Note that an application specific RF band filter and LNA can be added easily to improve the element sensitivity, due to the impedance matched RF input.

The chip is implemented in 65nm LP CMOS (fig. 7.) with a 1.2V supply and an active area of $0.18mm^2$. Fig. 4. (top left) shows the measured phase steps of a single element for different LO frequencies. The associated gain variation is plotted in Fig. 4 (top right). As the phase shift

depends only on capacitor ratios, the phase settings are stable over a wide frequency band (with some degradation above 4GHz due to finite clock rise/fall times). To test the performance of the summing node, all RF inputs were excited with an equal-phase signal and the phase shifters were set to provide an increasing phase difference between elements. The resulting transfer is plotted in Fig. 4 (bottom), showing a quantized beam pattern shape. As expected, cancellation occurs for $\Delta\varphi$=-180, -90, 90 and 180 degrees, with a null depth of more than 30dB.

Fig. 5 (top) shows that the input matching follows the LO frequency and forms a high-Q bandpass filter with bandwidth set by the mixer effective pole frequency of 300 MHz, which suppresses out-of-band interferers [5]. Fig. 5 (bottom) plots the gain, noise figure (NF), and 1dB compression point (P_{1dB}) of a single element and the chip power consumption, for different LO frequencies. As there are no biased gm-stages, the supply voltage can be lowered without affecting functionality, for a lower power consumption. Dropping the supply from 1.2V to 1.0V reduces the supply power to 65%, with no significant changes in the phase shifter performance. The price to be paid is a maximum LO frequency of 4GHz before the clock divider fails, and a 4dB lower P_{1dB} and 0.3dB higher NF (kT/C noise is dominant) due to the decreased overdrive voltage on the switches.

Fig. 6. summarizes the measured performance and compares with [2] and [3]. The high 2dBm compression point of a receiver element provides excellent resilience to interferers before they can be cancelled by the beamforming. Moreover, the presented chip has a spurious free dynamic range better than or comparable to the state-of-the-art, in the smallest active area and for the lowest supply power.

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Captions:

Figure 1: Impedance-matched mixer with switched-capacitor vector modulator.

Figure 2: Implementation of sine/cosine-approximation slice.

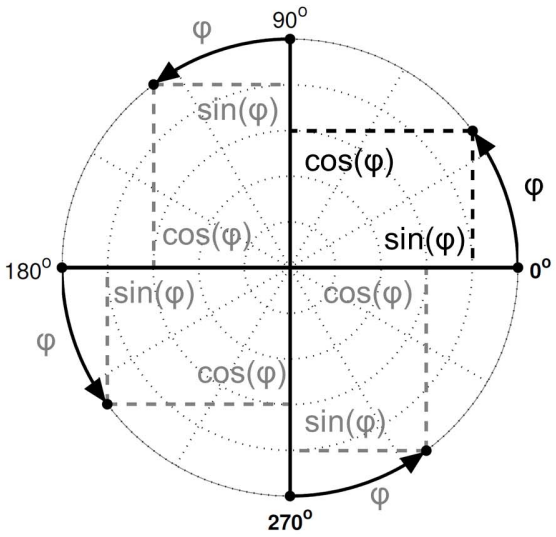
Figure 3: All-passive phased array receiver architecture.

Figure 4: Measured single-element phase shift and gain variation for the 32 phase shifter settings (top) and 4-element cancellation pattern (bottom).

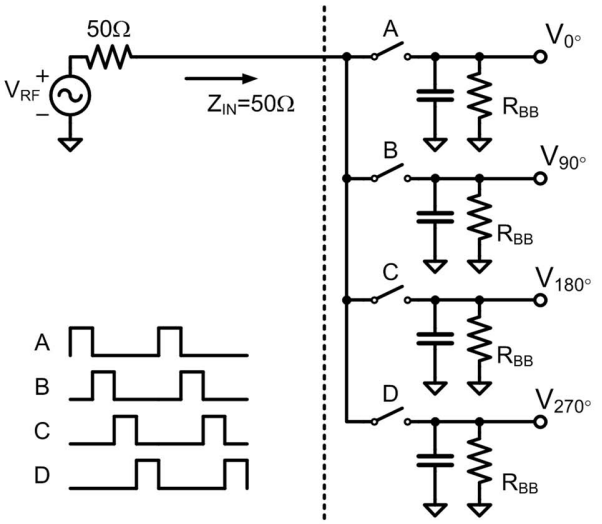
Figure 5: Measured S11 (top), gain, NF, P_{1dB} and power consumption (bottom).

Figure 6: Comparison table.

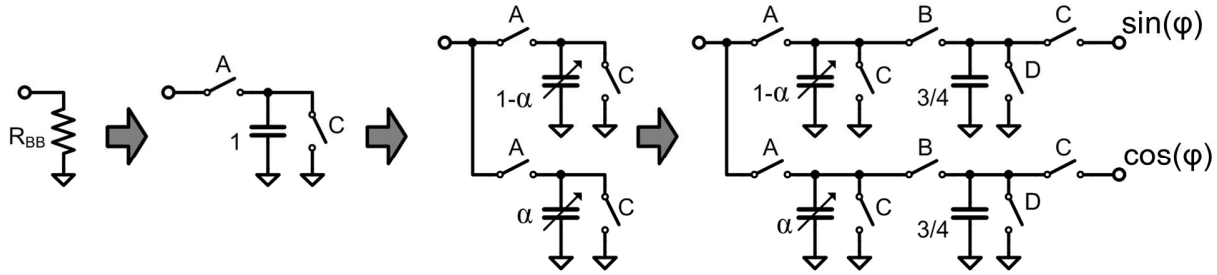
Figure 7: Chip micrograph.



4-phase vector modulator principle



Impedance-matched passive mixer with 25% duty cycle 4-phase clock



Transformation of a resistor into an approximate-sine/cosine slice, $\alpha=\varphi/90^{\circ}$

Figure 1: Impedance-matched mixer with switched-capacitor vector modulator.

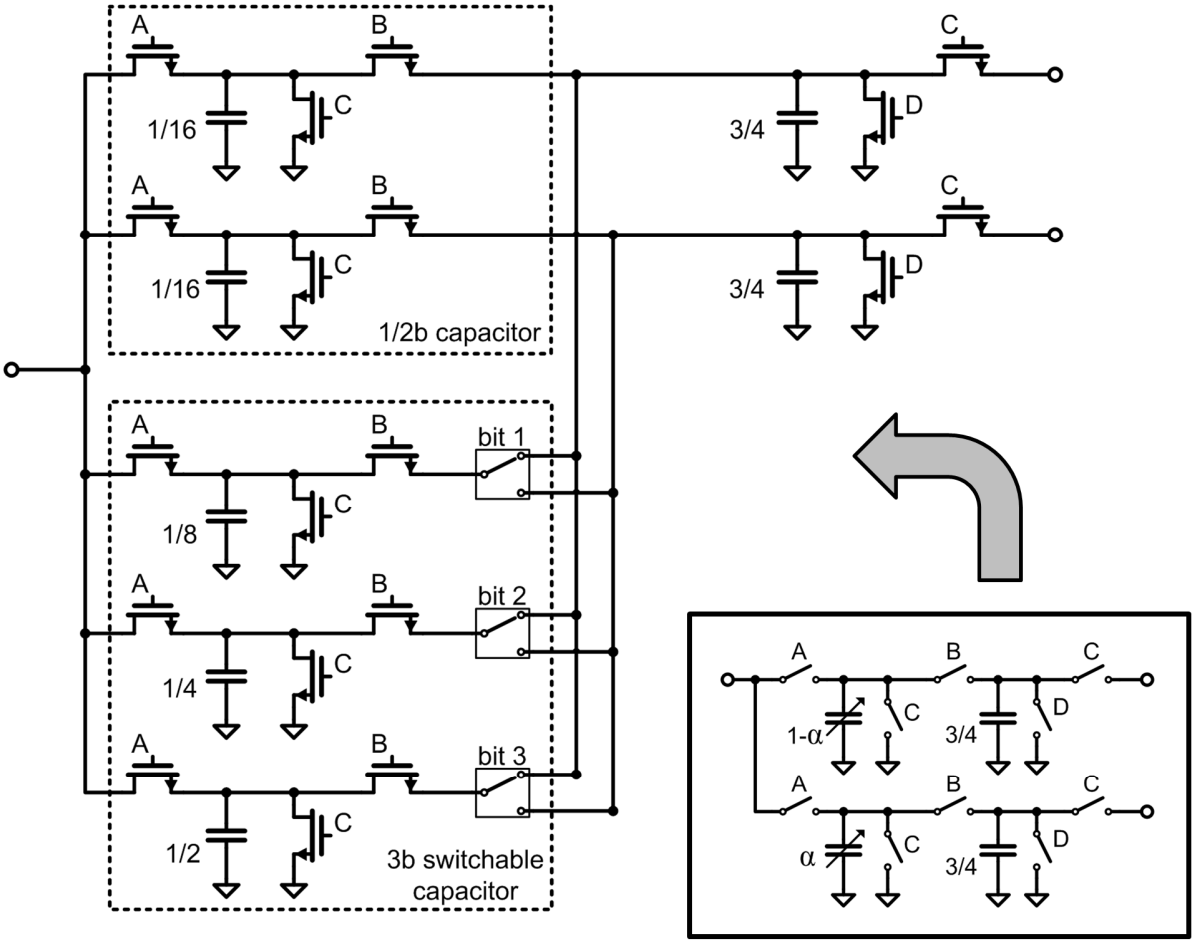


Figure 2: Implementation of sine/cosine-approximation slice.

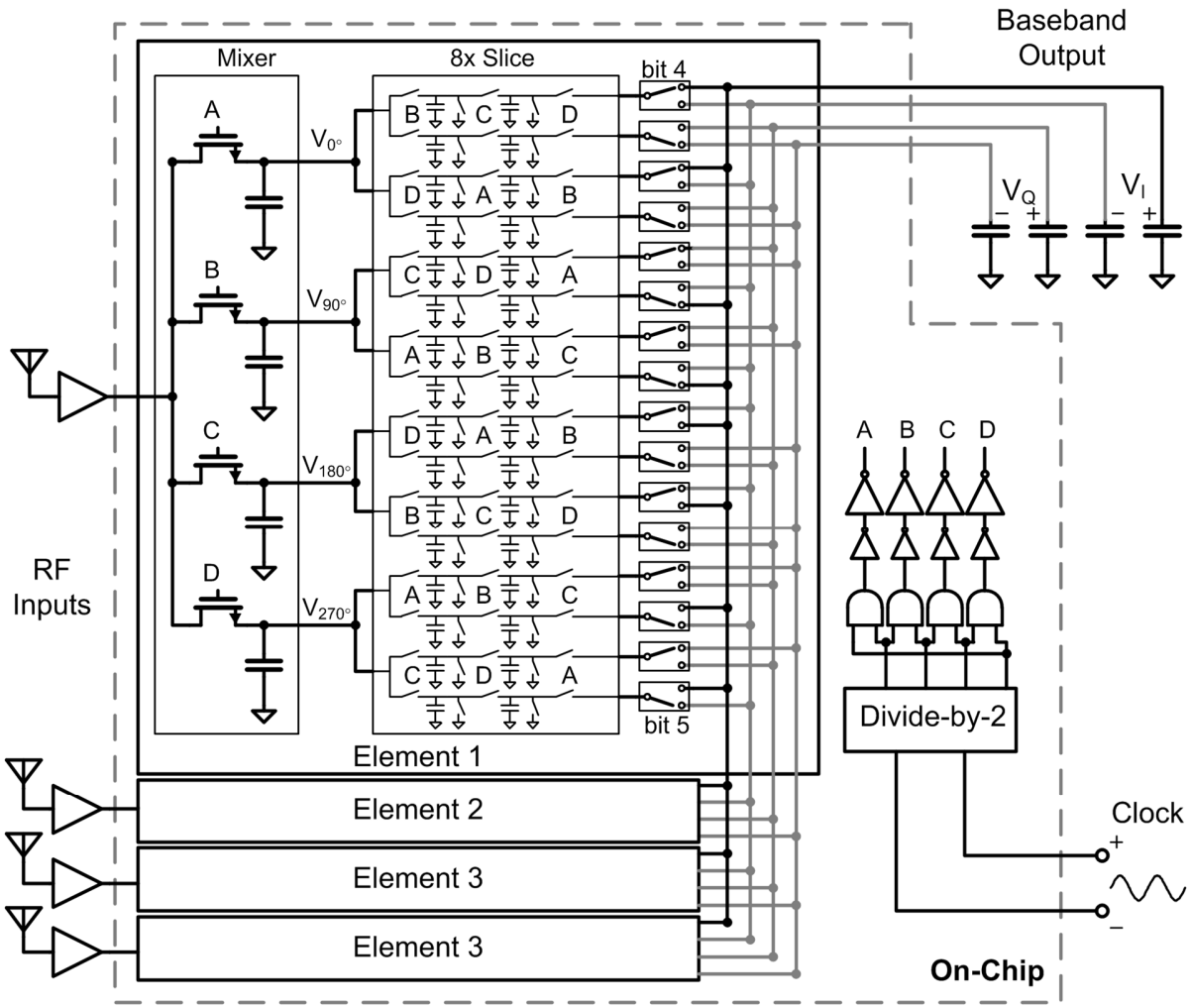


Figure 3: All-passive phased array receiver architecture.

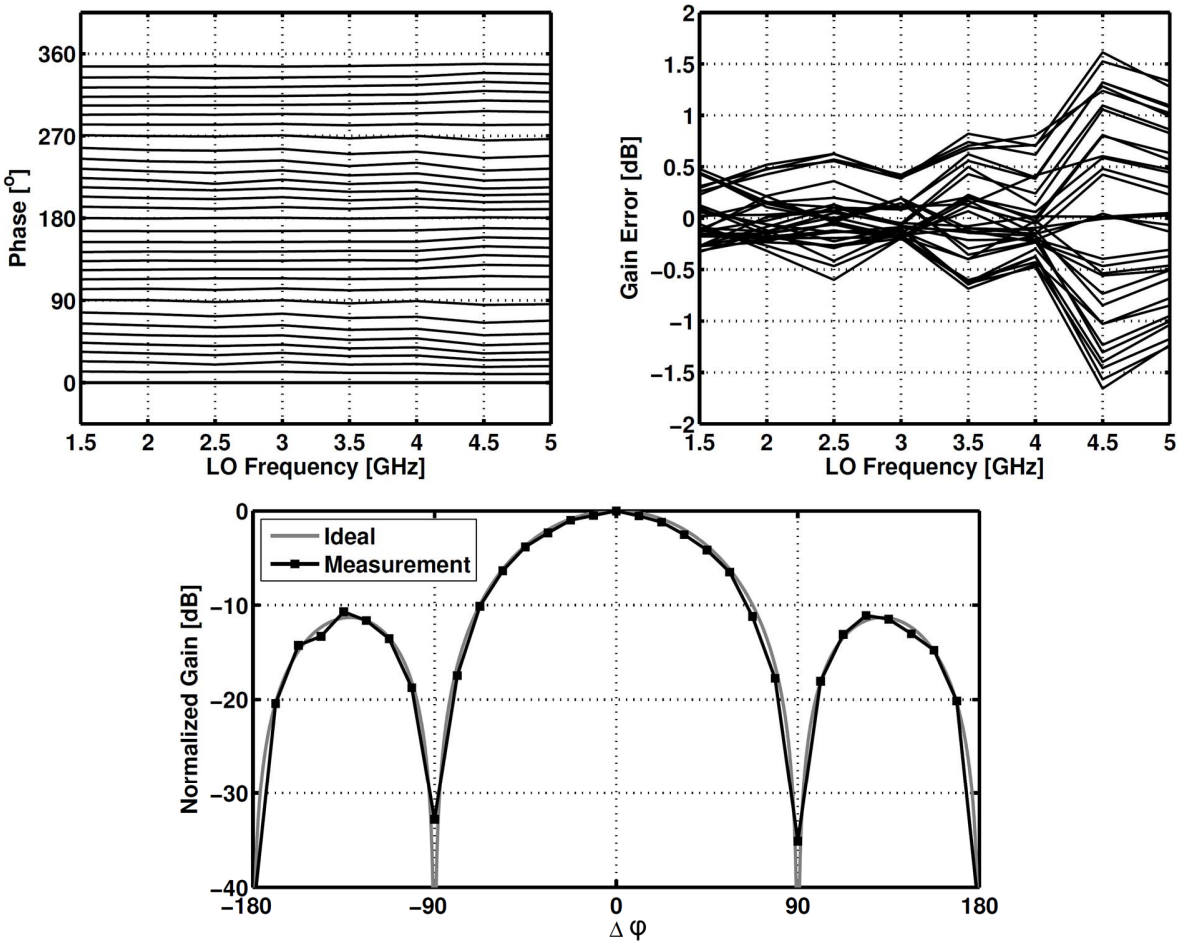


Figure 4: Measured single-element phase shift and gain variation for the 32 phase shifter settings (top) and 4-element cancellation pattern (bottom).

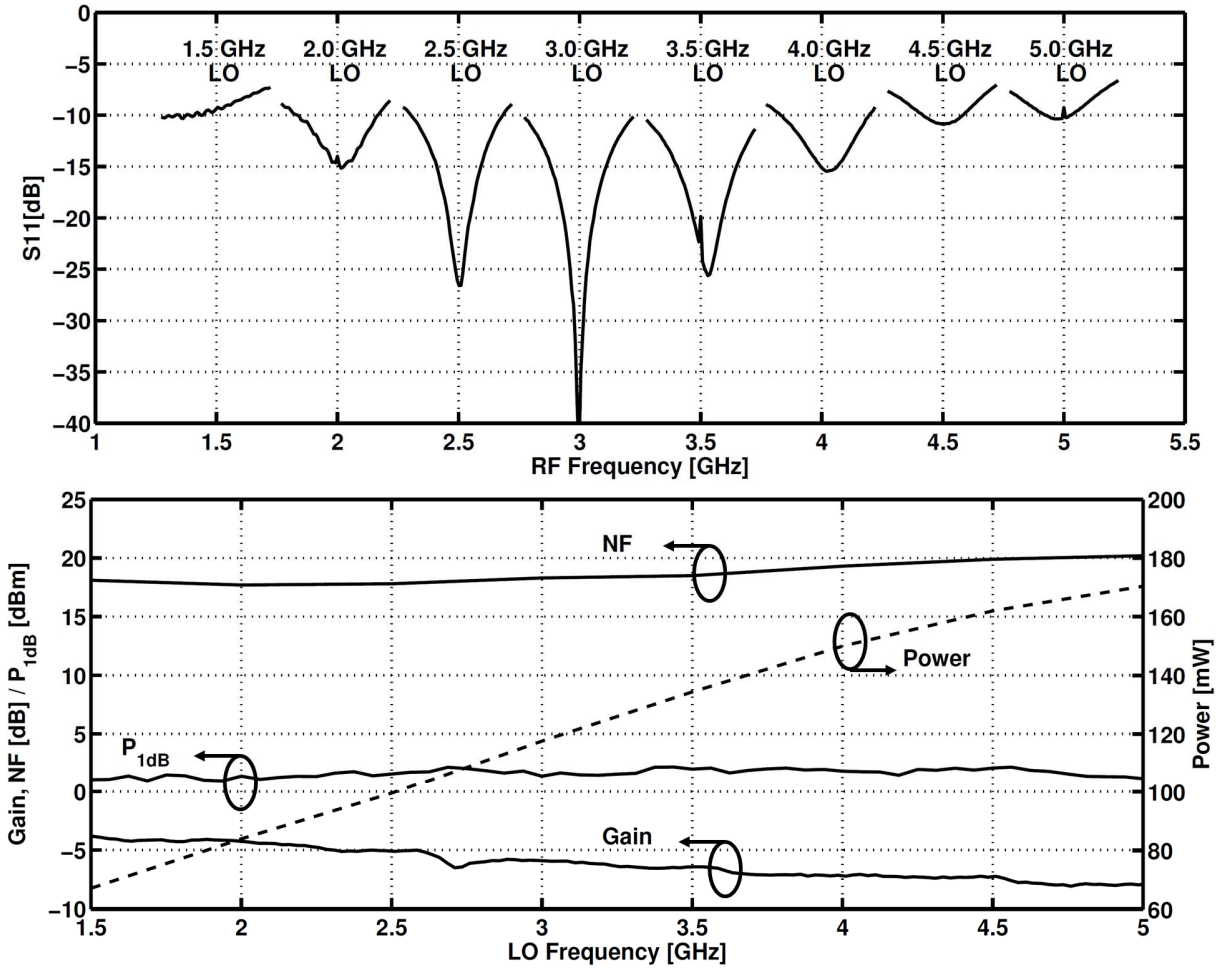


Figure 5: Measured S11 (top), gain, NF, P_{1dB} and power consumption (bottom).

	[2]	[3]	This Work	
Technology	90nm	65nm	65nm	
Active area	1.40 [a]	0.44	0.18	mm^2
Supply voltage	1.2	1.2	1.0 - 1.2 [b]	V
RF input-matched frequency band	4.0	1.0 – 4.0	1.5 – 5.0	GHz
Power consumption	166	308 [c]	65 – 168	mW
Array elements	4	4	4	
Single Element Performance:	@ 4.0 GHz	@ 2.5 GHz	@ 3.0 GHz	
Gain	12	16	-6	dB
Input-referred in-band 1dB compression point	N/A	-14	2	dBm
Noise figure	7.5	10	18	dB
Input-referred in-band IP3	2	-1	13	dBm
Input-referred in-band IP2	45	40	69	dBm
Spurious free dynamic range in 1MHz bandwidth	72	68	72	dB
Phase shift step	11¼	11¼	11¼	°
Phase error (RMS)	N/A	1.4	2.0	°
Amplitude error (RMS)	N/A	0.4	0.2	dB
Vector modulator EVM	2	5	4	%

[a] Estimated from chip photo.

[b] All figures are for 1.2V supply.

[c] For 2.5GHz RF.

Figure 6: Comparison table.

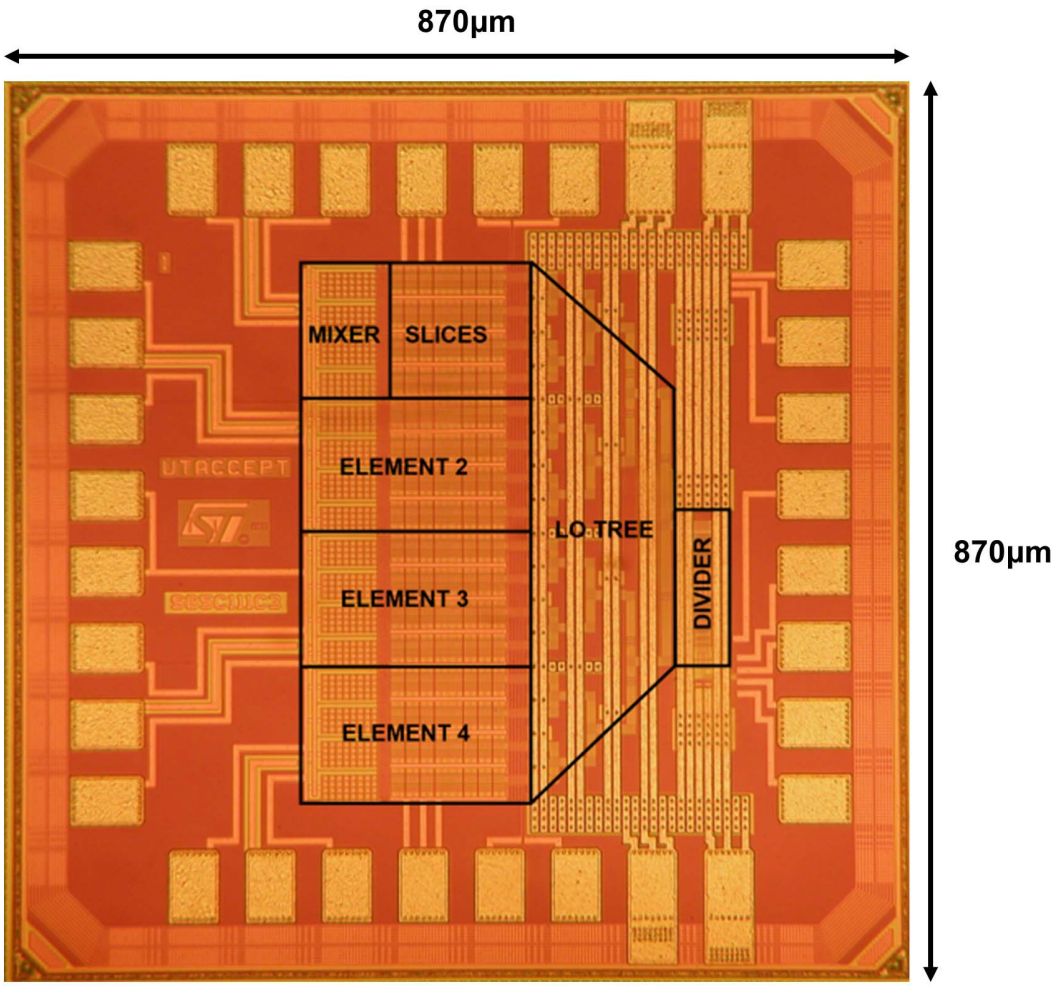


Figure 7: Chip micrograph.