Identifying Failure Mechanisms in LDMOS Transistors by Analytical Stability Analysis

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***Abstract*—In this work, analytical stability equations are derived and combined with a physics-based model of an LDMOS transistor in order to identify the primary cause of failure in different operating and bias conditions. It is found that there is a gradual boundary between an electrical failure region at high drain voltage and a thermal failure region at high junction temperature. The theoretical results are mapped onto a 3D space comprising gate-width normalized drain current, drain voltage and junction temperature, allowing an immediate visualization of the different failure mechanisms. The validity of the proposed analysis is supported by measurements of the safe operating limits of silicon-on-insulator (SOI) LDMOS transistors.**

***Index Terms*—Power MOSFET, Silicon-on-insulator (SOI), electro-thermal coupling, electrical runaway, thermal runaway, parasitic bipolar, impact ionization, self-heating, Safe Operating Area (SOA), Safe Operating Volume (SOV), stability factor, failure function.**

I. Introduction

In power transistors, failure is often associated to instability, which causes one or more device parameters (current, voltage and/or temperature) to diverge (runaway) [1]. Stability can be experimentally investigated by measuring the device characteristics close to the failure limit [2]–[6]. This allows calculation of a stability factor that is a measure of the device sensitivity to runaway. However, such a procedure has two drawbacks: 1) it can degrade device reliability; 2) it detects the occurrence of instability but not its physical origin (electrical or thermal). In order to overcome the first drawback, physics-based models [2], [3], [5], [7], [8] or TCAD simulations [9] have been used to predict and quantify instability. However, modeling and simulating runaway effects causes the output parameters to diverge and makes it difficult to identify the physical origin of the numerical instability.

In this work, it is shown how an analytical stability analysis can be used to identify the boundary between electrical and thermal failure mechanisms (Fig. 1). Electrical and thermal stability factors (and corresponding failure functions) are defined (Figs. 2-3) assuming that self-heating does not play a role in electrical runaway, while avalanche breakdown and parasitic bipolar do not affect thermal stability.

Device failure can be related to an electro-thermal stability factor (failure function) including both the electrical and thermal failure mechanisms. The individual analysis of runaway mechanisms allows determination of the relative contributions of electrical and thermal phenomena to failure, thus identifying the primary cause of runaway. This knowledge allows one to determine, depending on the operating conditions, whether the electrical or thermal device properties (or both) need to be improved to increase the Safe Operating Area (SOA).

The stability equations (Figs. 2-3) need to be combined with models of the different current contributions in an LDMOS (MOS current I_{dMOS}, bipolar base and collector currents I_b and I_c, and impact ionization current I_{ii}) and their temperature dependencies. For this purpose analytical models for LDMOS transistors, TCAD simulations, experimental data or combinations can be used [2], [3], [5], [7]–[10]. In this work, physics-based analytical expressions [11], [12] with experimental [6] fitting parameters have been used (Appendix).

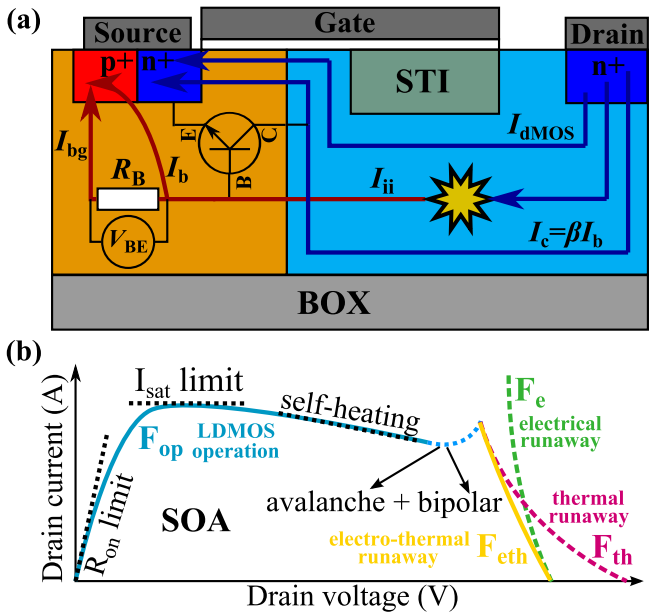

Fig. 1: a) Parasitic bipolar and avalanche multiplication in the operation of an LDMOS transistor. **b)** Schematic of the Safe Operating Area (SOA), showing the failure and operating functions which are analytically investigated in this work.

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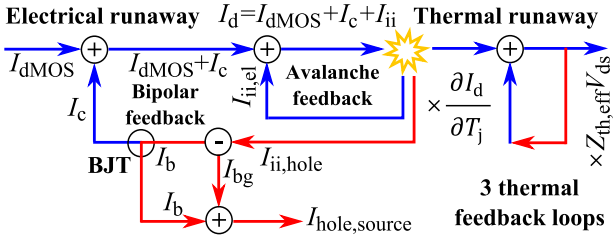

$$\begin{cases} I(V,T) \approx I(V_0,T_0) + g\,(V-V_0) + \phi\,(T-T_0) \\ T(V,I) \approx T(V_0,I_0) + Z_{th,eff} I_0\,(V-V_0) + Z_{th,eff} V_0\,(I-I_0) \end{cases}$$

$$\begin{cases} i = I - I_0 \\ v = V - V_0 \\ t = T - T_0 \end{cases} \quad \begin{cases} i = gv + \phi t \\ t = Z_{th,eff}\,(I_0 v + V_0 i) \end{cases} \quad \begin{cases} g = \left.\frac{\partial I}{\partial V}\right|_{T_0} \\ \phi = \left.\frac{\partial I}{\partial T}\right|_{V_0} \end{cases}$$

$$\begin{cases} i = Z_{th,eff}\phi V_0 i + \left(g + Z_{th,eff}\phi I_0\right) v & S_e = 1\ (g \to \infty,\ t = 0),\ \text{el. run.} \\ t = Z_{th,eff}\phi V_0 t + Z_{th,eff}\,(I_0 + gV_0)\,v & S_{th} = Z_{th,eff}\phi V_0 = 1\ (v = 0),\ \text{th. run.} \end{cases}$$

Fig. 2: Left. Schematic representation of the origin of electrical and thermal runaway. **Right.** Procedure for deriving the analytical stability equations by linearization around a bias point (V_0, I_0, T_0). Applying these equations to I_{dMOS}, I_c and I_{ii} and combining the results leads to the actual expressions for the stability factors and failure functions in Fig. 3.

II. Origin of Electro-Thermal Runaway

A. Feedback mechanisms

A general overview of the positive electrical and thermal feedback mechanisms leading to instability and runaway is provided in Fig. 1. At high drain voltages V_{ds}, the MOS electron current I_{dMOS} generates electron-hole pairs contributing to an impact ionization current I_{ii} with an electron and a hole component. The electrons flow towards the highly doped n^+ drain contact, the holes move towards the p^+ body contact inducing a voltage drop V_{BE} over the base resistance R_B. This switches on the internal parasitic bipolar with a base current I_b and a corresponding collector current $I_c \approx \beta I_b$, where β is the current gain. This current I_c is in turn multiplied by avalanche when flowing in the drift extension, resulting in a positive feedback behavior. Self-heating [5], [8], [13] is included in the model by introducing an effective thermal impedance $Z_{th,eff} \approx (T_j - T_{amb})/P_d$ [6], where it is assumed for simplicity that the dissipated power P_d is independent of pulse time t_{pulse}.

B. Electrical, thermal and electro-thermal failure

Electrical failure occurs because of the interaction of the parasitic bipolar with the current I_{ii}. Part of this current flows through the base of the bipolar and contributes to $I_c \approx \beta I_b$, which is avalanche multiplied and fed back into the base. Thermal failure can occur because of thermal runaway in each of the current components I_{dMOS}, I_c or I_{ii}. The temperature coefficient of I_{dMOS} depends on V_{gs} [14], I_{ii} has a slightly-negative temperature coefficient [15] (not included in the model), and I_c has a positive temperature coefficient [16]. In most cases, the increase in I_c (also including thermal leakage) induced by self-heating determines thermal instability [2], [3], [5], [8]. However, for V_{gs} below the zero-temperature coefficient point, I_{dMOS} also contributes to instability [5], [8], [14]. Although electrical and thermal failure mechanisms often both play a role in transistor failure, their relative contributions can be identified by introducing the analytical failure functions F_e and F_{th} (Fig. 1b)).

III. Analytical Stability Analysis

A. Stability factors and failure functions

In order to quantify the relative contributions of electrical [17] and thermal [5], [8] runaway to coupled electro-thermal [2], [9], [18] failure mechanisms, analytical stability equations are derived following the linearization procedure in Fig. 2. The electrical, thermal and electro-thermal stability factors

$$\begin{cases} I_{ii} = (M-1)\,(I_{dMOS} + I_c) & \textbf{(1a)} \\ I_{bg} = \frac{V_{BE}}{R_B} & \textbf{(1b)} \\ I_{ii} = I_{bg} + I_b \Rightarrow V_{BE} = c_1 + c_2 \cdot \exp\left(\frac{V_{BE}}{V_T}\right) & \textbf{(1c)} \\ c_1 = R_B (M-1) \cdot (I_{dMOS} + I_R) & \textbf{(1d)} \\ c_2 = R_B\,[\beta(M-1) - 1]\,\frac{I_S}{\beta} & \textbf{(1e)} \end{cases}$$

$$\begin{cases} I_{dn} = M \cdot \frac{(I_{dMOS}+I_c)}{W_{gate}} = f_e\left(V_{gs}, V_{ds}, V_{BE}, T_j\right) & \textbf{(2a)} \\ T_j = T_{amb} + Z_{th,eff}(t_{pulse}, A) W_{gate} V_{ds} I_{dn} & \textbf{(2b)} \end{cases}$$

$$\begin{cases} \phi_{dMOS} = \left.\frac{\partial I_{dMOS}}{\partial T_j}\right|_{V_{gs},V_{ds}} & \textbf{(3a)} \\ \phi_c = \left.\frac{\partial I_c}{\partial T_j}\right|_{V_{BE}} & \textbf{(3b)} \\ S_e = \beta(M-1) - \frac{r_b}{R_B},\ r_b = \left.\frac{\partial V_{BE}}{\partial I_b}\right|_{T_j} & \textbf{(3c)} \\ S_{th} = Z_{th,eff} V_{ds} \cdot (\phi_{dMOS} + \phi_c|_{V_{BE}=0}) & \textbf{(3d)} \\ S_{eth} = Z_{th,eff} V_{ds} \left[M \cdot \frac{1 + \frac{r_b}{R_B}\left(1 + \frac{\phi_c}{\phi_{dMOS}}\right)}{1 - S_e} \right] \phi_{dMOS} & \textbf{(3e)} \end{cases}$$

$$\begin{cases} F_x = S_x - 1\ (x = e, th, eth) & \textbf{(4a)} \\ F_{op} = \left\{ (I_{dn}, V_{ds}, T_j) \in \mathbb{R}^3 :\ \left[I_{dn} - f_e\left(V_{gs}^{max}, V_{BE} = 0\right) = 0 \right] \right\} & \textbf{(4b)} \\ V_x = \left\{ (I_{dn}, V_{ds}, T_j) \in \mathbb{R}^3 : F_x(I_{dn}, V_{ds}, T_j) < 0 \right\} & \textbf{(4c)} \\ V_{SOV} = V_{eth} \cap V_{op} & \textbf{(4d)} \end{cases}$$

Fig. 3: Physics-based model and analytical stability equations. The equations used for modeling the avalanche coefficient M, the MOS current I_{dMOS} and bipolar currents I_c and I_b are provided in the Appendix.

S_e, S_{th} and S_{eth} are evaluated in Fig. 3 together with the corresponding failure functions F_e, F_{th} and F_{eth} defined such that $F_x(I_{dn}, V_{ds}, T_j) = S_x - 1$. For safe operation, all failure functions need to obey $F_x < 0$, and failure occurs when $F_{eth} = 0$ in practice. In order to determine F_{eth}, the gate-width (W_{gate}) normalized drain current I_{dn} and the junction temperature T_j are found in each bias condition by solving the system (2a)-(2b) in Fig. 3. The base-emitter voltage V_{BE} has to be determined numerically from Eq. (1c) [7] in order to calculate I_c. The expressions used in this work for M, I_{dMOS}, I_c, I_b and their temperature dependencies are provided in the Appendix.

B. Determining the root of instability

Electrical failure is described by S_e in Eq. (3c) (Fig. 3), derived as in Fig. 2 assuming that self-heating does not occur (small-signal analysis with temperature variation $t = 0$). Avalanche and bipolar contributions (but not leakage) are excluded from thermal failure by assuming $M = 1$ and $V_{BE} = 0$ in the stability analysis. A small-signal voltage variation $v = 0$ in Fig. 2 leads to S_{th} in Eq. (3d). A complete stability analysis including all runaway mechanisms ($t \neq 0$ and $v \neq 0$) yields S_{eth} in Eq. (3e). In this expression it can be seen how electrical instability can trigger thermal runaway, since S_e appears as a feedback term in S_{eth} (electrically-induced thermal instability [2]).

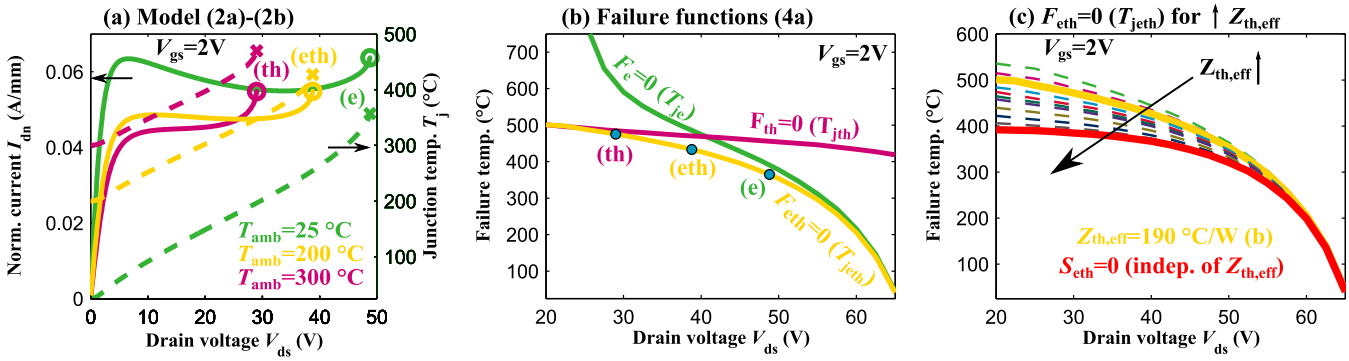

Fig. 4: a) Modeled I_{dn}-V_{ds} and T_j-V_{ds} curves for $V_{gs} = 2$ V and three different ambient temperatures T_{amb} until the edge of the SOA. **b)** Failure temperature ($T_{j,fail}$) vs. V_{ds} for $V_{gs} = 2$V showing the gradual boundary between thermal and electrical failure as V_{ds} increases and $T_{j,fail}$ reduces. **c)** Same as **b)** for different values of the effective thermal impedance $Z_{th,eff}$. The red line corresponds to a safer operating condition obtained for $S_{th} = 0$ rather than $S_{th} = 1$.

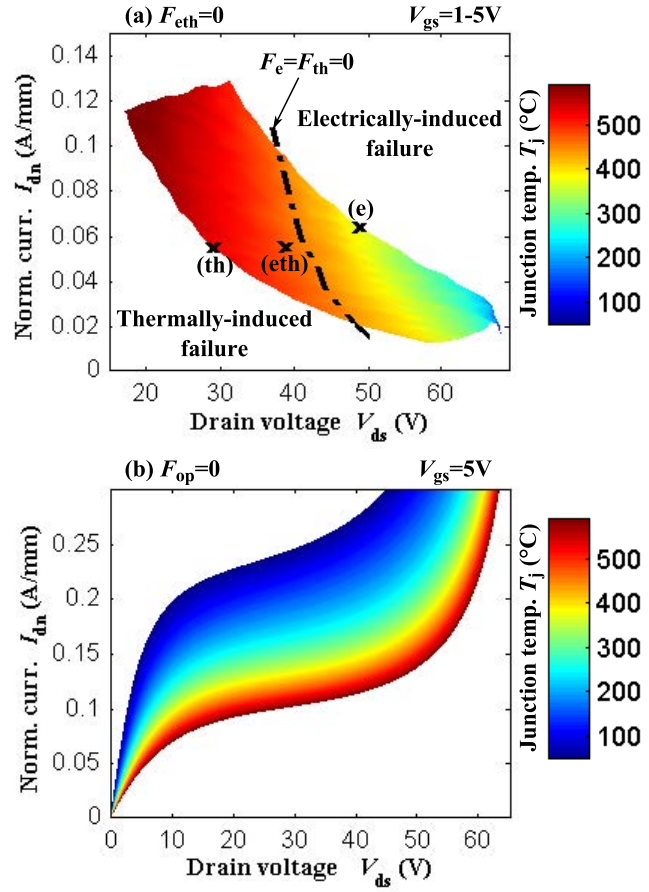

Fig. 5: a) Color plot of the surface $F_{eth} = 0$ for different V_{gs} values. The black line corresponds to the bias points where $F_e = F_{th} = 0$ and allows separation of the regions of electrically and thermally induced failure. **b)** The MOS operating function $F_{op} = 0$ for various junction temperatures defined for $V_{gs,max} = 5$ V and $V_{BE} = 0$ V.

IV. The Safe Operating Volume (SOV)

A. Building the failure function F_{eth}

Figure 4a) shows the modeled I_{dn}-V_{ds} and T_j-V_{ds} curves for $V_{gs} = 2$V at three different ambient temperatures T_{amb} (Eq. (2a)-(2b) in Fig. 3). The failure points at the edge of the SOA ($F_{eth} = 0$) where the model stops converging are investigated by analyzing the temperature (T_j) behavior of failure functions (Eq. (4a) in Fig. 3), as indicated by the circles in Fig. 4b). This analysis allows determination of the failure junction temperatures ($T_{j,fail}$) corresponding to electrical (T_{je}), electro-thermal (T_{jeth}) and thermal failure (T_{jth}). In all cases failure is limited by $F_{eth} = 0$ ($T_{j,fail} = T_{jeth}$), but there is a gradual boundary between thermal to electrical runaway as V_{ds} (and therefore the multiplication factor M) increases and T_j reduces.

B. Influence of the device area and operating conditions

In Fig. 4c), the dependence of $F_{eth} = S_{eth} - 1$ upon the effective thermal impedance $Z_{th,eff}$ is investigated. The failure temperature is affected by $Z_{th,eff}$ mainly for low V_{ds}, where failure is thermally induced, while tends to become independent of $Z_{th,eff}$ for large V_{ds}, where failure is electrically induced. However, if a safer operating failure criterion is used ($S_{eth} = 0$ rather than $S_{eth} = 1$, red line in Fig. 4c)), the failure temperature becomes independent of $Z_{th,eff}$ and therefore of ambient temperature, pulse time and device area. This is a significant result of this work, as discussed in Section V.

C. Mapping electro-thermal failure

In Fig. 5a), it is shown how electrical and thermal failure mechanisms are mapped on the failure function F_{eth}. The black dash-dotted line ($F_e = F_{th} = 0$) indicates the boundary between electrical and thermal failure regions, and the three crosses correspond to the failure points in Fig. 4a). In addition, the operating range is limited by the on-resistance and saturation current that are included using the operating function F_{op} in Eq. (4b) (Fig. 3). This is defined from Eq. (2a) for $V_{gs} = V_{gs,max}$, $V_{BE} = 0$ at different temperatures in absence of self-heating. In Fig. 5, the operating and failure functions F_{op} and F_{eth} are mapped onto a 3D space comprising gate-width normalized drain-current I_{dn}, drain voltage V_{ds} and junction temperature T_j. Intersecting the corresponding volumes V_{op} and V_{eth} (Eq. (4d) in Fig. 3) yields a new volume describing the operating limits of LDMOS transistors, which was defined as Safe Operating Volume (SOV) in earlier work [6]. For comparison with measurement results, the total SOV has been constructed using the model equations (2a)-(2b) (Fig. 3) and compared with the experimental data from [6] in Fig. 6.

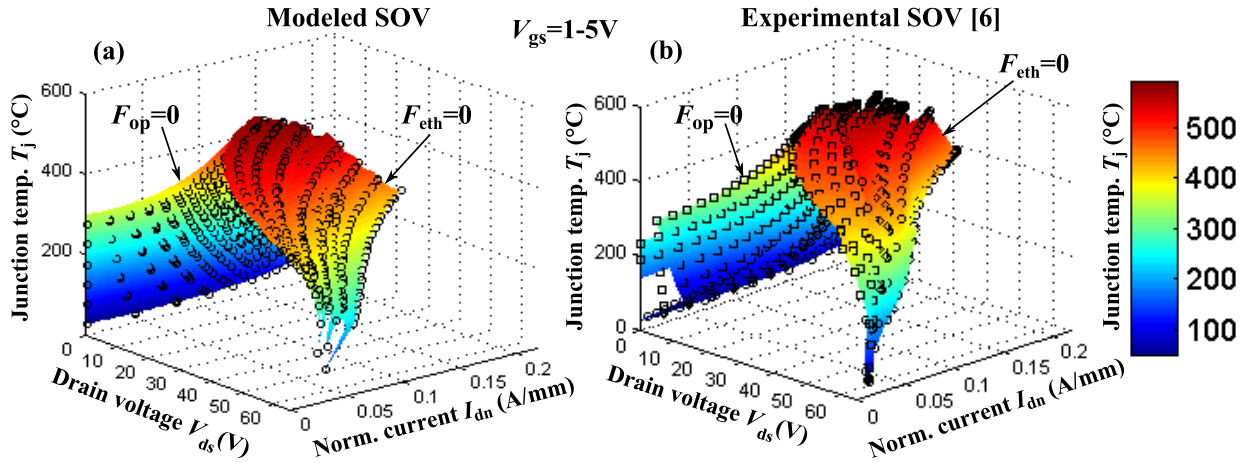

Fig. 6: Comparison between **a)** modeled and **b)** experimental [6] SOV, showing qualitative agreement across a wide range of bias conditions.

V. Discussion

The presented analysis is useful for the following reasons.

1) It allows identification of the main failure mechanism (electrical, thermal, electro-thermal) of LDMOS transistors on a theoretical basis, which is important for device optimization.
2) It shows that there is a gradual boundary between an electrical failure region at high drain voltage V_{ds} and a thermal failure region at high junction temperature T_j.
3) It explains why the SOV can be used as a general measure for the operating range of transistors, which is to a large extent independent of the size and operating conditions.
4) It suggests that the failure functions can be combined with the model results in Fig. 6a) to reduce the number of measurements needed to construct the experimental SOV in Fig. 6b).

While in theory the electro-thermal runaway condition is given by $S_{eth} = 1$ [1] ($F_{eth} = 0$), experiments [6] show that the range $0 < S_{eth} < 1$ is often unsafe due to the high value of $\frac{dS_{eth}}{dV_{ds}}$. Therefore, a safer operating condition can be introduced that is given by $S_{eth} = 0$, which leads to a reduction of the estimated safe operating limits (mainly in the thermal runaway regime) but makes the SOV independent of $Z_{th,eff}$ (Fig. 4c)). In practice, the condition $S_{eth} = 0$ cannot be achieved for V_{gs} values below the zero temperature coefficient point [14] since the temperature coefficient of the MOS current is positive in this range. For this reason, a practical value of $S_{eth} = 0.2$ was used in [6] for the different operating conditions, yielding a good trade-off between transistor safety and experimental accuracy.

VI. Conclusions

In this work, an analytical procedure for identifying electrical, thermal and electro-thermal failure in LDMOS transistors has been presented. The results allow the operating limits to be mapped on the Safe Operating Volume (SOV), which is defined as an extension of the Safe Operating Area (SOA). Suitable modifications of the stability analysis and SOV representation can extend their applicability to other kinds of transistors (see, e.g. [16]).

References

[1] P. L. Hower and P. K. Govil *in Trans. El. Dev.*, vol. 21, p. 617, 1974.
[2] P. Hower *et al., Proc. ISPSD'01*, p. 153, 2001.
[3] P. L. Hower *in Proc. ISPSD'02*, p. 1, 2002.
[4] V. Khemka *et al., Electron. Device Lett.*, vol. 25, p. 705, 2004.
[5] D. Dibra *et al., Trans. Electron. Dev.*, vol. 58, p. 3477, 2011.
[6] A. Ferrara *et al., IEDM'13*, p. 6.7.1, 2013.
[7] U. Radhakrishna *et al., Trans. Electron. Dev.*, vol. 58, p. 4035, 2011.
[8] M. Pfost *et al., Trans. Electron. Dev.*, vol. 60, p. 699, 2013.
[9] Y. S. Chung and B. Baird *in Microel. Reliab.*, vol. 42, p. 211, 2002.
[10] S. J. Sque *et al., Proc. IEDM'13*, p. 12.7.1, 2013.
[11] D. B. M. Klaassen *in Solid-State Electron.*, vol. 35, p. 953, 1992.
[12] N. Arora, *Mosfet Modeling for VLSI Simulation: Theory And Practice.* World Scientific, 2007.
[13] A. Ferrara *et al., Proc. ICMTS'13*, p. 115, 2013.
[14] G. Breglio *et al., Proc. ISPSD'99*, p. 233, 1999.
[15] S. Reggiani *et al., Trans. Electron. Dev.*, vol. 52, p. 2290, 2005.
[16] T. Vanhoucke and G. A. M. Hurkx *in Proc. BCTM'05*, p. 37, 2005.
[17] S. Reggiani *et al., Trans. Electron. Dev.*, vol. 56, p. 2811, 2009.
[18] P. Moens and G. Van den Bosch *in Trans. Device Mat. Rel.*, vol. 6, p. 349, 2006.

Appendix

Avalanche, MOS and bipolar model equations used in this work:

$$\begin{cases} M = \frac{1}{1-\left(\frac{V_{ds}}{BV}\right)^m} & \textbf{(A1)} \end{cases}$$

$$\begin{cases} K(T_j) = K(T_{ref})\left(\frac{T_j}{T_{ref}}\right)^{-m_{ch}} & \textbf{(M1)} \\ V_{th}(T_j) = V_{th}(T_{ref}) - k_{th}\left(T_j - T_{ref}\right) & \textbf{(M2)} \\ R_{on}(T_j) = R_{on}(T_{ref}) \cdot \left(\frac{T_j}{T_{ref}}\right)^{m_{drift}} & \textbf{(M3)} \\ I_{dsat}(T_j) = I_{dsat}(T_{ref}) \cdot \exp\left(-\frac{T_j - T_{ref}}{\theta}\right) & \textbf{(M4)} \\ V_{dsat}(T_j) = R_{on}(T_j) \cdot I_{dsat}(T_j) & \textbf{(M5)} \\ I_{ch} = \frac{K\cdot(V_{gs}-V_{th})^{\alpha_{ch}}}{1+\theta_{V_{gs}}(V_{gs}-V_{th})} \cdot \frac{1}{\left[1+\left(\frac{V_{ch}}{V_{gs}-V_{th}}\right)^{\eta_{ch}}\right]^{1/\eta_{ch}}} & \textbf{(M6)} \\ I_{drift} = I_{dsat} \cdot \frac{(V_{ds}-V_{ch})}{V_{dsat}} \cdot \frac{1+g_{ac}(V_{ds}-V_{ch})}{\left[1+\left(\frac{V_{ds}-V_{ch}}{V_{dsat}}\right)^{\eta_{drift}}\right]^{1/\eta_{drift}}} & \textbf{(M7)} \\ I_{dMOS}(V_{ds}) = I_{ch}(V_{ch}) = I_{drift}(V_{ds} - V_{ch}) & \textbf{(M8)} \end{cases}$$

$$\begin{cases} I_s(T_j) = I_s(T_{ref}) \cdot \exp\left[-\frac{qE_g}{k_B}\left(\frac{1}{T_j} - \frac{1}{T_{ref}}\right)\right] & \textbf{(B1)} \\ I_R(T_j) = I_R(T_{ref}) \cdot \exp\left[-\frac{qE_g}{2k_B}\left(\frac{1}{T_j} - \frac{1}{T_{ref}}\right)\right] & \textbf{(B2)} \\ R_B(T_j) = R_B(T_{ref}) \cdot \left(\frac{T_j}{T_{ref}}\right)^{m_{npn}} & \textbf{(B3)} \\ \beta(T_j) = \beta(T_{ref})\left(\frac{T_j}{T_{ref}}\right)^{m_\beta} & \textbf{(B4)} \\ I_b(V_{BE}, T_j) = \frac{I_S}{\beta}(T_j) \cdot \exp\left(\frac{V_{BE}}{V_T}\right) & \textbf{(B5)} \\ I_c(V_{BE}, T_j) = I_S(T_j) \cdot \exp\left(\frac{V_{BE}}{V_T}\right) + I_R(T_j) & \textbf{(B6)} \end{cases}$$