SoC Mixed-Signal Dependability Enhancement: A Strategy from Design to End-of-Life

Muhammad A. Khan, and Hans G. Kerkhoff

Testable Design and Test of Integrated Systems (TDT) Group,
University of Twente, Centre of Telematics and Information Technology (CTIT),
Enschede, the Netherlands
m.a.khan / h.g.kerkhoff@utwente.nl

Abstract— **The ever shrinking technology dimensions have increased the degradation levels in integrated mixed-signal circuits mainly because of issues that were not considered in older technologies. These issues have posed new challenges and require a complete strategy starting from the design phase of the product to the end-of-life. This paper presents such a strategy starting with an early selection of dependable blocks at IP level and combines this with an efficient hardware platform architecture to address lifetime dependability issues especially for mixed-signal frontends. The proposed approach links the circuit/IP level dependability with the block level dependability enhancement and finally with the system level dependability enhancement strategy. The approach is supported by extensive simulations and provides confidence in using the proposed strategy.**

Keywords- mixed-signal dependability; dependable IPs; self-diagnosis; hardware redundancy; design space exploration for dependable system; dependability recovery scheme; dependability characterization

I. INTRODUCTION

Different degradation mechanisms like Negative Bias Temperature Instability (NBTI), Positive Bias Temperature Instability (PBTI), Hot Carrier Injection (HCI), and Time Dependent Dielectric Breakdown (TDDB) have become very important while moving designs into nanoscale technology levels. Generally these degradation mechanisms have been studied for digital circuits but it has been reported [1-3] that they also play an important role in analog and mixed-signal circuit performance degradation. Although the introduction of surface-channel pMOSFETs for analog circuits has provided the way to fabricate both analog and digital circuits on the same chip, NBTI degradation in pMOS is a significant concern for these analog circuits. Many analog operations require matched parameters and therefore any mismatch introduced by these degradation mechanisms can result in analog circuit failures.

In order to estimate the effect of these degradation mechanisms (NBTI, HCI etc.) in analog and mixed-signal circuits, reliability simulations are commonly used as the first tool. These simulations are usually carried out in two phases. In the first phase, fresh circuit simulations are carried out using fresh and original device models. Based on these simulations, circuit activities and their impact on circuit lifetime are evaluated. These are further used to generate degraded device models. In the second phase of simulation fresh and original device models are replaced with these degraded models to evaluate circuit performance after a certain amount of operational time [1, 4]. This shows that the accuracy of reliability simulations is very much dependent on the accuracy of degraded models generated based on circuit activities and their impact on lifetime of the circuit. The results of these simulations then can be used to reconsider the designed circuit for better reliability or lifetime performance.

Another technique based upon reusable IPs has been proposed in [5]. In this technique different analog and mixed-signal IPs, which are already designed to be reliable under different applications and lifetime conditions, are stored in an IP library. The designer makes use of this information to choose the best combination of components to meet the dependability requirements of the designed circuit/system.

Most efforts have been made in manipulating circuits at the design stage to tackle dependability, especially reliability, issues. Like in the case of reliability simulations, degraded models are extracted and simulated for lifetime behavior of analog and mixed-signal circuits. This information is then further used to redesign or incorporating circuit strategies for reliability or dependability improvements. It will result in a number of IPs having the same functionality, but belonging to different reliability or dependability levels. This can be further used to select the best combination of IPs for desired reliability or dependability levels of the designed system. Both these techniques are used at design levels but they lack in dealing with lifetime dependability issues related to complete IP failures, and system availability and maintainability issues. These issues require further considerations that will deal with lifetime dependability issues. To address these issues, we propose an improved hardware platform for dependability enhancement [6] and combine this platform with an early selection of IPs for best possible combination to get a better solution in terms of dependability.

This paper has been divided into seven sections. Section II briefly summarizes important attributes of dependability. Section III gives information about some important dependability, or reliability issues in different IPs used in analog and mixed-signal front-ends. The proposed strategy and hardware platform will be discussed in section IV and V while simulation results and conclusions are presented in sections VI and VII respectively.

II. Dependability and its Attributes

Dependability is often partially considered and reliability, being only one attribute of dependability, has been mostly discussed for analog and digital circuits. Dependability being a set of a number of attributes, like reliability, maintainability, availability, safety, security and survivability [7-9], gives a measure of trustworthiness that in a given environment the system will operate as expected and will not fail during its normal operation [10].

The focus of this paper is mainly on some important attributes of dependability, more precisely reliability, maintainability, and availability. These attributes are probabilistic quantities and can be defined in terms of probabilities. For example reliability is defined as the percentage probability as a function of time that the system will be correctly functioning at that time. Maintainability can be defined as the percentage probability as a function of time that the system will be repaired if it fails at that time and availability as the percentage probability as a function of time that the system will be available for correct service at that time [6]. These attributes can be further related to probabilistic quantities like "Mean Time To Failure" (MTTF), "Mean Time To Repair" (MTTR) and "Mean Down Time" (MDT) [5, 9, 10].

III. Dependability of Analog and Mixed-Signal Front-ends

A conventional analog and mixed-signal front-end can be considered as composed of a sensor, amplifier/filter and an analog-to-digital converter. For simplicity, a temperature sensor can be considered to serve the purpose of a general sensor followed by an operational amplifier (OpAmp) and an ADC as shown in Fig. 1. The output of the temperature sensor is amplified by an operational amplifier and then converted into a digital value by an ADC for further processing in the digital domain.

The dependability of such a system (front-end) can be highly effected by different degradation mechanisms as they play an important role in degrading the performance of an operational amplifier (OpAmp) [1-3] and analog-to-digital converters (ADC) [1, 11]. It has been reported in [3] that the gain of an operational amplifier degrades exponentially as a function of time if both HCI and NBTI effects are expected. Furthermore, if mismatch is considered then the gain is highly effected and degrades super-exponentially as time goes. This will result in an earlier failure in an operational amplifier as compared to its normal use under normal conditions. It has also been shown in [11] that any error in the gain of an operational amplifier in pipelined A/D converters is highly sensitive to is performance and will cause nonlinearity in the overall A/D conversion.

With designs moving towards smaller dimensions, electric fields in the channels are becoming larger, causing more energetic electrons to damage channel-oxide and hence degrading circuit performance. The introduction of surface-channel pMOSFETs for analog circuits, on one side, has made it possible to fabricate both digital and analog circuits on the same chip, while on the other hand, has increased the effects due to NBTI and HCI [2] .

In case of analog circuits, dc biasing voltages always exist irrespective of the input signal. Because of the high-density of digital circuitry, a high temperature may also exist in addition to the applied dc gate and drain voltages. This would result in a continuous stress in analog circuits as compared to digital circuits where a continuous dc stress is seldom seen. As many analog circuit operations require matched parameters therefore any mismatches introduced by these continuous stresses will cause circuit failures [2] and will impose a fundamental limit to the analog and mixed-signal circuit dependability.

IV. Proposed Strategy

As technology is scaling, the area and power consumption of analog circuits is not scaling with the same pace as their digital counterparts. Furthermore, digital circuits are cheap and flexible in terms of performance improvements. This has introduced the new concept of digitally assisted analog and mixed-signal circuits. In these digitally assisted analog and mixed-signal circuits, digital signals are used to realize, control, improve, and change the circuit functionalities in the analog domain [12]. These digitally assisted analog and mixed-signal circuits can be found in many applications including amplifiers [13], ADCs [13-15], RF transceivers [16] and sigma-delta modulators [17]. They also provide the opportunity to estimate analog performance based on digital domain data.

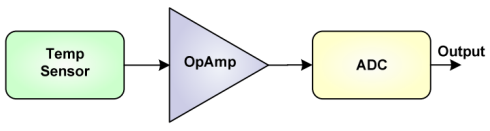

Figure 1. Block diagram of a conventional analog and mixed-signal front-end

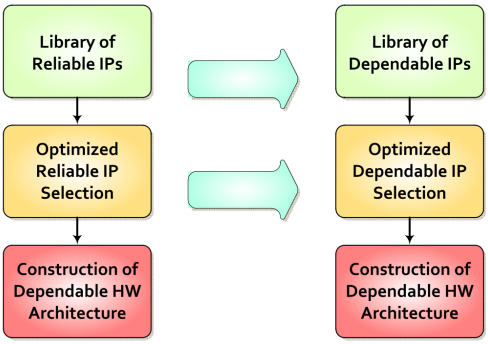

Figure 2. The conceptual flow of the proposed strategy

A recent paper [12] has introduced an on-chip measurement architecture based on the IEEE 1500 standard to test these digitally assisted analog circuits. The designed architecture is scalable and capable of performing concurrent on-chip measurements. The author claims that moderate measurements can be achieved by using this architecture, while further accuracy can be achieved by post processing to reduce measurement errors. The suggested strategy is based upon the same concept of digitally assisted analog and mixed-signal circuits where some on-chip measurement architecture has been proposed to calibrate the performance of each analog and mixed-signal IP. While dependability issues have been resolved at the design stage by selecting suitable IPs for better dependability performance, and for the lifetime of the product some built-in tuning/trimming and switching techniques have been added.

Fig. 2 shows the conceptual flow of the proposed strategy. It starts with a library of reliable IPs which is used to select the best combination of IPs to optimize the reliability issues followed by the construction of the dependable hardware platform. The library of reliable IPs is a collection of different IPs having the same functionalities but different reliability levels, speed, area and power overheads. These libraries of reliable IPs can be constructed by using reliability simulations on designed circuits and studying reliability-critical substructures or devices. These substructures or devices can then be redesigned or new structures can be inserted to achieve different levels of reliability along with their price in terms of speed, area, and power overhead.

The reliability simulation flow usually consists of two phases. In the first phase the given circuit is simulated using models according to the technology information. Based on these simulations different stress profiles (e.g power) are extracted which are further used in combination with different failure models, built from experimental testing work and structural circuit information, to select reliability critical substructures or devices. In the second phase equivalent circuits are generated and incorporated into the original circuit. These are then simulated for degraded or lifetime behaviors. Based on these simulation results, reliability improvement suggestions can be made [1]. These suggestions can lead towards different circuits that could have different reliability levels based on a compromise between area, speed, power etc. In this way one can generate multiple copies of the same functional circuit with different reliability levels along with their speed, area, and/or power overheads.

Once a library of different reliability-level IPs is obtained, the next step is to select the best IP(s) that can give us a better compromise between reliability, speed, area, power etc. as required by the application or customer. This can be achieved by Linear Programming (LP) techniques like the Simplex algorithm. For example, an analog and mixed signal front-end which has only two IPs being an operational amplifier and analog-to-digital converter. If each of these IPs has four different flavors in the IP library in terms of different reliability levels, speed, area and power consumption then there will be sixteen different combinations in which these IPs can be connected (OpAmp followed by an ADC). The reliability of these two IPs connected in series can be calculated using Reliability Block Diagrams (RBD) whereas the speed, area and power requirements can be simply added. By having this information one can determine which combination is the best option from either reliability point of view or area point of view etc. In this way one can select the best option for combining IPs to meet the requirements set by the application or customer.

In order to optimize the dependability of the selected IPs at this stage, the designer has to incorporate other attributes of dependability at this stage. Since here only reliability has been considered therefore other important attributes like availability, maintainability, and safety should be incorporated in optimal selection of IPs to get better levels of dependability. In case of a repairable system, the availability of the system can be related to its Mean Time Before Failure (MTBF) and Mean Down Time (MDT) due to repair as shown in the following equation [5]:

$$Availability = A_v = \frac{MTBF}{MTBF + MDT} \qquad (1)$$

Where maintainability essentially means the probability as a function of time that the system will be repaired if it fails at that time [6]. In case of repairable systems, the availability of the system is highly dependent on the maintainability, or in other words the time an IP is available for correct service is highly dependent on how much time it takes to repair this IP in case of any failure. The longer the maintaining or repair time of an IP, the lesser will be the availability of that IP. Safety on the other hand, being the absence of catastrophic consequences on the user(s) and the environment [7], can be related to its Safety Integrity Level (SIL) [5]. This, indeed, is related to the functional importance of an IP in the designed system. For example an OpAmp in a car radio will require a basic SIL value while if used in a car tire pressure sensor will require a higher SIL value.

Many manufactures of analog and mixed-signal chips provide information about reliability in terms of FIT (Failure In Time) which can then be converted into MTBF by using (2) [5]. Similarly, the maintainability of an IP can be related to MDT and will be a function of the time required to detect a failure, diagnose the problem and to take proper actions to correct this problem. This will be further dependent on the complexity of the circuit and the degree/accuracy to which this problem has to be resolved. High complexity of the circuit (IP) and high tuning/trimming accuracy will require more time to diagnose and repair the problem. Therefore, the MDT of an IP can be calculated based upon the fault detection time, communication time with the diagnosing circuit, and the time required to properly diagnose and repair the problem. Normally these parameters (MTBF and MDT) can be measured in two different ways. One way is to determine these parameters at simulation level, where by observing performance parameters and their deviation from normal values (failure) as a result of degradation process or other faults will give us an estimate of MTBF. Similarly, by having a repairing mechanism, simulations can be run to estimate the time required to detect, diagnose and repair the fault and hence resulting in MDT. Other way of obtaining these parameters (MTBF, MDT), which may require more efforts in terms of time and cost, is conducting real test measurements under different stress conditions and measure the real MTBF and MDT values with much higher accuracy as compared to simulations. Furthermore, by having these values of MTBF and MDT the availability of an IP can be calculated using (1). Whereas safety of an IP can be indicated in terms of the Safety Integrity Level (SIL) and can be correlated with the reliability, availability, and complexity of that IP. This will also be a function of exposure, the environment where the IP is being used, the level of controllability and severity [5] and hence requires detailed information on the actual application.

$$MTBF = \frac{10^9}{FIT * 8760} \qquad (2)$$

Based on this information, each IP can be labeled with its reliability, availability, maintainability, SIL [5], area, speed, and power requirements. This can be further used to build a library of dependable IPs instead of a library of only reliable IPs and optimization can be done to select the best IPs for better dependability levels along with their speed, area and power requirements as shown in Fig. 2. As described above, availability in case of repairable system is highly dependent on maintainability of the system. Therefore, in order to achieve higher availability, one has to reduce the maintenance or repair time. In some cases, especially for analog and mixed-signal circuits, it can be quite hard. This is because of the fact that they require a longer time to calibrate the performance and diagnose the problem in case of any failure in performance. Furthermore this early selection of dependable IPs for achieving better dependability levels lacks the scenario when any of the selected IP completely fails, resulting in complete system failure. These problems of achieving higher availability and avoiding complete system failures require in addition a new hardware architecture. Such a hardware platform is shown in Fig. 3.

V. PROPOSED HARDWARE PLATFORM

The proposed hardware platform (Fig. 3) resembles a duplicate system in which two redundant hardware blocks are connected by means of two switches SW_1 and SW_2 to provide two active paths. The upper active path in which upper two IPs

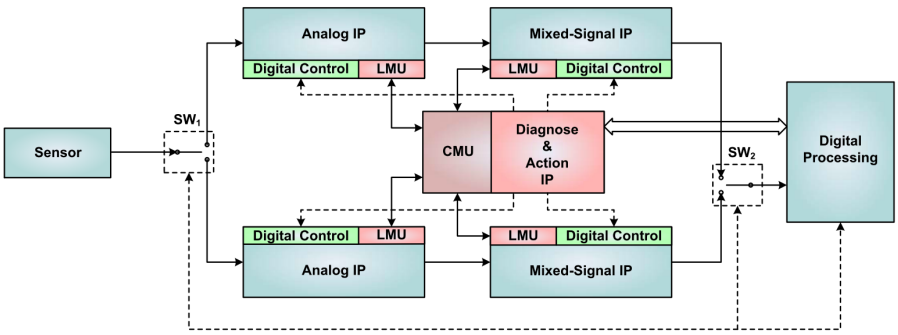

Figure 3. Proposed hardware platform for achieving higher dependability levels for analog and mixed-signal front-ends at system-level

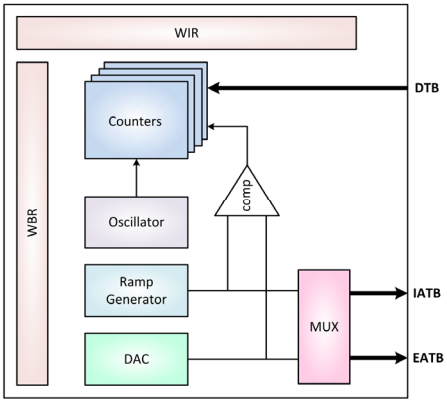

Figure 4. The Central Measurement Unit (CMU) [12]

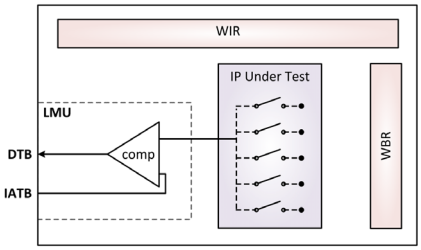

Figure 5. The Local Measurement Unit (LMU) [12]

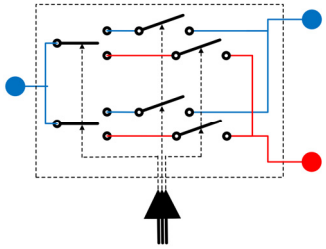

Figure 6. A possible fault tolerant architecture for switches $SW_{1\&2}$ (Fig. 3)

are active and the lower active path in which the lower two IPs are active. The switches SW_1 and SW_2, which are used to change one active path with the other active path at predefined regular intervals of time, are controlled by the central "Digital Processing" IP. The "Diagnose and Action" IP is responsible to calibrate the performance and diagnose the problem of each IP using an on-chip measurement architecture. These on-chip measurement units, the Local Measurement Unit (LMU) and Central Measurement Unit (CMU), are described in [12].

Figs. 4 and 5 show the details of the CMU and LMU respectively as described in [12]. Depending on the measurement needs, each IP may have one or multiple LMUs. The width of the digital data bus (DTB) depends on the number of LMUs whereas a single-wire internal and a single-wire external analog test bus (IATB and EATB) is required. The Wrapper Boundary Register (WBR) and Wrapper Instruction Register (WIR) can be controlled by the "Diagnose and Action" IP. The WBRs are used to capture measurement data.

As described in [12] the CMU consists of a DAC, a ramp generator, high-frequency oscillator, and a number of ripple counters. The high-frequency oscillator is used to run ripple counters which can be stopped by the signals on the DTB. The main part of the LMU is a comparator whose inputs are connected to the IATB and IP internal test points via analog switches. Whereas the output of the LMU comparator controls the counter in the CMU via the DTB. The basic responsibility of the CMU is analog-to-digital conversion using the built-in ramp generator and counters, assisted by the LMU. The purpose of using a comparator in an LMU is twofold: it compares the analog signal at the test point with the ramp voltage and isolates the test point from parasitics in the test buses [12]. Using this measurement architecture one can measure the voltages at different test points within the analog circuit. In order to measure DC currents, an additional I/V converter needs to be placed between the test point and the input of the comparator in the LMU. The purpose of these measurements is to estimate the performance of the analog and mixed-signal circuit/IP which can then be analyzed by the "Diagnose and Action" IP to take further actions.

Let initially all of the analog and mixed-signal IPs be fully dependable and the upper active path is being used for normal operation. At predefined regular intervals of time this active path (upper active path) will be changed with the lower active path by using switches SW_1 and SW_2. At this time the IPs in the upper active path will be calibrated and diagnosed by the "Diagnose and Action" IP using on-chip measurement units (LMU and CMU). In case there will be any mismatch between the measured values and the expected values proper tuning actions will be carried out by the "Diagnose and Action" IP using digital tuning knobs as shown in Fig. 3. At the next regular interval of time the upper active path will be switched back by using switches SW_1 and SW_2 to be used for normal operation. While IPs in the lower active path will be calibrated and diagnosed by the "Diagnose and Action" IP and if required, proper tuning actions will be taken by using digital tuning knobs. The calibration and repairing process of each path will take place in such a way that their performance will be within a predefined tolerance band to reduce sensitivity at the output while switching one active path with the other active path by means of switches SW_1 and SW_2.

The position of the switches, SW_1 and SW_2, in the proposed hardware architecture is very critical and any failure in these switches will result in a complete failure of the whole system. Therefore, these switches (SW_1 and SW_2) are made highly fault tolerant. A possible architecture could be a switch having parallel and serial duplication, as shown in Fig. 6, where these switches are connected in parallel and in series for obtaining better dependability levels. The use of these fault tolerant switches will enhance the availability of the whole system and will provide a better way to diagnose the faults, if any, in the analog and mixed-signal IPs. In this way a longer time will be available for thoroughly evaluating the performance of each IP and if required, taking proper actions using on-chip digital tuning capabilities. On one hand, the overall availability of the whole system to provide the desired functionality has been increased, while on the other hand the time required to properly

diagnose the fault and take further actions of compensation has been also increased. These improvements will play an important role in enhancing lifetime dependability levels of these analog and mixed-signal front-ends, which are discussed in the next section.

I. DEPENDABILITY IN CASE OF PROPOSED STRATEGY

The dependability of the proposed strategy can be analyzed at two levels: 1) at the IP selection level and 2) at the proposed hardware platform level. Fig. 7 shows some calculations based on Linear Programming (LP) for optimizing dependability at IP selection stage. Here two IPs, OpAmp and ADC, have been considered in an analog and mixed-signal front-end with four different flavors for each IP having different dependability attributes along with their area, power and speed values. In Fig. 7 the Rel and Avl parameters are used to represent reliability and availability attributes, Mean Down Time (MDT) to represent the repair or maintainability attribute, Safety Integrity Level (SIL) is used to represent the safety attribute of the overall dependability of each of the sixteen possible combinations (OpAmp followed by an ADC) for analog and mixed-signal front-end. A possible set of OpAmp and ADC can be selected by using calculations presented in Fig. 7, depending on the requirements set by the application or user. For example, case 8 can satisfy dependability requirements with Rel > 85 %, Avl > 95%, MDT < 500 ms, SIL ≥ 3, area overhead < 1500 μm^2, speed < 40 ns and the power overhead less than 2.5 mW. Further dependability enhancements can be achieved by using the proposed hardware platform.

In order to calculate the dependability enhancements due to the proposed hardware platform, first, the reliability enhancement has been calculated using the Markov analysis and Reliability Block Diagrams (RBDs). While using Markov analysis, each repairable analog and mixed-signal IP can be divided into a number of states represented by circles (bubbles) to formulate a state model. These circles are then connected by directional arcs representing the transition rates (in our case failure and repair rates; failure per hour and repair per hour) at which the system moves from one state to another state. Solution of this state model using state-space approach will give the probabilities that the system will be in different states at a particular time. Subsequently, the sum of the probabilities over non-failure states will provide the reliability of the system at that time. By having these reliabilities for each IP, the overall reliability of the system can be calculated using Reliability Block Diagrams. Further details of this technique for the proposed hardware platform can be found in [6]. Fig. 8 shows the results of MATLAB reliability simulations for the proposed hardware platform. It is clear from these simulations that the reliability of a system using the proposed hardware platform with repairable components (WRC) has been increased as compared to a system using the same hardware platform but with no repairable components. This increase in reliability can be further increased if the switching time from one active path to other active path is decreased and the repair time for the non-active path is reduced. The reduction in repair time for the non-active path will make it possible to reduce system failure possibilities in the active path. That is failure in the performance of the active path while diagnosing the performance of the non-active path. This effect can be minimized by carefully selecting the interval time from one active path to the other active path relative to the system degradation profile.

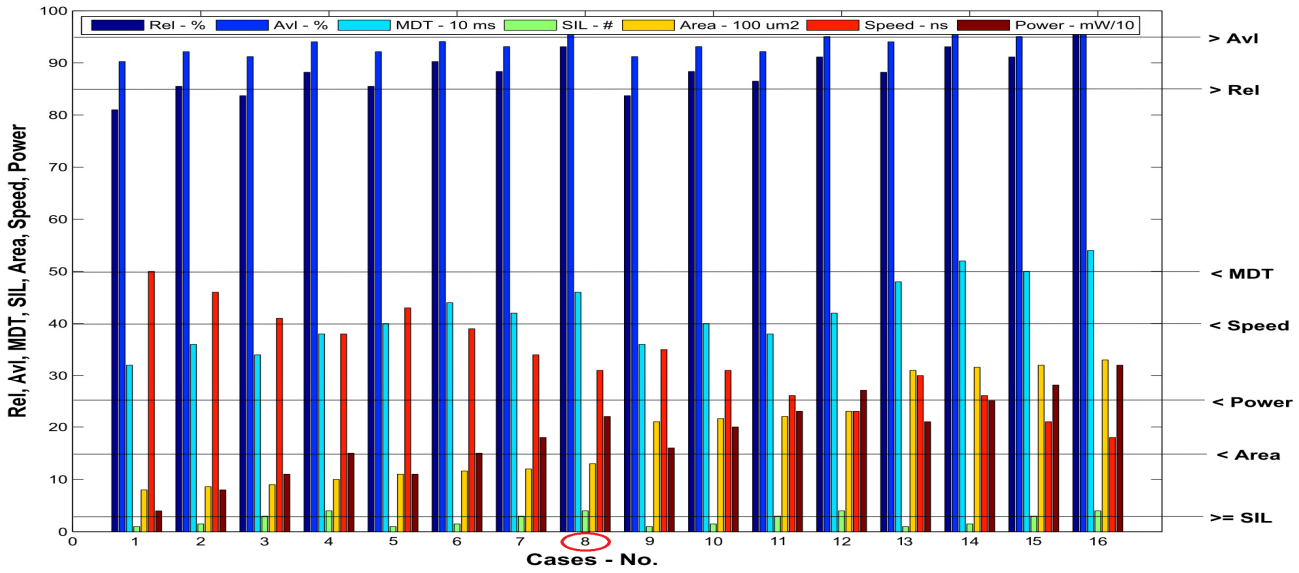

Figure 7. Some calculations on the optimization of dependability attributes along with area, power and speed parameters

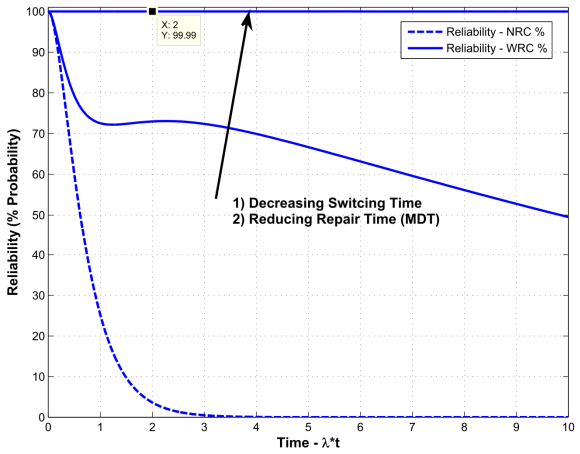

Figure 8. : Reliability for the proposed hardware platform (* NRC=No Repairable Components, WRC=With Repairable Components, λ=1/1000)

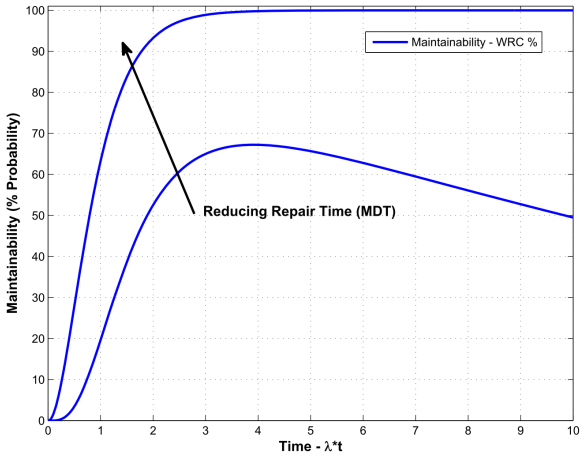

Figure 9. Maintainability of the proposed hardware platform (λ=1/1000)

The availability of the system, being the probability as a function of time that the system will be available for correct service at that time, is directly related to the switching time and has been increased up to 100 % for slow or low frequency applications. For example, in case of a temperature sensor where temperature values after every 100 ms are sufficient for a particular application, a switching time of 10 ns will make the availability of the system close to 100 %. The maintainability, being the probability that the system is successfully repaired while it fails, can be calculated by measuring the contribution of the repair mechanism (i.e. the introduction of repairable components and the central Diagnose and Action IP) to decrease the unreliability (1-reliability) or to increase the reliability of the system having no repairable components (i.e. no repair mechanism). This is directly related to the tuning capabilities for each IP. The larger the number of possibilities to digitally tune the performance of an IP, the higher will be the probability for the "Diagnose and Action" IP to tune an analog or mixed-signal IP in case of any performance failure. This is further related to repair time or MDT and will be increased by reducing repair time or MDT as shown in Fig. 9.

II. CONCLUSION

Different degradation mechanisms for dependability of the integrated circuits due to NBTI, HCI and TDDB have become quite apparent in recent submicron technologies and this require strategies starting from circuit design phase to end-of-life of a product. This paper presented a dependability enhancement strategy that combines the efforts at circuit/IP level to block level up to system level. Initial reliability simulations at circuit/IP level can be utilized to establish libraries of reliable IPs and can be further extended to develop libraries of dependable IPs by utilizing digitally assisted and digital repairing techniques for mixed-signal SoCs. Simple optimization techniques based on Linear Programming (LP) can further lead to choose the best possible combination of IPs from these libraries of dependable IPs for better dependability levels. These decisions can be further combined with a hardware platform having on-chip measurement and digital tuning capabilities with some switching techniques for enhancing lifetime dependability levels. The proposed strategy was investigated using extensive simulations and the results presented provides a confidence in its usage.

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