On the degradation of field-plate assisted RESURF power devices

B.K. Boksteen, S. Dhar[x], A. Ferrara, A. Heringa*, R.J.E. Hueting, G.E.J. Koops*, C. Salm, J. Schmitz

MESA+ Institute for Nanotechnology, University of Twente, 7500AE, Enschede, The Netherlands
Phone: +31 53 489 2645, Fax: +31 53 489 1034, Email: b.k.boksteen@utwente.nl
Central R&D, NXP Semiconductors, [x] Eindhoven, The Netherlands; *Leuven, Belgium

Abstract

Hot-carrier degradation phenomena in field-plate assisted reduced surface field (RESURF) devices caused by high voltage off- and on-state stressing have been investigated. The device *I-V* characteristics are analyzed and modeled in detail. It is shown that via noninvasive low-voltage leakage characterization the surface generation velocity profiles after (high-voltage) stress can be extracted, enabling *I-V* degradation predictions across wide temperature ranges.

Introduction

Field-plate (FP) assisted RESURF power devices in silicon-on-insulator (SOI) (1) (Fig. 1) provide a cost-effective solution for power and high-voltage switching. Typically, these devices contain a linearly graded doped drift region for improving the tradeoff between the on-resistance (R_{on}) and breakdown voltage (*BV*). They are applied in several markets ranging from power conversion IC's (adapters) to lighting solutions such as CFL light control IC's and the fast growing market of LED drivers (2). As LEDs for instance have intrinsic lifetimes in the 20-30 years range, reliability demands for the high voltage transistors incorporated in the drivers are stringent. In particular the off-state reliability is a key concern given the low duty cycle in certain LED mission profiles. A sound reliability prediction of these devices requires knowledge of the degradation phenomena and their acceleration factors. Ideally, the *I-V* characteristics of a device can be predicted after any realistic stress sequence (3,4). Recent studies (5,6) have dealt with hot-carrier (HC) stress modeling in extended drain MOS (EDMOS) and STI-extension EDMOS. However, to date, a complete and accurate description of the degradation of linearly graded drain extension based RESURF devices is still missing.

In this paper we show that 1) degradation in these devices is HC dominated; 2) the off-state HC damage concentrates strongly at the drain side of the drift region but manifests itself in both the low-voltage and high-voltage (avalanche) drain bias regimes; 3) the *I-V* characteristics after degradation can be quantitatively reproduced with a new analytical device model based on well-established theory; and 4) with this model degradation predictions at different temperatures can be made through non-invasive low-voltage scanning at a single temperature.

Leakage current model

Since a leakage current model for linearly graded drain extension RESURF devices did not yet exist a new analytical model is first presented. This model will subsequently form the basis for understanding (and modeling) changes seen in device *I-V* characteristics after stress.

The field distribution plays an integral part in understanding leakage behavior in high-voltage devices. Fig. 2 shows schematic cross-sections and simulated (7) field distributions at reverse bias of pn-junctions mimicking various drift region constructs (1,8). The ideal FP assisted RESURF drain extension (9) with doping slope *a* (Fig. 2c) has an optimal surface field distribution which (uniquely) expands laterally with V_{DS} (10). This distinct field expansion enables field distribution extraction (10,11) and helps to separate, understand and model the different degradation phenomena and their influence on the complete device (leakage) *I-V* behavior. The leakage current and impact ionization (II) reverse bias dependencies of these devices (Fig. 3) allow for a modular look at the leakage *I-V* as described by the model proposed in Fig. 4 (Eq. 1, thermal generation, I_{Gen}^{Tot} ; Eq. 2, the multiplication factor, *M*).

With the proposed model a methodology has been developed which separately takes into account thermal generation in the bulk SOI layer (I_{Gen}^{S}) and at the (degraded) Si/SiO_2 interfaces (I_{Gen}^{I}). The depletion profile shown in Fig. 5 graphically represents how this separation is made and why it can contribute to separate scanning of different degradation phenomena.

Fig. 6 shows the II-behavior in the subthreshold region ($0<V_{gs}<V_{th}$) and in off-state respectively. In subthreshold the source injected majority electrons flow along the E_y=0 path (Fig.6a, path 1) where the II-contribution is solely determined by the lateral field. In off-state however there is a more uniform distribution of generated carriers along the fully depleted Si volume making the vertical II-paths determined by the vertical field (Fig. 6a, path 2) equally important. The multiplication along these paths (Fig. 6b) is then incorporated with the thermal generation current model (Eq. 2) to obtain the (leakage) I-V curves (Fig. 7a). The analytical model, TCAD-simulation and experimental *I-V* data were compared for a wide temperature range and show good agreement (Fig. 7b). The analytical model, if applied inversely, can be used for extracting (effective) interface trap density or surface generation velocity (s_g) profiles at the Si/SiO_2 interfaces. Leakage

current increases at relatively low V_{DS} for drain-side localized interface damage (Fig. 5) with the onset and shape of this increase depending on the position and shape of the s_g profile (Fig. 8). The absolute values extracted for s_g depend on the extracted (virgin device) bulk-SOI thermal generation lifetime (τ_g, Fig. 1). This is the only parameter requiring extraction while all other physical parameters are calculated or obtained from previous works (12-15).

Stress Analysis/ Results

The degradation phenomena are experimentally investigated through accelerated off-state stressing at V_{DS}=650V and T=100°C doing hourly *I-V* characterizations at the stress temperature and full temperature sweep characterizations (25, 50, 75 and 100°C) performed at 2, 12 and 24h (Fig. 9a). As expected, an increased interface generation is seen at relatively low V_{DS} with the accompanying trapped charge (Fig. 9b) identified through extra multiplication seen at high V_{DS}. The subthreshold *I-V* curves also show an increase in multiplication after degradation (Fig. 9c) due to the injected/trapped interface charge at the Si/SiO_2 interface. As the injected charge affects the charge balance needed for the RESURF effect, it creates (lateral) field peaks ultimately causing premature breakdown due to runaway multiplication at such a local E_X field peak (Fig. 10e). The R_{on} and threshold voltage V_T are shown not to be affected by the local (drain side) Si/SiO_2 interface off-state degradation (inset Fig. 9c) as V_T is mainly determined by the channel region, while R_{on} is governed by the current flow in the center of the drift region away from the degraded interface.

An extensive degradation analysis has been performed on the stress induced increased interface generation seen in the leakage current (T=50°C), extracting the time-evolution of the s_g profiles (Fig. 10c) from the 2, 12 and 24h characterizations. Surface generation velocity profile extraction is performed by subtracting the measured virgin leakage current from the degraded leakage current *I-V* (Fig. 10a-b, with $I_{Gen}^{Si} \sim I_D^{virgin}$ at low V_{DS}) leaving only the increase in generation rate originating from the degraded interface ($I_{Gen}^{I\_dgr}$). From these $I_{Gen}^{I\_dgr}$ relations (Fig. 10b), the surface generation velocity s_g (or D_{it}) profile is extracted using the (fitted) quadratic l_I vs. V_{DS} relation for interface degradation location (Fig. 4: Eq. 1d, Fig. 5 bottom). A slight offset is seen in the extracted profiles (Fig. 10c) due the injected charge influencing depletion at the degraded interfaces.

From the leakage multiplication curves (Fig. 10d), extracted using $I_{Gen}^{I\_dgr}$ as the generation component (Eq. 2), and the subthreshold multiplication curves (Fig. 10e), the lateral field was extracted employing the method presented earlier (10,11). An increasing field peak is seen near the drain after stressing. Using the s_g profiles, extracted at relatively-low V_{DS} and a single temperature, the degraded *I-V* curves at different temperatures can be predicted for the whole V_{DS} range where leakage is dominated by generation (using Eq. 1 and 2). As shown in Fig. 10f, the prediction is quite accurate for low and medium V_{DS} values. The drain current versus temperature slope is lower at high V_{DS} (avalanche regime) than at low V_{DS} (generation regime) highlighting the positive T-dependence of (interface) generation and the negative T-dependence of II (lower M) seen in the degraded curves (Fig. 10f : inset). For higher $V_{DS,}$ the increasing II-current results in a mismatch between the predicted and the measured values due to the stress-induced drain field peaks not being (fully) taken into account by the predictive model. Nonetheless, performing quick, nondestructive low V_{DS} scanning allows for extracting T-dependent degradation information in a voltage range significantly broader than the scanning range itself.

Conclusions

The degradation phenomena in FP assisted RESURF power devices have been investigated. The results show that after high voltage off-state stressing at various temperatures the Si/SiO_2 interface is degraded at the drain side of the drift region. Due to the unique depletion expansion in these devices the effect of this localized damage appears in two different regimes of the *I-V* curves, as the stress-induced damage affect both the low-V_{DS} leakage current and the high voltage breakdown behavior, respectively. A model has been developed which allows for surface generation velocity profile extraction, from which *I-V* degradation predictions across temperature can be made via noninvasive low-voltage scanning. Combined with lateral field extraction from the subthreshold characteristic of these FP RESURF devices, a detailed profiling of the full HC induced degradation through electrical characterization is shown. The low voltage ("leakage") changes allow monitoring of degradation without adding additional stress.

Acknowledgement

The author would like to thank the Point-One frame work for their financial support, and Dr. G.A.M. Hurkx and Dr. R. van Dalen for their discussions and reviewing this work.

References

(1) S.Merchant *et al.,* ISPSD, pp. 31, 1991.
(2) B.Weir, IEEE Spectrum, Vol. 49(3), pp. 42, 2012.
(3) D.K.Schroder, ISBN 978-0-471-73906-7, 2006.
(4) A.Neugroschel *et al*., TED, 42(9), pp. 1657, 1995.
(5) D.Varghese *et al*., TED, 57(10), pp. 2704, 2010.
(6) S.Poli *et al*., ISPSD, pp. 152, 2011.
(7) Silvaco's ATLAS (Version: 5.16.3.R).
(8) J.A.Appels & H.M.J.Vaes, IEDM, pp.238, 1979.
(9) S.Merchant, TED, 46(6), pp. 1264, 1999.
(10) B.K.Boksteen *et al.,* ISPSD, pp. 145, 2012.
(11) R.v.Dalen *et al.,* ISPSD, pp. 89, 2010.
(12) D.K.Schroder, TED, 44(1), pp. 160, 1997.
(13) S.Merchant *et al.,* ISPSD, pp. 130, 1995.
(14) S.M.Sze & K.K.Ng, ISBN 978-0-471-14323-9, 2006.
(15) M.Ershov & V.Ryzhii, Sem.Sci.Tech, 10(2), pp. 138, 1994.

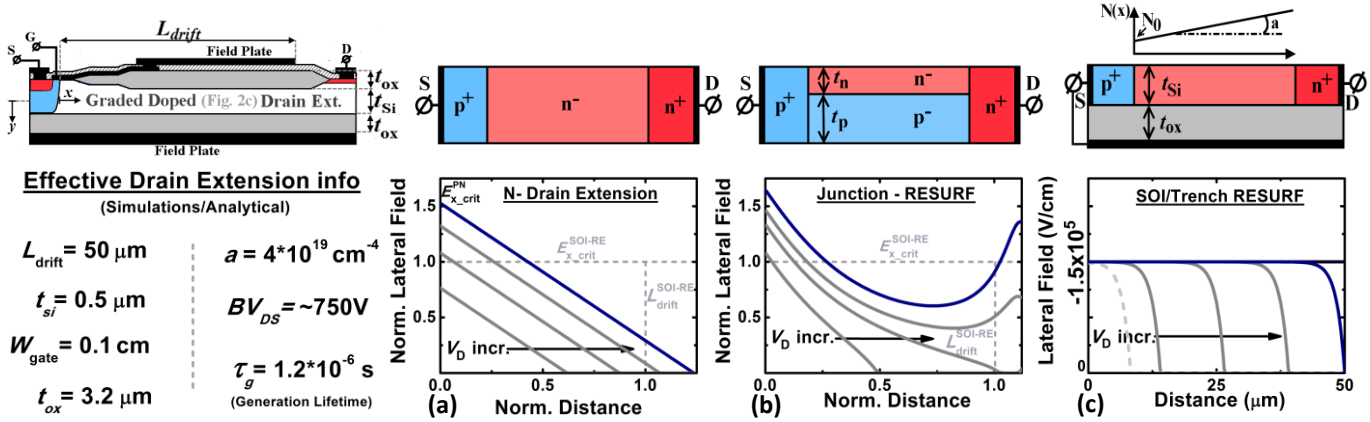

Fig. 1: Schematic cross-section of a typical HV-SOI FP assisted (double) RESURF (N)LDMOS and the extension parameters used to simulate and model the device.

Fig. 2: Schematic cross-sections and their lateral field distribution of (a) conventional, (b) junction RESURF (8) and (c) field-plate (FP) assisted RESURF pn-junctions. Lateral Field distributions are taken at the surface (BV_{DS}=750V). The field and drain extension depletion distances of (a) and (b) are normalized to that of (c) for comparison.

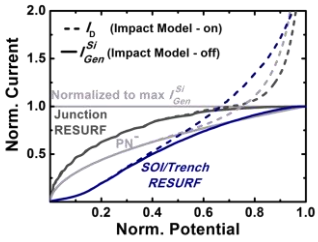

Fig. 3: Simulated leakage *I-V* characteristics of the various pn-junctions (Fig. 2). Currents are normalized to maximum "bulk" generation currents and voltages to BV_{DS}. Since a ΔV_{DS} does not significantly affect the lateral peak field at the already depleted zone, a more evenly distributed increase in II is seen along a larger part of the bulk generation component (dashed vs. solid) in the FP-RESURF device.

(Eq.1) $$I_{Gen}^{Tot}(V_{DS}) = I_{Gen}^{S}(V_{DS}) + I_{Gen}^{I}(V_{DS}) + I_{B2B}(V_{DS})$$

$$I_{Gen}^{S} = \frac{q \cdot n_i \cdot l_S \cdot t_{Si} \cdot z}{\tau_g} \quad (1a)$$

$$I_{Gen}^{I} = \frac{2 \cdot q \cdot n_i \cdot (l_I - l_S) \cdot t_I \cdot z \left(\frac{s_g \cdot \tau_g \cdot f}{t_I} + 1 \right)}{\tau_g \cdot f} \quad (1b)$$

$$V_{DS}^{S} = \frac{a q \lambda^3}{\varepsilon_{Si}} \left(\frac{l_S}{\lambda} - \tanh\left(\frac{l_S}{\lambda} \right) \right) \quad (1c)$$

$$V_{DS}^{I} = \frac{q \cdot a \cdot l_I \cdot t_{ox} \cdot \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot \varphi_b(l_I)}{q \cdot a \cdot l_I}}}{\varepsilon_{ox}} \quad (1d)$$

$$\lambda = \sqrt{\frac{t_{Si}}{2} \left(\frac{t_{Si}}{4} + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \cdot t_{ox} \right)} \quad (1e)$$

$$t_I(x) = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot \varphi_m(x)}{q \cdot a \cdot x}} \quad (1f)$$

(Eq.2) $$I_{leak}(V_{DS}) = I_{Gen}^{Tot}(V_{DS}) \times M$$

$$M = \frac{1}{1 - \alpha} \quad (2a)$$

$$\alpha_x = \int_0^{l_S} a_n \cdot exp\left(\frac{-b_n}{E_x(x)} \right) dx \quad (2b)$$

$$\alpha_y = \int_0^{\frac{1}{2} t_{Si}} a_n \cdot exp\left(\frac{-b_n}{E_y(l_S)} \right) dy \quad (2c)$$

Fig. 4: Equations for modeling leakage. **Eq. 1:** Overview of the total thermal generation component (12) with contribution of (1a) the fully depleted (bulk SOI) part of the extension, (1b) the interface depleted part of the extension. The band to band tunneling (B2B) component is calculated using (13). The voltage dependence of the FD-SOI depletion length l_S (1a) and interface depletion length l_I (1b) is obtained from (1c) and (1d). The interface depletion thickness t_I is derived using (1f). The temperature dependence of I_{Gen} is taken into account using the n_i vs. temperature relation from (14). **Eq. 2:** Calculation of the leakage including impact ionization induced multiplication M (2a). The impact ionization integral for electrons along the horizontal and vertical multiplication path is given by (2b) and (2c), respectively (Fig. 6). The II temperature dependence is included in the a_n, b_n parameters taken from (15).

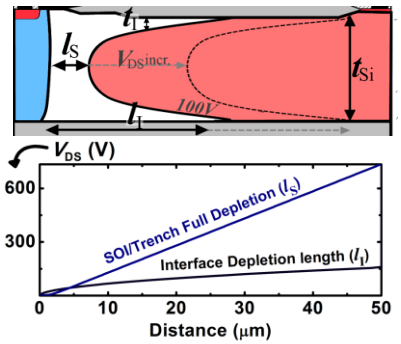

Fig. 5: Top: Graphical overview of the drain extension depletion profile used to calculate charge volume for the generation current (Fig. 4, Eq.1). Bottom: The voltage dependence of the FD-SOI depletion layer length l_S and interface depletion layer length l_I. This separation of interface depletion vs. SOI depletion allows for separate scanning of different degradation phenomena.

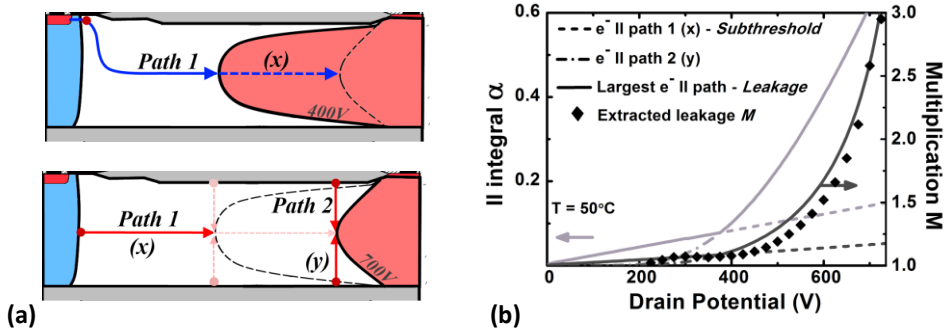

Fig. 6: Main impact ionization paths for the semi-on ($0<V_{GS}<V_{th}$) subthreshold regime and off-state (V_{GS}=0) leakage. **Fig. 6a:** Top: In subthreshold the main electron flow path is along the center of the SOI (blue arrows, path 1) where the E_Y field is 0 V/cm and thus II induced multiplication is due to the E_X field. Bottom: Carrier generation in off-state happens along the fully depleted volume and 2 paths have to be evaluated: (x) low E_X field but longest path from S to D (center SOI, path 1) and (y) extremely high E_Y (9) but short path from Si/SiO_2 interface to center Si (path 2). The path giving the largest II integral becomes dominant (>400V) in calculating avalanche multiplication in case of the leakage current. **Fig. 6b:** The calculated II integral and M values along the different paths are visualized for the ideal case.

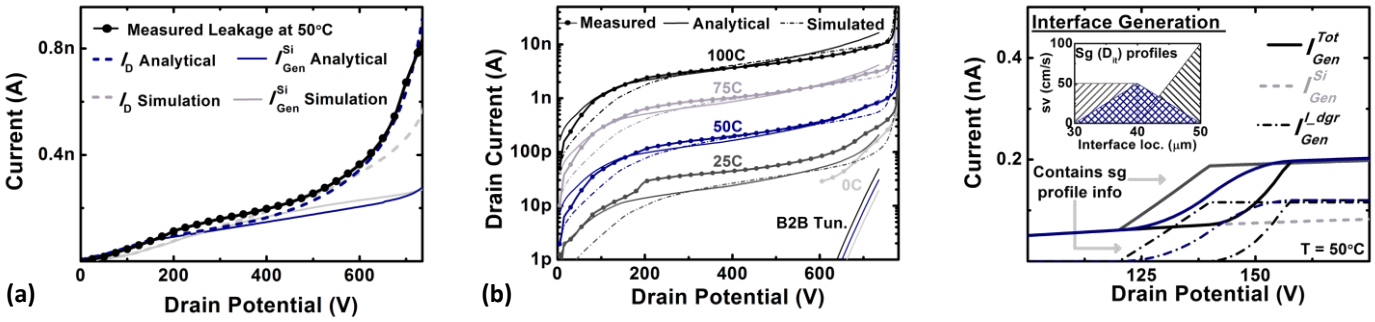

Fig. 7: Analytical, simulated and measured leakage current comparison of a virgin device showing good agreement over a wide temperature range. **Fig. 7a:** Linear scale. **Fig. 7b:** Log scale comparison at different temperatures. The B2B tunneling component (13), due to the high E_Y field (Fig. 6b), becomes apparent at 0°C and below while it is overshadowed at higher temperatures. Given this lack of temperature dependence, the hump around 200V in the measured leakage current of the device at 25°C is due to a local B2B tunneling effect.

Fig. 8: The influence of degraded surface generation profiles on leakage, modeled using Eq. 1. An increase in the surface generation velocity (s_g) component (Eq. 1b) results in an increase of I_{Gen}^{Tot}. Different s_g profiles result in different shapes of the *I-V* curves.

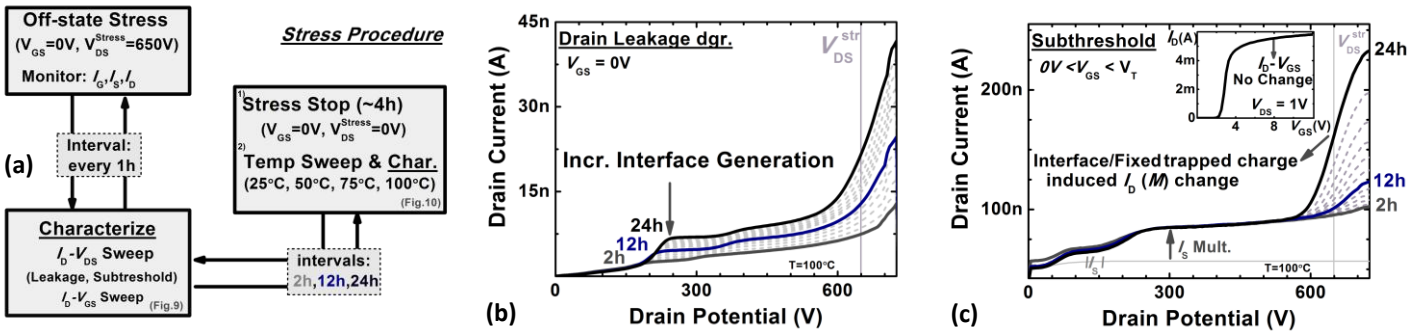

Fig. 9: Device degradation as seen in measured off-state stressed *I-V*. **Fig. 9a:** Flow chart of the complete off-state stress procedure. **Fig. 9b:** Measured leakage degradation clearly shows a more than double increase in "low" voltage leakage current due to increased surface generation at a high voltage degraded interface (seen at low voltages due to interface depletion; Fig. 5, Fig. 8). **Fig. 9c:** Measured subthreshold I_D-V_{DS} curves show a clear increase in I_D at high V_{DS} due to an increase in multiplication after stress. Inset shows that local degradation does not affect the on-state device characteristics (e.g. R_{on}, V_{th}).

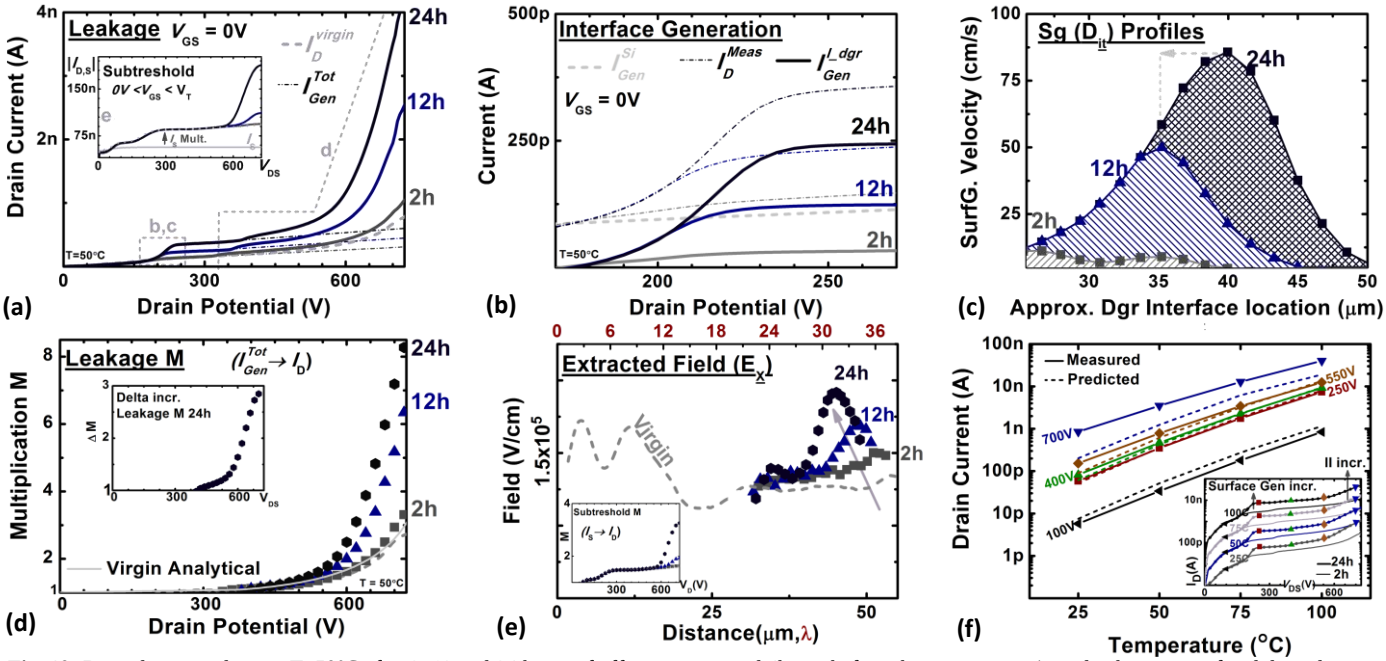

Fig. 10: Degradation analysis at T=50°C after 2, 12 and 24 hours of off-state stress and 4h rest before characterization (to only characterize fixed degradation components). **Fig. 10a:** Leakage and Subthreshold (inset) I_D-V_{DS}'s analyzed. Thin light gray dotted lines indicate what regions of the *I-V* curves are used in the subsequent figures. **Fig. 10b**: Measured and extracted ("inverse", Fig. 8) degraded interface generation rate, $I_{Gen}^{I\_dgr}$. **Fig. 10c:** Extracted surface generation velocity (or D_{it}). **Fig. 10d:** Injected/interface trap charge influence as seen in leakage *M*. Inset shows *M* change normalized with the virgin *M*. **Fig. 10e:** The extracted lateral field (10,11) due to the trapped interface/oxide charge distribution changes, extracted from the subthreshold *M* (inset). **Fig. 10f:** The s_g profile extracted at T=50°C allows for accurate predictions over a wide temperature range using the analytical model.