SIGNIFICANCE OF INCLUDING SUBSTRATE CAPACITANCE IN THE FULL CHIP CIRCUIT MODEL OF ICs UNDER CDM STRESS

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In CDM type of ESD, the IC is both the source and part of discharge current path. To study the CDM performance of an IC, a full-chip circuit model that includes the various static charge sources and its discharge path through the circuit as it occurs in reality is needed. Static charge sources in a CDM event are the various package capacitors. The CDM circuit models presented before only include the capacitors formed by the IC circuit design on the package and not that of die attachment plate on which the die is placed. This paper emphasizes the need to include this capacitance and presents a simple method of including this capacitor and its discharge path through the circuit during CDM stress. [*Keywords: CDM*]

INTRODUCTION

Most of the CDM simulation works has focused on modeling the behavior of individual protection devices [1]. But CDM performance of an IC does not only depend on the performance of the protection devices but on its entire circuit design layout and its package parasitics as well [2,3]. A charged IC under CDM stress is equivalent to several pre-charged capacitors formed by the various conducting layers in the IC with the package. The influence of these capacitors on the CDM performance of an IC, depends on the amount of charge stored in it and its discharge path through the circuit [4]. The CDM circuit models presented before, includes only those capacitors formed by the IC circuit design, namely bus lines, metal interconnects, junction capacitors and so on. The voltage overshoot across the gate-oxides always referred to the voltage drop between the gate node and source node of a MOSt. The capacitance formed by the die attachment plate (or die) with the package, the substrate capacitance is not included. This capacitor is generally much larger than any of the capacitors formed by the circuit design and hence can be considered as the major source of static charge during CDM stress [5]. Moreover all circuit elements in a given circuit design are either directly or indirectly connected to the substrate. The general picture is that tribo-electric charge on the package surface mirrors as charge on the die (+attach). For simplicity this charge can be considered present on the back side of the die. During discharge via one pin, this charge finds its way through the substrate and all possible connections of the substrate (substrate contacts –guard rings- to V_{SS}, via parasitic n-well junction diodes to V_{DD}) ultimately via a protection device to the discharging pin. During this process of discharge, gate-oxide failure can result when the voltage transients across the gate-substrate nodes of a MOSt increases beyond its breakdown threshold. But if a dense mesh of substrate contacts or guard rings is present, properly connected to low-Ohmic ground and/or power line system, core circuits can be properly protected. So for a complete study of the CDM performance of a given IC, the voltage transients across both the gate-source and gate-substrate have to be taken into account. This paper is organized as follows: In the first section, an equivalent circuit model for an IC, including its substrate capacitance and its discharge path during a Field Induced CDM (FCDM) test method is presented. In the second section, the full chip model is applied to evaluate the CDM performance of an IC with I/O cells of two different designs in 0.18mm technology node.

EQUIVALENT CIRCUIT MODEL FOR COMPLETE IC

The most commonly used test method to study CDM robustness of an IC is FCDM. An equivalent circuit model for an IC under FCDM is shown in Figure 1. The parasitic parameters of both the IC and the test set-up, are taken into account in this circuit model. The package capacitors C_{PIN} and C_{SUB}, are pre-charged to the initial stress level. CDM discharge is initiated by the sudden switching of V_{SWITCH} from the stress level say V_{CDM} V to 0V. Notice that the discharge current from C_{PIN} does not flow through the circuit and hence does not have much influence in the CDM performance of the IC, but can have a considerable contribution to the total CDM current measured. The discharge path of the substrate capacitance consists of the silicon substrate and the circuit elements which are directly or indirectly connected to it. To model the discharge current path the substrate is subdivided into smaller unit volumes. Each unit volume is modeled into a 3-D resistive network as shown in Figure 2. One end of this resistive network in the Z direction is connected to C_{SUB} and the other end to the circuit elements in that volume. Any circuit in general consists of protection devices, bus lines and internal core circuitry.

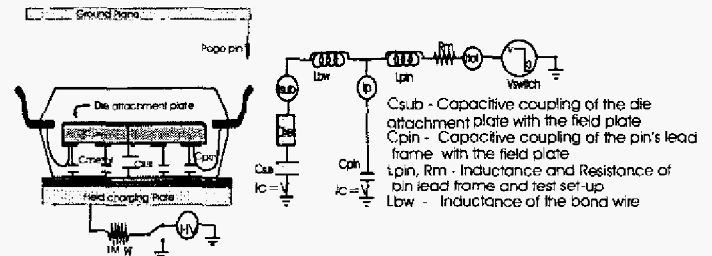

Figure 1. IC chip under FCDM test condition along with its equivalent circuit model (C's carry an initial stress V).

The CDM behavior of the protection devices are modeled by its compact circuit model [1]. The parasitic bus line resistances of the supply lines are also taken into account. The circuit elements have either direct or indirect contact to the substrate. Figure 3 shows the parasitic contacts which a single inverter inside a guard ring makes with the substrate. This circuit representation holds good under the assumption that the IC is not powered up during CDM discharge.

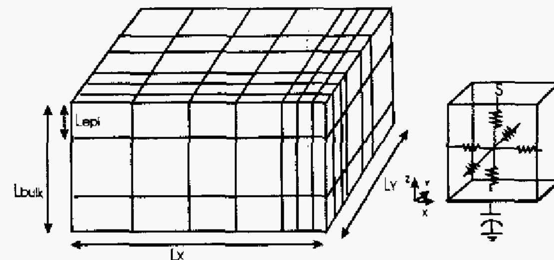

Figure 2. Equivalent 3-D resistive network of substrate

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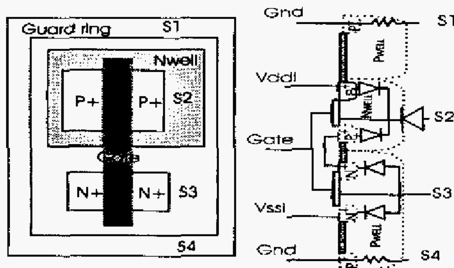

Figure 3. Equivalent circuit model of an inverter inside a guard ring and its parasitic contacts with the substrate.

SIMULATION AND EXPERIMENTAL RESULTS

IC test structures with a ring of input and output cells were made in 0.18mm technology node with two different protection designs. We will refer to them as design 1 and design 2. Basic schematic sketch of the input cell is shown in Figure 4. Each I/O pin is clamped to the supply lines via large protection devices, PD as shown in figure 4. The internal circuitry consists of two input inverters placed inside a guard ring region. IC with design 2 is identical to design 1 in all aspects such as package type, die size, pin counts and protection devices at the I/O pads, but has additional clamping devices PD 5 and PD 6 placed closer to the inverter as shown inside the dotted lines in the schematic sketch. The sources of both nMOSt and pMOSt have only a parasitic diode contact to the substrate. Hence even if the gate-source voltage is well guarded below its breakdown threshold, the gate-substrate voltage can be higher than its gate-source voltage, depending on the voltage drop across the substrate resistance which in turn depends on the distance of the MOSt from its closest source-substrate contact. CDM measurements on the ICs showed that all the I/O cells with design 1 failed at -400V stress level, while those of design 2 did not fail even at -1000V CDM stress. Failure Analysis on the failed ICs showed gate-oxide failure at the first input inverter and that it was most often at the nMOSt.

The full chip circuit model as explained above was applied to study the CDM performance of the two ICs. In Figure 5, the potential at the substrate nodes with respect to the gate of the first input inverter of the discharged I/O pin, in the area directly below the inverter during -300V CDM stress at 450ps is shown. From Figure 5, we see that the substrate potential under the nMOSt of the first input inverter is higher than that at the pMOSt. In Figure 6, the potential drop across both the gate-source and gate-substrate nodes of the nMOSt in the first input inverter in design 1 and design 2 is plotted. Note that the potential drop across the gate-substrate nodes is higher than the potential drop across the gate-source nodes of the nMOSt.

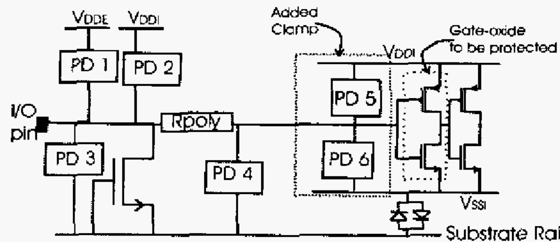

Figure 4. Schematic sketch of input cell protection structure of design 1 and design 2.

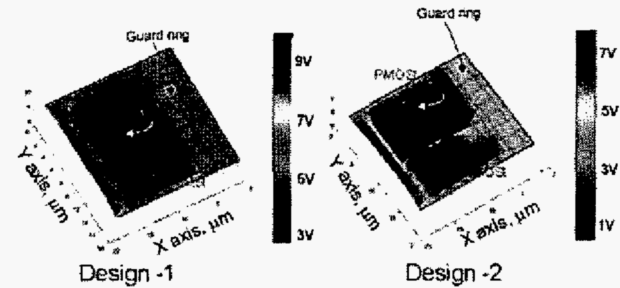

Figure 5. Potential drop distribution across the substrate in the region below the inverter at 450ps during -300V CDM stress

Also the gate-source and gate-substrate voltage transients across the nMOSt gate-oxide of design 1 are higher than that in design 2. Apart from avoiding the additional voltage drop along the bus line to be seen by the gate-source node, the added clamping device also brings the substrate potential closer to its source potential.

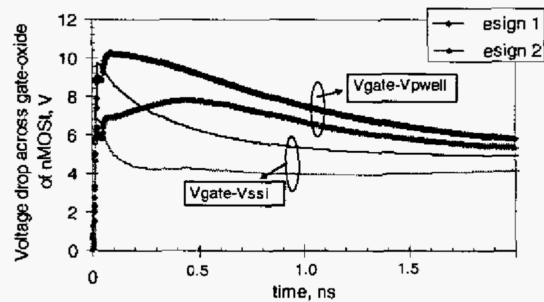

Figure 6. Voltage transient across nMOSt gate-oxide during -300V CDM stress.

CONCLUSIONS

Among the various CDM current sources, the substrate capacitance is one of the significant current sources. Hence should not be neglected in the CDM circuit model used to evaluate the CDM performance of an IC. A suitable method by which one can model the substrate capacitance and its discharge path during CDM stress is presented. This model helps us not only to study the effect of bus line resistance but also the possible gate-oxide damage resulting from gate-substrate voltage overshoot. The circuit model is applied to explain the observed CDM performance of two ICs with different input protection designs. Simulation shows that gate-oxide damage could originate from gate-substrate voltage overshoot as well. Thus for a complete CDM performance analysis of an IC, the substrate capacitance needs to be included.

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