ON JITTER DUE TO DELAY CELL MISMATCH IN DLL-BASED CLOCK MULTIPLIERS

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ABSTRACT

This paper describes the jitter problem in DLL-based clock multipliers that arises due to stochastic mismatch in the delay cells that are used in the Voltage Controlled Delay Line of the DLL. An analysis is presented that relates the stochastic spread of the delay of the cells to the output jitter of the clock multiplier. This analysis shows that relative time deviations are highest in the middle of the Delay Line and proportional to the square root of the frequency multiplication factor of the structure. A circuit design technique, called Impedance Level Scaling, is presented that allows the designer to optimize the noise and mismatch behavior of a circuit independent from other specifications such as speed and linearity. Applying this technique on delay cell design yields a direct trade-off between noise induced jitter and power usage, and between stochastic mismatch induced jitter and power usage.

1. INTRODUCTION

An important building block in almost all digital and mixed signal Integrated Circuits is the clock multiplier, which multiplies the incoming reference clock frequency by a certain factor, *e.g.* because no crystals are available with a clock frequency as high as needed on-chip. Also, when parallel data is to be serialized using a multiplexer, clock multiplication is needed to time the outgoing bits. In these applications, the quality of the multiplied clock with respect to timing jitter is an important specification.

Apart from the usual Integer-N PLL implementation of the clock multiplier, where a Voltage Controlled Oscillator (VCO) is locked to a clean reference clock, architectures based on a Delay Locked Loop (DLL) have been successfully used recently as Clock Multipliers [1][2][3]. In such an architecture, which is schematically shown in Fig. 1, a Voltage Controlled Delay Line (VCDL) is locked to a clean reference. The extra timing information needed to generate the high frequency clock is obtained by using a VCDL that consists of several tuneable delay cells, thus generating multiple phases of the low frequency clock, which are combined into one high frequency clock using a circuit that is referred to as Edge Combiner. The advantage of the DLL-based architecture is that the VCDL is 'reset' with respect to stochastic jitter every time a new reference edge is applied at the input, whereas in the VCO of a PLL the jitter accumulates [4].

There is however another very important source of jitter in this type of architecture. The stochastic mismatch between the delay cells causes clock skew of the intermediate clock phases. This phenomenon will be measurable as systematic jitter on the high-frequency clock that is at the output of the Edge Combiner.

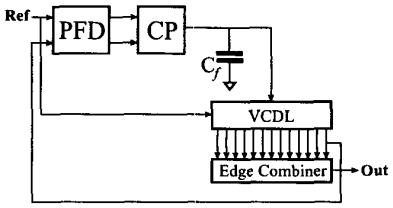

Fig. 1. The DLL-based clock multiplier architecture

The delay cell mismatch will cause spurious peaks in the output frequency spectrum of the clock multiplier [5]. In this paper, however, we analyze the effects of delay cell mismatch on the time domain output signal (meaning *jitter*). This offers a design equation useful for determining the feasibility of a DLL-based implementation of the clock multiplier.

Because the mismatch parameters of devices depend on the chip area that is used, the effect of scaling on the delay cell mismatch is analyzed, using a technique called Impedance Level Scaling [6]. This design technique proves useful in decoupling the noise and mismatch properties of a circuit from other properties such as speed or linearity.

In section II of this paper, the DLL architecture and the Edge Combination process are described briefly. Section III gives an analysis of the effects of delay cell mismatch on the output signal of the clock multiplier, linking output jitter to stochastic properties of the mismatch of the delay cells. The effects of so called Impedance Level Scaling are examined in section IV of this paper. The results of the analyses are discussed in section V. The paper finally concludes in Section VI with a summary of the results.

2. THE DLL ARCHITECTURE

Fig. 1 shows the general architecture of a DLL with edge combiner. The feedback mechanism consists of a Phase Frequency Detector (PFD) that is combined with a Charge Pump (CP). The loop filter consists of a simple capacitor that integrates the charge pulses coming from the CP. In a PLL such a simple filter would lead to stability problems because of the integrating function of the VCO used in a PLL; in a DLL, however, there is no pure integrator other than the CP combined with the loop filter capacitor, which guarantees stability.

The basic idea behind a DLL-based clock multiplier is that the total delay of the multi-tapped VCDL is controlled by the loop to be equal to the input period of the reference clock. The different output taps now deliver different phases of the input clock which

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contain extra timing information that can be combined into one clock with a frequency that is an integer multiple of that of the reference clock. This has been illustrated in Fig. 2, where the multiplication factor N equals 4.

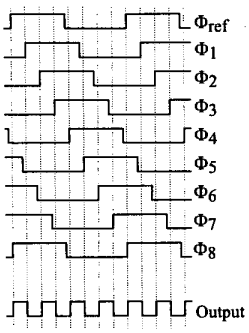

Fig. 2. The edge combination process for $N = 4$, using only rising edges to generate the output clock

If only the rising edges of the different clock phases are used to generate both the rising and falling edges of the generated clock, it is easy to show that the number of output taps needed is equal to twice the frequency multiplication factor. In some cases it is possible to also use the falling edges of the different clock phases to generate timing information. However, timing dependency on the duty cycle of the reference is now introduced, which might form a problem in some applications.

It is also possible to generate the rising edges of the output signal directly from the rising edges of the different clock phases, while the falling edges of the output signal are generated by the use of a resonator, as described in [1]. A disadvantage of this method is that an inductor is used, which consumes area and is more difficult to port to newer technologies than a purely digital solution.

In this paper, we assume that only the rising edges of the different clock phases are used without a resonator (Fig. 2 being an example of this), and thus the number of delay cells M in the VCDL equals:

$$M = 2N \tag{1}$$

where N is the ratio between the output frequency of the edge combiner and the incoming reference frequency.

3. DLL OUTPUT JITTER ANALYSIS

Because of stochastic component mismatch, the delay of different delay cells in the VCDL will not be exactly equal for a certain tuning voltage, which will result in jitter as all the intermediate edges on the different output taps are not corrected by the loop. The amount of jitter caused by this effect is calculated here.

Although mismatch is caused by a stochastic process, the jitter that originates from it is deterministic, because once the chip has been processed, the mismatch properties are more or less fixed. Therefore, the timing errors that are caused by this fixed mismatch are from then on systematic. Knowing the stochastic properties of the mismatch, predictions can be made *a priori* about the deterministic jitter.

The delay mismatch can be described mathematically as follows:

$$d_n = \{1 + e_n(v_c)\}\, d_{tune} \tag{2}$$

where d_n is the particular delay of delay cell number n, d_{tune} is some nominal delay which is controlled by the VCDL tuning voltage v_c and $e_n(v_c)$ is a random variable, describing the delay cell mismatch for a certain value of v_c. For simplicity, this dependency on v_c will not be shown explicitly in the remaining equations. The variable e_n is assumed to have zero mean. The delay mismatch of different cells is assumed to be uncorrelated.

The total delay of the VCDL will be equal to one period of the input clock after lock has been achieved. This results in the following equation for the individual delay of the delay cells:

$$d_n = T_S \frac{1 + e_n}{M + \sum_{n=1}^{M} e_n} \tag{3}$$

where M denotes the number of delay cells in the VCDL and T_S the period time of the reference signal.

Now an expression for the total systematic jitter of the signal on the m-th tap (at the output of the m-th delay cell) can be derived. If all the delay cells would be perfectly matched, the delay between the input and the m-th tap would be $\frac{m}{M}T_S$. In case of mismatch, the systematic jitter after m cells can then be calculated to be:

$$\Delta t_m = \sum_{n=1}^{m} d_n - \frac{m}{M}T_S = T_S \left(\frac{m + \sum_{n=1}^{m} e_n}{M + \sum_{n=1}^{M} e_n} - \frac{m}{M} \right), \tag{4}$$

the variance of which can be shown to be:

$$\sigma^2_{\Delta t_m} = E\left\{(\Delta t_m)^2\right\} \approx T_S^2 \frac{m\,(M-m)}{M^3} \sigma^2_{e_n} \tag{5}$$

assuming uncorrelated values of e_n with zero mean. A first order Taylor expansion has been used, assuming $\sigma^2_{e_n} << 1$.

It is interesting to note that the variance of Δt_m is highest for $m = \frac{1}{2}M$, *i.e.* halfway the VCDL. This is to be expected: the loop controls the VCDL such that the time error at its output is zero, while the error at the input of the VCDL is also zero. The highest timing uncertainty will be in the middle of the VCDL, where the distance to these clean points is highest. This is comparable to mismatch in resistors in a resistor string based A/D converter, where the highest deviation is also found in the middle of the string [7].

The sigma value of the phase time error halfway the VCDL can be approximated, using (5), to be:

$$\sigma_{\Delta t_{\frac{1}{2}M}} \approx \sigma_{e_n} \cdot \frac{T_S}{2\sqrt{M}} \tag{6}$$

Equation (5) has been verified using numerical statistical analysis for a constant value of the nominal delay of a single delay cell, the results of which are shown in Fig. 3. This figure shows a very good agreement between the predicted time deviations and the simulations. It also shows clearly the peak of the time deviation variance at the middle of the VCDL.

The jitter due to delay cell noise is also shown in the figure, for an arbitrary value of $\Delta t_{d\text{-rms}}$, the RMS jitter of a single delay cell due to noise. Using the fact that DLL output jitter due to delay cell noise is approximately equal to the stochastic jitter of the *uncontrolled* VCDL [4] yields:

$$\sigma_{\Delta t_m} \approx \sqrt{m}\Delta t_{d\text{-rms}}, \tag{7}$$

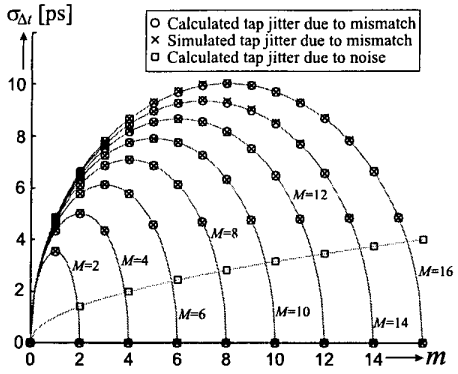

Fig. 3. Numerical statistical simulation results of the jitter due to delay cell mismatch

showing that the effect of delay cell noise is highest on the *last* output tap, as opposed to mismatch induced jitter.

If we define a measure of relative jitter, where the sigma value of the maximum time deviation is related to the output period of the clock multiplier, the following result is obtained:

$$\frac{\sigma_{\Delta t_{\frac{1}{2}M}}}{\left(\frac{T_S}{N}\right)} \approx \sigma_{e_n} \cdot \frac{\sqrt{N}}{2\sqrt{2}} \tag{8}$$

using (1), which shows that the relative jitter of the output signal is proportional to the square root of the frequency multiplication factor N, making a DLL architecture less suitable for high values of N.

4. IMPEDANCE LEVEL SCALING

It is a well-known fact that increasing the area of on-chip MOS-transistors improves the matching properties of those transistors [8]. The same also goes for the matching of resistors and capacitors on an IC [9]. This leads us to investigate the effect of increasing the area of a complete circuit in a systematic manner that we call *Impedance Level Scaling* [6].

The concept of Impedance Level Scaling is fairly simple, yet leads to very useful design considerations. This technique enables a decoupled optimization of the noise and mismatch properties of a circuit independent from other properties such as speed and linearity, thus simplifying the task of the designer.

Starting from a circuit that has been optimized with respect to specifications other than noise and mismatch, one can scale the *width* of every component of that circuit by a certain factor n. This is shown conceptually in Fig. 4, where the effect on the component values is also shown.

Using the analogy that scaling is similar to putting identical circuits in parallel, as illustrated in Fig. 5 where $n = 2$, it is easy to deduce that the node voltages of the scaled circuit are equal to those of the original circuit, provided the circuit is not heavily loaded externally. From this analogy it is also clear that the scaling will not change linearity and speed of the circuit.

A fact that is familiar to many designers is that Impedance Level Scaling will improve the Signal to Noise ratio of the circuit at the cost of increased power usage. More precisely, scaling the

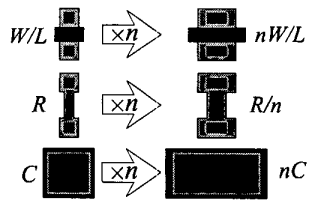

Fig. 4. The concept of Impedance Level Scaling

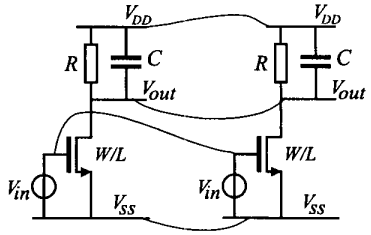

Fig. 5. Impedance Level Scaling presented as putting identical circuits in parallel

circuit by a factor n will decrease the RMS value of the noise voltage by a factor $\sqrt{n}$ while increasing the power usage by a factor n, meaning there is a direct trade-off between power usage and noise.

A less familiar but important property of Impedance Level Scaling is the effect it has on the mismatch errors of a circuit. Assume the relative change in the value of a certain component changes some circuit parameter (*e.g.* the offset voltage, or the delay of a delay cell) *linearly*. This is reasonable as long as mismatch changes the value of a component just slightly. The same *relative* change of the corresponding component in the scaled circuit will result in the same change of the output parameter, which can again be understood by the scaling analogy depicted in Fig. 5. But the mismatch of the component value of the scaled circuit will reduce by a factor $\sqrt{n}$ (see Table 1), which means the sensitivity of circuit parameters such as offset and delay errors will be $\sqrt{n}$ times less in the scaled circuit than in the starting circuit, at the cost of increased power usage.

Starting Circuit	After Scaling
$\sigma_{v_n} = \sqrt{\frac{4kT\gamma}{g_m}\Delta f}$ v_n ⊖ W/L $\sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{W \cdot L}}$ $\sigma_{\Delta V_T} = \frac{A_{V_T}}{\sqrt{W \cdot L}}$	$g'_m = g_m \cdot n$ v'_n ⊖ nW/L $\sigma'_{v_n} = \sigma_{v_n} \cdot \frac{1}{\sqrt{n}}$ $\sigma'_{\Delta\beta/\beta} = \sigma_{\Delta\beta/\beta} \cdot \frac{1}{\sqrt{n}}$ $\sigma'_{\Delta V_T} = \sigma_{\Delta V_T} \cdot \frac{1}{\sqrt{n}}$
v_n ⊖ R $\sigma_{v_n} = \sqrt{4kTR\Delta f}$ $\sigma_{\Delta R/R} = \frac{A_R}{\sqrt{\text{Area}}}$	v'_n ⊖ R/n $\sigma'_{v_n} = \sigma_{v_n} \cdot \frac{1}{\sqrt{n}}$ $\sigma'_{\Delta R/R} = \sigma_{\Delta R/R} \cdot \frac{1}{\sqrt{n}}$
C $\sigma_{\Delta C/C} = \frac{A_C}{\sqrt{\text{Area}}}$	nC $\sigma'_{\Delta C/C} = \sigma_{\Delta C/C} \cdot \frac{1}{\sqrt{n}}$

Table 1. Effect of Impedance Level Scaling on component properties

5. DISCUSSION

For a delay cell, the implication of the Impedance Level Scaling is that increasing the power by a factor n yields a stochastic jitter reduction of $\sqrt{n}$ (which also follows from the jitter analysis in [10]). Also the mismatch of the delay between different cells will improve by a factor $\sqrt{n}$.

Monte Carlo simulations have been performed on a Delay Line in order to verify the effect of Impedance Level Scaling on the delay mismatch and to compare the jitter due to mismatch to the jitter that is caused by circuit noise. The delay cells were realized as differential NMOS pairs with a resistive load, in a modern $0.18-\mu$ CMOS process. The delay of a single cell was about 50 ps; the differential voltage swing was 500 mV. The delay cell mismatch spread was simulated for various values of the scale factor n. The results of the simulations are presented in Fig. 6, where the results are used in combination with (6) with M=16 and T_S=800 ps. The upper solid line through these points has been calculated by applying the scaling theory on the simulation point at P=5.8 mW. The graph shows very good agreement between the theory and the simulations.

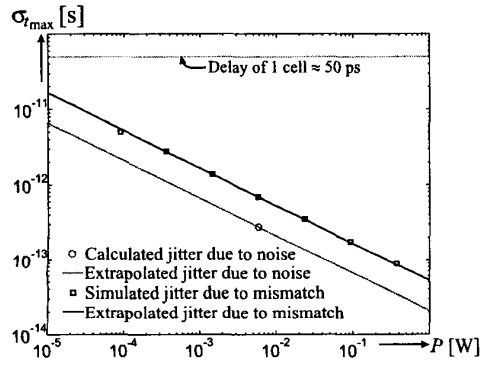

Fig. 6. Relation between power per delay cell and jitter, due to noise and mismatch; M=16, T_S=800 ps

Using results presented in [10], it is possible to estimate the jitter of one delay cell due to circuit noise. This has been done using operation point information obtained from simulations of the cells at P=5.8 mW. Using (7) leads to:

$$\sigma_{\Delta t_M} \approx \sqrt{M}\Delta t_{d\text{-rms}} \tag{9}$$

where $\Delta t_{d\text{-rms}}$ is the RMS jitter of a single delay cell as calculated in [10]. The calculated jitter due to noise is shown in Fig. 6, where the solid line represents the extrapolation of this calculation according to the scaling theory.

It is obvious from the graph that jitter due to mismatch is in this case dominating the jitter behavior of the delay line. Another important observation is that increasing the power has the same effect on both the jitter due to noise and the jitter due to mismatch (increasing the power per delay cell with a factor n, decreases the jitter by a factor of $\sqrt{n}$). Because the increase of power leads to a decrease in the total jitter, it is in theory possible to meet strict jitter specifications with a DLL- based architecture. This might however lead to unrealistic power usage of the structure.

6. CONCLUSIONS

Although a DLL-based frequency multiplier at first glance seems a better choice than a PLL based architecture because of the jitter accumulation effects in the PLL, another very important source of jitter should be taken into consideration: the stochastic mismatch of the delay cells in the VCDL. Monte Carlo simulations seem to indicate that this type of jitter is dominant in a DLL where intermediate clock phases of the VCDL are also used, due to the clock skew that is caused by the mismatch. The relative output jitter due to delay cell mismatch is proportional to the square root of the frequency multiplication factor N.

It has been shown, using the concept of Impedance Level Scaling, that there is a direct trade-off between power usage and output jitter of the frequency multiplier, both due to noise and to mismatch. The amount of output jitter is limited directly by the power budget of the circuit. It can be shown that if the delay cell mismatch is the most dominant jitter source for a certain circuit, it will still be dominant in an impedance level scaled version of this circuit.

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