A roadmap to a technological platform for integrating nanophotonic structures with micromechanical systems in silicon-on-insulator

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ABSTRACT

On the foundation of joint experience acquired by several research centres there was defined the roadmap to the desired single technological platform for fabrication of a specific class of photonic integrated circuits, which are controlled by mechanical means. In the paper the challenges of fabrication of such photonic circuits are discussed. The main arguments in favour of the Silicon-on-Insulator materials system as the basis for the platform are presented. Options for the mechanics-to-optics arrangement, materials and processes are described and illustrated with the current achievements from the authors' labs. In the roadmap the preference is given to the vertical arrangement in which, the mechanical part is stacked above the waveguiding layer. A flexible trimming routine is designed to complement the process flow if the technologies developed cannot provide the required reproducibility.

Keywords: waveguide optical resonators, add-drop filters, mechanically assisted photonic integrated circuits, micro/nano-mechanical systems, silicon-on-insulator technology

1. INTRODUCTION

Looking ahead, let's say 5 to 10 years, optical techniques will be largely employed in the Metro- and Access networks[1]. The optical systems will operate with multiple wavelengths at a speed exceeding 1 Gbit/s per WDM channel and will use compact devices, eventually with thousands of functional elements, to allow complex optical routing, wavelength selection, amplification and data processing. Reliability and low cost will be the most important issues. The only reasonable answer to these challenges will be the massive introduction of very large-scale integrated (VLSI) photonics based on high index contrast waveguiding structures with nanometre dimensions.

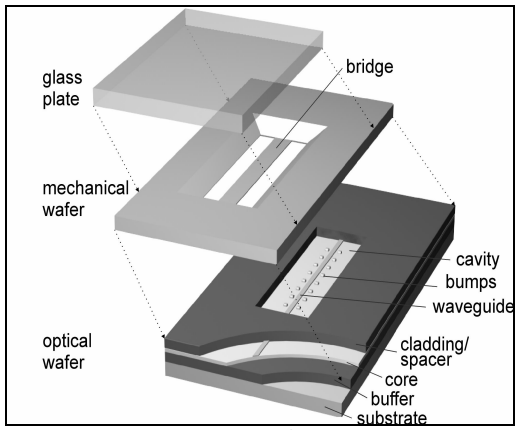

Figure 1: Schematic view of an electrostatic driven MOEMS device[6].

Since the pioneering work of Little et al.[2], who introduced the concept of VLSI photonics[3] much work has been done, see e.g.[4], and the EC project NAIS[5]. However, active control of photonic functional devices still lacks effective mechanisms despite a number of options investigated, including modulation of refractive index through carriers injection[7], photo-generation[8,9], depletion/enhancement[10] or thermo-optic effect[11] and modulation of absorption through carriers injection[12]. In semiconductors nonlinearities are weak that results in poor change of characteristics of a device in response to a control signal, e.g. filter tuning is practically limited to 1 nm. Increasing the density of active elements a heat bottleneck may arise when using thermo-optic or electro-optic effects.

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Even in the case of nanophotonic structures, like optical microresonators, tens of mW per active element is needed. The total heat generated in a VLSI photonic circuit would therefore require active cooling in contradiction with the demand of low-cost.

Controlling a photonic device via mechanical means, especially when micro/nano-mechanical systems (MEMS) are considered, can be an attractive alternative in a range of applications[13]. Switching and tuning by micro/nano-mechanical ways would offer a way to avoid the heat bottleneck, as in this case the active functions are voltage rather than power controlled. In addition, MEMS structures with sub-micrometer dimensions could have high resonance frequencies allowing switching and tuning within tens of microseconds.

Micromechanics and photonics have been developing separately for a long time. Despite sound results achieved in both domains, the realisation of photonic circuits integrated with mechanical subsystems is not straightforward, at least from technological perspective. Technological realization of MEMS controlled PICs has not been a subject for intensive research so far. There have been five relevant publications[6, 14, 15, 16, 17]. To our knowledge, no technological platform for commercial scale fabrication of MEMS driven high contrast PICs has been demonstrated up to now. On the foundation of joint experience acquired by a consortium formed by Lublin University of Technology, MESA+, KTH, Institute of Electron Technology, Heinrich Hertz Institute, Slovak Academy of Sciences and Lionix BV the roadmap to the desired single technological platform using Silicon-on-Insulator was defined. In the following the concept of the technological platform is presented. The challenges of fabrication of MAPICs are discussed.

2. A SILICON MAPIC DEVICE

The mechanically controlled photonic integrated circuits (MAPICs) can be a wide family of functional devices including: variable attenuators, dispersion compensators, non-selective and selective switches, tuneable filters, variable delay lines, drop filters, drop multiplexers, etc. A MAPIC device consists of nanophotonic circuits formed with nanowaveguides, couplers, resonant nano/microcavities etc. and a set of micro and submicro-scale mechanical subsystems, which perform actuation causing some photonic components to be tuned or switched. Technically, photonic devices can be mechanically controlled via actuating waveguides[17] or blocks of a lossy material or a dielectric[6]. Changing a relative position of waveguides alters coupling between them or, in case of a microresonator, it changes the resonance frequencies of the cavity. Rearranging localisation of dielectric blocks in vicinity of a waveguide core causes a change of its effective refractive index. Whereas it is applied to a block of a lossy material it causes the change of the waveguide loss through the evanescent field coupling. Actuation can be applied via a membrane, which is located over the waveguides.

There are four main types of microactuators that can be used for light manipulation: electrostatic, piezoelectric, electromagnetic and electrothermal. The advantage of electrostatic actuator[18] results from the fact that it is voltage rather than power controlled. The three remaining options are unattractive for MAPICs, because of limitations for miniaturisation (piezoelectric), low precision (electromagnetic) or problems with heat dissipation (electrotermic)[19, 20, 16]. The electrostatic actuator can be a comb or a parallel plate driver.

A SOI material system was chosen for fabrication of the MAPICs. The use of Silicon-on-insulator system is favourable as this material system is common in semiconductor industry and existing technologies can be adjusted to obtain the necessary resolution required for manufacturing of photonic components. Both nanowaveguides and micro/nano-mechanical parts can be fabricated on the base of SOI material system. With its silicon core and oxide cladding SOI has a high refractive index contrast, which is very advantageous for potential of future densely integrated devices. High index contrast materials allow making nano-wires and micro/nano-scale cubic or stripe shaped resonant cavities. Both, silicon and silicon oxide are transparent at the telecom wavelengths of 1.3 μm and 1.55 μm. The silicon slab waveguide can be single mode and can exhibit low mode leakage to the substrate provided that the top silicon layer and the buried oxide have proper thickness (0.25 μm and 1 μm respectively). Moreover, recent studies have shown that nanophotonic components in SOI are less sensitive to surface roughness than similar components made in III-V semiconductor[21].

Polycrystalline form of silicon has been extensively used for fabrication of MEMS for its good and reproducible mechanical properties: Young's modulus (164 Gpa), Poisson's ratio (0.3), fractures strength (2÷3 GPs). Weibull modulus is approximately 10, a value close to that of single crystal silicon (SCS), which would indicate a similar reliability of the two materials. However, using a SCS for micromechanics adds advantages such as lack of residual stress and stress gradients.

Many materials can be deposited on a SOI wafer, if necessary. In particular, these include SiO_2, Si_3N_4, polysilicon and amorphous silicon. All of them can form well controlled layers, fill gaps, be selectively cut and chemically or mechanically removed.

3. TECHNOLOGICAL REQUIREMENTS AND FABRICATION OPTIONS

Requirements for fabrication technology of nanophotonics on SOI are formulated primarily with respect to resolution and accuracy of written patterns and sidewall roughness resulting from processes of shape structuring. Nanowires can be as narrow as 400 nm and are typically isolated structures placed micrometers away from each other, while when being parts of a coupler can be 100 nm spaced. In photonic crystals holes can have a diameter of 300 nm with a pitch of 500 nm. Consequently the required resolution for writing such structures should be better then 100 nm. One can estimate the necessary accuracy to be around 10 nm. Particularly, inaccuracy of the realisation of a coupling gap between a bus waveguide and a microring severely affects the cross-talk figure of a microring-based drop multiplexer if worse than 10 nm. When defining a set of optical paths the accuracy should be below 1 nm, if the path lengths determine spectral behaviour of a device, which should comply with a frequency grid e.g. ITU-T DWDM.

Loss can be due to absorption, scattering, mode leakage and radiation. Loss not only manifests as insertion loss of a device. It severely affects Q-factors of microring resonator cavities reducing resonator selectivity. Scattering due to sidewall roughness origins from the technology related loss. It is a severe problem in nanowaveguides (both nanowires and photonic crystal waveguides). Decreasing the waveguide cross-section increases the loss dramatically[4], e.g. for a 500 nm nanowire 2.4 dB/cm loss was shown compared to 7.4 dB/cm for a 450 nm wide nanowire[22]. This component loss also tends to increase (together with radiative loss) with decreasing bend radius. Roughness should be in a range of nanometres to keep scattering acceptably low in narrow nanowaveguides.

The requirements for fabrication of micro-mechanical subsystems are of a very different character. Generally, they are related to the structuring processes, mechanical properties of materials, reliability. The dimensions of the nanophotonic components are hundreds of nanometres while the state-of-the-art mechanical ones are in the range of a few micrometers to tens of micrometers. Some mechanical components cannot be arbitrary miniaturized due to the effect of thermal vibrations. When defining mechanical components some features may have a high vertical to horizontal aspect ratio of 50 to 1. Narrow deep trenches should be created with almost vertical walls. Highly planar surfaces are required for almost every step of fabrication of a MEMS device. The vertical topography, which often is a result of a massive etch used for definition of mechanical components, can produce mechanical interference between moving parts. The mechanical interference arises when an upper layer of a deposited material must pass over the edge of a previously etched lower layer. Also, photolithographic definition of subsequent layers becomes problematic over severe topography. Photoresist becomes difficult to apply, expose, and develop, without loss of resolution and definition. Components have to avoid static curvature induced by residual stress and stress gradients in the deposited films. Such stress can be detrimental to cantilevered structures with high aspect ratios, which are often used in MEMS applications. Also, excessive residual stress can lead to mechanical failure during fabrication. Careful control of the deposition process conditions is necessary for the stress can be made reproducibly low. The primary obstacle to overcome in MEMS technology is adhesion causing one part sticking to another. Stiction occurs under different conditions: surface tension during release, electrostatic attraction due to trapped charge, etc. Sticking reduces the fabrication yield. Another concern is operational wear in actuators. Although some MEMS have been shown to operate for billions of operating cycles, the erosion of sliding surfaces and contamination must be controlled. Various solutions include: using harder structural materials, lubricants, optimising device design[23].

The mechanical subsystems can be kept in-plane with nanophotonic structures or stacked over the photonic part. Here, the focus is on the latter concept known as “vertical integration”. Vertical integration leaves more freedom for processing mechanical and photonic parts, as they are located in different layers. The vertical arrangement has attributes of a 3 dimensional construction: more functional components can be packed on the same wafer area compared to the 2D alternative. In the vertically integrated mechano-optical device the single crystal silicon layer is used for critical optical (and possibly electronic) components while mechanical subsystems are structured in the other layers or in another wafer. Any movement of mechanical components with respect to the nanophotonic part is restricted to the vertical plane.

Both the photonic and mechanical parts of a MAPIC are fabricated using deposition, lithography and etching processes, which combined may interfere degrading the device performance. For MAPICs the problem is to make the optical parts actuated while not compromising the resolution, accuracy and sidewall roughness as well as to assure the required

precision of movement. The challenge is to integrate the technological approaches and materials systems, individually optimised for nanophotonics and micromechanical subsystems, in a single technological platform.
The experience collected in fabrication of nanophotonic and micromechanical components[6, 24, 25 26, 27] support the two general approaches to fabrication of photonic circuits integrated with micro/nano mechanical subsystems which are considered in the following: (1) manufacturing separately the photonic and mechanical parts and then bonding them with precision and, (2) fabricating all components of the system i.e. waveguides and actuators starting from one SOI wafer, so wafer-bonding step can be avoided with the expense of more complicated process flow (see the fig 2). In any of the two approaches the fabrication sequence is complemented with a trimming procedure, which corrects the fabrication inaccuracies. Both options are discussed in detail in the following.

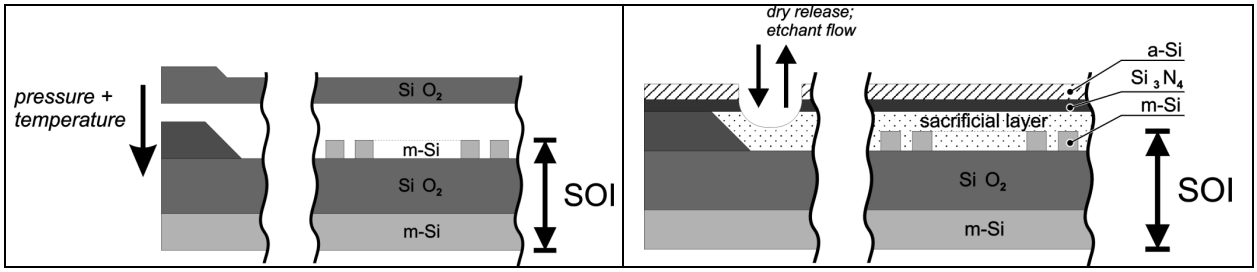

Figure 2: Bonding a membrane to a SOI wafer (left). Dry release to form a freestanding membrane (right).

3.1. Two wafer approach

The advantage of the first concept comes from absolute separation of the processing of mechanical and nanophotonic parts. This adds a degree of freedom, which allows using state-of-the-art dedicated materials and processes for manufacturing each part to give the best performance/yield otherwise not possible to achieve. In particular, using a separate SOI wafer of a selected thickness for structuring micromechanics can result in better uniformity of the thickness of the mechanical structures (± 0.5 µm BESOI, ± 0.05 µm SMARTCUT) as compared to structures fabricated by the timed etching in which case thickness variation can be of 5 µm across a wafer[28]. An optical part can also benefit from the separation as in this case smoothness of unprotected sidewalls of waveguides is not exposed to a danger of deterioration due to long etching typically required for structuring and release of micromechanics.
The integration of nanophotonic structures with micromechanical systems takes place in the final stage of the fabrication sequence during which the two separate wafers are brought into contact, aligned and securely bonded. Some pre-processing applied to wafers can be advantageous or even indispensable for bonding with success. The actual experience shows that the processes preceding this step do not have to watch bonding that follows, possibly except usage of DRIE. It is experimentally observed that the silicon surface exposed to DRIE etching does not bond[28].
For secure connection of both wafers a direct wafer bonding is the choice. Direct wafer bonding can be applied to Si-Si, SiO_2-SiO_2, Si- SiO_2 and some other configurations. Experience on wafer bonding shows that this process puts heavy demands on the wafers[6]. Stress induced bending of the wafer surface should be below 10 micrometer and the roughness of a wafer surface has to be less than 1 nm in order to be able to bond both wafers. Wafers have to be handled carefully in the clean, preferably Class 1, room to prevent scratching and contamination of the front surfaces, which can destroy a bond.
If no large areas are etched on the MEMS wafer, the wafer is expected to be very flat. This can be supported by a practise of the design of the layout, which allocates about 50% of the wafer surface as contact area (free of features) to guarantee adequate force. A possible residual bond of a SOI wafer can be balanced by an oxide layer of an adequate thickness retained on its backside. The bow of a SOI wafer is mainly induced by the mismatch of thermal expansion coefficient between silicon and oxide, causing excess mechanical stresses in the SOI wafer after annealing at elevated temperatures and subsequent cooling. A simple model that can be used to calculate the optimal thickness of the compensating oxide layer is presented in[29]. For some wafers the necessary thickness of the oxide layer was a few micrometer[28].
Surface smoothness and cleanness is another significant condition for successful wafer fusion bonding. The initial hydrogen bonding that pre-bonds two wafers is weak and operates over a short range, only when the two wafers are very close together. Therefore, having wafers smooth and free with particles are critical prior to bonding. The front side of the mechanical wafer can be protected with a Si_3N_4 layer during most of the processing and should then be very smooth.

Since a CMP process can be applied to the optical wafer, the condition for low roughness is expected to be met easily. Using CMP a SiO_2, Si_3N_4 and Si surface roughness can be reduced to less then 0.2 nm RMS[6]. Prior to bonding, both wafers have to be thoroughly cleaned. To ensure cleanness of the front surfaces during handling a vacuum pen can be used to grab a wafer on its backside whenever applicable.

Bonding and associated with it processes are the only ones that can possibly affect the characteristics of the both parts of the device. The bonding process can affect the optical characteristics of the optical part through the change of refractive index due to the stress induced and through the misalignment of both parts. Bonding Si-Si and SiO_2- SiO_2 introduces little or no thermal stress because of the well-matched thermal expansion between the bonded layers and the fabricated monolithic single crystal structures are completely compatible with subsequent high-temperature process steps, such as oxidation and diffusion[28]. The stress-induced change of refractive index is mostly due to the residual bow of wafers.

Potentially, optical characteristics of waveguiding structures can be affected in the result of the edge erosion during CMP process that precedes bonding[30]. Although not applied directly to the waveguiding layer, CMP rounds edges of features possibly changing geometry of the top section of a waveguide stack and modifying an effective refractive index.

The concept of the process flow (see the Fig 3) that respects the limitations of integration of nanophotonics with micromechanical subsystems is based on the technology developed in MESA+[6]. From the beginning the flow is split into two parallel paths, one for structuring nanophotonic wafer and the other for a mechanical one. Both paths start from an optional thermal oxidization of SOI wafers with the aim to balance the possible residual bow. At the front end of a SOI wafer the oxide layer can be stripped in HF, which is recommended while processing a nanophotonic wafer because tiny shapes of nanophotonic structures can be directly replicated from the photoresist mask onto the silicon layer[21]. Alternatively, it can be retained for masking during subsequent etching, as in the case of a mechanical wafer.

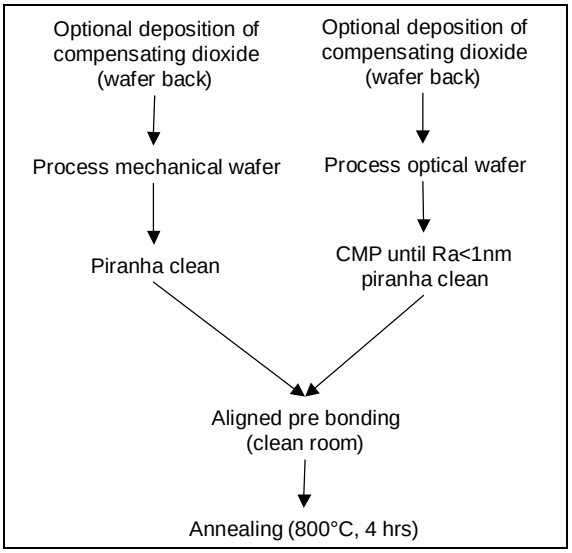

Figure 3: The integration through wafer bonding

The next steps are specific and optimised for separate fabrication of nanophotonic circuits and nano/micromechanical subsystems. After the last process on the front of the mechanical wafer is performed LPCVD deposition of a 60 nm thick [6] protective silicon nitride layer, which follows with the aim to protect the surface during the subsequent handling. When both structuring sequence paths are completed, the Si_3N_4 is removed and the CMP is applied to the front surface of the optical wafer. The CMP uses slightly alkaline slurry containing nanometre-sized silica particles. The combined action of wear and etching yields the smooth surfaces. Subsequent cleaning is performed with polyvinyl alcohol brushes that mechanically wipe the surface of the wafer and remove the abrasive particles. A diluted ammonium hydroxide reduces the electrostatic attraction of the slurry particles to the wafer surface. Bath in piranha, RCA1, RCA2 with de-ionised water rinsing in between completes the cleaning step.

The bonding of both wafers is performed with a double-sided mask aligner. A mask aligner that allows an alignment accuracy of about ±1μm can be used (e.g. EV AL-6, or EV 620) . After bonding, the wafer pair is annealed at an elevated temperature of 800 °C for 4 hours in order to get the final bonding strength, which can be as high as[6] 2 J/m^2.

The experience gained so far in the process of integration as described above concern CMP and aligned bonding. Durable direct Si-Si bonds were performed with ±1μm aligning precision however, stiction problems were reported[6]. They can be solved by a careful design of the device. Other problems, which still are to be investigated, are related to the influence of bonding on optical characteristics of a device. Particularly, stress induced change of refractive index and resultant detuning of spectral characteristics of a final MAPIC device call for thorough examination. So does the edge rounding effect of nanophotonic waveguides due to CMP. Modifications to CMP will be necessary if the examination shows that the effect of rounding cannot be compensated during a design phase. A usage of Fixed Abrasive Pads could be a candidate modification[30]. The balancing of a wafer bow via thermal oxidization, although reported in literature[28], requires experimental examination with various wafers.

3.2. Single wafer approach

In the other concept the fabrication process starts from a single SOI wafer and the bulk micromachining is used followed by a surface micromachining which involves sequence of layer deposition processes, all completed by sacrificial layer etching leading to formation of a freestanding mechanical components. The bulk micromachined SCS components have no residual stress or stress gradients if high doping levels and deposited thin films are avoided. However, this process has limitations in the geometrical shapes that can be formed which restrict some MEMS designs. On the contrary, surface micromachining has the capability to fabricate arbitrary geometries in the plane of the wafer, including the ability to release structures and rotate them out of the plane of the wafer. It can involve as many layers as is needed with a different mask (producing a different pattern) on each layer[31]. Surface micromachining has not been optimised for optical applications. Optical components fabricated using this process often exhibit both static curvature induced by residual stress and stress gradients in the deposited films, and dynamic curvature, associated with bending of thin elements subjected to high accelerations[31]. Nanophotonic components if they were located in the top SCS layer would require about a quarter of micrometer layer thickness to allow formation of single mode waveguiding structures, which is then incompatible with micrometer sized mechanical components. The 10-nanometre accuracy required for photonic subsystems call for the use of a highly precise lithography like a direct write Gaussian beam e-beam, deep-UV or nanoimprint lithography techniques, while the microactuator part may be patterned using standard optical lithography. The silicon nanowaveguides should exhibit extremely low sidewall roughness, especially required for high Q-factor microresonators. SOI etching deep into the buried oxide layer has shown the effect of unacceptable increase of the sidewall roughness. The massive etch of a sacrificial layer required for the release of mechanical components can be similarly aggressive.

The advantage of the use of surface micromachining is that the spacing between planes (and vertically stacked components) is formed through depositions (or growth) of intermediate layers. If necessary, thickness of such layers can be controlled with great precision, better than the precision of lateral spacing of any shapes determined by accuracy and resolution of lithography. Masks can be aligned with ± 0.25 μm tolerance[32] in standard optical lithography.

The practical solution that trade-offs the factors discussed above is a design strategy which makes critical photonic components fixed and locates them in the SCS layer of the base SOI wafer, so they will be processed according to the bulk micromachining procedure and even sealed from the subsequent processing. Fixed mechanical and actuated photonic and mechanical components can be designed stacked over the SOI wafer and formed in deposited layers by surface micromachining. Hence, a combination of different structuring techniques can be used, with the surface micromachined layers formed using conventional methods, and the bulk micromachined layer (with nano-photonic components) created using more precise techniques. If the best performance extra photonic layer is required a usage of an epitaxial lateral overgrowth process should be considered. This concept capitalizes on the benefits, yet avoids the weaknesses, of these two different processes and materials used.

In order to fabricate a practical mechano-photonic device of which the mechanical components are actuated in the vertical plane at least seven deposition (or growth) processes have to be executed, most of them followed by a selective etch, to form components that constitute the device: fixed and actuated nanowaveguides, membranes, anchors and dimples, actuators etc. The cross section through the device is depicted in the Fig 2.

The high precision required for structuring the critical photonic components in the bulk micromachining process can be achieved by the means of a high resolution lithography followed by a shallow SCS etch. The direct e-beam writing is a well mastered but rather slow patterning technique and thus, it can be considered as a main tool in the development phase, to be replaced with mass production compatible process. From the other side, the character of the nano-photonic pattern is well e-beam suited and thus relatively fast pattern definition of this part of the device may be expected. The technique, which seems to be the most prospective for this purpose is nanoimprint.

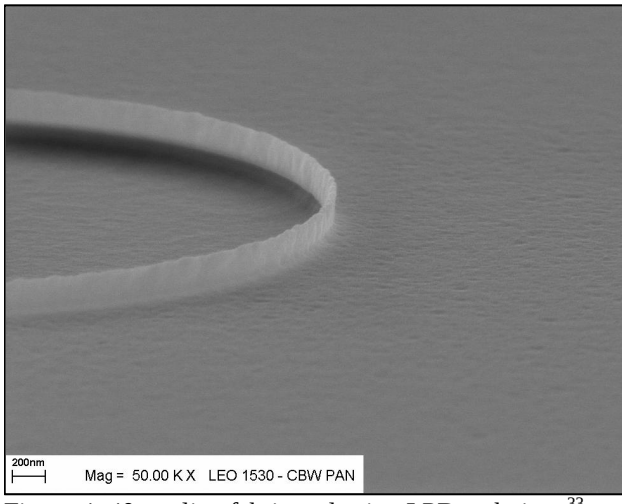

Figure 4: 40 nm line fabricated using LPD technique[33].

This technique has a potential to be precise, inexpensive and fast enough for industrial applications however, fabrication of the template still remains a critical issue. An alternative process, which shall be considered as a back-up solution in some specific cases, is a newly developed so called Lateral Pattern Definition (LPD) technique capable of manufacturing of nanometre-sized structures (Fig 4).

Shallow etch, only through the SCS layer, provides acceptably low sidewall roughness of the nanowaveguides. Enhancement to the resultant surface roughness can be achieved by means of two techniques, special, low temperature oxidation and wet chemical polishing by combination of oxidising and oxide etching agents.

It is necessary to level the topography created by the massive etching the SCS during the bulk micromachining. Planarisation can be performed using chemical mechanical polishing (CMP). In the result of the edge erosion during CMP optical characteristics of waveguiding structures can be potentially affected[30].

The holes and trenches cut in SCS have to be filled in before glamorisation. One interesting possibility when using dioxide for the fill is that, if retained, it can additionally allow UV trimming the optical characteristics of the device. Retaining a dioxide around silicon waveguides can be even more advantageous. Sidewall smoothness can benefit from the elimination of deep etching, which is aimless if oxide deposition is to follow. The fixed photonic components remain sealed from the agents used during the next processing. On the other side, the presence of the dioxide reduces the index contrast between the core and the cladding. One consequence is that radii of bends cannot be as small as with air cladding for increased radiation loss.

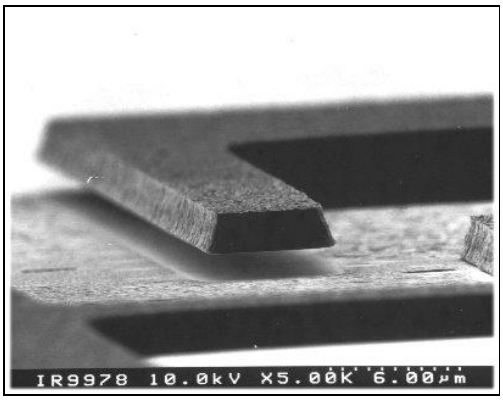

Figure 5: Well-controlled stress in LPCVD deposited freestanding silicon structures.

Two extra layers have to be deposited before the actuated components can be defined. These are the sub-micrometer thick buffer and the few micrometer thick sacrificial layers. The sacrificial layer fixes the standby distance (no actuation) between fixed and actuated photonic components. The buffer layer dictates the minimum distance between these components under conditions of a maximum actuation. The sacrificial layer will be etched away during release of mechanical components and the buffer one should retain and even withstand CMP process (can be a stop layer CMP), so they require different materials. Both should provide flat surfaces of a well controllable thickness.

On the sacrificial layer an optically active material (waveguiding, lossy or dielectric) of desired characteristics has to be deposited. A high optical quality is required if the layer has to perform optical functions but attenuation. Single crystal silicon and amorphous silicon can be a material of choice for a layer where photonic structures require high light confinement, like nanowires or microrings. SCS cannot be grown directly on a sacrificial layer due to lattice constant mismatch. However, if contacts to underlying SCS layer (or deeper to the substrate) are etched a well-controlled SCS layer can grow starting from the contact spot in the Epitaxial Lateral Overgrowth (ELO) process[34]. The new layer preserves the same crystallographic characteristics as the parent layer. In particular, dependent on the crystal orientation, excellent parallel layers can be fabricated. The thickness of an ELO layer can be controlled within sub-micrometer to micrometer range. Alternatively, an amorphous silicon material can be deposited. Although as low as 0.7 dB/cm losses for amorphous silicon were shown elsewhere, the scattering discovered to be the minority loss in bulk samples[1] can be more severe in nanowires due to possibly high sidewall roughness. It has to be noted furthermore, that properties of the a-Si depends strongly on the layer formation technique and process parameters. Typically a-Si is chemically deposited in LPCVD or PECVD processes. The latter of the processes has an important advantage to produce a hydrogen rich a-Si films. Hydrogen, saturate dangling bonds present in the amorphous silicon structure and thus reduce optical scattering.

On the top of the structure the mechanical components are defined. Polysilicon is typically a material of choice. However, when amorphous silicon is deposited first to form a layer for the actuated waveguiding structures it can recrystalise during subsequent deposition of polysilicon. In such a case, a PECVD of amorphous silicon, also for the mechanical components, is the right choice. The mechanical components to be released need anchoring to the wafer. Anchors can be made through etching holes deep into the silicon substrate and subsequently filling them a polysilicon during a common polysilicon deposition step. If an electric isolation is necessary, as in the case of electrostatically driven actuators, the anchors can be made only to the buried oxide while the neighbouring top SCS can be cut.

On the basis of the experience with micromachining the concept of the single wafer process flow has been formulated. It is depicted in the Fig. 6. There are 16 steps and 8 masks involved. The process uses SOI wafers with 0.25 μm thick SCS layer on top on the at least 2 μm buried silicon dioxide[21]. The sequence begins with the deposition of a Si_3N_4 buffer layer. Its thickness is set to the minimum gap required between fixed photonic components, located in the top SOI layer, and the actuated components which will be vertically stacked over the fixed ones. Then selective etch (1-st mask) is performed through the SCS to form the fixed high contrast ratio waveguiding components. This step is followed by the second SCS etch (2-nd mask) which is mainly to cut large areas in SCS while the preceding step cuts with precision only trenches and holes of similar dimensions to avoid loading effects. During the next steps the cut SCS areas are filled with boron doped germanosilica dioxide by means of plasma enhanced chemical vapour deposition (PECVD) then planarised using chemical mechanical polishing (CMP) for which a silicon nitride layer retained on top of photonic components (and uncut SCS areas) serves as a polishing stop. On the polished surface a TiW sacrificial layer is deposited by magnetron sputtering. Thickness of this layer is set to the designed standby distance between fixed and actuated photonic components.

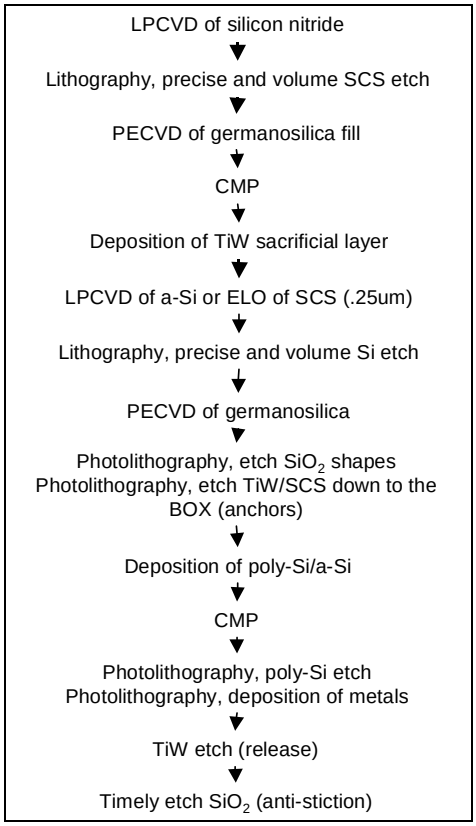

Figure 6: Single wafer process flow

The next steps are for the structuring actuated components of the device. A 0.25 μm thick monocrystalline silicon layer is formed by means of the epitaxial lateral overgrowth (ELO) starting from opened to the top SCS. Alternatively, this layer can be formed from amorphous silicon in an LPCVD process. A selective etches, a precise (3-th masks) and a volume (4-th mask), are used to yield waveguiding structures that will be actuated in the vertical direction after the final release process. A 2 μm boron doped germanosilica is deposited (PECVD), then it is patterned (5-th mask) in a standard photolithography end etched to form blocks of a dielectric required for device control or necessary to prevent excessive mode leakage from actuated waveguides to an actuator. Then, windows are opened to the BOX layer (6-th mask) in order to allow subsequent formation of anchors. In the next step polysilicon is deposited in the low stress optimised LPCVD process. Alternatively, amorphous silicon is deposited through PECVD. It will be used for static and actuated mechanical structures. Excessive material is mechanically removed using CMP, which provides a flat surface for further lithography. The 7-th mask is used for patterning the silicon and the mechanical components are cut. The last mask (8-th mask) is used to open windows in silica blocks where metals have to be deposited. Then the sacrificial layer is etched away in H_2O_2/HCl, which releases the mechanical components. The process flow ends with the timely etch of SiO_2 which removes a thin silica layer from the regions that where mechanically contact can occur during actuation. This prevents sticking effects during operation.
Structuring silicon is performed through plasma etching using ICP plasma source and SF6 chemistry.
The success of this concept is believed to be backed by the partial results obtained so far. Particularly, the technology that allows fabrication of nanophotonic circuits on semiconductor substrate was developed during the EC project NAIS[5]. The ability of the Lateral Pattern Definition (LPD) to provide as narrow as 40 nm silicon lines was proven[33], which shows that this technique can be considered for patterning submicron scale shapes, at least of some type. PECVD technology was optimised for deposition of low loss amorphous silicon. The preliminary results showed that the absorption peak at 1.51 μm (Si-H vibration) became undetectable in 0.5 μm thick films. Optical losses of the fabricated waveguides[35] were about 2 dB/cm, quite satisfactory for straight nanowaveguides. Single crystal silicon 0.2 micrometer thick layers were grown using Epitaxial Lateral Overgrowth technique[34].
Although many of the technological steps designed in the process flow from the Fig 6 have been used in similar configurations their applicability to provide a MAPIC on a single wafer basis has to be proved yet. The open issues are related to the stress induced in thin films by deposition of next layers and possibly to the influence of the high temperature necessary for some further processing. In particular, a UV sensitivity of the germanosilica material can

change when high temperatures are used after it has been deposited. Like in the two wafer concept, detuning of spectral characteristics of a final MAPIC in the result of stress induced change of refractive index as well as the edge rounding effect of nanophotonic waveguides due to CMP, call for thorough examination.

3.3. Trimming procedure

In fact, patterning accuracy required from the optical point of view is higher than achievable using existing tools, especially if the device contains resonant cavities (e.g. microring). To solve this problem a special trimming procedure is considered, changing optical properties of the optical elements in the post-processing manner in the final phase of the fabrication process. The difficult challenge here is to achieve this goal without sacrificing mass production compatibility. The extensive experience with UV induced change of refractive index in SiO_2 can be exploited for the trimming of nanophotonic components fabricated on SOI.

The photosensitivity of planar waveguides is quite complex and consists of contributions from different processes, like colour-centre formation, stress relaxation and compaction. A large compressive stress at the germanosilica – silicon interface plays here an important role, but due to complicated microstructure the relaxation of this stress upon UV irradiation can be accompanied by localised compaction and positive index change. Usually the UV sensitivity is quite low and the method commonly used in germanium doped fibre cores to increase it is so called hydrogen loading. Unfortunately this method is not very convenient for planar devices, where top cladding is to be UV-sensitive, because hydrogen can escape from the sample before all the devices are UV processed. Boron co-doped germanosilica is a promising candidate to solve this problem (see Fig 7)[34].

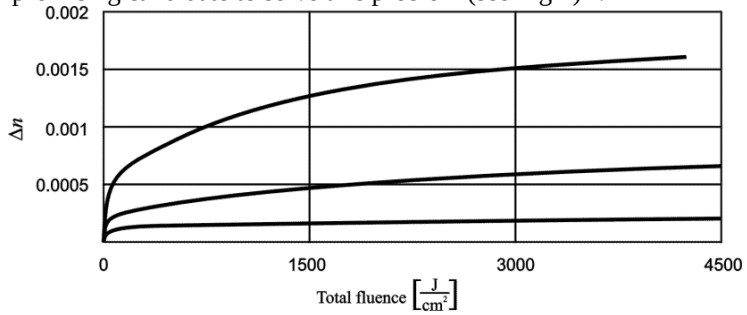

Figure 7: Variation of the refractive index in the germanium doped, boron co-doped waveguide core upon UV exposure at 248nm. Pulse energy density 30mJ/cm2. Curves present from bottom: pure Ge-doped material, 2 at% B co-doped, 5 at% B co-doped

A fine wavelength adjustment of the fabricated components can be are done by selective modification of the silica in the vicinity of the critical parts of the nanophotonic circuit. The output from the device can be monitored during the illumination and the process is stopped when the matching is reached. The method was tested for balancing a planar Mach-Zehnder interferometer[36]. It was possible to introduce a several p phase shift by illuminating a 5 mm long element of arm by 193 nm light from the excimer laser.

4. CONCLUSIONS

The integration of nanophotonics and micro/nano-mechanics opens the route to a new class of devices with specifications not achieved by other methods. Nanophotonics on its own has the potential of VLSI photonics. On the foundation of joint experience acquired by a consortium formed by Lublin University of Technology, MESA+, KTH, Institute of Electron Technology, Heinrich Hertz Institute, Slovak Academy of Sciences and Lionix BV the roadmap to the desired single technological platform for fabrication of mechanically controlled photonic integrated circuits using Silicon-on-Insulator was defined. Two concepts were formulated: (1) manufacturing separately the photonic and mechanical parts and then bonding them with precision and, (2) fabricating all components of the system i.e. waveguides and actuators starting from one SOI wafer using a hybrid bulk and surface micromachining. In any of the two approaches the fabrication sequence is complemented with a trimming procedure, which corrects the fabrication inaccuracies, which can result if required patterning accuracy cannot be achieved using existing tools.

The candidate processes were selected and process flows designed. Although the processes have not been fully realized, the success of the both concepts is believed to be backed by the partial results obtained so far. They concern the key processes required: wafer bonding, chemical mechanical polishing, low stress optimised deposition of amorphous silicon, polysilicon and silica, epitaxial lateral overgrowth of silicon, UV induced modification of refractive index in doped silica. The open issues are related to the detuning of spectral characteristics of a final MAPIC device in the result of stress induced change of refractive index as well as the edge rounding effect of nanophotonic waveguides due to chemical mechanical polishing.

REFERENCES

1. *Harnessing the speed of light*, The IST Optimist EU photonic roadmap, Optimist brochure edition date: June 2004.
2. B.E. Little, S.T. Chu, H.A. Haus, J. Foresi and J.P Laine, *Microring resonator channel dropping filters*, J. Light Wave Techn. 15, 998-1005, 1997.
3. B.E. Little, S.T. Chu, W. Pan, Y. Kokubun, *Microring resonator arrays for VLSI* photonics, Phot. Techn. Letters 12, 323-325, 2000.
4. A. Driessen, F. Michelotti, *Microresonators as Building Blocks for VLSI Photonics*, edited by M. Bertolotti, AIP Conference Proceedings 620, Melville, New York, 2004.
5. http://www.mesaplus.utwente.nl/nais/
6. G.J. Veldhuis, T. Nauta T, C. Gui, et al., *Electrostatically actuated mechanooptical waveguide ON-OFF switch showing high extinction at a low actuation-voltage*, IEEE Journal of Selected Topics in Quantum Electronics 5 (1): 60-66 Jan-Feb 1999.
7. K. Djordjev, S-J. Choi, S-J. Choi, P. D. Dapkus, *Microdisk Tunable Resonant Filters and Switches*, IEEE Photonics Technology Letters, Vol. 14, No. 6, June 2002.
8. T. A. Ibrahim, R. Grover, L.-C. Kuo, S. Kanakaraju, L. C. Calhoun, P.-T. Ho, *All-Optical AND/NAND Logic Gates Using Semiconductor Microresonators*, IEEE Photonics Technology Letters, Vol. 15, No. 10, October 2003.
9. V. R. Almeida, C. A. Barrios, R. R. Panepucci, M. Lipson, *All-optical control of light on a silicon chip*, Nature, Vol. 431, 28 October 2004.
10. C. A. Barrios, M. Lipson, *Modeling and analysis of high-speed electro-optic modulation in high confinement silicon waveguides using metal-oxide-semiconductor configuration*, Journal of Applied Physics, Vol. 96, No. 11, 1 December 2004.
11. D. Geuzebroek, E.J. Klein, H. Kelderman, N. Baker and A. Driessen, *Compact wavelength-selective switch for Gigabit filtering in access networks*, IEEE Photonics Technology Letters, 17, 336-338, 2005.
12. K. Djordjev, S-J. Choi, S-J. Choi, P. D. Dapkus, *Vertically Coupled InP Microdisk Switching Devices with Electroabsorptive Active Regions*, IEEE Photonics Technology Letters, Vol. 14, No. 8, June 2002.
13. W. Lukosz, *Integrated optical nanomechanical devices as modulators, switches, and tunable wavelength filters, and as acoustical sensors*, Proc. SPIE, vol. 1793, 1992.
14. Gregory N. Nielson, Dilan Seneviratne, Francisco Lopez-Royo, Peter T. Rakich, Ytshak Avrahami, Michael R. Watts, Hermann A. Haus, Harry L. Tuller, George Barbastathis, *Integrated Wavelength-Selective Optical MEMS Switching Using Ring Resonator Filters*, IEEE Photonics Technology Letters, Vol.. 17, No. 6, June 2005.
15. Veldhuis GJ, Gui C, Nauta T, Koster TM, Berenschot JW, Lambeck PV, Gardeniers JGE, Elwenspoek M, *Mechano-optical waveguide on-off intensity modulator*, Optics Letters 23 (19): 1532-1534 Oct 1, 1998.
16. H. A. Haus, L. C. Kimerling, M. Romagnoli, *Application of High Index Contrast Technology to Integrated Optical Device*, exp in search of innovation, Telecom Italia Lab, Volume 3 - n. 4 - December 2003.
17. M.-C. M. Lee and M. C. Wu, *A MEMS actuated tunable microdisc resonator*, Proc. 2003 IEEE/LEOS Conf. on Optical MEMS, pp. 28-29, Hawaii, 2003.
18. W. A. Johnson, L.K. Warne, *Electrophysics of Micromechanical Comb Actuators*, J. MEMS, 4, pp. 49-59, 1995.
19. http://www.littleoptics.com/
20. http://www.lionixbv.nl/
21. W. Bogaerts, V. Wiaux, P. Dumon, D. Taillaert, J. Wouters, S. Beckx, J. Van Campenhout, Bert Luyssaert, Dries Van Thourhout, R. Baets, *Large-scale production techniques for photonic nanostructures*, Proc. SPIE (invited), 5225, United States, p.101-112, 2003.
22. P. Dumon, W. Bogaerts, V. Wiaux, J. Wouters, S. Beckx, J. Van Campenhout, D. Taillaert, B. Luyssaert, P. Bienstman, D. Van Thourhout, R. Baets, *Low-loss SOI Photonic Wires and Ring Resonators Fabricated with Deep UV Lithography*, IEEE Photonics Technology Letters, 16(5) p.1328-1330, 5/2004.
23. G. Sunada, *MicroElectroMechanical Systems*, Selected Topics in Assurance Related Technologies, Vol 8, No 1, 2001, http://rac.iitri.org/DATA/START.
24. M. Dainese, M. Swillo, L. Thylen, M. Qiu, L. Wosinski, B. Jaskorzynska and V. Shushunova *Narrow Band Coupler Based on One-Dimensional Bragg Reflection Waveguide*, Proceedings of the 2003 Optical Fiber Communication Conference, March 23-28, 2003, Atlanta, Georgia, vol.1, 44-46, 2003.

25. Z.J. Zawistowski, B. Jaskorzynska, *Electrically tunable filter based on directional coupler with 1D photonic crystal arm infiltrated with smectic liquid crystal*, Proceedings of 2004 6th International Conference on Transparent Optical Networks (IEEE Cat. No.04EX804), pt. 2, p 127-30 vol.2, 2004.
26. K. Domanski, P. Janus, P Grabiec, R. Perez, N. Chaillet, S. Fahlbusch, A. Sill, S. Fatikow, *Design, fabrication and characterization of force sensors for nanorobot*, Microelectronic Engineering, Vol. 78-79 (Special Issue), March 2005.
27. P. Hudek, I. Rangelow, I. Kostic, G. Stangl, P. Grabiec, E. Rangelow, M. Belov, F. Shi, *Chemically Amplified Deep UV Resists for Micromachining Using Electron Beam Lithography and Dry Etching*, in: S*ensor & Packaging*, ÖVE, Wien, Austria, 2003, ISBN: 3-85133-032-3.
28. L. Zhou1, J. M. Kahn, K. S. Pister1, *Scanning Micromirrors Fabricated by an SOI/SOI Wafer Bonding Process*, submitted to IEEE Journal of Microelectromechanical Systems, February 2005.
29. H. C. Liu, S. P. Murarka, *Elastic and viscoelastic analysis of stress in thin films*, Journal of Applied Physics, vol. 72, no. 8, P3458-63, 1992.
30. M. Kulawski, *Polishing of ground Silicon Polishing of ground Silicon Wafers with Fixed Abrasive Wafers with Fixed Abrasive Pads*, presented at the 9th CMP User Meeting, Neuss, October 25th 2002.
31. J. Kubby, *Hybrid silicon-on-insulator micromachining for critical MEMS components*, Solid State Technology, September, 2004.
32. R. Grover, P. P. Absil, V. Van, J. V. Hryniewicz, B. E. Little, O. King, F. G. Johnson, L. C. Calhoun and P.-T. Ho, *Vertically coupled GaAs-AlGaAs and GaInAsP-In microring resonators*, Optics Letters, Vol. 26, Issue 8, April 2001.
33. P. Grabiec, M. Zaborowski, K. Domański, T. Gotszalk, I. Rangelow, *Nano-with lines using latteral pattern definition technique for nanoimprint template fabrication*, Microelectronic engineering, vol. 73-74, 2004.
34. I. Jozwik, J. Kraiem, J.M. Olchowik, A. Fave, D. Szymczuk, A. Zdyb, *Epitaxial lateral overgrowth of Si on patterned Si substrates by liquid phase epitaxy*, Molecular Physics Reports 39, 85, 2004.
35. L. Wosinski, *Silica-on-Silicon technology for photonic integrated devices*, proceedings of the 6th International Conference on Transparent Optical Networks: ICTON 2004, Wroclaw, Poland, July 4 - 8, 2004.
36. L. Wosinski, M. Swillo, M. Dainese, *Imprinting of low dispersion Bragg gratings in planar devices for 40 Gbps DWDM systems*, paper 5956-14 at this conference.