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SiC MOSFET and GaN FET in high voltage switching applications

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ABSTRACT:
For several decades, silicon-based semiconductor devices, such as Si MOSFETs have been the main choice for switching applications. However, their level of performance is approaching its maximum potential, and further development becomes increasingly challenging. As a result, semiconductor manufacturers and the electronics industry are exploring new technologies to meet current requirements.

One promising option is the use of WBG (Wide Band Gap) devices, such as GaN FETs and SiC MOSFETs, which have gained attention due to their superior performance characteristics. Compared to traditional Si transistors, WBG devices can withstand higher voltages and temperatures, are faster, can be packed in smaller sizes, and are more efficient.

This study aims to serve as a guide for designers seeking information on the technology and usage of WBG transistors, particularly in high voltage switching applications. The study includes an examination of the structures of SiC MOSFETs and GaN FETs, as well as their most important electrical characteristics. Additionally, the efficiency of an LCC converter was measured to compare the performance of various FET types, with a specific interest in the use of WBG devices in soft switching applications.

Scientific articles, application notes, and datasheets were investigated to provide a thorough understanding of the theory behind SiC MOSFETs and GaN FETs. According to resources, the primary SiC MOSFET and GaN FET technologies suitable for high voltage switching are planar SiC MOSFET, trench SiC MOSFET, p-GaN FET and GaN/Si cascode transistor. These devices are currently available with breakdown voltages of 1700 V (planar SiC MOSFET), 2000 V (trench SiC MOSFET), 650 V (p-GaN FET) and 900 V (GaN/Si cascode transistor).

The efficiency of an LCC converter with a maximum output power of 40 W was measured using 1500 V Si MOSFET, 1700 V planar SiC MOSFET, 1700 V trench SiC MOSFET, and 900 V GaN/Si cascode transistor. A constant load of 1 A was used, and the input voltage was incrementally increased from 300 V to 900 V in 100 V steps. According to results, using planar and trench SiC MOSFETs, LCC converter had the highest efficiency, reaching up to 89,6 % while Si MOSFET exhibited slightly lower efficiency, which was 87,7 % at its best. GaN/Si cascode transistors showed comparable efficiency to SiC MOSFETs at lower input voltages but fell significantly behind as the voltage increased, having eventually much worse efficiency than Si MOSFET.

KEYWORDS: WBG transistor, GaN FET, SiC MOSFET

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TIIVISTELMÄ:
Useiden vuosikymmenien ajan pii-pohjaiset puolijohteet, kuten pii MOSFETit, ovat olleet pääasiallinen teknologia katkojasovelluksissa. Niiden suorituskyky lähestyy kuitenkin ylärajaa, ja niiden kehittäminen käy yhä vaikeammaksi. Tämän vuoksi puolijohdevalmistajat ja elektroniikkateollisuus etsivät uusia teknologioita täyttää nykyiset vaatimukset.

Yksi lupaava teknologia ovat laajan energiavyön puolijohteet, kuten galliumnitridi FETit ja piikarbidi MOSFETit. Viime vuosina ne ovat herättäneet paljon huomiota niiden ylivoimaisten ominaisuuksien vuoksi. Verrattuna perinteisiin pii MOSFETeihin, laajan energiavyön transistorit kestävät suurempia jännitteitä ja lämpötiloja, ovat nopeampia ja ne voidaan pakata pienempään kokoon. Lisäksi ne ovat tehokkaampia.

Tämä diplomityö pyrkii toimimaan oppaana elektroniikkasuunnittelijoille, jotka etsivät tietoa laajan energiavyön transistoreista ja niiden käytöstä erityisesti suurjännitekatkojasovelluksissa. Työssä tarkastellaan piikarbidi MOSFETien ja galliumnitridi FETien rakenteita sekä niiden tärkeimpiä sähköisiä ominaisuuksia. Lisäksi mitattiin kelaan ja kahteen kondensaattoriin perustuvan LCC resonanssiteholähteen hyötysuhde eri FET-tyypeillä, koska haluttiin saada tietoa laajan energiavyön transistorien käytöstä pehmeässä jännitteen katkonnassa.

Tiedon keräämiseksi tutkittiin tieteellisiä artikkeleita, sovellusohjeita ja datalehtiä. Lähdeaineiston perusteella pääasialliset piikarbidi MOSFETien ja galliumnitridi FETien teknologiat suurjännitesovellusten alueella ovat planaarinen piikarbidi MOSFET, erityiseen kaivanto teknologiaan (trench) perustuva piikarbidi MOSFET, p-tyypin galliumnitridi FET ja galliumnitridi/pii kaskadi transistori. Tällä hetkellä näitä teknologioita on kaupallisesti saatavilla enimmillään 1700 V (planaarinen piikarbidi MOSFET), 2000 V (kaivanto piikarbidi MOSFET), 650 V (p-tyypin galliumnitridi FET) ja 900 V (galliumnitridi/pii kaskadi transistori) jännitteillä.

Nimellisteholtaan 40 W LCC resonanssi teholähteen hyötysuhde mitattiin 1500 V pii MOSFETeilla, 1700 V planaarisilla piikarbidi MOSFETeilla, 1700 V kaivanto piikarbidi MOSFETeilla ja 900 V gallium-nitridi/pii kaskadi transistoreilla. Kuormana käytettiin 1 A vakiokuormaa ja tulojännitettä nostettiin asteittain 300 voltista 900 voltiin 100 voltin nostoin. Tulosten mukaan paras hyötysuhde oli 89,6 %, joka mitattiin planaarisella piikarbidi MOSFETilla ja kaivanto piikarbidi MOSFETilla. Pii MOSFETien tapauksessa hyötysuhde oli hieman huonompi, ollen parhaimmillaan 87,7 %. Alhaisilla jännitteillä galliumnitridi/pii kaskadi transistorien hyötysuhde oli verrattavissa piikarbidi MOSFETeihin, mutta hyötysuhde laski jännitettä nostettaessa, ollen lopulta merkittävästi huonompi kuin pii MOSFETeilla.

Avainsanat: WBG transistor, GaN FET, SiC MOSFET

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Symbols

η	Efficiency
g_m	Transconductance

Abbreviations

BV_{DS}	Drain-to-Source Breakdown Voltage
B	Base
B	Body
BJT	Bipolar Junction Transistor
C	Collector
C_{GD}	Gate-to-Drain Capacitance
C_{GD_GaN}	Gate-to-Drain Capacitance of GaN FET
C_{GD_Si}	Gate-to-Drain Capacitance of Si MOSFET
C_{GS}	Gate-to-Source Capacitance
C_{GS_GaN}	Gate-to-Source Capacitance of GaN FET
C_{GS_Si}	Gate-to-Source Capacitance of Si MOSFET
C_{iss}	Input Capacitance
$C_{O(ER)}$	Energy-Related Effective Ouput Capacitance
C_{OSS}	Output Capacitance
C_{OSS_GaN}	Output Capacitance of GaN FET
C_{OSS_Si}	Output Capacitance of Si MOSFET
C_{RSS}	Reverse Transfer Capacitance
C_S	Secondary Side Resonance Capacitor
$C_1 \ldots C_2$	Primary Side Resonance Capacitors
$C_3 \ldots C_4$	FET Parallel Capacitors
D	Drain
D_B	Body Diode
DC	Direct Current
DPAK	Decawatt Package
E	Emitter

E_{OSS}	Energy Stored in Output Capacitance
FET	Field-Effect Transistor
f_{SW}	Switching Frequency
G	Gate
HEMT	High Electron Mobility Transistor
I_A	Avalanche Current
I_D	Drain Current
$I_{D(SAT)}$	Drain Saturation Current
IGBT	Insulated Gate Bipolar Transistor
I_{off}	Current During Turn-Off
I_{on}	Current During Turn-On
I_{SD}	FET Reverse Current
I_{rr}	Reverse Recovery Current
I_S	Body Diode Current
I_{in}	Input Current
I_1	Displacement Current
JFET	Junction-Gate Field-Effect Transistor
L_S	Leakage Inductance
P_{CON}	Conducting Loss
P_D	Dead Time Loss
PQFN	Power Quad Flat No-Lead
P_{rr}	Reverse Recovery Loss
P_{SW}	Switching Loss
Q_G	Gate Charge
Q_{HS}	High-Side FET
Q_{LS}	Low-Side FET
Q_{rr}	Reverse Recovery Charge
R_B	Base-Emitter Resistance
R_{CH}	Channel Resistance
R_{dg}	Drain-Gate Resistance

R_{drift}	Drift Region Resistance
R_{DSON}	On-State Resistance
$R_{DSON(REV)}$	FET Reverse Conducting Resistance
R_{Gint}	Internal Gate Resistance
R_L	Load Resistance
R_{sg}	Source-Gate Resistance
R_{sub}	Substrate Resistance
$R_{TH(JA)}$	Junction-to-Ambient Thermal Resistance
$R_{TH(JC)}$	Junction-to-Case Thermal Resistance
SBD	Schottky Barrier Diode
SJ	Super Junction
SMPS	Switched Mode Power Supply
SW	Switch
SWN	Switching Node
TO	Transistor Outline
t_D	Dead Time
T_j	Junction Temperature
t_{off}	turn-off time
t_{on}	turn-on time
t_{rr}	Reverse Recovery Time
T_1	Transformer of LCC Resonant Converter
V_{DD}	DC Voltage Source
V_{DS}	Drain-to-Source Voltage
V_{Drr}	Body Diode Reverse Voltage
V_{GS}	Gate-to-Source Voltage
V_{DS_Si}	Drain-to-Source Voltage of Si MOSFET
V_{GS_GaN}	Gate-to-Source Voltage of GaN FET
V_{in}	Input Voltage
V_L	Load Voltage
V_{SD}	FET Reverse Voltage Drop

V_{SWN}	Switching Node Voltage
WBG	Wide Band Gap
ZCS	Zero Current Switching
Z_{GS}	Impedance of Gate Drive Circuit
ZVS	Zero Voltage Switching
2DEG	Two-Dimensional Electron Gas

1 Introduction

Switched mode power supplies (SMPS) are widely used in both consumer and industrial electronics due to their high efficiency when compared to traditional linear power supplies. In order to minimize power losses and optimize efficiency, the choice of switching device is crucial. Insulated gate bipolar transistors (IGBTs) are commonly used in high-power switching applications such as inverters, but their maximum switching frequency is limited to around 30 kHz (Schulz, 2019, p. 4), which is not ideal for the general switching frequencies required for SMPS (ranging from tens of kHz to several hundred kHz). As power MOSFETs (metal-oxide-semiconductor field-effect transistors) are capable of much higher switching speeds than IGBTs, they are often the preferred choice for SMPS.

Although power MOSFETs have a high switching speed, their voltage blocking capability falls short of that of IGBTs. While SJ (super junction) technology has enabled power MOSFETs to increase their voltage blocking capability, the physical properties of silicon (Si), the basic material used in conventional power MOSFETs, impose limits on their further development. Although there are Si MOSFETs on the market with blocking voltages of several thousand volts, their usage in power converters may not be reasonable if high efficiency is a critical requirement. This is due to the significant increase in on-state resistance of silicon with the blocking voltage, which in turn leads to higher power losses. Thus, those devices are not considered in this work.

To balance the trade-off between voltage blocking capability and on-state resistance, chip size must be increased. However, an increase in chip size results in an increased input capacitance, which in turn decreases switching frequency (Vishay, 2015, p. 1–2). A high switching frequency is desirable as it offers benefits such as a reduced transformer size. With smaller transformers, less copper is required, leading to reduced power losses. Additionally, the increased switching speed allows for smaller capacitors.

Wide bandgap (WBG) technology, such as silicon carbide (SiC) and gallium nitride (GaN), is emerging as a potential alternative to silicon. According to Ravinchandra et al. (2022,

p. 1398–1399), the band gap refers to the minimum amount of energy required to move an electron from the valence band to the conduction band, thereby enabling electrical conduction. The wider the bandgap, the higher the amount of energy that the material can withstand without breakdown. As their name implies, WBG devices have a wider bandgap than conventional silicon devices, allowing them to operate at higher voltages and temperatures than Si MOSFETs. The higher voltage blocking capability of WBG transistors enables them to be packed into smaller chips, reducing junction capacitance, and increasing switching speed. Additionally, WBG transistors have significantly lower on-state resistance than Si MOSFETs of the same chip size. The term “WBG transistor” can refer to any transistor with a wider bandgap compared to Si MOSFET. In the context of this work, it includes SiC MOSFET and GaN FET.

The flyback topology has long been popular for SMPS configurations due to its simplicity and low component count. However, significant switching losses occur during MOSFET turn-on and turn-off. Additionally, parasitic components in the circuit cause oscillation during turn-off transitions, necessitating the use of snubber circuits to dampen the oscillation, which leads to dissipation of energy as heat. To address these issues, soft-switching technique-based topologies, such as LLC and LCC resonant converters, have gained popularity in recent years due to their ability to provide much lower power losses compared to traditional hard-switching topologies like flyback. By combining WBG transistors with soft-switching techniques, the full benefits of modern technology can be realized.

The fundamental structure and electrical characteristics of conventional Si MOSFETs are widely understood by electronics engineers. However, WBG transistors have only recently emerged on the market and there is a limited understanding of their structure and electrical characteristics, as well as their implementation in power supply designs. This thesis is made for Danfoss, with the goal of providing a comprehensive and detailed guide to aid designers in the implementation of power supply designs utilizing WBG transistors. Additionally, there is a particular interest in gaining insight into the usage of

WBG transistors in LCC resonant power supplies. The primary objectives of this research are to clarify:

- What SiC MOSFET and GaN FET technologies are available in the field of high voltage switching applications?
- What kind of electrical characteristics do SiC MOSFET and GaN FET have?
- What is the efficiency of 1350 V LCC resonant converter when comparing Si MOSFET, SiC MOSFET and GaN FET?

Chapter 2 introduces the basic theory of semiconductors and transistors, including a brief overview of different transistor types and the working principle of MOSFETs. Chapter 3 delves into the detailed structure of Si MOSFETs, SiC MOSFETs, and GaN FETs, providing fundamental understanding of their structures to aid in understanding their electrical characteristics. Chapter 4 focuses on the electrical characteristics of these transistors, while also briefly discussing common reliability issues related to WBG transistors. In Chapter 6, the empirical part of the thesis is presented, where the efficiency of LCC resonant converter is tested in a laboratory setting using four different transistor types, and the results are analyzed. Finally, conclusions are drawn in Chapter 7. While the thesis primarily emphasizes SiC MOSFETs and GaN FETs, conventional Si MOSFETs are also discussed throughout to help explain the advantages of WBG transistors.

There is not clear definition of “high voltage switching application”. However, in this work, it refers to applications with DC voltages starting from 300 V. The main interest in this work is for FET technologies which come with as high breakdown voltage as possible while keeping maximum on-state resistance as few Ohms and current rating below 10 A. However, trade-offs are necessary due to the current status of GaN-based transistor technologies.

2 Basics of transistors

A transistor is a semiconductor device that can be utilized for signal amplification or electronic switching. In 1947, Bell Laboratories created the first operational transistor, and in 1958, Fairchild Semiconductor introduced the first high-performance silicon transistor, the 2N697 bipolar junction transistor (BJT) (Grundmann, 2016, p. 788). The first power MOSFETs were introduced in 1976 and have later become a mainstream technology for high-voltage and high-speed switching applications (EPC, 2012, p. 1).

2.1 Semiconductors

A semiconductor is a material that falls between being a conductor and an insulator. Silicon is a typical semiconductor material. In its pure form, silicon does not conduct electricity, but its semiconductor properties can be achieved by adding impurities to its crystal structure, a process called doping. According to Bogart Jr. et al. (2001, p. 727–723), there are two types of doping: n-type and p-type. In n-type doping, a 5-valent dopant like phosphorus (P) replaces some of the silicon atoms, resulting in an extra free electron that can act as a charge carrier. In p-type doping, a 3-valent dopant like boron (B) replaces some of the silicon atoms, creating holes on the valence bands that can also function as charge carriers.

Figure 1 illustrates the crystal structure of a semiconductor. Bogart Jr. et al. (2001, p. 729–730) state that when n-type and p-type materials are brought together, a depletion region is formed at the pn-junction between them. This region lacks charge carriers. When a positive bias voltage is applied between the p-type and n-type regions, an electric field is created in the depletion region, which enables electrons to move from the negatively charged n-type region to the positively charged p-type region. This results in a current flow from a positive potential to a negative potential. However, if the polarity is reversed, electrons and holes move away from the edges of the depletion region, and current flow is blocked.

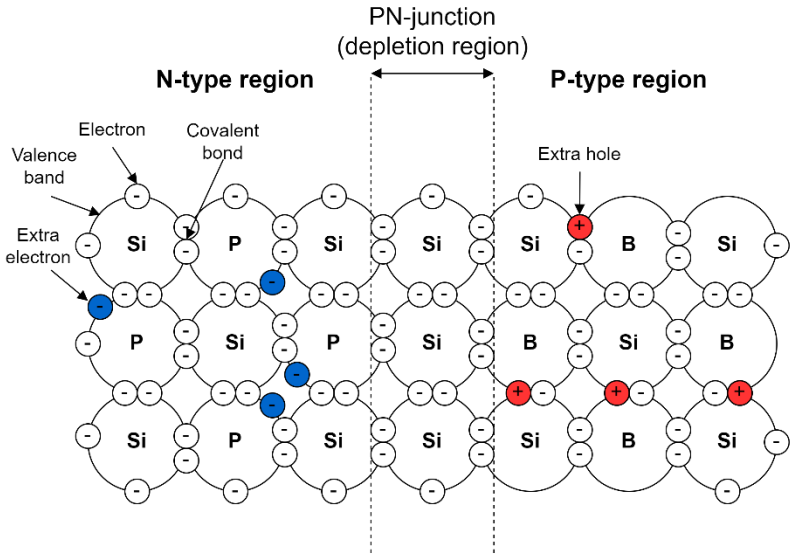

Figure 1. Crystal structure of silicon semiconductor.

Other semiconductor materials besides silicon include for example germanium, silicon carbide, and gallium nitride. The process for gallium nitride semiconductors differs from the others mentioned because it does not involve pn-doping (Sun, 2019, p. 3). Chapter 3 covers a discussion of the physical properties of semiconductor materials that are particularly relevant to this thesis.

2.2 Transistor types

The most common types of transistors include BJTs, IGBTs, and FETs. BJTs can be npn or pnp type while IGBTs and FETs can be n-channel or p-channel type. FETs can be further categorized into MOSFETs, GaN FETs and JFETs (junction-gate field-effect-transistors). According to Horowitz & Hill (2015, p. 134–136) the two operation modes of FET are depletion mode and enhancement mode. In practice, the main difference between the two modes is that a depletion mode FET acts as a normally closed switch, while an enhancement mode FET acts as a normally open switch. While MOSFETs can operate in either mode, JFETs only operate in depletion mode.

Since the behavior of depletion type FETs is not practical for switching applications, enhancement mode MOSFETs are often preferred over JFETs in modern designs. MOSFETs designed for high-voltage and high-current applications are referred to as power MOSFETs. The distinctions between a standard MOSFET and a power MOSFET are discussed in Chapter 3. Figure 2 presents a simplified chart of various types of transistors.

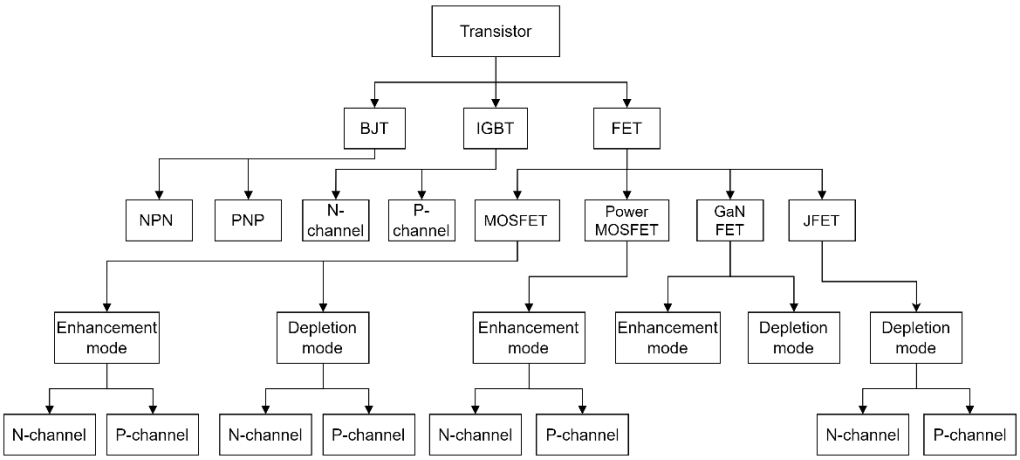

Figure 2. Transistor chart.

JFET and GaN FET has three terminals, which are the drain (D), gate (G), and source (S). MOSFET has the same terminals as well as a fourth terminal, the body (B), which is usually internally connected to the source terminal. BJT has three terminals, which are the collector (C), base (B), and emitter (E). The basic principle for FET and BJT is the same: one terminal controls the current flow between the other two terminals. In the case of FET, the voltage at the gate terminal controls the current flow between the drain and source, whereas in BJT, the current provided to the base terminal controls the current flow between the collector and emitter. IGBT has three terminals: collector, gate, and emitter, making it a combination of FET and BJT. Figure 3 shows the general electrical symbols and locations of the terminals for the different types of transistors.

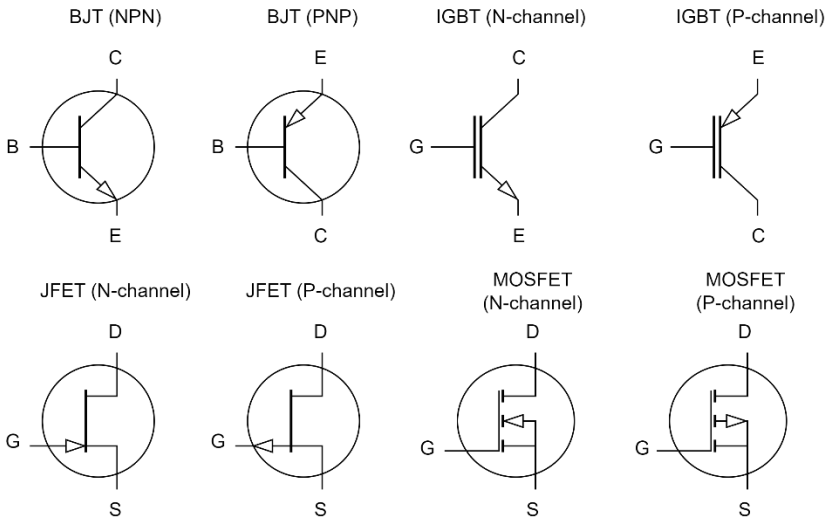

Figure 3. Symbols of most common transistor types.

The schematic symbols for GaN FETs can vary among manufacturers, but generally, the enhancement mode GaN FET can be represented by the same symbol as the enhancement mode n-channel MOSFET (EPC, p. 11, 2012).

2.3 Operation of MOSFET

According to Bogart Jr et al. (2001, p. 214–217), MOSFET operates based on the electric field between the gate and body terminals, with the intensity of the electric field determined by the voltage applied between these terminals. As shown in Figure 4, the enhancement mode n-channel MOSFET consists of heavily doped n-type regions for the drain and source terminals, a p-type substrate for the body terminal, and an insulated gate terminal. When a positive voltage V_{GS} is applied between the gate and source terminals of a transistor, electrons are drawn from the negative potential of V_{GS} to the substrate. As the gate is insulated from the substrate, the electrons accumulate at the interface of the insulator and substrate, creating a channel of electrons between the drain and source terminals. This channel is also referred to as the inversion layer. The channel width increases as V_{GS} increases, and with a sufficiently high voltage bias, the channel

allows the drain current I_D to flow when positive drain-to-source voltage, V_{DS}, is applied between the drain and source. The gate-to-source voltage at which the channel begins to conduct is called the gate-to-source threshold voltage, $V_{GS(TH)}$.

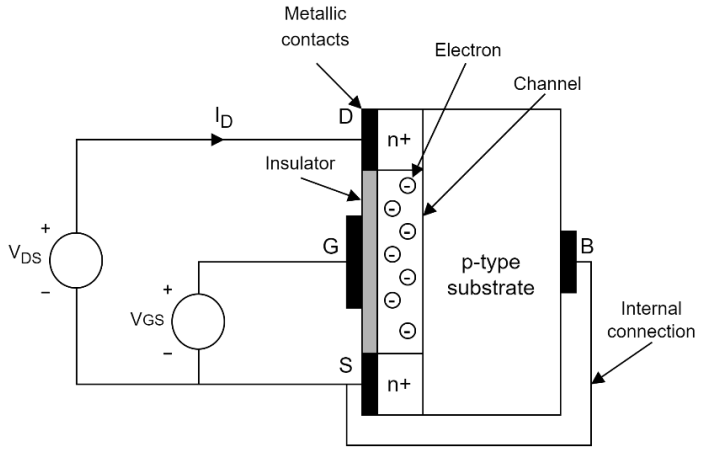

Figure 4. Working principle of enhancement mode n-channel MOSFET.

According to Bogart Jr et al. (2001, p. 214–217), MOSFET can function in two regions: the ohmic region and the saturation region. The principle of I-V characteristics of an enhancement mode n-channel MOSFET are shown in Figure 5. In the ohmic region, the magnitude of I_D relies on both V_{DS} and V_{GS}, with 0 A at cut-off (when $V_{GS}<V_{GS(TH)}$). If V_{GS} is larger than $V_{GS(TH)}$ and kept constant, at high enough V_{DS}, the MOSFET enters the saturation region where the increase in V_{DS} no longer affects the magnitude of I_D. The voltage at which saturation occurs is known as the drain-to-source saturation voltage ($V_{DS(SAT)}$), and the current at that voltage level is called the drain-to-source saturation current ($I_{DS(SAT)}$).

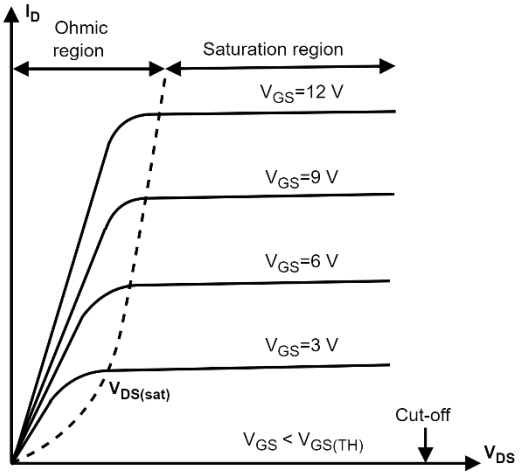

Figure 5. Drain characteristics of enhancement mode n-channel MOSFET (Bogart, Jr. et al., 2001, p. 216).

The operation of enhancement mode p-channel MOSFET is similar to that of n-channel MOSFET, but the drain and source terminals are formed of heavily doped p-type regions, and the substrate is made of n-type material. As a result, the voltages V_{GS} and V_{DS} are negative, and the current I_D flows from the source to the drain (Bogart, Jr et al., 2001, p. 217). The MOSFETs discussed in further chapters are n-channel enhancement mode MOSFETs.

2.4 Transistors in switching applications

Figure 6 demonstrates the principle of a transistor operating as a switch. A load (R_L) is connected in series with a FET (SW), and both are connected to a DC voltage source (V_{DD}). The FET gate is driven by voltage pulses which, when in a high state, turn the FET on, and when in a low state, turn it off. The voltage across the load is determined by the duty cycle of the voltage pulses used to drive the FET.

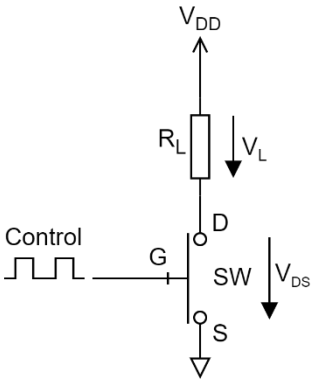

Figure 6. Transistor as a switch.

Two primary techniques for switching applications are hard switching and soft switching. Figure 7 depicts the principle and formation of switching losses in (a) hard switching and (b) soft switching. As per the figure, during hard switching, the FET is turned on when V_{DS} corresponds to its maximum value, whereas in soft switching, the FET is turned on with zero voltage (zero voltage switching, ZVS), zero current (zero current switching, ZCS), or both. This leads to a significant reduction in switching losses.

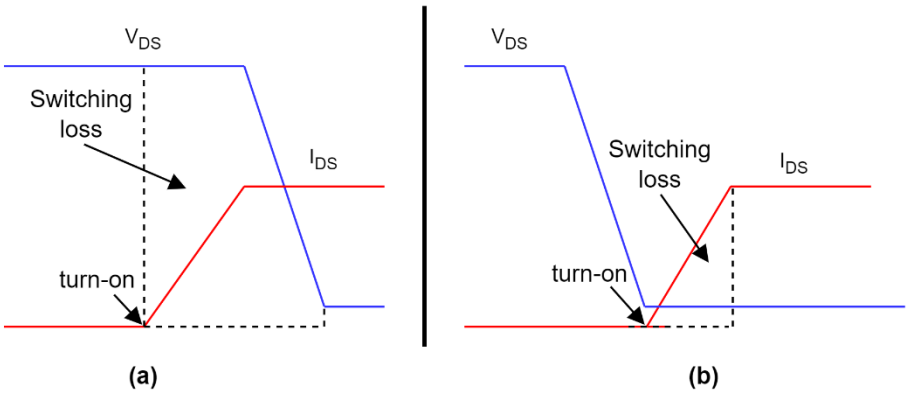

Figure 7. Principle of (a) hard switching and (b) soft switching.

The following equation demonstrates the reduced switching losses achieved through soft switching as opposed to hard switching:

$$P_{SW} = \frac{1}{2} \cdot f_{SW} \cdot V_{DS} \cdot \left(t_{on} \cdot I_{on} + t_{off} \cdot I_{off}\right) \quad (1)$$

where P_{SW} represents switching loss, f_{SW} is switching frequency, t_{on} is turn-on time, I_{on} is current during turn-on, t_{off} is turn-off time and I_{off} is current during turn-off (Prado et al., 2022, p. 2–3). Typical hard switching topologies include flyback and buck-boost converters, while LCC and LLC converters are common soft switching topologies.

3 Structure of FETs

The performance of a FET is determined by its structure and the physical properties of the semiconductor material used. This chapter covers the most common concepts that arise due to physics and structures of WBG technologies.

3.1 Semiconductor materials

Table 1 presents the key physical properties of the semiconductor materials utilized in Si MOSFET, SiC MOSFET, and GaN FET. As discussed in Chapter 1, SiC and GaN have significantly larger bandgaps compared to Si, which results in superior performance characteristics such as a higher breakdown field. GaN exhibits the highest electron mobility, whereas SiC has the lowest. Moreover, SiC has the best thermal conductivity, which allows it to operate at higher temperatures than Si or GaN.

While table provides valuable information about the performance of each transistor type in theory, it cannot be used alone to determine the best transistor type, as their actual performance depends on various factors. For instance, although GaN can theoretically handle voltage levels close to those of SiC, the technical challenges in fabricating GaN FETs mean they still lag behind SiC MOSFETs in terms of breakdown voltage.

Table 1. Physical properties of semiconductor materials (Ravinchandra, p. 1399, 2022).

Property	Si	4H-SiC	GaN
Band-gap energy, E_g (eV)	1,12	3,3	3,4
Breakdown field, E_c (10^6 V/cm)	0,3	3,5	3,3
Electron mobility, μ_n (cm^2/Vs)	1350	950	1500
Thermal conductivity, λ (W/cmK)	1,5	4,9	1,3

3.2 Basic structure of MOSFET

The two fundamental MOSFET structures are the lateral and vertical designs. The lateral design is shown in Figure 8, based on the application note of Onsemi (2022, p. 3). It has the drain, gate, and source terminals on the same side, with current flowing horizontally from drain to source. To ensure sufficient voltage blocking capability, the distance between the drain and source terminals must be large. However, increasing the channel length increases the on-state resistance, which is typically undesirable in high-power applications.

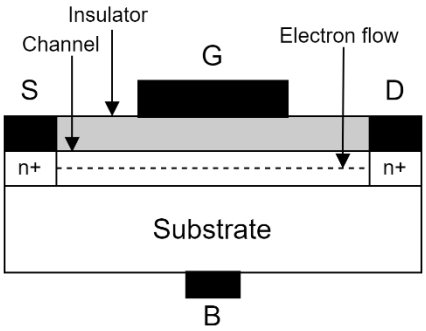

Figure 8. Lateral structure of MOSFET.

Figure 9 illustrates the simplified structure of an n-channel vertical MOSFET. According to Onsemi (2022, p. 3) in this structure, the drain is located opposite to the gate and source terminals, and the current flows vertically through the drift region from drain to source. This vertical structure offers both a short channel length and high voltage blocking capability, making it more suitable for high power applications than the lateral structure. This is the key difference between regular MOSFETs and power MOSFETs, as the latter typically utilize a vertical structure to block high voltages while maintaining a small on-state resistance. Throughout the rest of the text, the term "MOSFET" will refer specifically to power MOSFETs.

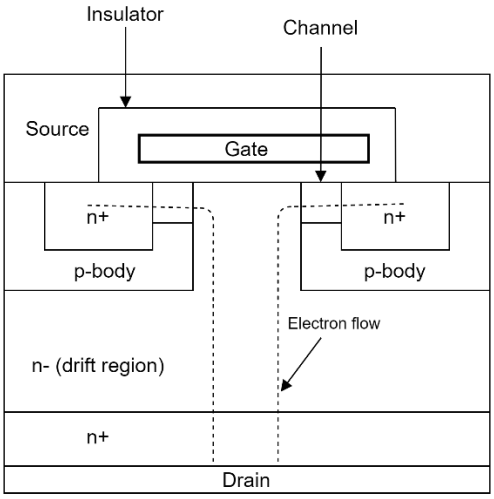

Figure 9. Vertical structure of MOSFET.

Vertical MOSFETs can be designed with different types of gate structures, with planar (DMOS) and trench (UMOS) being the most commonly used. These gate structures are described in an application note of Toshiba (2018, p. 3–4). Figure 10 illustrates the basic structure of these two designs, where (a) shows the planar gate structure with the gate located on the surface of the semiconductor, and (b) shows the trench gate structure with the gate located within the trench that has been etched into the semiconductor surface.

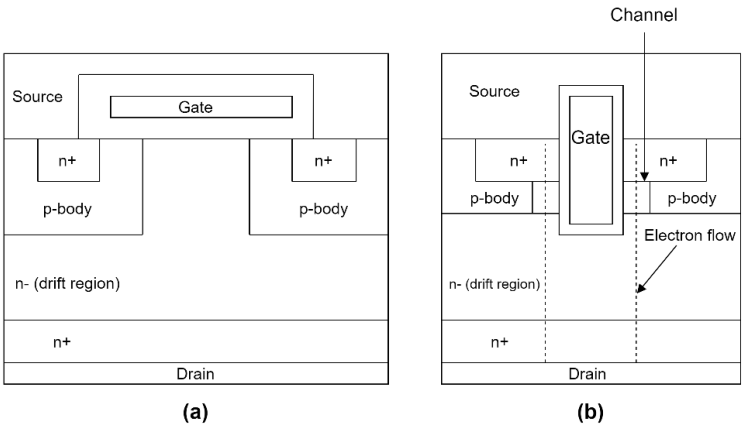

Figure 10. Structure of (a) planar MOSFET and (b) trench MOSFET.

MOSFETs are available in various packaging options including multiple thru-hole, surface mount, and PQFN packages. For power MOSFETs, popular packages include TO-220, TO-247, TO-3PF and TO-252 (DPAK). Additionally, manufacturers often offer their own unique package designs. The package shown in Figure 11 is a TO-3PF package, which is similar to TO-247 package, except that the creepage distance of drain (center terminal) with respect to other terminals is increased to provide proper isolation.

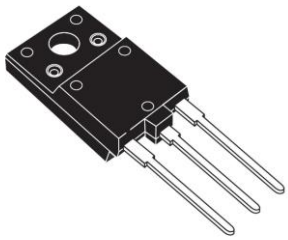

Figure 11. TO-3PF package (captured from www.mouser.fi).

The design of the package affects the thermal properties of the device, among other factors. Ravinchandra et al. (2022, p. 1041) also state that packages with long leads, such as TO-3PF, also have parasitic inductance that can limit the switching frequency to 1 MHz. This is why conventional enhancement GaN FETs, which are suitable for very high switching frequencies, are typically only available in surface-mount and chip-scale packages.

3.3 Si MOSFET

The typical modern Si MOSFET has vertical DMOS structure. The structure is illustrated in Figure 12, where the device is made up of a silicon die doped with $n^+pn^-n^+$ layers. The heavily doped n^+ type substrate serves as the drain terminal, while the source terminal is made up of a double diffusion pn^+ region (Sattar, n.a, p. 1). The electrodes are utilized to establish electrical connections to the MOSFET terminals. Typically, gate electrode is made of polycrystalline silicon (Grundmann, 2016, p. 820) while the drain and source electrodes are fabricated using metals. The region between the drain and source

terminals is called the n^- epitaxial layer, which is a lightly doped n^-type drift region. It is essential to block the current flow when there is insufficient gate voltage (You et al., 2012, p. 862). Silicon dioxide (SiO_2) is typically used as a gate insulator material (Grundmann, 2016, p. 827). For making electrical contact between electrodes and MOSFET leads, bond wires are used, which are for example made of gold, aluminum, or copper (Heraeus, 2017, p. 10–18).

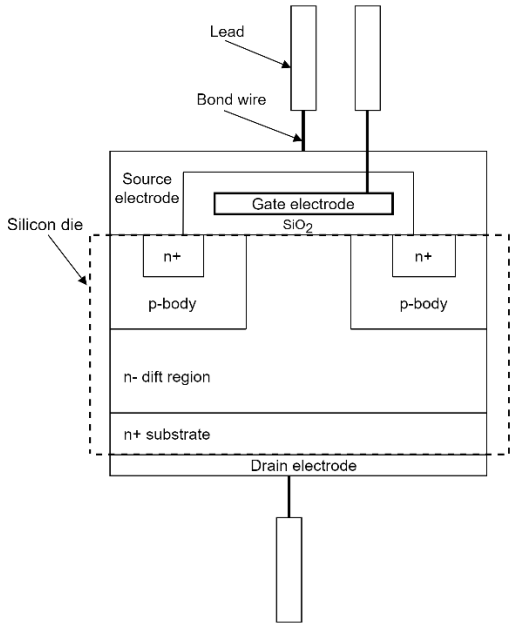

Figure 12. Structure of Si MOSFET.

According to application note of Vishay (2015, p. 1), planar silicon MOSFETs are known for their high on-state resistance. The application note also states that to reduce the on-state resistance, cell density and die size can be increased. This results in increased input capacitance, leading to increased gate drive losses and slower switching speeds. Furthermore, voltage blocking capabilities are determined by the doping level and thickness of the n^- drift region. Increasing the breakdown voltage of the Si MOSFET while keeping the same die size requires a thicker and less doped n^- drift region, which increases the on-state resistance. For traditional planar Si MOSFETs, doubling the breakdown voltage while keeping the same die size results in a three- to five-fold increase in on-state resistance.

To improve the breakdown voltage and decrease on-state resistance in Si MOSFETs, the latest technology is super junction (SJ) technology (Vishay, 2015, p. 1). The structure and operation principle of SJ MOSFETs is described by Oonishi et al. (2010, p. 65-66). SJ MOSFETs have a structure that consists of multiple p-type doped pillars placed into an n^- drift region, as shown in Figure 13. This design allows the n^- drift region to be more heavily doped, as the positive charges from the p-type pillars help to neutralize the negative charge that accumulates in the drift region during gate-source reverse voltage bias conditions. In other words, SJ MOSFETs can achieve higher breakdown voltage with less impact on on-state resistance.

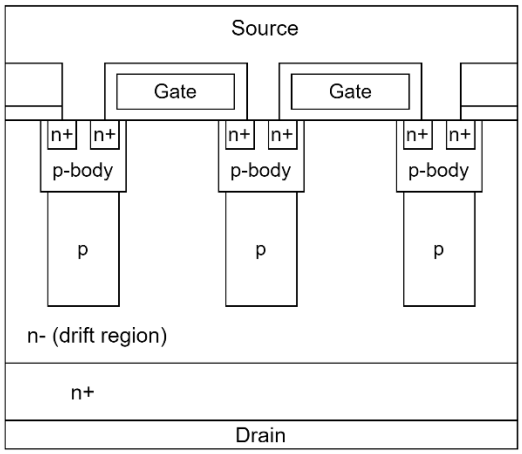

Figure 13. Structure of SJ MOSFET.

The application note of Vishay (2015, p. 1–2) states that SJ MOSFET has a linear dependence between breakdown voltage and on-state resistance. Therefore, increasing the breakdown voltage of SJ MOSFETs has a much smaller impact on the on-state resistance than it does with traditional Si MOSFETs. Despite the improved functionality of SJ MOSFETs, there is still a limit to how low the on-state resistance of silicon can be reduced.

3.4 SiC MOSFET

The structure of a SiC MOSFET is similar to that of Si MOSFET, but the semiconductor material used is silicon carbide instead of silicon. According to Yamaguchi (2017, p. 99), SiC exists in several different polymorphs, which means it has many crystal structures. The 4H SiC polymorph offers the best electrical properties, making it the most used polymorph in SiC MOSFETs.

In 2008, the first SiC power transistors were introduced to the market. These devices were 1200 V JFETs (Speer et al., 2017, p. 72). The main SiC MOSFET technologies currently used are enhancement mode n-channel devices with planar, trench or double-trench structures. Planar SiC MOSFETs feature a planar gate structure, similar to conventional Si MOSFETs, and they have gained significant market share in recent years. Chen et al. (2020, p.1081) state that planar SiC MOSFETs have a drawback in that the gate oxide is grown on the SiC surface through a thermal process, which results in a high density of SiC/SiO_2 interface traps. This, in turn, leads to low conductivity of the planar channel. To address this issue, a relatively thin gate oxide is needed, which can result in reliability concerns (Peters et al., 2017, p. 25).

The performance of SiC MOSFET has been enhanced through the development of trench and double trench SiC MOSFETs. The structures are shown in Figure 14 (a) and (b), respectively. Anwar et al. (2018, p. 1040) state that the trench gate structure enables vertical channel formation, leading to improved conductivity of the channel in comparison to planar designs. Thus, gate oxide can be made thicker for better reliability. The trench structure allows for the source and gate terminals to be positioned within a smaller area, resulting in reduced chip size and capacitances. However, for voltages under 1000 V, trench SiC MOSFETs exhibit higher output capacitance compared to planar SiC MOSFETs. Beyond 1200 V, the output capacitances of trench SiC MOSFETs become comparable to those of planar SiC MOSFETs.

Single trench SiC MOSFETs have issues with the concentration of the electric field at the base of the gate trench, which increases the potential risk of gate oxide breakdown during high voltage operations (Tamaso et al., p. 91, 2018). Additionally, according to Cheng et al. (2022, p. 1), single trench SiC MOSFETs have a large gate-to-drain capacitance that negatively impacts their switching characteristics. To address these limitations, a double trench SiC MOSFET was developed. The structure includes source trenches etched into the SiC n^- drift region, promoting a more uniform electric field. Furthermore, according to Rohm (2022, p. 2), the double trench structure allows for the placement of the source and gate terminals within an even smaller area compared to the single trench structure, further reducing chip size and capacitances.

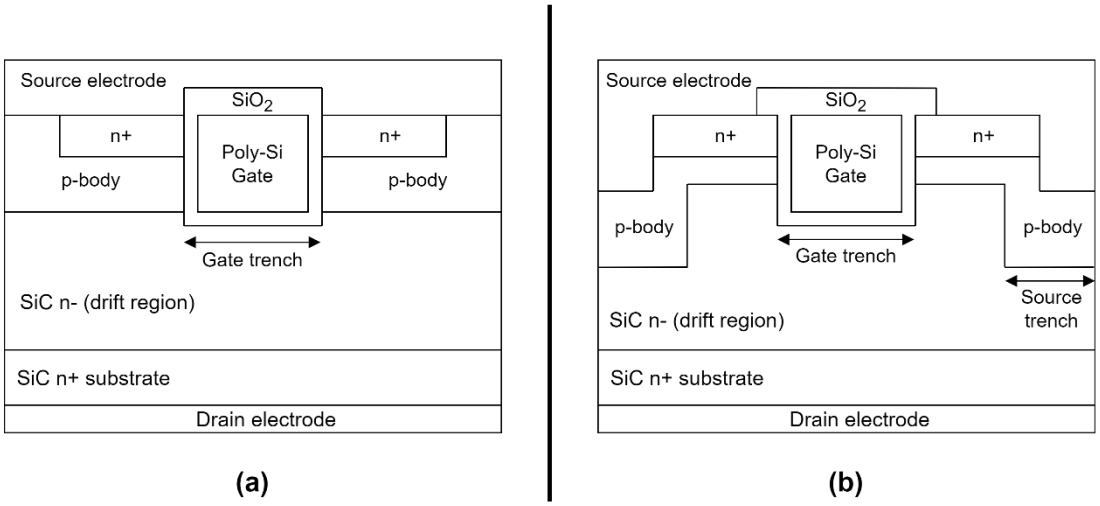

Figure 14. Structure of (a) single trench and (b) double trench SiC MOSFET.

Trench technology has also been employed with Si MOSFETs, but due to the properties of Si combined with the limitations of the trench structure, they can only be fabricated with a breakdown voltage of up to 250 V (Toshiba, 2018, p. 4). Some SiC MOSFET manufacturers, like Rohm, provide several SiC MOSFET generations, referring to different kind of technologies. The generations of Rohm are second generation for planar SiC MOSFET and third and fourth generations for trench SiC MOSFET (including single- and double trench). Datasheets or application notes of manufacturers do not generally separate the

trench and double trench SiC MOSFETs. Thus, it is hard to exactly know in which technology a certain SiC MOSFET is based on. Because of that, this work refers to trench SiC MOSFETs including both, single- and double trench technologies.

3.5 GaN FET

GaN FET, also known as GaN HEMT (High Electron Mobility Transistor), is a type of FET that distinguishes itself from Si- and SiC MOSFETs due to its lateral structure. The first GaN FET was showcased by Ghan et al. in 1993 (Zhong et al., 2021, p. 462). In 2010, the first commercial enhancement mode GaN on Si transistor, using Si as a substrate, was launched by International Rectifier and Efficient Power Conversion corporations (Zhong et al., 2021, p. 462).

Figure 15 illustrates the structure of the GaN on Si transistor, where an AlGaN/GaN heterostructure is grown on Si. The source, gate, and drain electrodes are positioned on top of the AlGaN (aluminum gallium nitride) layer. According to Zhong et al. (2021, p. 463), GaN and Si have a considerable lattice mismatch and thermal expansion coefficient mismatch, hence the requirement for an intermediate layer between them. Several solutions, including AlN/GaN superlattice, low-temperature Al/N intermediate layer, and Al/GaN buffer layer, have been proposed to address this issue. GaN FETs commonly use metal gates instead of polysilicon (EPC, 2020, p. 2).

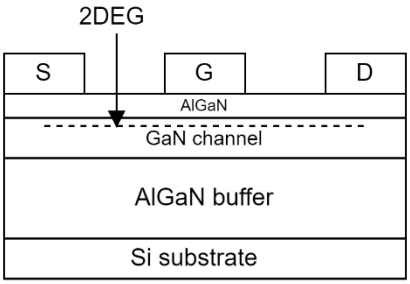

Figure 15. Structure of GaN on Si transistor.

The operating principle of GaN FET is based on the presence of a two-dimensional high mobility electron gas (2DEG), which is induced by the polarization effect of the AlGaN/GaN heterojunction (Islam et al., 2022, p. 10). According to Zhong et al. (2021, p. 462), the 2DEG is highly conductive, which accounts for the large electron mobility of the device. This also results in an extremely low on-state resistance. Due to the presence of the 2DEG, GaN FET conducts naturally even in the absence of an external gate voltage. Since the normally-on behavior in high voltage applications can lead to safety issues and impractical implementation, various techniques have been developed to provide enhancement mode GaN FETs. Of these techniques, the GaN /Si cascode technology and p-GaN FET are perhaps the most well-known.

The structure of a GaN/Si cascode configuration is described by Islam et al. (2022, s. 16). The structure can be seen in Figure 16. It consists of a high-voltage depletion mode GaN FET in series with a low-voltage enhancement mode Si MOSFET. The switching operation is controlled by the Si MOSFET, while the GaN FET blocks the high voltage. The source terminal of the Si MOSFET is connected to the gate of the GaN FET, and the drain terminal of the Si MOSFET is connected to the source of the GaN FET. When Si MOSFET is turned on, the gate-to-source voltage of the GaN FET is close to 0 V or positive, and the cascode device is conducting. After the Si MOSFET is turned off, the GaN FET is affected by a negative gate-to-source voltage, causing the cascode device to turn off.

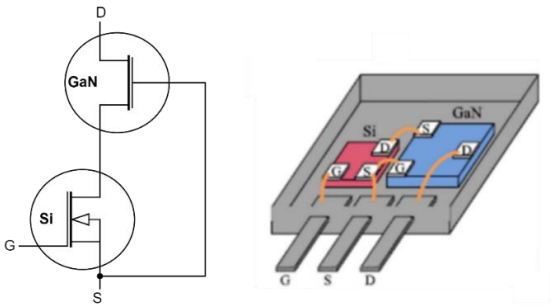

Figure 16. Structure of Si/GaN cascode transistor (Zhong et al., 2022, p. 465).

The cascode structure has some drawbacks, including capacitance mismatch, increased parasitic inductance, and high-temperature stability issues with the Si MOSFET (Zhong et al., 2021, p. 464; Islam et al., 2022, p. 16). Parasitic inductance increases due to the use of bonding wires to connect the terminals of Si MOSFET and GaN FET, but advanced packaging methods like the chip-on-chip technique can help reduce it (Du et al., 2017, p. 1002). Capacitance mismatch can be a problem, particularly in soft-switching applications, and is discussed in more detail in Chapter 4.

Figure 17 illustrates the p-type gate structure of GaN FET. This design relies on the doping of Mg (magnesium) acceptor impurities into the GaN crystal structure, which creates a depletion region and a high-voltage barrier under the gate region at 0 V or negative gate voltage (Qi et al., 2019, p. 1). When applying a sufficient positive gate voltage, the positively charged gate region accumulates electrons under the gate, making the channel electrically conductive (Islam et al., 2022, p. 17). According to Zhong et al. (2021, p. 467), p-GaN FET has robust operation, but it still faces challenges, with the most significant being the appropriate Mg acceptor doping level. Low Mg concentration results in a low gate threshold voltage, while too high doping level leads to increased on-state resistance.

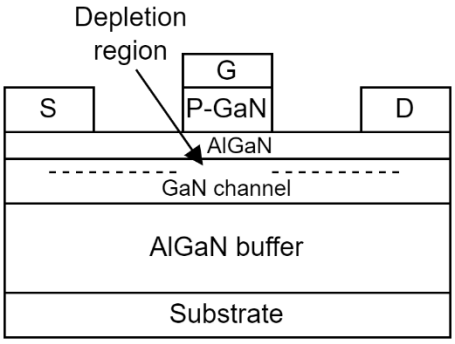

Figure 17. The structure of p-GaN FET.

In literature, the terms "E-mode GaN FET" or "e-GaN FET" are commonly used to refer to GaN FETs that operate in enhancement mode without the cascode structure.

3.6 Intrinsic components of FETs

Si- and SiC MOSFETs have inherent components known as parasitic BJT and body diode. Figure 18 illustrates (a) their location within an n-type MOSFET and (b) their equivalent circuit. According to Sattar (n.d, p. 2), the parasitic BJT is formed of an n^+ region that acts as the emitter, a p-body region that acts as the base, and a drain region that acts as the collector. Typically, the p-body is connected to the n^+ region via the source electrode to prevent the turn-on of the BJT. The body diode of Si- and SiC MOSFETs is formed as a result of this connection, and it exists between the source and drain of the MOSFET. Although it is a parasitic component, the body diode has the advantage of allowing current to flow in the reverse direction through the MOSFET.

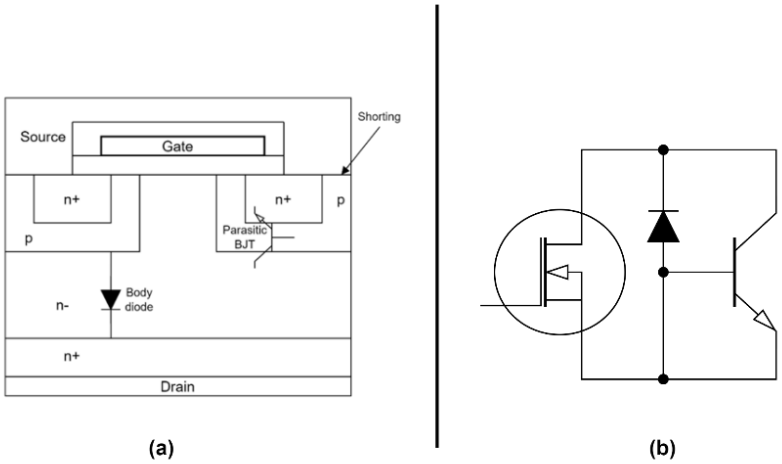

Figure 18. Intrinsic components of MOSFETs.

According to Sun (2019, p. 3), GaN FET does not have a parasitic BJT or body diode due to lack of pn-doping. Despite the lack of a body diode, it is still able to conduct in the reverse direction through the mechanism of self-commutating. The effects of intrinsic components on MOSFET's functionality and reverse conducting characteristics of GaN FET are discussed in more detail in Chapter 4.

4 Electrical characteristics of FETs

In this chapter, the most important electrical characteristics of FETs are studied. The basic theory behind each characteristic is first clarified in each subsection, followed by an examination of the specific transistor type with respect to that characteristic.

4.1 Drain-to-source breakdown voltage

When the voltage blocking capability of a transistor in the off-state is exceeded, it results in a drain-to-source breakdown. In Si- and SiC MOSFET, it occurs when the pn-junction between the source and drain breaks down (Barkhordarian, n.a, p.5), while in GaN FET, it occurs when the voltage barrier under the gate breaks down (Saito et al., 2015, p. 1682).

Commercial planar SiC MOSFETs have a maximum breakdown voltage (BV_{DS}) of up to 1700 V, while trench SiC MOSFET has 2000 V. The breakdown voltage of conventional Si MOSFETs has been enhanced to 1700 V with SJ technology. The lateral structure of GaN FET limits its high voltage operation (Prado et al., 2022, p.2), and as a result, GaN FETs are only available with breakdown voltages up to 650 V (E-mode GaN FET) and 900 V (Cascode). Although there are ongoing studies of GaN FETs with a vertical structure (Zhong et al., 2022, p. 463), the lack of good-quality bulk substrates remains a significant challenge (Prado et al., 2022, p.2).

4.2 Avalanche ruggedness

When breakdown voltage of transistor is exceeded, device enters the avalanche mode (Toshiba, 2018, p. 1-5). This event can lead to two possible failure modes: avalanche current breakdown and avalanche energy breakdown (Toshiba, 2018, p. 1-5). Figure 19 illustrates the two distinct avalanche breakdown mechanisms, wherein D_B represents the

body diode, R_B represents the resistance between the base and emitter of parasitic BJT, and I_A represents the avalanche current.

The avalanche characteristics of MOSFET are described in an application note by Onsemi (2022, p. 13-14). When MOSFET is operating in avalanche mode, it allows the flow of avalanche current through the body diode in reverse direction. If I_A is high enough, a voltage drop greater than the base-to-emitter threshold voltage of the parasitic BJT can be induced across the resistance R_B. This causes the parasitic BJT to turn on, providing a low-impedance current path from collector to emitter, which eventually leads to excessive current and destruction of the device. However, since the anode of the body diode is typically connected to the source via a metallic contact, R_B is small. As a result, the voltage drop across R_B is small, and the risk of parasitic BJT turn-on is low. The possibility of parasitic BJT turn-on should still be under consideration, especially in high voltage switching applications where the dv/dt rates can be large.

According to Toshiba (2018, p. 5), the device can still experience avalanche energy breakdown even if I_A is within the safe limits and the parasitic BJT is not triggered. This occurs when the power loss due to V_{DS} X I_A exceeds the maximum rated pn-junction temperature, leading to the device's destruction.

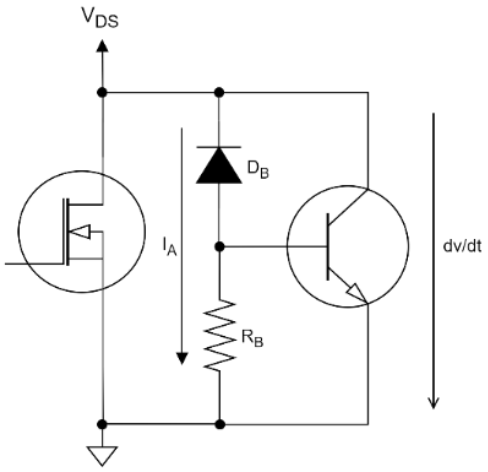

Figure 19. Avalanche current and mechanism of parasitic BJT turn-on.

Si- and SiC MOSFET datasheets sometimes report their avalanche current and avalanche energy, which refer to the maximum current and energy that the device can withstand when the breakdown voltage is exceeded. SiC MOSFETs are known to have excellent avalanche capability, as shown in a study made by DiMarino & Hull (2015, p. 263). They found that a 1200 V planar SiC MOSFET could withstand avalanche currents more than twice its rated current, unlike Si MOSFETs used for comparison. Additionally, according to the same study, it seems that SiC MOSFETs require a higher avalanche current to turn on the parasitic BJT than Si MOSFETs.

The lack of pn-junctions in GaN FET means that it does not have any avalanche ratings, unlike Si- and SiC MOSFET. However, studies suggest that it has better transient overvoltage capability, which compensates for the absence of avalanche capability (Ravinchandra et al., 2022, p. 1402). Moreover, Transphorm, a manufacturer of E-mode GaN FETs and GaN/Si transistors, states that GaN FETs have dielectric breakdown voltage similar to a capacitor, which is often as much as three times their maximum rated voltage (Transphorm, 2017, p. 2).

4.3 V_{GS} characteristics

The key V_{GS} characteristics of FETs include maximum V_{GS}, $V_{GS(TH)}$, and recommended V_{GS} for turn-on and turn-off. The recommended V_{GS} for turn-on is mainly determined by the output characteristics of the FET, which depend on the device's transconductance (g_m). According to Onsemi (2022, p. 11). transconductance is defined as the ratio of change in I_D to the change in V_{GS}:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \tag{2}$$

Transistors with high g_m can provide high I_D with low V_{GS}, while those with low g_m require higher V_{GS} for the same I_D. High-voltage Si MOSFETs typically have a recommended V_{GS} for turn-on of around 10 V. On the other hand, SiC MOSFETs are generally low-gain devices due to their low g_m, and higher V_{GS} is recommended for turning them on compared to other transistor types (Onsemi, 2022b, p. 3). Planar SiC MOSFETs have a recommended V_{GS} for turn-on of about 18-20 V, which is close to their maximum positive limits (SCT2H12NZ datasheet, 2017, p. 3; Onsemi, 2022b, p. 2). The recommended V_{GS} for turn-on in single trench and double trench SiC MOSFETs is typically 15-18 V (Infineon, 2018, p. 12; Rohm, 2022, p. 16).

Unlike SiC MOSFETs, GaN FETs are high-gain devices and typically have much lower V_{GS} ratings than other transistor types. The recommended turn-on V_{GS} for GaN FET is usually around 5-6 V, with a common maximum rating of 6-7 V (Mohamed & Sanchez, 2022, p. 2; GS66504B datasheet, n.d, p. 2-3). However, it should be noted that GaN/Si cascode transistors are an exception due to presence of Si MOSFET. Transphorm recommends their GaN/Si cascode transistors to be turned on with 12 V V_{GS} (Transphorm, 2018, p. 6).

Figure 17 illustrates the typical output characteristics of six commercially available transistors at a temperature of 25 °C. The devices included are IPW65R125C7 SJ MOSFET from Infineon (700 V, 111 mΩ, 18 A), S2206 2nd gen planar SiC MOSFET (650 V, 120 mΩ,

29 A) from Rohm, SCT3120AL 3rd gen trench SiC MOSFET from Rohm (650 V, 120 mΩ, 21 A), SCT4045DW7HR 4th gen trench SiC MOSFET from Rohm (750 V, 45 mΩ, 31 A), GS66504B E-mode GaN FET from GaN Systems (650 V, 100 mΩ, 15 A), and TP65H050WS GaN/Si cascode transistor from Transphorm (650 V, 50 mΩ, 36 A).

When analyzing the I-V curves, it can be noted that the ohmic region of SiC MOSFETs is considerably smoother compared to other transistor types and SiC MOSFETs do not have obvious saturation region (Onsemi, 2022a, p. 11–14) especially when considering notable currents. On the other hand, for other transistor types, particularly Si MOSFET, the curve at the ohmic region is much steeper, and the transition to the saturation region is abrupt, followed by completely flat curve.

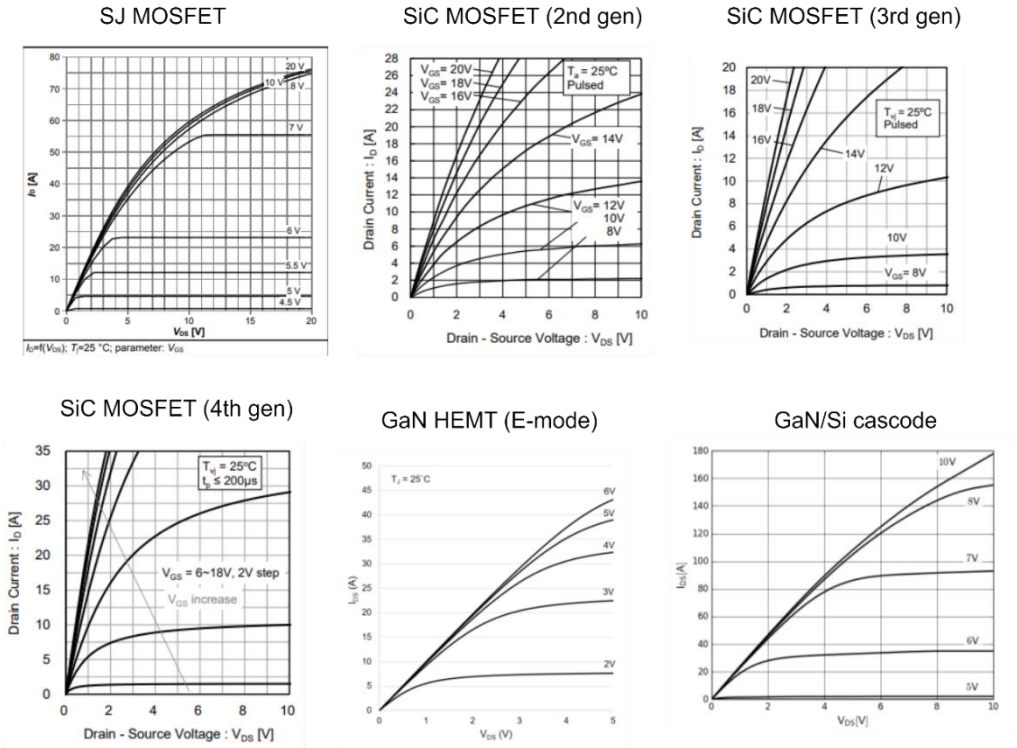

Figure 20. Comparison of output characteristics (IPW65R125C7 datasheet, 2013, p. 9; S2206 datasheet, 2016, p. 5; SCT3120AL datasheet, 2022, p. 6; SCT4045DW7HR datasheet, 2023, p. 6; GS66504B datasheet, n.d, p. 4; TP65H050WS datasheet, 2021, p. 6).

Equations (3) and (4) (Onsemi, 2022b, p. 3) demonstrate the significance of high V_{GS} for low-gain devices such as SiC MOSFETs. Increasing V_{GS} results in a decrease in the required V_{DS} for the desired current, allowing for a smaller R_{DSON} to be achieved.

$$I_D = g_m \cdot \left(V_{GS} - V_{GS(TH)}\right) \tag{3}$$

$$R_{DSON} = \frac{V_{DS}}{I_D} \tag{4}$$

Determining the recommended V_{GS} for turn-off is primarily based on the transistor's $V_{GS(TH)}$. According to Onsemi (2022a, p. 11–14), $V_{GS(TH)}$ for MOSFETs is determined by the thickness of the gate oxide and the density of the p-body region. A thicker gate oxide and a denser p-body region lead to a higher $V_{GS(TH)}$. $V_{GS(TH)}$ also has a negative temperature coefficient, which means that it decreases with an increase in temperature. Due to the thin gate oxide of planar SiC MOSFETs, their $V_{GS(TH)}$ is typically low.

E-mode GaN FETs have an even smaller $V_{GS(TH)}$ due to their lateral structure, low C_{GD}, and almost flat relationship between temperature and $V_{GS(TH)}$ (Mohamed, 2022, p. 2). To prevent false turn-on, it is recommended to turn off planar SiC MOSFETs and E-mode GaN FETs with negative V_{GS} (Onsemi, 2022b, p. 4; Mohamed & Sanchez, 2022, p. 2). Si MOSFETs, GaN/Si cascode transistors, and trench SiC MOSFETs have a higher $V_{GS(TH)}$ and can be turned off with V_{GS} 0 V (SCT3120AL datasheet, 2022, p. 6; SCT4045DW7HR datasheet, 2023, p. 6; TP65H050WS datasheet, 2021, p. 6). Table 2 summarizes the recommended V_{GS} values of various transistor types.

Table 2. Recommended gate-to-source voltages for various transistor types.

Device	Recommended V_{GS} turn-on	Recommended V_{GS} turn-off
Si MOSFET	10 V	0 V
Planar SiC MOSFET	18 V to 20 V	-5 V
Trench SiC MOSFET	15 V to 18 V	0 V
E-mode GaN	5 V to 6 V	-2 V to -3 V
GaN/Si cascode	12 V	0 V

4.4 On-state resistance

Figure 21 illustrates the resistive components of (a) vertical power MOSFET and (b) GaN FET. In conventional Si MOSFETs with voltage rating beyond 600 V, the most of total resistance (about 96%) comes from drift region resistance (R_{drift}), with the rest coming from substrate resistance (R_{sub}) and channel resistance (R_{ch}) (Vishay, 2015, p. 1). For SiC MOSFETs, the proportion of R_{drift} in total R_{DSON} is significantly smaller (Rohm, 2022, p. 7). In the case of GaN FETs, the resistive components include R_{CH} (directly under the gate), connection resistance (R_{con}) from the ohmic contacts between AlGaN barrier layer and GaN layer (Zhong et al., 2021, p. 470), as well as R_{sg} and R_{dg} resulting from the resistance of the GaN layer (Islam et al., 2022, p. 23). The main factor affecting the R_{DSON} of GaN FETs is the 2DEG density (Zhong et al., 2021, p. 467). R_{DSON} in all transistor types can be calculated by summing all resistive components (Vishay, 2015, p. 1).

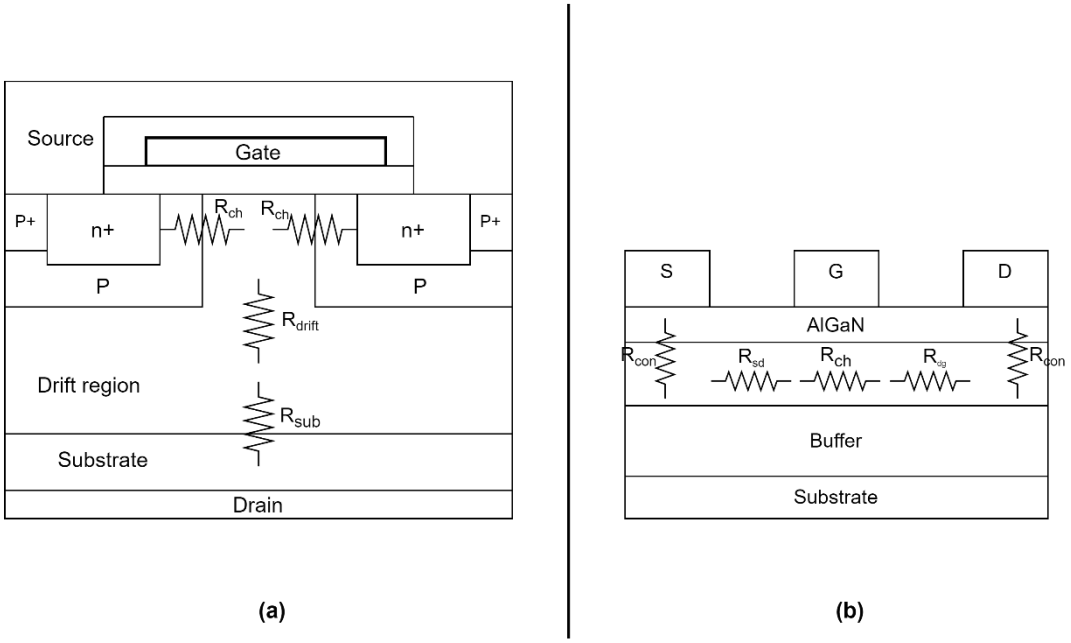

Figure 21. Resistive components of (a) vertical power MOSFET and (b) GaN FET.

R_{DSON} increases as temperature increases due to its positive temperature coefficient (On-semi, 2022, p. 11). According to Rohm (2022, p. 7), R_{drift} is the resistive component that is particularly affected by the temperature variations. Since SiC MOSFETs have a much smaller R_{drift}/R_{DSON} ratio compared to Si MOSFETs, they have much less R_{DSON} variation with temperature. Datasheets indicate that also R_{DSON} of GaN FET is more temperature-sensitive than that of SiC MOSFET (GS66504B datasheet, 2021, p. 6)

The conducting loss during FET is on can be calculated:

$$P_{CON} = R_{DSON} \cdot I_D^2 \tag{5}$$

where P_{CON} is conducting loss.

4.5 Internal gate resistance

The internal gate resistance, which arises from the gate electrode and insulator, has a impact on the switching speed of a FET. It limits the gate current required to charge the input capacitance. R_{Gint} is typically around 1 Ω for Si MOSFET and GaN FET, so it can be ignored. However, according to datasheets and application note of Onsemi (SCT2H12NZ datasheet, 2017, p. 3; Onsemi, 2022b, p. 4). R_{Gint} of SiC MOSFET can be significant and lead to slower switching speeds. Despite this, the relatively low input capacitance of SiC MOSFET still allows for faster switching speeds when compared to Si MOSFET. The internal gate resistance also causes switching loss as it dissipates energy during charging and discharging of the input capacitance.

4.6 Capacitances

The physical locations of parasitic capacitances are illustrated in Figure 22. Specifically, (a) shows the locations in Si- and SiC MOSFETs, (b) shows the locations in GaN FETs, and (c) presents a general equivalent circuit. According to Onsemi (2022a, p. 8), the parasitic capacitances include C_{GD}, which refers to the gate-to-drain capacitance, also known as Miller capacitance, C_{GS}, which represents the gate-to-source capacitance, and C_{DS}, which is the drain-to-source capacitance. The sum of C_{GD} and C_{GS} is defined as the input capacitance, C_{iss}:

$$C_{iss} = C_{GD} + C_{GS} \tag{6}$$

The sum of C_{GD} and C_{DS} is output capacitance C_{OSS}:

$$C_{OSS} = C_{GD} + C_{DS} \tag{7}$$

Reverse transfer capacitance C_{RSS} equivalents to C_{GD}:

$$C_{RSS} = C_{GD} \quad (8)$$

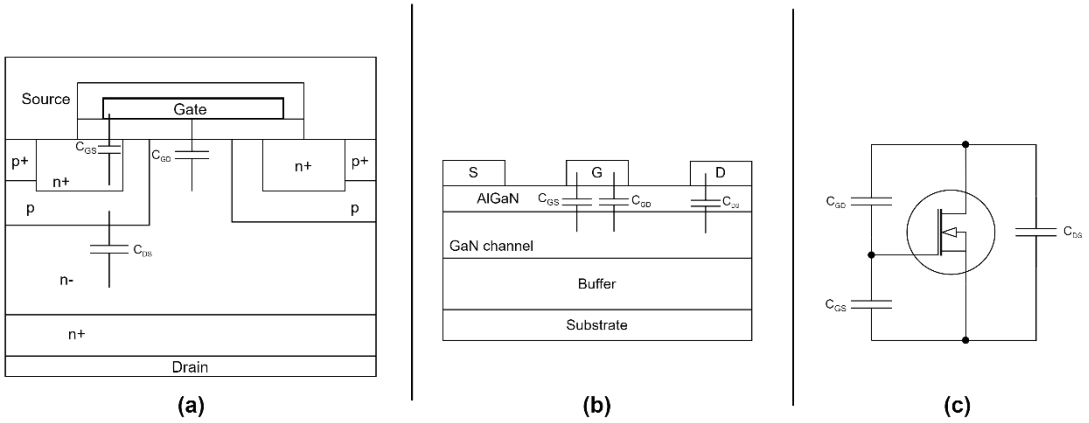

Figure 22. Parasitic capacitances of FETs.

The main factor that affects a FET's switching characteristics is the input capacitance. While datasheets provide input capacitance as a static value, in reality, the input capacitance of a FET changes with the drain-to-source voltage (Vishay, 2016, p. 3). Therefore, using input capacitance in design-related calculations can be complicated. A more practical parameter is the gate charge, Q_G, which represents the total charge required to switch the FET on or off (Vishay, 2016, p. 3). The gate charge, Q_G, as well as the input capacitance, is directly proportional to the chip size of the FET. Apart from impacting the switching speed, Q_G also has an effect on the gate drive loss (Toshiba, 2023, p.4).

According to Toshiba (2023, p. 5), the output capacitance C_{OSS} changes with variations in the drain-to-source voltage, just like the input capacitance C_{iss}. To simplify calculations and estimate the energy stored in the output capacitance during V_{DS} variations, an energy-related effective output capacitance $C_{O(ER)}$ is often used. This parameter is a fixed capacitance value that can be used to calculate the energy stored in the output capacitance during V_{DS} variations.

Capacitance mismatch in GaN/Si cascode transistors can be a problem in soft-switching applications. Figure 23 shows a GaN/Si cascode structure with junction capacitances. In

a study made by Sugiyama (2020, p. 1–3), he describes a scenario where the cascode transistor shown in the figure acts as the low-side FET in a half-bridge configuration. When the upper FET turns off, the output capacitance of both the GaN FET and Si MOSFET begins to discharge. If C_{OSS_Si} is smaller than C_{OSS_GaN} , then C_{OSS_Si} discharges first before C_{OSS_GaN}. At this point, if V_{DS_Si} is negative with respect to V_{GS_GaN}, the gate threshold voltage of the GaN FET can be exceeded, causing it to turn on. Since V_{DS} can still be relatively large, the breakdown voltage of the Si MOSFET may be exceeded, leading to it entering avalanche mode. As a result, current flows through the cascode device, and the soft switching is lost, resulting in additional power loss.

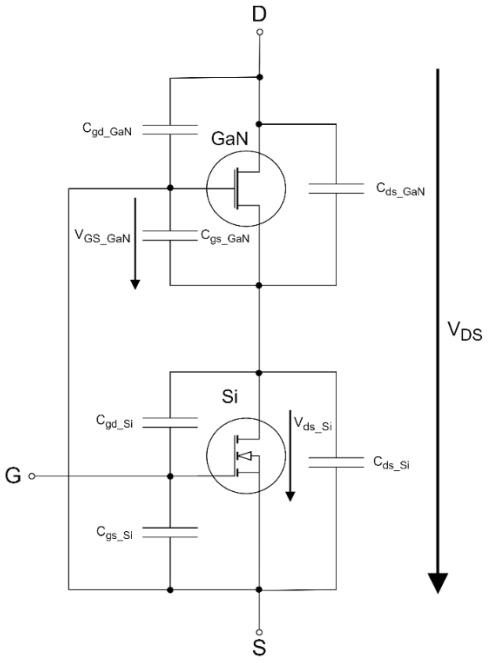

Figure 23. GaN/Si cascode structure with junction capacitances.

According to Zhong et al. (2022, p. 465), to address capacitance mismatch, the simplest approach involves integrating a capacitor in parallel with C_{DS_Si} during the fabrication process. However, determining the appropriate capacitance value can be challenging due to the dynamic characteristics of C_{OSS}. Capacitance mismatch arises due to differences in the chips of Si MOSFET and GaN FET, and in addition to causing soft-switching problems, it can also result in oscillation.

4.7 Third quadrant operation

In soft-switching applications, the reverse conducting characteristics of FETs become crucial. While Si- and SiC MOSFETs can conduct in the reverse direction due to their body diodes, there are reliability issues associated with the operation of the body diode in SiC MOSFETs. The crystal structure of the SiC-drift region is susceptible to defects, which can cause the body diode to degrade when it is forward-biased, leading to an increase in R_{DSON} over time (Kang et al., 2019, p. 416). This is why a general practice has been adding internal Schottky barrier diode (SBD) in parallel with parasitic body diode (Cheng et al., 2022, p. 1).

According to Infineon (2018, p. 7), SiC MOSFET has a high reverse-voltage drop (V_{SD}) due to its physical properties. However, Infineon also states that it is possible to operate SiC MOSFET in a mode where the body diode is bypassed and current flows through the channel from source to drain, resulting in a low V_{SD}. This can be achieved by applying a sufficiently positive V_{GS} (about 15 V) when the drain is negative with respect to the source. However, for example in bridge topologies, dead time between the high- and low-side MOSFETs is necessary, during which the channel of the MOSFET is not conducting and the body diode conducts instead.

The concept of reverse conducting operation of GaN FET by self-commutating was introduced in Section 3.5. According to Sun (2019, p. 3), for this operation to take place, V_{GD} must be higher than $V_{GS(TH)}$. During self-commutation, the gate potential becomes more positive than the drain potential, resulting in a switch of the drain and source positions, allowing the current to flow from the source to the drain. The reverse voltage drop across the device can be calculated using the equation:

$$V_{SD} = \left(V_{GS(TH)} - V_{GS}\right) + I_{SD} \cdot R_{DS(ON)REV} \tag{9}$$

The equation given above relates the source-drain current (I_{SD}) and the on-state resistance in the reverse conducting direction ($R_{DS(ON)REV}$). When the channel is fully on,

$R_{DS(ON)REV}$ is equivalent to $R_{DS(ON)}$. Due to the higher voltage drop across the reverse conducting path of GaN FETs compared to the voltage drop of Si MOSFET body diodes, GaN FETs can experience higher reverse conducting losses (Sun, 2019, p. 3). Magnitude of GaN FET's V_{SD} is also strongly depended on V_{GS} and increases when V_{GS} is more negative (Ravinchandra et al., 2022, p. 1401)

Power losses formed during FET reverse conducting are called dead time loss and they can be calculated using equation:

$$P_D = 2 \cdot V_{SD} \cdot I_{SD} \cdot t_D \cdot f_{SW} \tag{10}$$

where P_D represents dead time loss, t_D is the dead time and f_{SW} is the switching frequency (Rohm, 2016, p. 1). The equation highlights the significance of minimizing dead time, particularly with SiC MOSFET and GaN FET.

The principle of body diode reverse recovery is illustrated in Figure 24. According to Toshiba (2018, p. 4), prior to t_1, the body diode is forward biased, allowing body diode current I_S to flow through it while V_{DS} of the FET is negative. At t_1, the polarity of V_{DS} changes to positive, causing I_S to decrease. At t_2, I_s has reduced to zero, while a significant number of charge carriers remain in the n^- drift region of the semiconductor structure. Between t_2 and t_3, the remaining charge carriers are rapidly removed by reverse current, which reaches its peak at t_3. This current peak is referred to as reverse recovery current, I_{rr}. After t_3, I_{rr} starts to decrease and is completely eliminated at time t_4. The period between t_2 and t_4 is known as reverse recovery time, t_{rr}.

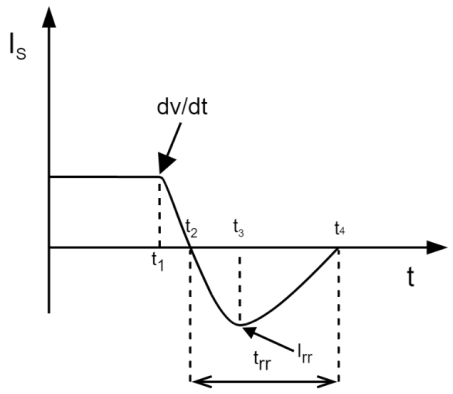

Figure 24. Principle of body diode reverse recovery.

Body diode reverse recovery current can in worst case turn on the parasitic BJT (Onsemi, 2022, p. 15). Less severe, but still noteworthy consequence of the reverse recovery phenomenon is additional power losses. Power loss caused by body diode reverse recovery can be calculated:

$$P_{rr} = f_{SW} \cdot V_{rr} \cdot Q_{rr} \tag{11}$$

where P_{rr} is reverse recovery loss, V_{rr} body diode reverse voltage (which in worst case calculation equals to supply voltage) and Q_{rr} reverse recovery charge. Reverse recovery charge refers to the amount of charge that needs to be removed from the pn-junction during the reverse recovery process (ST Microelectronics, 2021, p. 18).

P_{rr} should be considered in hard-switching topologies, although according to Costinett et al. (2013, p. 7), with SiC MOSFET, P_{rr} is reduced because SiC diodes generally have much smaller Q_{rr} compared to Si MOSFETs. Costinett et al. also state that in soft-switching topologies using SiC MOSFET, the effect of body diode reverse recovery is insignificant. On the other hand, Si MOSFETs operating at high frequency (beyond 500 kHz) can result in significant P_{rr}, even in soft switching.

One of the advantages of E-mode GaN FET is the absence of body diode reverse recovery due to lack of pn-junction (Sun, 2019, p. 2). However, when using GaN/Si cascode transistors, it naturally comes into play.

4.8 Thermal characteristics

The power loss in a FET is converted into heat. Figure 25 presents a thermal model of a FET, based on application note of Onsemi (2022a, p. 16) and the directions of heat flow, where T_J is the junction temperature, T_C is the case temperature, T_S is the heatsink temperature, and T_A is the ambient temperature. The arrows indicate the direction of heat flow. Approximately 80% of the heat flows in the direction of 2, 4, and 5, while the remaining 20% flows to 1 and 3 (Onsemi, 2022a, p. 16).

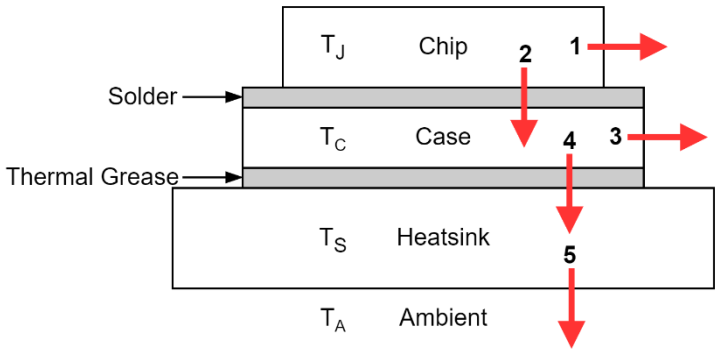

Figure 25. Thermal model of FET.

High junction temperature can negatively impact the performance of a FET, as it can reduce the device's lifetime and compromise its reliability (Mu et al., 2021, p. 285). The thermal conductivity is the best parameter for estimating the thermal properties of a material as it measures its ability to transfer heat to its surroundings. Thermal resistance is the inverse of thermal conductivity. Therefore, to maintain the FET at a low temperature, a low thermal resistance is desirable (ROHM, 2021, p. 1). Thermal resistance is generally declared as junction-to-case thermal resistance ($R_{TH(JC)}$) and junction to ambient

thermal resistance ($R_{TH(JA)}$). Thermal resistance depends on semiconductor material, chip size and package design (Onsemi, 2022a, p. 16).

In Section 3.3, it was stated that SiC have a thermal conductivity that is more than three times greater than that of Si or GaN. However, when exploring the datasheets, it appears that SiC MOSFETs generally have larger $R_{TH(JC)}$ and $R_{TH(JA)}$ values compared to Si MOSFETs in the same package, current class, and voltage class. This appears to conflict with the thermal properties of SiC, but it can be explained by the size of the chip. SiC MOSFETs are packed into smaller chips than Si MOSFETs, which allows smaller gate charge but can lead to deteriorated thermal properties (Mu et al., 2021, p. 285).

One of the major drawbacks of GaN FET is its poor thermal conductivity, which is further reduced when GaN FETs are made in small chip sizes. Figure 26 depicts power losses of GaN FET and SiC MOSFET at different junction temperatures and switching frequencies in a simulation conducted by Shah et al (2018, p. 5). The simulation employed transistor models of 650 V TPH3207WS GaN FET and 900 V C3M0065090D SiC MOSFET in a dc-dc buck-boost converter model. As shown in figure, the overall power loss of GaN FET is lower than SiC MOSFET but is heavily influenced by junction temperature, while the power loss of SiC MOSFET remain consistent apart from the junction temperature.

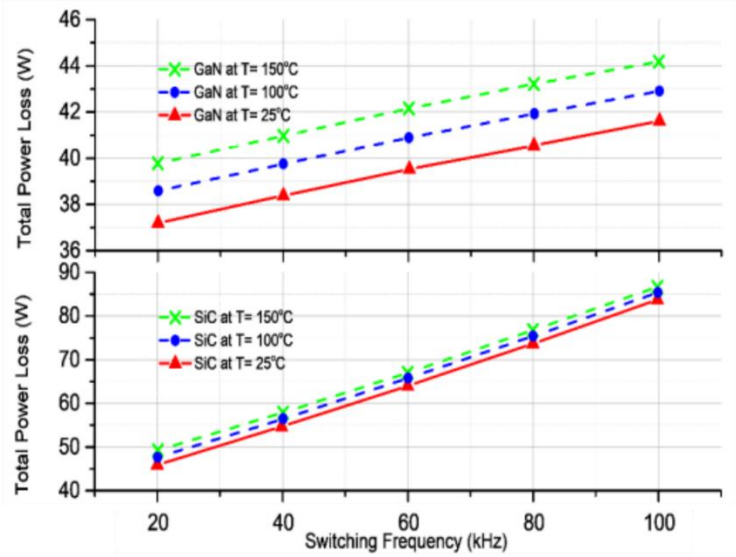

Figure 26. Power loss of GaN FET and SiC MOSFET at various junction temperatures and switching frequencies (Shah et al., 2018, p. 4) (published with permission of authors).

Max T_j of commercial SiC MOSFETs at moment is generally 175 °C when corresponding value for Si MOSFETs and GaN FETs is 150 °C.

4.9 Common reliability issues of SiC MOSFET and GaN FET

Although SiC MOSFETs and GaN FETs have shown good overall performance, they are still known to have reliability issues that have been widely studied. This chapter aims to cover the most well-known reliability issues associated with these devices.

4.9.1 False turn-on

The mechanism of false turn-on is illustrated in Figure 27, where Z_{GS} represents the impedance of the gate drive circuit. According to Onsemi (2022a, p. 13-14), during turn-off, the rapid increase in V_{DS} results in a displacement current (I_1) flowing through C_{GD},

causing a voltage drop across Z_{GS}. If the voltage drop across Z_{GS} exceeds the gate-source threshold voltage, the FET may turn on, leading to possible destructive consequences.

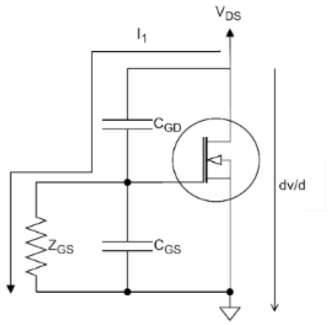

Figure 27. Mechanism of false turn-on.

As $V_{GS(TH)}$ has a negative temperature coefficient, the probability of false turn-on increases with rising temperature (Barkhordarian, n.a, p. 12). The use of a high impedance load limits the displacement current and reduces the likelihood of false turn-on (Onsemi, 2022a, p. 14). However, the risk of false turn-on is greater when employing FETs with low $V_{GS(TH)}$.

4.9.2 Gate reliability

As mentioned in Section 3.3, planar SiC MOSFETs have a relatively thin gate oxide layer, which can lead to reliability issues, including $V_{GS(TH)}$ instability. Sreejith et al. (p. 5, 2022) state that the instability can occur if the gate of the device is driven near its maximum limits for extended periods. It has been observed that when the gate is stressed near its positive limits, $V_{GS(TH)}$ shifts in the positive direction, while the shift is in the negative direction when the gate is stressed near its negative limits. This problem is particularly prevalent in high-temperature conditions. Since planar SiC MOSFETs have a smaller $V_{GS(TH)}$ compared to Si MOSFETs, a negative shift in $V_{GS(TH)}$ can lead to false turn-on. However, according to Nel & Perinpanayagam (2016, p. 281), the change in $V_{GS(TH),}$ which is approximately ±0.25 V, is still negligible in most applications.

Despite the improved gate reliability of trench SiC MOSFETs, they are not completely immune to reliability issues. As stated in Section 3.4, due to the structure of single trench SiC MOSFET, high electric fields can cause damage to the gate oxide. Additionally, there is some evidence that gate oxidation breakdown can occur on double trench SiC MOSFETs under short-circuit conditions, unlike in the case of planar SiC MOSFETs (Sreejith et al., 2022, p. 10)

Also GaN FET has gate reliability issues. According to Zhong et al. (2022, p. 469), $V_{GS(TH)}$ shift can occur if the gate of GaN FET is stressed for long periods with high bias voltage due to the generation of defects on the gate region. Over time, gate stress can also lead to increased gate leakage current, which can eventually become so large that gate breakdown occurs.

4.9.3 Short circuit robustness

Because of the fast switching speed and low $R_{DS(ON)}$, WBG transistors are vulnerable for short circuit conditions. According to Sreejith et al. (2022, p. 8), two most common short circuit failure modes of SiC MOSFETs are simultaneous short-circuit between drain and source and drain and gate as well as short-circuit between source and gate due to degradation of gate oxide. It is reported that the drain current of SiC MOSFET can exceed 10x the nominal current rating after 10-20 us from the start of short circuit (Nel & Perinpanayagam, 2016, p. 284).

GaN FETs are particularly sensitive for short circuit conditions due to their ultra-fast switching speed. Their poor thermal conductivity also results in large heat dissipation under short circuit conditions. Some studies have shown that short circuit withstand time of GaN FET is in its worst only 400 ns (Kim et al., 2022, p. 1-3). It has been noticed that at voltage levels below 300 V, E-mode GaN FETs have better short-circuit withstand time compared to GaN/Si cascode transistors but decreases when the voltage is increased (Kim et al., 2022, p. 3).

4.9.4 Dynamic R_{DSON} of GaN FET

Despite the extremely low R_{DSON} of GaN FET, according to Zhong et al. (2022, p. 468-469), there can be a significant increase in R_{DSON} immediately after device is switched from high voltage off-state to low voltage on-state. This is called dynamic on-state resistance and it leads to increased conduction losses. For the lateral GaN on Si devices, the main fault mechanisms behind the dynamic R_{DSON} are surface trapping, buffer trapping and gate instability.

According to Zhong et al. (2022, p. 468-469), after certain time after turn-on, de-trapping occurs which means that dynamic R_{DSON} settles to static R_{DSON}. However, in high frequency applications, it is possible that de-trapping does not occur because of very short on-state times. The amount of dynamic R_{DSON} depends on off-state voltage, load current, switching frequency and soaking time. Also switching mode has an impact on dynamic R_{DSON} as it has larger values in hard-switching mode when compared to soft-switching mode. Zhong et al. also state that some studies show that under the hard-switching mode and with 400 V off-state voltage, dynamic R_{DSON} can be approximately 1,55-1,60 times greater than the value of static R_{DSON}.

Though multiple studies of dynamic R_{DSON} are made, the values are not generally reported by the manufacturers. According to Khoshzaman et al. (2019, p. 1431), so far, the only reliable method to get information of dynamic R_{DSON} is to measure it. The standard method is double pulse test.

5 Laboratory measurements

In this chapter, the empirical part of thesis is presented. First, test board and devices under test are presented. Lastly, efficiency of LCC resonant converter is measured with four different transistor type.

5.1 Test board

The test board used was an LCC resonant converter with a maximum output power of 40 W, operating at input voltages ranging from 300-1350 V. A simplified block diagram of the circuit is shown in Figure 28. When a high voltage DC supply is connected to the input, the control circuit, consisting of a resonant controller and gate driver, drives the FETs in a half-bridge configuration with a constant 50% duty cycle. The leakage inductance of the primary winding and resonant capacitors located on both the primary and secondary side form a resonant tank whose resonance frequency depends on the load. As the output power is increased, the resonance frequency decreases, and when the output power is decreased, the resonance frequency increases. The frequency also depends on the input voltage; the higher the input voltage, the higher the frequency. The switching frequency is kept slightly above the resonance frequency to maintain soft switching. A feedback loop is connected from the output to the input to adjust the switching frequency according to the output voltage, which is kept constant at 24 V.

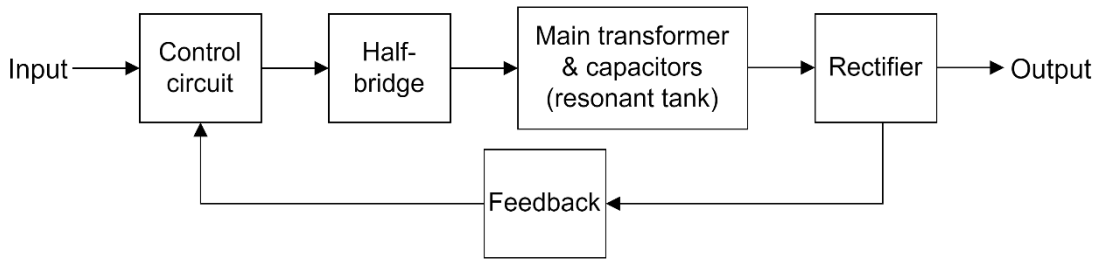

Figure 28. Block diagram of test board.

General schematic diagram of a half-bridge LCC resonant converter is shown in Figure 29. The figure shows the gate driver, high-side FET (Q_{HS}), low-side switch (Q_{LS}), main transformer connected to the switching node (SWN), leakage inductance (L_S), primary side resonance capacitors (C_1 and C_2), secondary side resonance capacitor (C_S), and rectifier.

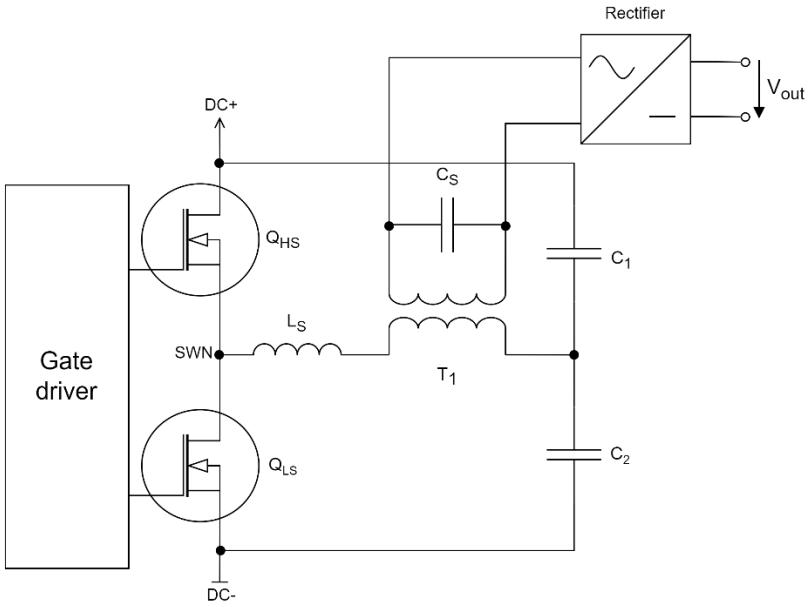

Figure 29. General schematic diagram of LCC resonant converter.

Another more commonly used resonant topology is the LLC converter. In this type of topology, the resonant tank is formed by the leakage inductance (L_S), magnetizing inductance of T_1, and an external capacitor (Nielsen, 2013, p.3) However, LCC topology is more suitable for applications where the input voltage varies by 2:1 or more (Nielsen, 2013, p.20).

5.2 Devices under test

Devices under test (DUT) are shown in Figure 30. The tested transistors were 900 V GaN/Si cascode TP90H050WS from Transphorm, 1700 V SCT2H12NZ planar SiC MOSFET

from Rohm, 1700 V IMBF170R1K0M1 trench SiC MOSFET from Infineon and 1500 V STFW4N150 SJ MOSFET from ST Microelectronics. Test board was originally assembled with SCT2H12NZ.

Figure 30. Devices under test. From left to right: GaN/Si cascode transistor, planar SiC MOSFET, trench SiC and SJ MOSFET.

The most important electrical characteristics taken from the datasheets of devices are shown in Table 3. When comparing the performance of transistors, it is desirable for them to have similar BV_{DS}, R_{DSON}, maximum I_D and package. From the table, it can be seen that BV_{DS}, R_{DSON}, and I_D of GaN/Si cascode and the R_{DSON} of Si MOSFET differ significantly from the SiC MOSFETs. However, since one of the most important parameters when choosing transistors was as high BV_{DS} as possible, some trade-offs had to be made.

The problem with E-mode GaNs is that at the moment they are only available with BV_{DS} up to 650 V. For that reason, GaN/Si cascode transistor was chosen, although with them, the maximum input voltage is still limited to 900 V (with 1000 V max transient). In addition, the gate driver of the test board was optimized to drive SCT2H12NZ with approximately -5 V for turn-off and +18 V for turn-on $V_{GS.}$ Using E-mode GaN would have required modifications to the gate driver circuit since they are driven with V_{GS} between -3

to 5 V. Instead, GaN/Si Cascode transistor with -20 to 20 V gate voltage range was used, making it easy to implement in the circuit.

According to Table 3, Q_G of the GaN/Si cascode transistor is larger than that of the SiC MOSFETs. The Si MOSFET in cascode structure may increase the Q_G, but when considering the rated I_D, which is multiple times larger than that of other transistor types, Q_G is still very small. The Si MOSFET also brings along a body diode, which is why there is a notable Q_{rr}. Thus, the benefit of GaN FET being reverse recovery loss-free is missed. However, it matters less since the device is tested in a soft-switching application. $C_{O(ER)}$ of the device is also large, which must be taken into consideration in dead time. R_{DSON} of the device is reported as including both static and dynamic values, by way of exception.

When examining the table, it is evident that the SCT2H12NZ MOSFET has a low $V_{GS(TH)}$, which is typical for planar SiC MOSFETs as discussed in earlier chapters. The table provides the minimum and maximum values of $V_{GS(TH)}$, where the minimum value indicates that turn-off can only be ensured with V_{GS} below that value. Additionally, the specific characteristics of SiC MOSFETs, such as large V_{SD} and R_G, can be observed. The improvements in performance of SiC MOSFETs due to trench technology is apparent, as IMBF170R1K0M1 trench SiC MOSFET has significantly larger $V_{GS(TH)}$ compared to planar SCT2H12NZ SiC MOSFET. Consequently, negative V_{GS} for turn-off is no longer necessary, and the recommended V_{GS} for turn-off is 0 V (see note a). The characteristics of IMBF170R1K0M1 also realizes the fact that trench technology enables SiC MOSFETs to be packed in much smaller sizes (see Figure 30) while still providing very low R_{DSON}.

Since the recommended V_{GS} range for IMBF170R1K0M1 is from 0 V to 15 V, it is not optimal for the gate driver of the test board. With 18 V_{GS} for turn-on and -5V for turn-off, the gate is being overdriven. This can, according to Infineon's application note (Infineon, 2019, p. 2), lead to positive shift in $V_{GS(TH)}$ over time, leading to an increased R_{DSON}. However, a negative shift in $V_{GS(TH)}$ has not occurred within the allowed V_{GS} range (Infineon, 2019, p. 2). IMBF170R1K0M1 also features a Kelvin connection. According to

Infineon (2013, p. 4), it serves as a voltage reference for the gate driver. By providing a short path to the source terminal, this connection eliminates voltage drops caused by parasitic inductance between the gate driver and source.

The tested Si MOSFET is a 1500 V SJ MOSFET from ST Microelectronics. When studying the R_{DSON}, Q_G, and Q_{rr} of Si MOSFET, and comparing them to the ones of GaN/Si cascode transistor and SiC MOSFETs, the advantages of WBG technology are evident. It should be still mentioned that STFW4N150 does not represent the very newest SJ technology. A newer SJ MOSFET model from the same manufacturer, the 1700 V STW12N170K5, is particularly attractive. With an R_{DSON} of 2.3 Ω, it would have been a better candidate for comparison with SiC MOSFETs. It also has a Q_G of 37 nC, which is an improvement from the 50 nC of the STFW4N150, although its Q_{rr}, at 5070 nC, is larger compared to its older counterpart. However, due to availability issues of semiconductors, the STFW4N150 was used instead.

Table 3. Electrical characteristics of DUT (@ 25°C).

Type	GaN Cascode	Planar SiC MOSFET	Trench SiC MOSFET	Si MOSFET
Manufacturer	Transphorm	Rohm	Infineon	ST Microelectronics
Model	TP90H050WS	SCT2H12NZ	IMBF170R1K0M1	STFW4N150
Package	TO-247	TO-3PF	TO-263-7	TO-3PF
V_{DS} (V)	900	1700	1700	1500
V_{GS} (V)	-20 to 20	-6 to 22	(-10 to 20)[a]	-30 to 30
$V_{GS(TH)}$ (V)	3,3 to 4,8	1,6 to 4	3,5 to 5,7	3 to 5
V_{SD} (V)	2,3	4,3	N/A	2
I_D (A)	34	3,7	5,2	4
T_{jmax} (°C)	150	175	175	150
$R_{\Theta JC}$ (°C/W)	1,05	4,32	2,2	0,78
$R_{\Theta JA}$ (°C/W)	40	50	62	50
$R_{DS(ON)}$[b] (mΩ)	63[c]	1500	880	7000
R_G (Ω)	NA	64	35	NA
Q_G (nC)	16	14	5	50
Q_{RR} (nC)	145	13	N.A	3000
$C_{O(ER)}$ (pF)	150	17	2,6[d]	N/A

Notes :

[a]Maximum transient voltage, <1% duty cycle. Recommended V_{GS} for turn-on=12 V to 15 V and for turn-off=0 V.

[b]Maximum value.

[c]Reflects both static and dynamic on-resistance.

[d]Datasheet reports only E_{OSS}. C_{OSS} calculated by using equation:

$$C_{O(ER)} = \frac{2 \cdot E_{OSS}}{V_{DS}^2}, \quad (12)$$

where E_{OSS} is energy stored in output capacitance during turn-off (Toshiba, 2023, p. 5).

5.3 Test setup

The test setup is shown in Figure 31. The high-voltage power supply was connected to the test board, and the electronic load was connected to the output. The switching node voltage (V_{SWN}) and V_{GS} of the low-side FET were measured with an oscilloscope. In addition, current of the low-side FET was measured in two measurements. The input voltage and input current were observed from the screen of the HV-supply. The load voltage (V_L) was measured with a multimeter, and the load current was observed from the screen of the electronic load. The temperatures of the FETs were measured with a thermal camera during testing. The tests were conducted at a temperature of 25°C. The test equipment is shown in Table 4.

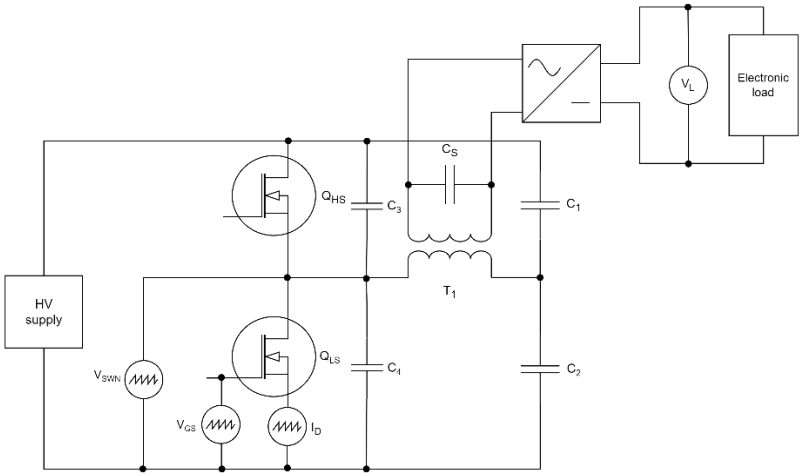

Figure 31. Test setup.

Table 4. Test equipment.

LPS 750-HVP high-voltage power supply
Tektronix DPO 3034 oscilloscope
Tektronix P5205 differential probe
Metrahit M249A multimeter
B&K Precision 8540 electronic load
CWT015 Rogowski current waveform transducer
Flir E53 thermal camera

5.4 Inspection

Before beginning the efficiency measurement, each transistor was tested with a 300 V input voltage and no load to ensure that ZVS was achieved, and the FETs were operating correctly. It is crucial for V_{SWN} to go negative before the transistor is switched on, as it indicates that device conducts in reverse direction and ZVS is achieved.

In the case of the GaN/Si cascode, it was observed that the transistor was switched on before the ZVS condition was reached. This can be seen in Figure 32 where it is evident that V_{DS} is forced to go low by V_{GS} while V_{DS} is still decreasing. Furthermore, significant oscillations occur at V_{GS} during Q_{LS} off-state (Q_{HS} on-state), which could inadvertently turn on Q_{LS} while Q_{HS} is conducting, resulting in shoot-through between the transistors.

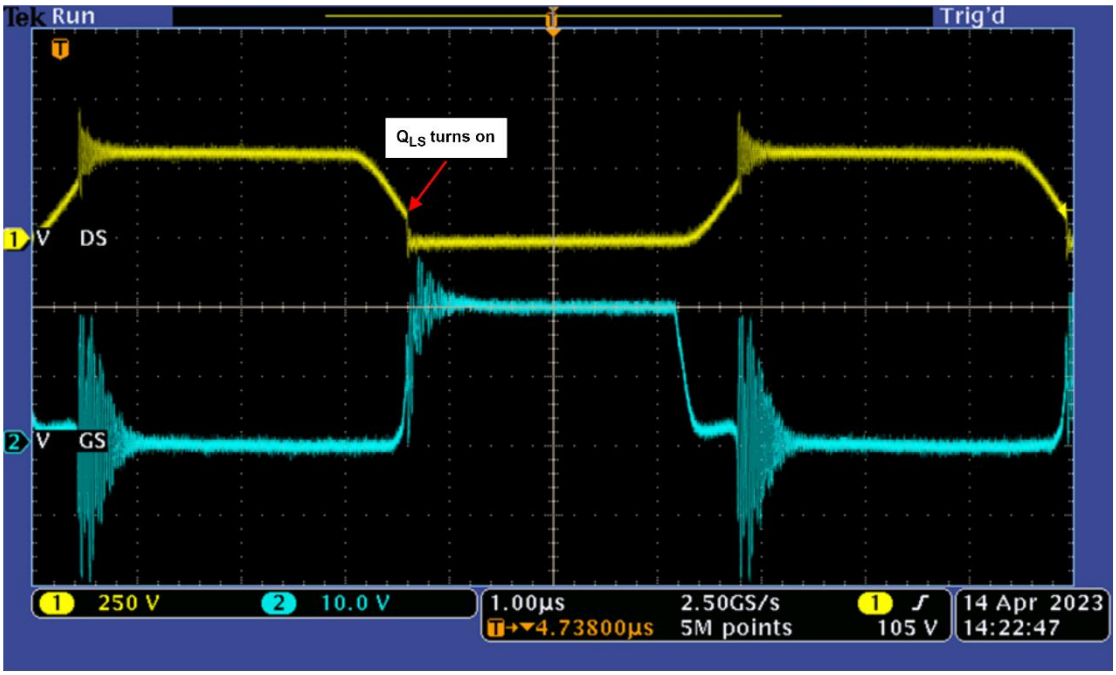

Figure 32. Voltage waveforms of GaN/Si cascode with 300 V input voltage and without load. CH1: V_{SWN}, CH2: V_{GS}.

The removal of capacitors C_3 and C_4 appeared to reduce the oscillation, although it persisted, and the transistor still turned on prematurely. However, when the dead time was increased from its initial value of 548 ns to 812 ns, the oscillation issue was entirely

resolved, and ZVS was achieved. Figure 33 shows the voltage waveforms of the GaN/Si cascode after the modification.

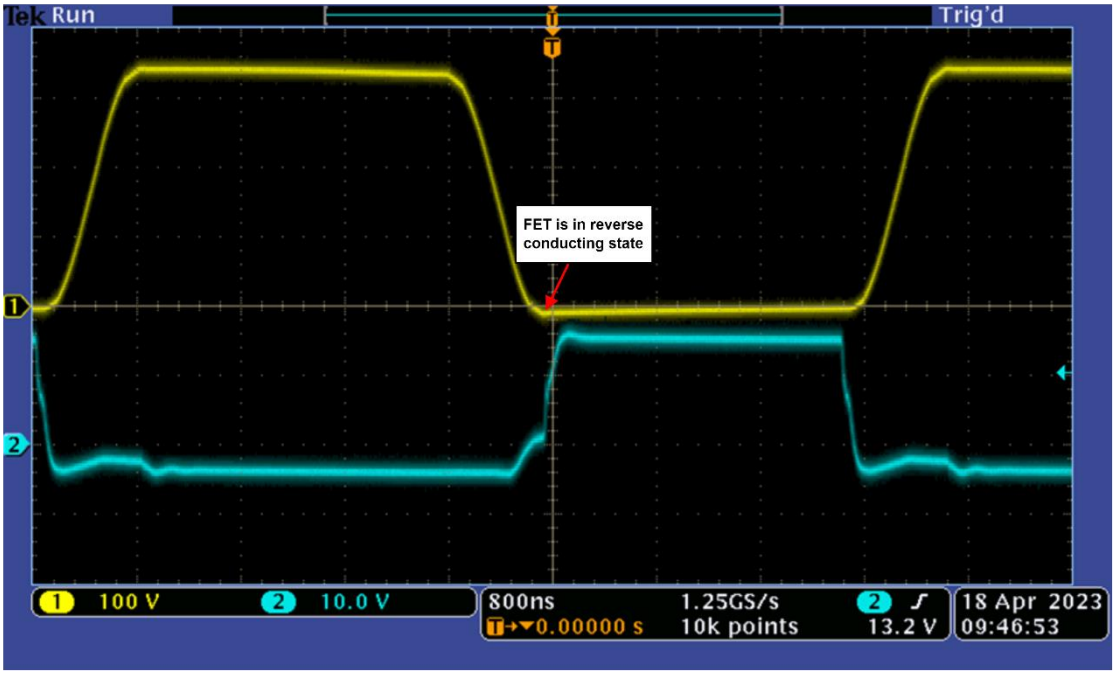

Figure 33. Voltage waveforms after modification. CH1: V_{SWN} , CH2: V_{GS}.

5.5 Efficiency measurements

Electronic load was set to a constant current of 1 A, and the input voltage was increased from 300 V to 900 V in 100 V steps. The output voltage was measured to be 24,2 V, resulting in an output power of 24,2 W. The input current was checked at each step, and the efficiency was calculated using the equation:

$$\eta = \frac{V_L \cdot I_L}{V_{in} \cdot I_{in}}, \tag{13}$$

where V_L is output voltage, I_L load current, V_{in} input voltage and I_{in} input current.

The results are presented in Figure 34. The efficiency curves for planar and trench SiC MOSFETs overlap and are equal at every input voltage level. In contrast, the efficiency of the Si MOSFET is lower than that of the SiC MOSFETs at every input voltage level. The difference between the Si MOSFET and the SiC MOSFETs slightly increases with increasing input voltage, reaching a maximum of about 2,5%.

The efficiency of the GaN/Si cascode is equal to the values of both SiC MOSFETs at 300 V and 400 V input voltage, but it starts to fall behind after 400 V, eventually falling below the efficiency of the Si MOSFET after 500 V. After 700 V, its efficiency begins to fall very dramatically, having approximately a 9,3% difference from the SiC MOSFETs at 900 V input voltage. The poor efficiency was easy to realize when the case temperature of the device was measured to be 86,4 °C immediately after increasing the input voltage to 900 V, whereas the case temperature of the other transistors under the same conditions were 32.1 °C (planar SiC MOSFET), 31.9 °C (trench SiC MOSFET), and 36.2 °C (Si MOSFET). Although it would have been desirable to increase the output power since efficiency increases when the load increases, it was not reasonable to do so due to the strong power dissipation of the GaN/Si cascode.

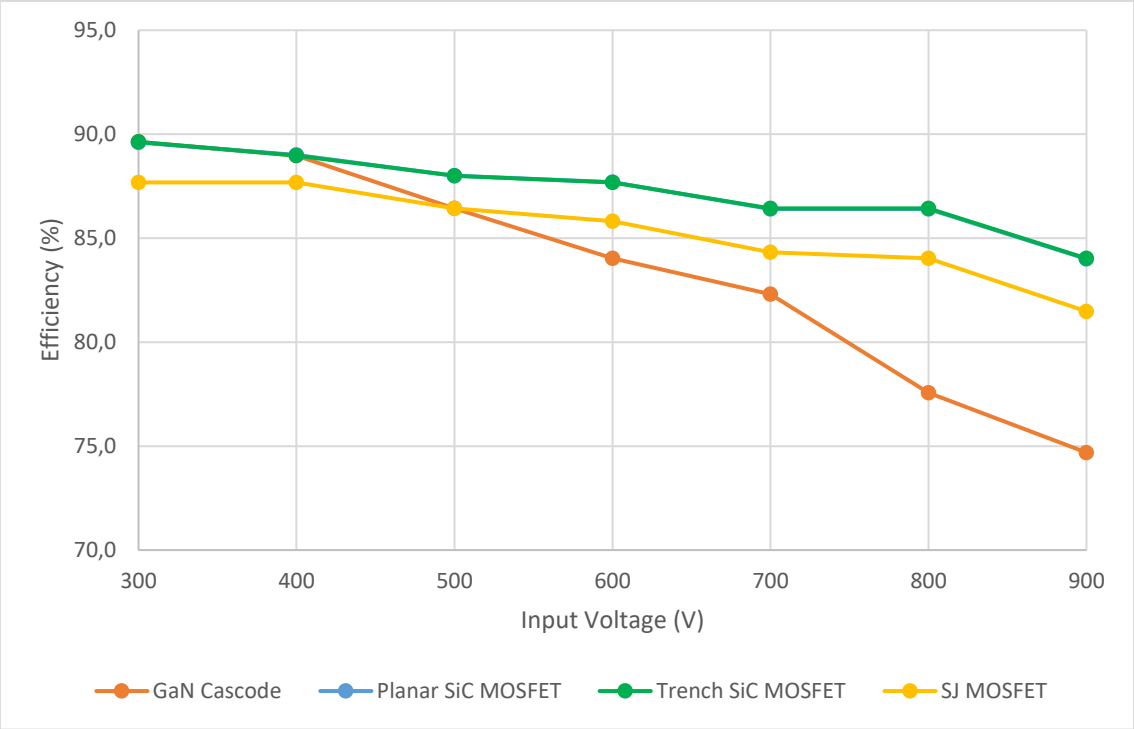

Figure 34. Efficiency of transistors at 300–900 V voltage and 1 A constant load. The efficiency curves for the planar and trench SiC MOSFETs overlap.

V_{SWN} and V_{GS} of each transistor at 900 V input voltage and with 1 A load current are shown in Figure 35, Figure 36, Figure 37 and Figure 38. According to figures, voltage waveforms of each transistor look clean and stable. Measured switching frequency at 900 V and 1 A was 175 kHz.

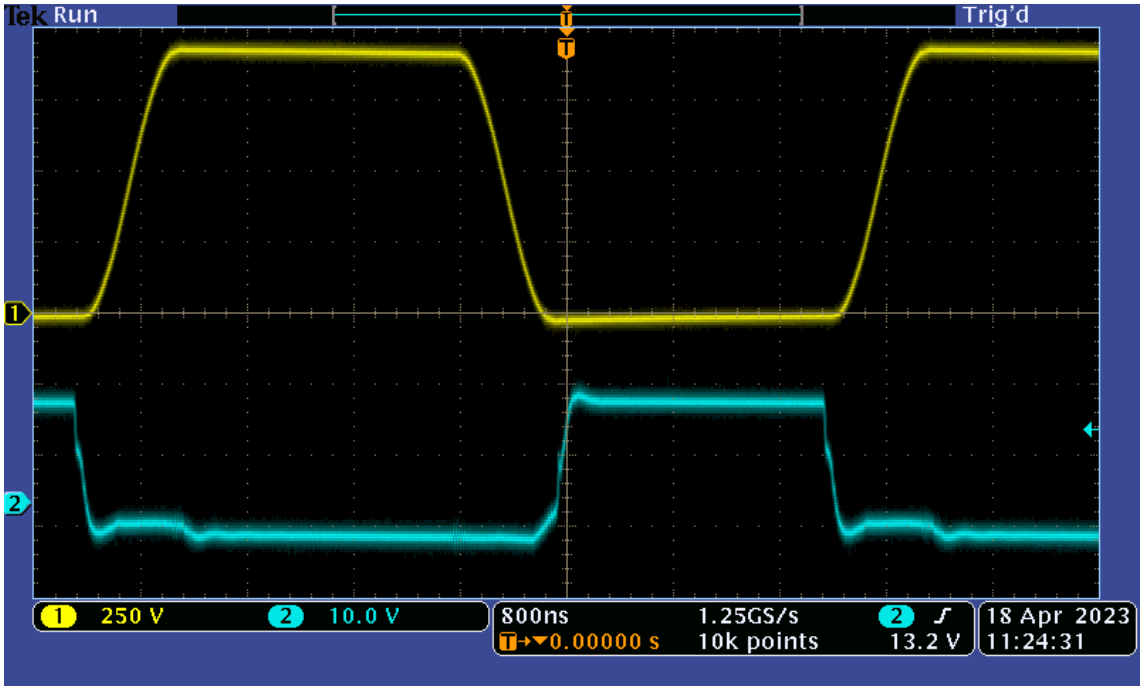

Figure 35. Voltage waveforms of GaN/Si cascode transistor with 1 A load and 900 V input voltage. CH1: V_{SWN}, CH2: V_{GS}.

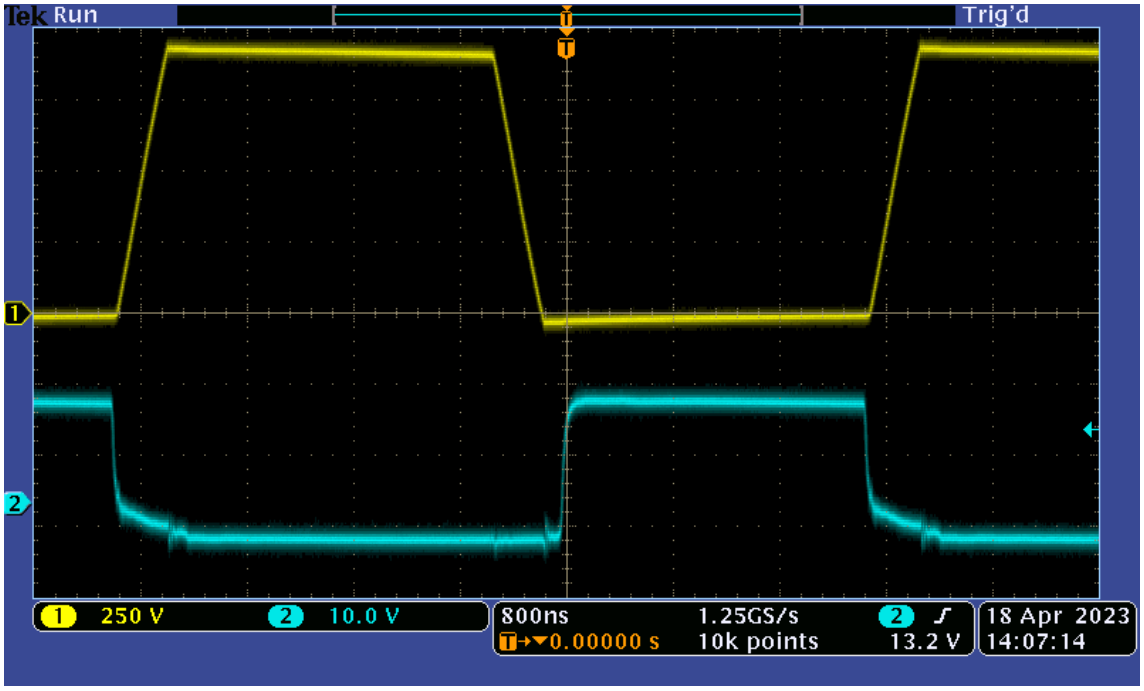

Figure 36. Voltage waveforms of planar SiC MOSFET with 1 A load and 900 V input voltage. CH1: V_{SWN}, CH2: V_{GS}.

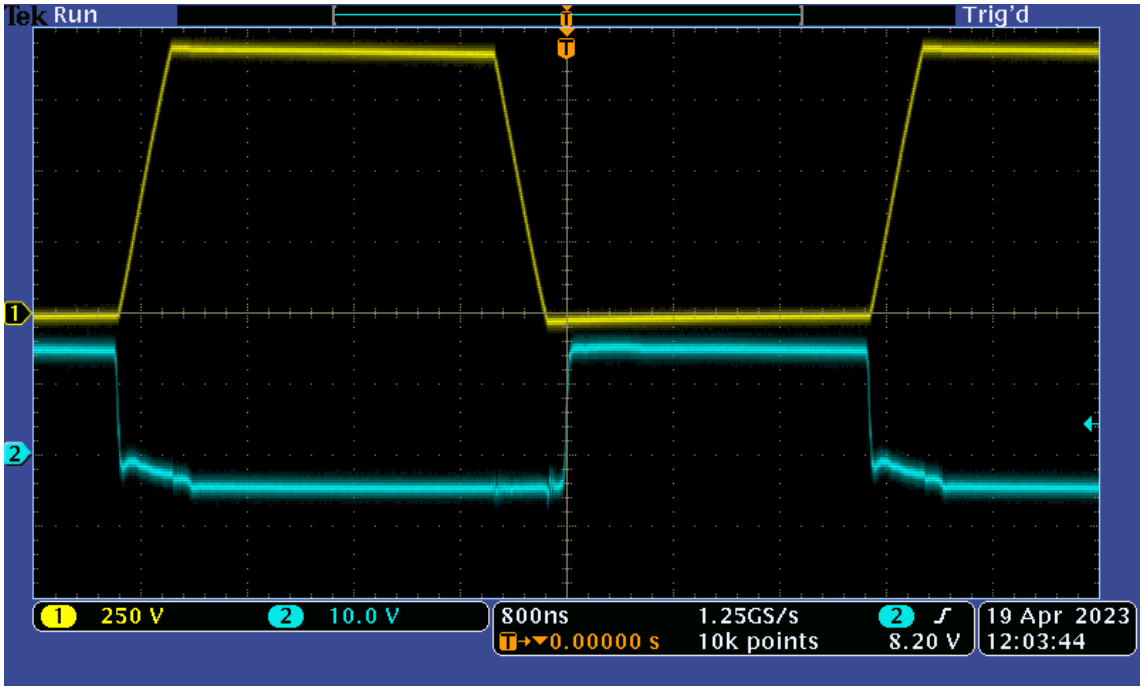

Figure 37. Voltage waveforms of trench SiC MOSFET with 1 A load and 900 V input voltage. CH1: V_{SWN}, CH2: V_{GS}.

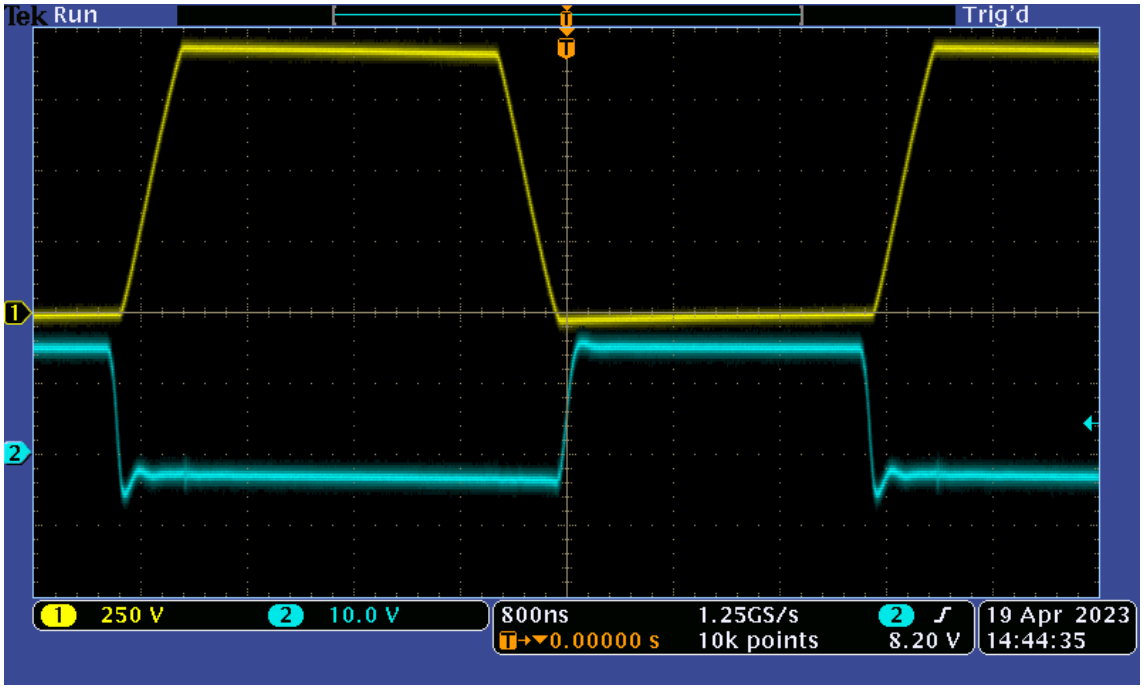

Figure 38. Voltage waveforms of Si MOSFET with 1 A load and 900 V input voltage. CH1: V_{SWN}, CH2: V_{GS}.

The current waveform of the low-side GaN/Si cascode transistor was inspected using an oscilloscope to determine the reason for the large heat dissipation. Figure 39 shows the waveform of the current and voltage V_{SWN} at 900 V input voltage and 1 A load current. According to the measurements, nothing unusual that explains the large heat dissipation of the GaN/Si cascode was found. Capacitance mismatch-related current leakage, discussed in Section 4.6, was under suspicion, but if that were the case, there should be a positive current peak on the negative-going slope after V_{DS} starts to decrease and C_{OSS} discharges. There is neither a large negative peak at the point where the reverse current (I_S) peaks. The current waveform and V_{SWN} of the planar SiC MOSFET were measured as a reference, and the results are shown in Figure 40.

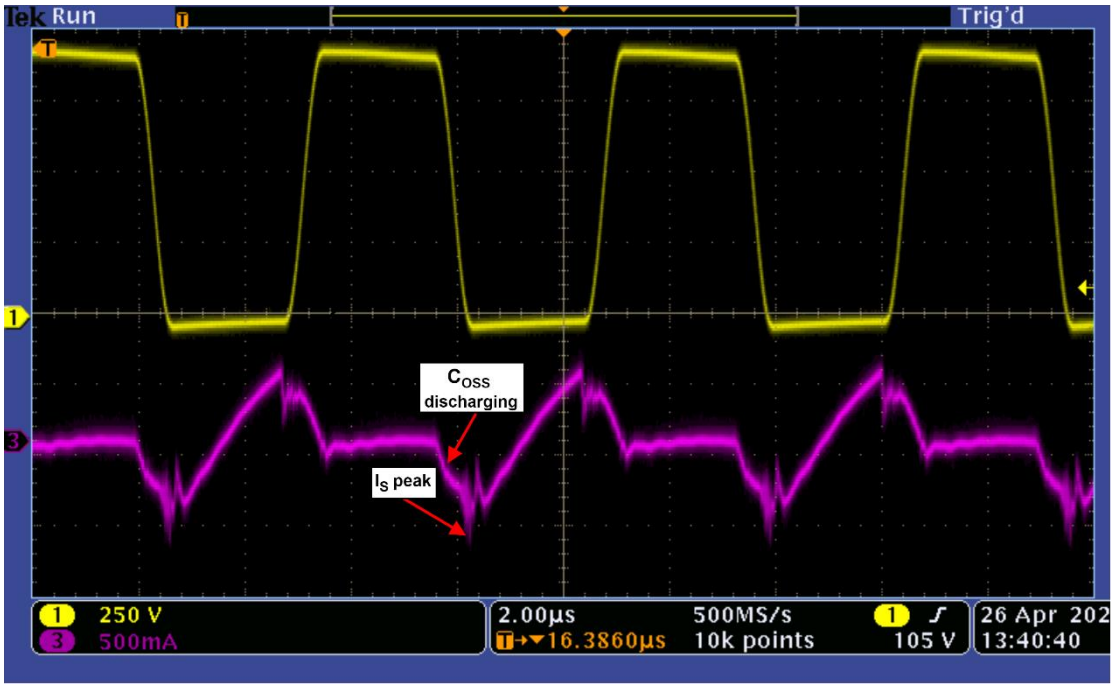

Figure 39. Current and V_{SWN} of low-side FET with 1 A load and 900 V input voltage. GaN/Si cascode. CH1: V_{SWN}, CH3: Current of FET.

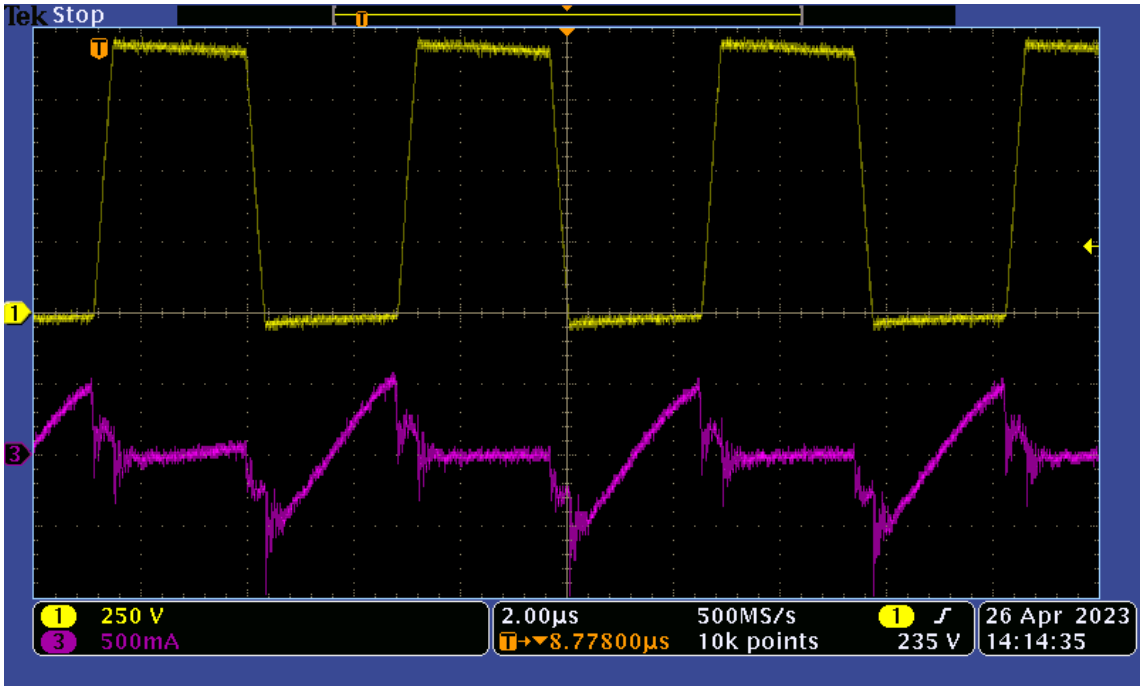

Figure 40. Current and V_{SWN} of low-side FET with 1 A load and 900 V input voltage. Planar SiC MOSFET. CH1: V_{SWN}, CH3: Current of FET.

6 Conclusions

At moment, main SiC MOSFET and GaN FET technologies available in the field of high-voltage switching applications are planar SiC MOSFET, trench SiC MOSFET, double-trench SiC MOSFET, p-GaN FET and GaN/Si cascode transistor. While planar SiC MOSFETs are widely studied and used in converter designs, their biggest disadvantage is their thin gate oxide, which leads to reliability issues. On the other hand, single trench technology provides improvement to those issues, still suffering about new reliability issues which come mainly from the electric field concentration to the gate trench. The technology has further developed with the double-trench technology, which provides more uniform electric field. Manufacturers do not generally separate trench and double-trench technologies on their application notes or datasheets, so it may be hard to know if the technology is single trench or double trench. P-GaN FETs have superior switching capabilities and extremely low R_{DSON} while their usage in high voltage applications is significantly limited due to their lateral structure, which reduces their voltage blocking capability. GaN/Si cascode technology combines depletion mode GaN FET and Si MOSFET, which allows a little higher blocking voltage, but at the same time, some GaN technology advantages, like avoiding recovery loss is missed. It has to be mentioned, that while WBG technologies outperform conventional Si MOSFETs in many features, super junction technology still makes Si MOSFET a good choice in many applications.

All WBG transistor technologies have their unique characteristics. The first to mention is breakdown voltage. When considering technologies with reasonable R_{DSON} (<5 Ω), planar SiC MOSFETs come with the breakdown voltage up to 1700 V, while trench SiC MOSFETs are capable up to 2000 V breakdown voltages. The lateral structure of GaN FET limits its breakdown voltage to max 650 V (p-GaN FET) and 900 V (GaN/Si cascode). Table 5 shows electrical characteristics studied in this research. While max BV_{DS} and max T_j are stated as absolute values, other parameters are normalized to Si MOSFET.

Table 5. Electrical characteristics of WBG transistors. Max BV_{DS} and max T_j are stated as absolute values while other parameters are normalized to Si MOSFET.

Technolgy	Planar SiC MOSFET	Trench SiC MOSFET	P-GaN FET	GaN/Si cascode transistor
Max BV_{DS} (V)	1700	2000	650	900
Avalanche capability	High	High	N.A	Low
$V_{GS(TH)}$	Low	Similar	Low	Similar
V_{GS} turn-on	High	High	Low	Similar
V_{GS} turn-off	Low	Similar	Low	Similar
R_{DSON}	Low	Low	Low	Low
R_G	High	High	Similar	Similar
Q_G	Low	Low	Low	Low
V_{SD}	High	High	High	High
P_{RR}	Low	Low	N.A	Low
Max T_J (°C)	175	175	150	150

The LCC converter's efficiency was tested using four different transistor technologies. The best efficiencies measured were 87,7 % for SJ MOSFET and 89,6 % for planar SiC MOSFET, trench SiC MOSFET, and GaN/Si cascode transistor. However, it is not possible to draw any major conclusions based on this minor test. A more in-depth analysis would be required, for example, by varying the load and temperature. Additionally, the efficiency of the GaN/Si transistor strongly decreased with higher voltages, and a significant temperature increase was observed when measuring the case temperature of the device. More experiments are still needed to gain comprehensive knowledge about using GaN/Si in high voltage switching applications.

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