CHALMERS
UNIVERSITY OF TECHNOLOGY

Parameters Design and Optimization of SiC MOSFET Driving Circuit with Consideration of Comprehensive Loss and Voltage Stress

micromachines

MDPI

Article

Parameters Design and Optimization of SiC MOSFET Driving Circuit with Consideration of Comprehensive Loss and Voltage Stress

Haihong Qin [1,*], Zhenhua Ba [1], Sixuan Xie [1], Zimo Zhang [1], Wenming Chen [1] and Qian Xun [2]

[1] Department of Electrical Engineering, the Center for More-Electric-Aircraft Power System, Nanjing University of Aeronautics and Astronautics, Nanjing 211106, China
[2] Department of Electrical Engineering, Chalmers University of Technology, 41279 Gothenburg, Sweden
* Correspondence: qinhaihong@nuaa.edu.cn; Tel.: +86-025-84890132

Abstract: In conventional parameters design, the driving circuit is usually simplified as an RLC second-order circuit, and the switching characteristics are optimized by selecting parameters, but the influence of switching characteristics on the driving circuit is not considered. In this paper, the insight mechanism for the gate-source voltage changed by overshoot and ringing caused by the high switching speed of SiC MOSFET is highlighted, and we propose an optimized design method to obtain optimal parameters of the SiC MOSFET driving circuit with consideration of parasitic parameters. Based on the double-pulse circuit, we evaluated the influence of main parameters on the gate-source voltage, including driving voltage, driving resistance, gate parasitic inductance, and stray inductance of the power circuit. A SiC-based boost PFC is constructed and tested. The test results show that the switching loss can be reduced by 7.282 W by using the proposed parameter optimization method, and the over-voltage stress of SiC MOSFET is avoided.

Keywords: driving circuit; parameters optimization; gate-source voltage; SiC MOSFET

Citation: Qin, H.; Ba, Z.; Xie, S.; Zhang, Z.; Chen, W.; Xun, Q. Parameters Design and Optimization of SiC MOSFET Driving Circuit with Consideration of Comprehensive Loss and Voltage Stress. *Micromachines* **2023**, *14*, 505. https://doi.org/10.3390/mi14030505

Academic Editors: Jose M. Sosa-Zuñiga and Sadia Ameen

Received: 10 January 2023
Revised: 8 February 2023
Accepted: 19 February 2023
Published: 21 February 2023

1. Introduction

To reduce carbon emissions, it is crucial to improve the efficiency of motor drives to promote the development of electric vehicles, new energy power generation, and other industries [1,2]. As a typical wide bandgap (WBG) device, silicon carbide (SiC) metal-oxide-semiconductor field-effect-transistor (MOSFET) shows great advantages over silicon (Si) MOSFET in terms of on-resistance, switching speed, and thermostability [3–5]. The replacement of Si MOSFETs with SiC MOSFETs can improve the efficiency and power density of power electronics and promote the development of motor drives [6]. However, the high switching speed of SiC MOSFET makes it very sensitive to parasitic parameters in the circuit [7,8], and the voltage and current are susceptible to producing overshoot and oscillation [9,10]. Also, this increases the electrical stress of the device, resulting in accelerated aging and even failure of the device. To ensure the safety of SiC MOSFET devices, designing an efficient and reliable driving circuit is necessary and becomes an urgent task.

At present, for the design of driving circuit parameters of SiC MOSFET, researchers have noticed the characteristics of SiC MOSFET and made special consideration from the aspects of driving voltage setting, driving chip current capacity, rise/fall time, PCB layout, and so on. SiC device manufacturers provide recommended driving voltage in their technical manuals, but these values are simply estimated and are not considered in conjunction with other driving parameters of the actual driving circuit. In ref. [11], the effects of driving resistance and parasitic capacitance of SiC MOSFET on the maximum turn-on speed are studied. However, turn-off switching characteristic analysis and driving resistance selection guidance methods are not given. In ref. [12], the influence of different

driving voltage, driving resistance, and gate-source capacitors on the switching characteristics of SiC MOSFET are analyzed to suppress the oscillation and overshoot, but this method will increase the switching time of the device. In ref. [13], the appropriate driving resistor is selected by comprehensively considering the switching loss and temperature rise. In ref. [14], the RLC response of the driving circuit is analyzed, and the parasitic inductance optimization method is given considering the nonlinear characteristics of the capacitor. Reference [15] studies the influence of driving voltage and driving resistance on suppressing gate oscillation through the loss change and damping effect. Among these methods, the coupling effects of the power circuit are not considered, which may cause the actual gate-source voltage to exceed the design value.

However, due to the high $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ of SiC MOSFET, its interaction with circuit parasitic parameters will produce obvious voltage and current oscillation. In ref. [16], the influence of circuit parasitic parameters on gate-source voltage is mainly discussed. In ref. [17], the RLC second-order equivalent circuit model is proposed for the turn-on and turn-off of SiC MOSFET. A simple mathematical formula is derived, which provides a theoretical analysis basis for the study of the switching oscillation phenomenon of SiC MOSFET and has important guiding significance for the design of buffer or damping circuits. During the actual testing, we found that the overshoot and ringing of the power circuit will have a great impact on the gate-source voltage and increase the gate voltage stress. However, this phenomenon is often mistaken for the second-order oscillation of the driving circuit itself. Therefore, the influence of high-frequency oscillation on the gate-source voltage must be considered when designing the driving circuit parameters of SiC MOSFET. Since the dynamic characteristics of SiC devices are closely related to stray parameters in the circuit, a method to extract stray inductance and capacitance of the power circuit is proposed [18]. In ref. [19], the gate oscillation caused by $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ feedback is analyzed. It is proposed to increase the driving resistance and parallel gate-source capacitance to suppress the oscillation, but the selection guideline of driving resistance is not given. In ref. [20], the switching dynamic characteristic analysis model is proposed according to the datasheet and the parasitic effect of the external circuit, but the dynamic characteristic of gate-source voltage is not analyzed. Moreover, due to the additional loss caused by the oscillation peak, the switching loss will also increase. Therefore, the influence of oscillation loss should be considered in the loss calculation to make the calculation results more accurate [21].

In this paper, the mechanism of voltage and current ringing coupled to gate-source voltage is analyzed, the relevant mathematical model is established, and the parameters optimization design method is proposed. This method can reduce the switching loss and conduction loss as much as possible and ensure gate reliability. The rest of the paper is organized as follows. In Section 2, the mathematical model of gate-source voltage considering the coupling relationship of the power circuit is developed. In Section 3, based on the consideration of balancing comprehensive loss and overvoltage stress, the parameter-optimized design method for the driving circuit is proposed. Section 4 gives the experimental results and Section 5 concludes the work.

2. Modeling of Transient Gate-Source Voltage

The SiC MOSFET double pulse test circuit is shown in Figure 1 where the main parasitic parameters are also considered. V_{DC} is the bus voltage, I_{l} is the load current, and C_{L} is the parasitic capacitance of the load inductor. $\mathrm{D_H}$ is the ideal SiC SBD and C_{J} is the equivalent junction capacitance of SiC SBD. C_{GS}, C_{GD}, and C_{DS} are the gate-source capacitance, gate-drain capacitance, and drain-source capacitance of SiC MOSFET respectively, $L_{\mathrm{D(int)}}$ and $L_{\mathrm{S(int)}}$ are parasitic inductance introduced by drain and source pins in SiC MOSFET package respectively, $R_{\mathrm{G(int)}}$ is the gate internal resistance of SiC MOSFET, and $R_{\mathrm{G(ext)}}$ is the external driving resistance, L_{G} is the parasitic inductance of the driving circuit. $L_{\mathrm{D(ext)}}$ and R_{loop} are the equivalent parasitic inductance and stray resistance of the PCB wiring between the

positive terminal of the DC bus and the drain of SiC MOSFET respectively, $L_{S(ext)}$ is the parasitic inductance of the line between SiC MOSFET source and ground.

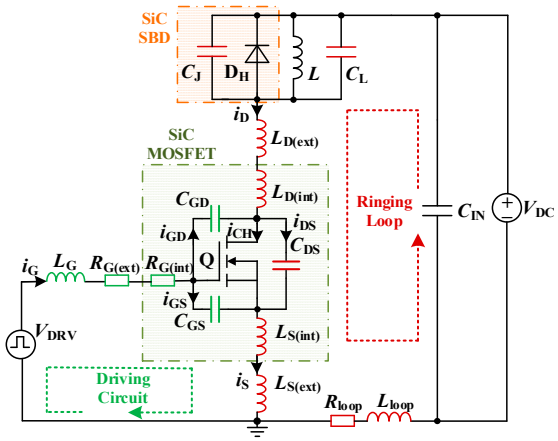


Figure 1. Double pulse circuit considering parasitic parameters for SiC MOSFET.

The double pulse test circuit is used to develop the mathematical model of gate-source voltage. Due to parasitic parameters, the switching process of the SiC MOSFET is shown in Figure 2.

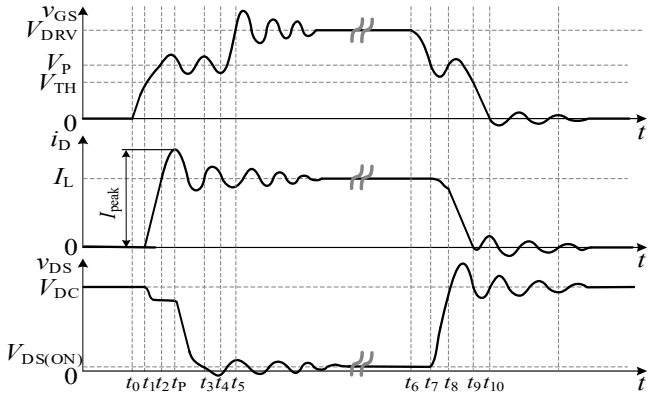


Figure 2. Switching waveform of SiC MOSFET considering parasitic parameters. From top to bottom: gate-source voltage v_{GS}, drain current $i_{D,}$ and drain-source voltage v_{DS}.

The turn-on process can be divided into five stages according to the change of current and voltage, which is described below:

1. Stage 1 [t_0~t_1]

At the time instance t_0, the input capacitance C_{ISS} starts to charge, and the gate-source voltage v_{GS} rises, whereas, the drain current i_D and drain-source voltage v_{DS} do not change. The gate-source voltage at this stage can be expressed as:

$$v_{GS} = \frac{1}{L_{GS}C_{ISS}s^2 + R_G C_{ISS}s + 1} \times \frac{V_{DRV}}{s} \quad (1)$$

where the input capacitance follows $C_{ISS} = C_{GS} + C_{GD}$, the gate-source inductance follows $L_{GS} = L_G + L_{S(int)}$, and the driving resistance follows $R_G = R_{G(int)} + R_{G(ext)}$. The driving voltage is V_{DRV}, which is equivalent to step excitation in the zero-state response of the driving circuit.

According to (1), the driving circuit parameters are the main factors affecting the gate-source voltage v_{GS}.

2. Stage 2 [t_1~t_2]

At the time instance t_1, the gate-source voltage reaches the threshold voltage, the channel begins to turn on and the drain current i_D gradually rises. Due to the small dv_{DS}/dt, the current flowing through the parasitic capacitance of SiC MOSFET is also small, the channel current i_{CH} can be approximately regarded as the drain current, which can be expressed as:

$$v_{GS}(t) = \frac{i_D(t)}{g_{fs}} + V_{TH} \tag{2}$$

$$i_D = \frac{\omega_{0(2)}^2 g_{fs}(V_{DRV} - V_{TH})}{s^2 + 2\delta_{(2)}s + \omega_{0(2)}^2} \tag{3}$$

where

$$\begin{cases} \delta_{(2)} = \frac{R_G\left(C_{GS}+C_{GD}+g_{fs}R_{loop}C_{GD}\right)+g_{fs}L_{S(int)}}{2g_{fs}R_G L_{stray}C_{GD}} \\ \omega_{0(2)} = \frac{1}{\sqrt{g_{fs}R_G L_{stray}C_{GD}}} \end{cases} \tag{4}$$

The gate-source voltage increases from the threshold voltage to the Miller voltage with the drain current increasing. It can be seen from (4) that the factors affecting the gate-source voltage include the parasitic capacitance and transfer characteristics of SiC MOSFET, driving resistance, stray parameters of the power circuit, and working conditions.

3. Stage 3 [t_2~t_3]

At the time instance t_2, the drain current i_D increases to the load current I_L, and the current of SiC SBD decreases to zero. At this time, the parasitic capacitances of the power circuit (C_J and C_L) are charged by the reverse voltage, and the drain current i_D spikes and causes high-frequency oscillation. This stage is in the Miller platform stage, which can be subdivided into two stages [t_2~t_P] and [t_P~t_3] according to the changes in drain current and drain-source voltage. More details are shown below.

(a) [t_2~t_P]

The drain current i_D begins to overshoot at the time instance t_2 and reaches the current peak I_{peak} at the time instance t_P, while the drain current change rate di_D/dt decreases to zero. Due to the change of i_D, the gate-source voltage v_{GS} starts to rise from Miller voltage V_P, and the peak of Miller platform voltage at t_P can be expressed as:

$$v_{GS}(t_P) = \frac{I_{peak}}{g_{fs}} + V_{TH} \tag{5}$$

The drain current i_D can be expressed as:

$$i_D = \frac{L_{stray}\left.\frac{di_D(t)}{dt}\right|_{t=t_2}}{L_{stray}(C_J + C_L)s^2 + R_{loop}(C_J + C_L)s + 1} \tag{6}$$

Since the stray resistance, R_{loop}, is very small and follows ${\delta_{(31)}}^2 < \omega_{0(31)}$, the power circuit works in the underdamped state. From (6), it can be seen that the current peak I_{peak} is related to the switching speed and stray parameters of the power circuit. These factors will also affect the voltage peak of the gate-source voltage v_{GS} at this stage.

(b) [t_P~t_3]

At the time instance t_P, the drain current i_D begins to decrease and the drain-source voltage v_{DS} also decreases. Due to the large change rate of drain-source voltage dv_{DS}/dt, the displacement current on the parasitic capacitance of SiC MOSFET cannot be ignored. Therefore, the channel current i_{CH} is no longer approximate to the drain current, which can be expressed as:

$$i_{CH}(t) + g_{fs}\Delta v_{GS}(t) = g_{fs}(V_{DRV} - V_{TH}) \tag{7}$$

$$v_{GS}(t) = \frac{i_{CH}(t)}{g_{fs}} + V_{TH} \tag{8}$$

$$i_D = \frac{\frac{g_{fs}(V_{DRV}-V_{TH})C_H+(C_{OSS}+g_{fs}R_GC_{GD})I_L}{C_H(C_{OSS}+g_{fs}R_GC_{GD})}}{L_{stray}s^2 + \left(R_{loop} + \frac{g_{fs}L_{S(int)}}{C_{OSS}+g_{fs}R_GC_{GD}}\right)s + 1} \tag{9}$$

where

$$\begin{cases} \delta_{(32)} = \frac{R_{loop}+\frac{g_{fs}L_{S(int)}}{C_{OSS}+g_{fs}R_GC_{GD}}}{2L_{stray}} \\ \omega_{0(32)} = \sqrt{\frac{C_H+C_{OSS}+g_{fs}R_GC_{GD}}{L_{stray}C_H(C_{OSS}+g_{fs}R_GC_{GD})}} \end{cases} \tag{10}$$

where the output capacitance follows $C_{OSS} = C_{GD} + C_{DS}$, and the equivalent parasitic capacitance follows $C_H = C_J + C_L$.

According to (7)~(9), the gate-source voltage is related to the drain current at this time. It can be seen that there is an oscillation component in the drain current, which is related to the parasitic capacitance and transfer characteristics of SiC MOSFET, driving circuit parameters, power circuit stray parameters, and working conditions.

4. Stage 4 [t_3~t_4]

At the time instance t_3, the drain-source voltage v_{DS} drops to $V_{DS(ON)}$. At this time, the drain current i_D can be expressed as:

$$i_D = \frac{I_L}{L_{stray}(C_J + C_L)s^2 + R_{loop}(C_J + C_L)s + 1} \tag{11}$$

The general solution of drain current i_D can be expressed as:

$$i_D(t) = I_L + e^{-\delta_{(4)}(t-t_3)}\left\{K_{1(4)}\cos\left[\omega_{(4)}(t-t_3)\right] + K_{2(4)}\sin\left[\omega_{(4)}(t-t_3)\right]\right\} \tag{12}$$

where

$$\begin{cases} K_{1(4)} = i_D(t_3) - I_L \\ K_{2(4)} = \frac{\frac{di_D(t)}{dt}\Big|_{t=t_3} + \delta_{(4)}K_{1(4)}}{\omega_{(4)}} \end{cases} \tag{13}$$

The gate-source voltage v_{GS} continues to rise from Miller voltage V_P. At the same time, the current ringing senses the voltage ringing on the common source parasitic inductance $L_{S(int)}$ and is coupled to the gate circuit to become an excitation source, so that the gate-source voltage v_{GS} superimposes high-frequency oscillation.

$$\Delta v_{GS} = \frac{K_{3(4)}\left[s\sin\psi + \omega_{(4)}\cos\psi\right]}{\left[\left(s+\delta_{(1)}\right)^2 + {\omega_{(1)}}^2\right]\left[\left(s+\delta_{(4)}\right)^2 + {\omega_{(4)}}^2\right]} \tag{14}$$

where

$$\begin{cases} K_{1(4)} = i_D(t_3) - I_L \\ K_{2(4)} = \frac{\frac{di_D(t)}{dt}\Big|_{t=t_3} + \delta_{(4)}K_{1(4)}}{\omega_{(4)}} \end{cases} \tag{15}$$

Then the expression of gate-source voltage v_{GS} at this time is:

$$v_{GS}(t) = V_{DRV}\left\{1 + 2\left|K_{4(4)}\right|e^{-\delta_{(1)}(t-t_3)}\cdot\cos\left[\omega_{(1)}(t-t_3) + \theta\right]\right\} + \Delta v_{GS}(t) \tag{16}$$

where

$$\left.\frac{\frac{V_{\mathrm{DRV}}}{L_{\mathrm{GS}}C_{\mathrm{GS}}}\cdot\left(s+\delta_{(1)}-\mathrm{j}\omega_{(1)}\right)}{s\cdot\left[\left(s+\delta_{(1)}\right)^2+{\omega_{(1)}}^2\right]}\right|_{s=-\delta+\mathrm{j}\omega}=\left|K_{4(4)}\right|e^{\mathrm{j}\theta} \tag{17}$$

It can be seen from (16) that in addition to the second-order oscillation caused by the driving circuit, the gate-source voltage will also superimpose the high-frequency oscillation from the power circuit. The factors affecting the gate-source voltage include driving circuit parameters, power circuit parameters, and working conditions.

5. Stage 5 [t_4~t_5]

At the time instance t_4, the gate-source voltage rises to V_{DRV}, and then the gate-source voltage spike and attenuation oscillation appear. The gate-source voltage at this stage is:

$$v_{\mathrm{GS}}(t)=V_{\mathrm{DRV}}\{1+2\left|K_{(5)}\right|e^{-\delta_{(1)}(t-t_4)}\cdot\cos\left[\omega_{(1)}(t-t_4)+\theta\right]\}+\Delta v_{\mathrm{GS}}(t) \tag{18}$$

where $K_{(5)} = K_{4(4)}$, and the definition of other parameters is the same as that in stage 4.

The generation mechanism of Δv_{GS} in the turn-off process is similar to that in the turn-on process, which will not be repeated. According to the mathematical model, when considering the influence of switching ringing, the driving circuit cannot be simply equivalent to an RLC circuit and the gate-source voltage will superimpose a high-frequency oscillation voltage Δv_{GS}, which is related to the switching speed and power circuit parameters. Δv_{GS} will increase the overshoot and oscillation amplitude of gate-source voltage. Therefore, the influence of $\mathrm{d}i/\mathrm{d}t$ and stray inductance of the power circuit must be considered when designing driving parameters.

3. Parameter Optimized Design Method

We propose an optimized design method for driving parameters considering the influence of parasitic parameters in the power circuit, as shown in Figure 3. The methodology is divided into three steps to illustrate the process of selecting the optimal driving parameters. The main steps are described as follows.

Step I: Since the gate-source inductance and stray inductance are the main factors causing gate oscillation, the PCB layout should be optimized as much as possible to make the parasitic inductance less than the recommended value.

Step II: To ensure gate reliability, there is a margin between the maximum allowable gate-source voltage $v_{\mathrm{GS(max)}}$ and the gate-source withstand voltage V_{GSS}. Then the driving parameters combination (V_{DRV}, R_{G}) is calculated according to the $v_{\mathrm{GS(max)}}$.

Step III: Since the switching loss and conduction loss of the power transistor is different under different driving parameters, the driving circuit parameters should be determined according to the principle of optimal comprehensive loss, which means the combination of switching loss and conduction loss for the device approaches minimum under this set of driving parameter.

This parameter optimization design method fully considers the influence of ringing caused by parasitic parameters on gate-source voltage and ensures the gate reliability of SiC MOSFET by optimizing stray inductance without affecting the switching speed as much as possible.

3.1. Parasitic Parameters Design of Power Circuit

To reduce the turn-on current spike, the equivalent junction capacitances C_{J} and C_{L} should be as small as possible. Therefore, SCS240AE2 (SiC SBD, Rohm) and an air-core inductor are selected. Also, to reduce the stray loss, the stray resistance R_{loop} should be as small as possible.

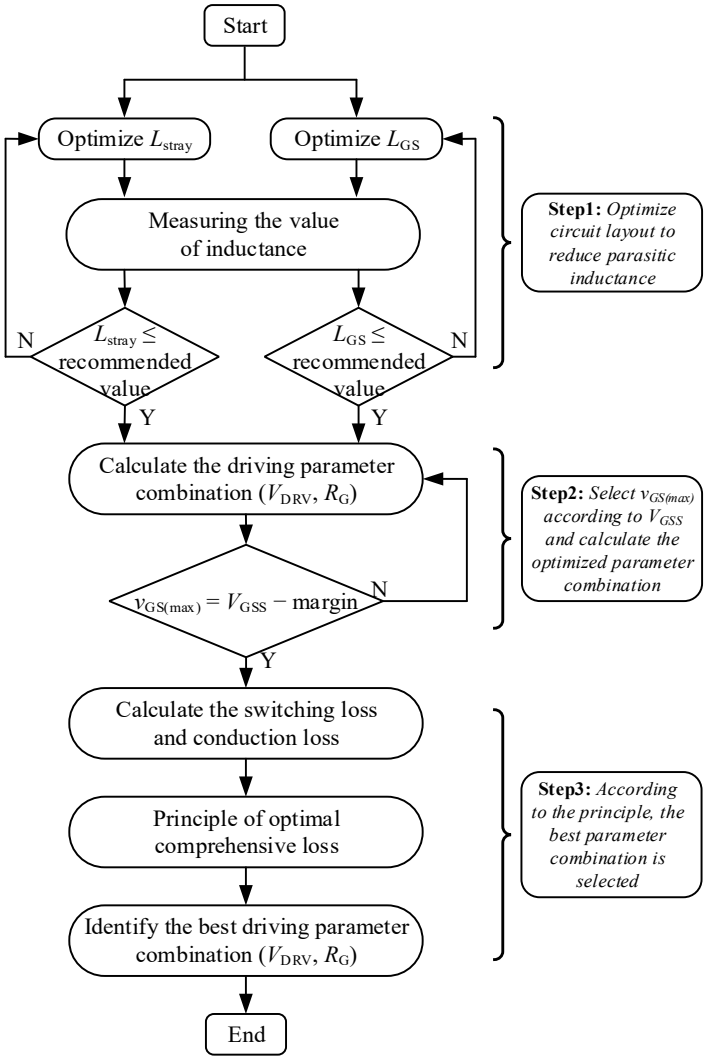


Figure 3. Methodology for optimizing driving parameters of SiC MOSFET.

When designing the stray inductance L_{stray}, for different stray inductances, the maximum gate-source voltage $v_{GS(max)}$ is limited by dynamically changing the gate-source inductance L_{GS} and the driving resistance R_G. At the same time, the switching energy loss and device stress are paid attention to, and the acceptable design range of stray inductance L_{stray} is obtained. The specific parameters and experimental test data are shown in Table 1, and SiC MOSFET SCT3060AL (650 V/39 A, Rohm) used for simulation has 12 Ω internal gate resistance.

Table 1. Circuit parameters and testing data.

V_{DRV}/V	L_{GS}/nH	L_{stray}/nH	R_G/Ω	$v_{DS(max)}$/V	E_{on}/μJ	E_{off}/μJ
18	40	3	13.5	421	210.78	29.957
		60	17	569	187.78	81.901
		100	19	572	190.47	97.740
		105	21	582	194.02	131.39
		260	32	641	222.21	310.43
18	20	15	12	497	188.70	25.689
		60	13	608	163.65	42.792
		80	14	631	155.68	54.227
		95	15	640	152.85	69.766
		125	17	645	148.47	102.05

In the simulation, the bus voltage V_{DC} is 400 V and the load current I_L is 20 A. The maximum voltage $v_{GS\,(max)}$ is limited to 21 V when the gate-source inductance L_{GS} is 40 nH and 20 nH, respectively. Figure 4 shows the switching processes of SiC MOSFET with various stray inductances.

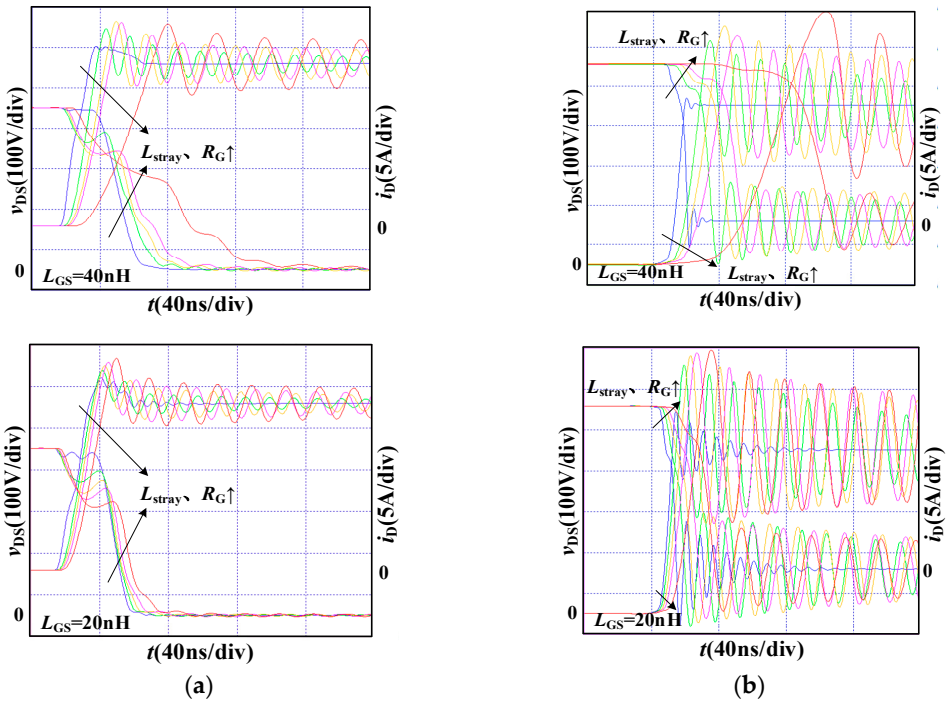


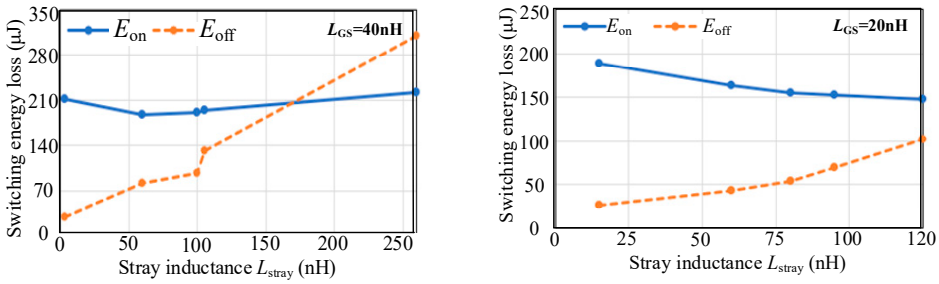
Figure 4. Switching waveforms under different stray inductance L_{stray}. (**a**) turn-on process; (**b**) turn-off process.

Under the condition that V_{DRV} is 18 V and R_G is 17 Ω, the stray inductance L_{stray} is designed with the following constraints. It cannot exceed 60 nH when the gate-source inductance L_{GS} is 40 nH and cannot exceed 125 nH when L_{GS} is 20 nH. The larger gate-source inductance L_{GS} causes the larger gate-source voltage oscillation under the same V_{DRV} and R_G, then the acceptable stray inductance L_{stray} will be smaller.

When the gate-source inductance L_{GS} is 40 nH and 20 nH respectively, the maximum stray inductance L_{stray} limited by the voltage stress is reduced from 260 nH to 125 nH. The smaller gate-source inductance L_{GS} allows a faster switching speed under the same V_{DRV} and R_G. This results in the increase of the turn-off voltage spike and the decreasing acceptable range of stray inductance L_{stray}.

Figure 5 shows the influence of different gate-source inductance L_{GS} and stray inductance L_{stray} on the switching energy loss of the device. The larger L_{stray} results in the larger driving resistance R_G to suppress the gate-source voltage oscillation leading to a slower switching speed. During the turn-on process, it can be seen from (9) that the larger L_{stray} gives the smaller voltage platform in stage 2 and the turn-on loss is reduced. In summary, the turn-on energy loss decreases first and then increases, and the turn-off energy loss increases due to the increase of R_G.

According to the above analysis and considering the voltage stress, switching energy loss, and physical space limitation of the circuit, the stray inductance L_{stray} should not exceed 60 nH.



(**a**) (**b**)

Figure 5. Switching energy loss under different L_{stray}. (**a**) L_{GS} = 40 nH; (**b**) L_{GS} = 20 nH.

3.2. Parasitic Parameters Design of Driving Circuit

Under the optimized parasitic parameters of the power circuit, the gate-source voltage oscillation and voltage stress can be optimized. On this basis, by limiting the maximum gate-source voltage $v_{GS(max)}$ to 21 V and adjusting the parameters of the driving circuit, the switching loss and conduction loss of the device can be effectively reduced, and the driving parameters can be optimized with respect to the optimal comprehensive loss. When L_{stray} is 60 nH and $v_{GS(max)}$ is 21 V, the specific driving circuit parameters and test data are shown in Table 2.

Table 2. Circuit parameters and testing data.

L_{GS}/nH	V_{DRV}/V	R_G/Ω	$v_{DS(max)}$/V	E_{on}/μJ	E_{off}/μJ
40	15.8	12	639	234.88	39.152
	17.2	15	602	197.48	56.987
	18.0	17	569	187.78	81.901
	18.7	19	538	181.85	91.592
	19.5	21	520	183.85	119.06
	21.0	40	468	290.55	270.85
20	17.1	12	618	185.59	34.702
	18.0	13	608	163.65	42.792
	18.6	14	597	157.93	52.501
	19.0	15	583	154.74	63.532
	19.3	16	564	154.00	73.093
	21.0	30	479	219.30	198.44

Figure 6 shows the switching processes under different gate-source inductance L_{GS}, driving resistance $R_{G,}$ and driving voltage V_{DRV}. When R_G increases, V_{DRV} will also increase at the same time under the same gate-source inductance L_{GS}, and the turn-on current peak increases slightly. Since the positive driving voltage does not affect the turn-off process, the turn-off voltage spike decreases. Under the same driving resistance R_G, the smaller L_{GS} gives the higher V_{DRV}, which makes the turn-on current peak decreases slightly. Since the positive driving voltage does not affect the turn-off process, the turn-off voltage spike decreases.

Figure 7 shows the effects of different driving parameters L_{GS}, $R_{G,}$ and V_{DRV} on the comprehensive loss of the device. When R_G increases and V_{DRV} also increases under the same L_{GS}, the turn-on energy loss E_{on} decreases firstly and then increases, and the conduction loss decreases. Since the positive driving voltage does not affect the turn-off process and the turn-off loss continues to increase, the comprehensive loss first decreases and then increases. Under the same R_G, the smaller L_{GS} is, the higher V_{DRV} can be, and the turn-on loss and conduction loss are reduced. Since the positive driving voltage does not affect the turn-off loss, thus the comprehensive loss is reduced.

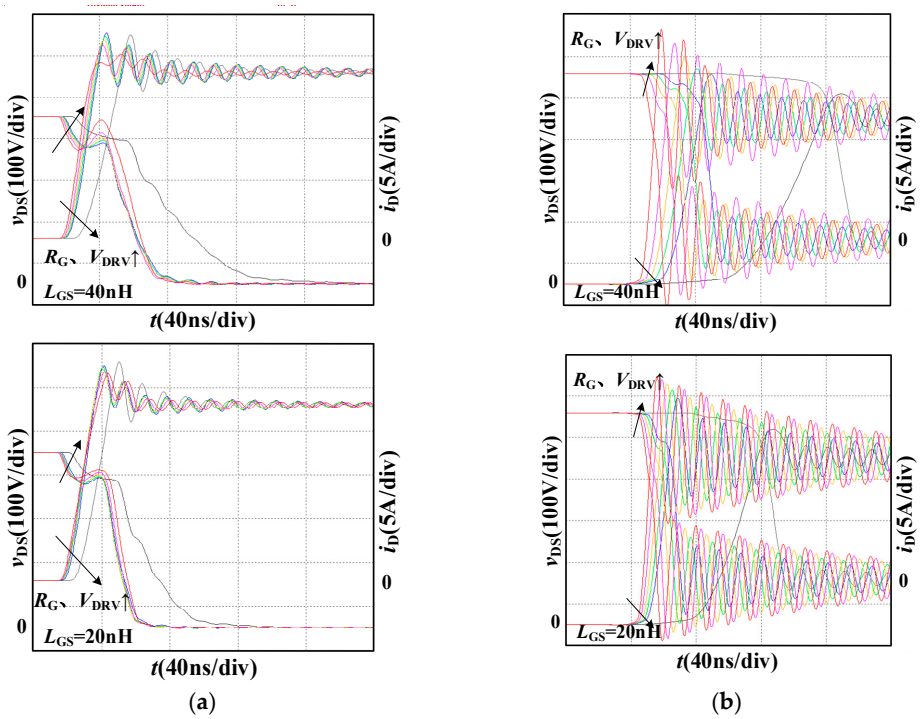


Figure 6. Switching waveforms under different driving parameters. (**a**) turn-on process; (**b**) turn-off process.

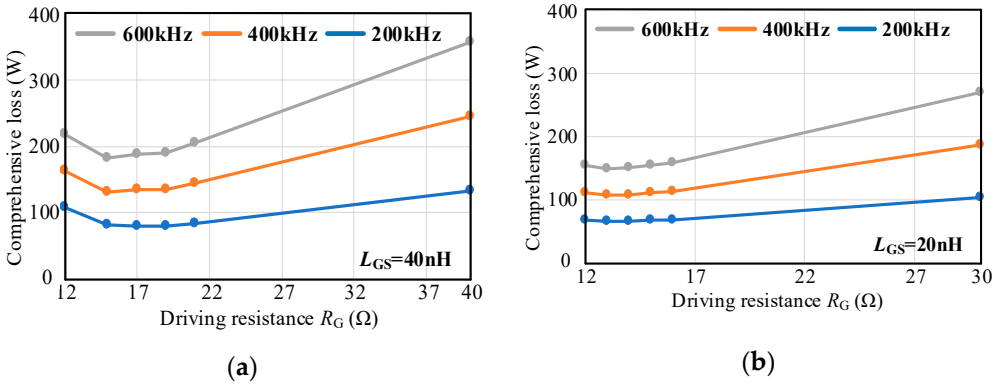
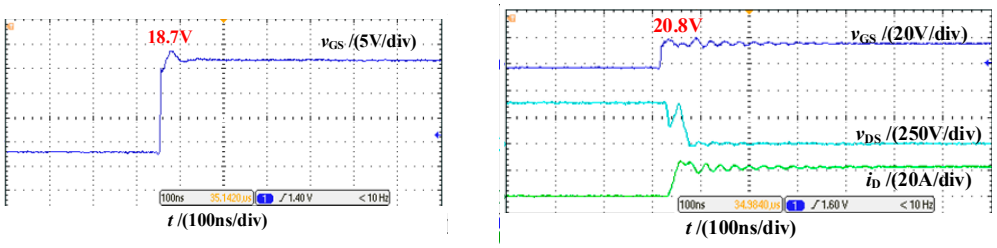


Figure 7. Comprehensive loss under different driving parameters. (**a**) L_{GS} = 40 nH; (**b**) L_{GS} = 20 nH.

According to the principle of optimal comprehensive loss, when L_{GS} is 40 nH, the optimized value of R_G is 15 Ω, and the damping ratio is 1.09. When L_{GS} is 20 nH, the optimized value of R_G is 13 Ω, and the damping ratio is 1.34. It can be seen that the smaller the gate-source inductance L_{GS}, the greater the damping ratio of the optimal driving parameters. This is because the decrease of L_{GS} increases the switching speed, resulting in more serious high-frequency oscillation and higher damping is required to suppress this oscillation.

4. Experimental Verification and Discussion

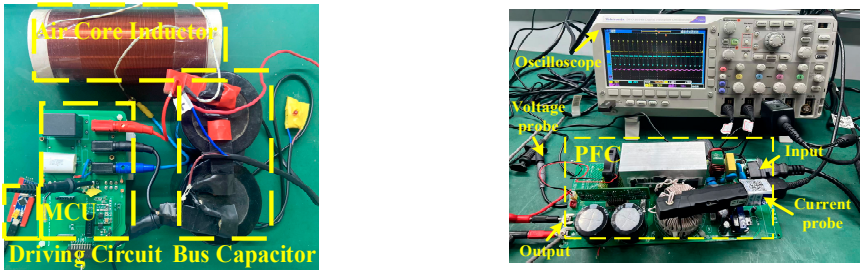
As shown in Figure 8, under the same driving circuit parameters, when SiC MOSFET is not connected to the power circuit, the gate-source voltage overshoot is 1.7 V and the steady-state recovery time is 125 ns. When SiC MOSFET operates at 400 V/20 A, the gate-source voltage overshoot increases to 3.8 V and the steady-state recovery time increases to 300 ns. This means that the ringing of the power circuit will be coupled to the driving circuit.



(**a**) (**b**)

Figure 8. Gate-source voltage waveform under different operating conditions. (**a**) Power circuit not connected; (**b**) Bus voltage & load current: 400 V/20 A.

To evaluate the influence of different driving parameter combinations (V_{DRV}, R_G) on the comprehensive loss and voltage stress of SiC MOSFET (SCT3060AL, Rohm, Kyoto, Japan), the switching characteristics of SiC MOSFET are tested on a double pulse test circuit and a multi-pulse test circuit, as shown in Figure 9. The test conditions are described in Table 3.



(**a**) (**b**)

Figure 9. Experimental platform. (**a**) Double pulse test (DPT); (**b**) Multi pulse test (MPT).

Table 3. Experimental test conditions.

Type	V_{DC}/V	I_L/A	L_{GS}/nH	(V_{DRV}, R_G)/(V, Ω)
DPT	400	20	42.52	(15.2, 12), (16.8, 14), (17.6, 16), (18.8, 18), (20.0, 20), (20.0, 22).
MPT	400	8	19.34	(17.0, 12), (17.6, 14), (18.8, 16), (20.0, 18), (20.0, 20), (20.0, 22).

4.1. Double Pulse Test

The switching waveform of SiC MOSFET under different driving parameter combinations is shown in Figure 10. Different combinations of driving parameters are selected to limit the maximum gate-source voltage $v_{GS(max)}$ to 21 V. Obviously, with the decrease of R_G, the oscillation amplitude of the gate-source voltage v_{GS} will increase. As R_G decreases from 22 Ω to 12 Ω, the voltage v_{GS} overshoot increases from 1.2 V to 7.2 V. R_G decreases while V_{DRV} decreases, and the turn-on current stress decreases from 24.5 A to 23.0 A. The positive driving voltage has little effect on the turn-off process, the turn-off voltage peak increases from 485 V to 595 V with the decrease of R_G, which increases by 22.68%.

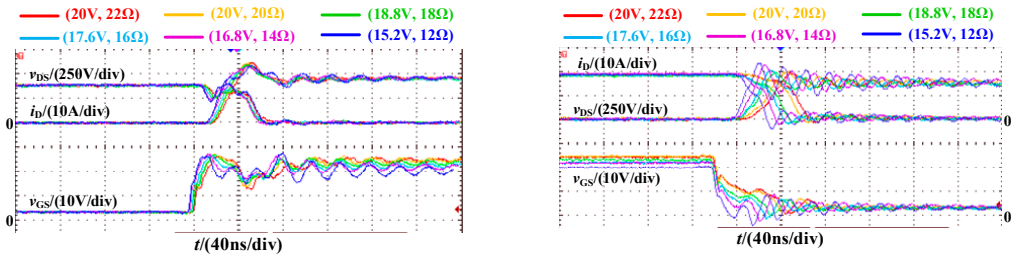


Figure 10. Switching waveform of SiC MOSFET under different driving parameter combinations in DPT. (**a**) Turn-on process; (**b**) Turn-off process.

Figure 11 shows the switching energy loss and comprehensive loss of SiC MOSFET under different driving parameter combinations, in which the switching energy loss is obtained by integrating the intersection part of voltage and current waveform of an oscilloscope, and the comprehensive loss includes switching loss and conduction loss, switching loss is obtained by multiplying the switching energy loss by the switching frequency. As R_G decreases, the gate-source voltage overshoot increases, resulting in limited V_{DRV} and increased turn-on energy loss. When the R_G decreases from 22 Ω to 12 Ω, the turn-on energy loss increases from 153.8 μJ to 217.2 μJ, which increased by 41.22%. The positive driving voltage has little effect on the turn-off process. Therefore, the smaller R_G gives the smaller the turn-off energy loss. When the R_G decreases from 22 Ω to 12 Ω, the turn-off energy decreases by 35.59%. According to the comprehensive loss under different switching frequencies, it can be seen that compared with the combination of (15.2 V, 12.0 Ω), the comprehensive loss of (22.0 V, 22.0 Ω) is reduced by 30.175 W at 200 kHz and 49.89 W at 600 kHz. With the increase in switching frequency, the combination of driving parameters with small switching energy loss shows better performance.

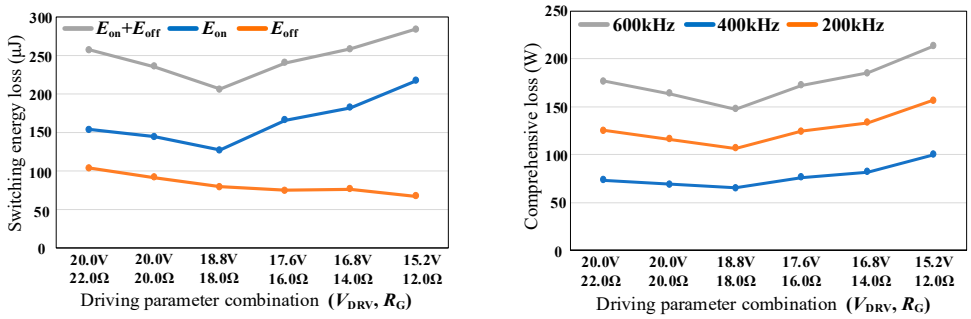


Figure 11. Switching energy loss and comprehensive loss under different driving parameter combinations. (**a**) switching energy loss; (**b**) comprehensive loss.

Based on the principle of optimal comprehensive loss, when L_{GS} is 42.52 nH, we select (18.8 V, 18.0 Ω) as the best combination of driving parameters (V_{DRV}, R_G).

4.2. Multi Pulse Test

To further verify the effectiveness of the proposed method, the experiment is conducted on a boost PFC converter through a multi-pulse test. The gate-source inductance L_{GS} is optimized below 20 nH. The multi-pulse waveforms and switching waveforms under different driving parameter combinations are shown in Figure 12. It can be seen that when the gate-source inductance L_{GS} is 20 nH, the driving circuit itself does not oscillate even if the driving resistance R_G is 12 Ω. At this time, the oscillation of gate-source voltage is only caused by the high-frequency oscillation of the power circuit. The influence of

driving parameter combination on switching characteristics decreases with the decrease of gate-source inductance. As the driving resistance R_G decreases, the switching speed increases slightly, and the high-frequency oscillation amplitude of the gate-source voltage also increases slightly.

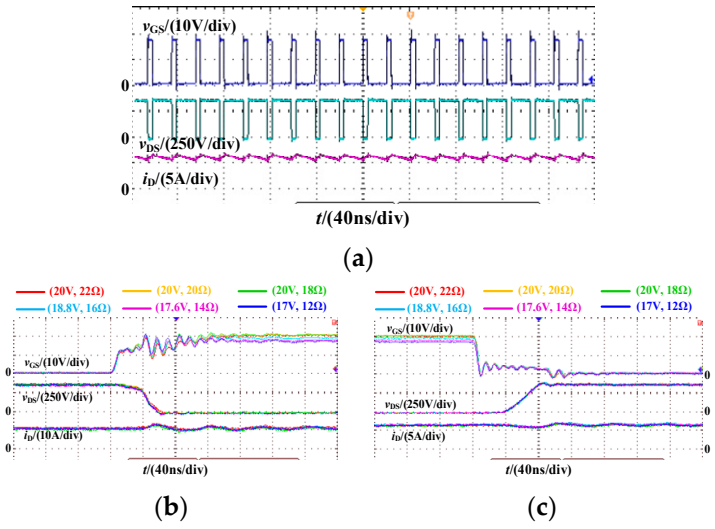


Figure 12. Multi pulse and switching waveform of SiC MOSFET. (**a**) Multi pulse; (**b**) Turn-on process; (**c**) Turn-off process.

The switching energy loss of SiC MOSFET and the efficiency of Boost PFC converter under different driving parameter combinations are shown in Figure 13. Similar to the double pulse experimental results, the total switching energy loss of SiC MOSFET also decreases first and then increases. The efficiency curve of Boost PFC corresponds to the switching energy loss of SiC MOSFET. In the optimized six groups of driving parameter combinations, the maximum difference in switching energy loss is 36.41 μJ, the maximum difference in switching loss is 7.282 W and the maximum difference in efficiency is 0.086%.

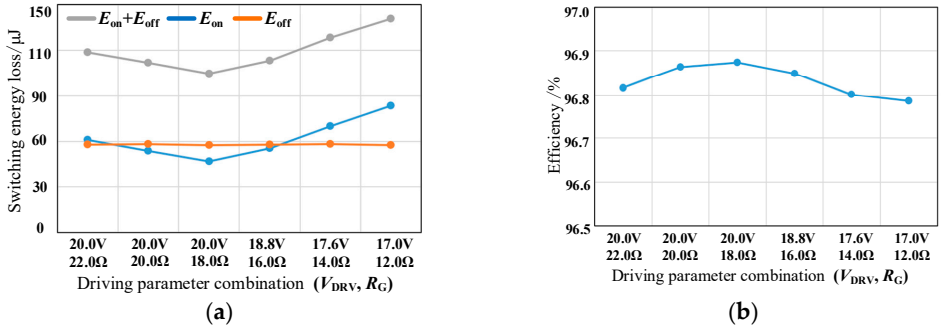


Figure 13. Loss and efficiency under different driving parameter combinations. (**a**) switching energy loss; (**b**) efficiency.

Figure 14 shows the total loss distribution of the Boost PFC converter at the switching frequency of 200 kHz. The loss of each part of the Boost PFC converter is calculated according to its commonly used loss model [22]. The switching loss of SiC MOSFET accounts for 30.7% of the total loss. Because the gate-source inductance L_{GS} is optimized and six groups of driving parameter combinations selected in the experiment are optimized, the change in efficiency is not obvious. The efficiency difference is calculated according to the switching energy loss difference and switching frequency, and the results are consistent with the experiment.

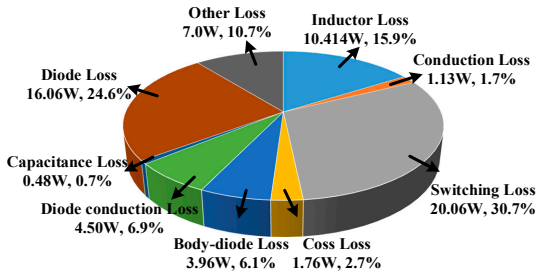


Figure 14. Power loss distribution of Boost PFC converter.

Based on the consideration of optimal comprehensive loss, when L_{GS} is 19.34 nH, select (20.0 V, 18.0 Ω) as the best combination of driving parameters. According to the previous analysis, if L_{GS} can continue to be optimized, V_{DRV} can be further increased under the same driving resistance and the comprehensive loss will be further reduced.

5. Conclusions

The ringing in the power circuit will be coupled to the driving circuit through the junction capacitance and common source parasitic inductance of the SiC MOSFET, so the gate-source voltage superimposes the high-frequency oscillation. Based on the parasitic parameters of SiC MOSFET, a mathematical model of gate-source voltage considering the influence of power circuit ringing is established in this paper. Then based on the model, a methodology is proposed to optimize the parameters of the SiC driving circuit with respect to an optimal comprehensive loss of SiC MOSFET and ensure its reliable electrical stress. Through comprehensive experiments, the reliability and comprehensive loss of the driving circuit are taken as evaluation indexes, this paper shows the influence mechanism of different stray inductances and driving circuit parameters on overshoot and ringing of gate-source voltage, gives the best driving parameters combination under different gate-source parasitic inductances.

The parameters optimization method consists of three main steps. In the first step, through the compact design of the circuit layout, the parasitic inductance in the circuit will be optimized below the recommended value, which will reduce the high-frequency oscillation and gate oscillation of SiC MOSFET, and optimize other driving parameters to reduce the comprehensive loss. In the second step, the combinations of driving parameters are optimized in a narrow range. In the third step, the optimal driving parameter combination is identified, which optimizes the comprehensive loss of SiC MOSFET under the condition of ensuring voltage stress. Using this method, the optimizing driving parameters can be obtained, and the switching loss is reduced by 7.28 W in a 200 kHz Boost PFC converter.

Author Contributions: Conceptualization, H.Q. and S.X.; methodology, H.Q. and S.X.; investigation, H.Q., Z.B., S.X., Z.Z., W.C. and Q.X.; writing—S.X. and Z.B.; writing—review and editing, H.Q., Z.B., S.X., Z.Z., W.C. and Q.X.; visualization, S.X.; supervision, H.Q. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the National Natural Science Foundation of China, under Grant 51677089, and in part by the State Key Laboratory of Wide-Bandgap Semiconductor Power Electronic Devices, China, under Grant 2019KF001.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Mohamed, A.H.R.; Vansompel, H.; Sergeant, P. Power density boosting techniques for reconfigurable integrated modular motor drives. *IEEE Trans. Energy Convers.* **2022**, *37*, 1634–1643. [CrossRef]
2. Luo, H.; Gao, H.; Zhu, C.; Li, W.; He, X. Review and prospect of IGBT chip technologies for electric vehicles. *Proc. CSEE* **2020**, *40*, 5718–5730.

3. Hazra, S.; Madhusoodhanan, S.; Bhattacharya, S.; Moghaddam, G.K.; Hatua, K. Design considerations and performance evaluation of 1200V, 100A SiC MOSFET based converter for high power density application. In Proceedings of the 2013 IEEE Energy Conversion Congress and Exposition (ECCE), Denver, CO, USA, 15–19 September 2013; pp. 4278–4285.
4. Qian, Z.; Zhang, J.; Sheng, K. Status and development of power semiconductor devices and its applications. *Proc. CSEE* **2014**, *34*, 5149–5161.
5. Zhou, W.; Yuan, X. Experimental evaluation of SiC MOSFETs in comparison to Si IGBTs in a soft-switching converter. *IEEE Trans. Ind. Appl.* **2020**, *56*, 5108–5118. [CrossRef]
6. Wang, R.; Tan, L.; Li, C.; Huang, T.; Li, H.; Huang, X. Analysis, design, and implementation of junction temperature fluctuation tracking suppression strategy for SiC MOSFETs in wireless high-power transfer. *IEEE Trans. Power Electron.* **2021**, *36*, 1193–1204. [CrossRef]
7. Qin, H.; Zhu, Z.; Dai, W.; Xu, K.; Fu, D.; Wang, D. Influence of parasitic inductance on switching characteristics of SiC MOSFET. *J. Nanjing Univ. Aeronaut. Astronaut.* **2017**, *49*, 531–539.
8. Lin, X.; Ravi, L.; Zhang, Y.; Burgos, R.; Dong, D. Analysis of voltage sharing of series-connected SiC MOSFETs and body-diodes. *IEEE Trans. Power Electron.* **2021**, *36*, 7612–7624. [CrossRef]
9. Yang, F.; Wang, Z.; Zhang, Z.; Campbell, S.L.; Wang, F. Analysis and experimental evaluation of middle-point inductance's effect on switching transients for multiple-chip power module package. *IEEE Trans. Power Electron.* **2019**, *34*, 6613–6627. [CrossRef]
10. Sugihara, Y.; Nanamori, K.; Yamamoto, M.; Kanazawa, Y. Parasitic inductance design considerations to suppress gate voltage oscillation of fast switching power semiconductor devices. In Proceedings of the 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), Niigata, Japan, 20–24 May 2018; pp. 2789–2795.
11. Cittanti, D.; Iannuzzo, F.; Hoene, E.; Klein, K. Role of parasitic capacitances in power MOSFET turn-on switching speed limits: A SiC case study. In Proceedings of the 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 1–5 October 2017; pp. 1387–1394.
12. Zeng, Z.; Li, X. Comparative study on multiple degrees of freedom of gate drivers for transient behavior regulation of SiC MOSFET. *IEEE Trans. Power Electron.* **2018**, *33*, 8754–8763. [CrossRef]
13. Li, P.; Guo, X.; Zhou, H.; Zhao, Q.; Jia, L. A drive circuit design based on SiC MOSFET and analysis of problems. In Proceedings of the 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), Harbin, China, 11–14 August 2019; pp. 1–5.
14. Peng, H.; Peng, H.; Dang, Z.; Kang, Y.; Wang, Z.; He, M.; Liu, X. A driving loss and speed co-optimized series resonant gate driver with novel time segmented methodology for high frequency SiC MOSFETs. In Proceedings of the 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), Orleans, LA, USA, 15–19 March 2020; pp. 1599–1603.
15. Wu, Y.; He, N.; Yu, L.; Xu, D.; Igarashi, S.; Fujihira, T. Effectiveness analysis of SiC MOSFET switching oscillation damping. In Proceedings of the 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), Nanjing, China, 29 November–2 December 2020; pp. 20–27.
16. Qin, H.; Xie, S.; Bu, F.; Wang, S.; Chen, W.; Fu, D. Optimized Parameter Selection Method of Driving Circuit for SiC MOSFET. In Proceedings of the 2021 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Wuhan, China, 25–27 August 2021; pp. 290–295.
17. Liu, T.; Ning, R.; Thomas, T.Y.W.; Shen, Z.J. Modeling and Analysis of SiC MOSFET Switching Oscillations. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 747–756. [CrossRef]
18. Hu, S.; Wang, M.; Liang, Z.; He, X. A frequency-based stray parameter extraction method based on oscillation in SiC MOSFET dynamics. *IEEE Trans. Power Electron.* **2021**, *36*, 6153–6157. [CrossRef]
19. Zhang, W.; Wang, X.; Dahidah, M.S.A.; Thompson, G.N.; Pickert, V.; Elgendy, M.A. An investigation of gate voltage oscillation and its suppression for SiC MOSFET. *IEEE Access* **2020**, *8*, 127781–127788. [CrossRef]
20. Roy, S.K.; Basu, K. Analytical model to study hard turn-off switching dynamics of SiC MOSFET and schottky diode pair. *IEEE Trans. Power Electron.* **2021**, *36*, 861–875. [CrossRef]
21. Zheng, D.; Zhang, S.; Li, L.; Cao, H.; Fan, T.; Ning, P.; Zhang, J.; Wen, X. Research on switching losses testing method for SiC MOSFETs. *Proc. CSEE* **2020**, *40*, 2975–2983.
22. Fariborz, M.; Deepak, S.G.; Wilson, E.; William, G.D. A Simplified Power Loss Calculation Method for PFC Boost Topologies. In Proceedings of the 2013 IEEE Transportation Electrification Conference and Expo (ITEC), Detroit, MI, USA, 16–19 June 2013; pp. 1–5.