4-26-2023 1:30 PM

A Novel Two-Stage AC-DC Power Converter with Partial Power Processing

Mina Fakhri,

Supervisor: Dr. Gerry Moschopoulos, *The University of Western Ontario*
A thesis submitted in partial fulfillment of the requirements for the Master of Science degree in Electrical and Computer Engineering

Abstract

A two-stage power converter with an AC-DC boost converter and a soft-switched DC-DC full-bridge converter is proposed in this thesis. The first stage has two interleaved modules that perform power factor correction; the second stage converts the output of the first stage to the desired output. An auxiliary circuit with a switch, a small transformer, and passive components is used to turn off the AC-DC converter switches with soft-switching; the auxiliary switch can also be turned on and off softly. The secondary of the auxiliary transformer is connected to the output of the overall converter so that some power can be transferred from the front-end converter to the output. This power is processed only once, thus reducing conversion losses. The thesis explains the operation of the converter and presents steady-state analysis and a design procedure. Results obtained from an experimental prototype are presented to confirm the converter's feasibility.

Keywords

Two stage AC-DC converter, Interleaved boost converter, soft switching, PWM – ZVS full bridge converter, power processing

Summary for Lay Audience

AC-DC power converters are used in many commercial and industrial applications to convert AC voltage into DC voltage to feed loads. This power conversion is typically done with two converter stages, an AC-DC stage followed by a DC-DC stage. The AC-DC stage shapes the input current so that it is sinusoidal and in phase with the input voltage to maximize power factor. The DC-DC stage takes the output of the AC-DC converter and converts to the required output voltage.

Power fed from the input to the load is processed by two converter stages with this type of converter. Each stage generates power losses when converting power, which decreases converter efficiency. This thesis proposes a novel two-stage converter that processes some of the power fed to the load using only one converter stage. This direct power transfer reduces losses that would have been generated by the second-stage converter. In this thesis, the operation of the proposed converter is explained, its steady-state operation is analyzed, and a procedure for the design of key components and parameters is developed and demonstrated with an example. The feasibility of the converter is confirmed with results obtained from an experimental prototype.

Acknowledgments

I am honored to express my sincere appreciation to my advisor, Dr. Gerry Moschopoulos, for his invaluable patience, expertise, and guidance throughout my Master's research. His unwavering support has been instrumental in shaping this work, and I am proud to have had the opportunity to learn from him.

Furthermore, I would like to express my deep gratitude to Dr. Adel Abosnina, my fellow researcher at the Power Engineering Lab, for his invaluable guidance and support. His expertise in power electronics has been crucial to my academic pursuits, and I am grateful for the opportunity to have worked alongside him. I would like to thank Asad Hameed for his help with some of the experimental work as well.

Last but not least, my deepest gratitude goes to my lovely husband, Saeed, for his endless love and support. I would also like to express my profound appreciation to my parents, who have been the driving force behind my success. Their unwavering support and encouragement have been the greatest gift anyone could ask for, and I am forever indebted to them for allowing me to pursue my dreams and achieve my full potential.

.

Table of Contents

List of Tables

List of Figures

Acronyms

AC	Alternative Current
DC	Direct Current
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
BJT	Bipolar Junction Transistor
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
CCM	Continuous Current Mode
DCM	Discontinuous Current Mode
PFC	Power Factor Correction
RMS	Root Mean Square
PWM	Pulse Width Modulation
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
DPT	Direct Power Transfer
HF	High Frequency

Abbreviations

C_f	Output Capacitor
C_r	Resonant Capacitor
C_{dc_link}	Dc Link Capacitor
C_1	Intrinsic Capacitor of the Switch Q1
C_2	Intrinsic Capacitor of the Switch Q2
C_3	Intrinsic Capacitor of the Switch Q3
C_4	Intrinsic Capacitor of the Switch Q4
C_{lag}	Parallel-connected capacitor for lagging leg
C_{lead}	Parallel-connected capacitor for leading leg
D_{T1}	Rectifier diode 1 of the HF transformer
D_{T2}	Rectifier diode 2 of the HF transformer
D_{R1}	Antiparallel Diode of the Switch Q1
D_{R2}	Antiparallel Diode of the Switch Q2
D_{R3}	Antiparallel Diode of the Switch Q3
D_{R4}	Antiparallel Diode of the Switch Q4
D_{x1}	Auxiliary Transformer Diode 1
D_{x2}	Auxiliary Transformer Diode 2
D_{a3}	Auxiliary Diode 3
D_{a1}	Auxiliary Diode 1

D_{a2}	Auxiliary Diode 2
D_1	Main Diode 1
D_2	Main Diode 2
L_1	Main Inductor 1
L_2	Main Inductor 2
L_{r1}	Resonant Inductor 1
L_{r2}	Resonant Inductor 2
L_r	Resonant Inductor in the Full Bridge Converter
L_f	Output Inductor
L_{fp}	Output Filter Inductance Referred to the Primary
T_r	High Frequency Transformer
T_x	Auxiliary Transformer
S_1	IGBT Main Switch 1
S_2	IGBT Main Switch 2
S_a	IGBT Auxiliary Switch
Q_1	MOSFET Switch 1
Q_2	MOSFET Switch 2
Q_3	MOSFET Switch 3
Q_4	MOSFET Switch 4
V_{in}	Input Voltage

V_o	Output Voltage
V_{rec}	Rectified Voltage
V_{pri}	Primary Voltage of the HF Transformer
V_{bus}	Bus Voltage
V_{bus_min}	Minimum Bus Voltage
V_f	Diode Rectifier Forward Voltage
V_{in}	Input Voltage
N	High Frequency Transformer Turns Ratio
N_x	Auxiliary Transformer Turns Ratio
N_{pri}	Primary Turns Ratio of the Transformer
N_{sec}	Secondary Turns Ratio of the Transformer
i_p	Primary Current of the HF Transformer
$I_{critical}$	Critical Current
I_{in}	Input Current
I_{s1}	Current through the Main Switch S1
I_{s2}	Current through the Main Switch S2
I_{sa}	Current through the Auxiliary Switch Sa
I_o	Output Current
D	Duty Cycle of the Main Switches
P_o	Output Power

D_{eff}	Effective Secondary Duty Cycle
R	Output Resistive Load
R’	Output Resistive Load Reflected to the Primary
T_h	Hold-up Time

Chapter 1

1 Introduction

1.1 Introduction to power electronics

Power electronics involves the study of electronic circuits that convert power from an input source to meet the requirements of an output load, using power semiconductor devices along with passive elements such as capacitors, inductors, transformers. A feedback controller is used to compare the power output unit with a reference value, and the controller minimizes the error between the two, as shown in the block diagram in Fig. 1.1 [1]. The focus of this thesis is on a two-stage AC-DC converter topology. This proposed converter is comprised of two main converters, the first stage is an AC-DC interleaved boost converter, and the second stage is a DC-DC full bridge converter.

In this chapter, basic power electronic concepts which describe the technical background of this thesis will be discussed, and a literature review of previous works is performed, then the objectives of the thesis are explained.

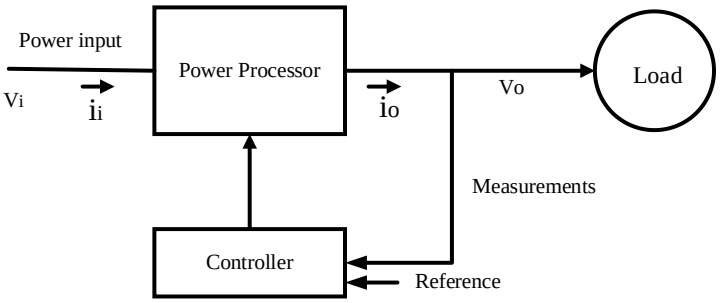


Fig. 1.1. Block diagram of a power electronic system

1.2 Power electronic devices

There are several types of power semiconductor devices that can be used in power converters. In this section, three types are briefly reviewed: diodes, metal-oxide-silicon field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs).

1.2.1 Diodes

The behavior of the semiconductor diode in a circuit is given by its linear and non-linear current-voltage characteristics as shown in Fig. 1.2(a), and Fig 1.2(b), respectively. As it can be seen from the ideal characteristic in Fig. 1.2(a), an ideal diode conducts only positive current, and no negative current can flow through it.

A non-ideal diode has a non-linear characteristic that can be divided into three regions: the forward-biased region, the reverse-biased region, and the breakdown region. Current flows through the device between anode and cathode when it is forward-biased, when the voltage between its anode and cathode tries to exceed its forward voltage drop, which is typically about 0.7 V.

When a positive current flows through a non-ideal diode, there is a voltage drop of about 0.7 V between anode and cathode. The amount of forward voltage drops changes slightly the current through the device is increased. When voltage is applied between the diode's cathode and anode, no current flows through the device except for a very small amount of leakage current. The device enters the breakdown region if the voltage placed across the cathode and the anode exceeds the voltage rating of the device [2].

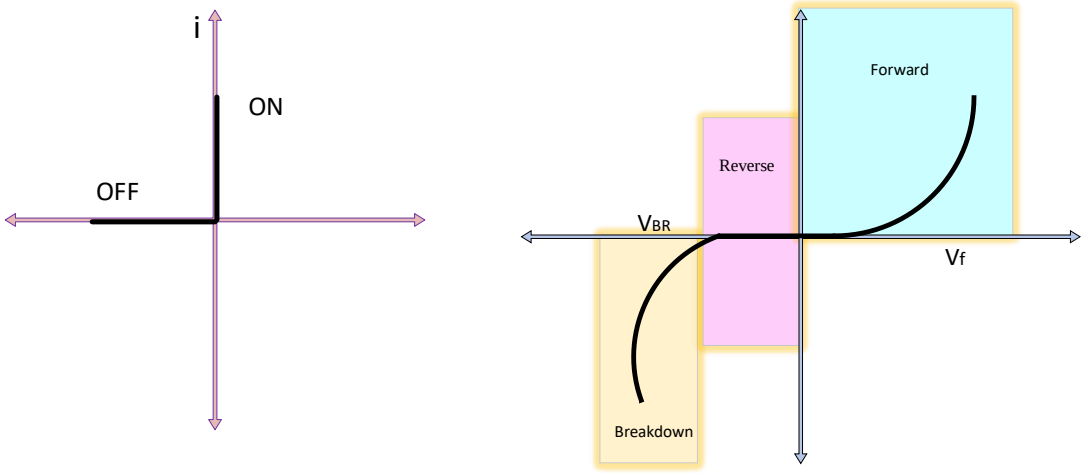


Fig. 1.2. Diode characteristics: (a) idealized i-v characteristic: (b) actual i-v characteristic

It is possible for current to flow in the reverse direction, from cathode to anode, in a non-ideal diode, as can be seen in Fig. 1.3. This can happen when the diode is in the process of turning off. In a non-ideal diode, the current flowing through it falls to zero, then becomes negative, temporarily, as it is trying to turn off. Eventually, the device does turn off and the current becomes zero. This negative current is defined as reverse recovery current and has a duration of t_{rr} [2]. This current increases switching losses and it increases peak current stresses in other converter components as well.

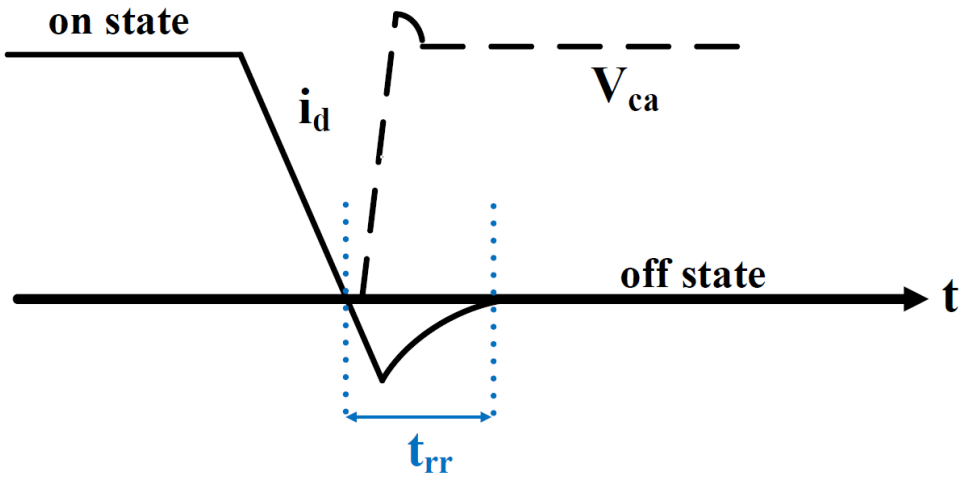


Fig. 1.3. Reverse recovery current of a diode [1]

1.2.2 The metal-oxide-silicon field-effect transistor (MOSFET)

The MOSFET is a voltage-controllable device with fast switching response and minimal drive requirements due to its insulated gate. It has four terminals: gate (G), body (B), source (S), and drain (D), with the body connected to the source to reduce the number of terminals to three. Its operation can be controlled by the voltage between its gate and source. There are four types of MOSFETs as shown in Fig. 1.4. MOSFETs can be enhancement type with positive gate-source voltages or depletion type with negative gate-source voltages, n-type or p-type, as with bipolar junction transistors (BJTs). Fig. 1.5 shows a circuit symbol of a n-type enhancement MOSFET, which is by far the most commonly used MOSFET used in power electronics [3].

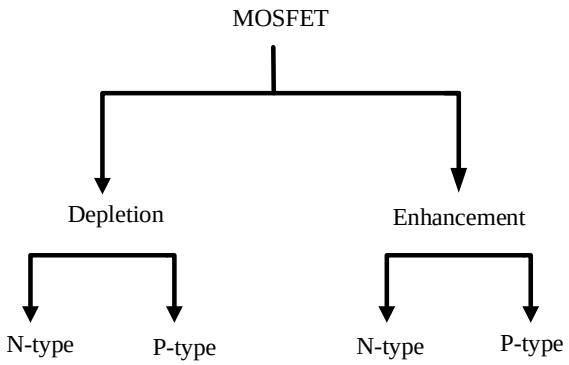


Fig. 1.4. Classification of MOSFET

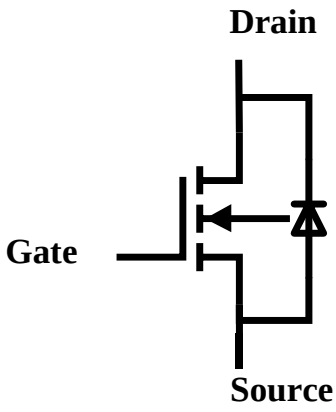


Fig. 1.5. Circuit symbol of an N-Channel power MOSFET

MOSFETs have three regions of operation: the cut-off region, the linear/triode region, and the saturation region. When operating in the cut-off region, a MOSFET is like an open circuit with no current flowing through it, it is off. When operating in the linear/triode region, a MOSFET acts like a voltage-controlled resistor and current flows through it, from drain to source. When operating in the saturation region, a MOSFETs acts like a closed switch with a small drain-source resistance between its drain and its source. When a MOSFET is operating in the saturation region, its equivalent circuit can be considered to be a small drain-source resistance. When it is off, its equivalent circuit can be considered to be a small, drain-source capacitance. MOSFETs are always operated in the saturation region when used in power converters. It should be noted that real-life MOSFETs have an

anti-parallel diode connected between their source and drain. This diode is very useful in many power electronics applications.

1.2.3 Insulated-gate bipolar transistor (IGBT)

Fig. 1.6 shows a circuit symbol of an IGBT. The device has three terminals: collector (C), emitter (E), and gate (G). An IGBT is essentially a combination of a MOSFET and a BJT as it has the gate of a MOSFET, but the body of a BJT. An IGBT requires minimal gate current as its gate is insulated, like a MOSFET, and it has a fixed voltage drop, called the saturation voltage, between its collector and emitter, like a BJT. IGBTs do not have the switching speeds of MOSFETs but have a lower collector-emitter drop when higher currents flow through them. In general, MOSFETs are used in lower power converters and IGBTs are used in higher power converters.

The following should be noted about IGBTs:

- They have a current-tail when they are turned off. In other words, the current in an IGBT does not fall to zero quickly when it is turned off but falls gradually. This current tail limits the speed of IGBTs and creates switching losses as well, as will be explained later in this chapter.
- IGBTs typically have anti-parallel body diodes like MOSFETs. For some applications, however, this body-diode needs to be blocked, thus IGBTs with series diodes that block the anti-parallel diode are commercially available for high power applications.

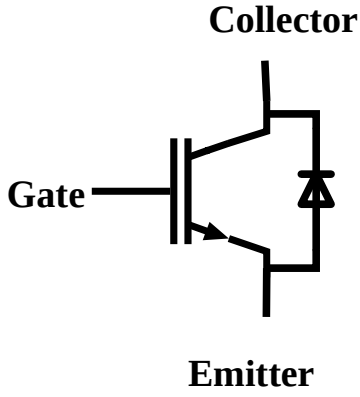


Fig. 1.6. Circuit symbol of an IGBT with an anti-parallel diode

1.3 Switching losses

Non-ideal power semiconductor devices such as MOSFETs and IGBTs have conduction losses and switching losses. As discussed above, MOSFETs have an equivalent drain-source resistance when they are on and IGBTs have a fixed voltage drop when they are on. Conduction losses are generated when these devices conduct current. Switching losses are generated when these devices are turned on and off as there is overlap between voltage and current during switching transitions, as shown in Fig. 1.7. Given that power is related to the product of voltage and current, this overlap of voltage and current creates power losses in MOSFETs and IGBTs.

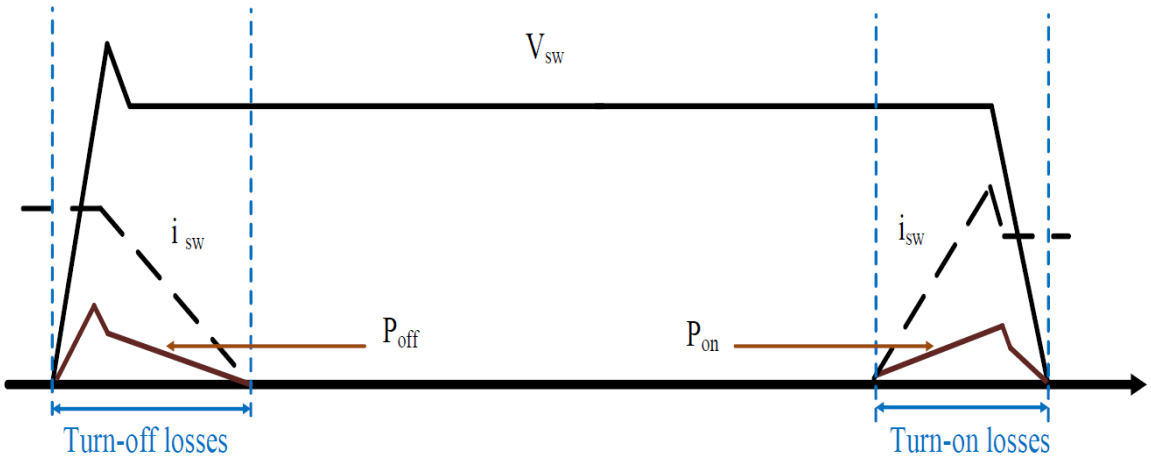


Fig. 1.7. Typical switch voltage and current waveforms

1.4 Soft switching

Power converters operating with high switching frequencies will have considerable switching losses unless something is done to reduce their switching losses. Switching losses can be reduced if either the voltage or current of a switching device is made zero at the time that a switching transition takes place. This can be done with either zero-voltage switching (ZVS) where the voltage across the switching device is zero during switching transitions [4] – [7] or zero-current switching (ZCS) methods when it is the current that is zero [8] – [11]. Both methods are classified as being soft-switching methods as the switching transition is gradual and considered to be “soft”, as opposed to conventional hard-switching where no such methods are used, and the switching transitions are sudden.

Due to the nature of the devices, ZVS is preferred for MOSFETs and ZCS is preferred for IGBTs. MOSFETs have larger drain-source capacitances than IGBTs, which makes ZVS preferable for MOSFETs while IGBTs have a current-tail when they turn off, which makes ZCS preferable.

A typical implementation of ZVS for MOSFETs is shown in Fig. 1.8. A ZVS turn-on is achieved by injecting current through the body-diode of the device before it is turned on. This clamps the voltage across the device to zero (one forward voltage drops, typically about 0.7 V) so that when the device is turned on, it is done with zero voltage across it. A ZVS turn-off is achieved by having a capacitor connected across the device, as shown in Fig. 1.8 This capacitor slows down the rate of voltage rise across the device when it is turned off so that the overlap between voltage and current is reduced during this switching transition. This reduction of overlap between the voltage and current results in lower power dissipation and thus fewer losses. The amount of capacitance that is used depends on the application. In some applications, the internal capacitance of the device is sufficient, while in other applications, additional capacitance must be added externally across the device.

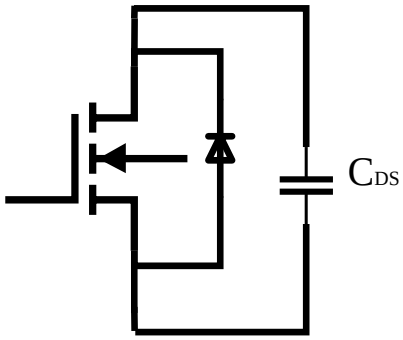


Fig. 1.8. ZVS implementation for MOSFETs

A typical application of ZCS for IGBTs is shown in Fig. 1.9. A ZCS turn-on is achieved by placing an inductor in series with the switching device. This inductor slows down the rate of rise of current in the device when it is turned on, this reducing the overlap between voltage and current during turn-on switching transitions. A ZCS turn-off is achieved by the gradual removal of current from the device before it is turned off. This can be done by the natural operation of the rest of the power converter, by providing an alternative path for

current to flow through, a path with lower voltage potential, or by reversing the polarity of voltage across the switch-inductor combination. ZCS operation helps eliminate the turn-off current tail in IGBTs during turn-off switching transitions, which reduces the losses that the current tail would cause otherwise [12].

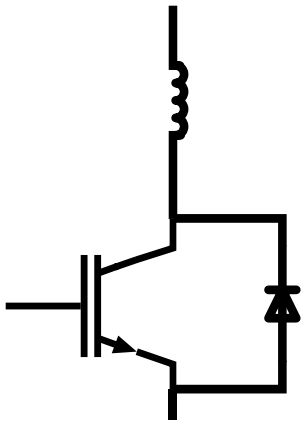


Fig. 1.9. ZCS implementation for IGBTs

1.5 AC-DC converters

AC-DC converters convert an AC input voltage into a DC voltage. The input may be obtained from the utility grid or an AC generator. The term “AC-DC converter” can refer to a single AC-DC converter module [13] or to a two-stage converter [14] that has an AC-DC front-end converter followed by a second converter, a DC-DC converter that converts the output of the front-end converter into a DC output voltage, as shown in Fig. 1.10. A two-stage approach is used when the output voltage must be low (e.g., 5-48 V) or isolation is needed between the input and output voltages [15].

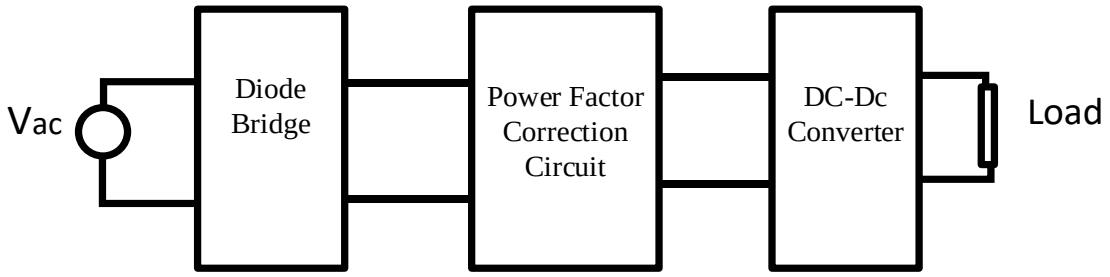


Fig. 1.10. Block diagram of a standard two-stage AC-DC converter

The most popular AC-DC option is some sort of boost converter that performs power factor correction (PFC) to meet the regulatory agency requirements on harmonic content [16]-[18], such as the one shown in Fig. 1.11. PFC is performed by shaping the input current that is drawn from the input AC source so that it is sinusoidal and in phase with the input voltage. The power factor of unity represents the most efficient use of power from the source.

The basic operation of a boost converter can be described as follows: When the switch is turned on, energy is placed in the input inductor and the current flowing through the inductor rises. When the switch is turned off, the energy that was stored in the inductor is transferred to the output and its current falls. The output of the converter depends on the width of the gating signal pulse or the width of the on-time of the switch so that boost converters are operated with pulse-width modulation (PWM) control.

Boost converters can operate in either continuous current mode (CCM) [19] or discontinuous current mode (DCM) [20]. When a boost converter is operated in CCM, a controller varies the converter's duty cycle (D), defined as the ratio of switch on-time T_{on} to switching cycle period T_S as follows:

$$D = \frac{T_{on}}{T_S} \tag{1-2}$$

The input current can be shaped to be a sine wave with some ripple current and is never zero except when its polarity changes from positive to negative. When a boost converter is operated with DCM, the converter's duty cycle is fixed throughout the input line cycle. The current starts from zero when the switch is turned on then falls back to zero after the

switch is turned off, some time before the start of the next switching cycle. The input current is a series of triangular pulses whose peak follows a sine wave. This current can be filtered to produce a sinusoidal input current with a converter power factor of unity.

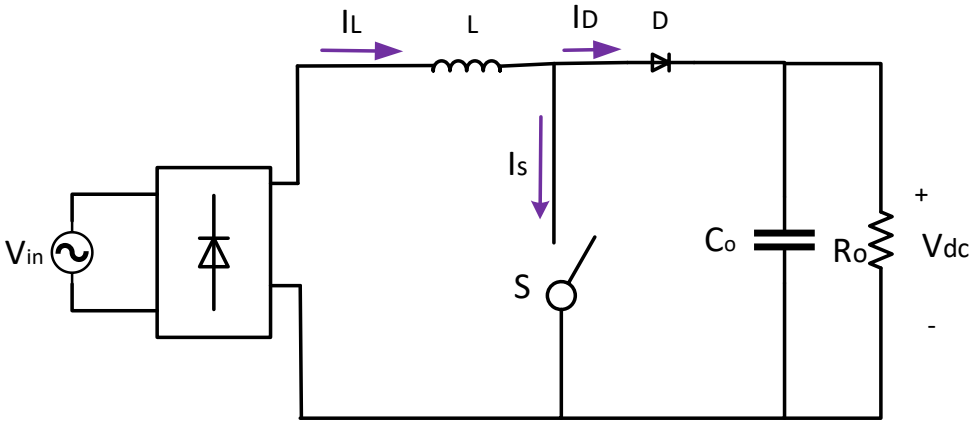


Fig. 1.11. AC-DC boost converter

1.6 Interleaved AC-DC boost converters

The input inductor of an AC-DC boost converter filters the high-frequency AC ripple current to make the input current as purely sinusoidal as possible. If the input inductor is large, then the input current ripple can be reduced, but such an inductor adds size and weight to the converter. If the input inductor is small, as is the case when the boost converter is operating in DCM, then the ripple current is large and power factor is reduced.

A common way to reduce input current AC ripple is to implement the boost converter with interleaving, as shown in Fig. 1.12. Interleaving in AC-DC boost involves the use of two or more individual boost converter modules connected in parallel. The switch in each boost converter module has the same duty cycle as those of the other switches, but its gating signal is phase-shifted relative to those of the other switches [21]-[24]. In the case of the interleaved converter shown in Fig. 1.12, the two switches have the same gating signals, but they are 180 degrees out of phase. Typical waveforms are shown in Fig 1.13 for the case when the switches are operating with $D > 0.5$ and $D < 0.5$.

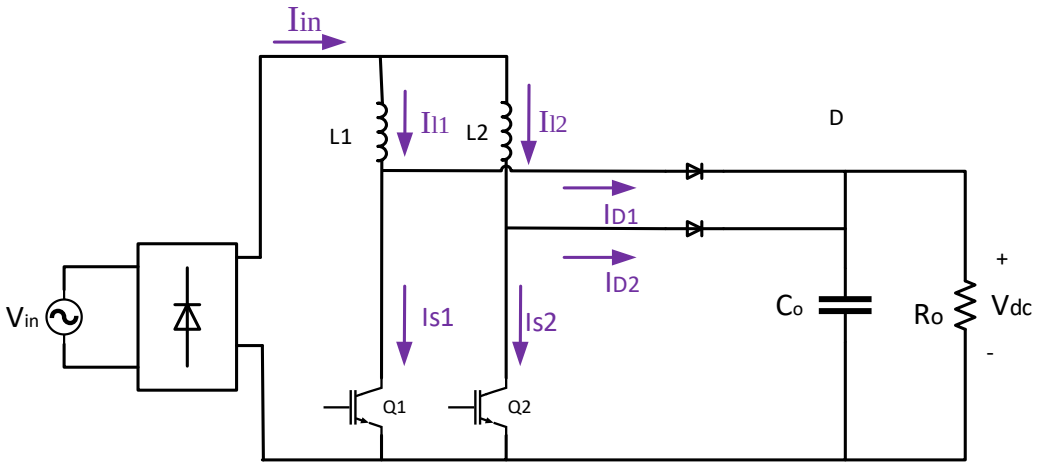
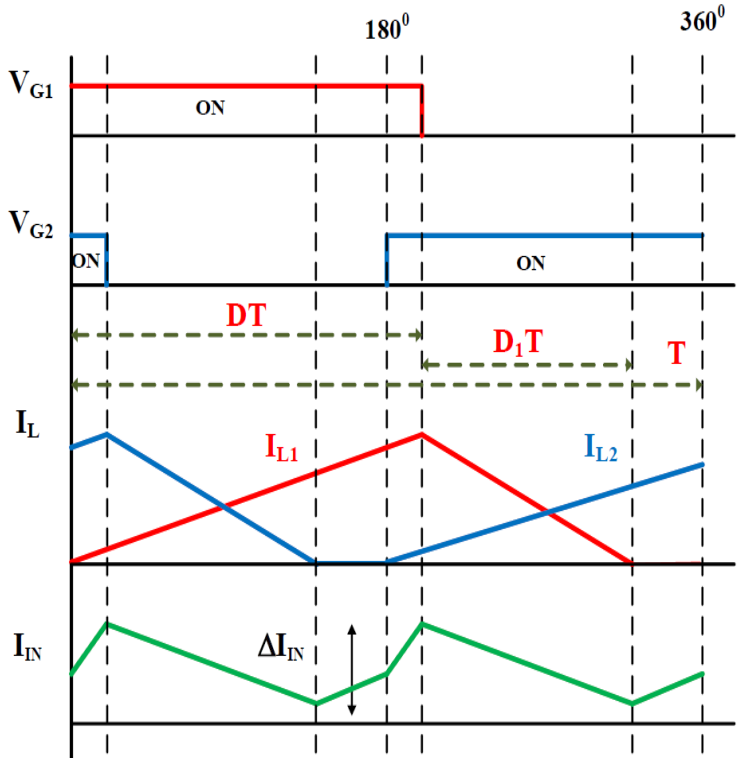


Fig. 1.12. Topology of a basic AC-DC interleaved boost converter

Although interleaved boost converters are implemented with multiple sets of boost converter switches and diodes, which makes them more expensive than a single boost converter module, they have several advantages [25]:

- They produce less input ripple.
- The net size and weight of their input inductance is lower than the input inductor of a single boost converter module.
- Power is processed by multiple modules instead of one, which reduces the stress of the converter components. This allows the converter to operate at higher power levels or cheaper components with lower current ratings can be used to offset somewhat the cost of additional components.
- Since the converter modules operate in discontinuous current mode, their switches can be turned on with ZCS as the current flowing in a module is zero at the start of a switching cycle.



(a)

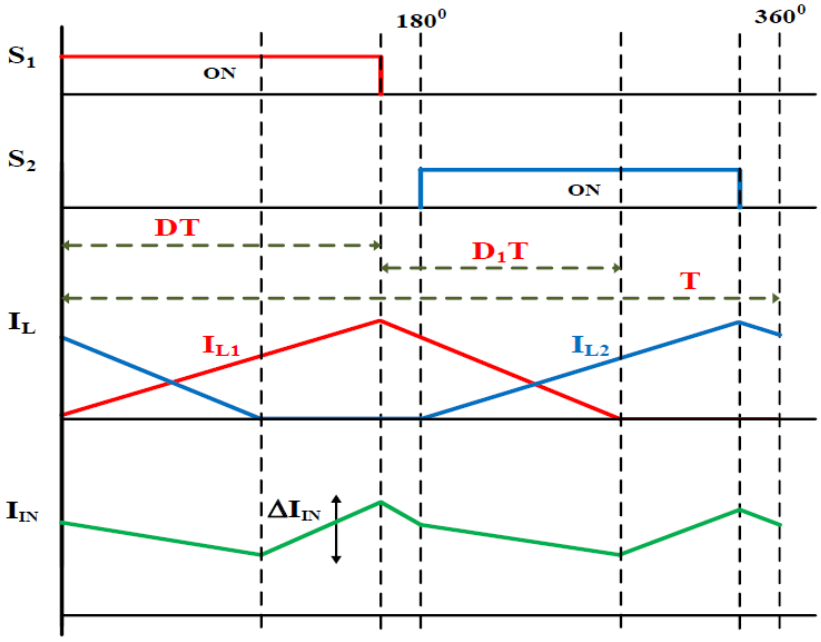


Fig. 1.13. Inductor current waveforms according to the switching pattern in DCM [26] (a) D > 0.5 (b) D < 0.5

1.7 DC-DC full bridge converter

The DC-DC converter in a two-stage AC-DC converter is typically a flyback or forward converter for low power applications or a full-bridge converter for higher power applications (> 500 W). Since a DC-DC full-bridge converter will be used in the converter proposed in this thesis, its basic structure and operation are discussed in this section. Its topology is shown in Fig. 1.14.

A full bridge DC-DC converter [27]-[32] consists of four switches $S_{1\text{-}4}$ that can be either MOSFETs or IGBTs. These switches are turned on using an appropriate sequence so that an AC square voltage is generated across the primary of the transformer. A high-frequency (HF) transformer is used to step down the primary to the required voltage of the output; it also provides isolation between input and output. The AC square voltage from the transformer is processed by a diode bridge rectifier, which rectifies it, and the result is fed to an output low pass filter to mitigate AC harmonics so that a DC output voltage is produced. Details of how a full-bridge converter is operated are explained in later chapters of this thesis.

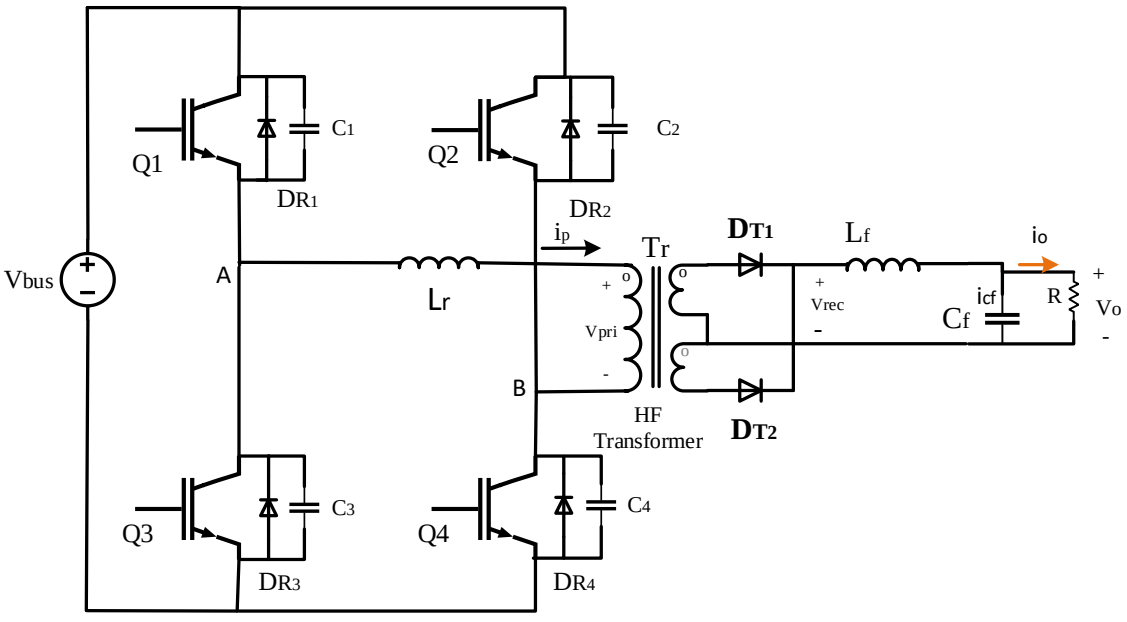


Fig. 1.14. DC-DC full bridge converter

1.8 Partial power processing

One issue that two-stage AC-DC converters have is that any input power that is transferred to the output must be processed twice, once by each converter. Since neither the AC-DC front-end converter nor the DC-DC back-end converter are ideal, this means that either converter produces losses as it performs power converter. Overall converter efficiency can be improved if, somehow, some of the input power can be processed by only one converter then fed directly to the load, thus bypassing the second converter. This type of operation is referred to as partial power processing in literature.

Partial power processing methods have been developed for various types of converters. The general principles of partial power processing can be seen in the block diagram shown in Fig. 1.15. The basic idea is that instead of a converter processing the full power that is fed to it, the converter processes a portion of this power with the remaining power fed directly to the output [33]. Partial power processing methods have been shown to be effective in increasing overall converter efficiency, but they are not often used because of limits in converter topology structures. Only some topologies can be implemented with partial power processing [34]-[38].

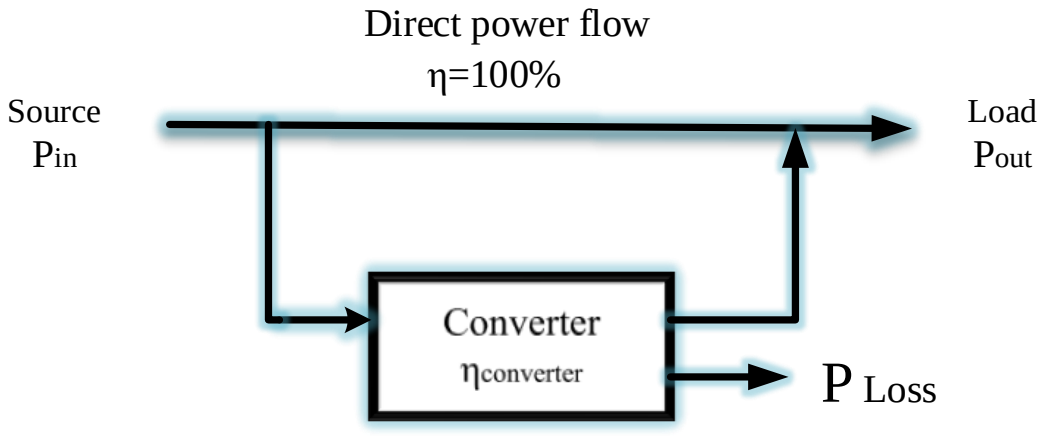


Fig. 1.15. Concept of power flow in a partial power converter

1.9 Literature review

The converter that is proposed in this thesis is a two-stage AC-DC converter. Since the second-stage converter is a conventional DC-DC full-bridge converter, the focus of the literature review presented in this section is on the AC-DC front-end converter. The front-end converter can be implemented with MOSFETs and ZVS or with IGBTs and ZCS. Given that the current flowing in the converter is not insignificant and that an interleaved approach with DCM operation that ensures that the converter switches are turned on with ZCS will be used, interleaved ZCS-PWM boost converters are emphasized in this literature review.

Several ZCS-PWM interleaved boost converters are shown in Fig. 1.16-1.20 [39] - [42], [26]. These converters have at least one of the following drawbacks:

- They use an auxiliary circuit to help the main switch of an AC-DC boost converter module operate with ZCS. This means that an interleaved boost converter made up of two converter modules needs two auxiliary circuits with two auxiliary switches, which increases the cost of the converter.
- The auxiliary circuit is a resonant circuit. Whenever it is activated, time is needed for the circuit to go through a resonant cycle before it is deactivated. The greater the amount of time that the circuit needs to be active, the greater its RMS current stress becomes, thus increasing the stresses and the losses of the converter.
- The auxiliary circuit components are in the main power path of the circuit instead of being in an auxiliary circuit that is parallel to the main power circuit. This increases auxiliary circuit component stresses and losses.
- There is no path for energy in the auxiliary circuit to be transferred to the output. As a result, this energy is trapped in the auxiliary circuit and dissipated, which creates power losses and limits the amount of power that the converter can process.
- The auxiliary circuit injects current into the main power switches. This is the case when the auxiliary circuit is some sort of resonant circuit. This additional current increases the peak current stress of the main switches so that they must be implemented with higher current-rated, more expensive components.

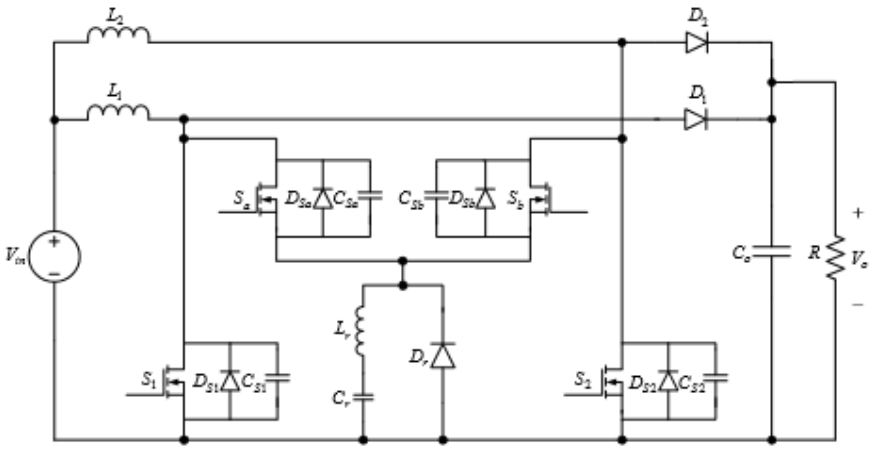


Fig. 1.16. Two-phase interleaved boost converter with soft switching [39]

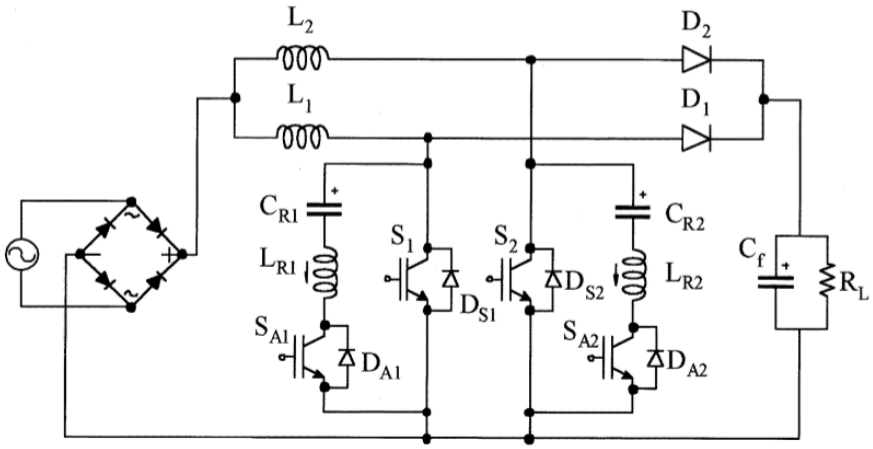


Fig. 1.17. Breadboarded interleaved ZCT boost converter [40]

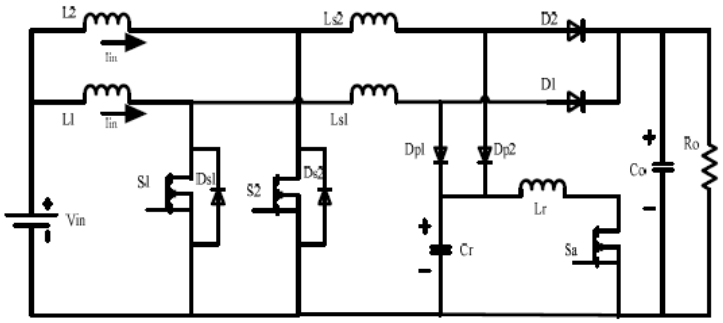


Fig. 1.18. Interleaved ZCS boost converter [41]

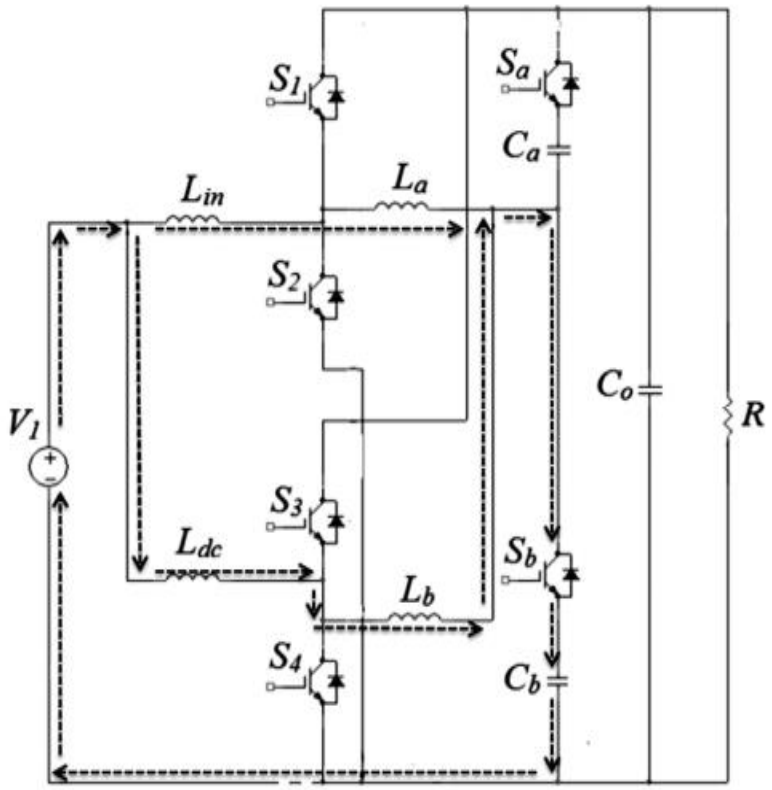


Fig. 1.19 ZCS interleaved bidirectional DC-DC Converter [42]

An interleaved AC-DC ZCS-PWM boost converter that does not have these drawbacks was proposed in [26]; the converter is shown in Fig. 1.20. A key feature of this converter is that it has a transformer in its auxiliary circuit. The secondary of this transformer is connected to the output of the converter. The main idea of this thesis is to use this converter as the front-end converter and connect the secondary of the auxiliary circuit transformer to the output of the whole two-stage converter instead of the output of the AC-DC converter, which is connected to the intermediate DC link. This connection allows some of the input power to be processed only by one converter instead of two converters, thus, presumably, reduce the overall losses of the converter.

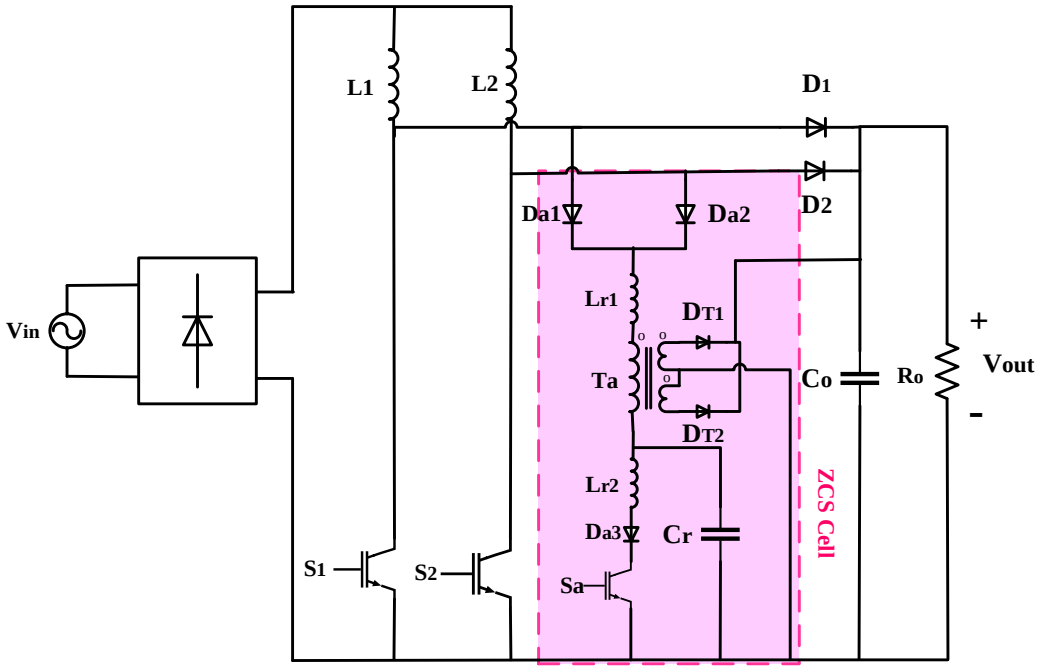


Fig. 1.20. Front-end interleaved AC-DC ZCS-PWM boost converter

1.10 Thesis objectives

The main objectives of this thesis are as follows:

- To propose a new two-stage AC-DC converter with the interleaved ZCS-PWM converter proposed in [26] as the first-stage converter and a conventional DC-DC full-bridge converter as the second-stage converter and investigate the effect to using the auxiliary circuit transformer for the first-stage converter to allow some of the input power to be processed by only one converter.
- To determine the steady-state characteristics of this converter by performing a mathematical analysis of the converter's modes of operation.
- To develop a procedure that can be used to design the converter. This procedure can be used to determine key converter component values and parameters that can be used in the implementation of a prototype of the converter.
- To confirm the feasibility of the converter and the effectiveness of its partial power processing ability with results obtained from an experimental prototype of the converter.

1.11 Thesis outline

The outline of this thesis is organized as follows:

In Chapter 2, a novel two-stage AC-DC power converter consisting of an interleaved AC-DC boost converter module that can perform power factor correction and a DC-DC full bridge converter that steps down the output voltage and provides isolation using a high frequency is proposed. The first-stage converter has an auxiliary circuit with a small-size transformer that allows all its switches to operate with ZCS and that can be used to improve the total efficiency. In this chapter, the operation of the proposed converter is explained, and its features will be described.

In Chapter 3, a steady-state analysis of the operation of the proposed converter is performed. Mathematical equations for each mode of steady-state operation are derived. These equations are the basis of the design procedure that is developed in the next chapter.

In Chapter 4, graphs of steady-state characteristic curves that can be used for design purposes are generated using MATLAB software, according to the steady-state equations derived in the previous chapter. Using these graphs and the steady-state equations, a procedure for the design of key converter components and parameters is developed and the procedure is demonstrated with an example. The results of the design example were used to implement an experiment prototype of the proposed converter.

In Chapter 5, experimental results that demonstrate the feasibility of the proposed converter are presented. The efficiency of the proposed two-stage converter is compared to that of a two-stage converter without direct power transfer.

In Chapter 6, the content of this thesis is summarized, and the conclusions and contributions of this thesis are presented, along with suggestions for future work.

Chapter 2

2 A novel two-stage AC-DC power converter with partial single-stage power processing

2.1 Introduction

The two-stage AC-DC converter proposed in this thesis is shown in Fig. 2.1. The proposed converter consists of an interleaved ZCS-PWM AC-DC boost converter with an auxiliary circuit in the first stage that operates with power factor correction and soft-switching and a ZVS-PWM full-bridge DC-DC converter that steps down the DC link voltage to the desired output voltage and provides isolation using a high-frequency transformer. Power is processed first by the AC-DC converter, then by the DC-DC converter. The soft-switching techniques used in the converters are different as their operating conditions are different. IGBTs are used in the first stage because of the high currents that flow through its converter switches, which can generate conduction losses. Since IGBTs are used, the soft-switching method that is used is ZCS, as explained in the previous chapter. MOSFETs are used in the second stage because the current that flows through their switches is relatively low. Since MOSFETs are used in this converter, the soft-switching method that is used for the full-bridge converter is ZVS, as explained in the previous chapter.

All input power that is transferred to the output in a two-stage AC-DC converter is generally processed by both converter stages. Given that each converter stage is non-ideal, each stage processes power with less than 100% efficiency. The basic premise of this thesis is that converter efficiency can be improved if some of the input power is transferred directly from the first converter to the output, thus being processed only once. In the proposed converter, some input power is transferred to the output through the auxiliary circuit of the first-stage converter.

In this chapter, the AC-DC first-stage converter and the DC-DC second-stage converter are described, and their general operating principles are explained. The modes of operation of the overall two-stage converter are then presented and the features of the converter are stated.

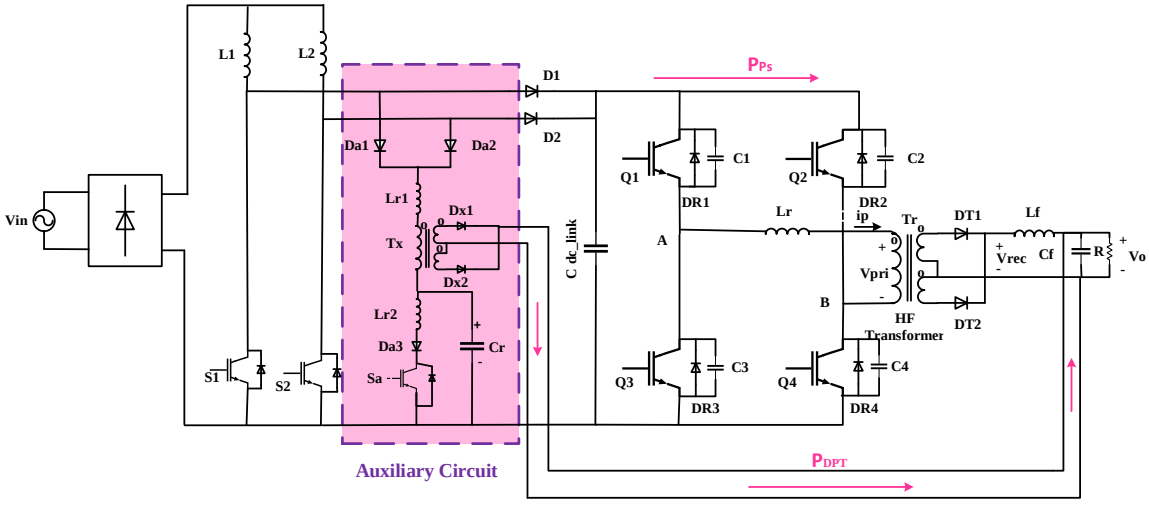


Fig. 2.1. Proposed two-stage AC-DC power converter with Direct Power Transfer (DPT)

2.2 AC-DC interleaved ZCS-PWM boost converter

The first-stage of the proposed AC-DC converter, shown in Fig. 2.1, consists of two boost converter modules: one with L_1, S_1 and D_1, the other with L_2, S_2 and D_2. The gating signals of the two main switches, S_1 and S_2 are identical, but shifted 180^o with respect to each other. The currents in L_1 and L_2 are discontinuous and identical, but also shifted 180 ^{o} with respect to each other.

The two boost modules are connected to the same auxiliary circuit, which consists of: connection diodes D_{a1} and D_{a2}, reverse blocking diode D_{a3}, inductors L_{r1} and L_{r2}, capacitor C_r, and center tap feed forward transformer T_x which has two diodes D_{x1} and D_{x2}. The auxiliary circuit is activated whenever a main switch is about to be turned off and its switch can be turned on and off with ZCS as well. The auxiliary circuit allows the converter to operate without an increase in the peak current or the voltage stresses of the main switches as it does not add current to the main switch and does not affect the peak voltage of these devices. The auxiliary switch in the converter is active for a much shorter time than in most other ZCS-PWM converters. This allows the converter to operate at higher power levels than other previously proposed interleaved ZCS-PWM converters with a single auxiliary switch as it is active for only a fraction of the switching cycle.

AC-DC converters that operate with input power factor correction (PFC) and consist of two or more interleaved boost converter modules are popular in industry. PFC is required in modern AC-DC converters as their input current must meet harmonic standards set by regulatory agencies. With interleaving, the input current of each module can be made to be discontinuous, and the size of their input inductors reduced. Interleaving can reduce the high ripple in each module and produce a net input current with a ripple that is comparable to that achieved by a single boost converter module with a large input inductor. Moreover, there is less current stress on the converter components because they each handle a fraction of the overall current and the control is easier as the more sophisticated control methods required for continuous current mode (CCM) operation are avoided. The AC-DC interleaved boost converter that is used in this thesis is shown in Fig. 2.2.

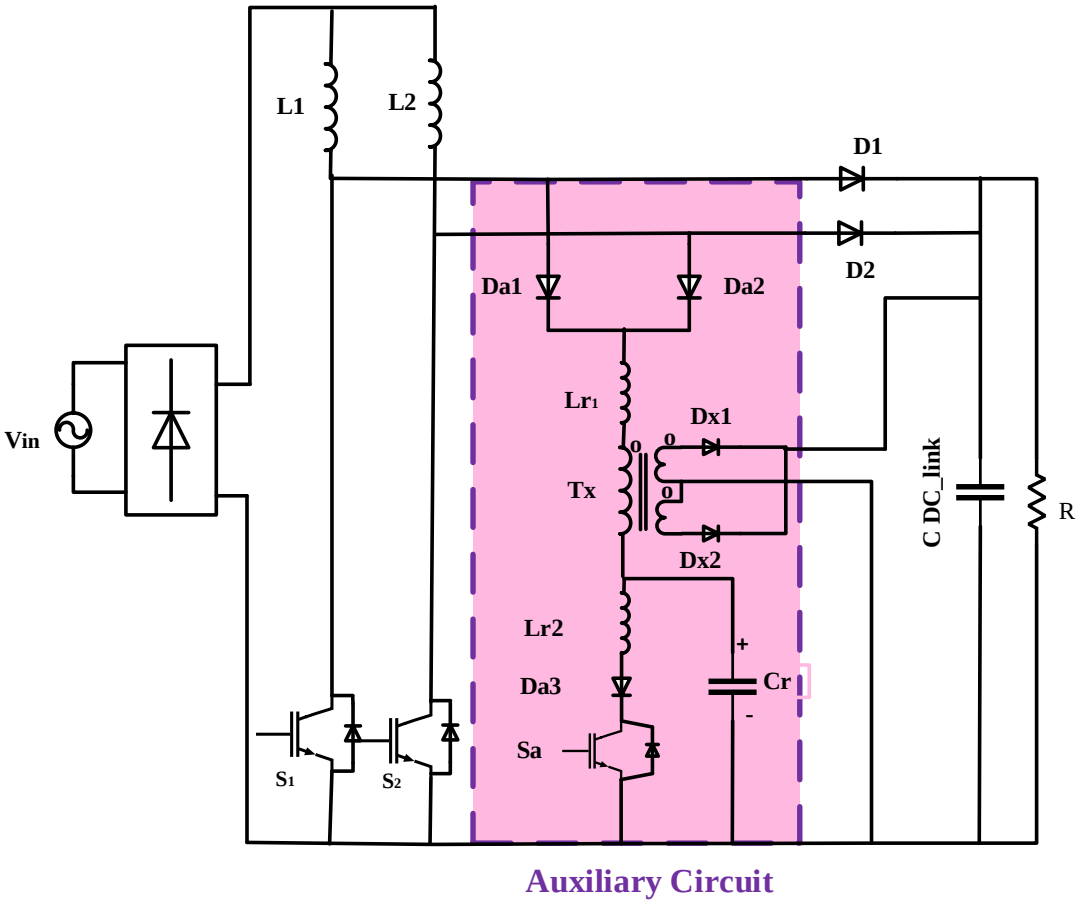


Fig. 2.2. Front-end interleaved AC-DC ZCS-PWM boost converter.

2.3 PWM full-bridge converter

The DC-DC full-bridge converter, shown in Fig. 2.3, is the converter that is most often used for applications when DC-DC power converter greater than 500 W is needed. This converter takes the voltage from the first AC-DC converter stage, typically about 400 V and converts to a lower DC voltage, typically 5-48 V DC [43]- [45]. The converter has four switches, Q_1, Q_2, Q_3 and Q_4 in two legs, with two switches each, a high frequency power transformer T, diode rectifier D_{T1}, D_{T2} and an output filter that consists of an inductor L_f and a capacitor C_f. The four switches transform a DC input voltage to a square wave voltage that is stepped down by the transformer, then rectified by the output diode rectifier at the secondary side.

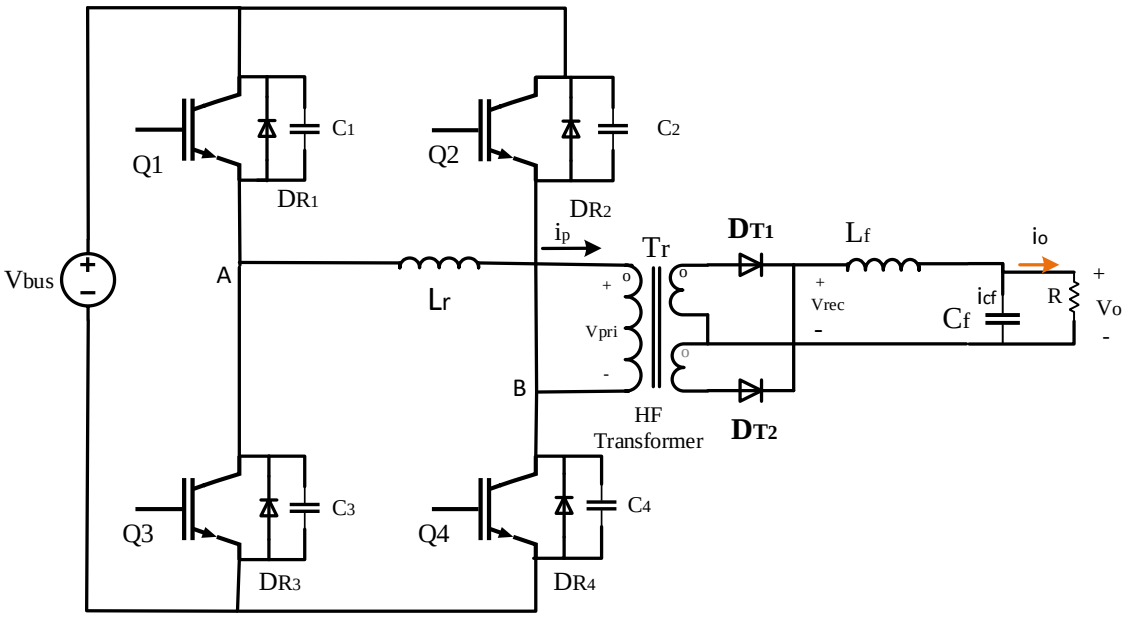


Fig. 2.3. DC-DC full bridge converter

There are generally two types of PWM methods by which the DC-DC converter can operate. In the first method, basic PWM as shown in Fig. 2.3, diagonally opposed switches Q_1 and Q_4 or Q_2 and Q_3 are turned on and off simultaneously. When diagonally opposed switches are on, the input DC voltage is impressed across the transformer primary with the voltage polarity depending on the switch pair that is on. The transformer primary voltage becomes zero when all the switches are off. The transformer voltage is rectified by the

secondary diodes, then filtered to produce the output DC voltage. This output voltage is dependent on the width of the square pulses of the transformer primary voltage waveform – as the output voltage increases as the square voltage pulses are made larger, or the zero voltage states are made smaller. Maximum output voltage can be achieved when the transformer primary voltage is a square wave with no zero voltage states. The output voltage is zero when the primary voltage is always zero.

At the secondary side, when switches Q_1 and Q_4 are conducting, the voltage across the transformer primary is stepped up or down (generally down) and secondary rectifier diodes D_{T1} conducts. The secondary rectified voltage V_{rec} is equal to V_{bus}/N, where N is the transformer primary-to-secondary-winding-turns ratio. This voltage, minus the output voltage, is applied across the output filter inductor L_f, causing the inductor current I_{Lf} to increase linearly. The primary current i_p is equal to the output filter inductor current reflected to the primary side, and correspondingly it increases linearly.

When switches Q_2 and Q_3 are conducting, the converter operates in the exact same manner as it does when switch Q_1 and Q_4 are on except that secondary diode D_{T2} conducts instead of D_{T1}. When all the power switches are off, the primary current i_p is zero and the output filter inductor current freewheels through the two rectifier diodes as the transformer secondary voltage is zero.

The second PWM method used to operate the DC-DC full-bridge converter is phase-shift PWM. With this method, the width of all the gating signals is fixed to be about 50% of the switching cycle. The gating signals of the switches in each converter leg, Q_1 and Q_3 or Q_2 and Q_4, are complementary to each other with both switches in a leg never being on at the same time. A small dead time when neither switch in a leg is on is implemented to give time for one switch in a leg to be fully off before its complementary switch is turned on, to avoid the possibility of a short-circuit.

The output voltage is adjusted by shifting the gating signals of one leg relative to those of the other. Voltage is impressed across the transformer whenever a pair of diagonally opposed switches is on. No voltage is impressed across the transformer and a zero-voltage state occurs whenever two top switches, Q_1 and Q_2 or two bottom switches, Q_3 and Q_4 are

on. The converter is said to be in a freewheeling mode of operation when two top switches or two bottom switches are on as current in the transformer circulates in the primary. The leg with the switches that put the converter in a freewheeling mode of operation when they are turned on is generally referred to as the leading leg, while the leg with the switches that put the converter out of a freewheeling mode of operation is referred to as the lagging leg. It should be noted that regardless of whether the full-bridge converter is operated with basic PWM or with phase-shift PWM, the operation of the converter at the secondary side is identical.

2.4 Modes of operation

The proposed converter has the following modes of operation for a half switching cycle when duty cycle is $D \geq 0.5$ and when S_2 is turned on and S_1 is turned off. Typical waveforms and circuit diagrams for these modes are shown in Fig. 2.4, Fig. 2.5 and Figs. 2.6 – 2.12 respectively. T_s in Fig. 2.5 is the period of the switching cycle.

The modes of operation for the other half-cycle when S_1 is turned on and S_2 is turned off are identical. The modes of operation are derived based on the following assumptions:

- Since the AC input voltage can be considered to be a DC input source in a very short amount of time, the steady-state analysis is done with DC input voltage.
- The proposed circuit has two boost modules that are designed to be operated in DCM, so the input inductor current of each one will become discontinuous. However, the input current of the converter, which is the sum of the inductor currents, should be continuous.
- The output filter capacitor (C_f) is large enough to be considered as a voltage source (V_o).
- All semiconductor switches are ideal with no switching or conduction losses.
- All inductors and capacitors are ideal; therefore, they have negligible resistances.
- All diodes are ideal and the reverse recovery time of each one of them is zero.

The converter's modes of operation are as follows:

Mode 1 ($T_0 < t < T_1$): This mode begins when switch S_2 is turned on. The rectified voltage is applied to L_2 and the current through L_2 linearly increases, as does the input current in the input inductor (I_{in}). The slope of the current is $\frac{v_{in}}{l_2}$. Since I_{in} is the summation of I_{L1} and I_{L2}, it will increase with greater slope. Meanwhile, switches Q_1 and Q_4 of the DC-DC full-bridge converter are on, and the DC link voltage is impressed across the primary. This voltage is stepped down by the transformer, then rectified through diode D_{T1} and fed to the output filter and the load.

Mode 2 ($T_1 < t < T_2$): This mode begins when the auxiliary switch (S_a) is turned on in preparation to turn off main switch S_1 with ZCS. S_a turns on with ZCS because L_{r2} limits the rise of the switch current. After S_a is turned on, C_r starts to resonate with L_{r2} so that the current in L_{r2} rises while the voltage across C_r decreases. Meanwhile, at the full-bridge converter, switch Q_1 begins turned off and the process of charging the switch capacitance of Q_1 and discharging that of Q_3 starts.

Mode 3 ($T_2 < t < T_3$): This mode begins when the voltage across C_r (V_{Cr}) is zero. During this mode, V_{Cr} is charged to a negative voltage and D_{a1} and D_{a2} start to conduct. D_{x1} starts to conduct so that the circulating energy from the auxiliary circuit is transferred to the output during this time. The current through L_{r1} and L_{r2} decreases and goes to zero. The currents through S_1 and S_2 then become negative and flow through their body diodes. When this happens, S_1 can be turned off with ZCS. During this mode, the current in L_{r2} reaches zero because of its resonance with C_r. Afterwards, the energy in L_{r1} is transferred to C_r, thus increasing its voltage so that V_{Cr} becomes less negative and eventually becomes positive. As the secondary side of the auxiliary circuit transformer T_x is connected to the output capacitor, C_f, a portion of power is transferred directly to the output from the auxiliary circuit.

At the full-bridge converter, the switch capacitance of Q_3 has been fully discharged and current is flowing through the body-diode of the switch. Q_3 can be turned on with ZVS as long as current is flowing through its body-diode.

Mode 4 ($T_3 < t < T_4$): This mode begins when S_a is turned off with ZCS. V_{Cr} keeps increasing, so the current through S_2 starts to become less negative. The negative current through body diode of S_2 rises to zero, thus the auxiliary diode D_{a2} stops conducting at the end of this mode. At the full-bridge converter, the converter is in a freewheeling mode of operation and current just circulates in the primary side of the converter. At the secondary side, both output diodes conduct current as the voltage across the transformer secondary is zero. During this mode, Q_4 is turned off and the output capacitance of Q_2 begins to discharge while that of Q_4 begins to charge. It should be noted that Fig. 2.9 shows that current flows through the output capacitance sometime in the mode after Q_4 is turned off.

Mode 5 ($T_4 < t < T_5$): This mode begins when the net voltage across the C_r and L_{r1} becomes positive, causing D_1 to start conducting. This mode ends when the current through L_{r1} reaches zero. At the end of this mode, the maximum voltage across the auxiliary capacitor (V_{cm}) can be derived. Meanwhile, current flows through the body-diode of Q_2 during this mode. Q_2 can be turned on with ZVS at the end of this mode.

Mode 6 ($T_5 < t < T_6$): This mode begins when I_{Lr1} reaches zero, thus D_{a1} and D_{x1} stop conducting. During this mode, the current in the magnetizing inductance of the feed forward transformer is discharged to the output by D_{T2}. The voltage across L_1 becomes $V_{in,rec}$-V_o and the current through L_1 starts to decrease linearly. Meanwhile, at the DC-DC full-bridge, the current flowing in the converter primary reverses direction and flows through Q_2 and Q_3 instead of their body-diodes. Current continues to flow through both secondary diodes, but the distribution of current is uneven as the current flowing through D_{T2} is increasing while that flowing through D_{T1} is decreasing.

Mode 7 ($T_6 < t < T_7$): This mode begins when the current in L_1 reaches zero. This is the last mode of the half-cycle. The next half-cycle begins when S_1 is turned on under ZCS. During this mode, the full-bridge converter is able to transfer power to the output as voltage is impressed across the transformer primary.

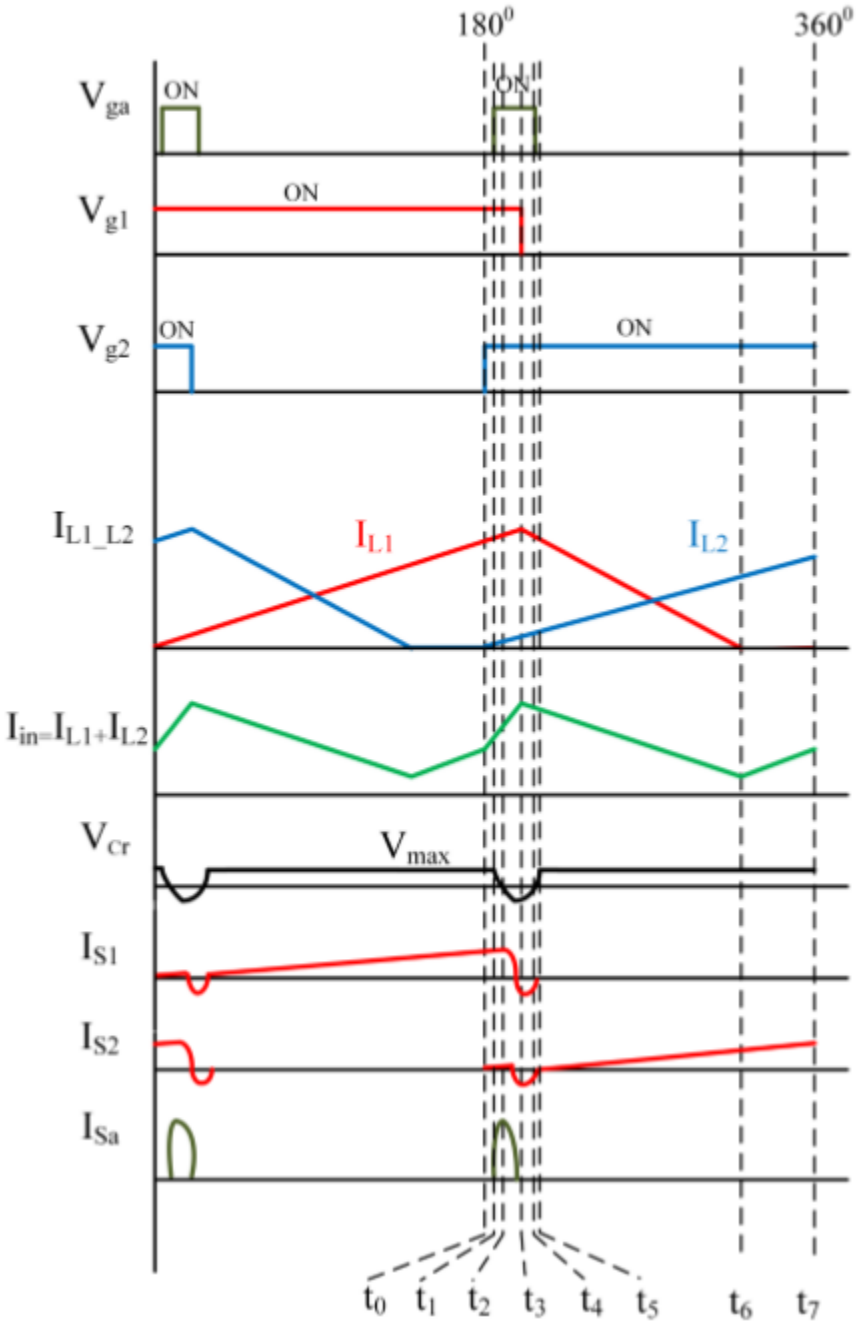


Fig. 2.4. Typical waveforms of the converter shown in Fig. 2.2 [26]

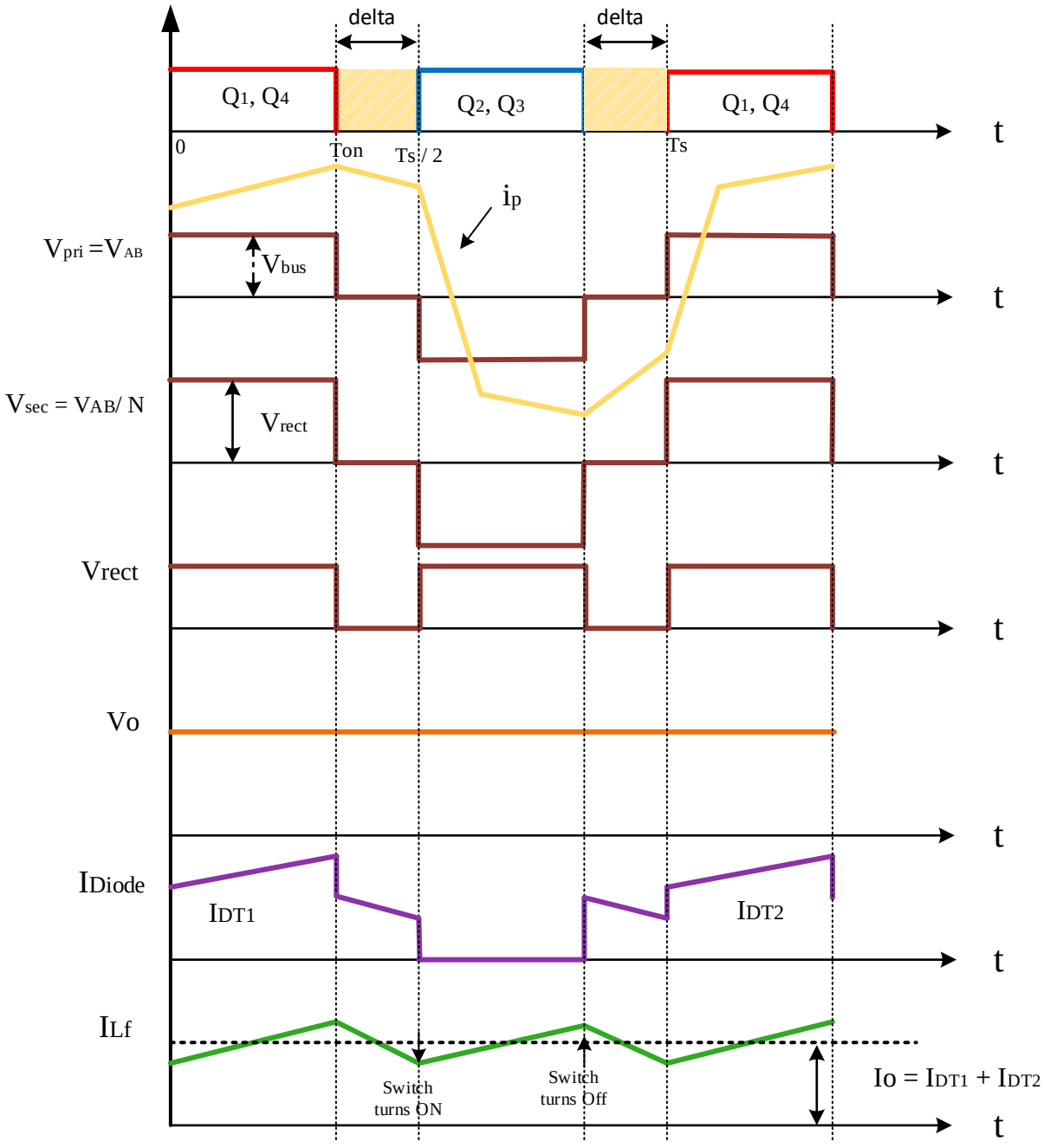


Fig. 2.5. Key waveforms of the full-bridge DC-DC converter

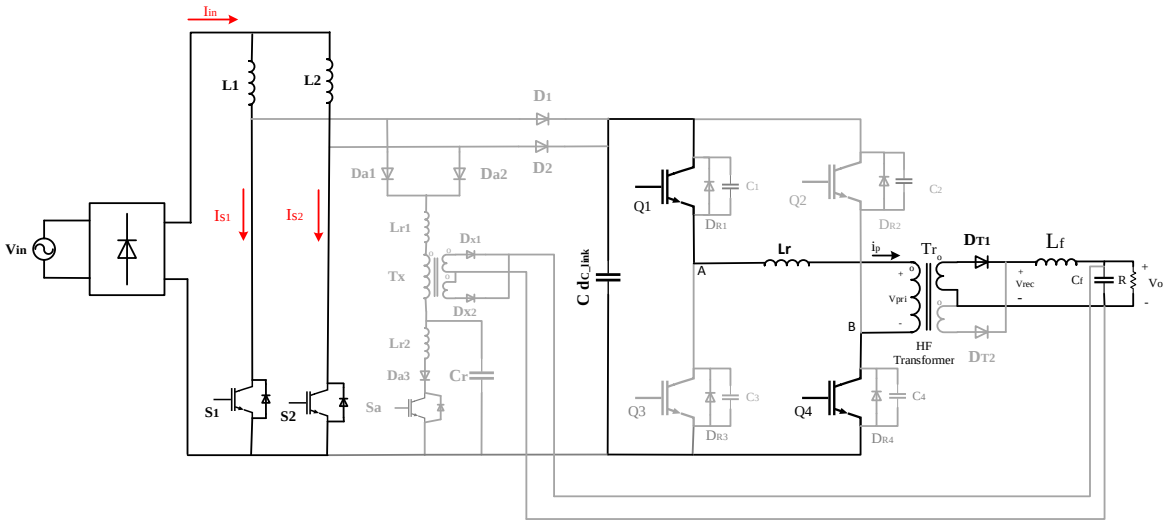


Fig. 2.6. Mode 1

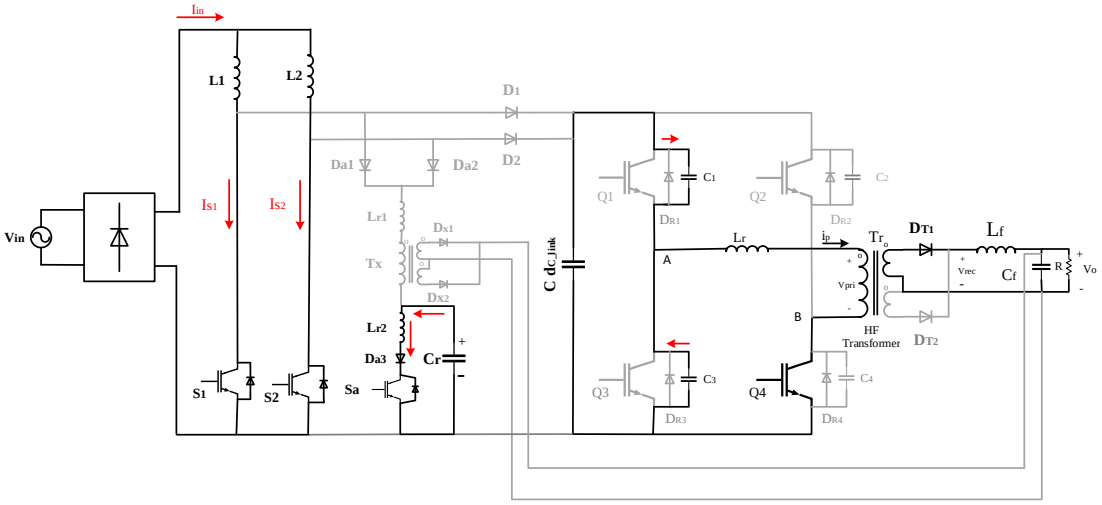


Fig. 2.7. Mode 2

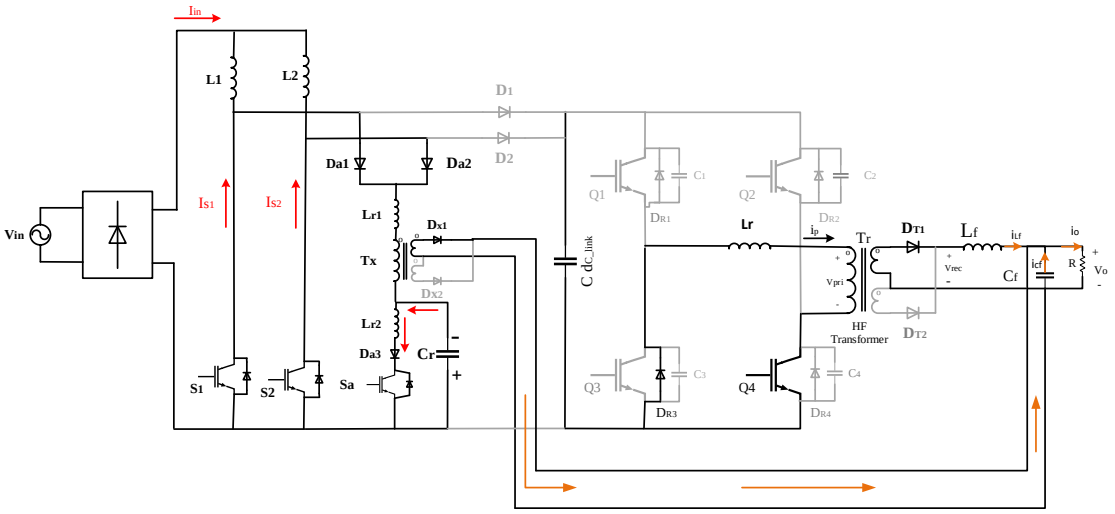


Fig. 2.8. Mode 3

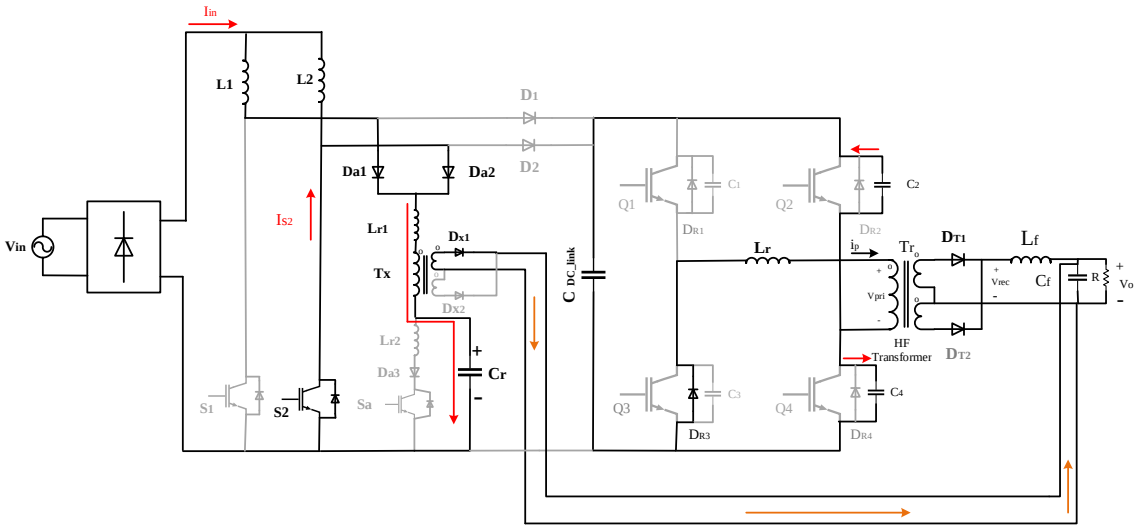


Fig. 2.9. Mode 4

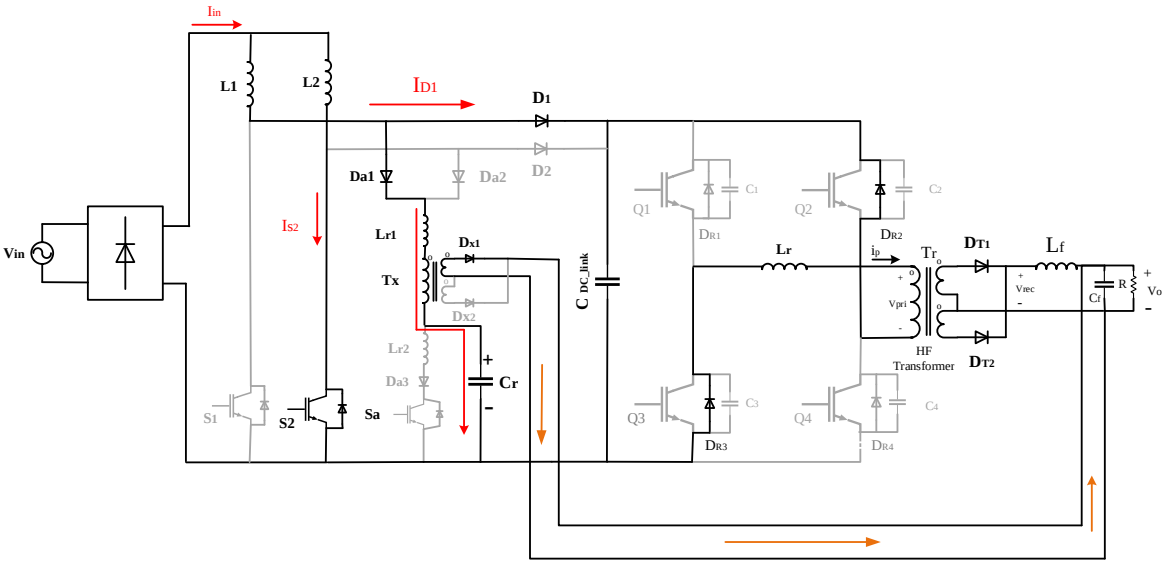


Fig. 2.10. Mode 5

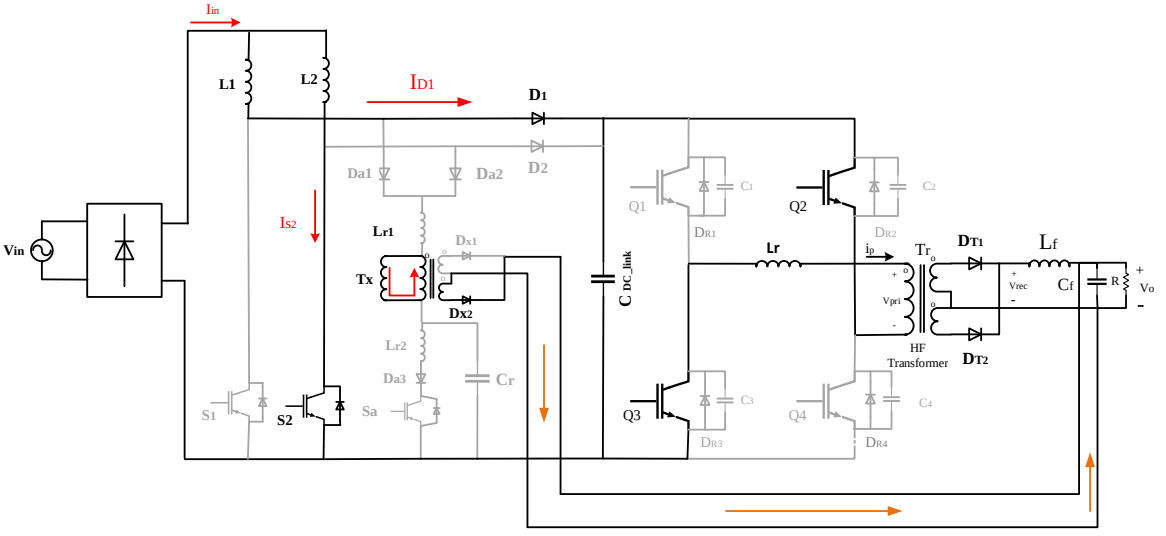


Fig. 2.11. Mode 6

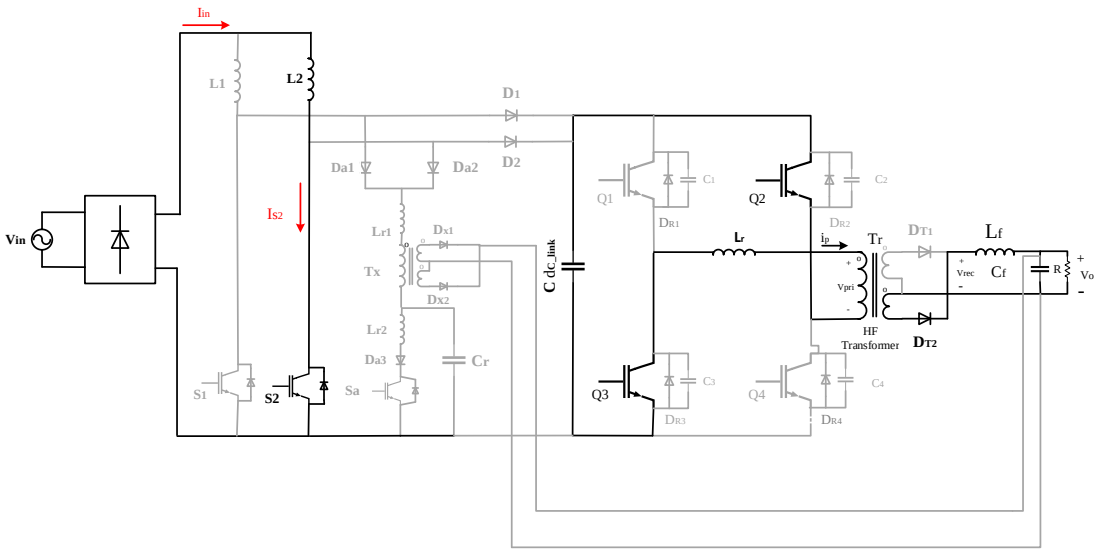


Fig. 2.12. Mode 7

2.5 Converter features

The proposed converter has the following features:

- All the converter switches turn on and off with ZCS.
- There is only one active auxiliary circuit for both main switches instead of each main switch needing its own active auxiliary circuit to help it turn off with ZCS.
- The main switch does not have increased peak and RMS current stresses, as is the case with resonant type ZCS auxiliary circuits, because no current from the auxiliary circuit flows into the main circuit.
- None of the auxiliary circuit components are in the main power path, therefore they only handle a fraction of the current that the main circuit components handle.
- The maximum voltage stress of the auxiliary switch is close to the output voltage because of the transformer. Also, the current in the auxiliary circuit can be transferred to the output to increase efficiency.
- The main boost diodes do not have reverse recovery current because the input inductor currents are discontinuous.
- The auxiliary circuit does not interfere with the interleaving operation of the converter; thus, all the advantages of interleaving are maintained.

- The auxiliary circuit can be deactivated when the converter is operating under light-load conditions, unlike most ZCS methods, where the auxiliary circuit must always be in operation, regardless of the load. This leads to an improvement in the light-load efficiency because it removes the auxiliary circuit losses under operating conditions where the current in the converter is low and ZCS is unnecessary. This can be done because there are no auxiliary circuit components in the main power circuit.
- The auxiliary circuit needs to be operational for a very short amount of time, typically around 0.7 μs. Since the auxiliary transformer is not in series with the auxiliary switch, the maximum voltage of the resonant capacitor increases which leads to faster soft switching for S_1. Also, because L_{r1} is in series with the resonant circuit, the auxiliary switch can go to zero current faster. In addition, since the converter operates in DCM, there is no reverse recovery current for the main diodes, therefore L_{r1} does not need to be chosen high enough to eliminate it. As a result, small L_{r2} can be chosen which decreases the operating time of the auxiliary switch.

2.6 Conclusion

The operation of the proposed two-stage AC-DC converter was discussed in this chapter. First, the operation of the PWM interleaved AC-DC boost front-end converter was explained. This converter uses only a single active auxiliary circuit to help all the main converter switches operate with ZCS and operates with ZCS itself. The auxiliary switch works for only a very small fraction of the switching cycle so that the converter generally operates as a conventional PWM interleaved boost converter. Next, the modes of operation of a conventional full-bridge ZVS-PWM DC-DC converter were explained. This converter steps down the output voltage produced by the first AC-DC stage and provides isolation using a high-frequency transformer. The modes of operation that the converter goes through during a half switching cycle were presented and explained. Finally, the features of the proposed converter were stated. The distinguishing feature of the converter is that it has a transformer in the auxiliary circuit of its front-end converter that not only ensures the soft-switching of its switches, but also provides a path for power to be transferred directly to the output, which helps reduce converter losses, as will be shown later in this thesis.

Chapter 3

3 Converter circuit analysis

3.1 Introduction

In this chapter, the steady-state analysis of the proposed two-stage AC-DC power converter is performed. The purpose of this analysis is to determine equations and formulas that can be used to develop a design procedure for key converter components in the next chapter. Since the operation of the two converter stages can be considered to be independent of each other, in general, the analysis of each converter will be considered separately.

3.2 AC-DC interleaved boost converter

The circuit analysis that is presented in this chapter will focus mainly on two things:

- The soft-switching operation of the converter switches.
- The amount of power that can be directly transferred from the first-stage to the output, bypassing the DC-DC full-bridge converter.

The analysis will be done by solving key equations that characterize the modes of operation that were presented in the previous section, then using these equations to develop a MATLAB program that can be used to develop graphs of steady-state characteristic curves that can be used to develop a design procedure for the converter. The following assumptions are made to simply the analysis of the circuit:

- The converter operates under steady-state conditions.
- Since the AC input voltage can be considered to be a DC input source for a very short portion of the AC line cycle, the steady-state analysis is done with DC input voltage when short switching cycles are considered.
- All components, including semiconductor switches, inductors, capacitors, and diodes of the converter are considered to be ideal.
- Transformer T_x, the main power transformer in the DC-DC full-bridge stage, is considered as an ideal transformer in series with a primary leakage inductance L_r.

- When current is flowing through the auxiliary circuit, the maximum primary voltage of the transformer T_x, is clamped to $V_x=V_o / N_x$, where $N_x= N_2 / N_1$. The polarity of the primary voltage of the auxiliary transformer is dependent on the polarity of the current and on whether it is secondary diode D_{x1} or D_{x2} that is conducting.
- The proposed circuit has two boost modules that are designed to be operated in DCM, so that the input inductor current of each one is discontinuous, but the actual input current of the converter, which is the sum of these inductor currents is continuous.
- When the auxiliary circuit is operating, the input current, I_{in}, and the output voltage, Vo, are considered to be fixed, with no ripple.
- As the second half-cycle of a switching cycle is equal to that of first half-cycle, circuit analysis is performed for the first half-cycle of the operation when the switch S_2 begins to turn on and switch S_1 begins to turn off.

The analysis can proceed as follows:

Mode 1 ($t_0 < t < t_1$): This interval begins when switch S_2 is turned on and current through L_2 starts to rise. The auxiliary circuit is not active during this mode and power P_{ps} is processed by two converter stages. During this mode, the resonant capacitor is charged to V_{cr0}.

Mode 2 ($t_1 < t < t_2$): This interval begins when the auxiliary switch, S_a, is turned on under ZCS condition. Since S_a is in series with resonant inductor L_{r2}, the rate of the auxiliary switch current is limited and thus the switch can be turned on with ZCS. During this mode, auxiliary circuit current rises, and the value of V_{Cr} reduces until reaches zero at the end of this mode. The current through resonant inductor L_{r1} is zero so the primary current passing through the auxiliary transformer is zero; therefore, there is no power to the output through the auxiliary transformer in this mode.

By applying KCL, the following equation can be obtained:

$$i_{Lr2}(t_2) = i_{cr}(t_2) = -\frac{d}{dt} q_{cr}(t_2) = -C_r \frac{d}{dt} V_{cr}(t_2) \quad (3\text{-}1)$$

By applying KVL and considering $V_{cr}(0) = V_{cm}$ as the initial condition for the capacitor voltage, where V_{cm} is the maximum voltage across the capacitor and $i_{Lr2}(0) = 0$ as the initial condition for the auxiliary inductor current, the following expression can be written

$$V_{cr}(t_2) = -V_{cm} \cos \omega_2 t_2 \qquad T_1 < t < T_2 \quad (3\text{-}2)$$

where $\omega_2 = \frac{1}{\sqrt{L_{r2} C_r}}$.

The maximum current through the auxiliary circuit at the end of this mode can be expressed as

$$i_{Lr2}(t_2) = i_{smax} = \frac{V_{Cm}}{Z_2} \qquad t = T_2 \quad (3\text{-}3)$$

Mode 3 ($t_2 < t < t_3$): This interval begins when the voltage across C_r, reaches zero and the current flowing through the auxiliary current reaches its maximum value. During this interval, current is diverted from S_1 and S_2 to auxiliary switch so that the current through the main switches becomes negative and their body diodes start to conduct. This allows S_1 to be turned off with ZCS condition at the end of this mode t_3. When the auxiliary circuit is operating, D_{a1} and D_{a2} begin to conduct, and a portion of the power in the auxiliary circuit is transferred to the output of the converter. The voltage across the primary of the transformer T_x, is no longer zero volts but is clamped to $V_x = \frac{V_0}{N_x}$, where N_x is the turn ratio of the auxiliary transformer, $N_x = \frac{N_2}{N_1}$.

In this mode of operation, input power can be transferred to the output through two different paths. Most of the power transferred to the output is through the DC-link capacitor and then the DC-DC full bridge converter. A portion of the energy in the auxiliary circuit is transferred through the auxiliary transformer to the output, P_{DPT}. The total power that is delivered to the output can be expressed as:

$$P_o(t) = P_{DPT}(t) + P_{ps}(t) \quad (3\text{-}4)$$

To calculate the average power through the auxiliary transformer transferred to the output, the instantaneous power v_x (t). i_x (t) is calculated. By applying KCL in the resonant circuit, the primary current through auxiliary circuit can be expressed as:

$$i_x(t_3) = i_{Lr2}(t_3) + i_{Cr}(t_3) \tag{3-5}$$

The initial values of $V_{Cr}(t_2)$ and $i_{Lr1}(t_2)$ are both zero. The initial current through the second auxiliary inductor $i_{Lr2}(t_2)$ in this mode is derived from the end of Mode 2 and is

$$i_{Lr2}(t_2) = \frac{V_{cm}}{Z_2} \tag{3-6}$$

Differentiating equ. (3-5) with respect to time results in the following equation:

$$\frac{V_{cr}}{L_{eq}}(t_3) = -C_r \frac{d^2}{dt^2} V_{Cr}(t_3) - \frac{V_x L_{r2}}{L_{r1} L_{r2}}(t_3) \tag{3-7}$$

where

By solving equation (3-7), the voltage across C_r can be expressed as follows:

$$V_{Cr}(t_3) = \frac{V_x \omega_1^2 (\cos(\omega_e t3) - 1)}{\omega_e^2} - \frac{(V_{cm} Ze)(\sin(\omega_e t3))}{Z_2} \tag{3-8}$$

where

$$\omega_1 = \frac{1}{\sqrt{L_{r1} C_r}}$$

$$\omega_e = \frac{1}{\sqrt{L_e C_r}}$$

$$Z_2 = \sqrt{\frac{L_{r2}}{C_r}}$$

$$L_{eq} = \frac{L_{r1} L_{r2}}{L_{r1} + L_{r2}} \tag{3-9}$$

If KVL is applied, the primary voltage across the auxiliary transformer V_x can be expressed as:

$$V_{D1} - V_{Cr} - V_{Lr1} - V_X + V_o = 0 \tag{3-10}$$

D_1 is off during this mode so that voltage across V_{D1} is:

$$V_{D1} = V_o \tag{3-11}$$

and the voltage across L_{r1} is:

$$V_{Lr1} = -(V_{Cr} + V_X) \tag{3-12}$$

V_{Lr1} is at its maximum since all the currents go to L_{r1} at that time so that:

$$V_{Lr1}(t_3) = \frac{(V_{cm} Z_e)\sin(\omega_e t_3)}{Z_2} - \frac{(V_x \omega_1^2)(\cos(\omega_e t_3) - 1)}{\omega_e^2} - V_x \tag{3-13}$$

By substituting equation (3-9) into (3-12) and then into equation (3-14), the primary current through the auxiliary transformer can be expressed as follows:

$$i_x(t) = i_{Lr1}(t) = \frac{1}{L_{r1}} \int_{t_2}^{t_3} V_{Lr1}(t) \tag{3-14}$$

which can be solved to give:

$$i_x(t_3) = \frac{(V_{cm} L_e)(1 - \cos(\omega_e t_3))}{Z_2 L_{r1}} + \frac{(V_X L_e)(t_3 - \frac{\sin(\omega_e t_3)}{\omega_e})}{L_{r1}^2} - \frac{V_x t_3}{L_{r1}} \tag{3-15}$$

By substituting the primary current and the primary voltage $V_x = \frac{V_o}{Nx}$ of the transformer in the instantaneous output power equation, we can calculate the amount of power transferred through the auxiliary circuit, when the auxiliary switch is turned on and the auxiliary circuit is operating, as follows:

$$P_{DPT\_Mode3} = \frac{1}{T_s} \int_{t_2}^{t_3} V_x(t)\, i_x(t) \tag{3-16}$$

By solving equ. (3-15) in Mode 3 the average power can be expressed as

$$P_{DPT\_ave3} = [\frac{v_o^2\ \omega_e^2 t^2 (l_e - l_{r1}) + 2 l_e\ \cos(\omega_e t)}{2\ \omega_e^2\ N_x^2 l_{r1}^2 \mathrm{fs}} + \frac{v_{cm} l_e l_{r1} v_o \sin(\omega_e t) - \omega_e t}{\omega_e N_x l_{r1}^2 Z_2 \mathrm{fs}}] \qquad t \in [t_2, t_3] \quad (3\text{-}17)$$

Equation (3-17) shows that P_{DPT} is inversely proportional to the turns ratio of the auxiliary circuit transformer. Consequently, as the turn ratio rises, the amount of power transferred to the output through auxiliary transformer decreases. To ensure ZCS operation in this mode, the current through the main switch, I_{S1} should go to zero or be negative; therefore, the direction of current through S_1 changes so that the current flows through the body diode of the device. This can be expressed as

$$i_{in}(t_3) - i_{Lr1}(t_3) \leq 0 \quad (3\text{-}18)$$

This means that current i_{Lr1} should be greater than input current in order for the main switches to turn off with ZCS. The auxiliary switch should be turned off soon afterwards. For this purpose, the current through the auxiliary circuit should go to zero or negative so that S_a turns off with ZCS at the end of this mode.

Mode 4 ($t_3 < t < t_4$): This mode begins when the current through the auxiliary switch goes to zero and S_a is turned off with ZCS. The voltage across C_r rises and the current through the main switch S_2 becomes less negative. Power continues to be transferred from the auxiliary circuit to the output.

By considering the initial value of the voltage across the resonant capacitor to be $V_{Cr\_4}(0)$ at t_3, the maximum voltage of the resonant capacitor in this mode can be expressed as:

$$V_{Cr}(t_4) = (V_{Cr\_4}(0) + V_x)(\cos(\omega_1 t_4)) + \frac{i_{Lr1}(0)\sin(\omega_1 t_4)}{C_r\ \omega_1} - V_x \quad (3\text{-}19)$$

To calculate the average power transferred to the output through the auxiliary transformer during this mode, instantaneous power $v_x(t).\ i_x(t)$ during the duration of this mode needs to be derived.

By considering the initial value of the primary current to be $i_{x\_4}(0)$ at t_3, the primary current through the auxiliary transformer can be expressed as:

$$i_x(t_4) = \frac{(V_{cm}L_e)(1-\cos(W_e t_3))}{Z_2 L_{r1}} + \frac{(V_x L_e)(t_3 - \frac{\sin(w_e t_3)}{w_e})}{L_{r1}^2} - \frac{V_x t_3}{L_{r1}} \quad (3\text{-}20)$$

By substituting (3-20) and V_x into (3-21)

$$P_{DPT\_Mode4} = \frac{1}{T_s}\int_{t_3}^{t_4} V_x(t)\, i_x(t) \quad (3\text{-}21)$$

and integrating, the following expression can be derived for P_{DPT}:

$$P_{DPT\_ave4} = \left[\frac{v_o^2\, \omega_e^2 t^2 (l_e - l_{r1}) + 2 l_e \cos(\omega_e t)}{2\, \omega_e^2\, N_x^2 l_{r1}^2\, fs} + \frac{v_{cm}\, l_e l_{r1} v_o \sin(\omega_e t) - \omega_e t}{\omega_e N_x l_{r1}^2 Z_2\, fs}\right] \qquad t \in [t_3, t_4] \quad (3\text{-}22)$$

Mode 5 ($t_4 < t < t_5$): During this mode, V_{cr} continues to increase until it reaches its maximum value at the end of this mode, at t_5, as a result of the resonant interaction among auxiliary circuit components. By considering the initial condition for the voltage across C_r to be $V_{Cr\_5}(0)$ at t_4, the following equation can be derived:

$$V_{cr}(t_5) = (V_{cr\_5}(0) + V_x)(\cos(\omega_1 t_5)) + \frac{i_{Lr1_5}(0)(\sin(\omega_1 t_5)}{C_r \omega_1} - V_x \quad (3\text{-}23)$$

Auxiliary switch S_a can be turned off during this mode so that all the current flowing in the auxiliary circuit goes to the capacitor C_r, which is in series with the primary winding of the auxiliary transformer. This current can be expressed as follows:

$$i_{Cr}(t_5) = i_x(t_5) = C_r \frac{dv_{cr}}{dt}(t_5) \quad (3\text{-}24)$$

By differentiating equ. (3-24) with respect to time, the following equation can be derived:

$$-\frac{d^2 V_{cr}(t_5)}{dt^2} - \frac{V_{cr}}{L_{r1} C_r}(t_5) - \frac{V_x}{L_{r1} C_r} = 0 \quad (3\text{-}25)$$

To calculate the portion of power transferred to the output, it is required to derive the primary current i_x flowing through the primary winding of the auxiliary transformer. By considering $i_{x\_5}(0) = I_{x\_5}$ as an initial value for the primary current and $V_{cr\_5}(0) = 0$ as an initial voltage for the auxiliary capacitor and solving equ. (3-25), the primary current through the auxiliary transformer can be expressed as follows:

$$i_x(t_5) = -((C_r w_1)(V_{Cr\_5}(0) + V_x)(\sin(\omega_1 t_5))) + (i_{x\_5}(0)(\cos(\omega_1 t_5))) \quad (3\text{-}26)$$

The power can be expressed as:

$$P_{DPT\_Mode5} = \frac{1}{T_s}\int_{t_4}^{t_5} V_x(t)\, i_x(t) \quad (3\text{-}27)$$

By substituting equ. (3-26) and V_x into equ. (3-27), the average power in Mode 5 can be expressed as:

$$P_{DPT\_ave5} = \left[\frac{2v_o I_{x\_5}\cos(\frac{\omega_1 t}{2})\sin(\frac{\omega_1 t}{2})}{N_x\omega_1^2 fs} + \frac{2\,v_o C_r \cos(\frac{\omega_1 t}{2})}{N_x^2\omega_1 fs}\right] \qquad t \in [t_4, t_5] \quad (3\text{-}28)$$

Mode 6 ($t_5 < t < t_6$): This mode begins when the current through L_{r1} goes to zero and the transformer begins to demagnetize. D_{x1} stops conducting current and D_{x2} start conducting. The amount of power transferred to the output during this mode will be less than that transferred during Modes 3-5.

The initial conditions for the auxiliary circuit capacitor voltage and the current through the primary winding are $V_{cr\_6}(0)$ and $i_{x\_6}(0)$ at t_5. At t_5, the voltage reaches its maximum value and remains fixed throughout this mode so that $V_{cr\_6}(0) = V_{cm}$. The following expressions can be written for C_r:

$$i_{Cr}(t_6) = i_x(t_6) = C_r\frac{dv_{Cr}}{dt}(t_6) \quad (3\text{-}29)$$

$$-\frac{d^2V_{Cr}(t_5)}{dt^2} - \frac{V_{Cr}(t_5)}{L_{r1}C_r} - \frac{V_x - V_0}{L_{r1}C_r} = 0 \quad (3\text{-}30)$$

Solving these equations gives the voltage of the auxiliary capacitor at the end of this mode, which is:

$$V_{Cr}(t_6) = (V_{Cr\_6}(0) + V_x - V_0)(\cos(\omega_1 t_6)) + \frac{i_{x\_6}(0)(\sin(\omega_1 t_6))}{C_r\omega_1} - V_x + V_o \quad (3\text{-}31)$$

The current through the primary winding of the auxiliary transformer can be expressed as:

$$i_x(t_6) = ((C_r\omega_1)(V_{Cr\_6}(0) + V_x - V_o)(\sin(\omega_1 t_6))) + (i_{x\_6}(0)(\cos(\omega_1 t_6))) \quad (3\text{-}32)$$

By substituting equ. (3-32) and V_x into equ. (3-33),

$$P_{DPT\_Mode6} = \frac{1}{T_s}\int_{t_5}^{t_6} V_x(t)\, i_x(t) \quad (3\text{-}33)$$

and considering $i_{x\_6}(0) = I_{x\_6}$, the average power in this mode can be determined to be:

$$P_{DPT\_ave6} = \left[\frac{2v_o\cos\left(\frac{\omega_1 t}{2}\right)\left[I_{x\_6}\sin\left(\frac{\omega_1 t}{2}\right)+v_{cm}C_r\omega_1\cos\left(\frac{\omega_1 t}{2}\right)+C_r v_o\omega_1\cos\left(\frac{\omega_1 t}{2}\right)\right.}{N_x\omega_1^2\, fs} + \frac{2\, v_0^2 C_r\cos\left(\frac{\omega_1 t}{2}\right)^2}{N_x^2 fs}\right] \; t \in [t_5, t_6] \quad (3\text{-}34)$$

Substituting the average power that has been calculated from Mode 3 to Mode 6 (i.e (3-17), (3-22), (3-28), (3-34)) in equ. (3-35), the entire power that the auxiliary circuit can transfer directly to the output can be calculated as follows:

$$P_{DPT} = P_{DPT\_ave3} + P_{DPT\_ave4} + P_{DPT\_ave5} + P_{DPT\_ave6} \quad (3\text{-}35)$$

By solving this equation, the output power can be expressed as an equation based on the variables C_r, L_{r1}, L_{r2}, V_o, N_x

In the proposed converter, the DC bus voltage V_{bus} is determined so that the charge/discharge current balance for the DC bus capacitor is satisfied. The steady-state DC bus voltage level can be derived by equating the averaged input power P_{in} with the output power P_o (the converter is assumed to be ideal); thus, the following equation must be satisfied:

$$V_{in}\, I_{in} = P_{tran} + P_{DPT} \quad (3\text{-}36)$$

Fig. 3.1, shows a flowchart that illustrates the steady-state operation of the auxiliary transformer. Steady-state operation is confirmed by determining whether the current through auxiliary transformer I_{Lr1} after the auxiliary circuit has completed a cycle is equal to its initial value, which is zero. Under this condition, the primary current through the auxiliary transformer remains constant over time. Once it is confirmed that the auxiliary circuit is operating under steady-state condition, the value of the certain current can be determined for a specific operating point so that a curve can be generated by repeating the process for multiple operating points.

Assuming that all the switches and the auxiliary transformer are ideal with negligible magnetizing inductance, then the current flowing through the primary winding can be determined for any operating point with a given resonant capacitor C_r, resonant inductor L_{r1} and L_{r2}, transformer turns ratio $N_x = N_2 / N_1$. This flowchart is to confirm that the value of the primary current through the auxiliary transformer at the beginning mode of the operation is equal to that of the last mode of operation; that is Mode 3 to Mode 6. If not, the initial values should be changed, and the procedure repeated with a new initial value assumed.

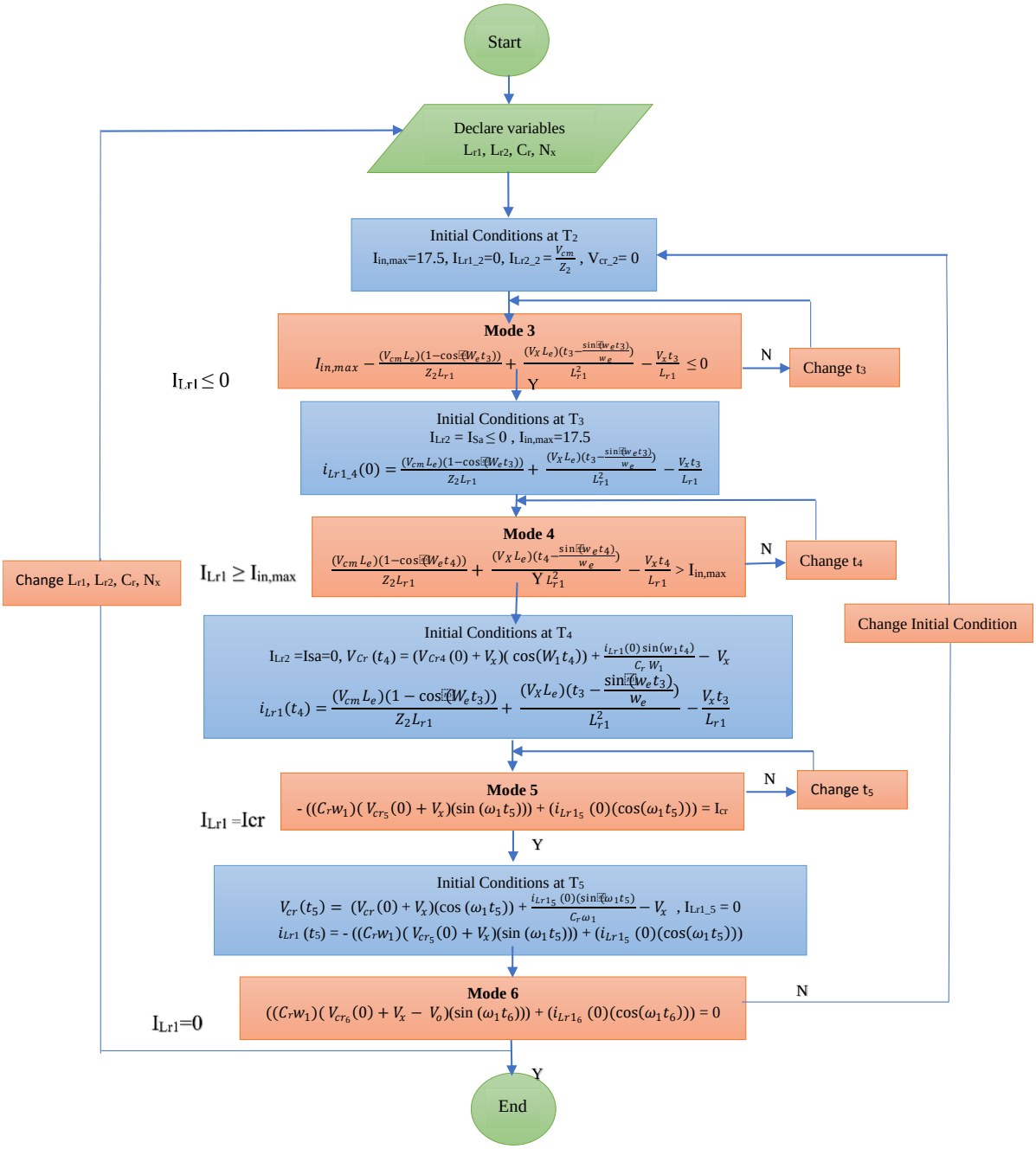


Fig. 3.1. Flow chart of the program to determine if the converter is operating under steady-state conditions to obtain the value of $i_{Lr1}=i_x$

3.3 Zero-Voltage Switching (ZVS) Pulse-Width Modulated (PWM) Full-Bridge Converter

The second stage of the proposed converter is a conventional ZVS-PWM full-bridge converter, as described in the previous chapter. The converter has 14 modes of operation over a switching cycle, but only 7 need to be considered in the analysis as the modes for one half-cycle are very similar to those of the other half-cycle. Although all four switches operate with ZVS, the mechanism by which each leg operates with ZVS is different. Q_1 and Q_3 use the energy stored in the output filter inductor and Q_2 and Q_4 use energy stored in the resonant inductance, L_r, to generate a ZVS turn on. A dead time is considered between drive signals to avoid cross conduction between switches of each leg, $Q_1 – Q_3$ and Q_2-Q_4 and to discharge the output capacitance of any switch that is about to be turned on.

The following assumptions are made for the analysis.

- The converter is operating under steady state condition.
- The output inductor current is continuous.
- The output voltage is a constant value of 48V.
- The converter switches, diodes, and transformer are ideal.
- The output switch capacitances are ideal with $C_1 = C_3 = C_{lead}$, $C_2 = C_4 = C_{lag}$.

It should be noted that the operation of the second DC-DC full-bridge is independent of that of the first-stage converter.

Mode 1 ($T_0 < t < T_1$): In this mode, Q_1 and Q_4 are in operation, allowing the primary current i_p to pass through them. At the same time, on the secondary side, rectifier diode D_{T1} is active.

Mode 2 ($T_1 < t < T_2$): As the output inductor is considered to be large enough, the primary current of the main power transformer, i_p, is nearly constant and can be expressed as:

$$i_p(t) = I_p(t_1) \triangleq I_1 \tag{3-37}$$

The voltages across parallel capacitors C_1 and C_3 can be expressed as:

$$V_{C1}(t) = \frac{I_1}{2C_{lead}}(t - t_1) \tag{3-38}$$

$$V_{C3}(t) = V_{in} - \frac{I_1}{2C_{lead}}(t - t_1) \tag{3-39}$$

At the end of this mode, C_1 is charged to V_{bus} and C_3 is completely discharged to zero, making the body diode of switch S_3, D_3, conduct.

Mode 3 ($T_2 < t < T_3$): In order to achieve ZVS for Q_3, the dead time should be larger than the time interval of Mode 2. This condition can be expressed as:

$$t_{d(lead)} > 2\, C_{lead}\, V_{bus} / I_1 \tag{3-40}$$

At t_3, the current through secondary winding is smaller than the current through the output inductor current; that is $i_{T1} < i_{Lf}$, so D_{T2} starts conducting. If the magnetizing current of the transformer is neglected, then:

$$i_{Lf} = i_{T1} + i_{T2} = N.i_p \tag{3-41}$$

Mode 4 ($T_3 < t < T_4$): The transformer primary current, i_p, can be expressed as

$$i_p(t) = I_2 \cos\omega_1 (t - t_3) \tag{3-42}$$

The voltages across C_2 and C_4 are defined as

$$V_{C4}(t) = Z_1 I_2 \sin\omega_1 (t - t_3) \tag{3-43}$$

$$V_{C2}(t) = V_{in} - Z_1 I_2 \sin\omega_1 (t - t_3) \tag{3-44}$$

where $Z_1 = \sqrt{L_r / (2C_{lag})}$ and $\omega_1 = \frac{1}{\sqrt{2LrC_{lag}}}$.

Mode 5 ($T_4 < t < T_5$): As discussed in Chapter 2, the dead time between high side and low side drive signals of Q_2 and Q_4 in Mode 5 should be larger than the dead time in Mode 4. That is:

$$t_{d(lag)} > \frac{1}{\omega 1} \sin^{-1} \frac{V_{bus}}{Z_1 I_2} \tag{3-45}$$

During this mode, a negative voltage is applied to the resonant inductor, which can be the primary-side transformer leakage inductance alone or the leakage inductance plus some additional inductance that is added in series with the transformer. This causes the primary current to decrease linearly and reach zero at the end of this mode. This current can be expressed as:

$$i_p(t) = I_p(t_4) - \frac{V_{bus}}{L_r}(t - t_4) \quad (3\text{-}46)$$

It should be noted that from t_3 to t_5, $i_p > 0$, and $i_{T1} > i_{T2}$. At t_5, $i_{T1} = i_{T2} = i_{Lf}/2$.

Mode 6 ($T_5 < t < T_6$): As discussed in Chapter 2 the current through the resonant inductor causes the primary current to start increasing in the reverse direction. The slope of the primary current can be expressed as

$$i_p(t) = -\frac{V_{bus}}{Lr}(t - t_5) \quad (3\text{-}47)$$

The rectifier diode D_{T1} turns off and the output inductor current flows through D_{T2}. It should be noted that during this mode, $i_p < 0$ and $i_{DR1} < i_{T2}$. At t_6, $i_{T2} = i_{Lf}$ and $i_{T1} = 0$.

Mode 7 ($T_6 < t < T_7$): The primary current slope during this mode can be expressed as

$$i_p(t) = -\frac{V_{bus} - NV_o}{Lr + N^2 Lf}(t - t_6) - \frac{I_{Lf}(t_6)}{N} \quad (3\text{-}48)$$

By considering $L_r \ll N^2 \cdot L_f$, where is N is the turn ratio of the transformer, equ.(3-48) can be simplified to:

$$i_p(t) = -\frac{\frac{V_{in}}{N} - V_o}{NL_f}(t - t_6) - \frac{I_{Lf}(t_6)}{N} \quad (3\text{-}49)$$

This mode ends once Q_3 is turned off and the second half-cycle starts.

3.3.1 ZVS for lagging leg

The required energy that ensures ZVS for the lagging leg switches (the switches that get the converter out of a freewheeling mode of operation when turned on) is stored in resonance inductor. This energy should be enough to charge and discharge the output

capacitor of the switches, otherwise the switches cannot be turned on with ZVS, thus causing switching losses. The maximum voltage across the output capacitors is equal to the V_{bus} at one fourth of the resonant cycle, $T_r/4$. To achieve ZVS for the lagging leg switches, the following condition must be met:

$$\frac{1}{2} L_r I_1^2 > \frac{1}{2} (C_2 + C_4) V_{bus}^2 \quad (3\text{-}50)$$

Where I_1 is the primary transformer current at turn-on/turn-off of Q_2 and Q_4. The critical current in which ZVS is lost is:

$$I_{critical} = \sqrt{\frac{C_2+C_4}{L_r}} \cdot V_{bus} \quad (3\text{-}51)$$

The choice of L_r inductance is made by taking into account the desired minimum load at which the converter starts to work in ZVS (usually 25% of maximum load). When $I_1 > I_{critical}$, the converter switches can turn on with ZVS.

3.3.2 ZVS for leading leg

The energy needed to ensure that the leading leg switches (the switches that force the converter into a freewheeling mode of operation when turned on) is supplied by the resonant inductor and the output filter inductor. This energy is larger than the energy required for lagging leg. ZVS operation for the leading leg switches can be ensured if the following condition is met:

$$\frac{1}{2} (L_r + L_{fp}) I_2^2 > \frac{1}{2} (C_1 + C_3) V_{bus}^2 \quad (3\text{-}52)$$

where I_2 is the primary transformer current at turn-off of Q_1 or Q_3 (peak value of transformer current) and $L_{fp}=N^2L_f$ is the output filter inductance referred to the primary.

3.3.3 Secondary duty cycle loss:

During the intervals [t_3, t_6] and [t_9, t_{12}], the primary current changes its polarity as the direction of primary current changes. Due to the presence of the resonant inductor at the primary, there is a loss in duty cycle so that the effective secondary duty cycle is less than that of the primary. This loss can be defined as:

$$\Delta D = \mathrm{D} - D_{eff} \tag{3- 53}$$

Where D_{eff} is the effective secondary duty cycle, D is the primary duty cycle. The relationship between the primary and secondary duty cycle can be expressed as:

$$\mathrm{D} = D_{eff}\,(1 + 4\,\frac{L_{lk}}{R'}\,f_s) \tag{3- 54}$$

where L_{lk} is the leakage inductance of the transformer and R' is the load resistance reflected to the primary side of the converter, which can be defined as:

$$R' = N^2\,R_0 \tag{3- 55}$$

The amount of the energy circulating in the circuit depends on the effective secondary duty cycle, which can be defined as:

$$D_{eff} = \frac{N\,(V_0 + V_f)}{V_{bus}} \tag{3- 56}$$

where V_f is the diode rectifier forward voltage at the secondary of the transformer. Assuming that the resonant inductor is the same as the transformer leakage inductance, L_{lk}, which is typically the case, L_{lk} needs to be large enough to ensure that the converter operates with ZVS, but not so large that the duty cycle loss is unacceptable.

The voltage gain of the converter can be determined by considering the effect of the secondary duty cycle as follows:

$$\frac{V_{out}}{V_{DC\_link}} = \frac{N_s}{N_p}\,D_{eff} \tag{3- 57}$$

3.4 Conclusion

In this chapter, the steady-state analysis of the proposed two-stage AC-DC power converter was performed. The power distribution and the ZCS operation for the AC-DC interleaved boost converter stage and the ZVS operation for the ZVS -PWM full bridge converter stage was explained, and relevant equations were derived for significant modes of operation. The

results of the analysis will be used to develop a design procedure for key converter components in the next chapter.

Chapter 4

4 Design procedure and example

4.1 Introduction

In this chapter, a procedure to design the key components of the first-stage AC-DC boost converter and the second-stage DC-DC full bridge converter is presented. The procedure has been developed based on the analysis that was performed in the previous chapter. The procedure is demonstrated with an example.

4.2 Design procedure for the AC-DC interleaved boost converter

A design procedure for the main components of the front-end AC-DC interleaved boost converter is presented in this section. The procedure has been developed using the analysis that was performed in the previous section and is demonstrated with an example. The components that are to be designed include L_1, L_2 which are the input inductor of each boost converter module, D_1-D_2 and S_1-S_2 which are the main diodes and main switches respectively.

The parameters are to be designed with the following specifications:

- DC Link Voltage: V_{bus}= 400 V DC
- Output Voltage V_o = 48 V DC
- Output Power: P_o = 1 kW
- I_{in}= Rectified input current,
- Input Voltage: V_{in}= 85- 265 V RMS
- Expected Efficiency: η = 95 %
- Main Switching Frequency: $f_s = \frac{1}{T_s}$ = 50 kHz.
- Auxiliary Switching Frequency: $f_s = \frac{1}{T_s}$ = 100 kHz

The circuit is designed and analyzed for the worst-case scenario, which is V_{in} = 85 V, which is when the input current is at its maximum rms value. If the converter can operate under worst-case conditions, then it can work under all other conditions.

4.2.1 Input inductors L_1 and L_2

Since the front-end AC-DC boost converter stage is an interleaved converter that is made up of two boost converter modules that operate in DCM, the value of the input inductors must be such that the input current is discontinuous, even when it is at its maximum value, which occurs when the input voltage is 85 V. This can be done by first determining the maximum duty cycle when the converter is operating in discontinuous mode as follows:

$$D_{max} < 1 - \frac{V_{in,peak}}{V_{bus}} \tag{4-1}$$

$$D_{max} < 1 - \frac{\sqrt{2} * 85}{400} \rightarrow \quad D_{max} < 0.7$$

A value of D_{max} =0.65 is chosen for the main boost converter switches, S_1 and S_2. A value for the input inductors can be determined as follows:

$$L_{in,max} < \frac{D(1-D)^2 \ V_{bus}^2}{2fsw\ P} \rightarrow \frac{0.65\ (1-0.65)^2 * \ 400^2}{2 * 50000 * 1000} < 127\mu H$$

where $L_{in,max}$ is the maximum value for L_1 and L_2, D is the duty cycle of the main switches, V_{bus} is the voltage at DC link and f_{sw} is the switching frequency of the main switches, 50 kHz. During each switching cycle, the auxiliary switch operates two times: once when it is turned on to ensure that S_1 is turned off with ZCS; a second time to ensure that S_2 is turned off with ZCS. The auxiliary switch operates with a switching frequency of 100 kHz.

4.2.2 DC link capacitor

The dc link capacitor is the capacitor that is placed between the two stages of the converter, right at the output of the front-end AC-DC stage. Although the main purpose of the capacitor is to act as a filter and smooth the output of the AC-DC stage so that it is a DC voltage, hold-up time is a key consideration that is typically taking into account when designing the DC link capacitor of a two-stage converter.

Given that AC-DC converters are almost always connected to the AC grid and thus are powered by the AC grid, there are times when there is no input AC voltage due to temporary disruptions in the grid. In order to ensure the existence of the desired output voltage, even with the temporary lack of input AC voltage, the DC link capacitor should be designed so that it can store enough energy for this to happen. In other words, it is the DC link capacitor that provides power to the DC-DC stage converter, for an amount of time called hold-up time, when the grid voltage is down. As a result, the DC link capacitor should be designed to meet hold-up time requirements. This can be done by satisfying the following relation:

$$C_{DC\_link} \geq \frac{2\,P_o\,T_h}{(V_{bus}^2 - V_{bus,min}^2)} \tag{4-2}$$

Where P_o is the output power, Th is hold up time, V_{bus} is the DC-link voltage and $V_{bus,min}$ is the minimum voltage refers to the level of voltage that a load can sustainably function with for a designated period in the absence of input voltage. If $P_o = 1000$, $T_h = 0.0145$, $V_{bus} = 400$ and $V_{bus,min} = 375$ are substituted into (4-2), then the DC link capacitor should be equal to 1.5 mF.

4.2.3 Main switches S_1 and S_2

Since the soft switching method for the proposed converter is ZCS, the main switches are implemented with IGBTs. The maximum current flowing through the main switches and the maximum voltage across them should be considered as the two major factors when designing the switches. Since the input current is sum of the current though each inductor, the current through the main switches is less than the input current. The maximum current through the switches can be determined by the following equation:

$$i_{s1,max} = i_{s2,max} < i_{in,max} = \frac{\sqrt{2}P_o}{\eta V_{in}} \tag{4-3}$$

The maximum voltage across the main switches is equal to the DC link capacitor voltage, which is specified as being 400V in this example.

When designing the proposed converter, a very important consideration to take into account is that the auxiliary circuit should be designed so that a portion of the energy in the auxiliary circuit of the front-end AC-DC converter is transferred directly to the output using the auxiliary circuit transformer, while ensuring that all the AC-DC converter switches operate with ZCS. Based on the circuit analysis that was performed in the previous chapter, especially the analysis of Modes 3-6, the current through auxiliary circuit inductor, I_{Lr1} should be larger than the maximum input current to divert current away from the main boost converter switches, so that the current through them goes to zero or negative. This allows the switches to be turned off with ZCS. The equation that verifies this condition can be expressed as follows:

$$i_{S1}(t_3) = i_{in} - \left(\frac{(V_{cm}L_e)(1-\cos(\omega_e t_3))}{Z_2 L_{r1}} + \frac{(V_X L_e)\left(t_3 - \frac{\sin(\omega_e t_3)}{\omega_e}\right)}{L_{r1}^2} - \frac{V_X t_3}{L_{r1}} \right) \leq 0 \qquad (4\text{-}4)$$

The peak input current can be determined as follows:

$$i_{in} = \frac{\sqrt{2}\,P_o}{\eta\, V_{in}} = \frac{\sqrt{2} * 1000}{0.95 * 85} = 17.5 \text{ A}$$

Where i_{in} is the peak input current, V_{in} is the minimum RMS input voltage, P_o is the output power, and η is the targeted efficiency of the proposed converter.

4.2.4 Design procedure for the auxiliary power circuit

In this section, key auxiliary circuit components are designed by using graphs of characteristic curves generated for these components using the results of the analysis that was performed in the previous chapter and MATLAB. These graphs help to see the effect of changing a particular component value has on the operation of the converter. Generally, the operating characteristics of the auxiliary circuit at any given value depend on the four key parameters: auxiliary inductor L_{r1} and L_{r2}, auxiliary capacitor C_r, and auxiliary transformer turns ratio. The effect that each of these parameters has on transferred power can be seen with graphs of characteristic curves that have been generated with MATLAB. For these graphs, most of the values of the above-mentioned parameters are fixed, while some are varied.

A. Resonant Capacitor (C_r):

The resonant capacitor is used in the auxiliary circuit to reduce the current through L_{r1} and to apply a negative voltage across L_{r2} to divert the current away from S_1 and S_2 when the main switch is about to be turned off. C_r affects the operation of the circuit in two ways: First, it affects the boost converter's ability to operate with ZCS for all its switches. Second, it affects the amount of power transferred that can be transferred through the auxiliary transformer.

Fig. 4.1, shows the effect of increasing C_r on the amount of power transferred to the output through the auxiliary transformer. This figure shows the output power of the auxiliary transformer versus its turns ratio, for various values of C_r, while the other parameters are fixed. As can be seen from this figure, the larger the value of C_r, the greater the amount of power that can be transferred directly to the output. If C_r is chosen to be less than 8 nf, the switches cannot turn off with ZCS as the current through the main switch cannot go to negative during the turn off transition of the switch. Sufficient time is needed for current from the main switches to flow into the auxiliary circuit so that one of these switches can be turned off with ZCS. If C_r is too small, then current may begin to flow back into the main switches before a ZCS turn-off can occur.

C_r should not be too large, however, as this would increase the peak current stress and slow down the transfer of current away from the auxiliary switch, which would require the auxiliary switch be turned on longer. Increasing the value of C_r also increases the duration of the resonant cycle, which increases RMS current stresses and conduction losses in the auxiliary circuit. This increase may offset some of the savings in losses that can result from direct power transfer. Moreover, if C_r is too large, then the duty-cycle of the converter is limited as time is needed for the auxiliary circuit to go through a resonant cycle and be properly reset, in preparation for the next time it needs to be activated.

Consequently, C_r should be designed so that auxiliary circuit peak and RMS currents are not excessive, the resonant cycle of the auxiliary circuit does not impact the operation of the main power circuits, and a net reduction of losses occurs with direct power transfer. In

order to have an appropriate margin for ZCS, maintain the maximum current through the auxiliary switch, and transfer the maximum power through auxiliary transformer the resonant capacitor, C_r is chosen to be 12 nf.

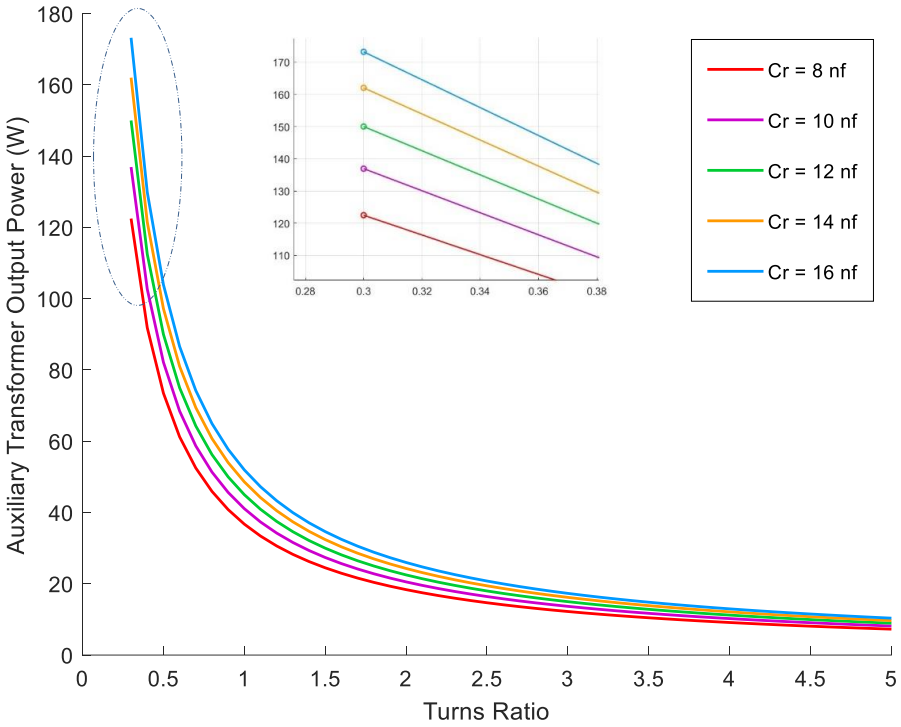


Fig. 4.1. Effect of increasing C_r on the power transferred to the output by the auxiliary transformer

B. Resonant inductors L_{r1} and L_{r2}

The ratio of the resonant inductors L_{r2} / L_{r1}, has two major effects on the circuit: First, it determines the amount of power that can be transferred through the auxiliary transformer. Second, it impacts the amount of time during which the switches can be turned off with ZCS.

Fig. 4.2, shows the effect of increasing L_{r2} / L_{r1} on the amount of power transferred to the output through the auxiliary transformer. This figure shows the output power of the auxiliary transformer versus its turns ratio by increasing the value of the L_{r2} /L_{r1} ratio, while

the other components are fixed. By increasing the ratio of the inductors, the amount of power transferred to the output will decrease. This ratio, however, should be small enough to minimize the time that the auxiliary switch is on, thereby reducing RMS switch current stress and conduction losses.

Fig. 4.3 shows the effect of increasing the L_{r2} / L_{r1} ratio on the ZCS operation for the auxiliary switch. It shows curves of auxiliary switch current versus time, for various ratios of L_{r2} / L_{r1}, with the other parameters fixed. As shown in Fig 4.3, L_{r2} / L_{r1} should be chosen less than 1, otherwise the auxiliary switch will not be able to turn off with ZCS as the current through auxiliary switch will not fall to zero at 1. The ratio of inductors cannot be too small, however, and it should be kept large enough to reduce the auxiliary peak current. As per characteristic curves the ratio is chosen to be 0.95 for the worst-case conditions, which occur when the input AC voltage is 85 V. The maximum power that auxiliary transformer can transfer to the output is 150W, which is 15% of the total power. L_{r2} can be determined as follows:

$$L_{r2} = \left(\frac{V_{cm}}{i_{samax}}\right)^2 . C_r \tag{4-5}$$

$$L_{r2} = \left(\frac{450}{22}\right)^2 . 12\ e-9 \rightarrow\ L_{r2} = 4.9\ \mu H$$

As a result, by having the ratio of L_{r2} /L_{r1} and L_{r2}, the value of the L_{r1} can be chosen to be 5.15 μH

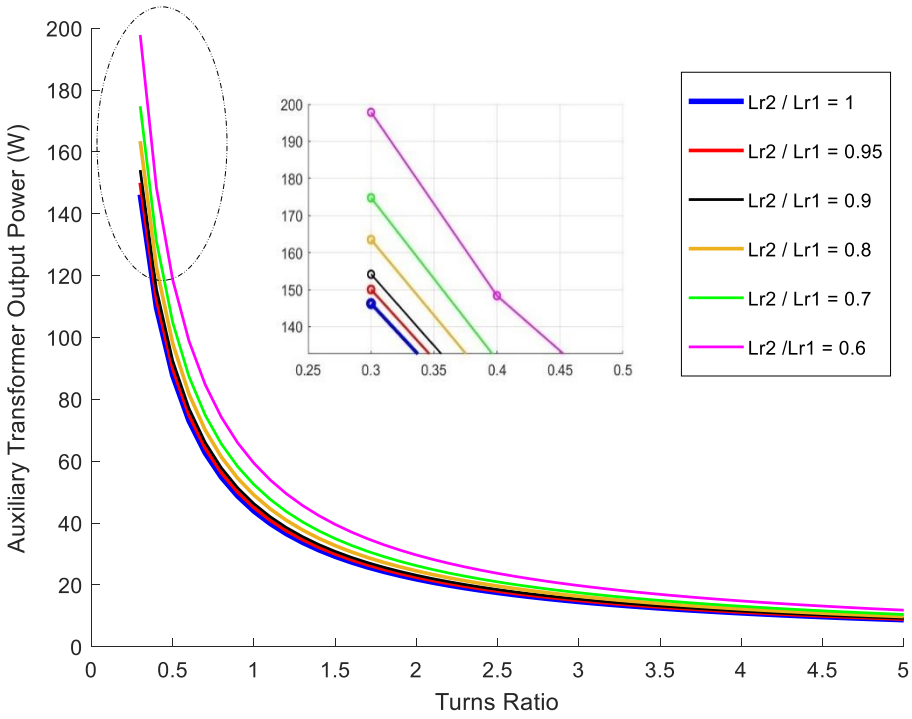


Fig. 4.2. Effect of increasing L_{r1}/ L_{r2} on the transmitted power to the output through the auxiliary transformer

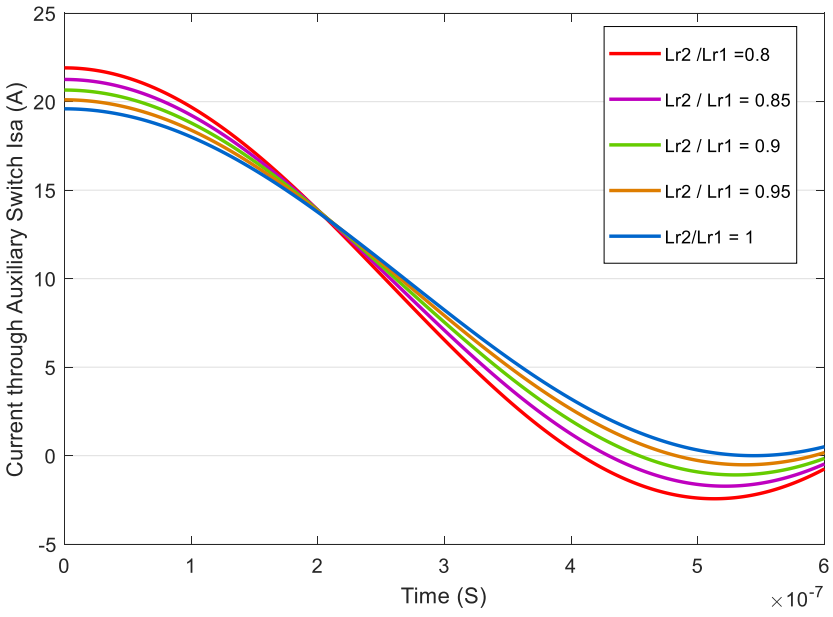


Fig. 4.3. Effect of increasing L_{r2} on the ZCS conditions for the auxiliary switch

C. Turns Ratio (N_x) of the Auxiliary Transformer

The turns ratio of the auxiliary circuit transformer T_x, which is defined as $N_x = N_2/N_1$, affects the amount of power transferred through the auxiliary transformer, the ZCS operation of the converter and the auxiliary circuit component stresses. The primary voltage of the auxiliary transformer, V_x is clamped to $V_x = V_o/ N_x$ when current flows through it. The polarity of this primary voltage depends on the direction of current that flows through it and on which of the secondary diodes of T_x conducts current.

Fig 4.4 shows the amount of power transferred to the output through the auxiliary circuit for various values of turns ratio. As the turn ratio of the transformer decreases, the amount of power transferred to the output increases. If the turns ratio is chosen to be too small, a high voltage is imposed across the primary winding of the transformer, which can cause two major issues: First, this high voltage increases the voltage stress of the switch and the rectifier diodes. Second, the high voltage across the primary counteracts the effect of the voltage across the auxiliary capacitor so that the switches will not operate under ZCS. When $N < 0.3$, the switches will not be able to operate with ZCS. Moreover, if the turn ratio is too small, then the auxiliary transformer needs to be larger in size, as it must handle more power, causing more losses and costs.

On the other hand, as can be seen from Fig 4.4, if N_x is too large, the amount of power transferred to the output will decrease. If $N_x > 5$, the ability of the auxiliary switch to turn off with ZCS is reduced as the current in the switch becomes less likely to fall to zero. Consequently, N_x should be designed at the minimum value that allows all the boost converter switches to operate with ZCS. A value of $N_x = 0.3$ should thus be chosen to maximize the amount of power transferred to the output and meet the ZCS condition for all the switches.

The value of turns ratio determines the amount of power transferred directly to the output. It should be the smallest value that allows the boost converter switches to be turned off with ZCS, while transferring the maximum possible power to the load. A suitable turns ratio can be determined through characteristic curves, as will be shown later in fig. 4.4.

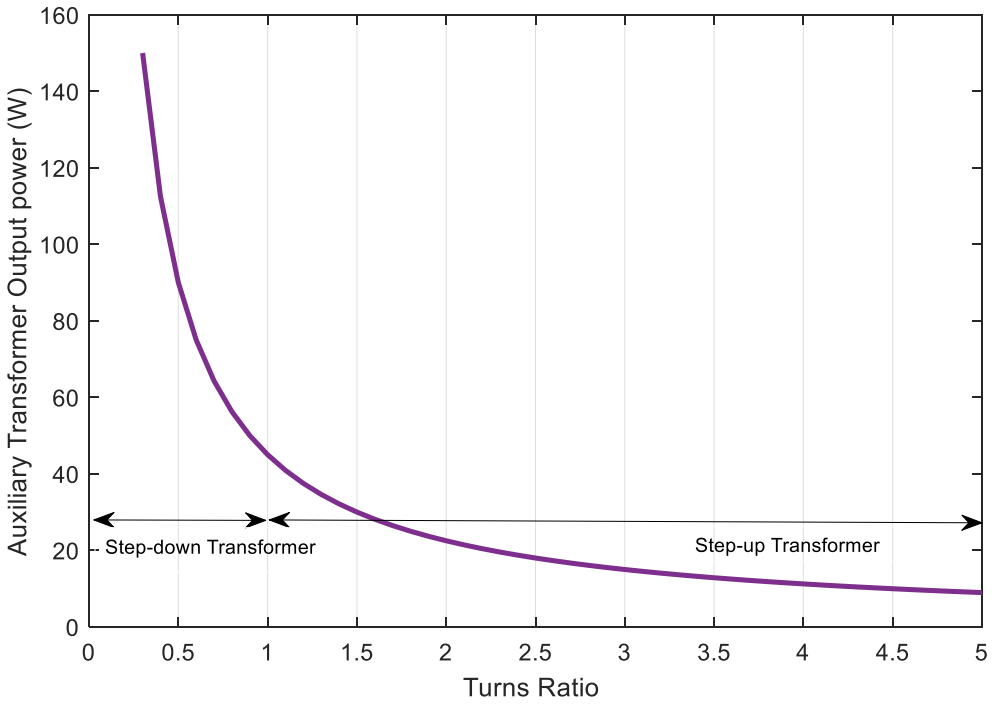


Fig. 4.4. Auxiliary transformer output power vs turns ratio

d. Auxiliary switch S_a

The maximum current through the auxiliary switch should be larger than the input current to satisfy ZCS operation when it is required. Based on the simulation and experimental results, a 25% margin is assumed so that the auxiliary circuit is designed at maximum current 22A.

$$i_{Sa,max} = \frac{V_{cm}}{Z_2} > i_{in,max} \quad (4\text{-}6)$$

$$i_{Sa,max} = \frac{V_{cm}}{Z_2} = 22\ A$$

In order to have less voltage stress on the auxiliary switch, the peak auxiliary switch voltage (V_{cr}) should be designed to be approximately 450 V. This value was chosen by considering the fact that the auxiliary switch is not directly connected across the anode of a boost diode

and ground. It should be noted that this voltage would be much higher if there was no transformer (T_x) to help transfer energy to the output.

C_r is a key parameter that can affect the amount of power transferred to the output and ZCS operation. Since the auxiliary switch is parallel to the auxiliary capacitor, the peak voltage across the auxiliary capacitor is equal to that of the auxiliary switch. The maximum voltage across the auxiliary capacitor is determined as follows:

$$V_{Sa-max} = V_{cm} = \left(V_{Cr_6}(0) + V_X - V_0 \right)(\cos(W_1 t_6)) + \frac{i_{Lr1_6}(0)(\sin(W_1 t_6))}{C_r W_1} - V_X + V_0 \quad (4\text{-}7)$$

4.3 Design procedure for the ZVS – PWM full bridge converter

The output of the AC-DC boost stage is fed to the input of the PWM full-bridge converter. A design procedure of the PWM full bridge converter is presented in this section and demonstrated with a design example. The design considerations and procedure are based on the steady state analysis performed in Chapter 3. It should be noted that the operation of the PWM full-bridge DC-DC converter is independent of that of the first stage converter. The main specifications of the prototype are as follows:

- Input voltage V_{bus} =400 Vdc
- Output voltage V_o =48 Vdc
- Maximum output power P_o =1000 W
- Maximum output current I_o =20.83A
- Switching frequency f_{sw} =50 kHz.

4.3.1 Turns ratio of the high-frequency transformer

There are two considerations that need to be taken into account when designing the transformer: First, the minimum primary current for which the ZVS operation of the switches can be ensured. The primary current that is used to discharge the switch capacitances of the converter switches is dependent on the turns ratio (N = Np/Ns) as this current is based on current that is reflected from the secondary to the primary. Second, the converter's ability to maintain the specified output voltage when the converter is operating

at full load. The turns ratio of the transformer should be designed to be as large as possible to minimize the primary current, yet small enough to ensure that the specified output voltage can be produced.

The transformer turns ratio can be calculated from the equation below:

$$\frac{\mathrm{Vo}}{\mathrm{V_{bus\_min}}} = \frac{\mathrm{Ns}}{\mathrm{Np}} / \delta_{\max} \tag{4-8}$$

where

N_s = number of secondary turns,

N_p = number of primary turns

δ_{max} = maximum effective duty cycle of the voltage appearing at the transformer secondary winding within a switching period.

It is essential to design the transformer turns ratio such that the negative effects of current stress on the switches and voltage stress on the rectifier diode are minimized. The minimum bus voltage should be taken into account when designing the transformer turns ratio to ensure that the desired output voltage can be achieved across the entire voltage range. The maximum duty cycle should be limited to δ_{max} = 0.8 due to the duty cycle loss caused by the resonant inductor. Additionally, assuming a minimum bus voltage of V_{bus_min} = 375 V the transformer turns ratio can be defined as follows:

$$\frac{Ns}{Np} = \frac{Vo}{V\mathrm{bus\_min}} \cdot \frac{1}{\delta_{max}} = \frac{48}{375} \cdot \frac{1}{0.8} = 0.16$$

$$\mathrm{N} = \frac{Np}{Ns} = 6$$

If the turns ratio of the transformer is increased, then the current through the primary winding will decrease, which limit the amount of current that will be available to discharge the output capacitances of the switches before they are turned on so that achieving ZVS operation is more difficult.

4.3.2 Resonant inductor

The value of resonant inductor L_r - which can be the leakage inductance of the transformer or a combination of leakage inductance and some additional, external inductance place in series with the transformer – determines the range of load over which the ZVS operation of the switches is possible. The resonant inductor should be large enough to allow ZVS operation for some minimum load (usually 25% - 35% of maximum load), but too large an inductor results in duty cycle loss at the secondary so that a trade-off of some kind must be considered when choosing a value for L_r.

The value of the resonant inductor can be defined by setting a maximum value of acceptable duty cycle, typically 0.15, and a maximum effective secondary duty cycle to be 0.8 (not 1 - 0.15 – 0.85 as the primary duty cycle cannot be 1 due to issues like dead-time). A value for Lr can be determined as follows:

$$L_r = \frac{N\,V_{bus\_min} D_{loss}}{4Io\ \max fs} = \frac{6\times 375\times 0.15}{4\times 20.86\times 50\times 10^3} = 80\ (\mu H)$$

The slope of the primary current when the converter is transferring from a freewheeling mode of operation to an energy-transfer mode, which is based on the resonant inductor, can be determined to be:

$$\frac{di_p}{\mathrm{dt}} = \frac{V_{bus}}{Lr} \tag{4-9}$$

The equivalent capacitance that is seen by the converter when a switching transition is made from a switch in one converter leg to the switch in the same leg is:

$$C_{eq} = 2C_{oss} + C_{tr} \tag{4-10}$$

Where C_{oss} is the equivalent output capacitance and C_{tr} is the transformer input capacitance.

By considering C_{eq} = 554 pf (determined from switch manufacturer data sheets and transformer measurements) the critical current in which the switches of the full bridge operate with hard switching is

$$I_{critical} = V_{bus}\sqrt{\frac{C_{eq}}{L_r}} = 400\sqrt{\frac{554*10^{-12}}{80*10^{-6}}} = 1.05\ \mathrm{A}$$

If the primary current is greater than the critical current, then the full-bridge converter operates with ZVS. For this example, the converter has been designed so that the converter starts losing full ZVS capability when the load is about 20 % of the full load. Ideally, the converter should be able to operate with ZVS over the entire load range from no load to full load, but this is not practical as this would result in a very high primary current that would increase switch stress and conduction losses. It should be noted that when the converter load does fall below the minimum ZVS load for full ZVS operation, there is still considerable savings in switching losses as the voltage across the switches are reduced, but not made completely zero, before they are turned on, except for very light loads.

4.3.3 Output filter inductor and capacitor

The output filter inductance can be expressed as:

$$L_f = \frac{V_{L\_max}}{I_{o\_ripple}} \cdot t_{on} \quad (4\text{-}11)$$

Where t_{on} is the corresponding on-time and I_{o_ripple} is the output current ripple and V_{L_max} is the maximum voltage across output inductance. V_{L_max} can be determined as follows:

$$V_{L\_max} = \frac{N_s}{N_P} \cdot V_{in\_max} - V_{o\_min} = \left(\frac{425}{6} - 45.6 \right) = 23.3 \text{ V}$$

The output ripple can be determined from the following equation:

$$I_{o\_ripple} = \frac{P_{o\_max} \cdot \Delta I_{Lf}}{V_{o\_min}} = \frac{1000 * 0.2}{45.6} = 4.38 \text{ A}$$

Where ΔI_{Lf} is the peak - to - peak ripple of the output inductor, which is usually about 20%, and P_{o_max} is the maximum output power and V_{o_min} is the minimum output voltage. The on-time duration can be calculated as:

$$t_{on} = \frac{1}{2} \cdot \frac{V_{o\_min}}{V_{in\_max}} \cdot \frac{N_p}{N_s} \cdot Ts = \frac{1}{2} \cdot \frac{45.6}{425} * 6 * 2 * 10^{-5} = 6.4 \text{ µs}$$

The filter inductance can be calculated by substituting t_{on}, I_{o_ripple} and V_{L_max} into the above equation, then rearranging

$$L_{f\_min} = \frac{V_{L\_max}}{I_{o\_ripple}} \cdot ton = \frac{23.3}{4.38} * 6.4 * 10^{-6} = 34.04 \text{ µH}$$

Where $0 < t_{on} / T_s < 0.5$.

The value of the output filter capacitor can be derived by setting the desired value of the peak-to-peak voltage ripple of the output voltage V_{ripple} to be 5%, which is a typical value. This results in $V_{ripple} = 0.05*48 = 2.4$.

the amount of time that output filter inductor needs to vary the 90% of the full current variation can be represented as follows:

$$\Delta t = \frac{P_{out}\,.\,L_{o\_min}}{V_{o\_min}^2} = \frac{1000*34.04*10^{-6}*0.9}{45.6^2} = 14.7\ \mu s$$

ΔV_c is accepted to be 10% of the maximum output ripple then the output capacitor filter is calculated as follows:

$$C_f = \frac{\Delta I}{10\%*\frac{\Delta V_C}{\Delta t}} = \frac{P_{out}\,.\,0.9}{\frac{0.1\,.\,V_{ripple}}{\Delta t}} = \frac{1000*0.9*14.7*10^{-3}}{45.6*0.1*2.4} = 1209\ \mu F$$

4.3.4 Output rectifier diodes

The voltage across each output rectifier diode is equal to the maximum output voltage when it is conducting, which is:

$$V_{DR\_max} = 2\,(V_o + \frac{V_{ripple}}{2}) = 2(48+1.2) = 98.4\ V$$

where V_{ripple} is the amplitude of the peak-to-peak ripple voltage across the output filter capacitor. Diodes are typically rated by average current so that the maximum average current that an output rectifier diode is expected to handle is:

$$I_{DR,avg} = \frac{P_{o,max}}{2Vo} = \frac{1000}{2*480} = 10.41$$

The maximum peak current flowing through the rectifier diodes is:

$$i_{DR\ (max)} = I_{o\_max} + \frac{1}{2}\Delta I_{Lf} = 20.83 + \frac{1}{2} \times 4.1 = 22.88$$

Where i_{DR} (max) is the maximum current flowing through the rectifier diodes.

4.4 Conclusion

In this chapter, a procedure to design the key components of the first-stage AC-DC boost converter and the second-stage DC-DC full bridge converter was presented. The procedure was developed based on the analysis that was performed in the previous chapter and was demonstrated with an example.

For the first converter stage, the AC-DC boost converter, the key considerations were the input inductors as the converter must operate with discontinuous input inductor current, the various switch stresses and the auxiliary circuit components, especially the auxiliary switch and resonant components L_{r1}, L_{r2}, and C_r. The main considerations that needed to be taken into account in the design of the auxiliary circuit components were the ZCS operation of the converter and the amount of power that can be directly transferred to the output.

For the second converter stage, the DC-DC full-bridge converter, the key considerations with the load range over which ZVS operation can occur and the ability of the converter to produce the specified output voltage from the input DC voltage. The key components that were designed were the transformer turns ratio and the resonant inductor. A procedure for the design of the output section of the DC-DC converter was presented as well.

Chapter 5

5 Experimental results

5.1 Introduction

In this chapter, experimental results of the proposed two stage AC - DC converter will be shown to confirm the operation and feasibility of the topology. Prototypes of the AC-DC interleaved boost converter and the PWM full-bridge converter were built. Key voltage and current waveforms are presented in this chapter and the efficiency of the proposed converter is plotted, then compared to a two-stage converter with no direct power transfer from the first stage to the output, and a converter with a front-end stage that operates with hard-switching instead of soft-switching.

5.2 Experimental setup

A prototype of the two-stage AC-DC converter was implemented according to the specifications and component values shown in Table 5.1

It should be noted that IGBT devices are used as the switches for the front-end AC-DC boost converter stage as current-related losses are dominant and IGBTs are more helpful in reducing such losses than MOSFETs. MOSFETs are used in the second DC-DC converter stage as voltage-related losses are dominant and MOSFETs are more helpful in reducing such losses than are IGBTs.

5.3 Experimental waveforms

This section presents waveforms that were obtained from the converter prototype for both the first AC-DC stage and the second DC-DC stage:

5.3.1 AC-DC boost converter waveforms (first stage)

Waveforms for the AC-DC converter are presented here. The waveforms have been split up into input waveforms and switch waveforms.

Table 1: Specification of the converter components

Symbol	Item	Value
V_{in}	Input voltage	85- 265 Volts
V_{out}	Output voltage	48 Volts
$P_{o,max}$	Maximum output power	1000 W
$P_{o,min}$	Minimum output power	200 W
$f_{sw,main}$	Main switches frequency	50 k HZ
f_{saux}	Auxiliary switch frequency	100 k HZ
S_1, S_2	Main switches, IGBT	RGCL60TS60DGC11
Sa	Auxiliary switch	RGCL60TS60DGC11
L_1, L_2	input inductors	120µH
C_{dc_link}	Output capacitor	1000µF
D_1, D_2	Output diodes	RFN20TF6SFHC9-ND
D_{a1}, D_{a2}, D_{a3}	Auxiliary diodes	RFN20TF6SFHC9-ND
D_{x1}, D_{x2}	Output auxiliary diodes	SDURF10P100B
C_r	Auxiliary capacitor	12nf
L_{r1}	Auxiliary inductance	5.15 µH
L_{r2}	Auxiliary inductance	4.9 µH
N_x	Turns ratio of the auxiliary transformer	0.3
Q_1, Q_2, Q_3, Q_4	Main switches, MOSFET	6R190P6
D_{T1}, D_{T2}		APT400060BG
N	The turns ratio of the high-frequency transformer	6:1:1
L_f	Output filter inductor	34.04 µH
C_f	Output filter capacitor	1209 µF

5.3.1.1 Input waveforms

Fig. 5.1 shows typical input voltage and input current waveforms. These waveforms show that the input current of the converter is sinusoidal and in phase with the input voltage. This figure confirms that the proposed converter can operate with power factor correction (PFC) and that the two interleaved boost converter modules can produce a continuous input current in tandem.

Fig. 5.2 shows the current through the input inductors L_1 and L_2. It shows that two boost modules operate with discontinuous current. This type of operation is a must to ensure that the overall input current is sinusoidal and in phase with the input voltage.

Fig. 5.3 shows the rectified current of the converter, which is sum of the two currents through the main inductors, I_{L1} and $I_{L2.}$ It can be seen this current is continuous.

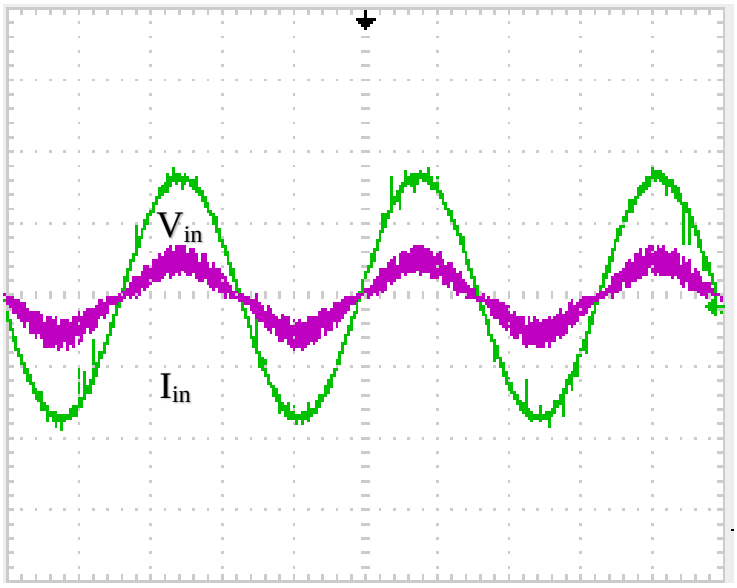


Fig. 5.1. Input current and input voltage (V_{in}: 75 V/div, I_{in} : 15 A/div, t = 5 ms/div)

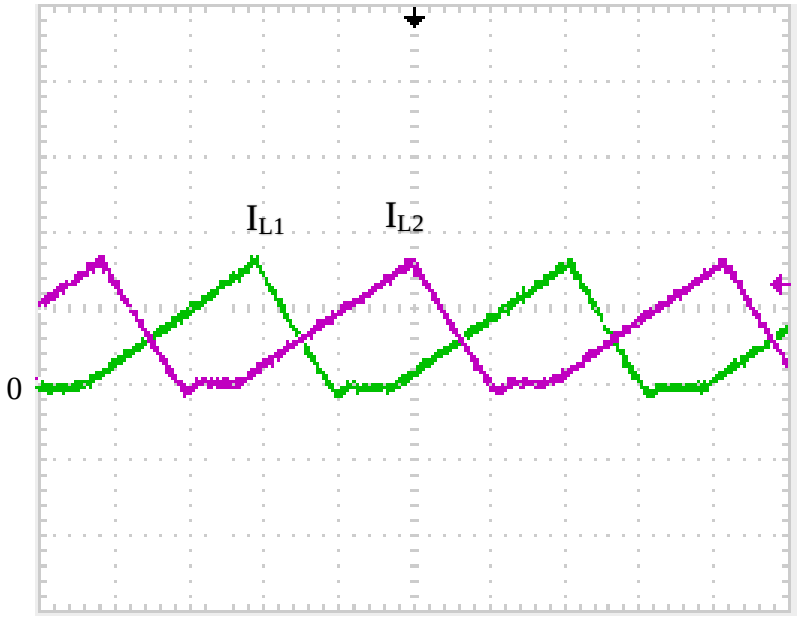


Fig. 5.2. Input inductor currents (I_L: 5 A/div, t = 5 µs/div)

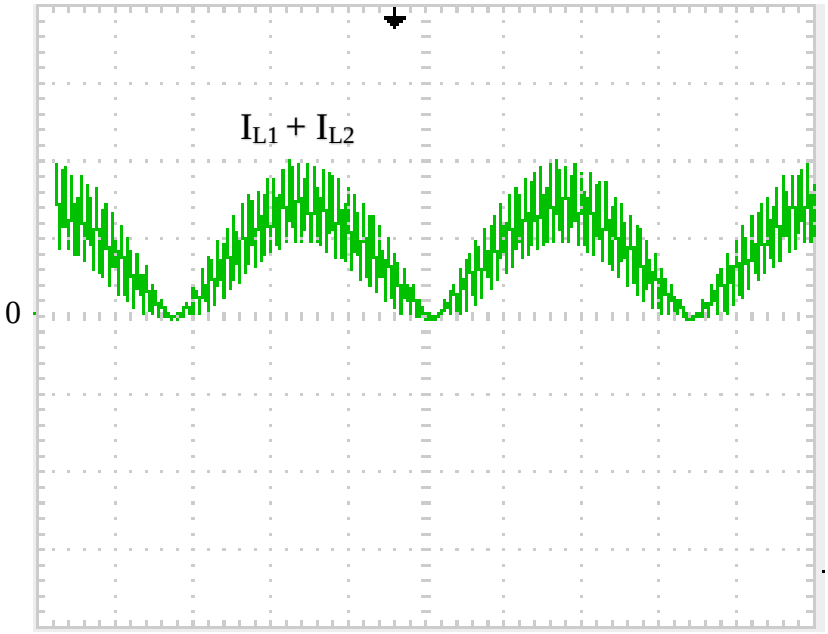


Fig. 5.3. Interleaved current of I_{L1} and I_{L2} (I_L: 5 A/div, t= 5 ms/div)

5.3.1.2 Switch waveforms

Fig. 5.4. shows the gating signals of the main and the auxiliary boost converter switches. It can be seen that the main switches have a 180° phase shift relative to each other. This causes the ripple currents of the input inductors to coincide in a manner that reduces the overall input current ripple, which makes the input current continuous and results in the need for less input filtering.

Fig. 5.5 shows the current and the gating signal of the switching waveforms applied to the main switch S_1. The illustration depicts that switch S_1 can be activated under zero-current switching (ZCS) state. The figure shows that the current passing through the switch drops to zero just before the switch is turned off, thereby preventing power losses caused by the overlap of voltage and current.

Fig. 5.6 shows a typical waveform of current flowing through the auxiliary switch S_{aux} and its gating signal. It can be seen that current goes to zero before the switch is turned off and turned on, which shows that the switch can operate with ZCS.

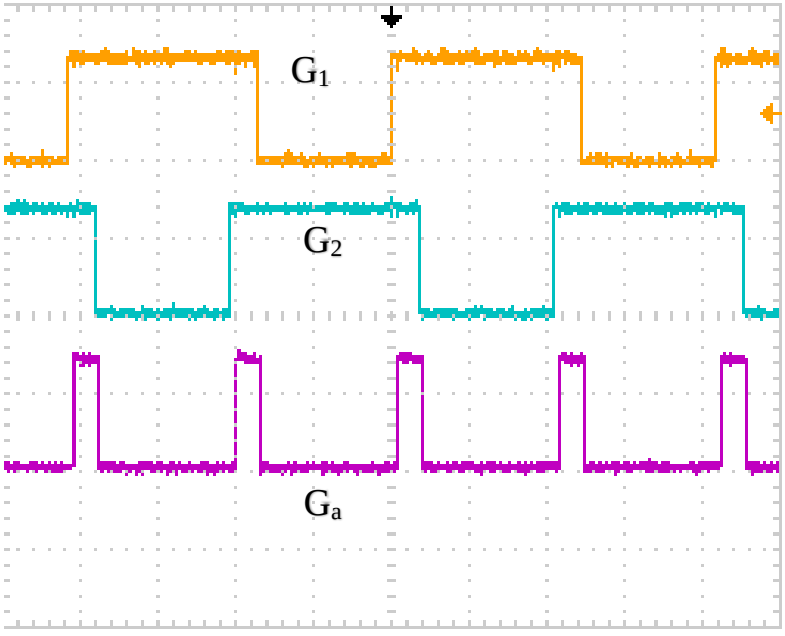


Fig. 5.4. Gating signals of the main and auxiliary switches (V: 20 V/div, t =5 µs/div)

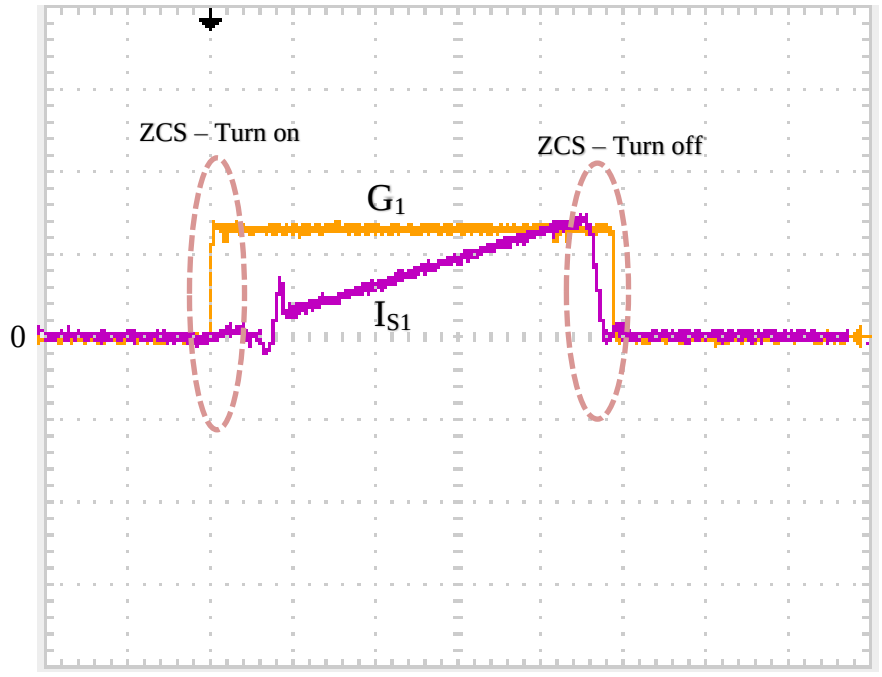


Fig. 5.5. Main switch S_1 gating signal and current waveforms G_1, I_{S1} (I_{S1}: 5 A/div, t= 2.5 µs/div)

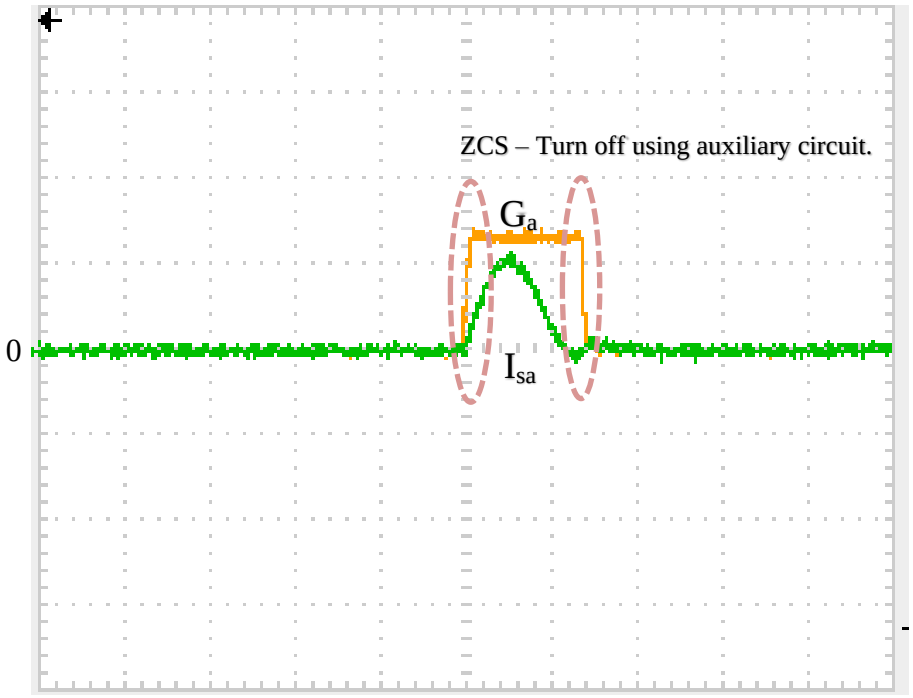


Fig. 5.6. Auxiliary switch gating signal and current waveforms G_a, I_{sa} (I_{Sa}: 10 A/div, t= 1 µs/div)

5.3.2 DC-DC full-bridge converter waveforms (second stage)

Fig. 5.8 shows typical gating signals for the MOSFET switches Q_1, Q_2, Q_3, and Q_4 for the DC-DC full-bridge converter. It can be seen that switches Q_1 and Q_2 have complementary gating signals with respect to each other, that Q_3 and Q_4 have complementary gating signals with respect to each other, and that the Q_3-Q_4 gating signals are the same as the Q_1-Q_2 signals but shifted. It should be noted that that are small gaps in time when neither Q_1 nor Q_2 are on and small gaps in time when neither Q_3 nor Q_4 is on. These small-time gaps are dead times when neither of the switches of the two switches of a converter leg are on, to provide opportunity to discharge the output switch capacitance of the switch that is about to be turned on so that it can be turned on with ZVS.

Fig. 5.9 shows typical transformer primary voltage and current waveforms. It can be seen that the primary voltage is a square waveform with positive and negative voltage and with zero-voltage states. The converter has zero-voltage states when either its two top switches or its two bottom switches conduct current. It has non-zero states whenever a pair of diagonally opposed switches are on. The current through the transformer's primary winding corresponds to the voltage across it. Whenever there is voltage across the transformer's primary winding, the primary current rises; whenever there is no voltage across the transformer, it falls.

Fig. 5.10 shows the voltage and current waveforms of switch Q_1 when it is in the process of being turned on. It can be seen that current begins to flow through the switch after the switch voltage has been forced to zero by the natural operation of the converter. Turn-on losses are therefore minimized with this ZVS operation. Fig. 5.12 shows the same waveforms, but when the switch is in the process of being turned off. It can be seen that there is no overlap of voltage and current during this switching transition as voltage does not begin to rise significantly until the switch current falls to zero. As a result, the switch has a ZVS turn-off.

Fig. 5.11 shows the experimental waveforms of the voltage and the gating signal of the switch Q_1 at falling edge. During switching transition, the voltage across the switch falls to zero before the switch is turned off.

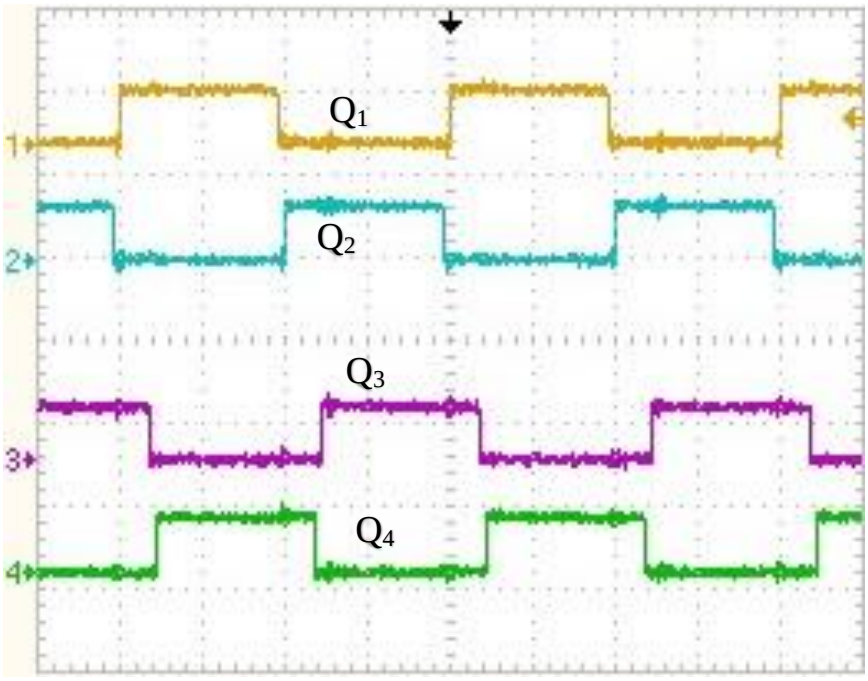


Fig. 5.7. Gate signals for switches Q_1, Q_2, Q_3, and Q_4 (V_{bus} : 20V/div, t = 5 µs/div)

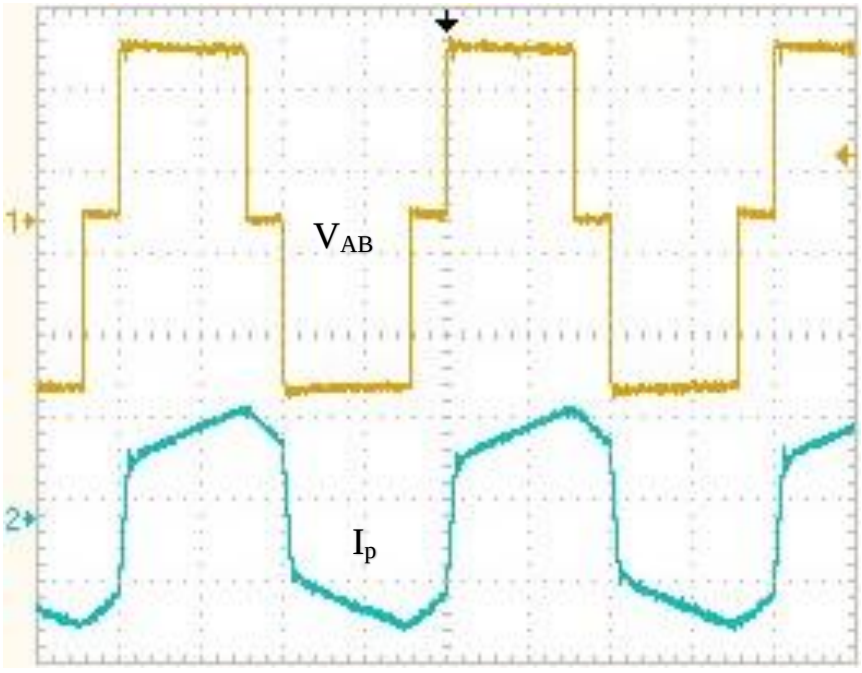


Fig. 5.8. Transformer primary current and voltage waveforms of the DC-DC full-bridge converter (V_{AB} : 200V/div, Ip : 2 A/div, t = 5 µs/div)

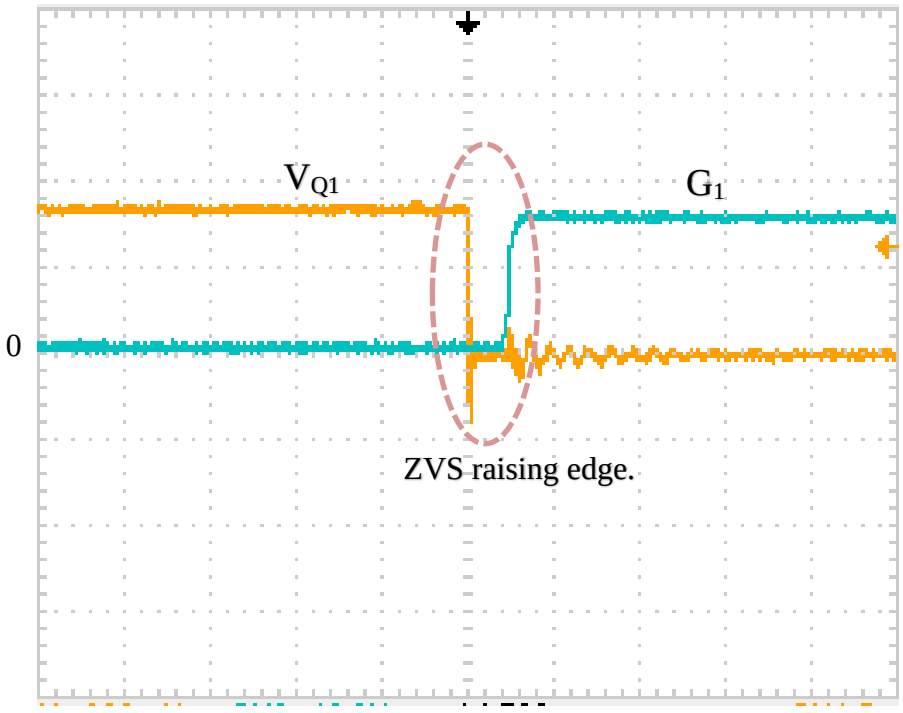


Fig. 5.9. Voltage and the gating signal of the switch Q_1 at rising edge (V_{bus} : 20V/div, t = 5 µs/div)

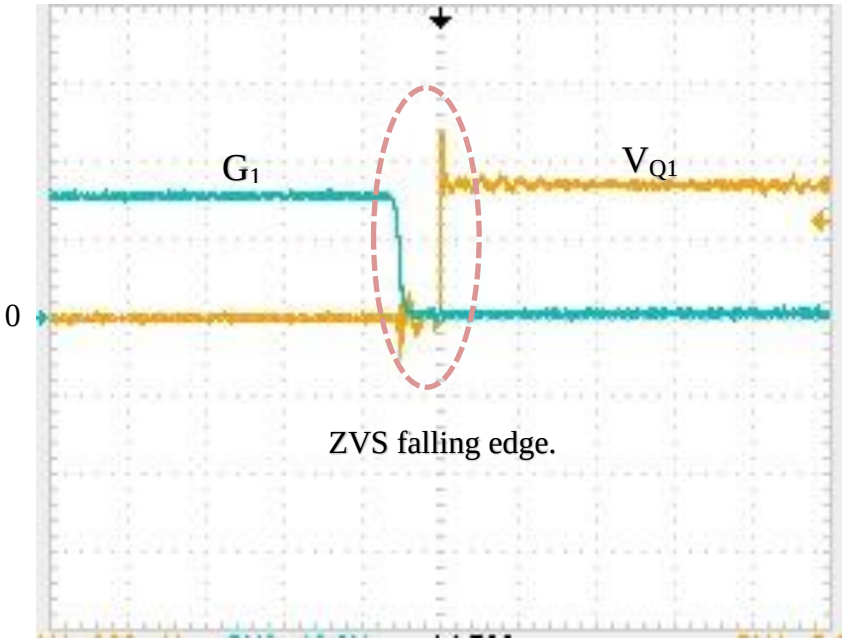


Fig. 5.10. Voltage and the gating signal of the switch Q_1 at falling edge (V_{bus} : 20V/div, t = 5 µs/div)

5.4 Converter efficiency

Fig. 5.11 shows a graph of efficiency curves for three converters obtained from experimental prototype:

- The proposed converter with direct power transfer from the input stage to the output stage.
- A two-stage AC-DC converter that is implemented with a front-end stage that has the secondary of the auxiliary circuit transformer connected to the DC link capacitor. This converter has no direct power transfer.
- A two-stage converter that has an AC-DC front-end boost stage with no auxiliary circuit to help its main power switches turn off with ZCS. In other words, the AC-DC boost converter operates with hard-switching instead of with of-switching.

The maximum output power for all three converters is 1 kW, the load range is from 20% to 100% of full load, the input voltage is set to 120 V_{rms} and the output DC voltage is 48 V.

It can be seen that the two converters that have an auxiliary circuit in their front-end AC-DC boost converters have considerably higher efficiency than the hard-switching converter, especially at heavy loads. When the load is increased, there is more current flowing in the converter and the overlap between voltage and current becomes greater in the hard-switching converter so that more switching losses are created and thus less efficiency. With the soft-switching converters, this overlap is essentially eliminated with soft-switching so that converter efficiency does not drop at heavy loads.

It can also be seen that the two converters have similar efficiency at heavy loads, about 92.4%. The converter with direct power transfer has significantly better efficiency at lighter loads, with a difference of about 2% when the load is 200 W. This improvement is significant, especially when it is considered how slight the proposed auxiliary circuit modification is to achieve DPT. The main reasons for this efficiency characteristic are as follows: The power that is directly transferred from the first stage to the output in the direct

power transfer converter is fairly fixed through the entire load range, with some small variation. Since the secondary of the auxiliary circuit transformer is connected to the output DC voltage, which is much lower than the DC link voltage, the converter will have more auxiliary circuit transformer secondary diodes losses than it would if these diodes were connected to the DC link capacitor. As a result, for heavy loads, there is not much difference in the relative amount of net power that is processed by the auxiliary circuit transformer compared to the power that is processed by the DC-DC full-bridge converter.

When the converter is operating with lighter loads, a more significant percentage of the power is directly transferred to the output when the auxiliary circuit secondary diodes are connected to the output. Given that this power is processed by only one converter instead of being processed by both converters, the proposed converter can thus operate with higher efficiency at lighter loads. It should be noted that an approximate gain of about 2% in efficiency can be achieved simply by reducing the number of turns in the auxiliary circuit transformer and by connecting the secondary diodes to the output instead of the DC link capacitor. There is no need for additional components.

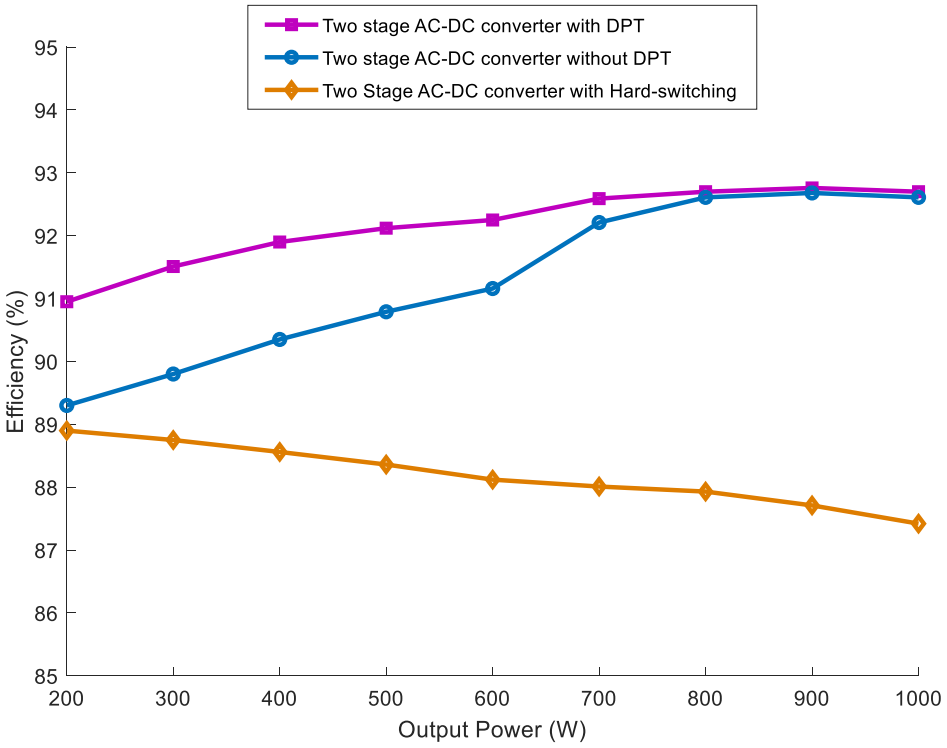


Fig. 5.11. Efficiency of the proposed converter vs load power.

Chapter 6

6 Conclusion

6.1 Summary

AC-DC converters are typically implemented with two converter stages. The first stage is usually an AC-DC boost converter that is made to operate with input power factor correction (PFC), to shape the input current so that it is sinusoidal and in phase with the input AC voltage. The second stage is an isolated DC-DC converter that takes the DC output of the first stage and converts it to a desired output DC voltage that is isolated from the rest of the converter. This second stage can be some sort of flyback or forward converter for low power applications, or some sort of full-bridge converter for higher power applications. In this thesis, a standard zero-voltage switching (ZVS) pulse-width modulated (PWM) converter was used as the second DC-DC converter as it is the most popular higher power DC-DC converter.

The ZVS-PWM full-bridge converter has inherent soft-switching, but the first-stage boost converter does not. The first-stage converter can be implemented with some sort of soft-switching method, either zero-voltage switching (ZVS) or zero-current switching (ZCS). This reduces power losses that are caused by the overlap of voltage and current during switching transitions, when active power converter devices (switches) are in the process of being turned on or off. ZVS methods are preferred for converters with MOSFET switching devices as they have significant output capacitances; ZCS methods are preferred for converters with IGBT switching devices due to their current tail, which appears when these devices are in the process of turning off. Since these power losses are related to the product of voltage and current during switching transitions, making either the voltage or the current zero reduces switching power losses and thus improves converter efficiency.

Numerous ZVS techniques and ZCS techniques have been proposed for boost converters. Many of these methods are implemented by using an active auxiliary circuit that helps the

main converter switches operate with ZVS or ZCS. This active auxiliary circuit typically consists of an active switching device and some passive components such as diodes, capacitors, inductors, and, in some cases, transformers. It is activated just before a switch is about to be turned on for ZVS-PWM boost converters and activated just before a switch is to be turned off for ZCS-PWM boost converters.

Regardless of whether ZVS or ZCS methods are used, the auxiliary switch in the auxiliary circuit is a device with better switching characteristics than those of the main switch. As a result, whatever switching losses may be caused by the auxiliary switch (in some cases, this switch may operate with some form of soft switching itself) are offset by the main switch switching losses that are saved. The auxiliary circuit is active for only a small fraction of a switching cycle so that its current ratings are much smaller than those of the main converter components. This allows the auxiliary circuit to be implemented with devices that are smaller and less expensive than those in the main power converter circuit.

ZVS and ZCS boost converters with active auxiliary circuit that contain small transformers have been proposed in the literature. For this thesis, a ZCS boost converter was used for the first converter stage because of the relatively high current that flow through the main switches and IGBTs were considered to be more devices for the main switches. With an IGBT implementation, ZCS methods were considered, as explained above. The particular topology that was used has the advantage that it can be implemented with interleaved boost converter modules, which reduces the size and weight of the input inductance, and only a single active auxiliary circuit is needed to help the two main switches turn off with ZCS.

The main focus of this thesis has been an investigation of a two-stage AC-DC converter where some of the input power can be transferred directly to the output through the auxiliary circuit transformer of the first stage, instead of being processed by two power stages. With this direct power transfer (DPT), this power is processed only once instead of twice so that converter losses can be reduced. In this thesis, after a literature review in Chapter 1, the basic operating principles of the converter were explained in Chapter 2, a steady-state analysis of the converter’s operation was performed in Chapter 3, the results

of this analysis were used to develop a design procedure that was demonstrated with an example in Chapter 4, and experimental results were presented in Chapter 5.

6.2 Conclusions

The following conclusions can be made based on the work that has been done for this thesis:

- The efficiency of a two-stage converter AC-DC with a first-stage AC-DC boost converter that has a transformer in the auxiliary circuit that allows its switches to operate with soft-switching can be improved if the secondary of this transformer is connected directly to the output. This is especially true if the converter is operating under light-load conditions where the percentage of power that is transferred directly to the output relative to the total input power is increased.
- The critical parameters that determine the operation of the auxiliary circuit of the first AC-DC converter stage are the resonant elements L_{r1}, L_{r2}, and C_r and the auxiliary circuit transformer turns ratio N_x, as determined by analysis. It is these elements that determine the first-stage converter's ability to operate with ZCS and the amount of power that can be transferred to the output through the auxiliary circuit.
- A condition for ZCS operation in the front-end converter is that the ratio of L_{r1} to L_{r2} must be greater than one. If this condition is not met, then current cannot be diverted away from the main power switches under all load conditions, when the auxiliary switch is turned on, so that they will not turn off with ZCS.
- The values of L_{r1} and L_{r2} affect the amount of power that can be delivered to the load. As these values are increased, less power can be delivered to the load.
- The resonant capacitor C_r affects the amount of power that can be delivered directly to the output. If the value of C_r is increased, then more power can be delivered and vice versa.

- The auxiliary transformer turns ratio N_x affects the operation of the converter in the following manner: As N_x is increased, the load range over which the front-end converter operates with ZCS is increased. This is because increasing N_x increases the primary current of the auxiliary transformer and decreases the clamping voltage. Increasing N_x also decreases the amount of power that is transferred to the output. This is because more conduction losses will be generated as a result of more circulating current in the auxiliary circuit.

6.3 Contributions

The contributions of this thesis are as follows:

- A way to improve the efficiency of a two-stage AC-DC converter was proposed. Efficiency can be improved if the front-end AC-DC boost converter of the two-stage converter is implemented with an active auxiliary circuit that has a transformer in its circuit. This type of circuit ensures that the converter switches operate with some sort of soft-switching, and it allows some of the input power to be transferred directly to the output. This direct power transfer allows some power to be processed by just one stage, instead of two stages, which reduces the amount of power lost in the second stage, thus increasing converter efficiency, especially at lighter loads. An improvement of approximately 2% was determined for an inpt voltage of 120 Vrms and a load of 200 W.
- The steady-state characteristics of the proposed converter were analyzed. The effect of varying individual components on the operation of the converter was determined, which allowed insight into the operation of the converter to be gained.
- A procedure for the design of the converter was derived, based on the steady-state analysis of the converter. This procedure allows circuit designers to design key circuit components and parameters, especially the soft-switching operation of the converter and the distribution of the input power. The design procedure was demonstrated with an example.

- The feasibility of the proposed converter with the direct power transfer mechanism was confirmed with results obtained from an experimental prototype. It was shown that the proposed converter's direct power transfer mechanism improved the efficiency of a two-stage AC-DC converter, especially at lighter loads where the improvement was significant.

6.4 Future Work

The following are suggested for future work:

- The front-end AC-DC boost converter stage was implemented with a particular soft-switching AC-DC boost converter with an auxiliary circuit that had a transformer in its circuit. Future work can be done to see how the proposed direct power transfer approach can work on other soft-switching AC-DC boost converter topologies that also have a transformer in its auxiliary circuit.
- The second DC-DC stage of the two-stage AC-DC converter was implemented with a conventional zero-voltage switching PWM full-bridge converter. Future work can be done to determine how the proposed direct power transfer approach can work with other DC-DC converters such as lower power flyback and forward converters, especially since the results in this thesis indicate significant efficiency improvement with lighter-load operation.

References

[1] N. Mohan, "Power Electronics: Converters, Applications, and Design," 3rd edition, NJ: John Wiley & Sons, Inc., 2003.

[2] Y. Rozanov, S. E. Ryvkin, E. Chaplygin, and P. Vorobev, "Power Electronics Basics: Operating Principles, Design, Formulas, and Applications, 1st edition, 2015.

[3] R. Erickson, “Fundamentals of Power Electronics, “Kluwer Press, 2nd edition, 2001.

[4] M. Ahmadi, E. Galvan, E. Adib, and H. Farzanehfard; “New fully soft switched bidirectional converter for Hybrid Electric Vehicles: Analysis and control,” IEEE IECON 2010, pp.2340-2345, 7-10 Nov. 2010.

[5] H. Bodur, A.F. Bakan; “A new ZVT-PWM Dc-Dc converter,” IEEE Trans. on Power Electronics, vol.17, no.1, pp.40-47, Jan 2002.

[6] H. Bahrami, E. Adib, S. Farhangi, H. Iman-Eini, and R. Golmohammadi, “ZCS-PWM interleaved boost converter using resonance-clamp auxiliary circuit,” in IET Power Electronics, vol. 10, no. 3, pp. 405–412, 2017.

[7] Q. Luo, H. Yan, S. Chen, and L. Zhou, “Interleaved high step-up zerovoltage-switching boost converter with variable inductor control,” in IET Power Electronics, vol. 7, no. 12, pp. 3083–3089, 2014.

[8] M. Rezvanyvardom, M. Mohammadi, H. Farzanehfard, and E. Adib, “Analysis, design and implementation of zero-current transition interleaved boost converter,” IET Power Electron., vol. 5, no. 9, pp. 1804-1812, November 2012.

[9] H. Bahrami, E. Adib, S. Farhangi, H. Eini, and R. Golmohammadi, “ZCS PWM interleaved boost converter using resonance-clamp auxiliary circuit,” IET Power Electron., vol. 10, no. 3, pp. 405_412, 2017.

[10] H. Bahrami, E. Adib, S. Farhangi, H. eini, and R. Golmohammadi, “ZCS-PWM interleaved boost converter using resonance-clamp auxiliary circuit,” IET Power Electron., vol. 10, no. 3, pp. 405–412, 2017.

[11] C. A. Canesin and I. Barbi, “Novel zero-current-switching PWM converters,” IEEE Trans. Ind. Electron., vol. 44, pp. 372–381, June 1997.

[12] Takagi, H. and Kano, G., "Complementary JFET Negative-Resistance Devices," in IEEE Journal of Solid-State Circuits, vol. SC-10, no. 6, pp. 371-375, Dec. 1975.

[13] L. Huber, J. Zhang, M. M. Jovanovic, and F. C. Lee, “Generalized topologies of single-stage input-current-shaping circuits,” IEEE Trans. on Power Electron., vol. 16, no. 4, pp. 508–513, Jul. 2001.

[14] S.Mao, J.Popovic, J.A. Ferreira,” Efficiency Impacts of 1.2kV Silicon Carbide MOSFETs for Isolated Two-stage AC-DC Power Conversion ”, 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia,May 2018.

[15] J. –E. Park, J. –W. Kim, B. –H. Lee, and G. –W. Moon, “Design on topologies for high efficiency two-stage ac dc converter”, in International Power Electronic and Motion Control Conference (IPEMC),2012, pp. 257-262.).

[16] W.Lin, H.Chen, Y.Fang, “A Single-stage PFC by Integrating quasi-Bridgeless Boost and LLC Converter”, 2018 IEEE International Telecommunications Energy Conference (INTELEC), January 2019.

[17] D.Wijerante, G.Moschopoulos, “ A Three-Phase Single-Stage AC-DC Full Bridge Converter with High Power Factor”, 2009 IEEE Energy Conversion Congress and Exposition, November 2009.

[18] D. D. C. Lu, D. K. W. Cheng, and Y. S. Lee, “Single-stage AC-DC power-factor corrected voltage regulator with reduced intermediate bus voltage stress”, Electric Power Applications, IEE Proceedings, vol. 150, no. 5, pp. 506-514, 2003.

[19] B. Bryant; M.K. Kazimierczuk, “Open-loop power-stage transfer functions relevant to current-mode control of boost PWM converter operating in CCM”, IEEE Transactions on Circuits and Systems, Vol. 15, no. 10, pp. 2158 – 2164, October 2005.

[20] B. C. Barry, J. G. Hayes, M. S. Ryłko and J. W. Masłoń, "Discontinuous Conduction Mode Operation of the Two-phase Integrated-magnetic Boost Converter," IEEE Energy Conversion Congress and Exposition (ECCE), pp. 5782-5789, 2014.

[21] D. Wang, Y. Deng, X. He, and F. Cao, “Designing and analysis of an interleaved boost converter with passive lossless clamp circuits,” in 2008 34th Annual Conference of IEEE Industrial Electronics, Nov. 2008, pp. 2149–2155.

[22] Yao-Ching Hsieh, Te-Chin Hsueh, Hau-Chen Yen, “An interleaved boost converter with zero-voltage transition”, IEEE Transactions on Power Electronics, April. 2009, Vol. 24, No. 4, pp. 973-978.

[23] Ritu, S. Mishra, N. Verma and S. D. Shukla, “Implementation of solar based PWM fed two phase interleaved boost converter”, International Conference on Communication, Control and Intelligent System (CCIS), pp. 470-476, Mathura, India, November 2015.

[24] M. Bhuvaneswari, R.Suresh Kumar, “A High Efficiency Power Factor Correction Using Interleaved Boost Converter With Fuzzy Logic Control,” International Journal of Engineering Science and Technology, vol. 5, no. 06S, Jun 2013..

[25] D.Sankar, C.A. Babu, “Comparative analysis of a resonant soft switching interleaved topology and single switch topology of a boost converter for a PV system, 2014 Annual International Conference on Emerging Research Areas: Magnetics, Machines and Drives (AICERA/iCMMD), July 2014.

[26] R. Rasoulinezhad, A. Abosnina, J. Khodabakhshand, G. Moschopoulos, “An AC-DC interleaved ZCS-PWM boost converter with reduced auxiliary switch RMS current stress,” IEEE Access, vol. 9, pp. 41320-41333, March 2021.

[27] Yang, B., Duarte, J. L., Li, W., Yin, K., He, X., & Deng, Y. Phase-shifted full bridge converter featuring over the full load range. In Proc. 36th Annual Conference of the IEEE Industrial Electronics Society, (2010).

[28] J. Dudrik, M. Bodor, and M. Pastor, “Soft-switching full-bridge PWM DC-DC converter with controlled output rectifier and secondary energy recovery turn-off snubber,” IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4116–4125, 2014.

[29] J. H. Kim, I. O. Lee, and G. W. Moon, “Integrated Dual Full-Bridge Converter with Current-Doubler Rectifier for EV Charger,” IEEE Trans. Power Electron., vol. 31, no. 2, pp. 942–951, 2016.’

[30] A. Mousavi, P. Das, and G. Moschopoulos, “A Comparative study of a new ZCS DC – DC full-bridge boost converter with a ZVS active-clamp converter,” IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1347–1358, 2012.

[31] A. Averberg and A. Mertens, “Analysis of a voltage-fed full bridge DC-DC converter in fuel cell systems,” in IEEE PESC, 2007, pp. 286–292.

[32] V. Vaisanen, T. Riipinen, and P. Silventounen, “Effects of switching asymmetry on an isolated full-bridge boost converter,” IEEE Trans. Power Electron., vol. 25, no. 8, pp. 2033–2044, 2010.

[33] K.Rustom, W.Wu, W. Qiu, and I. Batarseh, “Asymmetric Half Bridge Soft-Switching PFC Converter with Direct Energy Transfer”, 33rd Annual IEEE Power Electronics Specialists Conference, Vol.4, June 2002.

[34] J.R.R Zientarski, M.L.S. Martins, J.R. Pinheiro, and H.L. Hey, "Evaluation of Power Processing in Series-connected Partial-power Converters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 1, pp. 343-352, 2019.

[35] M. Agamy, M. Harfman-Todorovic, A. Elasser, S. Chi, R. Steigerwald, J. Sabate, A. McCann, L. Zhang, and F. Mueller, “An efficient partial power processing dc/dc converter for distributed pv architectures,” IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 674–686, Feb 2014.

[36] K. A. Kim, P. S. Shenoy, and P. T. Krein, “Converter rating analysis for photovoltaic differential power processing systems,” IEEE Transactions on Power Electronics, vol. 30, no. 4, pp. 1987–1997, April 2015.

[37] M. Zarei, B. Poorali, S. Erean, and M.Pahlevani,” New DC–DC Converter With Direct Power Transfer Capability”, IEEE Transaction on Power Electronics, Vol.36, no.5, May 2021.

[38] H.Wu, L.Zhu, F. Yang, “Three-Port-Converter-Based Single-Phase Bidirectional AC-DC Converter with Reduced Power Processing Stages and Improved Overall Efficiency”, IEEE Transactions on Power Electronics, Vol.33, no.12, PP.10021-10026, April 2018.

[39] Y. T. Yau, K. I. Hwu, and W. Z. Jiang, "Two-Phase Interleaved Boost Converter with ZVT Turn-On for Main Switches and ZCS Turn-Off for Auxiliary Switches Based on One Resonant Loop," IEEE Transactions on Power Electronics, vol. 35, no. 5, pp. 4893-4905, May 2020

[40] C. M. de Oliveira Stein, J. R. Pinheiro, and H. L. Hey, “A ZCT auxiliary commutation circuit for interleaved boost converters operating in critical conduction mode,” IEEE Trans. Power Electron., vol. 17, no. 6, pp. 954– 962, Nov. 2002.

[41] M. Rezvanyvardom, E. Adib, H. Farzanehfard and M. Mohammadi, "Analysis, design and implementation of zero-current transition interleaved boost converter," in IET Power Electronics, vol. 5, no. 9, pp. 1804-1812, November 2012.

[42] A.L.P Kumar, V.V. Subrahmanya Kumar Bhajana, P.Drabek, “A Novel ZCS Interleaved Bidirectional Buck-Boost DC-DC Converter for Energy Storage Applications”, 2016 ELEKTRO conference, July 2016.

[43] S.Ikeda, F.Kurokawa, “Boost Full Bridge DC-DC Converter Ensuring Safe Installation of PV Energy in Data Center Power Management Systems”, 2017 IEEE International Telecommunications Energy Conference (INTELEC), October 2017.

[44] D.B. Dalal, “A 500 KHZ multi-output Converter with Zero Voltage Switching”, Fifth Annual Proceedings on Applied Power Electronics Conference and Exposition, 1990.

[45] T. Etoh; T. Ahmed; E. Hiraki; K. Morimoto; N.A. Ahmed; Ki-Young Suh; Hyun Woo Lee; M. Nakaoka, “New auxiliary active lossless snubber-assisted full bridge soft switching PWM high frequency inverter-fed DC-DC power converter”, 2005 International Conference on Electrical Machines and Systems, Vol.2, PP. 1090-1094, 2005.

Curriculum Vitae

Name: Mina Fakhri

Post-secondary Education and Degrees:
University of Western Ontario
London, Ontario, Canada
2021-2023 M.E.Sc.

Kerman Graduate University of Technology
Kerman, Iran
2016-2019 M.E.Sc.

Honors and Awards:
Ministry of Science Graduate Excellence Scholarship
Kerman, Iran
2016-2018

Related Work Experience
University Lecturer
Apadana Institute of Higher Education
2019-2021

Teaching Assistant
The of Western Ontario
2021-2023

Publications:

[1] Mina Fakhri, Adel Abosnins, Gerry Moschopolous, “Novel Two-Stage AC-DC Power Converter with Partial Single-Stage Power Processing”, 14th international conference on PEDS, Canada, 2023.

[2] Mina Fakhri, Roohollah Fadaeinedjad, Hojatollah Moradi, Ebrahim Mohammadi,"Variable speed wind turbine control based on stall using switch mode rectifier converter", accepted for presentation in the 8th Annual Conference of the Smart Energy Network, Kordestan, Iran, November 2018.

[3] Houman Jamshidi, Amin Reze Jamshidi, Mina Fakhri," A review on energy management strategies at smart hospitals", 10th international conference on engineering and humanities, France, 2019.