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Synthesis and Transport Properties of Topological Crystalline Insulator SnTe Nanowires

Pengzi Liu
Yale University Graduate School of Arts and Sciences, liupengzi@gmail.com

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Abstract

Synthesis and Transport Properties of Topological Crystalline Insulator

SnTe Nanowires

Pengzi Liu

2022

Over the last decade, significant progress has been made in studying topological materials whose wavefunctions possess a distinct topological invariant signature barring adiabatic deformation from a trivial phase to a non-trivial phase. There has been mounting experimental evidence for the presence of topological nature in nanomaterials due to their favorable surface-to-volume ratio and phase-coherent confinement. Considering that the material synthesis and transport measurement challenges must be overcome before topological nanomaterials can be used in next-generation electronic devices, in my dissertation, I focus on improving crystal quality and controlling dimensions of topological crystalline insulator SnTe in nanoscale as it provides a rich playground to examine interactions of correlated electronic states, such as ferroelectricity, topological surface states, and superconductivity. To develop facile strategies to suppress surface defects during chemical vapor deposition growth of SnTe nanostructures, we systematically investigate the origin and evolution of three-dimensional surface defects commonly observed on SnTe microcrystals and nanostructures. By employing alloy nanoparticles as growth catalyst, SnTe nanowires are synthesized with reduced diameters and high crystalline quality, such that one-dimensional

confinement and phase coherence of the topological surface electrons can be ensured to probe the topological surface states. To further alleviate the high carrier density inside the bulk of SnTe nanowires and surface degradation, surface passivation of SnTe nanowires using *in situ* Te deposition during growth process is investigated. The material improvement approach in this dissertation aims to facilitate future research on understanding the extent of scattering of topological surface states due to crystalline defects, impurities, and coupling to bulk electron states.

Synthesis and Transport Properties of Topological Crystalline Insulator

SnTe Nanowires

A Dissertation

Presented to the Faculty of the Graduate School

of

Yale University

in Candidacy for the Degree of

Doctor of Philosophy

by

Pengzi Liu

Dissertation Director: Judy J. Cha

May 2022

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List of Abbreviations

Abbreviation	Meaning	Abbreviation	Meaning
1D	One-dimensional	MBS	Majorana bound state
2D	Two-dimensional	MEMS	Micro-electro-mechanical system
3D	Three-dimensional	MMA	Methyl methacrylate
ABO	Aharonov-Bohm oscillation	MR	Magnetoresistance
ADF	Annular dark field	n	Carrier density
ARPES	Angle-resolved photoemission spectroscopy	PDMS	Polydimethylsiloxane
B	Magnetic field	PMMA	Polymethyl methacrylate
BF	Bright field	QSHE	Quantum spin Hall effect
BN	Boron Nitride	qubits	Quantum bits
Cryo	Cryogenic	RRR	Residual resistance ratio
CVD	Chemical vapor deposition	SC	Superconductivity
DW	Domain wall	SdH	Shubnikov–de Haas oscillation
E_g	Energy gap	SEM	Scanning electron microscopy
EBL	Electron beam lithography	STEM	Scanning transmission electron microscopy
EDX	Energy-dispersive x-ray spectroscopy	TCI	Topological crystalline insulator
E_F	Fermi level	TEM	Transmission electron microscopy
FCC	Face-centered-cubic	TI	Topological insulator
FFT	Fast Fourier transform	TSC	Topological superconductor
G_T	Thermal conductance	TSM	Topological semi-metal
G_Q	The quantum of thermal conductance	VLS	Vapor-liquid-solid
HAXPES	Hard x-ray photoelectron spectroscopy	VS	Vapor-solid
HLN	Hikami-Larkin-Nagaoka	WAL	Weak antilocalization
I	Electric current	XPS	X-ray photoelectron spectroscopy
JJ	Josephson junction	$\hbar$	Planck's constant
k	Momentum	XRD	X-ray diffraction
k-PEEM	Momentum-resolved photoelectron microscopy	Φ	Magnetic flux

Abbreviation	Meaning	Abbreviation	Meaning
MD	Molecular dynamic	Φ_0	Quantum of flux

Table 0-1 List of abbreviations

Acknowledgements

I would like to express my gratitude to all those who helped me during these years at Yale and the writing of this dissertation.

First and foremost, my deepest gratitude goes to my advisor Prof. Judy J. Cha for her consistent and illuminating guidance. She led me into the amazing field of topological nanomaterials and kept helping me in all aspects of my life and study. Without her patient instruction and warm encouragement, the completion of dissertation would not have been possible. Also, I would like to thank Prof. Jan Schroers and Prof. Udo Schwarz for serving on my special committee.

Secondly, to all my collaborators from University of Maryland, Brookhaven national lab, Hitachi, and all of the research support staff at Yale.

I would like to thank all members of the Cha Research Group.

I am grateful to all my dear friends and cats for their support and patience all the time.

Additionally, I thank the Yale Graduate School of Arts and Sciences for their support and assistance through these years.

Last but certainly not least, my gratitude also extends to my beloved family who have been supporting me with their unconditional love since I came to this wonderful world. Without their loving considerations and great confidence in me I would not have so much freedom to chase my dream of pursuing knowledge and truth. Specials thanks to my daughter, Maxine(麦希), since she is the reason that I am still holding up.

Oh, and I should not forget to thank myself for always being positive and strong even in the darkest days.

I would like to dedicate this dissertation to my family, my friends and my supervisor, Professor Judy J. Cha.

Chapter 1: Introduction

1.1 Background of Topological Materials

Roughly, a quarter of all known materials are predicted to be topological[1]. Thus, topological materials research is of fundamental scientific significance and will have profound impact on a wide range of applications, such as spintronics, low-dissipation electronics, and topological quantum computing, exploiting the topologically protected spin-polarized electronic states with linear energy-momentum dispersion at the edge or surface of topological materials [2-9].

Such topological interfacial states have been investigated extensively using high-quality bulk crystals and thin films and sophisticated measurement techniques, which have directly visualized topological surface states and confirmed their helical nature. After the first prediction of topological insulators (TIs) characterized by nontrivial Z_2 index preserving time-reversal symmetry and gapless boundary states [7], both two-dimensional (2D) and three-dimensional (3D) TI systems have been extensively investigated. The mesoscopic systems confirmed to be 2D TIs include HgTe (sandwiched by CdTe) with strong spin-orbit-coupling [10, 11], and InAs/GaSb heterojunctions (sandwiched by AlSb) with hybridized band inversion [12-14]. The past decade has also witnessed mounting experimental evidence of topological surface states present in topological nanomaterials. Among 3D TIs, the most studied systems are the intrinsic or alloyed binary tetradymite compounds Bi_2Se_3 and Bi_2Te_3 in bulk form [15-19] or nanoscale [20-

[26]. The sufficiently high bulk resistivity with a high bulk mobility enable the manifestation of surface transport properties, although these materials typically suffer from high bulk carrier densities [3]. The thriving research on TIs draws wide attention on symmetry-protected topological phases. In recent years, a new class of topological insulators is recognized to have crystal-symmetry invariant, i.e. topological crystalline insulators (TCIs) [27], which will be briefly introduced in the following section.

1.2 Topological Crystalline Insulator

The gapless and dissipationless surface states of TCIs are protected by crystal symmetries, such as reflection and rotation symmetries. Compared to TIs, TCIs allow more pathways to tune the electronic properties associated with surface states, including ferroelectric structural distortion, magnetic impurity doping, mechanical strain and thickness engineering [28]. In my work, I focus on a TCI whose topological signatures are protected by mirror symmetry, namely, reflection symmetry with respect to a crystal plane. The mirror operation acts on a spinful wavefunction as $M \begin{pmatrix} \psi_\uparrow(\mathbf{r}) \\ \psi_\downarrow(\mathbf{r}) \end{pmatrix} = \begin{pmatrix} -i\psi_\uparrow(\bar{\mathbf{r}}) \\ i\psi_\downarrow(\bar{\mathbf{r}}) \end{pmatrix}$, where $\mathbf{r} = (x, y, z)$ and $\bar{\mathbf{r}} = (x, y, -z)$. For conventional fermions, $M^2 = -1$ considering the change of sign after 2π rotation, thus, the eigenvalue m can be either i or $-i$. In the momentum space, $|\psi_\mathbf{k}\rangle$ can be chosen as eigenstates of M, more specifically, $|\psi_{\mathbf{k}, m=\pm i}\rangle$ due to the existence of mirror symmetry. Each Bloch (crystalline periodic) wavefunction $|\psi_{\mathbf{k}, m=\pm i}\rangle$ is associated with one of the two topological invariants known as Chern number $N_{\pm i}$.

Now we can define the mirror Chern number as $N_M = (N_{+i} - N_{-i})/2$, a nonzero

integer determining a TCI phase protected by mirror symmetry [29].
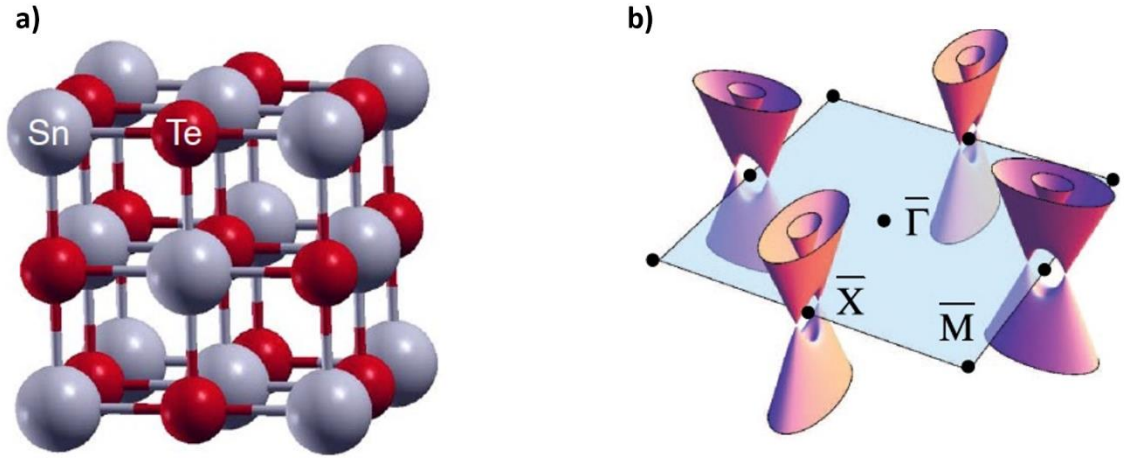
Figure 1-1: SnTe crystal structure and schematic band structure

a, The rock-salt crystal structure of SnTe. **b**, Schematic band structure of the surface states showing the surface Brillouin zone as a blue plane and the four pairs of Dirac nodes, placed across the X point in momentum space. Panel **a** is reproduced from ref.[30], Springer Nature Limited. Panel **b** is adapted with permission from ref. [31], AAAS.

As the first predicted TCI, SnTe has been extensively studied to explore the

physics and applications of the surface states both theoretically and experimentally

[5, 30, 32-40]. SnTe surface states exist on highly symmetric crystal planes of the face-

centered-cubic (FCC) crystal lattice including {100}, {110} and {111}. Fig.1-1 shows

the rock-salt structure of SnTe crystal and the location of the gapless Dirac cones

on the {001} surface Brillouin zones. It should be noted that high concentrations of

Sn vacancies inhibit the surface states to be easily revealed by transport

measurements [41-43], although the helical states are predicted to be immune to

ferroelectric phase transition at low temperature [30]. As dislocations can be sources

or sinks for point defects during crystal growth [44-46], studies that focus on formation and evolution of dislocations in SnTe crystals may be critical in order to reduce the high bulk carrier densities. This requires careful investigations of the crystal growth of SnTe, which remain challenging for nanoscale crystals, such as nanoribbons and nanowires.

1.3 1D Topological System for Next-Generation Electronics

The following section is partially adapted from the preview [47] as 1D topological systems for next-generation electronics. *Matter*, **2021**, 4(8), 2596-2598.

Authors: Hyeuk Jin Han, Pengzi Liu, Judy J. Cha

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The first topological materials studied as nanostructures were the binary tetradymite compounds Bi_2Se_3 and Bi_2Te_3 as TIs, quickly followed by nanoplates of SnTe, the first predicted TCI. Direct synthesis of nanoscale TIs, TCIs, and topological semi-metals (TSMs) via chemical vapor deposition (CVD) and vapor-liquid-solid (VLS) methods has facilitated measurements of nanoscale topological systems to elucidate the nature of topological surface states. Notable synthesis and electron transport results for topological nanomaterials have recently been reviewed[48].

The biggest promise of topological nanomaterials may be the potential realization of one dimensional (1D) topological superconductors, which can support localized Majorana bound states (MBSs) that can be leveraged for fault-tolerant and scalable topological quantum computing[49]. However, to realize 1D topological superconductors, serious challenges must be overcome in all fronts: synthesis of high-quality nanowires that can exhibit topological superconductivity, sophisticated nanodevice fabrication to measure and control the predicted MBSs, and unambiguous detection of MBSs. So far, most notable studies have used strong spin-orbit coupled semiconducting nanowires of InAs or InSb [50] grown by molecular beam epitaxy or metal organic CVD, with superconductivity induced by superconducting metals. However, nanowires of intrinsic TIs and TCIs offer distinct advantages over the spin-orbit coupled nanowires for realizing MBSs in three aspects: intrinsic $p + ip$ superconductivity preserved against disorder, tunable topological superconducting states controlled by magnetic fields, and no need to tune the Fermi level [48].

There are several studies of TI thin films and TCI SnTe nanowires with superconductivity induced by proximity. Much research is needed for topological nanomaterials to realize the ambitious goal of MBS detection. Despite the modest success of demonstrating various topological nanomaterials, our understanding of the topological surface states in these nanomaterials remains basic. For example, we do not yet know the extent of scattering of topological surface states due to crystalline defects, impurities, and coupling to bulk electron states –fundamental transport properties that must be characterized for electronic applications. Further,

the search for MBSs using nanowires, both the spin-orbit coupled semiconducting nanowires or topological nanowires, has been difficult, with no definitive experimental signatures to prove the presence of MBSs.

1.4 Outline of Dissertation

This dissertation will start with the investigation and review of topological materials in nanoscale highlighting recent development of both nanostructure synthesis and transport measurements.

Chapter 2: Topological Materials in Nanoscale

The importance of synthesizing high-quality nanowires raised in the previous section enlightens a number of experimental projects, which are detailed in the following chapters:

Chapter 3: Dislocation-Driven SnTe Surface Defects during Chemical

Vapor Deposition Growth

Chapter 4: Synthesis of Narrow SnTe Nanowires Using Alloy

Nanoparticles

Chapter 5: Ongoing Research: Passivation of SnTe Nanowires

In order to study topological surface states of SnTe nanostructures, the controllable synthesis and careful characterization of high-quality SnTe crystals in nanoscale is essential. Chapter 3 details the observations of various types of surface defects on SnTe nanostructures, arising from dislocations embedded

inside the bulk of SnTe nanostructures during CVD growth and the following cooling process. These surface defects have consequences for the predicted topological properties. The crystal symmetry, surface termination, and surface polarization contribute to distinct morphologies of the surface defects. Here, we develop an facile method, fast cooling, to suppress the formation of surface defects on grown SnTe crystals effectively, although growth conditions need to be further optimized in order to decrease the amount of embedded dislocations that are responsible for the surface defects on {100} and {111} surfaces of SnTe microcrystals and nanostructures. The reliable and reproducible suppression of SnTe surface defects is crucial for achieving the high-crystallinity and narrow SnTe nanowires in Chapter 4 for future investigations of topological surface states.

Chapter 4 details our probe of a reliable route to synthesize narrow SnTe nanowires with a high yield using Au-Sn-Te alloy nanoparticles as growth catalysts. The average diameter of the SnTe nanowires grown using the alloy nanoparticles is 85 nm, in contrast to 240 nm using the gold nanoparticles. This is achieved by applying CVD twice. In the first growth, alloy nanoparticles are formed by the reaction between gold nanoparticles and SnTe vapor. In the second growth, the alloy nanoparticles catalyze the growth of SnTe nanowires via VLS mechanism. Compared with gold nanoparticles, alloy nanoparticles can satisfy the supersaturation conditions more easily and lower the nucleation barrier for the solid phase. This can explain the narrow diameter of the SnTe nanowires grown in the second growth, where their diameter is close to the size of the alloy particle. The reduced diameter of the nanowires effectively removes the bulk carriers, which

is reflected in the higher ferroelectric transition temperature for the narrower nanowires. Transport measurements showed a size-dependent residual resistance ratio and magnetoresistance, suggesting increased electron scattering due to surface oxidation and other possible factors. The increase in the ferroelectric transition temperature suggests that the carrier density decreases for narrower nanowires, likely due to the removal of bulk carriers.

Chapter 5 builds upon the study of improving crystal quality of SnTe nanowires in order to easily reveal and control the topological properties. The major materials challenge facing topological materials is the high residual bulk carrier density and surface degradation, which dominates over surface states, making it difficult to observe transport properties of the surface state in nanoscale devices. For instance, the high bulk hole carrier density of SnTe is due to Sn vacancies and SnTe is prone to surface oxidation and ambient impurities. Therefore, the passivation of SnTe nanowires is of great importance for revealing their topological states. In order to realize surface passivation, SnTe nanowires with and without Te capping are grown under the same growth condition for comparison. After refining Te capping conditions, we are looking for dual evidence from both the ferroelectric phase transition temperature and quantum oscillations, which would suggest that *in situ* Te passivation can lower the carrier concentration in SnTe nanowires and nontrivial surface states are better revealed.

Chapter 2: Topological Materials in Nanoscale

The last decade has witnessed the emergence of a new frontier in condensed matter physics: topological materials with an electronic band structure belonging to a different topological class than that of ordinary insulators and metals.   This non-trivial band topology gives rise to robust, spin-polarized electronic states with linear energy–momentum dispersion at the edge or surface of the materials.   For topological materials to be useful in electronic devices, precise control and accurate detection of the topological states have to be achieved in nanostructures, which can enhance the topological states due to their large surface-to-volume ratios.   In this chapter, we discuss notable synthesis and electron transport results of topological nanomaterials, from TI nanoribbons and plates and TCI nanowires to Weyl and Dirac TSM nanobelts.   We also survey superconductivity in topological nanowires, a nanostructure platform that might enable the controlled creation of MBS for robust quantum computations.   Two material systems that can host MBS are compared: spin–orbit coupled semiconducting nanowires and TI nanowires, a focus of this chapter. Finally, we consider the materials and measurement challenges that must be overcome before topological nanomaterials can be used in next-generation electronic devices.

The following chapter first appeared[51] as Topological Nanomaterials. *Nature Reviews: Materials*, **2019**, 4(7), 479-496.

Authors: Pengzi Liu, James R. Williams and Judy J. Cha

2.1 Background and Motivation

A decade has passed since the first experimental observation of topological materials that do not require stringent experimental conditions to realize a topological state [52]. Topological materials are characterized by an electronic band structure that exhibits a special band topology [6-8], which is now essential to understand the physical properties of many materials. These materials possess topologically protected surface states with unique electronic properties; in TIs the surface states arise from the inversion of the bulk band gap, which is induced by the large spin–orbit coupling of the heavy atoms in the material, and are protected by time-reversal symmetry.

In TCIs, the surface states are protected by crystal symmetry instead. In recent years, topological materials have expanded to include TSMs: Weyl and Dirac semimetals [53] are 3D systems that possess gapless bulk states in the form of relativistic chiral fermions near nodal points and Fermi arc surface states, and are described by the 3D Weyl and Dirac [54] equation, respectively. With breaking of symmetry, either the inversion symmetry or time-reversal symmetry, a Dirac

semimetal can become a Weyl semimetal, as each Dirac point splits into a pair of Weyl points. The early development of topological materials, including notable experimental results and theoretical background on TIs [9, 55-63], TCIs [5, 30], and TSMs [5] are covered in several review articles [4, 28, 53, 64-66].

The electronic properties of the topologically protected surface states are attractive for future electronic applications. For example, the linear dispersion between momentum and energy is promising for high-speed electronics [67-69], the locking of spin and momentum for spintronics [70-74], and the helical nature of the electrons for low-dissipation electronics (where helical means that the direction of motion of the electrons depends on their spin direction) [75-77]. The unique features of the topological surface states have been investigated extensively using high-quality bulk crystals, thin films and surface-sensitive techniques. For example, the band structure and helical nature of the topological surface states have been directly visualized using angle-resolved photoemission spectroscopy (ARPES), hard x-ray photoelectron spectroscopy (HAXPES) and momentum-resolved photoelectron microscopy (k-PEEM) on cleaved TIs [15-19]. Exotic condensed matter states, such as the quantum spin Hall state and the quantum anomalous Hall state, have also been realized using epitaxially grown thin films of topological materials [20, 21, 52, 78-80]. These quantum states provide a rich playground to investigate fundamental interactions of correlated electrons under the topological protection and can be exploited for applications. For device applications, topological materials in the form of nanostructures are necessary for integration into existing device fabrication technologies. In particular, thin-film topological materials are attractive,

because artificial, design-specific heterostructures that interface topological materials with other functional materials, such as superconductors or ferromagnetic insulators, can be fabricated with atomic precision [81-87]. Device applications that are being explored include topological field-effect transistors based on the quantum spin Hall state, which can be rapidly switched off and may be useful for low-power quantum electronics [88], low-power topological magnetic memory devices that exploit the spin-polarized topological surface current [89], and perhaps most excitingly robust quantum bits (qubits) that do not suffer from decoherence [6]. All proposed device applications rely on nanostructures of topological materials.

Studying topological surface states in nanostructures has the advantage that nanostructures reduce as much as possible the influence of the undesirable bulk electronic states in transport measurements, while increasing the surface-to-volume ratio to enhance the contribution of the topological surface or edge states. Early studies of layered TIs, such as Bi_2Se_3 and Bi_2Te_3, used mechanical exfoliation to obtain thin flakes from bulk crystals to maximize the effects of the surface states. Direct synthesis of topological nanomaterials has advanced research into topological states of matter. Transport experiments were performed on TI and TCI nanostructures grown by the VLS and CVD methods (Appendix A.1). Additional advantages of using topological nanostructures for studying topological surface states include the possibility of using effective field-effect gating to tune the Fermi level, potentially adapting the wrap-around gate architecture to the topological nanowires; engineering the bulk bandgap and sub bands exploiting the

nanoscale confinement; and realizing new correlated electronic states due to quantum confinement, leading to phenomena such as the unexpected ballistic transport observed in $LaAlO_3/SrTiO_3$ quantum wires [90, 91].

The nanowire geometry is particularly suitable for nanoelectronic device measurements, such as measurements of the Aharonov-Bohm oscillations (ABO), oscillations in the resistance as a function of the magnetic flux. ABO studies allow phase-sensitive transport measurements of the topological surface states, which are made possible by the well-defined nanoscale cross-section of the samples. The ABOs were observed in several topological nanowire systems, such as Bi_2Se_3 and Bi_2Te_3 TI nanoribbons and nanotubes [24-26, 92], SnTe TCI nanowires [33], and more recently Cd_3As_2 TSM nanowires [93].

Finally, one of the most compelling reasons to study topological nanomaterials is the potential realization of 1D topological superconductors using TI and TCI nanowires with diameters ranging between ~ 10 nm and ~ 200 nm and lengths of more than tens of microns. Superconducting TI or TCI nanowires are predicted to host MBSs — quasiparticle excitations that are identical to their anti-particle counterparts [94] — which can be exploited for fault-tolerant and scalable topological quantum computations without decoherence [95].

In this chapter, we survey recent works on TI, TCI, and TSM nanostructures, grown primarily by the VLS and CVD growth methods, highlighting notable synthesis and transport measurements. We then focus on the control offered by TI nanowires for realizing 1D topological superconductivity to create MBSs, and compare them to another material system that can host MBSs, semiconductor

nanowires with strong spin–orbit coupling [50]. To demonstrate the benefits of TI nanowires, we present numerical simulations that demonstrate local control of the topological superconducting state using a TI nanowire. Finally, we discuss remaining challenges in realizing topological nanostructures with high crystal quality and precise morphology control and in growing robust topological superconducting nanowires.

2.2 Synthesis of Topological Nanomaterials

Most TIs and TCIs and some TSMs have been made into nanostructures, either by mechanical exfoliation from bulk layered crystals or by direct synthesis. This section focuses on the direct synthesis of topological nanomaterials. VLS and CVD growth methods (Appendix A.1) are the two most broadly used methods for the synthesis of topological nanostructures for the study of electrical transport properties. A chronological summary of the synthesis milestones of topological nanomaterials made of TIs, TCIs, and TSMs is presented in Fig. 2-1.
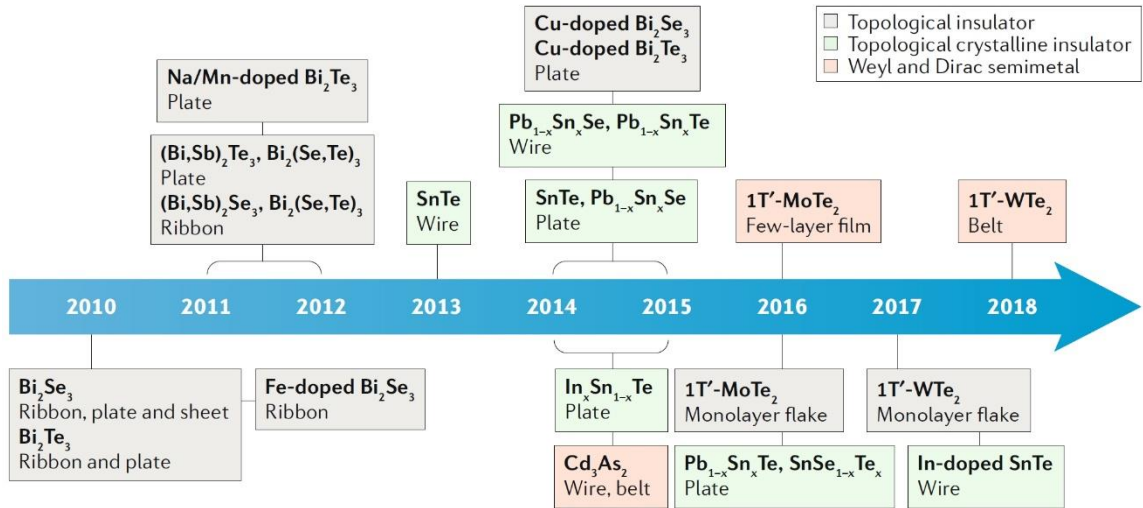
Figure 2-1: Historical timeline of the synthesis of nanostructures of topological materials

First synthesis of various topological materials as nanostructures obtained by vapour–liquid–solid and chemical vapour deposition growth methods.

2.2.1 TI nanostructures

Following the prediction that some binary chalcogenides are 3D TIs [9], Bi_2Se_3, Bi_2Te_3, Sb_2Te_3 and their alloys were quickly synthesized as nanoribbons and nanoplates using the VLS and CVD growth methods (Fig. 2-2a) [25, 96, 97]. Before this prediction, the binary chalcogenides have been extensively studied for their thermoelectric properties and have been made into a variety of nanostructures, including nanorods [98], nanotubes [99], nanosheets, nanospheres [100], and nanoplates [101].

Bi₂Se₃ nanoribbons were first synthesized by metal-catalysed CVD [102]. Gold nanoparticles were used to catalyse the growth and Bi_2Se_3 source powder was heated to form the vapour. The widths of the nanoribbons were larger than

the size of the gold nanoparticles, suggesting that the growth mechanism was a combination of VLS and CVD. Without the use of metal catalysts, Bi_2Te_3 nanoplates with thicknesses ranging from a few quintuple layers to tens of nanometers were grown by CVD [96]. Because Bi_2Se_3 and Bi_2Te_3 are layered, large nanoplates can be easily obtained via CVD. Ternary compounds, such as $(Bi_xSb_{1-x})_2Te_3$ and $Bi_2(Se_xTe_{1-x})_3$, have also been grown by mixing two binary source powders [23, 103]. Doping of TI nanomaterials has also been demonstrated [104-109]: Bi_2Se_3 nanoribbons have been doped magnetically using Fe metal catalysts or introducing ferrocene vapour during growth [104]. Doping Bi_2Se_3 nanoribbons with Sb has shown to be effective in achieving a low carrier density of 2×10^{11} cm^{-2} [107]. To reduce the bulk carrier density, which is key to maximizing the contribution from the topological surface states to the transport signal, the ideal approach would be to eliminate intrinsic chalcogen vacancies. However, it is unclear how easy it is to achieve this goal using the VLS or CVD growth methods. As an alternative, doping studies that explore different dopants and dopant concentrations should be carried out for TI nanostructures.

2.2.2 TCI nanostructures

Whereas TIs are protected by time-reversal symmetry and possess a single topological surface Dirac cone (for the binary chalcogenides), TCIs are protected by a crystal-symmetry invariant [27] and possess multiple topological surface Dirac cones. The TCI SnTe was grown as nanowires, nanoplates, and microcrystals using CVD (Fig. 2-2a) [32, 33]. Unlike the 3D TIs that have a layered crystal structure, SnTe is cubic. Thus, cubic nanocrystals or nanowires with square cross-sections

are expected. However, metal-catalysed CVD can produce large SnTe nanoplates with nanometer thickness and a lateral dimension on the micron scale. The use of metal catalysts and choice of growth substrates greatly affect the morphology of TCI nanostructures. Without the use of gold nanoparticles, cubic SnTe microcrystals were grown on SiO_2/Si substrates [32]. Systematic growths of SnTe and its alloy nanostructures on various amorphous and crystalline substrates were performed, [38, 110-112] and suggested that the strength of the interaction between the growth substrate and the surface adatoms can dictate the morphology of TCI nanostructures and the growth direction of TCI nanoplates; that is, whether TCI nanoplates grow standing vertically with minimum contact with the substrate or laying flat maximizing contact. The interaction strength also influences the diffusivity of the surface adatoms, controlling the growth kinetics of the nanostructures [111, 112]. The morphology of SnTe microcrystals as a function of growth conditions was also investigated, showing that the surface energies of different crystallographic planes can change with the local chemical potential of Sn or Te vapours [38], leading to different morphologies of SnTe microcrystals that minimize the total surface energy (Fig. 2-2b).

Additional TCI nanostructures, such as $Pb_xSn_{1-x}Te$, $Pb_xSn_{1-x}Se$, $In_xSn_{1-x}Te$ and $SnSe_xTe_{1-x}$ nanowires and nanoplates [111, 113-115], have been grown to study the trivial-to-non-trivial phase transition as a function of Pb doping [111], to induce superconductivity using In dopants [116, 117], and to reduce the bulk carrier density

via Se anion doping [118]. Doping was generally achieved by mixing dopant powders

directly with source powders during CVD growth.
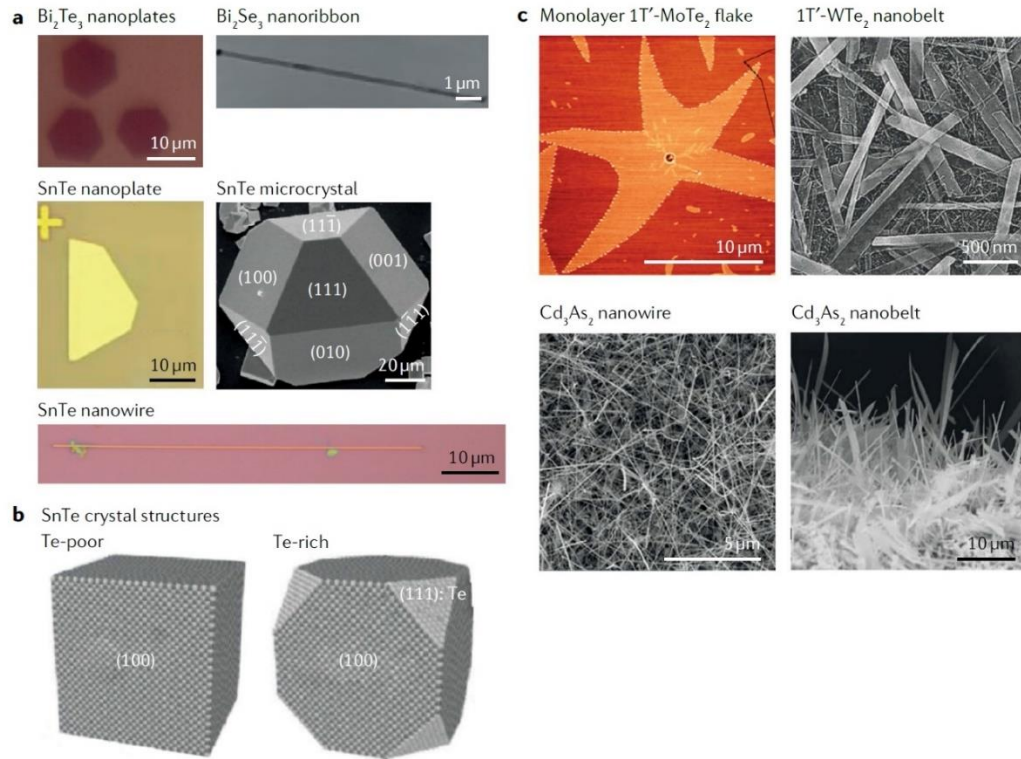
Figure 2-2: Topological insulators, topological crystalline insulators, and Dirac and Weyl semimetallic nanostructures.

a, Topological insulator and topological crystalline insulator nanostructures: Bi_2Te_3 nanoplates, Bi_2Se_3 nanoribbon, SnTe nanoplate, SnTe microcrystal and SnTe nanowire synthesized using the vapour–liquid–solid and chemical vapour deposition (CVD) growth methods. **b,** Wulff constructions of the thermodynamic equilibrium SnTe crystals at Te-poor and Te-rich conditions. **c,** Dirac and Weyl semimetal nanostructures: a monolayer 1T'-$MoTe_2$ flake, 1T'-WTe_2 nanobelts, Cd_3As_2 nanowires and Cd_3As_2 nanobelts grown by CVD. Panel **a** is adapted with permission from refs[96], [34], ACS; ref.[25], Springer Nature Limited; ref.[119], CC-BY-4.0; and ref.[37], Elsevier. Panel **b** is adapted with permission from ref.[34], ACS. Panel **c** is reproduced with permission from ref.[120], ACS; ref.[121], Wiley-VCH; and ref.[122], RSC.

2.2.3 TSM nanostructures

For the most part, Weyl and Dirac semimetals have been studied using bulk

crystals, such as TaAs, TaP [123, 124], NbAs [125] and NbP crystals [126]. Mechanical

exfoliation to obtain nanostructures is generally tricky as many of the TSMs are not layered crystals. For nanostructures, Type II Weyl semimetal $MoTe_2$ in the polymorph structure of 1T' was synthesized as few-layer films and flakes by CVD[120, 127], and 1T'-WTe_2 as nanoribbons and flakes [121, 128]. The distinction between Type I and Type II Weyl semimetals is whether the Weyl point is point-like at the Fermi surface (Type I) or the Weyl points appear as a line (Type II) [129]. Type I Dirac semimetal Cd_3As_2 has been grown by CVD as nanobelts and nanowires [93] (Fig. 2-2c).

Compared to TI and TCI nanostructures, the direct synthesis of Weyl and Dirac semimetals into nanostructures is more challenging. For example, CVD growths of tellurium-based transition metal dichalcogenides are more difficult than the CVD growths of sulfur- and selenium-based transition metal dichalcogenides due to the low formation energies of tellurium-based compounds, such as WTe_2. In addition, many Weyl and Dirac semimetals either contain toxic elements such as arsenic or involve precursors that can form toxic compounds, such as phosphorus. This makes the synthesis of nanostructures using simple VLS and CVD set ups challenging for TSMs, creating a need for growth set ups that can handle toxic gases.

2.3 Electron Transport in Topological Nanostructures

The nature of the topological surface states in nanostructures was probed by measuring electron transport properties of nanodevices. Sufficient experimental results have been reported on TI and TCI nanostructures to confirm the presence of the expected topological surface states and their helical Dirac nature. They include ARPES measurements on TI nanoplates to directly visualize the topological surface state [130], electron transport measurements of TI and TCI nanodevices to demonstrate the 2D and helical nature of the surface states [60, 63, 131, 132], and measurements using Josephson junction devices to study the nature of the superconductivity induced in TI nanostructures [133-136]. For Dirac and Weyl semimetals, topological surface transport has been inferred from quantum interference studies in Cd_3As_2, 1T'-$MoTe_2$ and 1T'-WTe_2 nanostructures [93, 137-139].

This section reviews notable electron transport results for topological nanostructures; a chronological summary is presented in Fig. 2-3. Additional transport results on TI and TCI nanomaterials are summarized in dedicated reviews [140, 141].
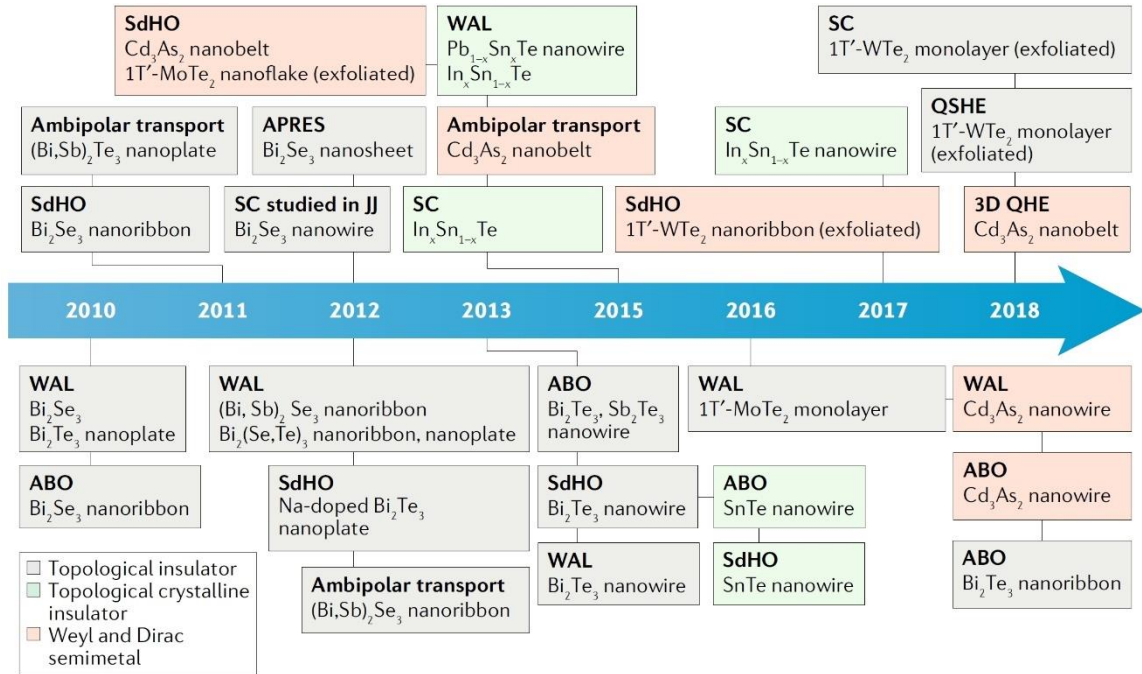
Figure 2-3: Historical timeline of transport measurements in topological nanostructures

Transport results probing the nature of the surface states in topological nanostructures. Before the discovery of topological insulators, many topological materials were extensively studied for thermoelectric properties, but those results are omitted for brevity. ABO, Aharonov–Bohm oscillation; ARPES, angle- resolved photoemission spectroscopy; JJ, Josephson junction; QSHE, quantum spin Hall effect; SC, superconductivity; SdHO, Shubnikov–de Haas oscillation; WAL, weak antilocalization.

2.3.1 TI nanostructures

For TI nanoplate devices, a combination of doping, alloying and field-effect gating can be used to effectively control the Fermi level and minimize the residual bulk carrier density [23, 96, 103, 111, 116]. Ambipolar transport obtained by gating through conventional dielectric layers or an ionic liquid layer has been demonstrated in CVD-grown $(Bi_xSb_{1-x})_2Te_3$ nanoplates [23], $(Bi_xSb_{1-x})_2Se_3$ nanoribbons [107] and $(Bi_xSb_{1-x})_2Se_3$ nanoplates [142], and exfoliated Bi_2Se_3 nanoplates [143]. This is an important demonstration, because it shows that the Fermi level can be tuned

through the Dirac cone and within the bulk gap, which ensures that only the topological surface states contribute to the transport signal.

Early transport studies of TI nanostructures focused on the weak antilocalization feature, which is linked to a quantum correction to the magnetoresistance due to the wave nature of the electrons in a diffusive regime. The feature appears as a dip in the magnetoresistance in small magnetic fields and can be fitted to 2D localization physics using the Hikami-Larkin-Nagaoka (HLN) equation [144] to infer the presence of the surface states [96, 103, 107, 145, 146]. However, localization physics in the diffusive transport regime is not ideal for probing the surface states, because scattering of electrons inevitably leads to the degradation of transport properties and loss of phase information. 2D Shubnikov-de Hass (SdH) oscillations, oscillations in conductivity that reflect the quantum mechanical nature of electrons in the presence of large magnetic fields, were investigated to probe the nature of the Fermi surface in several TI nanoflakes exfoliated from bulk crystals. [135, 147] Landau level fan diagrams obtained from the oscillations were analysed to see if the intercept was -1/2, a signature of Dirac fermions. This analysis can only be accurate if the carrier density is low enough that the Landau indices are small [148]. In one Bi_2Se_3 nanoribbon study [149], the observed 2D SdH oscillations indicated a low carrier density of 1.3×10^{12} cm^{-2} for the surface state, placing the Fermi level within the bulk band gap, at 95 meV below the bottom of the bulk conduction band. The helical nature of the topological surface state was inferred in exfoliated TI nanoflakes by generating a spin-polarized photocurrent with circularly polarized light [150].

Electron transport measurements that really exploit the nanoscale dimension of TI nanostructures are the Aharonov-Bohm oscillation (ABO) studies on narrow nanoribbons or nanowires (Fig. 2-4a) [25]. ABOs are a quantum interference effect produced by electrons encircling a magnetic flux and acquiring a Berry phase shift of π. This is manifested in the resistance, which oscillates as a function of magnetic field B with a periodicity of $\Phi_0 = h/e$ (conventional electrons) or $h/2e$ (helical electrons). The ABOs were first observed in Bi_2Se_3 nanoribbons and studied more carefully in a follow-up experiment using Se-coated Bi_2Se_3 nanoribbons (Fig. 4b–e) [24]. The Se coating was critical in preventing surface oxidation, which degrades the carrier mobility and introduces a low-mobility electron gas on the surface [151]. Careful analysis revealed that indeed the oscillations originated from the topological surface electrons. ABOs with conductance maxima at odd values of $\Phi = \pm\Phi_0/2$ have been reproduced in Bi_2Te_3 nanoribbons (Fig. 2-4f) and nanotubes [26, 92]. ABOs were also observed in SnTe TCI nanowires [33] and Cd_3As_2 TSM nanowires [93].

2.3.2 TCI nanostructures

Soon after the experimental identification of SnTe and its alloys as TCIs by ARPES, SnTe and doped SnTe nanowires and nanoplates were synthesized and their electron transport properties investigated. ABOs, SdH oscillations and weak anti-localization have been observed in VLS-grown pristine or Pb-doped SnTe nanowires (Fig. 2-4g) [33, 115]. One major distinction between TIs and TCIs is the number of topological surface states in the system. The binary chalcogenide TIs possess one surface state, whereas the SnTe-based TCIs possess 4 surface

states on each of the {001}, {111} and {110} surface planes [40]. In principle, information on the number of surface Dirac cones can be extracted from weak antilocalization measurements. The scaling parameter α in the HLN equation should reflect the number of cones present: a single Dirac cone would give $\alpha = -0.5$. For SnTe and its alloy nanoplates, values of $|\alpha|$ ranging from 0.5 to 5 have been reported, suggesting the presence of multiple Dirac cones [152]. However, a simple one-to-one correspondence between α and the number of cones is complicated by the presence of a conducting bulk. For example, even for TI nanostructures with a single Dirac cone, the value for α is often not -0.5 and depends on many factors. For TCI nanostructures with multiple Dirac cones, it is difficult to probe the surface states using weak antilocalization. One study suggests that the weak antilocalization observed in SnTe nanoplates is actually a bulk effect [116]. ABOs were reported in SnTe nanowires [33] (Fig. 2-4g), but there are no follow-up studies. More careful analysis of the ABOs is necessary to understand the nature of the multiple Dirac cones in SnTe and this remains an outstanding problem in the field.

Another factor to consider for TCIs, which is absent in TIs, is the structural transition from the high-temperature cubic structure to the low-temperature rhombohedral structure [153, 154]. This structural phase change is associated with a ferroelectric transition and mediated by electron–phonon interactions [155]. Theoretically, Dirac cones on {001} surfaces are predicted to become gapped due to the loss of crystal symmetry, whereas the ones on {111} surfaces are expected to remain intact. The structural transition has been observed in SnTe and

SnSe$_x$Te$_{1-x}$ nanoplates [32, 118], but its effects on the surface states have not been

probed in transport measurements.
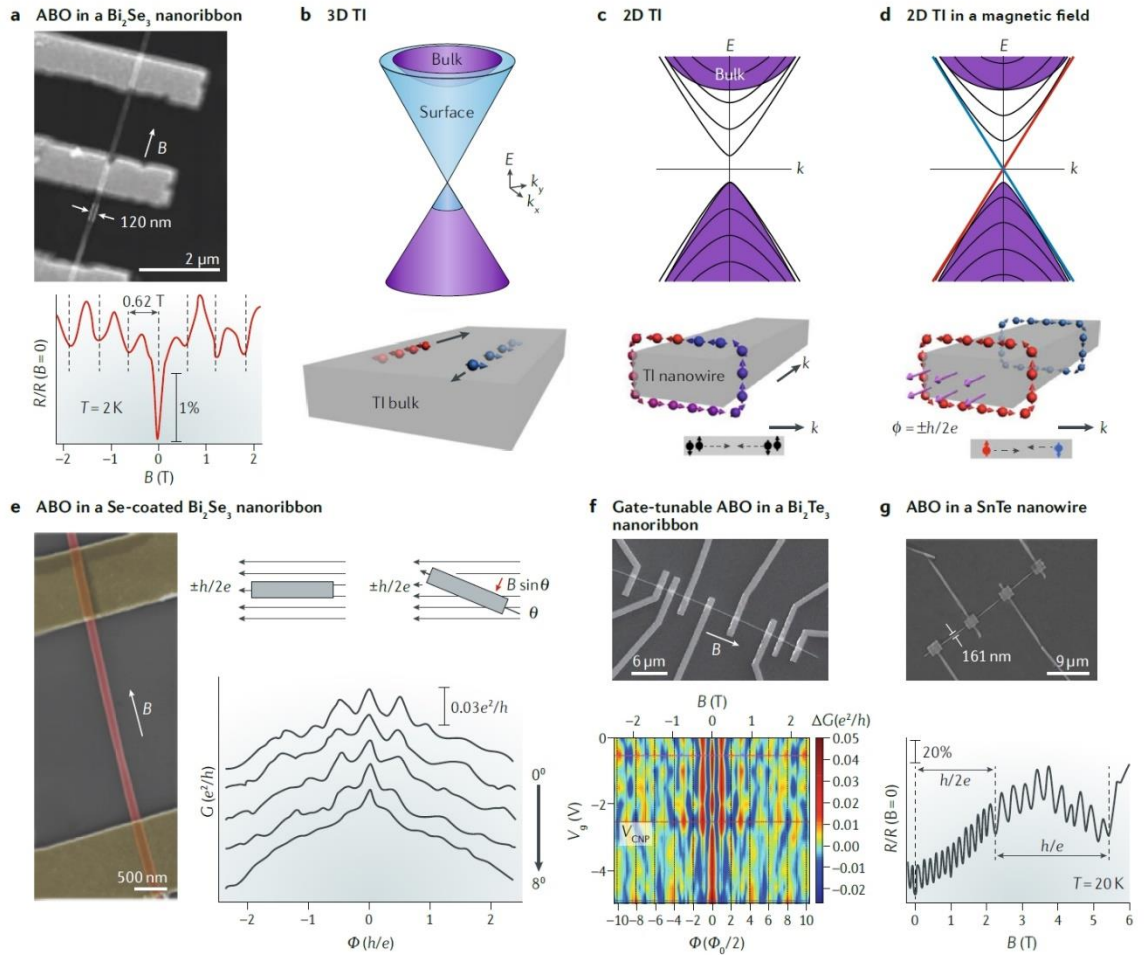
Figure 2-4: Aharonov–Bohm effects of topological surface states in TI and TCI nanostructures

a, Scanning electron microscope (SEM) image of a 120-nm-wide, 55-nm-thick Bi$_2$Se$_3$ nanoribbon contacted by four Ti/Au electrodes. In this system, magnetoresistance (*R*) oscillations with a period of 0.62 T, corresponding to one flux quantum (*h*/*e*) threaded into the cross- section of the nanoribbon, are observed at 2 K. **b,** Schematic band structure of the 3D topological insulator (TI) Bi$_2$Se$_3$. The surface states (blue) exist inside the gap of bulk bands (purple). Topological surface electrons are spin- polarized (red and blue arrows). **c,** Schematic band structure of a TI nanowire in zero magnetic field. The surface band transforms into discrete 1D sub-bands with spin degeneracy. The 2π rotation of the helical surface electron spin along the nanowire perimeter gives rise to a Berry's phase (π) in the electron wavefunction, which opens a gap in the 1D bands. **d,** Schematic band structure of a TI nanowire with magnetic flux *Φ* = ±*h*/2*e* (purple arrows). The gapless 1D band (red and blue lines) is predicted to be a topologically non- trivial electronic state with no spin degeneracy. Electrons with opposite spin orientations propagate in opposite directions.

e, SEM image of a Bi_2Se_3 nanoribbon device. Adding a perpendicular magnetic field component by rotating the device breaks the time- reversal symmetry condition at $\Phi = \pm h/2e$, resulting in localized helical 1D modes in a disordered TI nanowire. Quantum interference (helical 1D peaks at $\Phi = \pm h/2e$) is suppressed as the angle θ increases, as seen in the conductance (G) plots. **f,** SEM image of a 150-nm-wide, 60-nm-thick Bi_2Te_3 nanoribbon device. The colour map of the magnetoconductance ΔG versus gate voltage V_g and magnetic field B shows Aharonov–Bohm oscillations (ABO) with $\Delta G(B)$ maxima at both odd multiples of $\Phi_0/2$ (half- integer flux quanta, unique to topological surface states) and even multiples of $\Phi_0/2$ (except at $\Phi = 0$), suggesting a competition between π-ABO and 0-ABO at different V_g. **g,** SEM image of a 161-nm-wide, 240-nm-thick SnTe nanowire device. The magnetoresistance curve displays two oscillation frequencies, h/e (0.313 T) and $h/2e$ (0.165 T), indicating the diffusive transport regime. Panel **a** is adapted from ref.[25], Springer Nature Limited. Panels **b**–**e** are adapted with permission from ref.[24], ACS. Panel **f** is reproduced from ref.[26], Springer Nature Limited. Panel **g** is adapted with permission from ref.[33], ACS.

In-doped SnTe nanoplates and nanowires were reported to show superconductivity.   In-doped SnTe nanoplates were synthesized on silicon substrates using SnTe and InTe powders as precursors and a gold film as metal catalyst for growth [116]. The In doping concentration varied from 0 % to 10% with a loading ratio of SnTe:InTe = 1:2. Transport data showed the onset of superconductivity around 1.7 K (Fig. 2-5a). The bulk crystal growth, chemical vapour transport, was also adapted by inserting silicon substrates inside the sealed quartz tube to grow In-doped SnTe nanoplates without the use of metal catalysts or transport agents (Fig. 2-5b) [117]. An In-doped SnTe bulk crystal was first grown by mixing high-purity elements and then used as source for the nanoplate growth. A sharp transition to the superconducting regime was observed with a critical temperature just below 2 K, similar to the result shown in Fig. 2-5a.
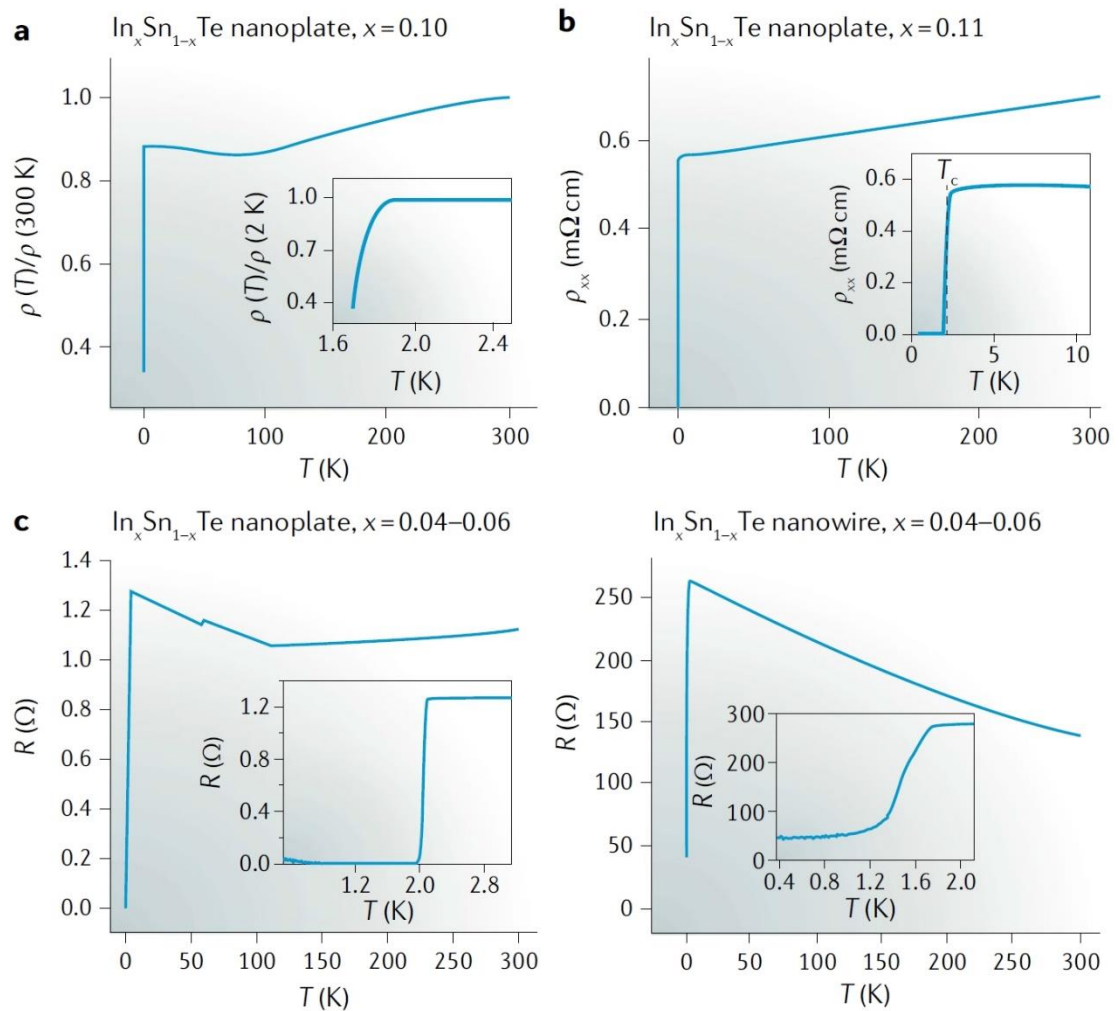
Figure 2-5: Superconducting transitions in various in$_x$Sn$_{1-x}$Te nanostructures

a | Temperature dependence of the normalized resistivity ρ of a nanoplate device with $x = 0.10$ and a thickness of 346 nm, showing a superconducting transition at 1.7 K. **b** | Temperature dependence of the resistivity of a nanoplate device with $x = 0.11$ and a thickness of 57 nm, showing a superconducting transition at 2.2 K. **c** | For a nanoplate device with $x = 0.04$–0.06, the superconducting transition occurs below 2.1 K. An upturn in the resistance R below 0.4 K is also observed. For a nanowire device with $x = 0.04$–0.06 and a width of 193 nm, the superconducting transition is gradual, and the resistance saturates to $R \approx 55$ Ω at the base temperature. Panel **a** is adapted with permission from ref.[116], ACS. Panel **b** is adapted with permission from ref.[117], ACS. Panel **c** is adapted from ref.[119], CC- BY-4.0.

A desired nanostructure for quantum computations is superconducting SnTe in nanowire form, which was first synthesized in 2017. In-doped SnTe nanowires were obtained using gold nanoparticles as growth catalysts and SnTe and InTe as source and dopant powders [119]. In the same growth, nanoplates, nanoribbons and nanowires were obtained, with their classification loosely determined by the width of the nanostructures. All of the nanostructures became superconducting below 2 K but displayed important differences (Fig. 2-5c). Nanoplates exhibited a sharp transition into a superconducting regime but, interestingly, the resistance began to increase from zero to finite values at 400 mK. Nanoribbons showed a gradual transition into the superconducting regime. Nanowires showed non-zero residual resistance after transitioning into the superconducting regime. The origin of this non-zero resistance is unclear. Quantum effects such as quantum phase slips due to nanoscale confinement and potential contact issues have been ruled out. A mundane reason could be material issues, such as inhomogeneous distribution of indium dopants or the presence of gold atoms as impurities. Gold atom impurities have been observed in some gold-catalysed SnTe nanostructure growth [156]. However, such material imperfections should also be present in nanoplates. The origin of the non-zero resistance in superconducting In-doped SnTe nanowires needs to be further investigated.

2.3.3 Weyl and Dirac semimetal nanostructures

The study of the predicted surface Fermi arcs through transport measurements in Weyl and Dirac semimetals is challenging, because the bulk metallic states are always present in these materials, making up a large fraction of

the transport signal.   Nanostructures can be advantageous due to their high surface-to-volume ratios, which can minimize the contribution from the bulk states. Moreover, by controlling the morphology of the nanostructures to maximize specific crystallographic planes, it may be possible to perform momentum-selective transport measurements. This is important because the surface Fermi arcs start and end at well-defined points in momentum space.

Due to the challenges related to the synthesis of these materials, most electron transport studies of Weyl and Dirac semimetals have used bulk crystals, but some transport studies on nanostructures are available, and here we discuss a few. Cd_3As_2, a Type I Dirac semimetal, was synthesized as nanowires, and ambipolar transport was achieved by field-effect tuning of the Cd_3As_2 nanowire device [93]. A Hall-bar device based on a Cd_3As_2 nanobelt showed anomalous, double-period SdH oscillations that resulted from two ellipsoidal Fermi surfaces, suggesting the dimensionality-dependent transport expected of a 3D Dirac semimetal [93]. ABOs were also observed in a Cd_3As_2 nanowire device with the peak positions at odd integers of $\Phi_0/2$ with a period of Φ_0, suggesting the presence of topological surface states [137]. Negative magnetoresistance was also observed in the nanowire and attributed to the chiral anomaly, a phenomenon that involves a current flow between the Weyl nodes in the presence of parallel electric and magnetic fields [157]. A negative magnetoresistance is expected in a Dirac semimetal due to its topological nature, but mundane effects, such as disorder in the system, can also lead to negative magnetoresistance. Thus, systematic transport studies that rule out other effects are critical. Recently, Weyl orbits in a

Cd$_3$As$_2$ nanobelt were reported to contribute to the 3D quantum Hall effect: transport measurements highlighted a dependence of the Landau levels on the sample thickness, unveiling the 3D signature of this new type of quantum Hall effect [158] (Fig. 2-6a). This is the first time the quantum Hall effect is observed in an intrinsically 3D crystal. Previously, wedge-shaped Cd$_3$As$_2$ slabs were prepared by milling of the bulk crystal by a focused ion beam [159]. The benefit of using nanostructures directly rather than focused ion beam milling is that no material damage is induced during the preparation, enabling the investigation of morphology-dependent transport to study the Weyl or Dirac state.
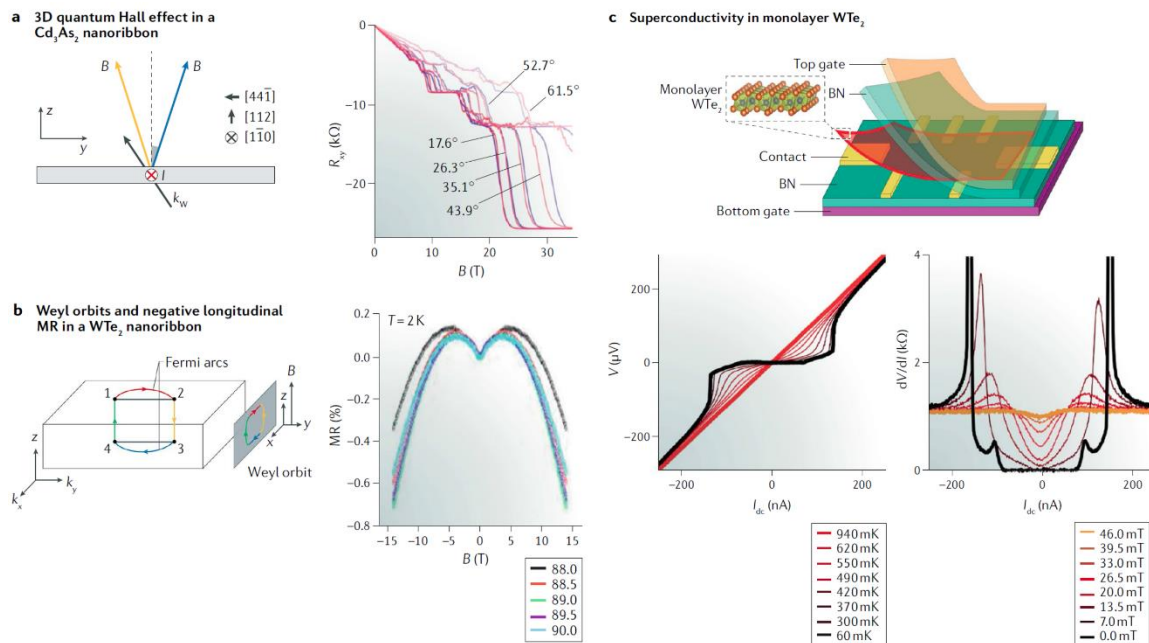
Figure 2-6: Electron transport studies of Weyl and Dirac semimetals

a, Angular dependence of the 3D quantum Hall effect in a Cd$_3$As$_2$ nanoribbon. The schematic shows the measurement geometry. The grey arrow denotes the Weyl vector kW, which is defined by a pair of Weyl nodes along the [100] axis. The magnetic field B is tilted by a positive or negative angle θ, marked by the blue or yellow arrow. In the Hall resistance (R_{xy}) plot, notable deviations can be observed between R_{xy} measured at positive and negative tilt angles (red and blue curves, respectively), which are attributed to the existence of Weyl nodes and to the Zeeman effect. Such deviations are not expected to occur owing to thickness- modulated changes in the Fermi level or band structure. **b,** Fermi-arc-induced Weyl orbits and chiral- anomaly-induced negative longitudinal

magnetoresistance (MR) in a WTe$_2$ nanoribbon. The formation of the Weyl orbit under a magnetic field in a WTe$_2$ nanoribbon is illustrated in the left part. Two pairs of Weyl nodes (1–2 and 3–4) with opposite chirality are connected by two real- space paths through chiral bulk Landau levels along the z direction and by two Fermi arcs in momentum space. The field- angle dependence of the negative longitudinal magnetoresistance shows that the absolute value of the magnetoresistance decreases significantly with a minor change of the field angle θ from 90° to 88°, which is a signature of magnetoresistance induced by the chiral anomaly. **c,** Superconductivity was observed in a gated monolayer WTe$_2$ device, shown in the top part. The voltage–current ($V–I_{dc}$) and dV/dI versus I_{dc} behaviours of this device at various temperatures and magnetic fields are shown. A zero- voltage plateau is observed at 60 mK, confirming the superconducting state in the WTe$_2$ single- layer sheet. Panel **a** is reproduced from ref.[158], Springer Nature Limited. Panel **b** is adapted from ref.[139], CC-BY-4.0. Panel **c** is adapted with permission from ref.[160], AAAS.

Some transition metal dichalcogenides are predicted to be Weyl semimetals, such as 1T'-MoTe$_2$ and 1T'-WTe$_2$. Chiral-anomaly-induced negative magnetoresistance and Fermi-arc-induced Weyl orbit oscillations were observed in an exfoliated 1T′-WTe$_2$ nanoribbon, providing evidence that WTe$_2$ is a type II Weyl semimetal [139] (Fig. 2-6b). A bandgap opening of ~ 60 meV was also observed by absorption spectroscopy in exfoliated 1T'-MoTe$_2$ flakes [138]. Recently, superconductivity induced by field-effect gating was observed in monolayer WTe$_2$ [160, 161], which is exciting as monolayer WTe$_2$ was established as a 2D TI with a quantum spin Hall state that persisted up to 100 K [162], a temperature easily accessible with liquid nitrogen for practical device realization. The quantum spin Hall state and the superconducting transition were realized in the same device by tuning the top and bottom gate voltages below 1 K, offering a promising route to explore a 2D topological superconductor (Fig. 2-6c). All transport measurements were carried out on exfoliated samples that were encapsulated with hexagonal boron nitride, which provide inert electric environment and prevent oxidation.

2.3.4 Inducing superconductivity in topological nanostructures

Topological quantum computation might be made possible by inducing superconductivity in topological nanowires to produce MBSs. Two routes to induce superconductivity into topological materials have been attempted. The first option is to place topological materials next to a superconductor to induce superconductivity by proximity. This was tried in Bi_2Se_3, Bi_2Te_3 and Sb-doped Bi_2Se_3 flakes exfoliated from bulk crystals or synthesized as nanoribbons and films, which were proximitized with superconducting metals and showed unconventional properties when characterized with Josephson junction devices[133, 135, 136]. Another route to induce superconducting correlations in topological materials is by intercalation or doping. In bulk crystals, superconductivity has been demonstrated in metal-intercalated TIs, such as Cu-, Sr- and Tl-intercalated Bi_2Se_3 and Bi_2Te_3 [163-165] and Sb_2Te_3 of a specific stoichiometry [166], In-doped SnTe [41, 167, 168], and WTe_2 and $MoTe_2$ under pressure or doping [169-172]. The nature of the superconductivity and the question of whether it is topological needs further study; evidence for unconventional superconductivity has been obtained in point-contact spectroscopic studies carried out on the surface of a Cu-intercalated Bi_2Se_3 bulk crystal and an In-doped SnTe bulk crystal [41, 164, 173].

Superconductivity has been demonstrated in a few topological nanostructures, including In-doped SnTe nanoplates and nanowires (TCI system) [116, 117, 119] and mechanically exfoliated monolayer WTe_2 flakes (TI system) [160, 161]. Although metal intercalation into TI nanostructures has been demonstrated using various metal atoms, which induced changes in the electrical and optical properties

[174, 175], superconductivity has not been achieved in metal-intercalated TI nanostructures.

2.4 1D Topological Superconductivity

Currently, there is an intense focus on realizing and manipulating MBSs for topological quantum computations. Topological nanowires are uniquely suitable for this purpose. In this section, we discuss 1D topological superconductivity and how to control the expected MBSs in such systems.

Before the discovery of TIs, topological phases of superconductors were predicted to exist for p-wave pairing of 2D fermions [176-178]. When TIs were discovered, a direct analogy between TIs and superconductors was observed: the Bogoluibov–de Gennes equation for a *p*-wave superconductor is identical in structure to the Dirac equation, though the two equations have different origins. As TIs exhibit novel excitations at the intersection of gaps of different sign — for example at the surface of the TI material — so do topological superconductors, producing MBSs at zero energy on the surface of a topological superconductor. Topological nanowires offer unique control over the topological superconducting states, providing clear advantages over other materials that may host MBSs.

The basics of 1D topological superconductivity and of the creation of MBSs in 1D systems are explained in Appendix C.1, which describes a helical metal that mimics the spinless Kitaev model. A topological superconducting state can be induced in the helical state by adding superconducting correlations.

2.4.1 Spin–orbit coupled nanowires versus TI nanowires

Two classes of nanowires have been studied to search for MBSs: nanowires made from topological materials, such as TI Bi_2Se_3 [133] or TCI SnTe [179], and from semiconductors with strong spin–orbit interactions, such as InAs or InSb [50, 134]. For the TI case we will only consider systems with a single Dirac cone, such as Bi_2Se_3. In systems where multiple Dirac cones are present, as in TCIs, it is also possible to host MBSs [28, 110], and the control mechanics described here are equally applicable. Adding superconducting correlations into TI nanowires or semiconducting nanowires with spin–orbit interactions is typically done via doping, as in the case of In-doped SnTe, or by exploiting the proximity effect, in which a superconductor is placed in contact with the material and superconducting correlations are allowed to 'leak' in.
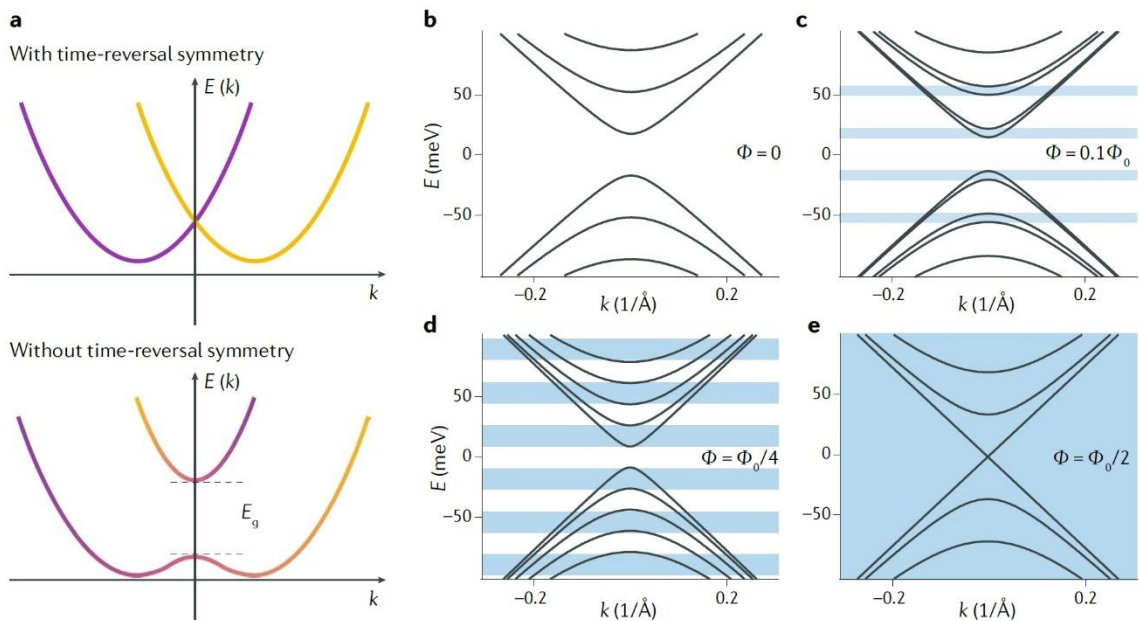
Figure 2-7: 1D topological superconductors

a, Band structure for a material with strong spin–orbit coupling in the presence and absence of time- reversal symmetry. To achieve a helical state, the Fermi energy must be in the energy gap E_g. The yellow and purple colours indicate spin orientation up and down, respectively. **b–e,** Band structure for a nanowire of a strong topological insulator material with a radius of 100 nm as a

function of magnetic flux, Φ; Φ_0 is the quantum of flux. For certain values of the chemical potential (shown in blue), the wire meets the criterion for topological superconductivity. When $\Phi = \Phi_0/2$, the wire is in the helical phase for all values of the chemical potential.

The most experimentally explored topological superconducting systems thus far are 1D semiconducting nanowires with strong spin–orbit coupling, such as InAs and InSb nanowires grown by molecular beam epitaxy [50] or metalorganic CVD [134]. The focus on these systems is largely due to the fact that the crystal quality of these nanowires is currently much better compared to that of other material systems, including TI nanowires. The energy band structure for semiconducting nanowires is shown in Fig. 2-7a: the conventional parabolic dispersion is split along the k-axis from the spin–orbit interaction. When time-reversal symmetry is present, the Kramers degeneracy at $k = 0$ must be preserved, and there is a two-fold spin degeneracy ($E_\uparrow(k) = E_\downarrow(-k)$). This degeneracy can be broken by removing the time-reversal symmetry, which is most commonly achieved by applying a magnetic field perpendicular to the spin–orbit field. When this is done, the Kramers degeneracy at $k = 0$ is removed and one of the double-degeneracies at the Fermi energy is absent. It is in this sense that the 1D wire is spinless and has the potential to realize Kitaev's model. Under these conditions the wire is said to be helical when the Fermi energy is within the gap that forms, which has energy E_g. The term helical refers to the fact that the spin eigenvalue is associated with the direction of propagation. The progress on synthesis and transport results on spin–orbit coupled semiconducting nanowires is summarized in a recent review [50].

In strong TI nanowires, a helical surface state can also be obtained but, unlike in strong spin–orbit coupled nanowires, time-reversal symmetry is preserved. The energy spectrum of eigenstates in a strong TI nanowire is given by

$$\epsilon_{n\pm} = \pm\hbar v_s \sqrt{\left[\left(n + \frac{1}{2} - \frac{\Phi}{\Phi_0}\right)/R\right]^2 + k^2}. \tag{2-1}$$

Here $\hbar$ is the reduced Planck's constant, v_s the surface velocity of electrons, k the momentum along the wire, $n = 0, \pm 1 \ldots$ the angular momentum states around the wire, Φ the magnetic flux through the wire, R the radius of the wire and Φ_0 the quantum of flux. What is important is that a zero-energy mode is created when a half flux quantum, $\Phi_0/2$, is passed through the wire. Given the flux-dependent band structure, the criterion for the TI wire to host MBSs when superconducting correlations are introduced can be analysed by looking at the degeneracy of each level as a function of the magnetic field. When $\Phi = 0$, each level is doubly-degenerate from different angular momentum states with the same energy (for example, $\varepsilon_{0-} = \varepsilon_{-1+}$ at $\Phi = 0$) and each MBS is doubly occupied (that is, it forms a conventional fermionic mode, Fig. 2-7b). The application of small parallel magnetic fields allows for these level degeneracies to be broken, so that regions of energy levels with odd occupancy grow with magnetic field (blue regions in Fig. 2-7c and d); in these regions, the criterion for topological superconductors containing MBSs is met. For $\Phi = \Phi_0/2$, and for a range of neighbouring values [180], only odd occupancies are permitted and a state with MBSs is permitted for all values of the Fermi energy (Fig. 2-7e). Thus, topological superconductivity can be controlled both with a magnetic field and, when $\Phi \neq 0$ or $\Phi_0/2$, with a gate voltage. Typically,

chemical potential changes of 200 meV can be obtained using a field-effect geometry, and it is possible to tune the chemical potential entirely through the zero-energy Dirac point [23].

Also of importance is the preservation of time-reversal symmetry when $\Phi = \Phi_0/2$. At $\Phi = 0$, each level is two-fold degenerate (Fig. 2-7b). The application of $\Phi_0/2$ along the axis of the wire produces an Aharonov-Bohm phase difference of $\theta_{AB} = \int \boldsymbol{A} \cdot d\boldsymbol{l} = 2\pi$ between time-reversal symmetry paths, and this trivial phase preserves the two-fold degeneracy observed when time-reversal symmetry is present. It is important to note that, unlike in conventional materials, the zero-field Kramers pairs are not the same pairs at $\Phi = \Phi_0/2$. For example, ε_{0-} and ε_{-1+} are degenerate at $\Phi = 0$, but ε_{0-} and ε_{0+} are degenerate at $\Phi = \Phi_0/2$. The swap of Kramers pairs is a hallmark of the Z_2 classification of the topological state obtained at $\Phi = \Phi_0/2$ [181].

The key transport property of TI nanowires that indicates the presence of the topological surface state is the presence of Aharonov-Bohm oscillations. However, a mere observation of the Aharonov-Bohm effect is not sufficient to probe the topological nature of the surface state. Conduction maxima at odd values of $n\Phi_0/2$ also have to be observed[182]. This is to be contrasted with a conventional Aharonov-Bohm effect where maxima are predicted at even values of $n\Phi_0$, including $n=0$. Experimental work has shown that TI nanowires do in fact conform to the theoretical expectation, as shown in Fig. 2-4f for a Bi_2Te_3 nanowire [26]. When the Fermi level is placed at or near the charge neutrality point, peak conduction

values occur at odd integers of $\Phi_0/2$. This persists for a small range of gate voltages on the hole side of the charge neutrality point before a conventional Aharonov-Bohm phase is observed, purportedly arising when the Fermi level enters the bulk valence band.

Generating a helical state in this way in TI nanowires offers several advantages over strong spin–orbit-coupled nanowires. The first is that no fine tuning of the energy level is required. For strong spin–orbit-coupled nanowires, the location of the Fermi energy plays an important role in creating MBSs rather than trivial zero-energy Andreev bound states [183]. Unlike strong spin–orbit coupled nanowires in which the helical state only exists over a narrow range of energies, at $\Phi = \Phi_0/2$ strong TI nanowires are guaranteed to be in the topological state regardless of the location of the Fermi energy, provided the Fermi energy lies in the band gap. This also alleviates the role of additional subbands, which have been experimentally shown to mask the interpretation of evidence for the helical state [184]. The second advantage is that for strong TI nanowires coupled to conventional s-wave superconductors, the $p + ip$ superconducting state can be created when time-reversal symmetry is preserved, and the resulting superconductivity is immune to disorder, as it is protected by Anderson's theorem [185]. The helical nature of the surface state in the TI guarantees that the induced superconductivity is $p + ip$ in nature, which allows for much larger energy scales for the MBSs, enhancing the prospects for creating this unique superconducting state [185]. The third advantage is that a magnetic field can be used to create and control the topological superconducting state. This should be contrasted with the use of electric fields in

spin–orbit coupled nanowires, which can be complicated by the fact that the MBSs exist very near a superconductor whose high density of electrons can obfuscate applied local electric fields for the control of the MBSs.

2.4.2 Prospect for 1D topological superconductors using TI nanowires

The control over the formation and location of MBSs is of upmost importance in the progression towards the use of MBSs in a topological quantum computer: for braiding operations to be performed, MBSs must be manipulated locally. Gate control of the location of a MBS is possible with an electric field, although it is difficult due to the proximity of the superconductor, which screens the electric field in the wire. Here we investigate the possibility of controlling the location of a MBS with magnetic fields using local B control gates made of current-carrying wires (Fig. 2-8). For TI nanowires with diameters as large as 300 nm, the parallel magnetic fields needed to create the topological superconducting state are as small as 23 mT. Current-carrying wires near the TI wire can locally produce magnetic fields that are an appreciable fraction of 23 mT. As a proof of principle, we present a finite element method simulation of three nearby wires (cross-section of 300 nm by 300 nm; the superconductor is not included in the simulations). Current is passed through one or all of the three wires (B control gates, Fig. 2-8) to generate a component of magnetic field B_x along the axis of the wire. In this configuration the topological quantum phase transition is tuned by two sources: a global magnetic field supplied by a large superconducting solenoid and a local magnetic field supplied by the B control gates. The special distribution of the x component of the magnetic field generated by passing 1 mA of current through the
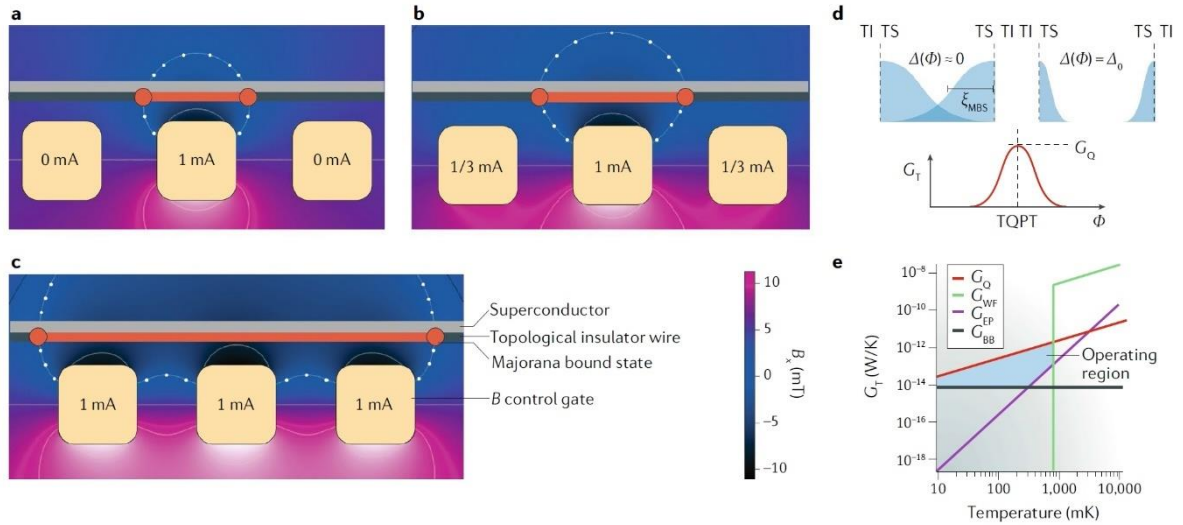
Figure 2-8: Controlling and detecting Majorana bound states in topological insulator nanowires

a–c, Finite element simulations for the magnetic field (B) profile generated by three B control gates, each 300 × 300 nm, used to manipulate the position of a pair of Majorana bound states (MBSs, red circles). The values of the current in the three wires are indicated. The dotted contour indicates Bx = 5 mT. The central wire is used to drive the initial topological quantum phase transition that generates the pair of MBSs, and the outer two wires are used to drive the pair towards the end of the wire. **d,** MBSs in a topological insulator–topological superconductor–topological insulator (TI–TS–TI) device. Illustration of the spatial extent $\xi_{MBS} = hv_F/\Delta$ (where h is Planck's constant, v_F the Fermi velocity and Δ the size of the topological gap) of the MBSs in the wire near (left) and away from (right) the topological quantum phase transition (TQPT). The MBSs are shown only on the inside of the TI–TS interface, indicated by the dashed line. At the TQPT, the overlap of the two MBSs produces a peak in the thermal conductance G_T that is equal to the quantum of thermal conductance G_Q, regardless of the amount of disorder. **e,** Estimation of the contributions to G_T in a TI nanowire. Below $T \approx 800$ mK, G_Q is the largest of the four contributions (also considered: G_{WF}, thermal conductance from electrons described by the Wiedemann–Franz Law, presumed to be zero below the critical temperature of the superconductor; G_{EP}, thermal conductance from electron–phonon coupling, as calculated for Bi_2Se_3 (ref.[186]); G_{BB}, thermal conductance from blackbody radiation[187]), which leads to the definition of a proposed operating region (blue).

central wire is shown in Fig. 2-8a, where the dotted contour indicates B_x = 5 mT. If

the global field is set to 5 mT below the value corresponding to the phase transition,

two MBSs (the red circles) arise where the 5 mT contour line intersects the

nanowire. As an example, the magnetic field necessary for the phase transition for

a 100 nm nanowire is 212 mT, so in this scenario the solenoid would be set to 207

mT and the local gate would provide the extra 5 mT to drive the transition. Here,

unlike in the case of electric-field gating in which the superconductor hinders the Fermi energy control, the screening (Meissner) properties of the superconductor enhance the parallel magnetic field seen by the wire, and 5 mT represents a lower bound on the magnitude of the field. If the current in the outer two wires is increased to 1/3 mA, the MBSs are pushed towards the ends of the nanowire (Fig. 2-8b) and finally to the ends of the nanowire when all the *B* control gates have currents of 1mA (Fig. 2-8c). This technique can be used to test fusion rules and, in T-shaped nanowires, to perform braiding operations and readout as prescribed in Ref. [95]. MBS detection via thermal transport (Fig. 2-8d) is discussed in a later section.

2.5 Key Challenges

For the realization of topological quantum computers that are resistant to errors, synthesizing robust 1D topological superconductors using topological nanowires is critical. However, several challenges remain. Efforts into studying superconducting topological nanowires should be accompanied by active research in various topological nanomaterials and nanostructures to tackle the synthesis and transport challenges specific to nanoscale systems.

2.5.1 Material challenges

Controlling the crystal quality and morphology of topological nanostructures remains challenging. For example, for chalcogen-based TIs and TCIs such as Bi_2Se_3, Bi_2Te_3 and $SnTe$ nanostructures, defect densities, primarily chalcogen

vacancies, remain high, contributing to a high residual bulk carrier density. Vacancy defects persist despite chalcogen-heavy synthesis conditions due to the low formation energies of vacancy sites. Thus, efforts to further reduce these vacancies or to find compensation doping schemes that do not degrade electron mobility are essential. Theoretical calculations of the energy levels of different dopants in topological materials would be helpful in aiding experiments. In addition, detailed knowledge on other types of defects, such as anti-site defects and line defects such as screw dislocations, is limited even though these defects do doubtlessly degrade transport properties or induce new topological edge states. The recent surface characterization of CVD-grown SnTe nanostructures indicates a rather high density of screw dislocations embedded inside the nanostructures [37], most likely formed due to fast growth kinetics. Hence, more detailed characterizations of the microstructures of topological nanomaterials using aberration-corrected (scanning) transmission electron microscopy and spectroscopy techniques are critical. Transport properties of topological nanomaterials should then be correlated with defect densities and types in order to find out the types of defects most important for transport properties. Presently, such structure–property relation studies are almost non-existent for topological surface states. For example, the scattering mechanisms of the topological surface states as a function of impurities, crystal defects or surface oxidation are all important, yet largely unknown. Detailed studies of structure–transport property relations were key in developing many of today's high-end electronic and

optoelectronic technologies. The same intense efforts must be made for topological nanomaterials.

To fully realize the potential of topological nanostructures and 1D topological superconductors, serious efforts must be dedicated to the synthesis of topological nanostructures, accompanied by detailed structural, chemical and transport characterizations. Property metrics for the crystal quality should be defined; these are often tied to specific technological applications or scientific objectives. The two most useful metrics would be the placing of the Fermi level within the bulk band gap and carrier mobilities of at least ~ 2000 cm^2/Vs for TI and TCI nanostructures. Samples exhibiting these properties will enable routine observation of quantum effects from the topological surface states in temperature and magnetic field ranges that are easily accessible in laboratories. To achieve these property metrics, which require improved material quality and controlled nanostructure morphology, understanding the growth mechanism of topological nanomaterials becomes essential. Because topological nanomaterials are often made via VLS or CVD growth methods at relatively high pressures in the presence of volatile gaseous precursors, understanding nucleation and growth is difficult. The lack of *in situ* diagnostic tools during growth contributes to challenges associated with nanostructure growth. Some laudable efforts have been made in *in situ* TEM growth studies of semiconducting nanowires catalysed with gold nanoparticles, which tried to understand VLS growth. Detailed analysis of these experiments has shown the complexity of the growth process [188-191], the control of which requires precise knowledge of chemical potentials of various reaction gases,

local growth temperature, growth pressure and the flow dynamics of reaction gases. For VLS growth, detailed understanding of the energy balance at the triple junction, the point at which the liquid metal catalyst, reaction gases and solid nanowire meet, is critical [191]. For CVD growth, its wide application to the growth of 2D transition-metal dichalcogenides has led to notable efforts in studying the growth dynamics, which incorporates flow dynamics of carrier gases and source vapours at the macroscopic scale with bonding interactions at the site of nucleation and growth at the molecular level [192-195]. The role of growth substrates and of different types of precursors and additives should also be considered carefully for CVD. The systematic growth study of TCI SnTe and its alloys as nanostructures on various substrates has shown the dramatic effect the substrate or the local chemical potential of precursors can have on the morphology of the final nanostructures [111, 112].

An additional challenge, particularly for nanowire synthesis, is the control of the nanowire diameter. In growing Bi_2Se_3 nanoribbons using a gold catalyst, the side growth from direct vapour-to-solid deposition occurs easily, widening the nanoribbon. This is undesirable for realizing 1D topological superconductors. Controlling doping is also problematic: for SnTe nanowires, the yield of In-doped SnTe nanowires with a dopant concentration high enough to induce superconductivity around 2 K remains low. Because the morphology of the nanostructures is governed by the minimization of the overall surface energy via the Wulff construction, careful investigation of the surface energies of different crystallographic facets with different atomic plane termination is important to

predict and control the nanostructure morphology. The variation of the surface energies with local chemical potentials of various source vapours will also need to be taken into consideration. Some detailed studies have been carried out for SnTe nanostructures. For example, for SnTe, the surface energies of different crystallographic planes were calculated as a function of the chemical potential of Sn or Te vapours [34, 36]. Synthesis studies can be greatly aided by theoretical simulations.

Among topological nanowires, only SnTe nanowires have been demonstrated to superconduct by indium doping. More topological nanowires should be made superconducting, so that the most suitable system for quantum computations can be found. Reproducing the induced superconductivity in metal-intercalated TI bulk crystals in narrow nanoribbons seems the next reasonable goal for the field. Recently, electrochemical intercalation of copper atoms into Bi_2Se_3 nanoribbons has been demonstrated [196]. This approach is promising to obtain doping within the narrow concentration window necessary for inducing superconductivity. Presently it is unclear whether it is intercalated copper atoms or substitutional copper atoms that donate electrons to Bi_2Se_3. Thus, the exact positions and role of copper atoms in Bi_2Se_3 should be studied, in particular in nanostructures. The observed superconductivity in monolayer WTe_2 is also promising [160, 161]. The synthesis of $MoTe_2$ and WTe_2 as nanowires and the realization of a superconducting state into these nanowires would be an exciting achievement.

Another important thing to keep in mind is that surface passivation is essential to prevent surface oxidation and to preserve the transport properties of topological surface states. Finally, the search for new topological materials that may already possess more desirable transport properties must continue. Recent theoretical works that identified thousands of topological materials are exciting, but experimentally verifying and studying these proposed materials is daunting [1, 197, 198]. More theoretical guidance to narrow the list would be most welcome.

2.5.2 Challenges in detecting surface state properties

Unlike spectroscopic techniques — like ARPES — that provide insight primarily on surface phenomena, electronic transport measurements comprise both surface and bulk contributions. Typically, transport is dominated by the large carrier concentration of the bulk, hiding the relatively miniscule contribution of the surface. This results in ambiguity in the interpretation of experimental data, as was evident in the investigation of weak antilocalization, where the number of surface Dirac cones was not clearly determined despite a clear recipe for its extraction. Hence, new types of probes are needed to unambiguously probe the surface state in transport measurements. While no clear-cut experimental method has yet been demonstrated, superconductor – TI – superconductor Josephson junctions provide a step in the right direction, showing that novel detection methods can reveal more about the surface state than conventional transport measurements.

Josephson junctions have been used to enhance the contribution of the surface state relative to the bulk in TIs like Bi_2Se_3 [133], HgTe [199], Pb-doped SnTe

[179] and Cs_3As_2[200]. The origin of this enhancement lies in the mechanism by which Cooper pairs are transferred between the adjacent superconductors in the junction. This process is facilitated by the presence of two symmetric energy levels formed by the repeated process of Andreev reflection that happens at the superconductor–weak link interface (Fig. 2-9a). These levels, called Andreev bound states, have a position relative to the Fermi energy that is dependent on the relative phase difference φ between the left and right superconductor forming the Josephson junction (Fig. 2-9b). These states depend sensitively on the transmission probability of an electron or hole in the weak link region, τ. As τ increases, the Andreev bound states vary more dramatically as φ evolves from 0 to 2π, resulting in both a larger maximum supercurrent I_S and a more skewed current-phase relation (Fig. 2-9c) [201]. Due to spin–momentum locking, surface state carriers typically have a larger value of τ than bulk carriers, hence surface electrons have both a larger maximal supercurrent and skewness of the current-phase relation. This skewness has measurable effects on the properties of the junction. For example, the skewness of the current-phase relationship results in a curve with higher harmonic content as the value of τ approaches unity. This higher harmonic content modifies the properties of the *I-V* curve under application of RF radiation, so that steps appear at quantized values (called Shapiro steps) [202]. The skewness of the current–phase relationship allows for fractional step values to appear; a measurement of the Shapiro step size can uncover contributions from highly-transmitting surface states, even in the presence of a large conducting background (Fig. 2-9d).

In addition to probing the surface state of TIs, the detection of MBSs in topological superconductors remains an important challenge in the investigation of superconducting TI and TCI nanowires. Whereas using charge transport to detect the helical mode is enticing, it suffers a drawback that plagues many of the charge transport experiments in superconducting TIs: unintentional doping of the bulk provides a large parallel conduction channel that can mask charges in electrical transport from the helical mode. This is reflected in Fig. 2-4f. The height of the conduction peak at $\Phi = \Phi_0/2$ is small, a fraction of e^2/h, whereas near the charge neutrality point a jump of e^2/h would be expected provided there is no contribution from the bulk. Further, the role of the trivial bulk carriers in charge transport remains unclear. In systems with strong spin–orbit coupling, which include TI and TCI nanowires, additional geometric phases become important in understanding the overall phase acquired by electrons encircling the magnetic field. For example, in quantum rings fabricated from a 2D electron gas with strong spin–orbit coupling, a gate-dependent shift in the conductance maximum from even to odd values of $n\Phi_0/2$ has been observed [203]. The clear detection of the helical mode is essential to move forward with generating MBSs in superconducting TI and TCI nanowires.

Experiments with superconducting strong TIs have shown that supercurrents in Josephson junctions can be more sensitive to the helical nature of the surface states than charge transport experiments[199]. This phenomenon can be enhanced by the presence of a zero mode, whereby the sequential tunnelling provided by the zero-energy mode is much more efficient than the co-tunnelling process enabled by conventional Andreev bound states. Still, to pick out a

contribution to the supercurrent of $e\Delta/h$ (which is 10 nA for aluminum leads) on top of a background that is 10^2 to 10^4 times larger can be difficult. A path forward might be provided by thermal transport: MBSs, being electrically neutral, naturally lend themselves to thermal transport. Theoretical work has demonstrated that a transition from a trivial ($\Phi = 0$) to a topological phase ($\Phi = \Phi_0/2$) is accompanied by a peak in the thermal conductance with a disorder-immune height of $G = G_Q$, the quantum of thermal conductance [204]. This technique has recently been used to explore the non-Abelian properties of the 5/2 quantum Hall state [205]. Although small, the thermal conductance arising from MBSs is expected to be dominant at low temperatures and within experimentally accessible values (Fig. 2-8d, e). Thermal transport may be the next breakthrough for work in topological superconductivity in strong TI nanowires.
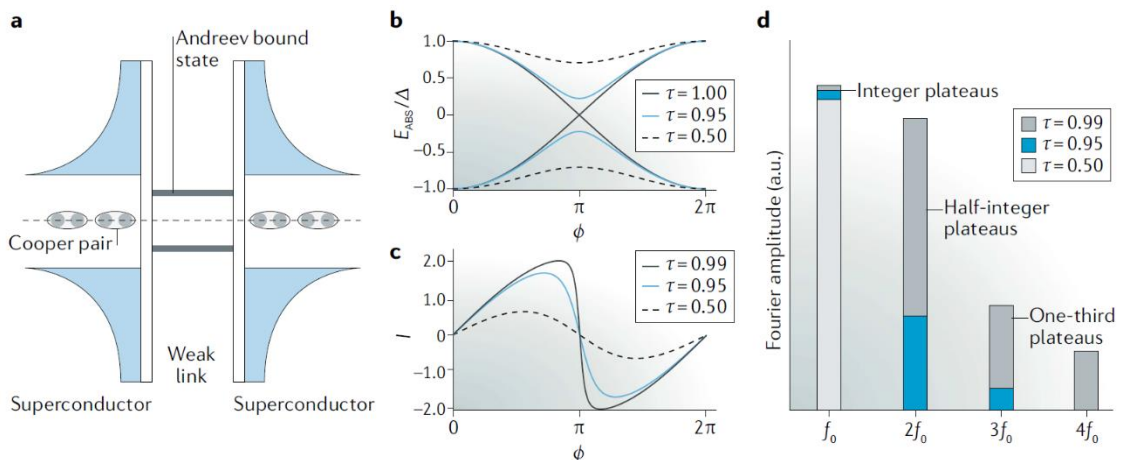
Figure 2-9: Josephson junctions

a, Schematic of a weak- link Josephson junction. A weak link made of conducting material facilitates transfer of Cooper pairs between two superconductors. **b,** Dependence of the Andreev bound states (ABSs) on the phase difference φ between the two superconductors for different values of the transmission probability τ, governed by the equation $E_{ABS} = \pm\Delta\sqrt{(1 - \tau \sin^2(\varphi/2))}$, where Δ is the size of the superconducting gap induced in the junction. **c,** Resulting current–phase relation for different values of τ. **d,** Varying harmonic content of the current–phase relation as a function of τ. Higher harmonic content results in the appearance of fractional (Shapiro) steps in the I–V (current–voltage) curve.

2.6 Conclusions

Since the inception of band topology for condensed matter systems, the field of topological materials has grown greatly, with recent theoretical works suggesting that ~ 25% of all the materials we know may be topological in nature [206]. Studying them in nanostructures is important for potential device applications, such as topological field-effect transistors with fast switching, low-power topological magnetic memory devices, and low-dissipation interconnects. The most attractive potential application for topological nanostructures is as qubits for robust quantum computers based on 1D topological superconductors; superconducting strong TI and TCI nanowires have been the most studied material candidates so far. Experimentally, much work is left, spanning from improving crystal quality and controlling the morphology of the topological nanostructures to developing transport measurement schemes that can overcome some of the limitations of charge-only transport measurements. Having witnessed the remarkable progress in the last decade in the field of topological materials, both theoretically and experimentally, it is exciting to imagine what lies ahead, particularly for topological nanomaterials.

Chapter 3: Dislocation-Driven SnTe Surface Defects During Chemical Vapor Deposition Growth

TCI SnTe has attracted growing interest due to its promise for spintronics and quantum computing applications. Because the topological protection stems from the crystal symmetry for TCIs, crystal defects on the surface of SnTe can strongly influence the topological phases and transport properties. The goal of this work is, therefore, to unveil the origin and evolution of surface defects, such as pits, open cores and steps, observed on SnTe microcrystals and nanostructures synthesized by CVD. We find that surface pits originate from different types of dislocations in SnTe crystals. Enlarging, deepening, and faceting of surface pits occur by sublimation of open cores and movement of steps during the cooling process of the CVD growth. In contrast, open cores and steps on surfaces form during growth. Surface crystal symmetry, surface polarization and growth conditions contribute to distinct morphologies of the observed surface pits. We show that a fast cooling, instead of the natural cooling, can suppress the formation of surface pits on the SnTe crystals. To decrease the number of open cores and steps on {100} and {111} surfaces of the SnTe microcrystals and nanostructures, the CVD growth conditions need to be further optimized.

The following chapter first appeared[37] as Dislocation-driven SnTe surface defects during chemical vapor deposition growth. *Journal of Physics and Chemistry of Solids,* **2019**, 128, 351-359.

Authors: Pengzi Liu, Yujun Xie, Eric Miller, Yuta Ebine, Piranavan Kumaravadivel, Sungwoo Sohn, Judy J Cha

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3.1 Background and Motivation

TIs [6, 15, 207, 208] and TCIs [5, 30] possess unique conducting surface states that arise due to large spin-orbit coupling. Protected by time-reversal symmetry or crystal symmetry, the spin-polarized surface states of TIs and TCIs can be exploited to develop spintronic devices [209] and to implement MBSs [28, 210], allowing realization of topological quantum computing. Currently, TIs and TCIs suffer from high bulk conductivity due to point defects, such as vacancies, antisites, and interstitials, which serve as charge dopants [116, 33]. On the other hand, symmetry-breaking dislocation lines in TIs are predicted to create robust topological modes, which can dominate spin and charge transports of the overall system [211, 212]. Therefore, to control and tune topological phases it is important to investigate how point defects, dislocations, surface topography and transport properties correlate with each other.

As a first predicted TCI, SnTe has been extensively studied to explore the physics and applications of the surface states both theoretically and experimentally[32, 117, 34, 38, 35, 213, 36]. SnTe surface states exist on highly symmetric crystal planes of the face-centered-cubic (FCC) crystal lattice including {100}, {110} and {111}. High concentrations of Sn vacancies inhibit the surface states to be easily revealed by transport measurements [41, 42, 43]. As dislocations can be sources or sinks for point defects during crystal growth [44, 45, 46], studies that focus on formation and evolution of dislocations in SnTe crystals may be critical in order to reduce the high bulk carrier densities. This requires careful investigations of the crystal growth of SnTe, which remain challenging for nanoscale crystals, such as nanoribbons and nanoplates grown by CVD. Experimental studies have investigated SnTe micro- and nanocrystals grown by the VLS and vapor-solid (VS) growth with and without gold as the growth catalyst [33, 32, 117, 34, 38, 214, 215, 216]. In general, microcrystals form primarily via the VS growth mechanism [32, 34, 38] while nanoplates and nanoribbons form via both the VS and VLS [32, 117], and nanowires via the VLS mechanism [32, 34, 38, 214, 215, 216]. Effects of surface energies and growth conditions on the morphology and facet formation of SnTe microcrystals were also examined. Under a Te-rich environment [34, 36] or low growth temperatures [38], a SnTe microcrystal can deviate from the thermodynamically stable octahedron shape, which is surrounded by eight {100} planes, because the Te-terminated {111} surface has a lower surface energy than the {100} surface. Despite several crystal growth studies however, detailed studies on possible surface defects on SnTe nanostructures grown via VLS and VS methods are lacking, which is

important as the topological surface states could be modulated by surface defects in SnTe.

In this work, we aim to demonstrate the origin and evolution of 3D surface defects commonly observed on SnTe microcrystals and nanostructures synthesized by the CVD method. In addition to SnTe, In-doped SnTe was recently rediscovered as a possible candidate for a time-reversal-invariant topological superconductor (TSC) [117, 168, 173, 119]. The superconducting transition temperature of $In_xSn_{1-x}Te$ increases with the increasing doping concentration of indium, x [41, 168, 173, 119]. Thus, influence of indium doping on morphologies of surface pits is also discussed. We classify surface defects by careful characterization of the surface topography of SnTe micro- and nanocrystals with surface-sensitive scanning electron microscopy (SEM) operated at low electron voltage. *In-situ* heating SEM experiments show that open cores, surfaces steps and pits form at different stages during CVD growth. The observed surface pits originate from dislocations based on cross-sectional transmission electron microscopy (TEM) and can be suppressed by fast cooling.

3.2 Materials and Methods

3.2.1 CVD synthesis of SnTe and In-doped SnTe microcrystals and nanostructures

SnTe   and   In-doped   SnTe microcrystals and nanostructures were synthesized in a horizontal tube furnace with a single temperature zone

(Lindberg/Blue M, Thermo Fisher Scientific, Fig. 3-1a). A mixture of 0.1 g SnTe powder (Sigma Aldrich, 99.999%) and 0.1 g Sn powder (Sigma Aldrich, 99.8%) was finely ground and placed in a quartz boat. The boat with precursors was placed at the center of a quartz tube with 1-inch diameter. The Sn powder was added to the precursors to create a Sn-rich environment during synthesis and to restrict the formation of Sn vacancies in SnTe crystals. Four Si substrates covered with 20 nm Au nanoparticles (Sigma Aldrich, Prod. # 741965) were used as growth substrates. We chose Si substrates instead of mica or 300 nm SiO_2/Si substrates because, for surface defect inspection using a low-voltage SEM, the charging issue induced by non-conducting substrates can degrade imaging conditions greatly in SEM. The Si substrates were first treated with a poly-L-Lysine solution (Sigma Aldrich, 0.01%), followed by blow-drying using pure nitrogen gas. Then a solution containing 20 nm Au nanoparticles were drop-casted on the substrates and blow-dried in 2 min. The growth substrates were placed at downstream inside the quartz tube at distances 10.5 cm–13.5 cm away from the center of the furnace. The quartz tube was sealed on both ends and purged with ultra-high purity argon gas (99.999%) for 5 times in order to exhaust air in the whole system. During the synthesis, pressure in the tube was maintained at 2 torr by feeding a constant Ar flow at a rate of 20 sccm. The center temperature of the furnace was held at 843 K for 1 h growth time after ramping the temperature from room temperature to 843 K within 30 min. After growth, the furnace was allowed to naturally cool down to room temperature (natural-cooling process) or finished with fast-cooling process as described later in this chapter. The micro- and nano-crystals we discuss in this

chapter were obtained from the substrate placed at 11.5 cm from the center. Representative morphologies of SnTe nanocrystals are presented in optical microscope images showing the SnTe nanowire (Fig. 3-1b), nanoribbon (Fig. 3-1c) and nanoplate (Fig. 3-1d).
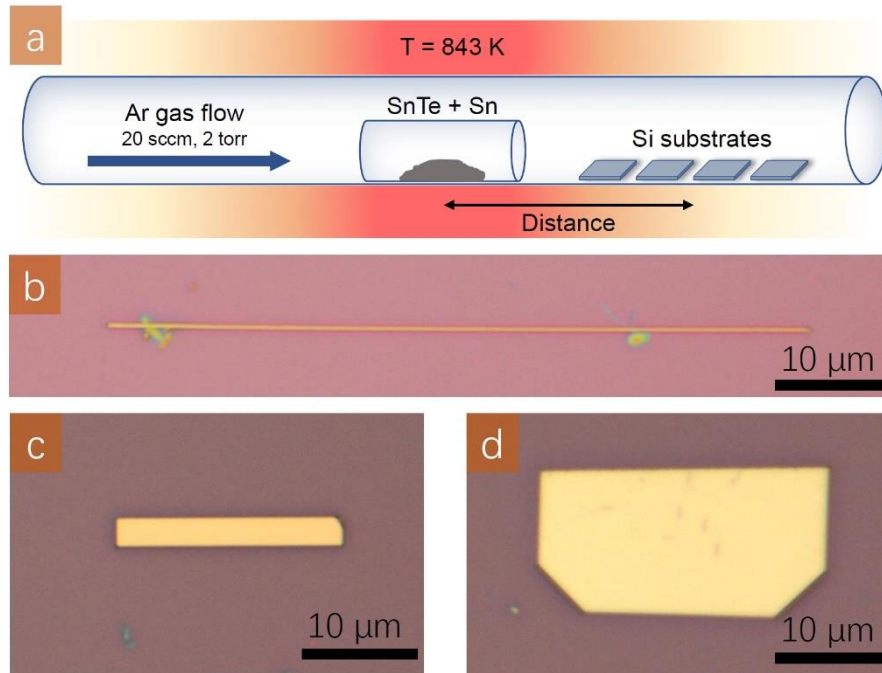
Figure 3-1: Synthesis and characterization of SnTe nanostructures

a, Schematic illustration of the quartz tube setup for CVD synthesis. Optical microscope images of as-grown SnTe nanostructures transferred to SiO_2/Si substrates with different morphologies: **b**, nanowire, **c**, nanoribbon, and **d**, nanoplate. Reproduced with permission from[37] P. Liu, et al. Journal of Physics and Chemistry of Solids. © 2017 Elsevier Ltd. All rights reserved.

Different from the synthesis of SnTe nanocrystals, precursors for the synthesis of In-doped SnTe nanocrystals consisted of 0.15 g InTe (Sigma Aldrich, 99.999%), 0.06 g SnTe (Sigma Aldrich, 99.999%) and 0.09 g Sn powder (Sigma Aldrich, 99.8%). A constant Ar flow rate of 200 sccm and pressure of 7.6 ± 0.2 torr were kept during growth. The center temperature stayed at 873 K for 10 min after

ramping from room temperature within 30 min. The temperature profile of the tube furnace measured by an external thermocouple is included in Appendix A (see Fig. A-2).

3.2.2 SEM imaging of SnTe and In-doped SnTe microcrystals and nanostructures

Surface defects of the SnTe and In-doped SnTe micro- and nanocrystals were characterized by SEM (Hitachi SU8230 cold field emission SEM operated at 1 kV–10 kV). Since electron beams with low accelerating voltages are more sensitive to surface topography, low accelerating voltages of 1–10 kV were used to reach the best imaging condition for imaging surface defects. Comparisons of SEM images taken at various acceleration voltages are provided in Appendix D (Fig. D-1).

3.2.3 *In-situ* SEM annealing experiments

A solution containing SnTe microcrystals and nanoplates was prepared for *in-situ* SEM annealing experiments as follows. Si substrates with freshly synthesized SnTe microcrystals and nanostructures were soaked in 2-Propanol (≥99.5%, Fisher Chemical) and sonicated for 10 min to obtain a solution with fragments of SnTe microcrystals and nanoplates. *In-situ* annealing experiments were performed on a Protochips Aduro heating holder accompanied with a Protochips Aduro thermal E-chip having a 50 nm Si_3N_4 (E-AHA11) support membrane. The chip is equipped with a micro-electro-mechanical system (MEMS) to electrically heat up the sample during annealing. We cast drops of the solution

onto a thermal chip fixed on the heating holder and allowed it to dry naturally in minutes. The *in-situ* experiments were carried out in a Hitachi S-3400 Variable Pressure SEM operated at 5 kV. During *in-situ* heating, the temperature was controlled by the Protochips computer software. The temperature was gradually ramped from room temperature to 673 K.

3.2.4 Sample preparation using FIB-SEM and cross-sectional TEM imaging

A SnTe microcrystal with rectangular pits and open cores on its (001) plane was chosen for cross-sectional TEM characterization. The sample was prepared using a FEI Helios NanoLab 660 SEM/FIB. A lamella with the thickness of ~120 nm and the side length of ~12 μm was lifted out from the original microcrystal and attached to a TEM copper grid. Its cross-sectional surfaces were terminated with {110} planes. Bright field (BF) TEM imaging was performed on a 200 kV FEI Tecnai Osiris TEM at an accelerating voltage of 200 kV. Two beam conditions taken along a diffraction vector of $\mathbf{g} = [001]$ were applied to characterize dislocations in the FIB-milled sample of a SnTe microcrystal.

3.3 Results and Discussion

The surface crystallographic orientations of the SnTe nanostructures were indexed by analyzing the facet angles of the surfaces. For example, due to the FCC lattice structure, the side facet angles of {100} surfaces are 45°, 90°, or 135°, while those of {111} surfaces are 30°, 60° or 120° [32]. Thus, surfaces with rectangular defects are identified as {100} planes as shown in Fig. 3-2a–e, while triangular facets, shown in Fig. 3-3, are {111} planes.
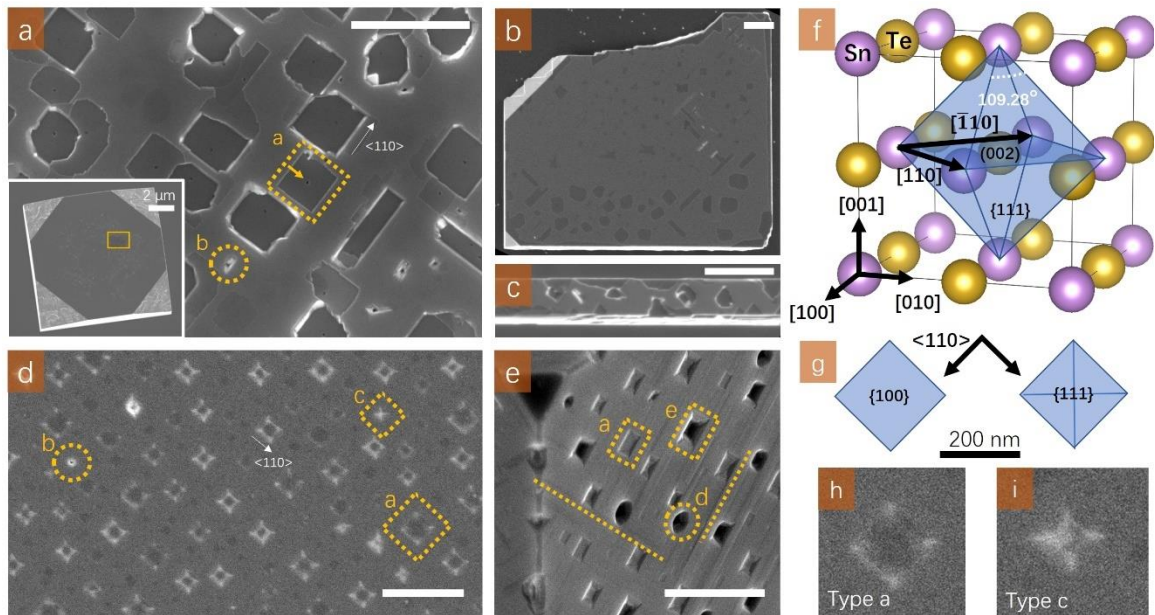
Figure 3-2: Characterization and classification of surface pits on SnTe and In-doped SnTe {100} surfaces

Surface pits on SnTe (001) surfaces are presented in SEM images of **a,** microcrystal, **b,** nanoplate, and **c** nanowire. The imaging area in **a** is highlighted in inset. Surface pits on In-doped SnTe {100} surfaces are presented in images **d** and **e**. Various types of pits are marked as "a" (truncated rectangular pits), "c" (inverted pyramidal pits), "d" (deep pits with irregular shape) and "e" (deep rectangular pits). Open cores are labeled with "b", and pointed out by an arrow in (a). Surface steps along <110> directions are highlighted in **e**. **f** The FCC crystal structure of SnTe. **g,** Illustration diagrams for plan views of pit "a" (left) and "c" (right), corresponding SEM images are shown in **h** and **i**. Scale bar is 500 nm unless labeled. Typically, with 1-h growth time, thicknesses of the SnTe nanoplates range from 300 to 500 nm.
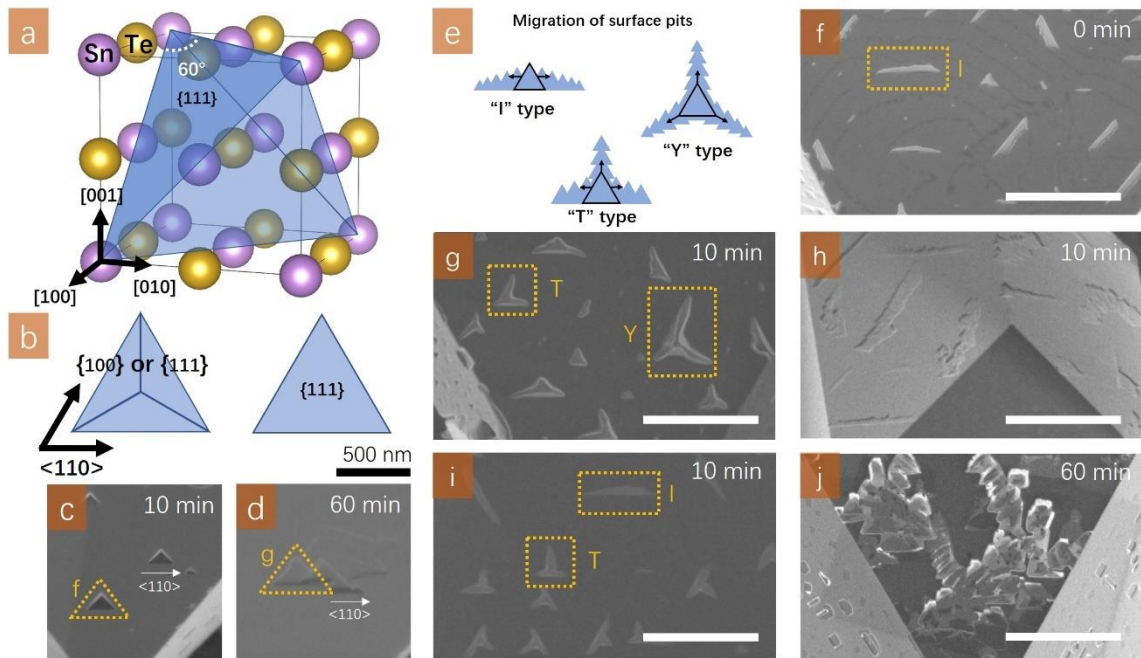
Figure 3-3: Characterization and classification of surface pits on SnTe {111} surfaces.

a, The FCC crystal structure of SnTe. **b**, Illustration diagrams for plan views of pit "f" (left) and "g" (right); corresponding SEM images are shown in **c** and **d**. **e**, Pit patterns "I", "T" and "Y" formed by migration of triangular surface pits; corresponding pit patterns are marked in **f**, **g**, and **i**. The original pits are highlighted by black frames and black arrows indicate migration directions. SnTe microcrystals are synthesized with different growth time **f,** 0 min, **g-I,** 10 min, and **j**, 60 min. Scale bar is 2 μm in **f-j** unless labeled.

3.3.1 Classification of surface pits on {100} surfaces

Surface topography of (001) planes on SnTe microcrystals, nanoplates, and nanowires was examined by SEM to observe surface pits, as shown in Fig. 3-2a–c. Rectangular pits denoted as "a" are observed on SnTe microcrystals with their sides parallel to the sides of {111} facets along <110> directions (Fig. 3-2a). In addition, open cores surrounded by small defective regions can be found on the (001) surface plane, marked as "b" (Fig. 3-2a). On SnTe nanoplates (Fig. 3-2b) and nanowires (Fig. 3-2c), the shapes of the surface pits appear irregular with the directions of pit sides randomly oriented. We believe that surface pits exist on all

{100} planes as exhibited on surfaces of SnTe nanowires (Fig. 3-4). We also find that only the type "a" pits appear on the surfaces of SnTe crystals regardless of growth conditions (see Table 3-1 and Table 3-2).
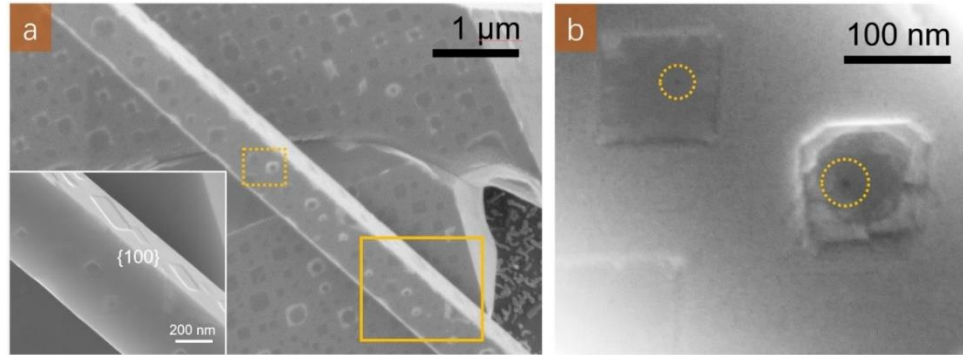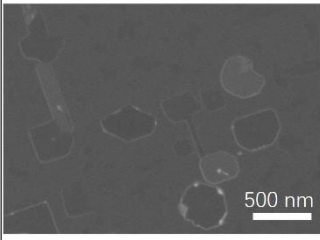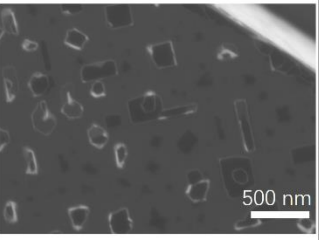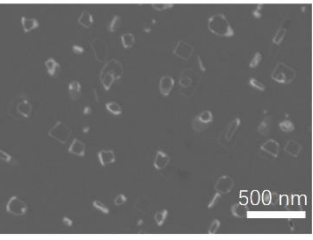
Figure 3-4: Rectangular pits on {100} surfaces of a SnTe nanowire

a, A SEM image showing a SnTe nanowire. In inset, surface pits can be observed on two {100} planes highlighted by solid lines in **a**. **b**, Rectangular pits associated with open cores circled by dashed lines. The imaging region of **b** is marked by dashed lines in **a**.

Table 3-1: SEM images of surface pits on {100} planes of SnTe samples synthesized with different growth conditions

With the same growth temperature (843 K), flow rate (200 sccm) and pressure (7.6 Torr), the density and depth of surface pits decrease with decreasing growth time (60 min, 30 min, and 0 min). With the same growth temperature (843 K) and growth time (1 hour), the density and size of surface pits seems to decrease with decreasing flow rate and pressure. Only the "type a" surface pits are observed in all growth conditions.

Growth Temperature	843 K	813 K	783 K
SEM Images	500 nm	500 nm	500 nm

Table 3-2: SEM images of surface pits on {100} planes of SnTe samples synthesized at different growth temperatures

With the same flow rate (200 sccm), pressure (7.6 Torr) and growth time (1 hour), surface pits become smaller at lower growth temperatures.

Pit formation can be promoted by suppression of local crystal growth as a consequence of impurity segregation around dislocation cores with large strains [217]. In the case of SnTe microcrystals, no foreign dopants or impurities were introduced to precursors. To study the influence of dopants on surface defects, we grew indium-doped SnTe microcrystals, which resulted in additional surface pits, labeled as 'c' and 'd' as shown in Fig. 3-2d–e. On the (001) plane of the In-doped SnTe microcrystal, edges and corners of the surface pits show higher intensity, which is due to the edge effect in SEM imaging and In segregation, which was discussed in our previous work [119]. In Fig. 3-2d, the pit labeled as "c" is found to be an inverted pyramidal shape, with a square opening faceted with four {111} planes and a pointed bottom. Moreover, on the tilted (001) plane (Fig. 3-2e), "a" pits having truncated bottoms rather than pointed bottoms are commonly observed. The non-rectangular shape of a deep pit "d", and the drastic change of contrast in the center of the rectangular pit "e" indicate that they are distinct from type "a" and

type "c" pits. In addition to the various types of surface pits and open cores, steps

and terraces are also observed on the tilted (001) plane in Fig. 3-2e. Fig. 3-2f is

the schematic diagram of the SnTe rock-salt structure. From the crystal symmetry,

the sides of the rectangular pits are found to be along the <110> directions, hence

the rectangular pits correspond to the octahedron bounded by eight {111} planes,

as illustrated in a blue shade cut by a (002) plane in Fig. 3-2g. Accordingly, the

shape of rectangular or square pits is determined by the (002) plane that cuts the

octahedron. Fig. 3-2h and 2i shows the morphology of the surface pit type "a" and

"c" at a larger magnification. Pit "a" corresponds to a truncated half-octahedron

(Fig. 3-2h) while pit "c" is related to a full half-octahedron (Fig. 3-2i).

3.3.2 Classification of surface pits on {111} surfaces

In addition to the {100} planes, we also observe two types of surface pits on

the {111} planes of the SnTe microcrystals synthesized with different growth times.

Typical examples of triangular pits having sides in the <110> directions on {111}

planes are presented in Fig. 3-3c and d. Similar to the rectangular pits on {100}

planes, the geometry of surface pits on {111} planes is determined by the crystal

symmetry in corresponding orientations. Therefore, as depicted in the plan view of

the pits (Fig. 3-3b), the triangular pit denoted as "f" in Fig. 3-3c has a triangular-

cone morphology with three sidewalls on either {111} or {100} planes,

corresponding to the tetrahedron shaded in blue (Fig. 3-3a), or a corner cut by a

{111} plane in the cubic structure. The triangular pit marked as "g" in Fig. 3-3d

corresponds to a truncated tetrahedron having a flat bottom terminated with a {111}

plane. We note that the contours of these pits deviate from equilateral triangles because the samples were imaged with tilted angles.

Since slip (or glide) easily occurs on {111} planes, individual surface pits can migrate along the <110> directions, leading to complicated pit patterns shown in Fig. 3-3f–j. As a result, triangular pits prefer migrating in slip directions and settle in various shapes, instead of remaining as isolated triangular pits on {111} surfaces. In our notation, "I", "Y" and "T" refer to new types of pits produced by slip in one, two and three <110> directions (opposite directions are counted as one), respectively (Fig. 3-3e–i).

The effect of growth time on the morphology of surface pits is inferred from comparing pit patterns on different SnTe {111} surfaces. For instance, triangular-cone pits, type "f", were only found on {111} surfaces of SnTe synthesized with growth time shorter than 10 min. Growth time is defined as the time period between the instant that the target temperature for growth is reached and the beginning of the cooling process. Compared with zero growth time (Fig. 3-3f), 10-min growth allows more types of pit patterns on {111} surfaces (Fig. 3-3g, i). With growth time up to 60 min, {111} surfaces are highly defective and dominated by random patterns generated by migration of triangular pits with flat bottom (Fig. 3-3j).

We note that the observed surface pits on {100} and {111} surfaces of the SnTe microcrystals and nanostructures are not isolated in our growth, but also found in other CVD-grown SnTe microcrystals [38].

3.3.3 Suppression of surface pits with fast cooling

We found that the cooling process of the CVD growth of SnTe can control the surface topography of SnTe microcrystals (Fig. 3-5a, d), nanoplates (Fig. 3-5b, e), and nanowires (Fig. 3-5c, f). Fig. 3-5a–c and d–f correspond to two growth cases with the same growth conditions described previously, but with different cooling processes. Sample A (Fig. 3-5a–c) was taken out of the furnace after natural cooling. For sample B, the furnace was opened when the center temperature of the furnace dropped to 840 K, then the temperature further decreased to 353 K in 8 min assisted by a fan (i.e. fast cooling). Natural cooling takes 4.5 h to reach room temperature. Thus, the cooling rates of the natural and fast cooling are ~2 and 61 K/min, respectively. It's worth noting that, during the natural/fast cooling process, a constant Ar flow rate of 200 sccm and pressure of 7.6 ± 0.2 torr were kept.
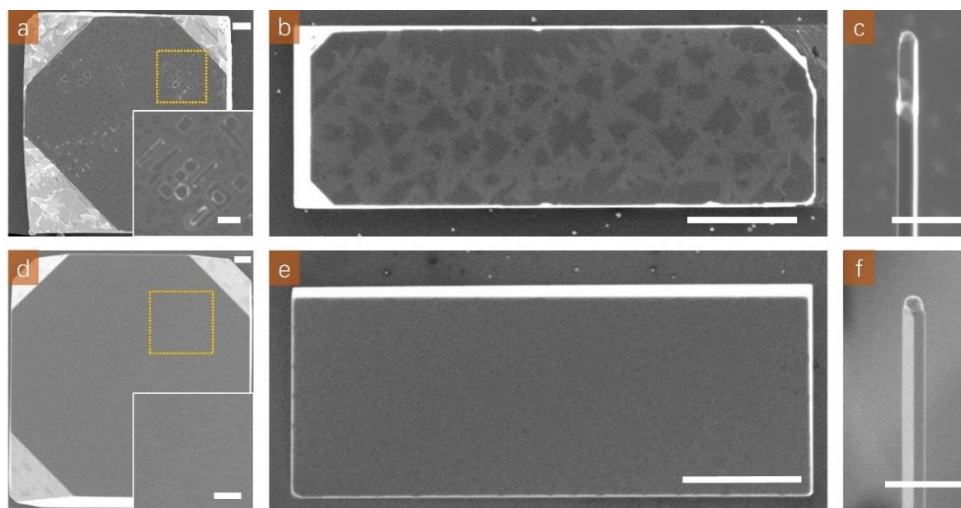
Figure 3-5: Comparison of surface topography between SnTe micro- and nanocrystals synthesized with two different cooling processes

a, b, c, A SnTe microcrystal, nanoplate, and nanowire synthesized with natural cooling. **d, e, f,** A SnTe microcrystal, nanoplate, and nanowire synthesized with fast cooling. Scale bar is 1 μm in **a-f**, and 500 nm in inset.

The Ar flow was found to be independent of the suppression of surface pits as shown in Fig. 3-6.
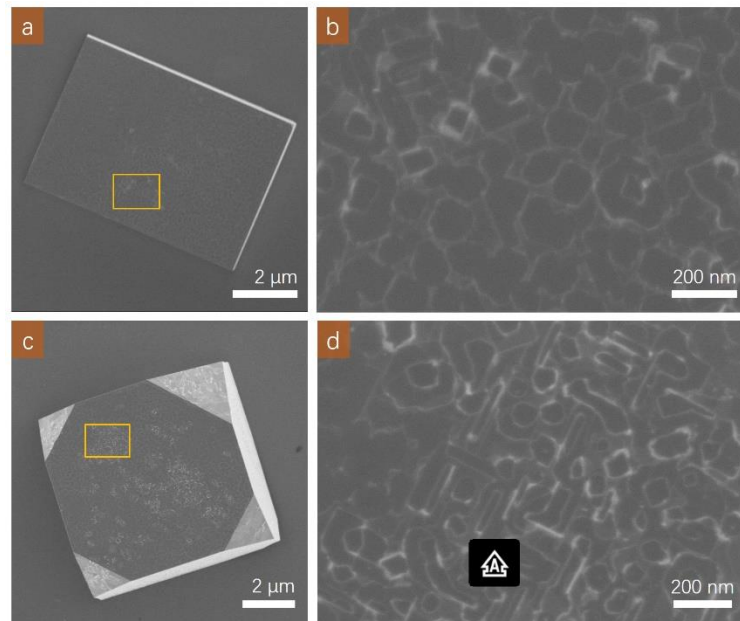
Figure 3-6: SEM images of surface pits on {100} planes of SnTe samples synthesized without Ar flow during natural cooling

a, c, A SnTe nanoplate, and microcrystal synthesized without Ar flow during natural cooling. Defective {100} surface planes on the SnTe **b** nanoplate and **d** microcrystal are observed. The imaging regions in **b** and **d** are marked by yellow boxes in **a** and **c**, respectively.

Visual comparison between the two samples reveals the striking suppression of the surface pits facilitated by the fast cooling. Inset in Fig. 3-5a shows typical square pits on {100} surfaces of SnTe microcrystals, and contrast variations on the surface of the SnTe nanoplate in Fig. 3-5b indicate changes in surface height. On the contrary, no noticeable surface pits are found in SEM images of sample B (Fig. 3-5d–f) although tiny holes are still observed on the surface as shown in Fig. 3-5d. Thus, we conclude that the surface pits form during the slow cooling after the CVD growth. We hypothesize that the slow cooling promotes sublimation in the grown SnTe crystals. In the natural cooling process, it

is possible that the growth substrate temperature is still high enough for sublimation of the SnTe crystal surfaces. This sublimation cannot be compensated by the source vapor that is no longer present as the furnace is turned off thus creating surface pits. With fast cooling, the sublimation time is drastically reduced, resulting in much less surface pits. The pristine surface morphology of sample B (Fig. 3-5d–f) supports our hypothesis.

To verify our hypothesis, we performed *in-situ* annealing experiments inside a SEM to directly track the sublimation process of SnTe microcrystals. We prepared a SnTe nanoplate sample that was grown with fast cooling such that initially no surface pits were present. In Fig. 3-7a, a few surface pits are visible on the (001) plane of the SnTe nanoplate at an early stage of annealing. At the critical temperature near 513 K, surface pits begin to form rapidly (Fig. 3-7b). The surface pits continue to enlarge and merge together (Fig. 3-7c), which is attributed to sublimation. Further raise in temperature causes more rapid sublimation of the SnTe nanoplate (Fig. 3-7d–f). A similar sublimation behavior is observed on {111} surfaces of a SnTe microcrystal as shown in Fig. 3-8. The triangular shapes of the surface pits indicate that the surfaces of the SnTe crystal are terminated by {111} planes. Initially, the surface of the SnTe microcrystal appears pristine (Fig. 3-8a). At 603 K, triangular surface pits appear (Fig. 3-8b) and grow (Fig. 3-8c). The pits coalesce (Fig. 3-8d) and the surface of the crystal continues to be etched away (Fig. 3-8e–h).

1 µm
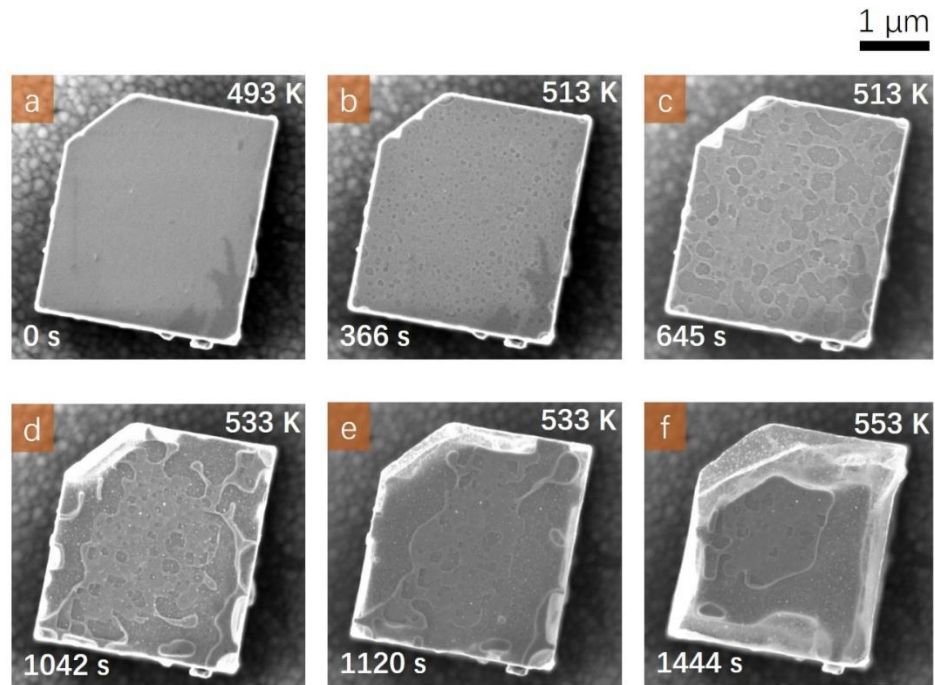
Figure 3-7: SEM images showing sequence of pit formation process on a (001) surface during the *in-situ* heating experiment.

Annealing temperatures are provided at the upper-right corner of each image. **a,** A few pits are found on the (001) surface at 493 K initially. **b,** At 513 K, pits rapidly emerge on the (001) surface. **c,** Surface pits enlarge and merge together. With higher annealing temperatures, the (001) surface is further deformed as shown in **d-f**. The nanoplate was heated from room temperature to 513 K at a heating rate of 10 K/min.

1 µm
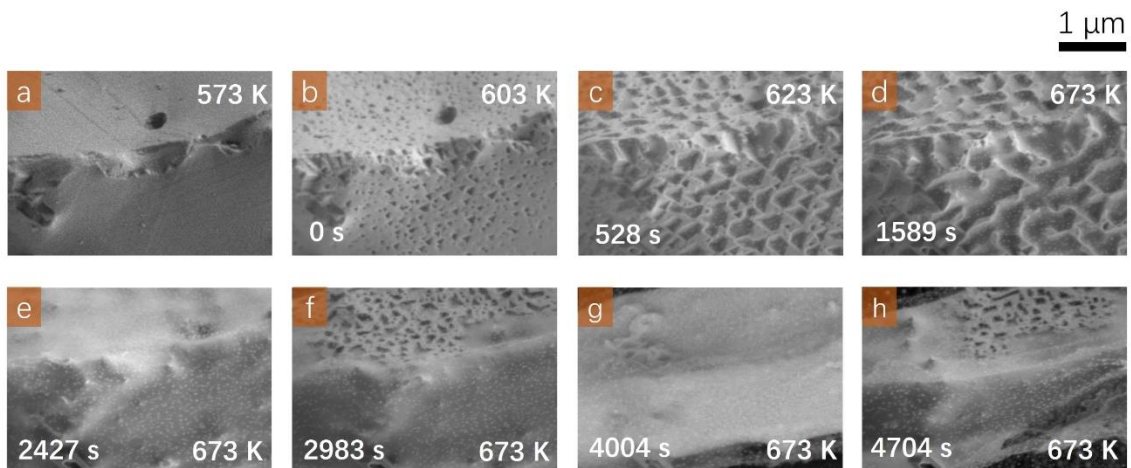
Figure 3-8: SEM images showing sequence of pit formation process on {111} surfaces during the *in-situ* heating experiment.

a, No noticeable pits are found on the {111} surfaces. **b,** At 603 K, triangular pits emerge on {111} surfaces. **c,** Surface pits enlarge and merge together. **d,** At higher annealing temperature, the {111} surface is further deformed and etched away. **e-h,** At 673 K, pits in random shapes appear and

disappear repeatedly on one of the crystal surfaces. The microcrystal was heated from 573 K to 673 K at a heating rate of 10 K/min.

The *in-situ* SEM annealing experiments confirm our hypothesis that the surface pits form due to sublimation during the natural cooling process after the CVD growth. This is similar to the widely known chemical and thermal etching that have been used to expose dislocations buried under surfaces of various crystals including CdTe, GaN, Ga_2O_3, and gypsum [218, 219, 220, 221, 222, 223]. The characteristic etch pits were found to be associated with the underlying crystallographic symmetry, and were connected to specific types of dislocations with Burgers vectors in and out of plane. In fact, the natural cooling process in CVD growth can be regarded as thermal etching. During cooling, the temperature in the furnace might be high enough for a grown crystal to sublime while not sufficiently high enough for precursors to vaporize. The hot carrier gas flowing through the quartz tube can further assist the sublimation during cooling. Therefore, the observed SnTe surface pits belong to etch pits and should be connected to dislocations in the SnTe crystals.

3.3.4 Origin and evolution of the surface pits during CVD synthesis

In Frank's model, dislocations with large Burgers vectors intersected with crystal surfaces will generate open cores at free surfaces in order to balance the elastic energy stored in the strained area with the surface energy [224]. With a higher magnification, we can find black spots with a uniform diameter of about 30 nm on the (001) surface of a SnTe nanoplate grown with the fast cooling (Fig. 3-9a). These black spots are likely the open cores originating from dislocations as

predicted by Frank's theory. Because the size of the open cores is determined by the magnitude of the Burgers vectors [224], open cores with small Burgers vectors might be too small to be resolved using a SEM. Thus, the density of the open cores observed via SEM imaging represents a lower bound for the dislocation density. Dislocations have been studied in detail for GaN [219], [220], [221], while still void for CVD-synthesized SnTe microcrystals and nanostructures. Frank's theory argues that open cores that stem from dislocations are generated during crystal growth, instead of during cooling. This agrees with our observation of open cores on the (001) plane of the SnTe microcrystal grown with the fast cooling. During natural cooling, these open cores serve as nucleation centers for sublimation [225], which create surface pits in the neighboring area. Thus, the observed surface pits should contain open cores. Indeed, the surface pits on {100} surfaces are always associated with small open cores, as pointed out by an arrow in Fig. 3-2a. All the surface pits in Fig. 3-2a have open cores at the center.
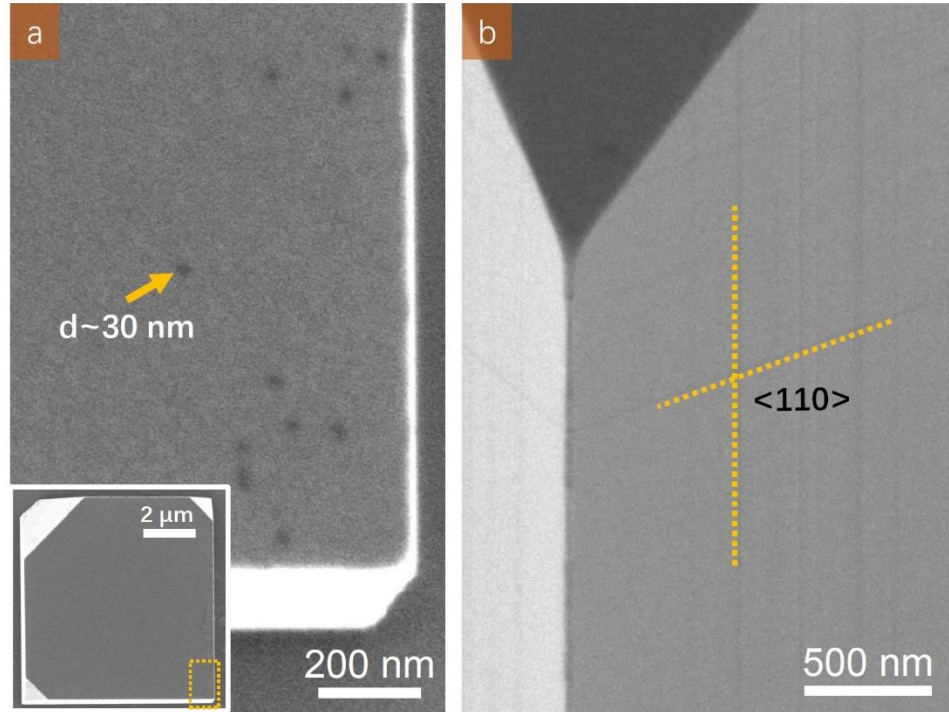
Figure 3-9: SEM images of open cores and steps on surfaces of SnTe microcrystals

a, Higher magnification image showing the region highlighted in inset. Black spots with diameter of ~30 nm correspond to open cores on the (001) surface. **b**, Surface steps highlighted with dashed lines in the <110> directions.

The formation of open cores is believed to be dominated by thermodynamics while the formation of surface pits is dominated by kinetics [220]. When SnTe crystals grow, formation of the open cores is a thermodynamic-equilibrium process that balances the elastic energy retained by dislocations with the energy of resulting free surface. During cooling, the size and shape of surface pits are governed by species of dislocations and surface energies. Generally, truncated pits are produced by screw-dislocations and inverted pyramidal pits reflect edge-dislocations or mixed-dislocations [219, 221]. Consequently, rectangular

pits "a" and "c" and triangular pits "f" and "g" might be characterized with different types of dislocations.

In our case, dislocations in the SnTe microcrystals and nanostructures do not stem from lattice mismatch between the substrate and crystals, because surface pits are observed on not only microcrystals but also on each {100} facets of nanowires, which either have small or no contact areas with the substrate. Molecular dynamic (MD) simulations have studied nucleation and propagation of dislocations during crystal growth. Liu et al. [226] argued that the relaxation process following the ejection of an atom at a surface step might lead to nucleation and propagation of a dislocation with a Burgers vector in or out of plane. In another case [227], MD methods were applied to simulate dislocations rooted in thermal misfit for FCC crystals. Squeezed-out tetrahedron clusters of atoms and non-stop ejection of atoms on crystal surfaces can induce irreversible local disorders, which later can develop into dislocations to relax the strain. It is thus possible that dislocations in the CVD-synthesized SnTe originate from depositions of adatoms from vapor environment. Growth conditions, such as temperature ramping rate, growth temperature, growth time, etc., can therefore influence the density and species of dislocations in conjunction with surface pits.

During crystal growth via vapor deposition, surface steps are energetically preferable sites for adatoms to be attached [224, 228]. Thus, step movements are likewise expected to control kinetics of the inverse process of deposition, namely, sublimation. On a SnTe microcrystal, the {100} surfaces have steps along two <110> directions, and terraces between adjacent steps (Fig. 3-9b). It is known that

slip lines are parallel to the <110> directions for FCC crystals, resulting in formation of surface steps on {100} and {111} surface planes during CVD growth. Subsequently, the anisotropic step movements combined with variations in local surface topography contribute to deepening and enlarging of surface pits [223].

Although steps move isotopically along all <110> directions on free surfaces, they tend to slow down when they encounter the surface pit regions. Compared with defective areas that surround the open cores, free surfaces are etched more slowly in the vertical direction. On the other hand, steps piling up around the surface pits increase the step density, and further inhibit step movements. Both aspects facilitate deepening and enlarging of the surface pits. Because enlarging of the surface pits is dominated by the step movements, the directions of the pit sides should reflect the orientations of step movements along the <110> direction, which is the case as shown in Fig. 3-2 and Fig. 3-3.

Faceting of pits is thought to be a kinetic process guided by minimization of the total surface energy. Sublimation would be initiated in defective areas on surfaces [220], leading to formation, expansion and deepening of surface pits around open cores. To demonstrate the above argument, we will introduce the Gibbs-Wulff construction of single crystalline SnTe, which confines the equilibrium shape of crystals with the lowest overall surface energy. In contrast to {100} and {110} planes, {111} planes hold unpaired Sn or Te atoms so that the {111} surfaces are polarized as either Sn-terminated or Te-terminated. Moreover, the surface energy can likewise be tuned through reconstructions of polarized {111} surfaces. With energetic information calculated [34, 36] for low-index surfaces of SnTe, {100} and Te-

terminated {111} surfaces are predicted to have the lowest energies near Sn-rich and Sn-poor limits, respectively. In practice, the cooling process after growth is a non-equilibrium process so that faceting of the surface pits consists of competitions between {100} and {111} surfaces.

3.3.5 Dislocation-driven surface pits during CVD synthesis

Here, we examine the cross-section of rectangular pits on a {100} surface of a SnTe microcrystal using TEM under two beam conditions taken along a diffraction vector of $\mathbf{g} = [001]$. The embedded dislocations connected to surface pits are extracted from contrast variations in the bright-field (BF)-TEM images. Cross-sectional TEM images reveal sidewalls of pits terminated with intermediate surfaces between {100} and {111} (Fig. 3-10a), and {111} surfaces (Fig. 3-10b). The {111} surface turns out to have a faster sublimation rate than that of the {100} surface since lateral dimensions of the pits are about 10 times larger than the vertical depth (Fig. 3-10a and b), which explains large rectangular pits seen in Fig. 3-2a. Hence, the {100} surfaces are the most stable termination during cooling process with the lowest surface energy. This is confirmed by the *in-situ* annealing experiment of the SnTe microcrystals (Fig. 3-8). Interestingly, the surface pits appear and disappear repeatedly on surfaces during annealing. Surface pits in Fig. 3-8b, f and h present a transition of pit shapes from triangles to rectangles, suggesting a transition of surface terminations from {111} to {100}, suggesting that SnTe {100} holds the lowest surface energy.
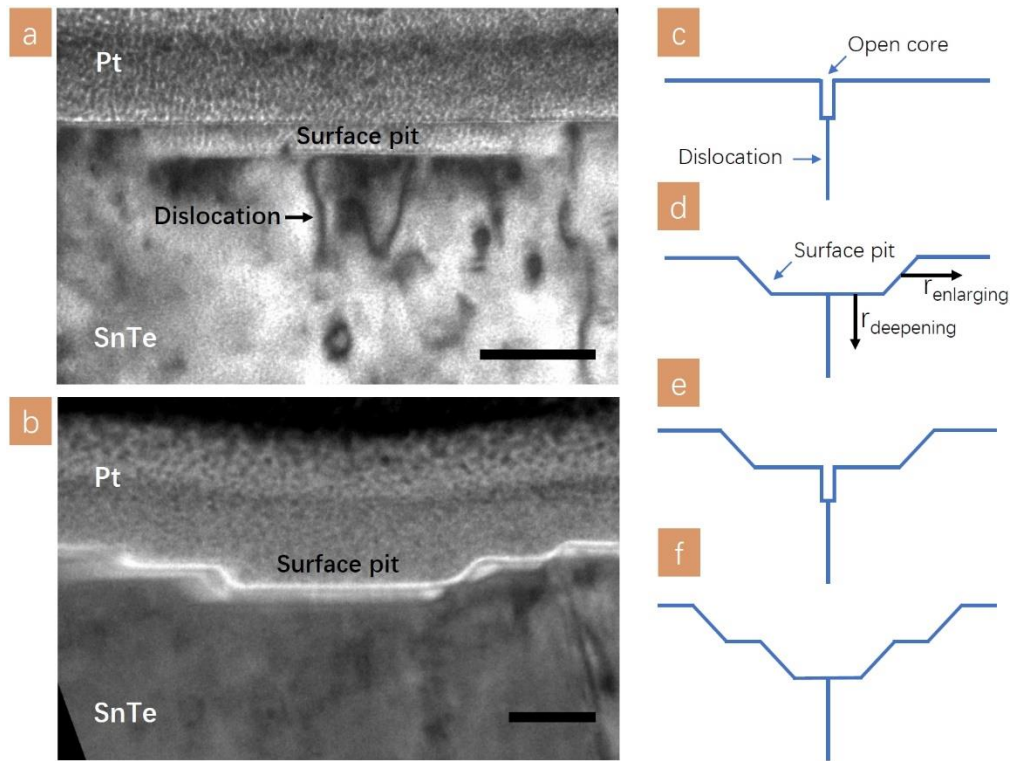
Figure 3-10: BF-TEM cross-sectional views of rectangular pits on a (001) plane

a, BF-TEM image under a two beam condition taken along a diffraction vector of g = [001]. A typical dislocation line is pointed out by an arrow. The formation process of a pit in **a** is depicted in **c** and **d**. **b,** The BF-TEM image shows the deepening process of surface pits. As indicated in **e** and **f**, further expansion of the open core at the bottom of the surface pit generates another pit. Scale bar is 50 nm.

Migration of dislocations during annealing is also reported in a wide range of materials. Similar to the surface pit patterns observed on {111} surface of the SnTe crystal in Fig. 3-3, elongated pits were observed along the glide directions on {111} surfaces of CdZnTe single crystals due to annealing [229]. Accordingly, migration of surface pits is the manifestation of dislocation movement. The surface cleaning procedure using thermally cracked atomic hydrogens might be effective in removing surface oxides and carbon, but limited in promoting smooth surfaces [230].

3.4 Conclusion

To summarize, we observe and characterize surface pits, open cores and steps on {100} and {111} surfaces of SnTe microcrystals, nanoplates and nanowires, synthesized by CVD. TEM images under two beam conditions reveal that surface pits originate from dislocations in SnTe crystals. Enlarging, deepening, and faceting of the surface pits were enabled by sublimation of open cores and anisotropic movement of steps during the natural cooling after the CVD growth. The crystal symmetry, surface termination, and surface polarization contribute to distinct morphologies of the surface pits. Fast cooling, instead of the natural cooling, sufficed to suppress the formation of surface pits on grown SnTe crystals, although growth conditions need to be further optimized in order to decrease the amount of embedded dislocations that are responsible for the surface defects on {100} and {111} surfaces of SnTe microcrystals and nanostructures.

The observed surface pits and open cores can potentially degrade the transport properties of the surface states despite the theoretically predicted topological protection. In particular, for SnTe nanostructures with a high surface to volume ratio, the effects of surface defects on transport properties could be more pronounced. Thus, the presented system could serve as a test bed to measure the degree of the topological protection in the context of transport measurements. In addition, new edge modes associated with dislocations could be possible, similar to the 1D edge mode bound to the screw dislocation of Bi_2Se_3 TIs. More broadly, it would be worthwhile to investigate if similar surface pits and open cores can be observed in SnTe thin films grown via molecular beam epitaxy [231] and other IV–VI

semiconductors with the same crystal structure [232], such as the recently reported

ultrathin $Pb_{1-x}Sn_xTe$ nanoplates [111] and few-layered $SnSe_2$ flakes [233].

Chapter 4: Synthesis of Narrow SnTe Nanowires Using Alloy Nanoparticles

TCI SnTe provides a rich playground to examine interactions of correlated electronic states, such as ferroelectricity, topological surface states, and superconductivity. The study of SnTe nanowires may lead to even richer physics owing to the 1D confinement effect and an increased contribution from the topological surface states. Thus, for transport measurements, SnTe nanowires must be synthesized with reduced diameters and high crystalline quality to ensure 1D confinement and phase coherence of the topological surface electrons. This chapter reports a facile growth method to produce narrow SnTe nanowires with a high yield using alloy nanoparticles as growth catalysts. The average diameter of the SnTe nanowires grown using alloy nanoparticles is 85 nm, nearly a factor of three reduction compared to the average diameter of 240 nm when using gold nanoparticles as growth catalysts. Transport measurements reveal the effect of the nanowire diameter on the residual resistance ratio and magnetoresistance. Particularly, the ferroelectric transition temperature for SnTe evolves systematically with the nanowire diameter. *In situ* cryogenic cooling of narrow SnTe nanowires in a TEM directly reveals the cubic to rhombohedral structural transition, which is associated with the ferroelectric transition. Thus, these narrow SnTe nanowires represent a model system to study electronic states arising from

1D confinement, such as 1D topological superconductivity and potential multiband superconductivity.

The following chapter first appeared[234] as Synthesis of Narrow SnTe Nanowires Using Alloy Nanoparticles. *ACS Applied Electronic Materials* **2021**, 3(1), 184–191.

Authors: Pengzi Liu, Hyeuk Jin Han, Julia Wei, David Hynek, James L. Hart, Myung Geun Han, Christie Jordan Trimble, James Williams, Yimei Zhu, and Judy J. Cha

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4.1 Background and Motivation

Making topological materials into nanostructures is advantageous to enhance the contribution of the topological surface states in transport measurements, as evident in ABO studies of the surface states in TI nanowires[24, 97, 145, 235] and nanoribbons[26, 236] and exotic quantum Hall oscillations observed in nanoslabs of Dirac semimetals.[158] Moreover, novel electronic states can emerge at the nanoscale, such as the MBSs expected in 1D topological superconductors.[176, 237-240] In TCI SnTe,[241, 242] the nanoscale confinement can have a profound impact on the nature of ferroelectric domains,[231] electron coupling between topological surface states,[243] and superconductivity.[41, 117, 119, 244] Several transport studies of SnTe nanostructures highlight the effects of the nanoscale confinement.[33, 117, 245] For example, the proximity-induced superconductivity in

SnTe nanowires is recently suggested to have a novel pairing symmetry of $s \pm is$, which was observed in nanowires with diameters < 250 nm, and the phenomenon was more pronounced for smaller diameter nanowires.[244] Thus, it is critical to develop precision synthesis for topological nanomaterials with controlled dimensions, morphology, and crystalline quality. Additionally, SnTe has also been explored for potential thermoelectric applications. [246]

Most of the topological nanomaterials studied to date have been synthesized using metal nanoparticle-catalyzed CVD,[32-34, 37, 93, 122, 236, 247, 248] in which the VLS growth and VS growth often occur concurrently to produce nanoribbons and nanoplates with a broad distribution of their widths, lacking control on the dimensions and morphology of the nanostructures. If the growth is strictly VLS, nanowires should be produced with their diameters identical to the sizes of the metal nanoparticles used for growth.[249, 250] It is possible to tune the growth conditions carefully to promote VLS growth over the VS growth in order to control the morphology of the nanowires, which has been exploited to grow heterostructure semiconducting nanowires with the heterostructure segments along the axial and radial directions.[251, 252] For topological nanomaterials however, such careful growth studies are sparse. For synthesis of SnTe nanostructures, several works have explored the effects of substrates, catalyst particles, and chemical potentials of gaseous species on the morphologies of SnTe nanostructures,[32, 38, 214, 253, 254] but most SnTe nanowires reported to date have large diameters. Another route to promote VLS growth for narrow nanowires is to tune the composition of the metal nanoparticles to satisfy the supersaturation

conditions more easily and lower the nucleation barrier for the solid phase.[255-259]

In this work, we use Au-Sn-Te alloy nanoparticles as growth catalysts to grow

narrow SnTe nanowires with a high yield. The average diameter of the SnTe

nanowires grown using the alloy nanoparticles is 85 nm, in contrast to 240 nm

using the gold nanoparticles. We also observe higher ferroelectric transition

temperatures for narrower nanowires. *In situ* cryo-TEM experiments confirm the

expected structural transition from the room temperature cubic phase to the low

temperature rhombohedral phase for these SnTe nanowires. Thus, the narrow

SnTe nanowires provide a rich playground to examine the possible multi-band

superconductivity, MBSs, and interplay between ferroelectricity and topological

orders.

4.2 Materials and Methods

4.2.1 Formation of alloy nanoparticles

The alloy nanoparticles were first produced by reacting Au nanoparticles

with SnTe vapor at elevated temperatures in a horizontal tube furnace with a single

temperature zone (Lindberg/Blue M, Thermo Fisher Scientific). A solution

containing 20 nm Au nanoparticles (Sigma Aldrich, Prod. #741965) was drop-

casted on the SiO_x/Si substrates that were pre-treated with a poly-L-Lysine solution

(Sigma Aldrich, 0.01%). The substrates were blow-dried with nitrogen gas for 2

minutes and placed at downstream inside a quartz tube with 1-inch diameter at

distances 9.5 cm to 12.5 cm away from the center of the furnace. 0.1 g SnTe

source powder (Sigma Aldrich, 99.999%) was finely ground and placed in a quartz boat, which was then loaded at the center of the quartz tube. The quartz tube was purged with argon gas (99.999%) 4 times and held at 600℃ for 1 hour after ramping from room temperature within 30 minutes. The pressure was maintained at 2 Torr with a constant Ar flow at the rate of 20 sccm. After the reaction, the furnace was cooled down to room temperature with the fast-cooling process as described in the previous chapter.[37]

4.2.2 Synthesis of narrow SnTe nanowires

For the synthesis of narrow SnTe nanowires, the SiO$_x$/Si substrates decorated with the alloy nanoparticles were loaded into a clean quartz tube at distances from 12.5 cm to 15.5 cm away from the center, along with 0.1 g SnTe source powder placed at the center of the furnace. The temperature profile, growth time, pressure, and the Ar flow rate were kept the same as the first reaction. Narrow SnTe nanowires were found from the substrates placed at 14.5 and 15.5 cm away from the center, which were approximately at 436 and 370℃ during growth, respectively (see Fig. A-3 for the temperature profile of the furnace).

4.3 Results and Discussion

4.3.1 Formation of Au−Sn−Te alloy nanoparticles

Fig. 4-1a shows a SEM image of the alloy nanoparticles after the anneal, which shows many particles with diameter < 100 nm. A TEM image of one of the particles shows a set of lattice fringes (Fig. 4-1b), and a fast Fourier transform of the TEM image shows diffraction spots that belong to either Au or AuSn (Fig. 4-1c). Energy dispersive X-ray (EDX) was performed to analyze composition of the alloy nanoparticles, which shows presence of Au, Sn, and Te (Fig. 4-1d). The annular dark field scanning TEM (ADF-STEM) image of the alloy nanoparticles (Fig. 4-1d inset) shows bright and dark regions, which suggests phase separation. The dark region contains slightly more Sn and Te than the bright region although both regions contain Au, Sn, and Te. According to the Au-Sn-Te phase diagram (Fig. 4-2), Au, AuSn, SnTe, and $AuTe_2$ are possible at room temperature. While the presence of Te could be due to nucleation of SnTe or $AuTe_2$, formation of SnTe is more likely than formation of $AuTe_2$ based on the phase diagram. Thus, we conclude that the nanoparticles are no longer pure Au nanoparticles, but contain Au and AuSn phases, as well as SnTe nuclei. This conclusion agrees with the observation that the Sn/Te ratios from the nanoparticles are higher than that of SnTe (Fig. 4-1e), indicating presence of SnTe and AuSn phases. The alloy composition of the nanoparticles changes with the growth substrate temperature (Fig. 4-3), which suggests varying fractions of Au, AuSn, and SnTe regions in the alloy nanoparticles as a function of substrate temperature. Our findings are in agreement with a previous report, which shows that the Au nanoparticles become

alloyed with Sn during synthesis of SnTe nanowires.[253] We note that this reaction

is essentially the metal-catalyzed CVD growth of SnTe nanowires,[32, 34, 37, 38, 214] and

indeed we observe SnTe nanowires and nanoribbons of varying diameters and

SnTe microcrystals in addition to the alloy nanoparticles.
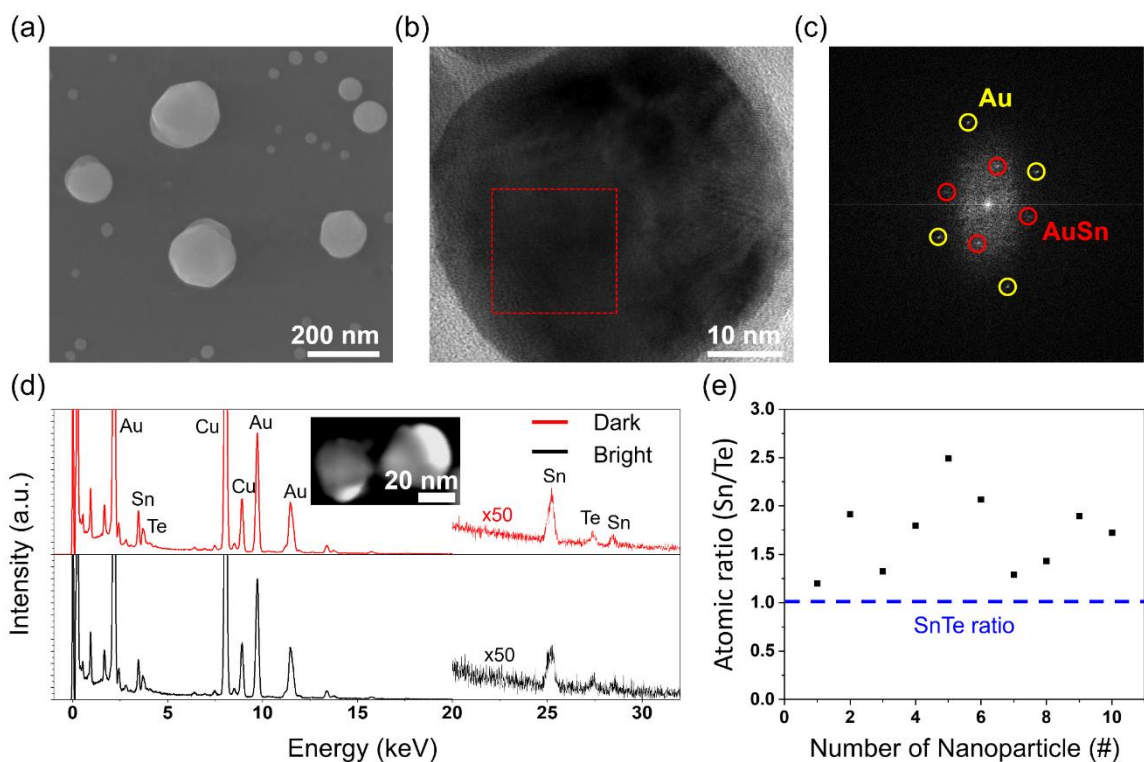
Figure 4-1: TEM characterization of formation of Au-Sn-Te alloy nanoparticles

a, SEM image of a typical substrate after reacting Au nanoparticles with SnTe vapor. **b**, TEM image of an alloy nanoparticle, showing lattice fringes. **c**, A fast Fourier transform taken from the region of the TEM image (red box in **b**) shows diffraction spots that agree with diffraction spots of Au and AuSn. **d**, EDX spectra of the nanoparticle show presence of Au, Sn, and Te. Cu is from the TEM grid. Inset shows the annular dark field STEM image of the nanoparticles; the EDX spectra were acquired from the particle on the right. **e**, Composition analysis of the nanoparticles shows excess Sn in the alloy nanoparticles in comparison to SnTe, suggesting presence of AuSn and SnTe in the alloy nanoparticles.

Fig. 9: The 80 at.% Au section
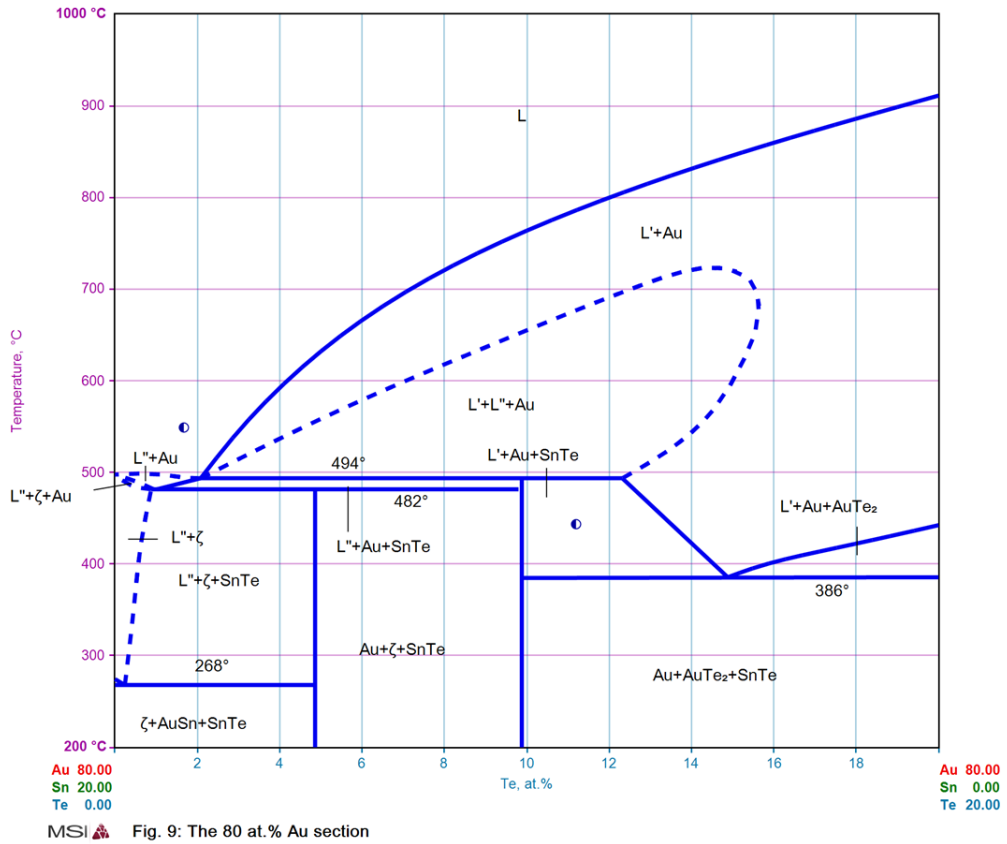
Figure 4-2: Au-Sn-Te phase diagram with 80 atomic % Au

From Mireille Harmelin and MSIT®®; Effenberg, G. (Ed.); SpringerMaterials; 10.19254.1.9
(Springer-Verlag GmbH, Heidelberg, 1995).
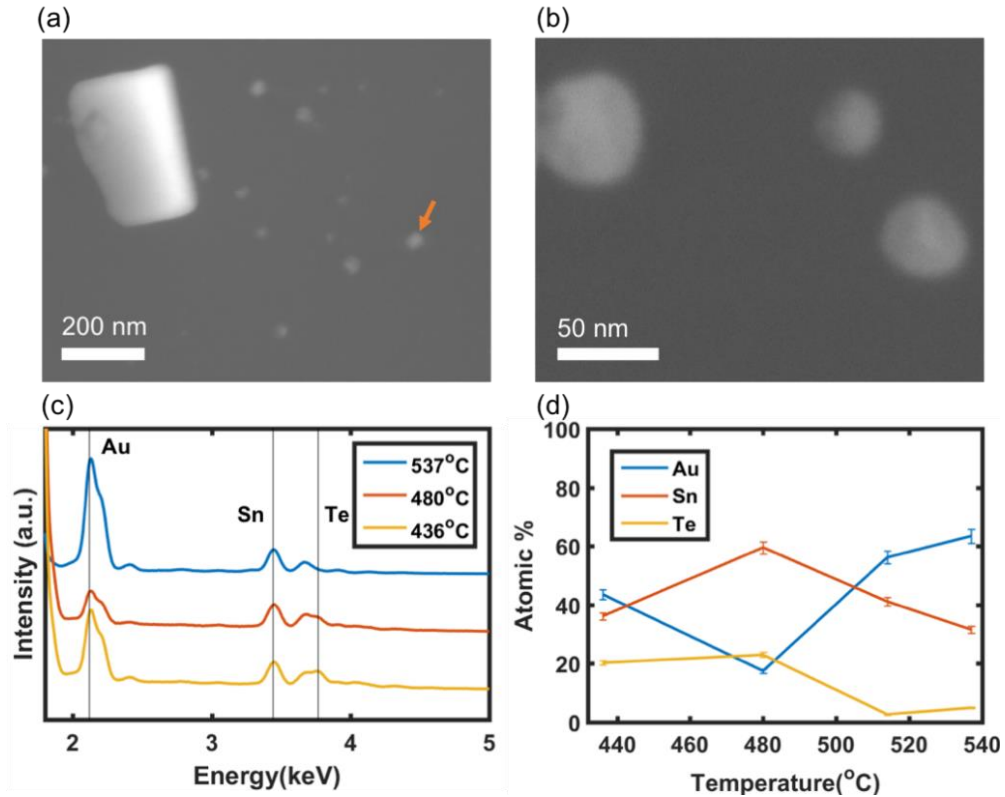
Figure 4-3: SEM characterization of Au-Sn-Te alloy nanoparticles

a, SEM image of a typical substrate after reacting Au nanoparticles with SnTe vapor. One of the particles is indicated by an arrow. **b**, Magnified SEM image of the substrate with nanoparticles. **c**, EDX spectra of the nanoparticles from different growth substrates at 436, 480, and 537°C. The intensities of the Au, Sn, and Te peaks change with the substrate temperature. **d**, Composition analysis of the nanoparticles as a function of the growth substrate temperature.

4.3.2 Synthesis of narrow SnTe single-crystalline nanowires using alloy nanoparticles

Fig. 4-4 shows the comparison of the dimensions and the growth yield of the SnTe nanowires grown using the Au nanoparticles versus the alloy nanoparticles. Fig. 4-4a and 4-4b show SnTe nanowires grown using the 20 nm Au nanoparticles, and Fig. 4-4c and 4d show SnTe nanowires grown using the alloy nanoparticles. The nanowire yield is significantly higher using the alloy nanoparticles. In addition, the nanowires grown with the alloy particles are much

narrower and shorter than the wires grown with the Au nanoparticles. The alloy nanoparticles were observed at the end of the SnTe nanowires, which indicates that they catalyzed the nucleation of the nanowires (Fig. 4-4d). Additionally, the diameter of the nanowire is similar to the diameter of the alloy nanoparticle. By contrast, the SnTe nanowire grown using the Au nanoparticle is much larger than the Au particle (Fig. 4-4b). Fig. 4-4e shows the summary of the comparison between the two cases. Using the alloy nanoparticles, the average diameter of the SnTe nanowires is 85 nm with a standard deviation of 26 nm, while it is 240 nm with a standard deviation of 102 nm using the 20 nm Au nanoparticles. The distribution of the nanowire diameter is significantly narrower and the diameter is reduced by more than a factor of two. SnTe nanowires with diameter below 250 nm would be well-suited to show quantum effects arising from the surface electrons as ABOs were observed in 161 nm-wide SnTe nanowires[33] and Josephson junction behaviors of novel superconductivity were observed in SnTe nanowires with diameter below 250 nm[244]. We also measured the aspect ratios of the SnTe nanowires grown using the Au and alloy nanoparticles, and found them to be nearly identical.
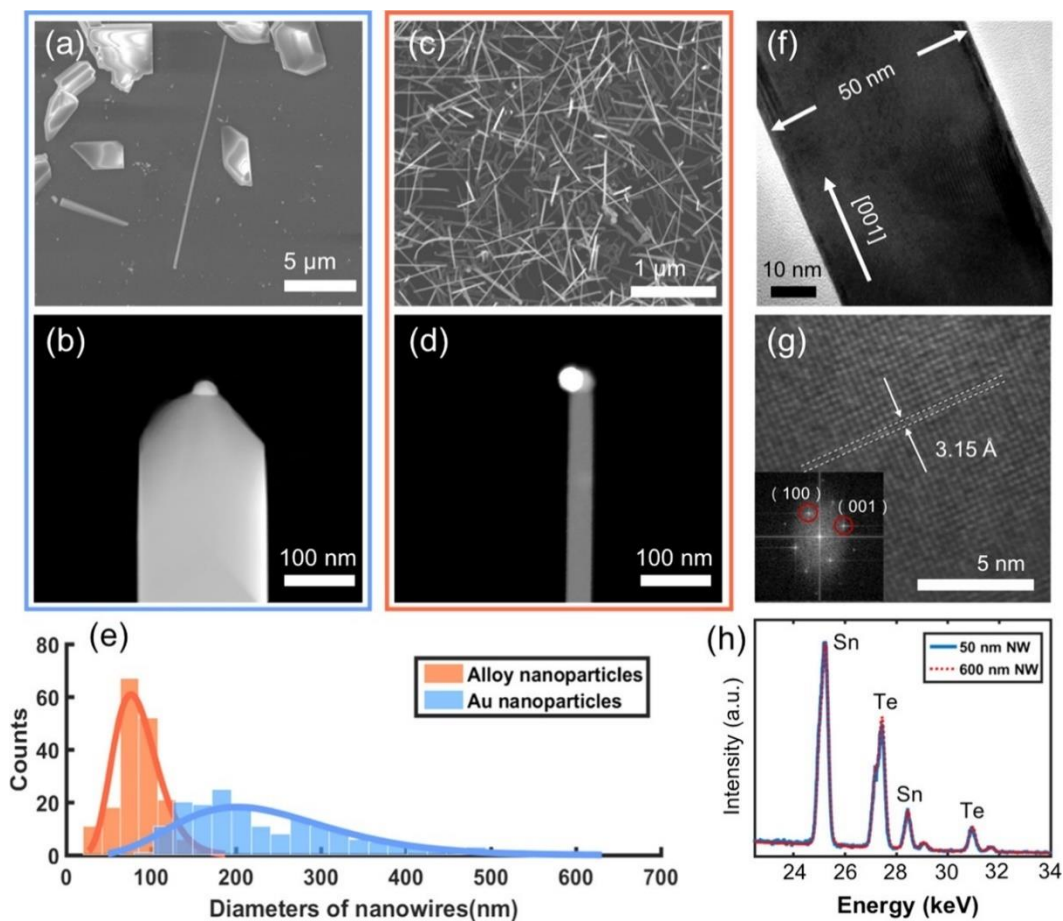
Figure 4-4: Comparison of SnTe nanowires synthesized using Au versus alloy nanoparticles

a, b, SnTe nanowires grown using Au nanoparticles. **c, d**, SnTe nanowires grown using the alloy nanoparticles. The width of the SnTe wire is much larger than the size of the metal particle in the case of using Au particles **b**, while it is the same in the case of using alloy nanoparticles **d**. **e**, Histogram of diameters of SnTe nanowires synthesized using the alloy nanoparticles (orange) and the Au nanoparticles (blue). The average diameters are 85 nm and 240 nm, respectively. **f**, TEM image of a 50 nm-wide SnTe nanowire. **g**, High-resolution TEM image of the SnTe nanowire showing the expected cubic lattice at room temperature with the lattice spacing of 3.15 Å. Inset: Fast Fourier transform (FFT) of the image, which shows the expected diffraction pattern of SnTe. **h**, EDX spectra of a SnTe nanowire grown using a Au nanoparticle (600 nm NW) and the SnTe nanowire grown using the alloyed nanoparticle (50 nm NW). The spectra are identical, confirming the composition of the narrow nanowire is SnTe.

The crystal structure of the narrow SnTe nanowires grown using the alloy nanoparticles was characterized by TEM. Fig. 4-4f and g show TEM images of a 50 nm-wide SnTe nanowire, which shows the expected cubic symmetry and lattice spacing of 3.15 Å at room temperature. The Sn/Te ratio of the narrow SnTe nanowire is identical to that of SnTe nanowires grown using Au nanoparticles based on the TEM-EDX data (Fig. 4-4h). While structural defects, such as surface stacking, strain, and vacancies, would exist in these nanowires, the crystalline quality of the nanowires is sufficient to show transport properties that stem from the topological surface states, such as the recent report of novel superconductivity observed in Josephson junctions using these narrow SnTe nanowires as weak links.[244]

The observed synthesis results can be attributed to the lowered nucleation barrier for the precipitation of the SnTe solid phase. Because the alloy particles already contain Sn and SnTe nuclei, the supersaturation conditions to nucleate a solid phase out of the metal catalyst can be reached more easily with the alloy nanoparticle than with the Au nanoparticle.[251] The reduced nucleation barrier thus would promote VLS growth over the side growth via the direct VS deposition, which can explain the small diameter of the SnTe nanowire. Intriguingly, the length of the nanowires got shortened significantly using the alloy nanoparticles, suggesting suppressed growth rates. The growth rate of a nanowire during a VLS growth is a complex function of growth parameters, such as the diffusivities and diffusion lengths of the precursor species, the rate of direct impingements of the precursor species at the metal catalysts, nanowire diameter, and spacings between the

nanowires.[260-265]   Detailed growth studies of GaAs,[266, 267] InAs,[268, 269] and GaP[270, 271] nanowires highlight the complexity of the growth dynamics. We conjecture that due to the high density of the SnTe nanowires grown on the substrate, growth by direct impingements at the alloy metal particles is unlikely and the nanowire growth stops when the diffusion lengths of the precursors from the substrates are reached. Systematic growth studies must be carried out to fully understand the suppressed growth rate of the SnTe nanowires grown using the alloy nanoparticles.

4.3.3 Transport measurement of SnTe nanowire devices

Transport properties of the narrow SnTe nanowires were measured by fabricating nanodevices with 4-point contacts using standard e-beam lithography. For ohmic contacts, the contact areas were etched with Ar gas for two minutes and Cr/Au contacts were thermally deposited immediately after the etching. Fig. 4-5b shows the resistance measurements of four SnTe nanowires as a function of temperature down to 1.7 K. The resistances were normalized to the room temperature resistance for comparison. The resistance values at room temperature were 55 Ω, 350 Ω, 154 Ω, 38 Ω for Device #1 (80 nm diameter), Device #2 (86 nm diameter), Device #3 (123 nm diameter), and Device #4 (300 nm), respectively. The gradual decrease in resistance at lower temperature indicates that the nanowires are heavily doped, which is common for SnTe due to Sn vacancies.[213]   Interestingly, the residual resistance ratio (RRR) decreases systematically with decreasing diameter of the nanowires. As the RRR is a measure of electron scattering, thus a proxy for crystalline quality, the decrease in RRR indicates increased electron scattering. The increased scattering may be due

to structural defects present in the nanowires, such as vacancies and surface stacking, and surface oxidation, which is more pronounced in transport measurements of nanoscale systems.[272]

The increased scattering is also reflected in the magnetoresistance curves measured at 1.7 K (Fig. 4-5d). The magnetoresistance has the largest increase for the 300 nm-wide nanowire and gradually gets suppressed with decreasing diameter of the nanowire. This behavior agrees with the reduced RRR for narrower nanowires. Structural defects, such as Sn vacancies, may be affected by the dimensions of the SnTe nanowires or by the composition of the metal nanoparticles used to catalyze growth. In such case, the carrier density and mobility may change as a function of the nanowire diameter or the metal alloy composition. Due to the small diameter of the nanowires, Hall bar devices could not be fabricated to measure the carrier densities and Hall mobilities. As a rough estimate of the carrier density, we assume the measured magnetoresistance originates from a single carrier channel with one mobility value, and fit the magnetoresistance using the following equation:

$$\rho_{xx} = \frac{1}{2enu}(1 + \mu^2 B^2), \tag{4-1}$$

where e is the electric charge, n is the carrier density, μ is mobility, and B is the magnetic field. From the fits to the magnetoresistance curves of Device #3 and #4, we estimate the carrier densities of 1×10^{20} cm^{-3} and 0.9×10^{20} cm^{-3} and mobility values of 4000 cm^{2}V^{-1}s^{-1} and 2100 cm^{2}V^{-1}s^{-1} for the two devices, respectively. These are on the lower end of the carrier densities we have

previously measured in Hall bar devices of SnTe nanoplates and nanoribbons.[32] However we note that the mobility values seem very high, and the obtained values of the carrier densities and mobilities should be considered only as a rough estimate. We also note that the magnetoresistance of the 300 nm-wide nanowire does not follow a quadratic relation in which the resistance scales with B^2. Rather, the magnetoresistance appears to be more linear in high magnetic fields.

The transport measurements also show the ferroelectric transition of SnTe, which is accompanied by a structural transformation from its cubic structure at room temperature to the distorted rhombohedral structure.[153, 273] The phase transition can be understood as two processes, one related to the rhombohedral distortion and another related to the polar distortion.[273] The rhombohedral distortion does not break inversion symmetry and does not produce a polar structure. The polar distortion, in which the Te sublattice is shifted from (0.5, 0.5, 0.5) to (0.5 - τ, 0.5 - τ, 0.5 - τ) with $\tau \sim 0.02$, breaks the inversion symmetry, and produces a polar structure with the polarization along [111]. The ferroelectric transition occurs at a temperature at which the resistance curve changes its slope with temperature. Fig. 4-5c shows the derivatives of the resistance curves with respect to temperature, $d\rho/dT$, of Devices #1-4. The kinks observed in the resistance curves (Fig. 4-5b, marked with arrows) are more clearly shown as sudden changes in the $d\rho/dT$ curves, which are marked by arrows in black and red (Fig. 4-5c). We observe broad temperature windows over which $d\rho/dT$ curves change their slopes, which are denoted by shaded rectangular boxes in Fig. 4-5c. Based on transport studies of bulk SnTe crystals,[153, 273] we attribute the resistance

change over the broad temperature window to the phase transition of the nanowires. The transition temperature is correlated with the carrier density; a higher carrier density results in a lower transition temperature.[273] In the case of SnTe nanowires, the broad temperature window for the phase transition as well as their dependence on the diameter of the nanowire may suggest additional effects, besides the carrier density, which determine the phase transition temperature, such as nanoscale effects on the mechanical stresses during phase transition and surface oxidation that might act as an anchoring layer during phase transition. Both effects would become more pronounced with decreasing diameter of SnTe nanowires. *In situ* cyro-TEM experiments to directly visualize the phase transition would provide important insight for this process. It is interesting to note that most bulk studies that show a clear phase transition exhibit a 'metallic' transport behavior in which the resistance gradually decreases with decreasing temperature even though SnTe is a TCI. Interplay between a large density of carriers and ferroelectric property remains to be explored.
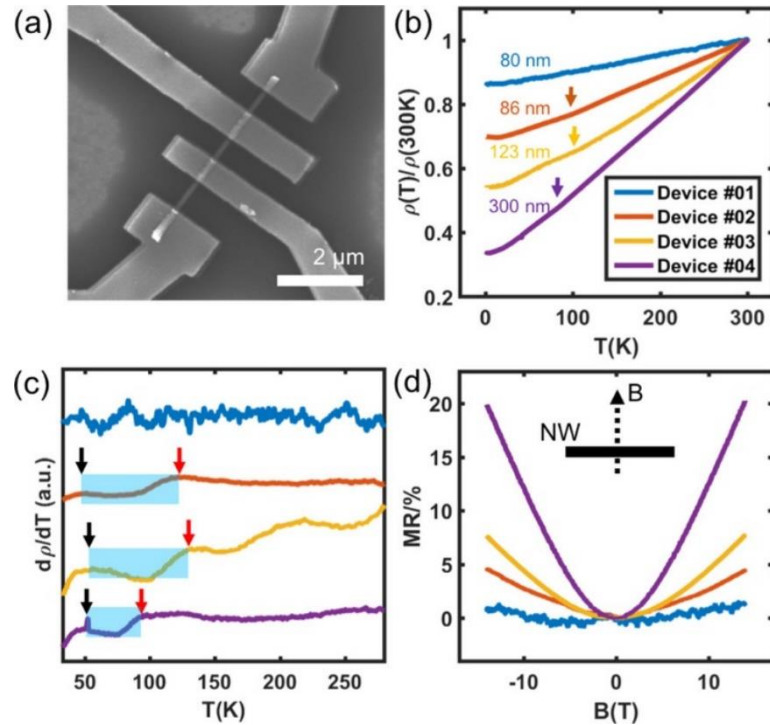
Figure 4-5: Transport properties of narrow SnTe nanowires

a, SEM image of Device #1. **b**, Temperature (T)-resistance (*ρ*) curves of SnTe nanowires of varying diameters: 80 nm (Device #1), 86 nm (Device #2), 123 nm (Device #3), and 300 nm (Device #4). The normalized resistance curves show slope changes at ∼ 100 K, which are marked by arrows. **c**, *dρ/dT* curves of the SnTe nanowires of varying diameters. Sudden changes in the *dρ/dT* reflect the slope changes in the T−ρ curves, as shown in **b**. The slope changes in the resistance indicate the structural phase transition. **d**, Magnetic field (B)–resistance curves of the SnTe nanowires of varying diameters. Magnetoresistances are measured at T = 1.7 K.

4.3.4 Ferroelectric phase transition by *in situ* cryo-TEM

To directly observe the structural phase transition and investigate the ferroelectric nature of the SnTe nanowires, we carried out *in situ* cryo-TEM experiments in which we cooled the narrow SnTe nanowires from room temperature to 12 K. At low temperature, dark bands appeared perpendicular to the nanowire [100] axis along the length of the nanowire, which were absent at room temperature (Fig. 4-6a, b). These bands are not bend contours that would

arise from local bending of the nanowire as swinging the electron beam did not change the locations of the dark bands. Additionally, the electron diffraction pattern taken at 25 K showed splitting of the (001) diffraction spots along the [100] axis (Fig. 4-6d), which were single spots at room temperature (Fig. 4-6c). Upon warming to room temperature, the dark bands as well as the splitting of the diffraction spots disappeared, indicating a reversible change. Thus, the *in situ* cryo-TEM data is indicative of a symmetry lowering structural phase transition at low temperature.
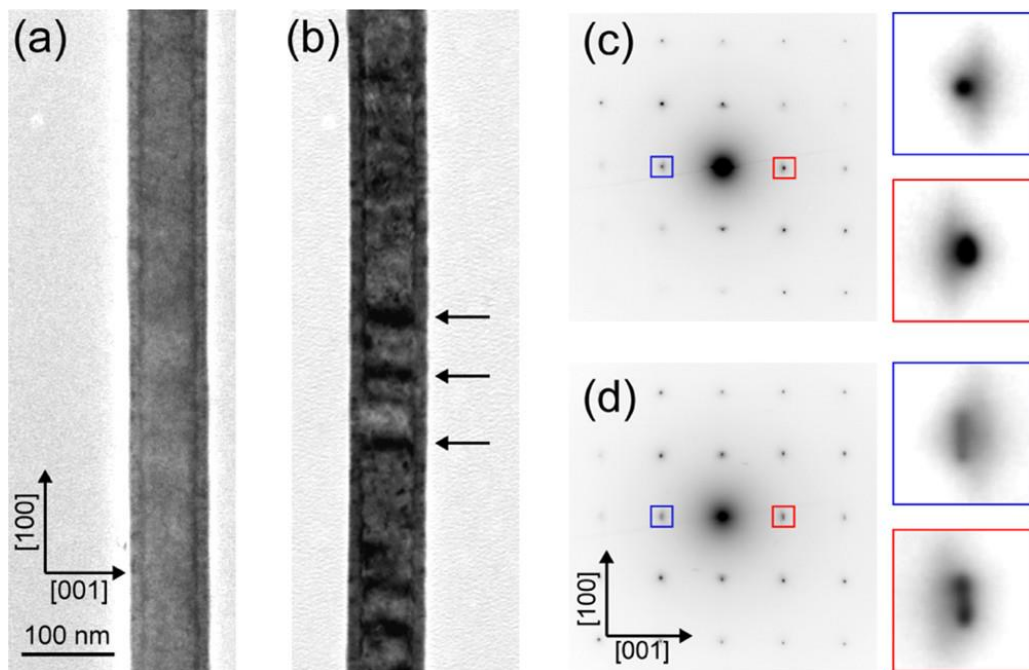
Figure 4-6: Phase transition of SnTe nanowire by *in situ* cryo-TEM

TEM images of a SnTe nanowire at **a**, room temperature and **b**, at 25 K. Dark bands appear along the nanowire at 25 K (marked by arrows in **b**), which are not present at room temperature. **c,d** Selected area electron diffraction patterns of the SnTe nanowire at room temperature **c** and at 25 K **d**. In both **c,d**, the insets show magnified (001)-type spots. Spot splitting is observed at 25 K but not at room temperature.

If the observed nanowire does, in fact, show similar ferroelectric order to that of bulk SnTe, the cubic rock-salt structure at room temperature (with $\alpha = 60°$ when described in the primitive rhombohedral cell) would undergo a rhombohedral distortion characterized by $\alpha \sim59°$ and a polar displacement of Te along the [111] axis.[274, 275] Within the pseudo-cubic unit cell, this results in a [111] oriented polarization, as illustrated in Fig. 4-7b. While the ferroelectric domain structure of bulk SnTe is not known, rhombohedral $BiFeO_3$ and $BaTiO_3$ are well-studied systems which, similar to SnTe, have [111] polarization with a pseudo-cubic unit cell. In both $BiFeO_3$ and $BaTiO_3$, mechanical compatibility and charge neutrality across domain walls (DWs) favor the formation of 109° DWs on {100} or 71° DWs on {110} planes.[276, 277] Fig. 4-7b shows an atomic schematic of a 109° DW for SnTe, and Fig. 4-7c shows a nanowire schematic with both a 109° and 71° DW. The dark bands observed with cryo-TEM imaging (Fig. 4-6b) are consistent with either a 109° DW on (100) viewed edge on, or a 71° DW on (110) viewed in projection. To relate the proposed domain structures to the diffraction data (Fig. 4-6d), we simulated the diffraction signals from both 109° and 71° DWs (see experimental details in Appendix D.2). Both simulations qualitatively match two key aspects of the experimental data: first, splitting of (100) spots is absent owing to the invariant (100) or (110) DW plane, and secondly, (001) spots split along the [100] direction. However, both the 71° and 109° DW simulations show splitting of (101) type spots, which is absent in the experimental data. We found that the (101) type spot splitting can be removed if one of the domains is tilted ~1° about the [001] axis in simulations (Fig. 4-8). Thus, the discrepancy between the

experimental and simulated data can be explained if there is a slight misorientation across the DW, possibly due to structural flexibility of unbounded nanowires. To summarize, the cryo-TEM data is fully consistent with ferroelectric SnTe with [111] polarization, and either 109° or 71° DWs.
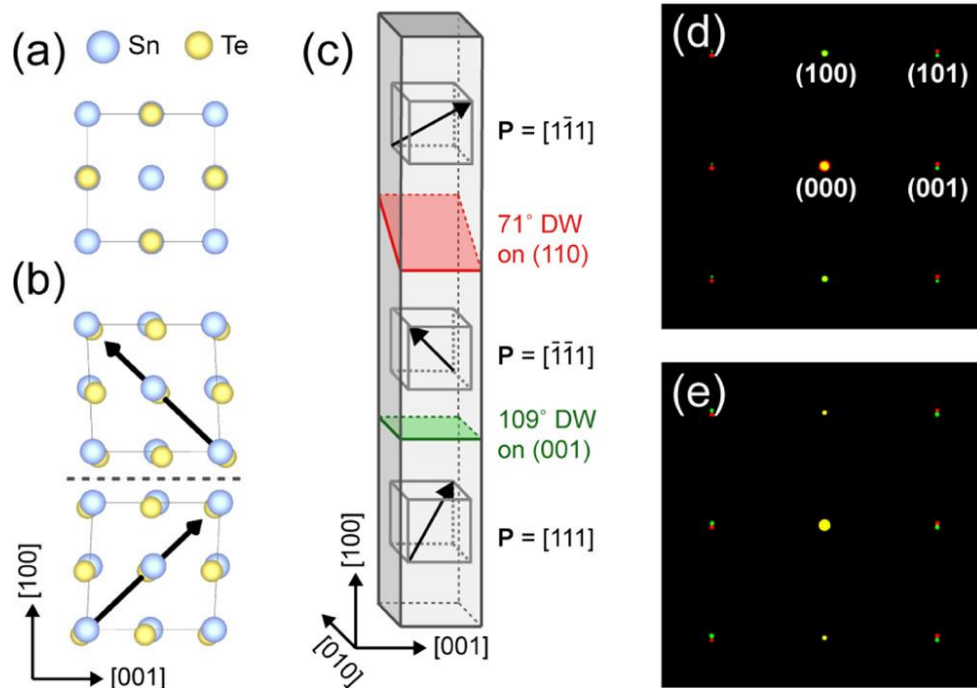
Figure 4-7: Ferroelectric domain structures in SnTe nanowire at low temperature

a, Schematic showing the cubic SnTe unit cell at room temperature. **b**, Schematic showing the polar SnTe pseudo-cubic unit cell at low temperature. The polar distortions were magnified for clarity. Two unit cells are shown to demonstrate a 109° DW on the (100) plane, indicated with the dotted line. The polarization changes from [111] to [1-1-1]. **c**, Schematic nanowire with three domains, showing a 71° DW on (110) in red and a 109° DW on (100) in green. The rhombohedral unit cell distortion and its effect on the nanowire geometry is suppressed in this schematic for clarity. **d**, Simulated electron diffraction of a 71° DW. **e**, Simulated electron diffraction of a 109° DW. In both d and e, the different color spots represent diffraction spots from different domains.
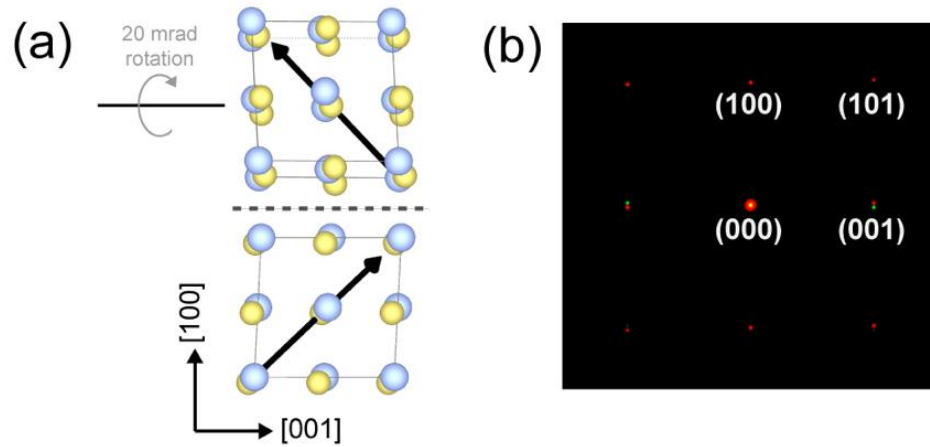
Figure 4-8: Ferroelectric domain structure in SnTe nanowire at low temperature with misorientation between two domains

a, Schematic showing the polar SnTe pseudo-cubit unit cell with a 109° DW on the (100) plane, indicated with the dotted line. In this case, the top domain is rotated by 20 mrad.. **b**, Simulated electron diffraction pattern of the 109° DW structure shown in **a**, with the 20 mrad mis-tilt between the two domains. The splitting of (001) spots are clear while (101)-type spots do not split anymore.

4.4 Conclusion

We developed a reliable route to synthesize narrow SnTe nanowires with diameters under 100 nm using alloy nanoparticles. Experimentally, this was achieved by performing CVD growths twice. In the first growth, gold nanoparticles react with SnTe vapor to form the alloy nanoparticles. In the second growth, the alloy nanoparticles catalyze the growth of narrow SnTe nanowires. Transport measurements showed a size-dependent RRR and magnetoresistance, suggesting increased electron scattering due to surface oxidation and other factors. The diameter-dependent ferroelectric transition temperature suggests that the carrier density decreases for narrower nanowires, likely due to the removal of

bulk electron carriers. *In situ* cryo-TEM experiments of SnTe nanowires showed the low temperature rhombohedral structure with the emergence of dark bands in the TEM image, suggesting domain boundaries between two rhombohedral domains. Simulation results suggest that both 109° and 71° DWs are possible. The synthesized nanowires are important for the investigation of the nature of the superconductivity induced in these nanowires, which was recently suggested to have a pairing symmetry of *s* $\pm$ *is* via Josephson junction measurements. They are also important for investigations of MBSs expected in this material [278].

Chapter 5: Ongoing Research: Passivation of SnTe Nanowires

5.1 Background and Motivation

With the scope of improving crystal quality of SnTe nanowires in order to easily reveal and control the topological properties, I continue investigating the surface passivation of narrow SnTe nanowires synthesized using the two-step CVD growth method described in Chapter 4. Among TIs, the most studied systems are the intrinsic or alloyed binary tetradymite compounds Bi_2Se_3 and Bi_2Te_3 in bulk form [15-19] or nanoscale [20-26]. Although sufficiently high bulk resistivity with a high bulk mobility enable the manifestation of surface transport properties, these materials typically suffer from high bulk carrier densities, surface oxide layers, impurities from ambient and contaminations in the fabrication process [3], which hinder the development of both topological physics and practical applications.

The major materials challenge facing TCIs is also the high residual bulk carrier density and surface degradation, which dominates over surface states, making it difficult to observe transport properties of the surface states in nanoscale devices. For instance, the high bulk hole carrier density of SnTe is due to Sn vacancies and SnTe is prone to surface oxidation and ambient impurities. Therefore, the passivation of SnTe nanowires is of great importance for revealing

their topological states. The goal of this ongoing work is to look for a controllable *in situ* surface passivation method during synthesis of narrow SnTe nanowires.

5.2 Methods and Preliminary Results

In order to realize surface passivation, SnTe nanowires with and without Te capping are grown under the same condition for comparison. After refining Te capping conditions, we are seeking dual evidence from both the ferroelectric phase transition temperature and quantum oscillations suggesting that *in situ* Te passivation can lower the carrier concentration in SnTe nanowires and nontrivial surface states are better revealed.

5.2.1 Refinement of Te capping

In the control experiment, SnTe nanowires are grown by the two-step CVD method, as described in the previous chapter. 0.1 g of SnTe and 0.05 g of Sn source powder (Sigma Aldrich, 99.99%) is placed at the center of a 1" tube furnace (Lindberg/Blue M) with 1 cm × 1 cm SiO_x/Si substrates located between 11 cm and 14 cm downstream. SiO_x/Si substrates are covered by 20 nm Au nanoparticles. After purging with Ar multiple times, the system is pumped down to 300 mTorr, then Ar is flowed at 120 sccm, bringing the furnace pressure up to ~ 3.5 Torr. The furnace is heated to 600°C over 30 minutes and held at that temperature for 1 hour before fast cooled to room temperature. The substrates from first step CVD growth are placed in the furnace for the second growth of narrow nanowires with Ar flow of 20 sccm, pressure of 2 Torr while other conditions remain the same.

For the passivated SnTe nanowires, we protect the surface of the nanowires with Te deposition immediately after the two-step growth of SnTe nanowires without opening the tube. Three parameters are tuned to achieve an effective protection Te layer: capping temperature, duration and furnace pressure. A moderate capping temperature ensures the generation of abundant Te vapor for homogenous deposition of a Te layer on SnTe nanowires surface instead of growth of Te nanowires on the substrates. The capping time affects the thickness of the Te capping layer and the morphology of SnTe nanostructures. And the furnace pressure can also be used to control the thickness of the Te capping layer.
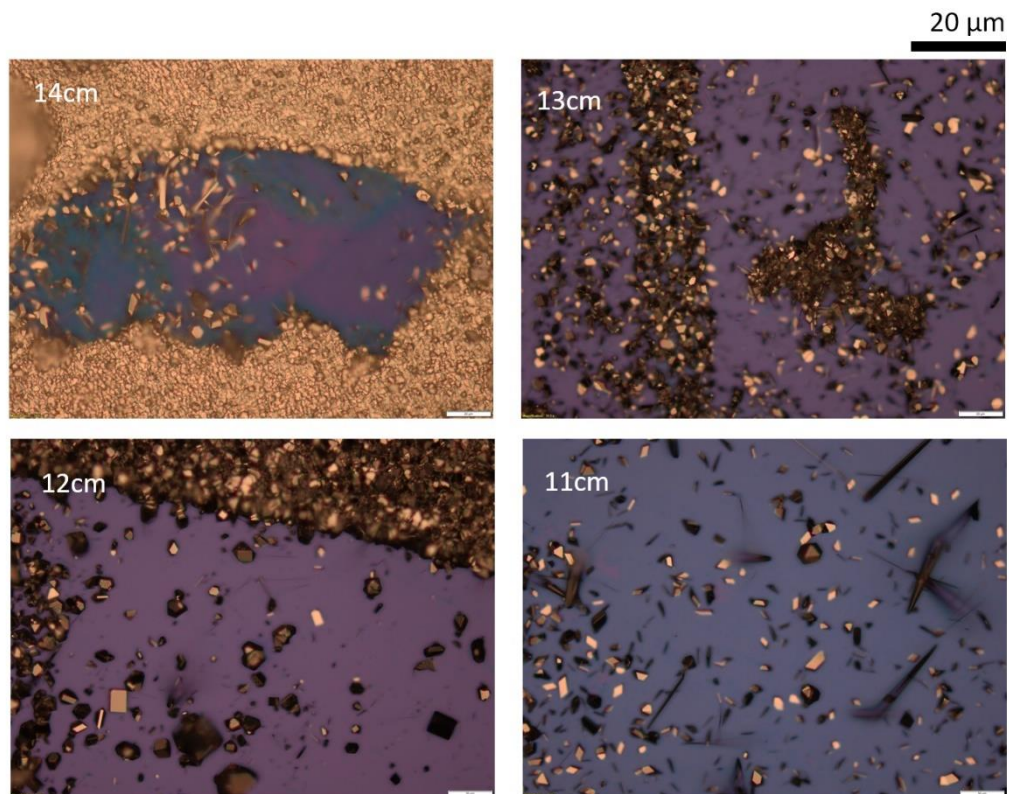
Figure 5-1: SnTe nanowires with *in situ* Te capping on as-grown substrates

Typical optical micrographs showing SnTe nanowires with Te capping on four as-grown substrates. The distance to the center of the furnace is labelled in each image.

For Te capping, we introduce the boat filled with Te powder immediately after the growth of SnTe nanowires. The furnace is cooled from 600°C to 370°C in 2 minutes and held at the temperature for 2 minutes, followed by a fast-cooling process. Ar flow rate and furnace pressure are kept the same as nanowire growth. Fig. 5-1 shows typical optical microscope images of SnTe nanowires with Te capping on the as-grown substrates. SnTe nanowires can be observed on all four substrates, while we only use nanowires transferred from 13 cm or 14 cm substrates for device fabrication due to their thinner diameters. The existence of Te passivation is confirmed by a TEM image and SEM-EDX as displayed in Fig. 5-2.
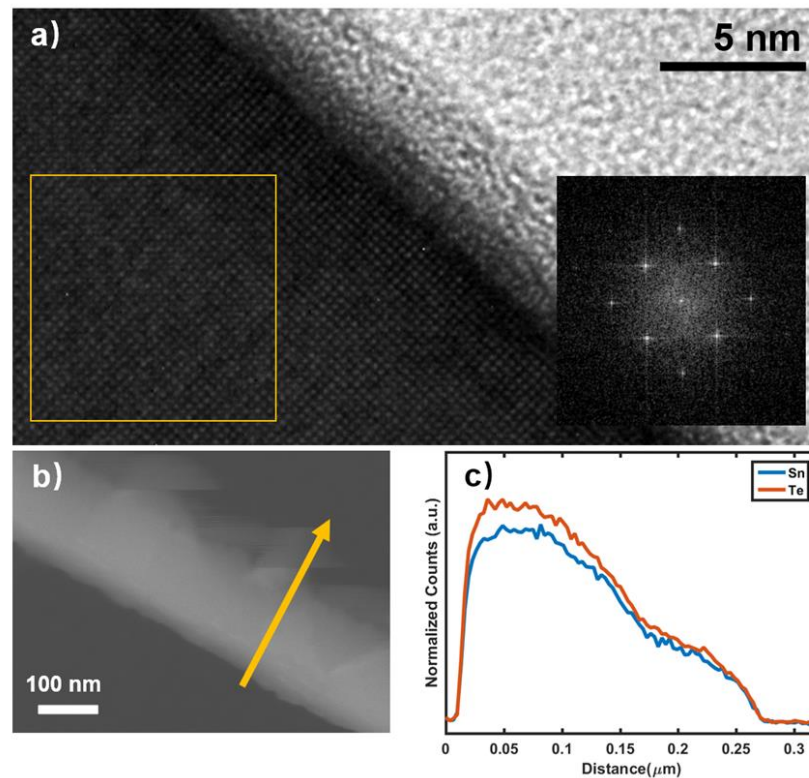
Figure 5-2: Characterization of Te-capped SnTe nanowires

a, High magnification BF-TEM image of a 77 nm SnTe nanowires with a Te capping layer. Inset shows the FFT of selected area indicated by the yellow box. **b**, SEM image of a 140 nm SnTe nanowire with Te passivation. **c**, Line-scan EDX spectrum along the direction indicated by yellow arrow of the nanowire imaged in **b**. The excess Te compared to Sn suggests the existence of Te passivation.

In conjunction with surface roughness observed along the SnTe nanowire in Fig. 5-2b, the higher concentration of Te in comparison to Sn demonstrates (Fig. 5-2c) the formation of Te passivation. Fig. 5-2a shows well-resolved cubic lattices corresponding to the {100} surface planes, confirming the good crystalline quality of the nanowire after Te passivation. To further understand the role of Te passivation, we perform transport measurement with four-terminal nanodevices fabricated using unpassivated and passivated SnTe nanowires.

5.2.2 Te capping layer removal during device fabrication

Detailed discussion about device fabrication on SnTe nanowires can be found in Appendix B. Here, I want to emphasize the process of etching before metallization of contact areas for passivated SnTe nanowires. For unpassivated SnTe nanowire devices discussed in previous chapters, 15/200 nm thick Cr/Au electrical contacts were deposited by thermal evaporation (Kurt Lesker Nano38 thermal evaporator) after short reactive ion etching (Oxford Instruments, 2 minutes at 50 W power with a 40 sccm flow of Ar and a pressure of 40 mTorr) to remove a surface oxide layer at the contact regions. Nevertheless, such process will expose the etched contact area to ambient for ~ 2 minutes before the device is transferred into the thermal evaporator. Hence, for the fabrication of Te-passivated SnTe nanowire devices, we switch to using a UHV electron beam evaporator for *in situ* plasma cleaning to remove surface impurities and the Te capping layer before metal deposition. We find that 2 minutes of *in situ* cleaning with 100 W power Ar

plasma are sufficient for making ohmic contacts of unpassivated SnTe nanowire

devices.

5.2.3 Preliminary results from transport measurement

The temperature-dependent resistance and magnetoresistance of the

unpassivated SnTe nanowires is examined as the control group (Fig. 5-3). The

following observations are largely consistent with the conclusions in Chapter 4. As

displayed in Fig. 5-3a and b, the gradual decrease in resistance at lower

temperature indicates that the nanowires are heavily p-type doped, which is

common for SnTe because of Sn vacancies. The residual resistance ratio (RRR)

decreases with decreasing diameter of the nanowires, suggesting increased

contribution from electron scattering for narrower SnTe nanowires, which may be

caused by structural defects present in the nanowires (vacancies, surface

stacking, and surface oxidation).
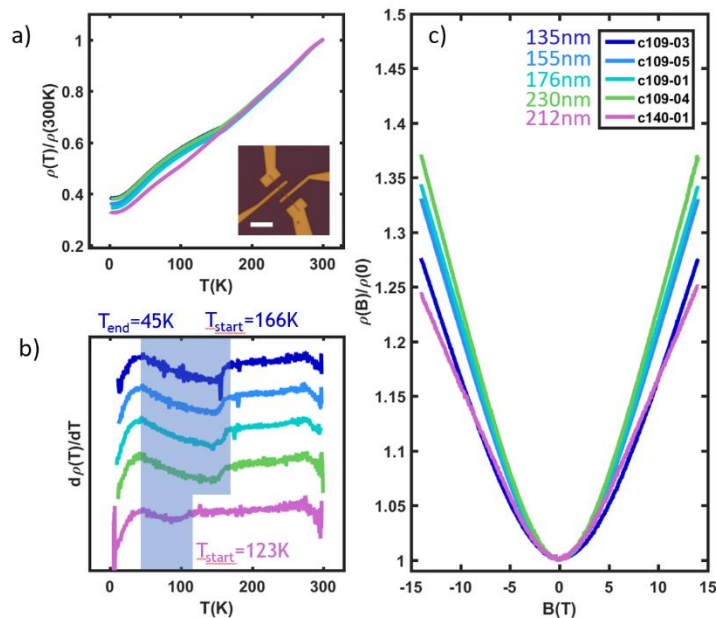
Figure 5-3: size-dependent resistance measured for unpassivated SnTe nanowires

a, Temperature (T)-resistance (ρ) data of unpassivated SnTe nanowires of varying diameters: 135 nm (Device #109-03), 155 nm (Device #109-05), 176 nm (Device #109-01), 230 nm (Device #109-04), and 212nm (Device #140-01). The normalized resistance curves show slope changes at ~ 166 K. Inset shows a typical optical micrograph of 4-probe nanowire devices. Scale bar is 10 µm. **b**, $d\rho/dT$ curves of the SnTe nanowires of varying diameters. Sudden changes in the $d\rho/dT$ reflect the slope changes in the T–ρ curves, as shown in **a**. The slope changes in the resistance indicate the ferroelectric phase transition. T_{start} represents the starting temperature of the transition and T_{end} marks the end of the phase transition during cooling. **c**, Magnetic field (B)–resistance curves of the SnTe nanowires of varying diameters. Magnetoresistances are measured at T = 1.7 K.

Fig. 5-3c indicates that magnetoresistance (MR) is the largest for the 230 nm-wide nanowire, and MR is gradually suppressed with decreasing the nanowire diameter. This behavior agrees with the reduced RRR for narrower nanowires as discussed in Chapter 4. It is worth mentioning that all devices were fabricated using SnTe nanowires grown in the same batch except for Device #140-01, which may explain the consistency for all measured devices in size-dependent RRR and MR measurement in Fig. 5-3, and again, emphasize that the cleanness of both material growth and device fabrication are essential for the investigation of topological nanomaterials.
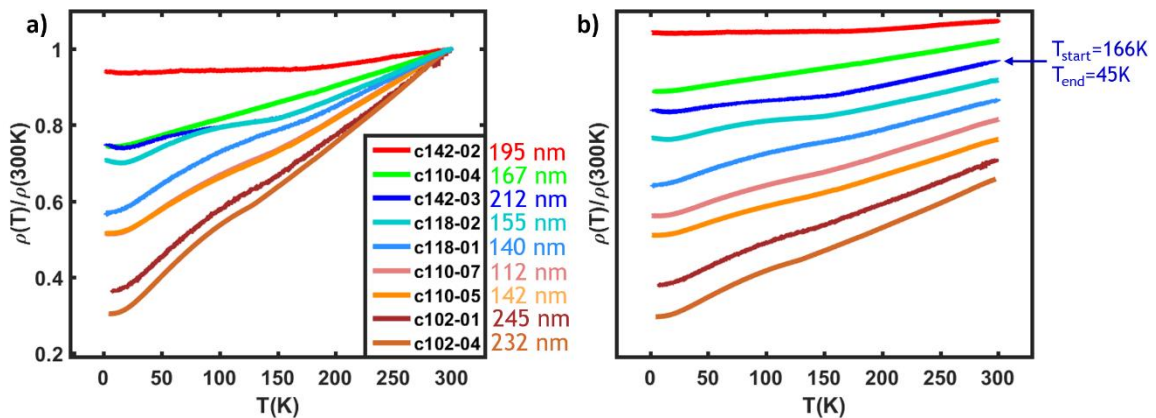
Figure 5-4: Resistance vs. temperature transport data for the passivated SnTe nanowire devices

a, b, Resistances as a function of temperature for devices with surface passivation. Diameters of nanowires are labeled for each device. **b,** The highest starting temperature, 166 K, of ferroelectric transition is obtained from Device #142-03, which is identical to the record of unpassivated nanowire devices.

In comparison, we also obtained resistance vs. temperature transport data of passivated SnTe nanowires. It fails to show size dependency even for the devices fabricated from the same growth batch of Te-capped nanowires (Fig. 5-4). We hypothesize that the presence of the Te capping layer complicates the temperature-dependent resistance. Other than dimensionality effect and variations of crystal quality, the inhomogeneous deposition on SnTe nanowire surfaces and the Te residue at contact areas can contribute to the nanowire resistance.

It is known that a higher carrier density results in a lower ferroelectric transition temperature for SnTe. Our transport results do not suggest an effective reduction of bulk carrier density for passivated nanowires, as the highest starting temperature, 166 K, of ferroelectric transition observed is identical to the the transition temperature of unpassivated nanowire devices. However, the slight upturn of resistance below 20 K for passivated samples #118-02 and #142-03 may be associated with surface electron states since the bulk carriers freeze out at such temperature range, and therefore surface conduction is enhanced.

5.3 State of Ongoing Research and Next Steps

We have investigated the capping conditions for Te passivation and obtained some preliminary transport data for both passivated and unpassivated SnTe nanowires as discussed in previous sections. Continued research will explore the following three directions.

5.3.1 Improving the etching process during device fabrication of passivated

SnTe nanowires

Currently, the device measurement process is still impacted by the Te residue at the contact areas, and this problem could be potentially addressed by metal assisted *in-situ* plasma cleaning prior to contact deposition.
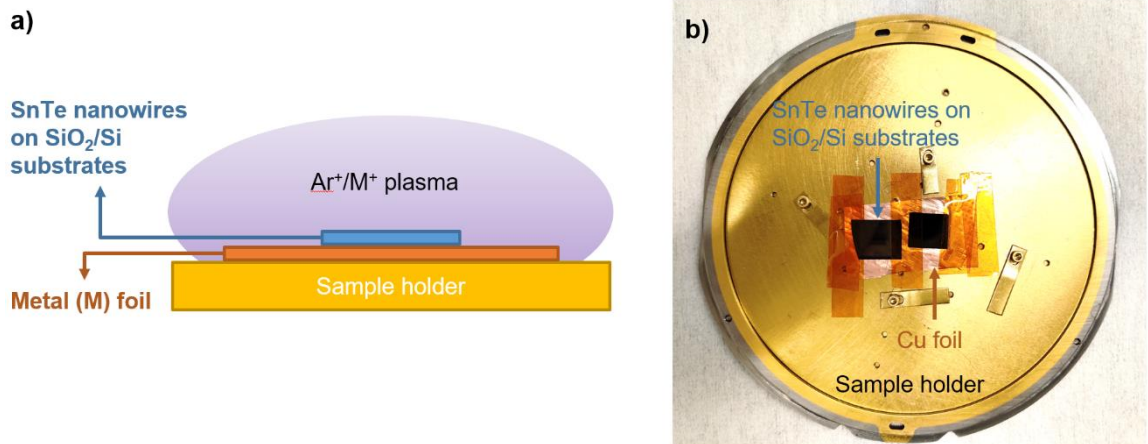
Figure 5-5: Ar cleaning with copper foil

a,b Schematic and experimental setup for Ar plasma cleaning before metallization using UHV e-beam evaporator.

Such improvement could be achieved by adding a copper foil between the sample and sample holder as illustrated in Fig. 5-5a. Although the effectiveness of metal-assisted plasma cleaning for Te-passivated SnTe nanowires remains unclear, it has been corroborated for layered chalcogenide nanostructures.

5.3.2 *In-situ* cryo-TEM imaging of narrow passivated SnTe nanowires

In-situ TEM experiments will capture changes in crystal structure through real-space imaging as well as by monitoring the diffraction pattern during

ferroelectric transition. In Chapter 4, we visualized the structural phase transition in both real and reciprocal space with cryo-TEM imaging. If Te passivation reduces the bulk carrier density effectively, then the transition temperature would be increased to a higher range and the ferroelectric phase transition might be observable above 100 K. To date, the interplay between ferroelectric phase transition temperature and bulk carrier concentration of SnTe nanowires remains unveiled.

5.3.3 Transport measurement of passivated nanowires

To fully understand the role of the Te passivation and the electrical behavior of Te-passivated SnTe nanowires, additional transport measurements are required at low temperatures and with applied magnetic fields using a.c. lock-in detection. More passivated SnTe nanowire devices will be measured in searching for nontrivial ABO and SdH oscillations, which indicate the presence of topological surface states. Furthermore, the surface Dirac 2D carrier concentration can be extracted from the SdH oscillation data, allowing a more quantitative understanding of the topological surface states of Te-passivated SnTe nanowires.

Chapter 6: Conclusion

6.1 Summary of Completed Works

This dissertation presents a few of my compelling works in pursuing high-quality and narrow TCI SnTe nanowires. In Chapter 2, I review the recent notable synthesis and electron transport achievements of topological nanomaterials, and survey two topological superconducting systems that can host MBSs in topological nanowires. Considering that materials and measurement challenges must be overcome before topological nanomaterials can be used in next-generation electronic devices, I choose to focus on improving crystal quality and controlling dimensions of TCI SnTe in nanoscale as it provides a rich playground to examine interactions of correlated electronic states, such as ferroelectricity, topological surface states, and superconductivity. Chapter 3 systematically characterizes and discusses the formation mechanism of surface pits, open cores and steps on {100} and {111} surfaces of SnTe microcrystals, nanoplates and nanowires, synthesized by CVD. We show that the fast-cooling process can effectively suppress the formation of surface defects. Chapter 4 details the reliable route to synthesize narrow SnTe nanowires with diameters under 100 nm using alloy nanoparticles. Transport measurements showed a size-dependent RRR and magnetoresistance, suggesting increased electron scattering due to surface oxidation and ambient contamination for narrower nanowires. *In situ* cryo-TEM experiments of SnTe nanowires showed the low temperature rhombohedral structure with the emergence of dark bands in the TEM image, suggesting domain boundaries

between two rhombohedral domains. To further mitigate the high residual bulk carrier density and surface degradation of SnTe nanowires, I start to explore surface passivation of SnTe nanowires using *in situ* Te deposition during CVD growth. This ongoing project in Chapter 5 achieves refined deposition conditions and demonstrates a promising signature of surface conductivity revealed by transport measurement.

In addition to the works discussed in the previous chapters, I also co-authored a number of additional projects in our research group investigating synthesis and transport measurement of WTe_2 nanowires [272] and MoP nanostructures [279], as well as Josephson detection of time-reversal symmetry broken superconductivity in SnTe nanowires [278].

6.2 Future Direction for Continued Research

The study detailed in this dissertation documents the bulk of my research endeavors in my Ph.D. studies, which aims to bridge the significant gap between TCI SnTe nanowires and 1D topological superconductors (TSC) served as robust quantum computation platforms. The research efforts required are multi-disciplinary, depending on tightly integrated, long-term collaborations between material scientists, electrical engineers, and condensed matter experimental and theoretical physicists. As such, I propose the following objectives to address challenges in material synthesis and transport studies.

The synthesis of narrow TCI SnTe nanowires with diameters $\leq$ 100 nm remains an area of great important due to the obstacles associated with crystalline defects, surface impurities, and bulk electron states. With the goal to control the dimensions and improve the crystal quality of TCI SnTe nanowires grown via CVD, the Te passivation of SnTe nanowires need to be further investigated. As conveyed in Chapter 5, careful improvement of cleaning process of the contact area is crucial for nanowire device fabrication. Furthermore, the *in situ* cryo-TEM experiment characterization of ferroelectricity in passivated SnTe nanowires would elucidate the role of the Te capping layer and the correlation between the bulk carrier density and ferroelectricity.

One of the biggest drawbacks to the CVD growth method and *in situ* passivation is the lack of precise control over nanowire dimensions and deposition thickness. Due to the high level of interdependence of growth parameters on one another, the mechanistic study of nanowire synthesis and passivation using CVD is time-intensive. In this regard, the recent thermomechanical molding of nanowires of ordered phases is promising [280] as it provides morphological control and high throughput screening of a top-down approach without the byproducts of creating defects induced during lithography process. Such nanomolding process also provide a potential route to fabricate In-doped SnTe nanowires, which are predicted to be intrinsic 1D topological superconductors.

From the previous findings reported by our group [119], incomplete superconductivity has been observed in In-doped SnTe nanowires, obscuring the origin and robustness of induced superconductivity via doping. Therefore, for the

realization of the 1D topological superconductor, efforts should be dedicated to optimizing the yield and dopant concentration in In-doped SnTe nanowires presenting a full superconducting transition around 2 K. In my CVD recipe, different from the synthesis of SnTe nanocrystals, precursors for the synthesis of In-doped SnTe nanocrystals consist of 0.15 g InTe (Sigma Aldrich, 99.999%), 0.06 g SnTe (Sigma Aldrich, 99.999%) and 0.09 g Sn powder (Sigma Aldrich, 99.8%). The Ar flow rate, pressure, ramping time and growth time are kept the same as growth conditions for SnTe nanowires during CVD growth. The center temperature stays at 873 K for 60 minutes followed by natural or fast cooling process. Despite a ~3% In concentration found in some In-doped SnTe nanowires, no superconducting transition has been observed above 350 mK. Our previous work [119] suggested a critical In concentration of ~5% for the onset of superconductivity in nanostructures below 2 K, which explains the absence of superconducting transition in my previous measurements. However, growth of $In_xSn_{1-x}Te$ nanowires is limited by solubility variations and limits when produced by CVD of co-evaporation of InTe and SnTe sources [41]. Hence, the nanomolding synthesis of $In_xSn_{1-x}Te$ nanowire is of paramount interest for yielding naturally passivated narrow nanowires and maintaining their composition and crystallinity throughout their length.

Equally important is exploring the solid evidence for robust topological surface states, which requires overcoming surface passivation, controlling defect formation, and optimizing fabrication process of SnTe and In-doped SnTe nanowires at the same time. Observing the nontrivial ABOs in a SnTe nanowire with a magnetic field threaded along its axis would be a clear indicator of robust

surface states, which Safdar et al. demonstrated in SnTe nanowires [24, 33] but no follow-up studies can be found by other groups. As such, follow-up studies that reproduce key transport results should be carried out. Besides, it is unclear how ABOs will be manifested when the electronic states are superconducting. Additionally, the surface Dirac 2D carrier concentration can be extracted from the SdH oscillation data, allowing a more quantitative understanding of the topological surface states of SnTe nanowires. Therefore, illuminating electron behaviors in topological nanowires is of fundamental importance to disentangle the puzzle behind all the fascinating topological properties as promised.

Although beyond the scope of this dissertation, I would like to bring up some practical questions to tackle in searching for pathways to braid MBSs. TCI/topological superconductor (TSC) heterojunctions and TSC nanowire networks provide promising platforms to braid and demonstrate the non-abelian properties of MBSs. What is the coherence length associated with the topological band gap? What is the strength of MBS coupling? What is the quasiparticle poisoning time in such systems? These immediate questions need to be addressed for understanding and controlling the braiding of MBSs, and ultimately, robust quantum computation.

It is my sincere hope that this dissertation may serve as a stepping stone for interdisciplinary researchers who seek to understand the development and future of topological nanomaterials.

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Appendices

## Appendix A: Growth of SnTe Nanowires and In-doped SnTe Nanowires

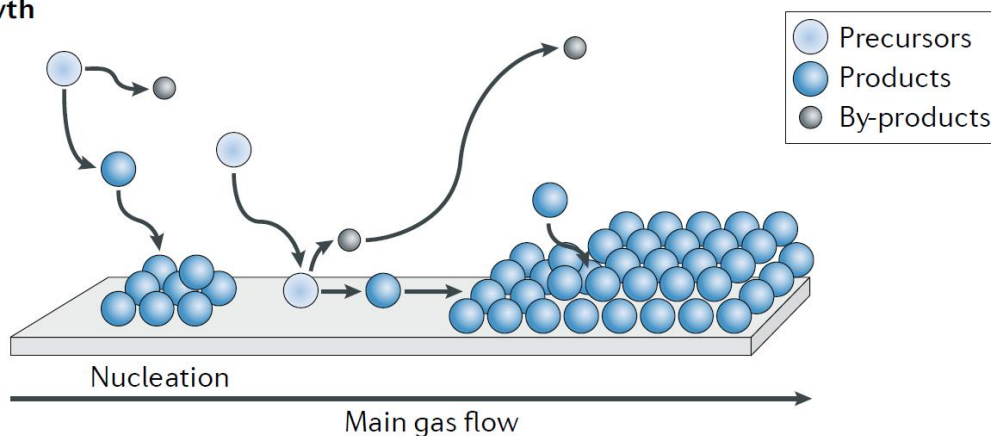### A.1 Vapor-liquid-solid and chemical vapor deposition growth of nanostructures

The two most popular growth techniques to synthesize topological nanomaterials are the VLS and CVD growth methods (Fig. A-1). VLS growth is a metal-catalysed nanowire growth method, which was first demonstrated to grow Si microwires [281]. In VLS growth, metal nanoparticles, typically gold nanoparticles, are used to catalyse growth, and the source materials are introduced as vapour. At growth temperature, the metal catalyst is in the liquid state and the gas molecules or atoms of the source material dissolve into the liquid metal particle. When the concentration of the source atoms in the liquid metal exceeds the thermodynamic solubility limit at the given growth temperature, the dissolved source atoms precipitate and form a crystalline solid at one end of the liquid metal particle. With continual supply of source vapour, an equilibrium is reached in which the metal particle maintains the solubility limit concentration by ejecting the excess dissolved atoms, lengthening the nanowire. A distinguishing feature of the VLS growth is that the diameter of the nanowire is precisely determined by the size of the metal nanoparticle [282]. This growth technique is widely used to obtain semiconducting nanowires, as well as heterostructure and core-shell nanowires

[283-285] for applications including field-effect transistors, solar cells, nanolasers, biosensors and thermoelectrics.
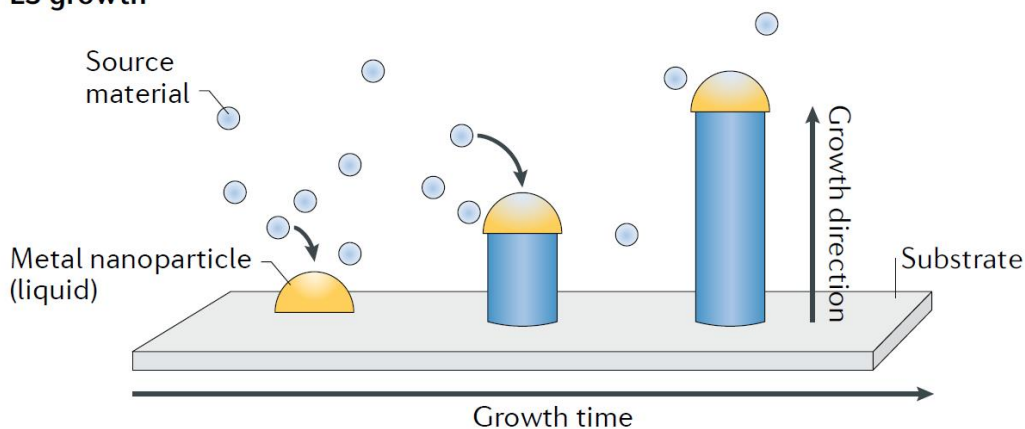
Figure A-1: Vapour-liquid-solid and chemical vapour deposition growth of nanostructures

(top) Schematic of liquid-solid growth of nanowires. (bottom) Schematic of chemical vapor deposition growth of nanostructures. Adapted with permission from P. Liu *et al.* Nature Reviews Materials. Copyright © 2019, Springer Nature Limited.

In CVD growth, gaseous source materials are deposited on a growth substrate to obtain thin films, microcrystals or nanostructures. The source materials can be introduced directly as vapour or can be vaporized by heating solid

powders. The source vapours are usually carried down to the substrate (which is kept at a lower temperature than the vapour) by an inert carrier gas and there they condense to form solid thin films or nanocrystals. If different source vapours are mixed, they may react with each other before condensing to form solids. Many 2D materials, such as graphene, hexagonal boron nitride and transition metal dichalcogenides have been grown by CVD [192, 286, 287]. Many topological nanostructures are grown using metal-catalysed CVD, which uses metal nanoparticles as nucleation catalysts. The metal-catalysed CVD is distinct from VLS because the width of the nanostructure is often much larger than the size of the metal nanoparticle.
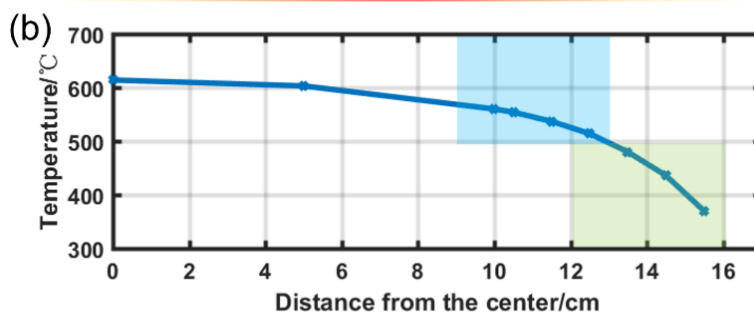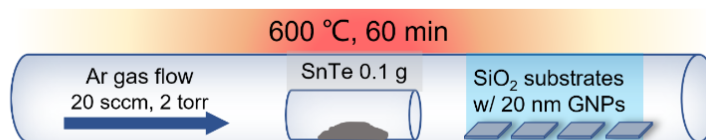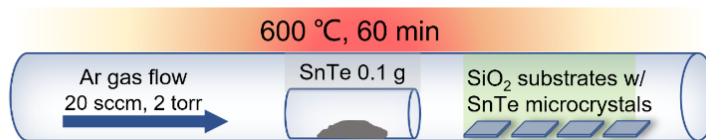
A.2 Thermal profile of the single-zone tube furnace

The following thermal profile is measured exclusively for the Lindberg-Blue Mini-Mite single-zone tube furnace (ThermoFisher) I used throughout the experimental study of this dissertation (Fig. A-2 and Fig. A-3). Fig. A-3 also displays the temperature range applied for the two-step CVD growth of narrow nanowires discussed in Chapter 4. It is noted that the temperature ranges for growth substrates are different in the first and second CVD process. In Chapter 5, I kept the temperature range of growth substrates identical in each CVD process to achieve a better comparison between passivated and unpassivated SnTe nanowires.
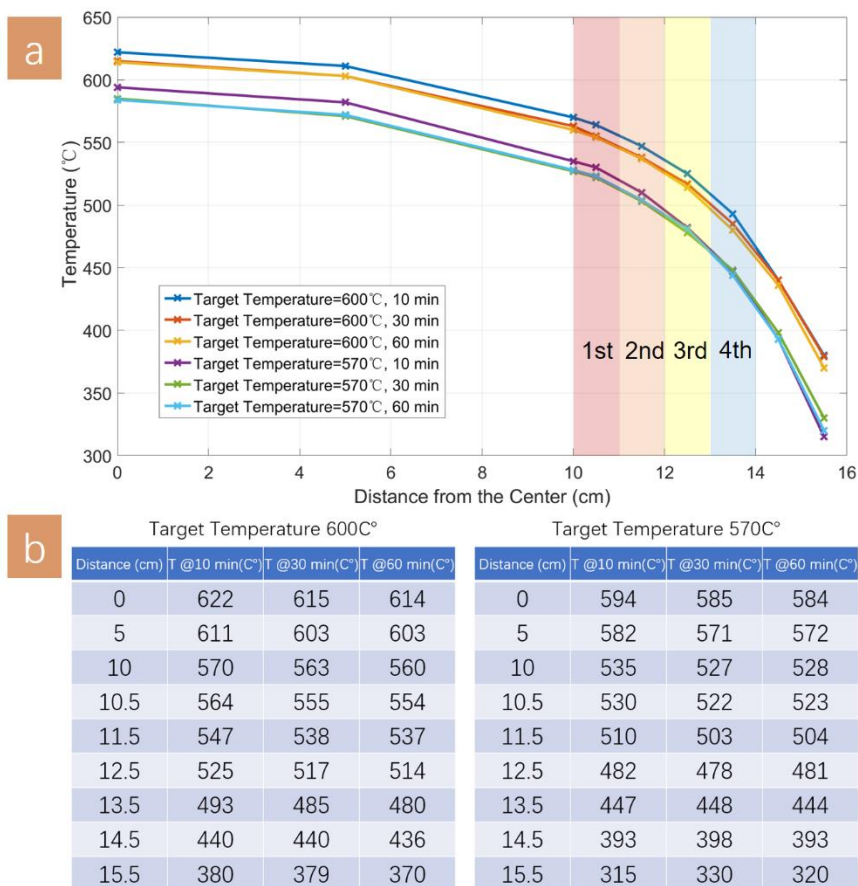
Figure A-2: Temperature profile of the tube furnace at various heating times

a, Temperature versus distance. Here, the distance is measured from the furnace center to substrate locations. Substrate temperatures were extracted from the shaded regions in **a**. The micro- and nanocrystals presented in the paper were obtained from the substrate placed at 11.5 cm from the center. **b**, Temperature measurements at corresponding positions.

(a) 1st Step: Growth

600 ℃, 60 min

Ar gas flow
20 sccm, 2 torr

SnTe 0.1 g

SiO$_2$ substrates
w/ 20 nm GNPs

(b)

Temperature/℃ (y-axis: 300, 400, 500, 600, 700)
Distance from the center/cm (x-axis: 0, 2, 4, 6, 8, 10, 12, 14, 16)

(c) 2nd Step: Annealing

600 ℃, 60 min

Ar gas flow
20 sccm, 2 torr

SnTe 0.1 g

SiO$_2$ substrates w/
SnTe microcrystals

Figure A-3: Thermal profile of the single-zone tube furnace

a, Substrates decorated with 20 nm Au particles were placed 9.5 cm to 12.5 cm away from the center of furnace during the first annealing step to make alloy nanoparticles. **b**, Temperature profile of the furnace as a function of substrate location. **c**, Substrates decorated with the alloy nanoparticles were placed 12.5 cm to 15.5 cm away from the center for the synthesis of narrow SnTe nanowires.

Appendix B: Device Fabrication Process of SnTe Nanowires

SnTe nanowires are fabricated into nanoscale devices for transport measurement as depicted in Fig. B-1. The synthesized nanowires are transferred onto 300 nm SiO_2/Si substrates and spin-coated with copolymer layers of ~300 nm methyl methacrylate (MMA EL 8.5, MicroChem) at 4000 RPM for 2 min and cured for 2 min at 180ºC, followed by ~200 nm poly-methyl methacrylate (PMMA A3, MicroChem) e-beam resist at 4000 RPM for 2 min and cured for 2 min at 180ºC (cross-sectional schematic in Fig. B-2). For nanoscale patterning, a CAD program (LayoutEditor) is used to design electrode patterns, and a Vistec EBPGRaith EBPG 5000+ electron-beam lithography system with a 100 kV beam is used to expose samples with a 1200 $\mu C/cm^2$ dose and 100 nA current. After exposure, samples are developed for 2 minutes in a solution of isopropanol:H_2O=3:1 by volume. Then, the Oxford 100 Reactive Ion Etcher is used to remove surface oxides and resist residues from the exposed areas after the four-terminal device pattern is developed. The samples are etched for 2 minutes at 40 W power with the Ar gas flow of 40 sccm. The samples are then loaded in a thermal evaporator for contacts formed by a wetting layer of 15 nm Cr followed by 200 nm Au. All of the electrical and magnetic field measurements are performed using the Quantum Design (QD) Dynacool system at a base temperature of 1.7 K. Four-probe resistance is measured with an AC lock-in technique at 17.78 Hz using source currents of 50 nA to 1 µA. Magnetoresistance is measured in perpendicular magnetic fields up to 14 T at 1.7 K.
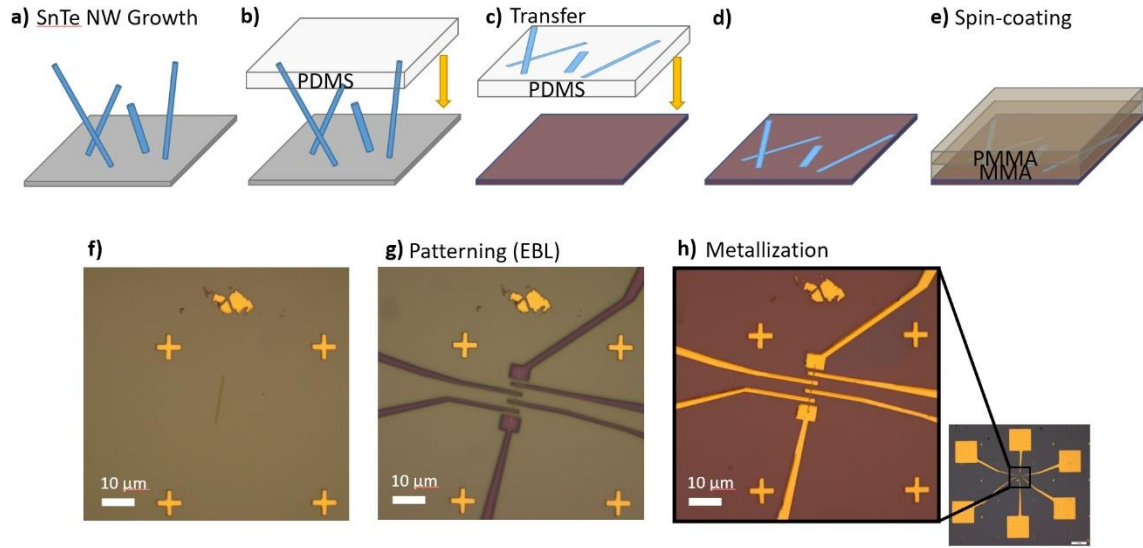
Figure B-1: Nanowire device fabrication process

a, The as-grown substrate of SnTe nanowires. **b,** Using a PDMS stamp to pick up SnTe nanowires from the as-grown substrate. **c,** Pressing the PDMS stamp onto a clean 300nm SiO_2/Si substrate with gold alignment markers to transfer nanowires. **d,** The SiO_2/Si substrate with transferred nanowires. **e,** Spin-coating of the PMMA/MMA resist. **f,** An optical image of the substrate prepared in **e**. **g**, After patterning using EBL and developing, the substrate is ready for metallization. **h**, A typical 6-terminal nanowire device after deposition of metal contacts and lift-off.
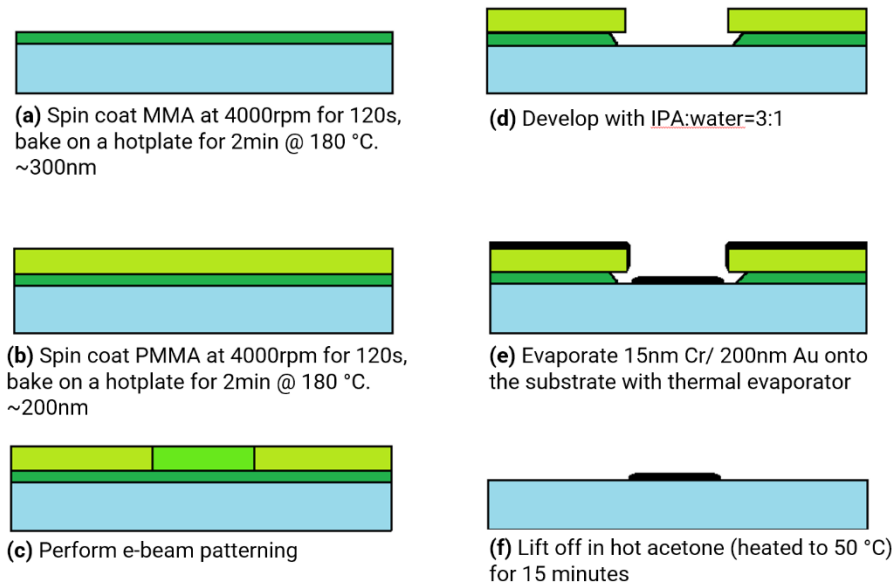
Figure B-2: Typical bilayer e-beam resists process

Schematics of the typical copolymer e-beam resists process, stating from (**a,b**) spin-coating of MMA/PMMA layers. **c**, electron beam lithography patterning. **d**, Develop the pattern. **e**, metallization of contacts using either thermal/e-beam evaporator. **f**, lift-off process to finalize the fabrication.

Appendix C: Study of Superconductivity in SnTe Nanowires

C.1 Kitaev model for a spinless 1D wire with *p*- wave superconducting pairings

The canonical model that captures the physics of topological superconductivity was originally developed by Kitaev [176]. Kitaev considered a 1D wire of spinless fermions with *p*-wave superconducting pairing and N total sites. The Hamiltonian is

$$H = -\mu \sum_j c_j^\dagger c_j - \frac{1}{2} \sum_j \left(-\omega \left(c_j^\dagger c_{j+1} + c_{j+1}^\dagger c_j \right) + \Delta c_j c_{j+1} + \Delta^* c_{j+1}^\dagger c_j^\dagger \right),$$
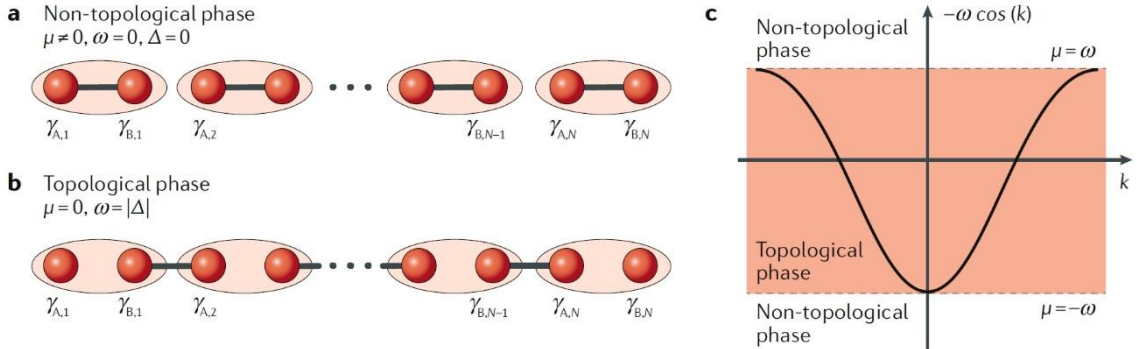
Figure C-1: Kitaev model for a spinless 1D wire with *p*-wave superconducting pairings

Where *c* are creation operators, ω is the nearest-neighbor hopping strength between sites (labelled *j*), μ is the chemical potential, and $\Delta = |\Delta| e^{i\varphi}$ is the *p*-wave pairing amplitude. We can rewrite this Hamiltonian by defining the creation and annihilation operators in terms of two MBSs, $\gamma_{A,j}$ and $\gamma_{B,j}$, at each site *j*, and

combine the superconducting pairing phase φ to get $c_j = \frac{e^{i\varphi}}{2}(\gamma_{A,j} + \gamma_{B,j})$. The Hamiltonian becomes

$$H = -\frac{\mu}{2}\sum_{j}^{N}(1 + \gamma_{A,j}\gamma_{B,j}) - \frac{i}{4}\sum_{j}^{N-1}\left[(\omega + |\Delta|)\gamma_{A,j+1}\gamma_{B,j} + (-\omega + |\Delta|)\gamma_{A,j}\gamma_{B,j+1}\right].$$

We can consider two limiting cases. When $\mu \neq 0$ (and $\omega = \Delta = 0$), each pair of MBSs is paired on a site j (Fig. C-1a). However, when $\mu = 0$ and $\omega = |\Delta|$, the Hamiltonian is given by $H = i\omega\sum_{j}^{N-1}\gamma_{A,j+1}\gamma_{B,j}$. In this scenario, a MBS on site j is coupled to a MBS on $j+1$ or $j-1$ and, importantly, the MBS A at $j = 0$ and the MBS B at $j = N$ are not coupled to their neighbour and do not appear in the Hamiltonian: the system supports unpaired zero-energy MBSs at the end of the chain (Fig. C-1b). In the Kitaev model, the fermionic operators are written in terms of two MBSs, which can be done for any system. This is just a mathematical construct, as the two MBSs are localized at the same spot. The key is that under the right conditions ($\mu = 0$ and $\omega = |\Delta|$), the system undergoes a phase transition accompanied by the opening of a topological gap [176], resulting in a pair of MBSs being localized far apart. Pairs of nonlocal MBSs like those at the ends of a 1D chain form a highly degenerate ground state, and exchange of any two such MBSs transforms the state in a non-commutative way, exhibiting non-Abelian statistics [178]. In this toy model, MBSs do not exist only at $\mu = 0$ and $\omega = |\Delta|$. An investigation of the parameter space shows regions with topologically trivial and non-trivial gaps (Fig. C-1c) [238], which can be tuned by changing μ with a gate voltage. At $\mu = |\omega|$, a topological quantum phase transition occurs.

C.2 Josephson detection of time-reversal symmetry broken

superconductivity in SnTe nanowires

In collaboration with Prof. James Williams and his group member Dr. Christie Trimble at University of Maryland, we report the detection of time-reversal symmetry broken superconductivity in SnTe nanowires [278]. A Josephson junction (JJ) couples the supercurrent flowing between two weakly linked superconductors to the phase difference between them via a current-phase relation (CPR). While a sinusoidal CPR is expected for conventional junctions with insulating weak links, devices made from some exotic materials may give rise to unconventional CPRs and unusual Josephson effects. In this work, our collaborators present such a case: they investigate the proximity-induced superconductivity in SnTe nanowires by incorporating them as weak links in JJs and observe a deviation from the standard CPR. They report on indications of an unexpected breaking of time-reversal symmetry in these devices, detailing the unconventional characteristics that reveal this symmetry breaking. These include an asymmetric critical current in the DC Josephson effect, a prominent second harmonic in the AC Josephson effect, and a magnetic diffraction pattern with a minimum in critical current at zero magnetic field. The analysis examines how multiband effects and the experimentally visualized ferroelectric domain walls give rise to this behavior, giving insight into the Josephson effect in materials that possess ferroelectricity and/or multiband superconductivity.

They also fabricate Josephson junctions using In-doped SnTe nanowires and measure them in their dilution refrigerator, which has a base temperature of

about 25 mK. They show the divergence of at least three devices from standard Josephson junction behavior using DC techniques. For In-doped SnTe JJs, the minimum resistance is not at zero magnetic field, and the differential resistance is asymmetric about zero DC current (Fig. C-2a). For SnTe JJs, the critical current is a minimum at zero field when the fridge temperature is below 240 mK (Fig. C-2b). Reasons for the origin of these exotic behaviors in terms of the interplay between *s*-wave and *p*-wave order parameters is still under investigation.
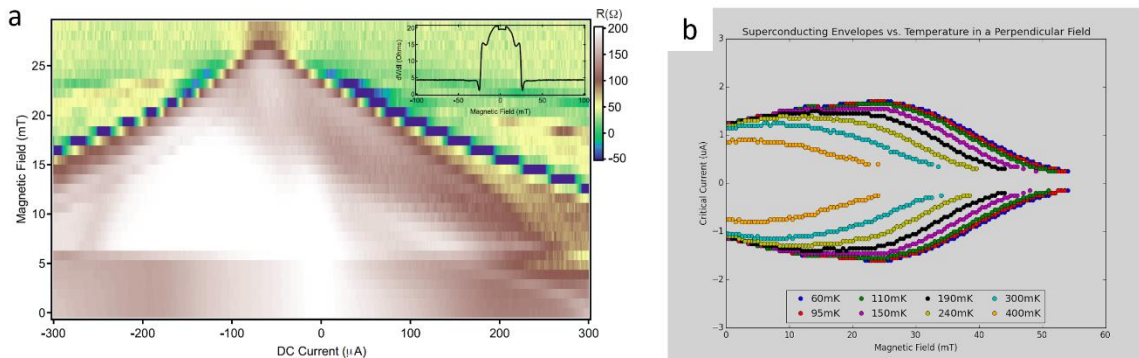

Figure C-2: Anomalous Josephson junction behavior detected using DC techniques

a, Magnetic diffraction pattern for In-doped SnTe nanowire Josephson junctions. **b**, Temperature-dependent superconducting envelopes. Courtesy of Prof. James Williams and Dr. Christie Trimble from University of Maryland, College Park.

Appendix D: **Material Characterization and Simulation**

D.1 Electronic microscopy imaging conditions

SEM images and SEM-energy-dispersive X-ray spectroscopy (EDX) of SnTe nanowires were recorded using a Hitachi SU8230 cold field emission operated at 10 kV. The surface defects in Chapter 3 were probed by lowering the acceleration voltage (Fig. D-1). In Chapter 4, TEM imaging and TEM-EDX analysis were carried out using a 200 kV FEI Tecnai Osiris TEM. The *in situ* cryo-TEM experiments were performed using Gatan liquid-helium cooling holder (HCTDT 3010) and JEOL ARM200CF operated at 200 kV at Brookhaven National Laboratory.
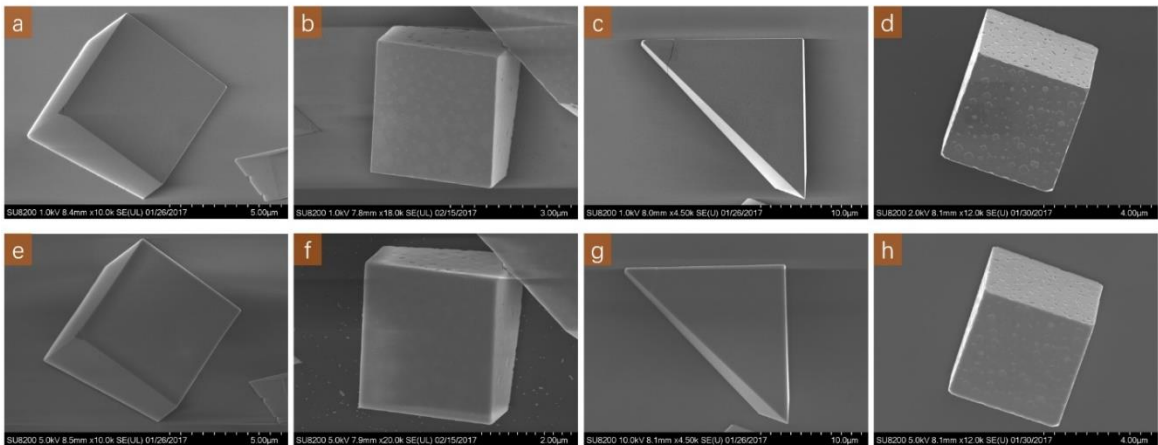
Figure D-1: Comparisons of SEM images taken at various accelerating voltages from 1 to 10 kV

SnTe microcrystals are synthesized on three different substrates. **a, e**, On a mica substrate; **b, c, f, g**, on 300 nm SiO_2/Si substrates; **d, h**, on a Si substrate. Images in each column correspond to the same microcrystal. Because of the charging issue, surface pits on SnTe microcrystals synthesized on mica and SiO_2/Si substrates are more difficult to be resolved than those ones on Si substrates. Compared with images taken at **e, f, h** 5 kV or **g** 10 kV, images acquired at lower accelerating voltages **a, b, c** 1 kV or **d** 2 kV can reveal surface pits more clearly. Imaging conditions are provided at the bottom of each image.

D.2 Diffraction simulations for *in situ* cryo-TEM data

In Chapter 4, electron diffraction simulations were performed with the multislice method using the Computem software package (Kirkland, Advanced Computing in Electron Microscopy, Springer US, 2010). The polar SnTe structure was taken from Ref.[275]. Initially, a polar SnTe crystal was aligned with the [001] crystal axis parallel to the simulation *z*-axis (the TEM optic axis). To form the 109° DW, the crystal was duplicated and rotated 90° about the simulation *z*-axis and then 90° about the simulation *x*-axis. The second crystal was then adjusted so that the (100) planes of the two crystals were coincident. Separate diffraction simulations were performed for the initial and rotated crystals, and then the simulation patterns were overlaid. A similar procedure was performed for the 71° DW, except the crystal was only rotated 90° about the *z*-axis, and then the (110) planes were made coincident. The crystals were disk-shaped, 16 nm thick and 40 nm in diameter, and were embedded in an 80 x 80 nm^2 simulation cell. The step size was 0.1 nm.

Appendix E: **Wire-Bonding Process**

In this dissertation, all of the electrical and magnetic field measurements are performed using the Quantum Design (QD) Dynacool Physical Property Measurement System (PPMS). To interconnect the metal leads on PPMS sample boards (pucks) to the electrodes on SnTe 4-probe nanowire devices, we use the Westbond 7476E ultrasonic wire bonder with 50 μm aluminum wires. Bonds are made by the wedge-wedge technique using ultrasonic vibration energy to attach aluminum wire at room temperature. Wire is clamped and threaded diagonally under the bonding wedge, allowing independent feeding action but requiring front-to-back bonding direction.
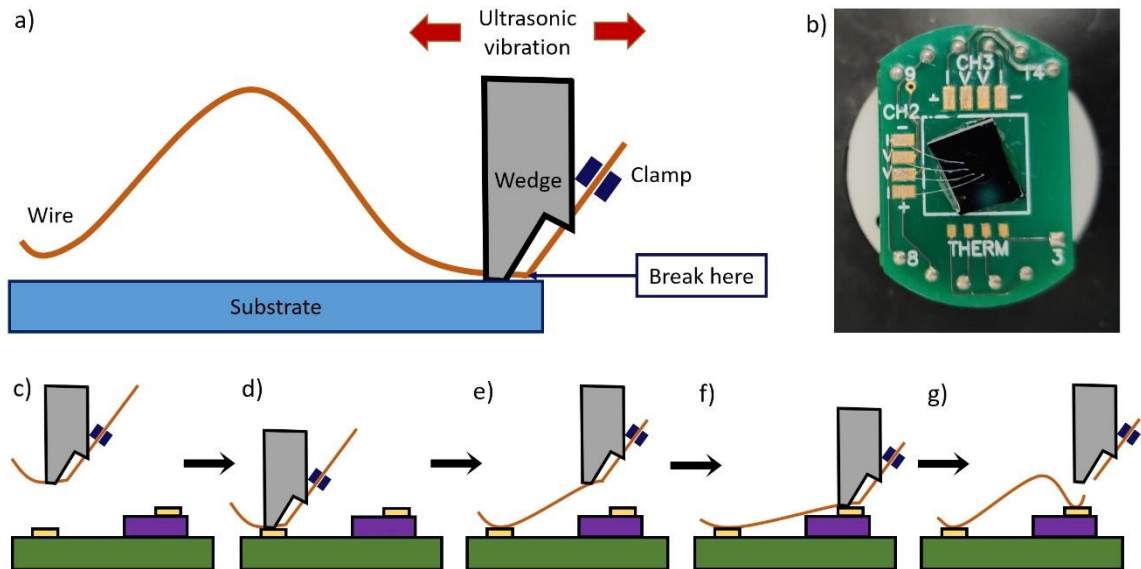
Figure E-1: Wire-bonding process

a, Schematic of wire attachment during the wire-bonding process. **b**, An image showing interconnected bonding between the metal leads on a rotator sample board and the electrodes of a 4-probe SnTe nanowire device. **c-g**, Step-by-step illustration of a bonding sequence as described in this section.

The wire-bonding process is depicted in Fig. E-1. First, an aluminum wire on the tip of the wedge is brought adjacent to a metal lead. To form an attachment, we gently press the wedge on the metal lead so that the ultrasonic energy at its tip can melt the aluminum wire. After forming the first bond, the wire is pulled towards the electrode on the device and pressed on it to form the second bond, followed by pulling and cutting the wire. There are two parameters that can be programmed to ensure successful wire bonding: ultrasonic power and ultrasonic time. Although proper bonding settings vary from puck to puck, I would like to offer my usual settings as a reference, as shown in Table E-1.

Type of sample puck	1st bonding power	1st bonding time	2nd bonding power	2nd bonding time
Regular	375	75	200	75
Rotator	400	75	200	75

Table E-1: Bond settings for wire-bonding process using different types of sample boards

Before the wire-bonding process, I always ground myself by wearing the anti-static wristband connected to the PPMS chamber. During the wire-bonding process, PPMS sample boards should be always grounded by connecting the user bridge to the real ground using an alligator clip or coated metal wire.