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Review

A Review on Direct Digital Conversion Techniques for Biomedical Signal Acquisition

Yizhao Zhou [1], Shuang Song [2], Shiwei Wang [3], Yalong Wan [2], Tian Yang [2], Xiaopeng Yu [2] and Menglian Zhao [1,*]

[1] College of Information Science and Electronics Engineering, Zhejiang University, Hangzhou 310027, China; zhouyizhao@zju.edu.cn
[2] School of Micro-Nanoelectronics, Zhejiang University, Hangzhou 310027, China; shuangsonghz@zju.edu.cn (S.S.); yalongwan@zju.edu.cn (Y.W.); 22241046@zju.edu.cn (T.Y.); yuxiaopeng@zju.edu.cn (X.Y.)
[3] Institute for Integrated Micro & Nano Systems, School of Engineering, University of Edinburgh, Edinburgh EH8 9JU, UK; shiwei.wang@ed.ac.uk
* Correspondence: zhaoml@zju.edu.cn

Abstract: Biomedical signals such as Electrocardiogram (ECG), Electroencephalogram (EEG) and photoplethysmography (PPG) are recorded routinely to provide helpful information for early diagnosis of disease. Low power consumption is very important to allow long-term ambulatory monitoring with battery-powered systems. A direct digital conversion (DDC) technique has been proposed in recent years, which employs preamplifier and data converters, reducing the complexity of the readout chain and thus its power consumption. This paper provides a review on DDC for biopotential signals and bio-optical signal acquisition. The state-of-the-art DDC-based readout architectures together with circuit implementations are provided.

Keywords: biomedical signal; electrocardiogram; electroencephalogram; photoplethysmography; direct digital conversion

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1. Introduction

Home-based health monitoring through wearable devices is becoming prevalent. Low power consumption is very important to allow long-time monitoring. Besides power consumption, for multiple-channel applications such as neural recording, there are also requirements of a small size and minimum off-chip components.

There are mainly two categories of biomedical signals: biopotential signals such as Electrocardiogram (ECG) and Electroencephalogram (EEG), and bio-optical signals such as photoplethysmography (PPG) and near infrared spectroscopy (NIRS). Interestingly, they share a similar signal pattern, which is a small useful component superposed on a large quasi-DC component [1]. Traditional biopotential signal readouts consist of an AC-coupled preamplifier followed by an analog-to-digital converter (ADC) [2]. To reliably achieve a sub-Hz high pass frequency, large off-chip components are needed. Meanwhile, DC-coupled structures have a limited gain, reducing the effective resolution on the useful AC signal at the ADC output. Traditional bio-optical signal readout circuits use an integrator or a transimpedance amplifier (TIA) to convert the photocurrent to a voltage that is then digitized by an ADC [3]. However, the architecture of using TIA is prone to noise folding. In addition, due to the low perfusion index (PI) of the chest PPG signal, a larger dynamic range (DR) is required for the readout circuit, which undoubtedly increases the complexity of the design and power consumption.

In recent years, a direct digital conversion (DDC) structure has been proposed to directly digitize biomedical signals, which overcomes the above problems by combining

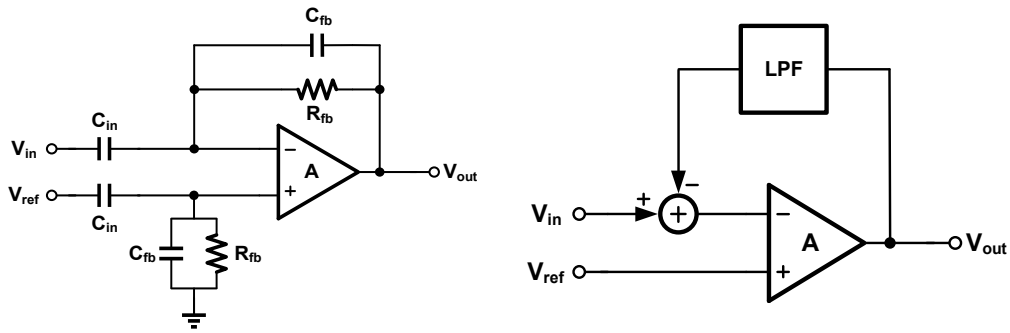
preamplifier and ADC into one stage while making compromises among area, noise, power, and input impedance, etc.

In Section 2, we describe the techniques for neural signal recording. In Section 3, the techniques for voltage-controlled oscillator-based signal recording are presented. In Section 4, we discuss the techniques for PPG/NIRS signal recording. In Section 5, we conclude with the focus of neural signal recording and PPG/NIRS signal recording.

2. Techniques for Biopotential Signal Recording

Multi-electrode neural recordings are becoming standard practice in neuroscience research to gain knowledge on the way the brain works and enable neuro-prosthetic applications. There is a clear need for a higher number of recording sites per given area, which provides real-time signals at the level of neurons from an ever-increasing brain volume. In parallel with the requirements of signal integrity and low power consumption, a miniature IC chip area with the minimum number of off-chip component is of paramount importance to enable hundred-channel neural probes [4].

One of the main issues leading to a large chip area is the electrode DC offset originating from the electrode–electrolyte interface [5]. This offset can reach the levels of up to 100 mV depending on the type of material of the electrode and the surrounding tissue and fluids [5], which is higher than the actual neural signals, i.e., action potential (AP) around 1 mV and local field potential (LFPs) around 10 mV. While accepting this large DC offset would lead to a limited gain of frontend amplifier and very high resolution of ADC with high power, the common solution is to reject the DC component with a passive or active filter, as shown in Figure 1.



(**a**) (**b**)

Figure 1. (**a**) Conventional AC-coupled neural amplifiers; (**b**) digitally assisted DC-coupled neural amplifiers.

The high pass corner frequency can be expressed as $f_{HP} = 1/2\pi R_{fb}C_{fb}$. With the properly chosen R_{fb} and C_{fb}, the filter cut-off should be made under 1 Hz to capture the complete signal band of the LFPs while rejecting the DC signal. In terms of circuit design, this approach may be challenging because high product $R_{fb}\bullet C_{fb}$ requires high values for one or both of the filter elements. Achieving both high capacitance capacitor and high resistance resistor values requires a large circuit area. Pseudo-resistors, as shown in Figure 2 (n is design parameter and U_T is the thermal voltage), can be used with a small area, but it can exhibit an X0.1 to X10 variation over PVT and be sensitive to light exposure [6]. The direct digital conversion technique can provide DC rejection capability with an extremely small chip area.

To the best of the authors' knowledge, the first DDC for biopotential signal readout was proposed by H. Kassiri et al. [7]. Figure 3a shows a conventional first-order $\Delta\sum$ ADC; this circuit has a tradeoff between integrated noise, oversampling rate (OSR), and power consumption. As a result, with an anticipatory design, it can satisfy a neural recording front-end requirement of bandwidth, noise, and power. However, any DC offset from the electrode can make the amplifier saturated.

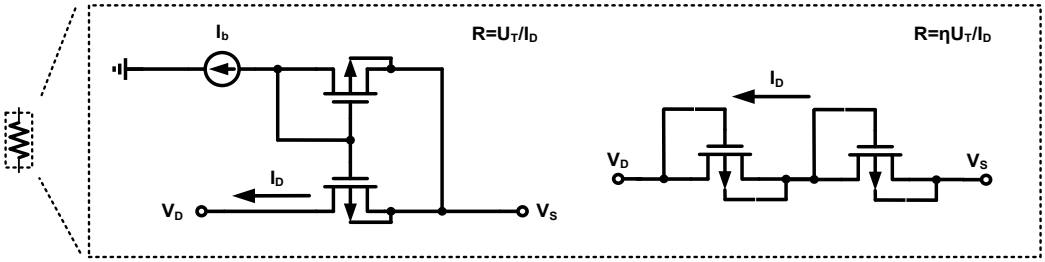


Figure 2. Pseudo-resistor realized by current bias.

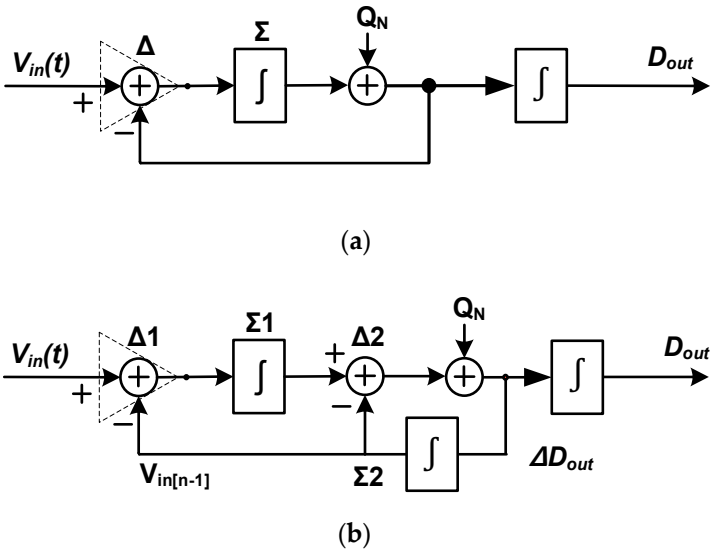


Figure 3. (**a**) Classical first-order Δ∑-based ADC; (**b**) first-order Δ^2∑-based ADC.

In order to improve the suppression of the electrode DC offset (EDO) while maintaining a high chain gain, the so-called Δ^2∑structure added an additional Δ stage to the Δ∑modulator as shown in Figure 3b. As a result, the difference of two consequent input signals is fed into the DDC, which removes the DC component, avoiding integrator saturation. The output of the quantizer is thus the derivative of the input signal, and it can be integrated into the digital domain to reconstruct the AC component of the original signal. In the feedback path, the DAC and integrator is implemented by a digital controlled charge pump. Although this structure enables EDO rejection in a rail-to-rail range, integration using IDAC results in an insufficient ability to track fast transients due to the large time constant of the integrator. Moreover, a DT Δ^2∑ADC needs a high OSR to avoid KT/C noise aliasing at the cost of limited input impedance. As a result, the differential-mode signal caused by different high impedances of the microelectrode attenuates the ability of immunizing large artifacts.

Figure 4 shows an op-amp-less Δ-modulator diagram using a continuous-time Δ-ADC [8] to achieve the shaping the spectra of neural signals such as LFPs and ECoG, which can decrease the DR requirement of recording front end by more than 30 dB. Meanwhile, this structure achieves above GΩ input impedance because it uses the DC-coupled front end without input capacitors. However, without noise shaping, low-frequency noise of the system is high, so that SNDR is limited.

A second-order hybrid continuous time to discrete time (CT-DT) Δ∑-∑modulator [9] was presented as shown in Figure 5. The structure adds a ∑ stage to a conventional two-order Δ∑-modulator, thus achieving three-stage noise shaping and one-stage input signal shaping. Therefore, by considering calculation and design, this architecture can offer a good tradeoff between input range, EDO cancelation, noise and linearity. In addition, to ensure the input impedance in case of using chopping, an auxiliary input impedance boosting path is implemented. However, the realized input impedance is only 34 MΩ.

A simple digital accumulator is used to obtain fast recovery from large motion artifacts (MA). This structure can simultaneously suppress EDO and an MA of >300 mV. However, the linearity of the system is limited due to the use of a five-bit quantizer and capacitive digital-to-analog converter (CDAC).

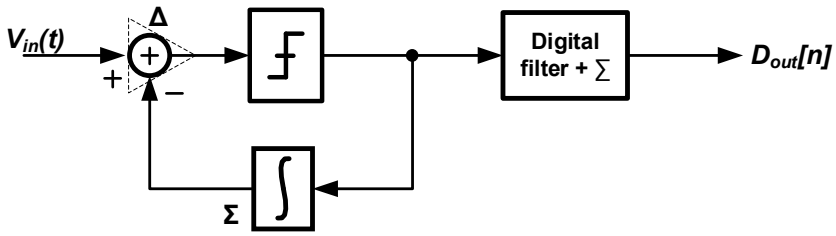


Figure 4. Block diagram of Δ-modulator.

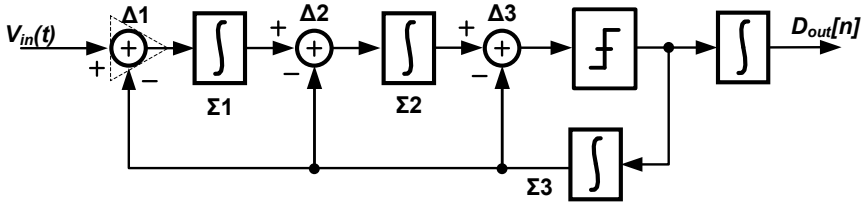


Figure 5. Block diagram of Δ∑-∑modulator.

C. Kim proposed another second-order hybrid DDC architecture [10] as shown in Figure 6. This system connects the biopotential signal directly to the second integrator which is implemented in continuous time and moves the sampling to the comparator to avoid sampling noise kT/C. Similar to [7], this structure uses predictive digital auto-ranging (PDA) for high-input-dynamic range and avoiding the need for substantial gain attenuation. Moreover, PDA substantially improves transient response to large artifacts, tracking full-swing signal excursions without saturation while quickly reestablishing noise-limited resolution upon the settling of the signal. Finally, fast transient recovery of 200 mV/ms is achieved with a 90 dB input dynamic range, less than 1 μVrms input-referred noise from DC to 500 Hz, at a 0.8 μW power consumption, and with a 0.024 mm^2 area. However, the input impedance of this work is still relatively low (26 MΩ).

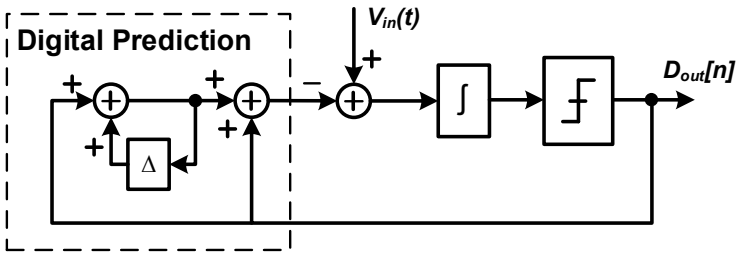


Figure 6. Block diagram of Δ-Δ∑modulator.

Works [7,9,10] employed switched cap/chopping circuit at the input as shown in Figure 7a, which leads to a limited input impedance. Recently, Gm-C-based structures have been proposed to solve this problem. S. Wang exploited the current feedback gm stage [11] as the CT-integrator within a $\Delta^2\sum$ architecture [12], which is shown in Figure 7b. The inherent high Z_{in} of the gm stage together with the proposed bootstrapping increase the input impedance to 663 MΩ, which is shown in Figure 8. The EDO rejection of this work is, however, only ±70 mV. M. Sporer proposed a Gm-C-based second-order delta sigma modulator in [13] using bulk-driven DSL. The structure achieves a bandwidth of 10 kHz and an input impedance of 238 MΩ, while the EDO rejection range is only ±100 mV. A similar structure was proposed in [14]; however, its linearity is limited due to the open-loop

Gm-C stage. Readout circuits in other fields [15,16] can also offer some ideas. An energy-efficient readout IC [15] achieves 133 dB SNR and 134 dB CMRR, which consists of a CCIA driving a CT-Δ∑M. In [16], a CT-integrated readout interface was presented for inertial sensors with high energy efficiency and high resolution.

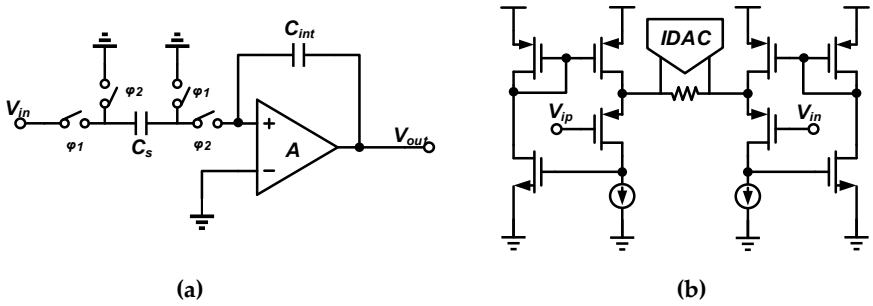


Figure 7. (**a**) A discrete-time integrator; (**b**) A continuous-time integrator Gm stage.

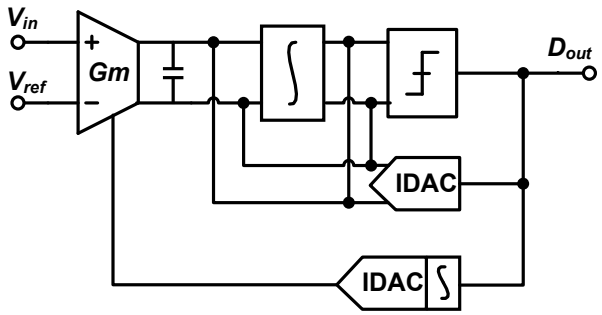


Figure 8. Gm-C-based Δ-Δ∑ modulator.

Table 1 summarizes the performance of state-of-the-art DDC-structured biopotential readout circuits. In [7], a DT Δ-Δ∑ structure was implemented to eliminate the input DC offset, which achieved rail-to-rail offset tolerance. A high OSR (1000) is needed to reduce kT/C noise. Such high switch frequency with a capacitor leads to a limited input impedance (<100 MΩ). In [9], a hybrid CT-DT Δ∑-∑ modulator was used which achieves three-stage noise shaping. The low-gain (gain = 8) stage needs large power consumption (15 μW) to reduce input-referred noise. The system linearity is limited by a five-bit quantizer and a five-bit CDAC. In [10], another second-order hybrid DDC architecture was proposed which connects the input signal to the second integrator avoiding kT/C noise. This work implemented a PDA for high input range, avoiding the requirements of gain. Therefore, the system offers a good tradeoff between noise (<1 μVrms) and input range (90 dB). However, the input impedance is still relatively low (26 MΩ). In [8], an op-amp-less Δ-modulator was proposed which achieves spectra shaping of low-frequency signals to relax the DR requirement. This work has an above GΩ (2.94 GΩ) input impedance because there are no input capacitors. Without an op-amp, the system only occupies 0.044 mm^2. However, without noise shaping, SNDR (60 dB) is limited. In [12], a current feedback gm stage was proposed as the CT-integrator within a $\Delta^2\sum$ architecture. A second-order noise shaping (OSR = 512) was used to achieve low quantization noise. However, the flicker noise of current mirror was not chopped, so that the noise (2.88 μVrms) of the system was not low enough. In order to boost input impedance, this work implemented bootstrapping first gm stage, which limited EDO tolerance (70 mV). In [13], a Gm-C-based second-stage Δ∑-modulator was used with bulk-driven DSL. It achieved a 238 MΩ input impedance with low OSR (136) and small input capacitor (60 fF). In [14], a similar structure was used, achieving low noise (3.9 μVrms) with a 0.0046 mm^2 area.

Table 1. Performance of state-of-the-art DDC biopotential readout circuits.

	[7]	[9]	[10]	[8]	[12]	[13]	[14]
Technology (nm)	130	180	65	130	55	180	180
Supply (V)	1.2/2.5	1.8	0.8	0.6/1.2/3.3	1.2	1.8	1.8
Architecture	$\Delta^2\sum$	$\Delta\sum^2$	$\Delta^2\sum$	Δ	$\Delta^2\sum$	2nd order $\Delta\sum$	Gm-C I-$\Delta\sum$
NO. of channel	64	-	16	16	16	16	8–24
Zin (MΩ)	<100	34	>26	2960	663	238	-
Input range (mVpp)	-	720	260	-	148	19	14
Input noise (μVrms)	1.13	0.98	0.98	2.6	5.53 [1]	5.55 [1]	3.93 [1]
Bandwidth (kHz)	0.5	0.1	0.5	0.5	10	10	10
EDO tolerance (mV)	±1200	>±300	±130	±1500	±70	±100	±100
SNDR (dB)	72.2	66.2	66	60	59.5	61.1	57.5
Power/channel (μW)	0.63	73.8	0.8	0.99	61.2	12.8	14.94
Area/channel (mm^2)	5.98	0.48	0.024	0.011	0.0077	0.02	0.0046

[1] Input noise at frequency of AP.

Overall, compared to the DT delta-sigma DDC structure, the CT (continuous-time) delta-sigma DDC structure is more favored in neural signal acquisition systems because it does not require a high oversampling ratio and hence avoids noise aliasing. If a large input range is the primary requirement of the system, the preferred approach is to use low gains and $\Delta\sum$-$\sum$ structures [10]. When input impedance is of paramount importance, a system that does not use a large input capacitance becomes the primary choice [8,12]. When considering the number of acquisition channels limited by chip area, using the Gm-C structure without capacitors as an integrator has advantages, as demonstrated in [13,14].

3. Techniques for Voltage-Controlled Oscillator (VCO)-Based Signal Recording

Although the CT-$\Delta\sum$modulator achieves a high dynamic range, low noise and high input impedance at the same time, the supply voltage cannot be easily reduced to a sub-1V range because the output signal amplitude and thus the overall SNR/SNDR are always limited by the supply. This makes the front ends difficult to implement in a more advanced technology node together with the ever-complicated digital processing circuits, which benefit significantly from Moore's law. Frequency-domain separation is a workable approach to reduce supply and cancel artifacts [17].

Therefore, W. Jiang proposed a VCO-based neural signal recording system [18] in 2017 which is able to work at a 1.2 V supply while providing similar performance as that of the CT-$\Delta\sum$ architecture. Instead of processing input signal in the voltage domain, it directly converts voltage into the frequency domain by using VCO. Due to the high voltage-to-frequency gain of VCO, the input signal can be applied directly to the VCO without preamplifier, as shown in Figure 9, achieving a high input range together with low noise. To maintain high SDNR of system, the VCO nonlinearity can be corrected by foreground correction. In this work, it is implemented by a fifth-order polynomial VCO tuning curve stored in the digital circuits. The VCO-based neural signal recording system achieves a ±50 mV input range and a 76 dB SNDR. Meanwhile, it occupies 0.135 mm^2 with an analog power of 3 μW and a digital switching power of 4 μW. The disadvantage of this loop architecture is that it may still limit the linearity of system because of PVT variations, even with a nonlinearity calibration effort.

To avoid this limitation of open-loop VCO-based system, a closed-loop CC-VCO-based sensor readout system featuring hybrid PLL-$\Delta\sum$modulator is proposed in [19]. As shown in Figure 10, the dual VCOs integrate the input voltage to create phase variation, which is subsequently detected by phase frequency detector (PFD). The PFD acts as an integrator that generates the sum of input phase difference. Compared to classic PLL, this work uses an array of 15 PFDs instead of only one PFD as an efficient quantizer. The dual VCO structure allows the PFD to perform self-comparison without an extra phase. The PFD array can detect every delay stage of VCOs which naturally create a set of evenly phase-shifted

PWM waveforms without a classic barrel-shifter. Thus, by sampling the PFD array, the quantized phase difference can directly be regarded as output and CDAC control signal. The use of all VCO phases allows low VCO frequency without information loss, which avoids high-speed VCO to save power and area. The prototype readout system achieves a 78 dB SNDR in 10 kHz BW, consuming 4.5 μW and a 0.025 mm^2 active area with a 172 dB FoM. Although this work has an excellent tradeoff between power, area, input range and noise, the input impedance is reduced since a chopper is applied.

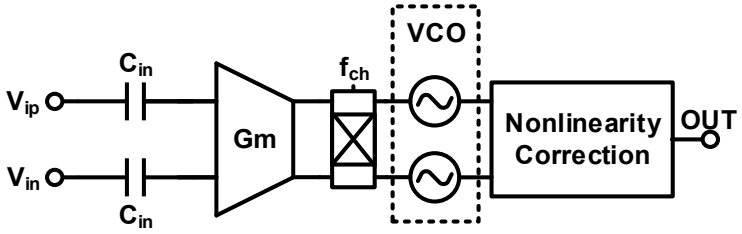


Figure 9. Block of VCO-based modulator.

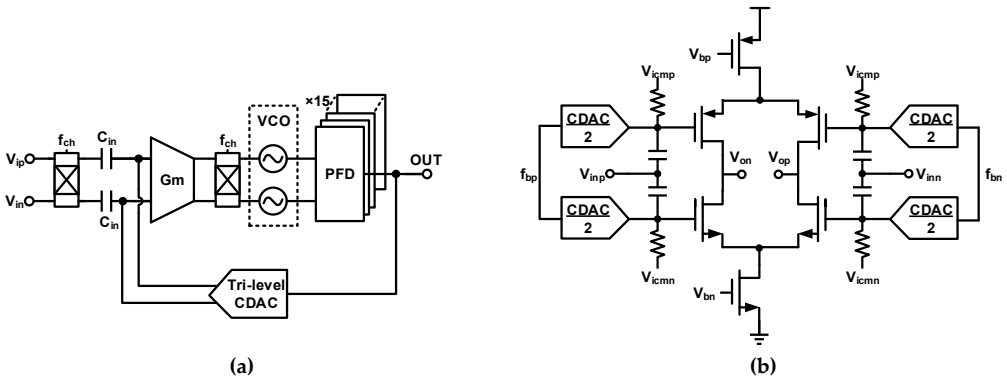


Figure 10. (**a**) The conceptual diagram of the proposed PLL-ΔΣM system; (**b**) schematic of Gm stage.

Jiannan Huang proposed a ΔΣ-modulator structure using a VCO-based quantizer [20] while avoiding the drawback of nonlinearity by applying differential pulse code modulation (DPCM). As shown in Figure 11, the predictor is designed to exploit the correlation between the adjacent sample of the input signal so that the quantizer only needs to deal with the remaining prediction error. It allows reducing the nonlinearity of the VCO quantizer by lowering the signal swing at the input of the VCO quantizer. In addition, oversampling increases the correlation between the adjacent sample of the input signal, so a high oversampling rate (OSR) leads to a good linearity of the VCO system. This sensor front end consumes 3.2 μW of power and achieves an SNDR of 89 dB and a DR of 94 dB in 500 Hz of bandwidth. Together with a 1.18 μVrms integrated input-referred noise, it achieves a noise efficiency factor (NEF) of 4 and a Schreier FoM of 171 dB. Despite the fact that other indicators are excellent, a nine-bit CDAC is needed to feedback prediction signal, leading to extra area; in addition, input impedance is limited by chopping frequency and input capacitance.

Corentin Pochet proposed a third-order VCO-based ΔΣADC [21] using a pseudo-virtual ground feedforward technique. As shown in Figure 12, each integrator is comprised of a Gm stage and VCO followed by PFD. The pseudo-virtual ground of the ADC feeds forward to the second and third integrators using Gm cells. The signal summation between the feedforward path and the integration path is performed in the current domain, and the resulting current drives the CCO of the next integrator. With third-order shaping, the system achieves a 1.8 V input range, a 92.1 dB SNDR over a 2.5 kHz bandwidth and consumes 4.4 μW with a 0.1 mm^2 area. However, the input impedance is still poor since a chopper is used.

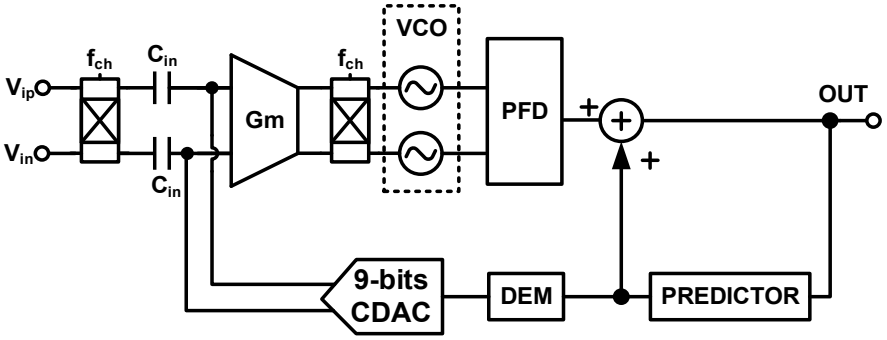


Figure 11. The diagram of the VCO-based system with DPCM.

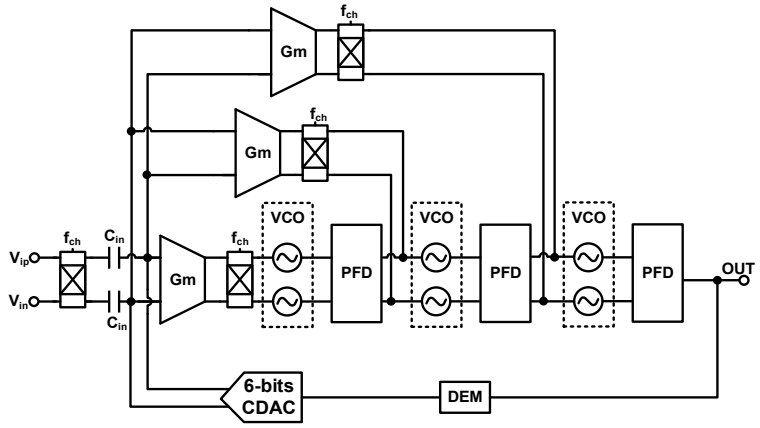


Figure 12. The diagram of the 3rd-order VCO-based system with pseudo-virtual ground.

To avoid impairing input impedance, work [22] presents a highly linear Gm-C-based CT-DSM (delta-sigma modulator) without chopping. As shown in Figure 13, a resistive feedback DAC (RDAC) is implemented in parallel with resistor R_S of first Gm-C integrator instead of CDAC. The signal current I_S through R_S and the feedback current I_{DAC} generated by RDAC are subtracted at the V_S. Due to the feedback-assisted Gm linearization, the magnitude of the I_{IN} maintains within the LSB of the feedback DAC current even with a large input voltage, which can significantly improve the linearity of the CTDSM system. This design achieves a high input impedance, a 300 mVpp linear input range, a 80.4 dB SNDR, a 81 dB DR and consumes only 6.5 µW with a signal bandwidth of 10 kHz. However, without chopping, this system has poor CMRR and the schematic of first Gm-C integrator is complex.

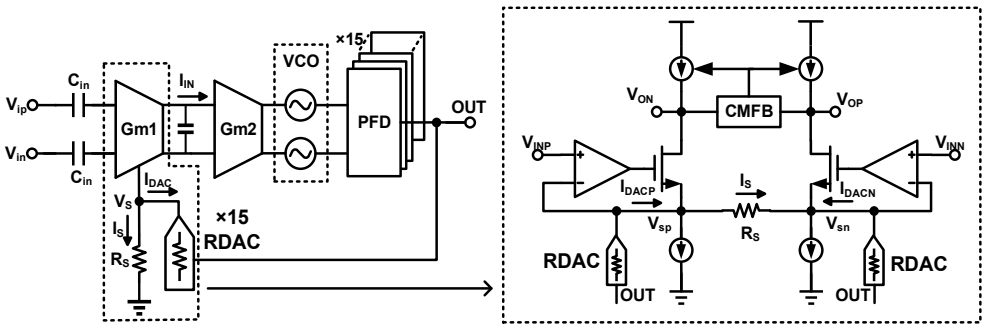


Figure 13. The diagram of Gm-C-based CTDSM.

In [23,24], several methods to save power and reduce noise for VCO-based modulators are provided. In [23], a modulation method is described for spread-spectrum clock generators (SSCGs) which reduce clock power. In [24], a noise reduction method for $\Delta\sum$

bang-bang PLL is presented. Table 2 summarizes the performance of state-of-the-art VCO-based DDC-structured biopotential readout circuits. In [18], a VCO-based neural recording system which works at 1.2 V supply is proposed. This work achieves good performance on SNDR (76 dB) compared with a conventional delta-sigma modulator. However, the linearity of the system depends on PVT variations of the calibration module. In [19], a closed-loop VCO-based system is presented using a PFD array as quantizer. With a PFD array, the system avoids high-speed VCO to save power (4.5 µW) and area (0.025 mm^2). Therefore, the FoM of the system is higher than that in [18]; however, the input impedance is not considered. In [22], a Gm-C-based CT-DSM is proposed without chopping. This work has good performance on SNDR (80.4), area (0.078 mm^2) and input impedance (13.3 MΩ@10 kHz). However, without chopping, the CMRR (76 dB) and noise (95 nV/$\sqrt{}$hz) are poor. In [20], a VCO-based quantizer is proposed using DPCM to avoid nonlinearity. With low OSR (OSR = 32), the system achieves an SNDR of 89 dB, consuming 3.2 µW. Although other performance values are excellent, the input impedance (4 MΩ) is limited by the chopper and input capacitor. In [21], a third-order VCO-based DSM was proposed using a pseudo-virtual ground to eliminate the large swing at the integrator output. This work also achieves good tradeoff between SNDR (92 dB) and power (4.4 µW), but input impedance is poor.

Table 2. Performance of state-of-the-art VCO-based DDC biopotential readout circuits.

	[18]	[19]	[22]	[20]	[21]
Technology (nm)	130	40	55	65	65
Supply (V)	1.2A/0.45D [1]	0.8A/0.6D [1]	1	1.2A/0.7D [1]	0.8
Fs (Hz)	5 K	2.5 M	1.28 M	32 K	400 K
Zin (MΩ)	∞ [2]	0.22	13.3 [3]	4	-
Input range (mVpp)	50	100	300	250	1800
Input noise (nV/$\sqrt{}$Hz)	95	36	95	53	
Bandwidth (kHz)	0.2	10	10	0.5	2.5
SNDR (dB)	76	78.5	80.4	89.2	92.1
CMRR (dB)	66	83	76	98	80–93
Power (µW)	7	4.5	6.5	3.2	4.4
Area (mm^2)	0.135	0.025	0.078	0.08	0.1
FOM [4] (dB)	150.5	172	172.3	171.2	179.6

[1] A represents analog-domain; D represents digital-domain. [2] Theoretical calculated value. [3] At 10 KHz. [4] FOM = $P/(2^{ENOB}*F_s)$.

Compared to the traditional DDC structure, the VCO-based DDC structure can achieve higher SNDR and FOM more easily because it has larger input range and displays lesser quantizer power consumption. The linearity of closed-loop structures is better [19–22] compared to the open-loop VCO-based structures in [18]. An obvious advantage of higher-order VCO-based DDC [21] is their ability to achieve large input range and high SNDR. When input impedance is the primary requirement, chopper-less designs [18,22] exhibit excellent performance at the cost of low-frequency noise. When considering the area of the acquisition chip, the hybrid PLL DSM structure proposed in [19] is suitable due to its low VCO center frequency.

4. Techniques for Bio-Optical Signal Recording

Photoplethysmogram (PPG) and near infrared spectroscopy (NIRS) are optical sensing modes that not only provide heart rate as conventional ECG, but also enable calculation of blood oxygen saturation (SpO_2). PPG obtains the pulsating changes in the volume of blood vessels along with the pulsation of the heart by recording the light absorption of the measured part in real time. Similar to biopotential signal recording systems, bio-optical recording systems should also feature low power, low noise and small chip area to reduce costs. What is more, the PPG signal consists of an AC component and a DC component, and the ratio of AC/DC can be as low as 0.1%; therefore, another challenge of

the PPG sensor readout system is to achieve a high DR [25,26]. A conventional PPG readout circuits includes a TIA, an anti-aliasing filter, a sample/hold circuit and an ADC. The ADC quantization noise and nonlinearity can limit the PPG sensor DR [27–30]. Therefore, DDC techniques play an important role in minimizing the power, noise and chip area while providing a high DR [31,32].

In terms of a low-power PPG system, reducing the power of LED drivers is significant. The system feedbacks the PPG output to the LED driver to control the driving current dynamically in [33]. As shown in Figure 14, a TIA followed with a nine-bit ADC is used to convert the PPG input current to a digital signal. Dynamic Range Enhancement (DRE) is implemented, which includes a digital filter to obtain the DC components of the PPG signal. This DC component is feedbacked to subtract the static photocurrents, so the accuracy requirement for Aa is relaxed. Moreover, the digital output value can dynamically adjust the LED driving current to ensure that the driving current is in a reasonable state. In this way, the system achieves a 87 dB time-varying interference attenuation with a 425 μW power consumption. However, the dynamic range is limited by DRE.

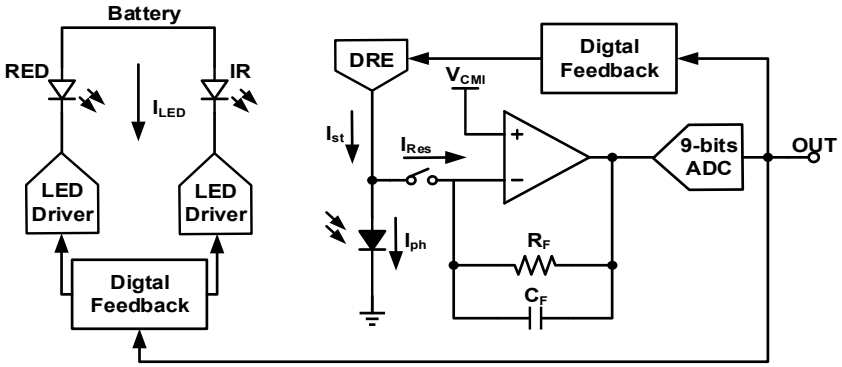


Figure 14. The static and time-varying interferer removal PPG system.

Compressive sampling is another technique to save LED driving currents [34]. As shown in Figure 15, the signal is sampled at a sub-Nyquist frequency and adjacent samples are uneven in time distribution. Hence, the LED driving current is proportionally reduced. The feature extraction units, which are included in the digital back end (DBE), analyze the digital signal and determine the systolic peaks of the PPG signals. Then, the system estimates when the next peak will arrive and enable the LED pulse at that time. The system uses a 30× compression ratio and finally reduces the whole power consumption to 172 μW. However, once the PPG signal changes, the system misses the peak information and needs time to recalibrate.

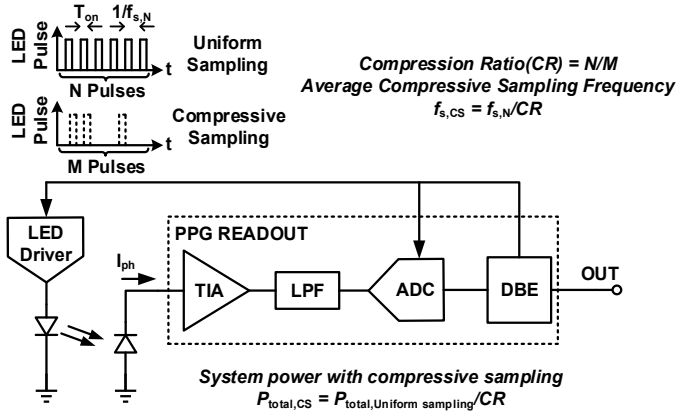


Figure 15. The diagram of compressive-sampling (CS)-based PPG system.

To obtain peak information more comprehensively and faster, a low-power PPG sensor with a heartbeat-locked loop (HBLL) is proposed in [35]. As shown in Figure 16, AFE consists of DC–current cancellation circuits, a transimpedance amplifier (TIA), switched capacitor low-pass filters (SC-LPF), two S/Hs and a comparator. The comparator compares two adjacent PPG samples and outputs PPGCLK signals according to the change in PPG signals. The HBLL receives the PPGCLK signals and estimates the heartbeat interval (HBI) by using a counter. Based on the HBI, the LED pulse and sampling are only enabled during the PPG peak windows precisely. Therefore, the power consumption of the LED driver is reduced from 105 μW to 16 μW with accurate HR monitoring. However, this work can only obtain PPG peak information. In SpO2 monitoring, the whole PPG signal should be recorded.

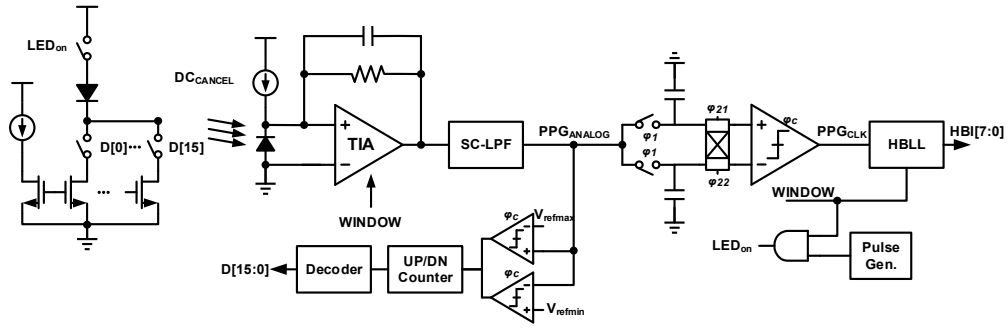


Figure 16. The AFE and LED driver schematic of HBLL.

Apart from reducing the power consumption of LED drivers, optimizing PD is another way to achieve low-power PPG sensors. Integrating the PD on the chip can save area and simplify the system architecture while offering good tradeoffs of power and noise. An integrated monolithic PPG sensor with on-chip pinned photodiodes (PPD) is proposed [36]. PPD is commonly used in CMOS image sensors (CIS) due to their high sensitivity. Therefore, this work achieves the same signal-to-noise (SNR) ratio compared to that of the conventional architecture at a significantly lower power. As shown in Figure 17, averaging is applied to reduce the read noise and relax DR requirements. Then, the PPG signal is adjusted to suitable voltage range by a programmable gain low-power SC amplifier. A 14-bit ADC is used for data conversion. Finally, with a low LED duty cycle, LED only consumes 1.97 μW and AFE consumes 2.63 μW.

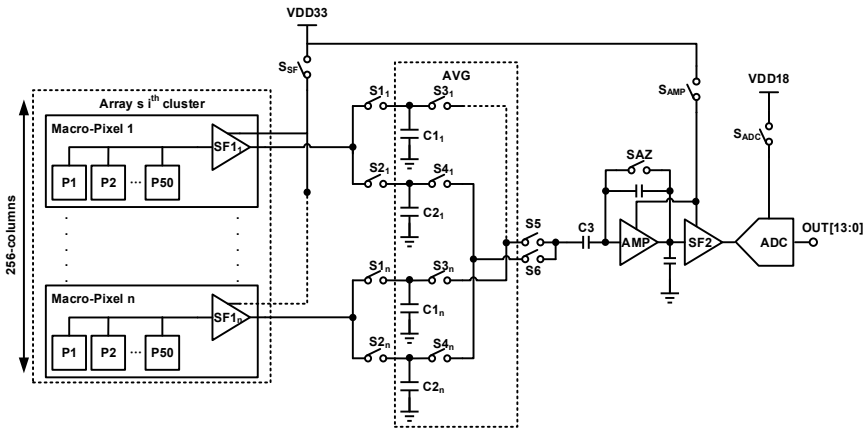


Figure 17. Architecture of the monolithic PPG sensor.

Table 3 summarizes the power consumption of state-of-the-art PPG readout circuits. It is worth noticing that various technologies have been implemented to rapidly reduce the LED power and AFE power of a PPG system, even at the cost of area.

Table 3. Performance of state-of-the-art PPG readout circuits.

	[33]	[34]	[35]	[36]
Technology (nm)	180	180	180	180
Supply (V)	1.8	1.2	3.3	1.8A/3.3D [1]
Pulse Frequency (Hz)	165	4–128	40–100	40
LED Duty cycle	0.7%	-	0.0175–1.75%	0.07%
LED Power (μW)	120–1125	43–1200	16–520	1.97 [2]
AFE Power (μW)	216	172	27.4	2.63
Area (mm^2)	1.84	10	1.51	20

[1] A represents analog domain; D represents digital domain. [2] Green LED = 12.04 μW; red LED = 1.97 μW.

As illustrated before, accurate recording of PPG signals requires high DR of the readout system. The majority of the PPG signal is the DC component; therefore, the main ADC power is used to quantify DC currents. A workable solution is the use of a DC servo loop to subtract the DC components before the input signals enter TIA. F. Marefat proposed a new light-to-digital convertor (LDC) which allows the measurements of DC and ambient components of the PD current for signal cancellation [31]. As shown in Figure 18a, two eight-bit IDACs are implemented to compensate the ambient light, as well as DC components, which are recorded for further processing as well. PDACs serve as main-feedback DAC of LDC, and nDACs replicating pDACs relax the current-drive requirements of the amplifier. This topology can achieve a 92.7 dB DR while consuming 8.1 μW power. Based on this concept, a second-order ΔΣ LDC is applied for benefiting from two-stage noise shaping [37]. As shown in Figure 18b, two 10-bit DACs instead of 8-bit DACs are employed to cancellate the ambient light and DC components. Multiple DACs are implemented to complete the closed loop while ensuring linearity. However, the second-order architecture benefits from lower noise, but also consumes higher amounts of power. In this work, a 108.2 dB DR is achieved while using a 15.7 μW AFE power. Since oversampling is necessary for noise shaping, a higher pulse frequency is required with higher LED power.

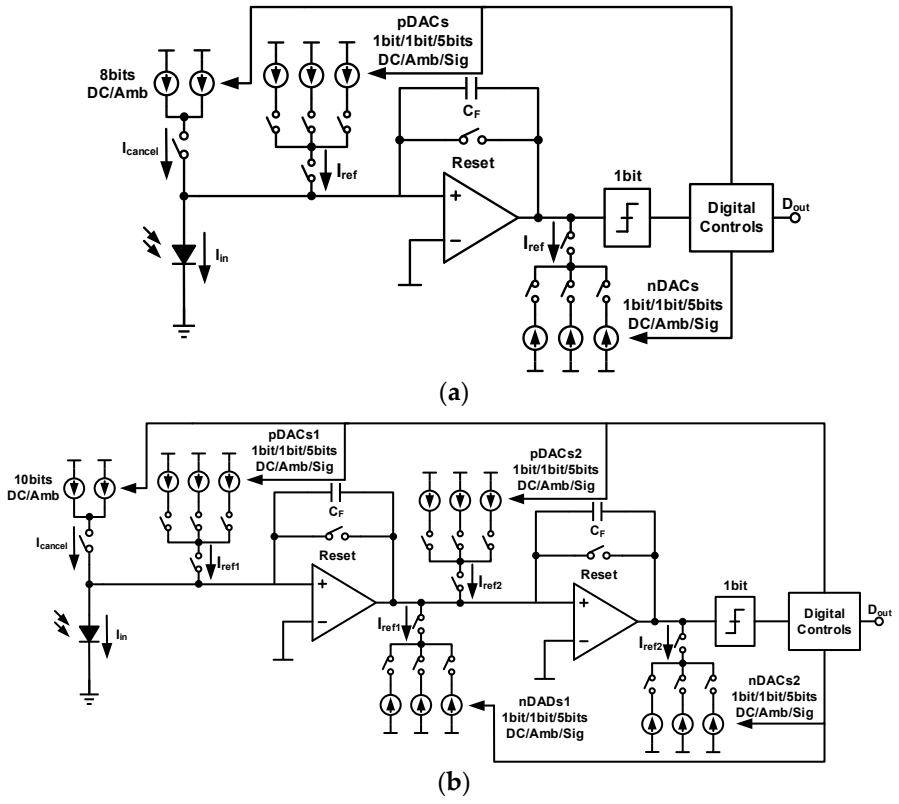


Figure 18. (**a**) Block diagram of I-ΔΣ LDC; (**b**) second-order I-ΔΣ LDC.

Q. Lin proposed a reconfigurable LDC for PPG sensor readout in [38] which utilizes a current integration and a charge counting to reduce noise contribution. As shown in Figure 19, this LDC consists of a latched comparator, a current reference, a counter and an integrator. A current DAC is implemented to cancel ambient current to increase DR. Finally, this work achieves a 119 dB DR with a 196 µW power consumption.

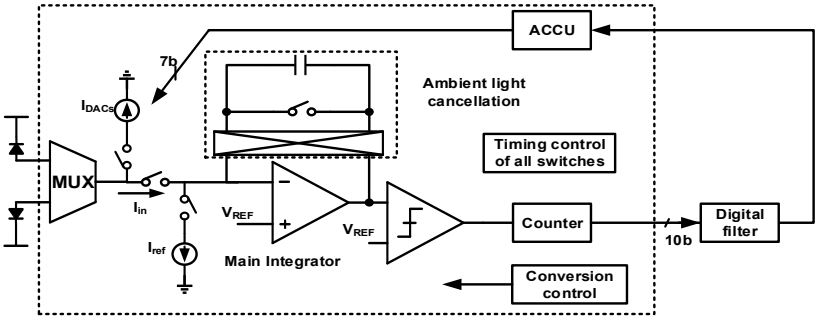


Figure 19. Block diagram of the LDC.

Dual-slope ADC is an excellent solution for the required high DR of PPG monitoring. Further, this architecture is also suitable for low-bandwidth and linearity requirements. To reduce AFE power consumption caused by dual-slope ADC long-time conversion, a hybrid-architecture-slope LDC is proposed [39]. With noise shaping, the hybrid architecture quantizer can be lower to achieve the same resolution as that of the pure dual-slope quantizer. As shown in Figure 20, a 10-bit quantizer is used to convert the integrator output to a digital code. An on-chip digital threshold filter controls a seven-bit IDAC to compensate the DC components of PPG signals. This work achieves a 134 dB DR while consuming 28 µW of power.

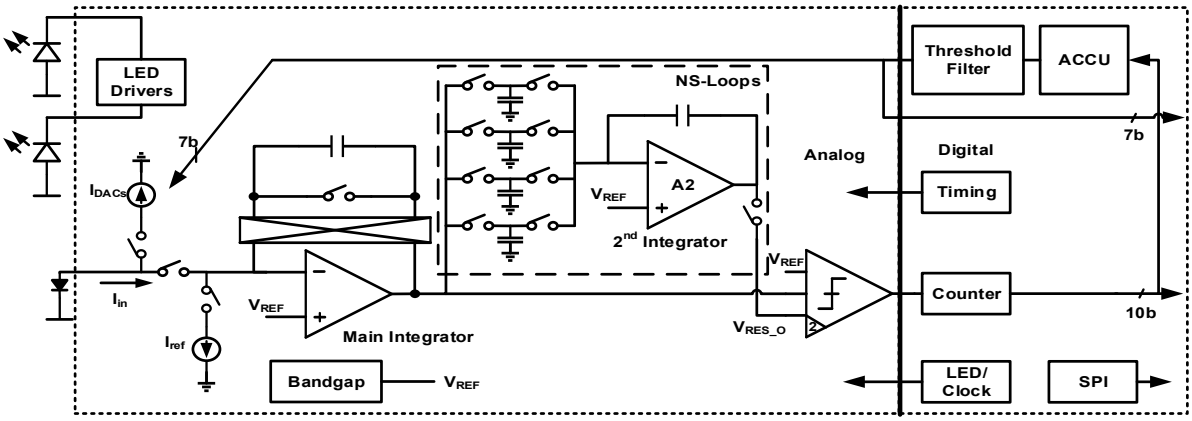


Figure 20. Architecture of NS LDC.

Table 4 summarizes the comparison of state-of-the-art high-DR PPG readout circuits. In [31], an LDC with an eight-bit IDAC was proposed consisting of pDACs and nDACs. With a 10.24% LED duty cycle, the system achieves 92.7 dB consuming 8.1 uW. Based on [31], in [37], a second-order LDC was proposed. In this work, the circuit benefits from lower noise (DR = 108.2 dB), but consumes a higher amount of power (15.1 µW). However, the systems in both [31] and [37] consume a large amount of LED power (1950 µW and 264 µW). In [38], reconfigurable LDC was proposed which uses a current integrator and a DAC. The model in this work achieves a 119 dB DR with a 196 µW power consumption. Although the power of AFE is high, with lower LED duty cycle (1%), LED power is lower than that of [31,37]. In [39], a hybrid-architecture slope LDC was proposed to reduce AFE power. The system in work achieves a 134 dB DR with only 28 µW of AFE power.

Table 4. Comparison of state-of-the-art high DR bio-optical readout circuits.

	[31]	[37]	[38]	[39]
Technology (nm)	180	180	180	180
Supply (V)	1A/2.5D [1]	1.5A/2.5D [1]	1.2/3.3 [1]	1.2A/3.3D [1]
Amb. Remove (μA)	28.2	25.6 [2]	50	50
Architecture	LDC (ISDM)	LDC (ISDM)	LDC (Slope)	LDC (NS-Slope)
Input range (μA)	51.2	51.2	200	200
Pulse Frequency (Hz)	100	250	512	2048
Noise BW	0.5–10	0.5–10	-	0.5–20
DR (dB)	92.7	108.2	119	134
LED Duty cycle	10.24% [3]	3.2%	1%	1%
LED Power (μW)	1950	264	107	305
AFE Power (μW)	8.1	15.7	89	28
Area (mm^2)	4.8	-	7 [4]	8.4

[1] A represents analog domain; D represents digital domain. [2] 10-bit ambient light removal. [3] Needs two LEDs. [4] External cap for filtering reference current.

In a bio-optical signal recording system, the LED power consumption is the main contributor to the system power consumption compared to AFE. Compared to using a one-bit quantizer LDC [31,37] structure, using slope-based LDC [38] and dual-slope-based LDC [39] can greatly reduce LED power consumption by low LED pulse frequency. Furthermore, compared to [38], although the dual-slope-based LDC has a higher rate of AFE power consumption, it has higher DR while consuming less LED power.

5. Conclusions

This paper describes an overview of biomedical signal readout circuits. In the ECG monitoring domain, a direct digital conversion technique has been proposed in recent years, which employs preamplifier and data converters, reducing the complexity of the readout chain and thus its power consumption. To be suitable for low power supply and process node, VCO-based architecture is proposed. However, all methods have poor performance in input impedance. Boosting input impedance is still a significant highlight of the biomedical sensor. For bio-optical monitoring, low power consumption and high DR are the main challenges. Determining a way to provide a good tradeoff between DR, AFE power and LED power is the focus of PPG design in the future.

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