Delta Configured Multi Busbar Sub-Module Modular Multilevel STATCOM with Partially Rated Energy Storage for Frequency Support

Delta Configured Multi Busbar Sub-Module Modular Multilevel STATCOM with Partially Rated Energy Storage for Frequency Support

Chuantong Hao, Paul Judge, Wenhao Ma, Stephen Finney, Michael Merlin

***Abstract*—This paper presents a delta-configured, modular multilevel, STATCOM with integrated partially-rated energy storage (ES) and submodules (SM) based on the Multi-Busbar Sub-module (MBSM) topology. The soft-paralleling of SM capacitors using the nature of diodes leads to lower SM voltage deviation and lower circulating current to be used for SM balancing and improves the overall operation of the converter. Partially rated ES are distributedly integrated in SMs to provide ancillary service, e.g. frequency support, in addition to the classic reactive power provision. The study uses the analytical formulation of the MBSM to derive the control system and the optimal phase angle of the circulating current required for SM balancing. A comparison of different operating modes (MBSM vs emulated full-bridge SM) is presented and confirmed by simulation results. Analysis indicates that the MBSM improves the power efficiency (30.5% total losses reduction at the 1 pu reactive power set-point and 3.56% reduction at 1 pu active power set-point) compared with the conventional full-bridge SM, at the cost of doubling the number of semiconductor devices; but not the number of sub-modules.**

***Index Terms*—Multi Busbar Sub-module, Modular Multilevel STATCOM, Energy Storage, Power Efficiency, Power Capability**

I. Introduction

THE continuously increasing proportion of distributed renewable energy has been giving rise to more challenges for reliability and robustness of the power grid. An effective solution to increase the stability of AC grid is Flexible AC Transmission Systems [1], among which Static compensator (STATCOM) is widely accepted to provide power quality management and voltage support by releasing and absorbing reactive power. Enhanced frequency stabilization against disturbance or unbalance is also offered with partially rated energy storage (ES) system integrated as active power can be exchanged between STATCOM and the AC grid [2], [3].

For medium and high voltage applications, e.g. large scale wind farms [4], modular multilevel converter (MMC) style topologies [5] is usually integrated into STATCOM to increase its voltage level and meanwhile reduce harmonic distortion and switching frequency [6]. In each converter arm, several submodules (SMs) are connected in series to generate staircase AC voltage waveform with capacitor voltages. Efforts and costs of periodical preventive maintenance are also reduced thanks to the modular design of SMs, especially in offshore converter stations [7]. Generally, full-bridge (FB) is the first choice for SMs in MMC-STATCOM as half-bridge (HB) is not able to output negative SM voltages, even though HBSMs are popular in classic MMC, in which only positive stack voltages are constructed during normal operation [8]. Fig. 1 illustrates a typical MMC-STATCOM (also commonly referred to as a Cascaded H-Bridge) with delta configured arms so that additional circulating current can be applied to promote the SM voltage balancing [9]. The connection manner of FBSMs within an arm is presented in Fig. 1(a).

Instead of implementing the ES elements into a large scale and concentrated pack, as has been introduced in [10], the characteristics of MMC-STATCOM allow ES to be distributed into the SMs themselves. The management of ES conditions, e.g. state of charge and state of health, are additionally integrated into converter control algorithm. Many excellent works have been done on the joint regulation of converter control and ES management. Ref. [11] analyses different operating modes in an ES-MMC and develop control algorithms that offer the flexibility to directly manipulate the active power components for state of charge balancing of the batteries. The MMC with partially rated integrated ES and its control system proposed in [12] is suitable for frequency support and ancillary service provision such as decoupled power oscillation damping. In [13], the partially rated energy storage (PRES)-STATCOM capable of providing both reactive and active power support and voltage balancing algorithm are introduced together. Fig. 1(c) depicts how ES interface is connected to SM capacitor. The interface could be through a passive filtering network, or through an actively controlled DC/DC converter, such as buck-boost converter or dual active bridge for isolated applications. When the interface is disabled, the ES-SM becomes a normal SM. The ES interface will be modelled as a controlled current source in simulation and analysis of its specific structure is not the focus of this paper.

The standard single-bus SMs, especially in partial rated ES topology, typically requires additional circulating current to maintain SM voltage balancing as well as suppress ripple current [14]. Additional circulating current, on the other hand, causes higher power losses and higher temperature rises in semiconductor junctions. Consequently, more challenges are faced in the cooling system design to ensure that the junction remains within its safe range. The parallel connection of devices [15], [16] provides ideas to solve the above problems by distributing the stack current to doubled conduction paths, as is shown in Fig. 1(b). In modular multilevel series parallel converter (MMSPC), SMs capacitors are parallelized instead of being bypassed to reduce the total parasitic inductance and resistance [16]. The MMSPC are verified by simulation and

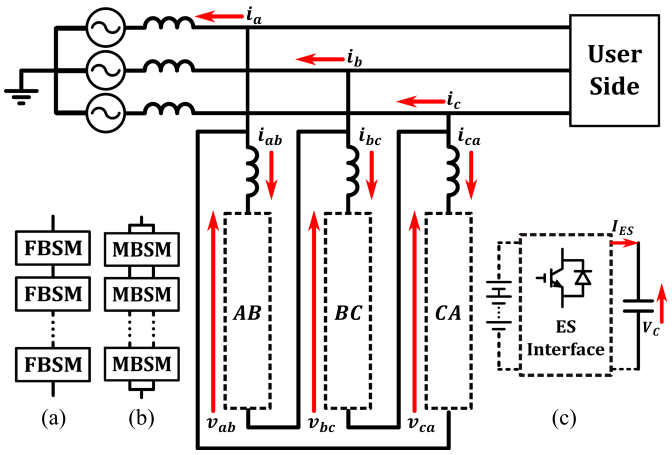

Fig. 1: A delta configured modular multilevel STATCOM and (a) a stack of FBSMs, (b) a stack of MBSMs, (c) the ES interface in a ES-SM

down-scaled experimental results in allowing wide frequency range operation [17]. Besides, SM voltage balancing is maintained by periodically paralleling SM capacitors, achieving the so-called sensorless balancing [18].

Despite the above-mentioned benefit of parallel SM design, additional inductors should be connected between two SMs to suppress the inrush current caused by capacitor paralleling [19], [20], [21]. The number of these additional inductors required is twice the number of SMs, resulting in extra converter costs and power losses. This paper presents a delta configured PRES-MBSM-STATCOM for frequency support. The characteristics of diodes are applied to suppress the inrush current, so no additional inductors are required while the benefit of parallel SMs can still be taken advantage of. The contribution of this paper can be summarized as follows:

(1) The structure, states and operation principles of the MBSM STATCOM with partially rated ES are examined in Section II. The soft parallel mechanism proposed can effectively suppress the inrush current between SMs without the requirement of implementing additional inductors.

(2) The low level controller presented in Section III dynamically selects the preferred mode to maintain the active power output capability and at the same time lower the power loss. In the soft-parallel based mode, a threshold of stack current is set below which the soft-parallel states are replaced with bypass states in order to compensate for current measurement errors and delays.

(3) The analytical solution of the optimal phase angle of the additional $3rd$ harmonic circulating current required for SM voltage balancing is presented in Section IV.

(4) Simulation results in Section V have confirmed that the proposed MBSM STATCOM has not only the capability of generating active and reactive power, but also excellent performances in power efficiency and active power capability.

II. Operation Principle of the MBSM STATCOM

A. Structure and Basic States

The MBSM is constructed by four half bridges and a capacitor. Twice the number of semiconductors, interfaces and busbars are utilized in a MBSM compared with a conventional FBSM. In the stack composed of two MBSMs shown in Fig. 2 (a), the adjacent MBSMs are connected together through two buses. The terminals and interconnections are also marked in the figure. ES interface is connected to the capacitor in a MBSM to form an ES-MBSM. Stack current is divided into two parts when passing a stack so that current load on certain semiconductor is mitigated.

When a MBSM is regarded as a controlled object of the low level controller, it can operate as a conventional FBSM with positive voltage state, negative voltage state and zero voltage state [22], as are presented in Fig. 2 (b). All FBSM oriented control methods can thus be applied to MBSMs.

Apart from being inserted (positively or negatively) or bypassed as similar to FBSMs, two adjacent MBSMs can be parallelized through proper actions of the semiconductors between them. The control targets become interconnections of two adjacent MBSMs and terminals of the stack as paralleling requires joint actions of two adjacent MBSMs. States of MBSMs are consequently defined in two categories: (1) The interconnections states include series positive, parallel and series negative; (2) the terminals states include series positive, bypass and series negative. Fig. 2 (c) and Fig. 2 (d) list typical interconnection states and terminal states proposed in previous publications [20], [21]. When the interconnection of two MBSMs is in parallel mode, the capacitors voltage will be equal thanks to the paralleling of capacitors. Voltage balancing can thus be achieved. Notice that additional inductors should be connected in the conduction paths to avoid the inrush current and extra capacitor paralleling loss resulting from the paralleling of two capacitors with a voltage difference, as is presented in Fig. 2 (c)(3) and Fig. 2 (c)(4). The soft-parallel states proposed in this paper (Fig. 3) don't need additional inductors, and can be seen as an upgrade of the interconnection states shown in Fig. 2(c).

B. Operation Modes

Two operation modes are defined here for the proposed MBSM STATCOM. The first mode is named as the FBSM based mode in which the MBSM can be regulated by any FBSM oriented control method with slight adjustment on the transition from state to gate signals. The other mode, named as the soft-parallel based mode, is based on the soft-parallel mechanism, which makes full use of the directional conduction characteristics of IGBT anti-parallel diodes. Inrush current and capacitor paralleling loss are both avoided without any change on the stack structure. Moreover, the average switching frequency of semiconductors can be further reduced.

Fig. 3 presents the interconnection and semiconductor states when the interconnection is desired to output zero voltage. While in the soft parallel states, as are shown in (a1), (a2), (b1), and (b2), two current paths are constructed respectively to connect the positive polar and negative polar of capacitors C_1 and C_2 in two adjacent MBSMs. Stack current will dynamically select one path to charge the capacitor with lower voltage, or discharge the capacitor with higher voltage, until achieving voltage balance. Hence not only is inrush current

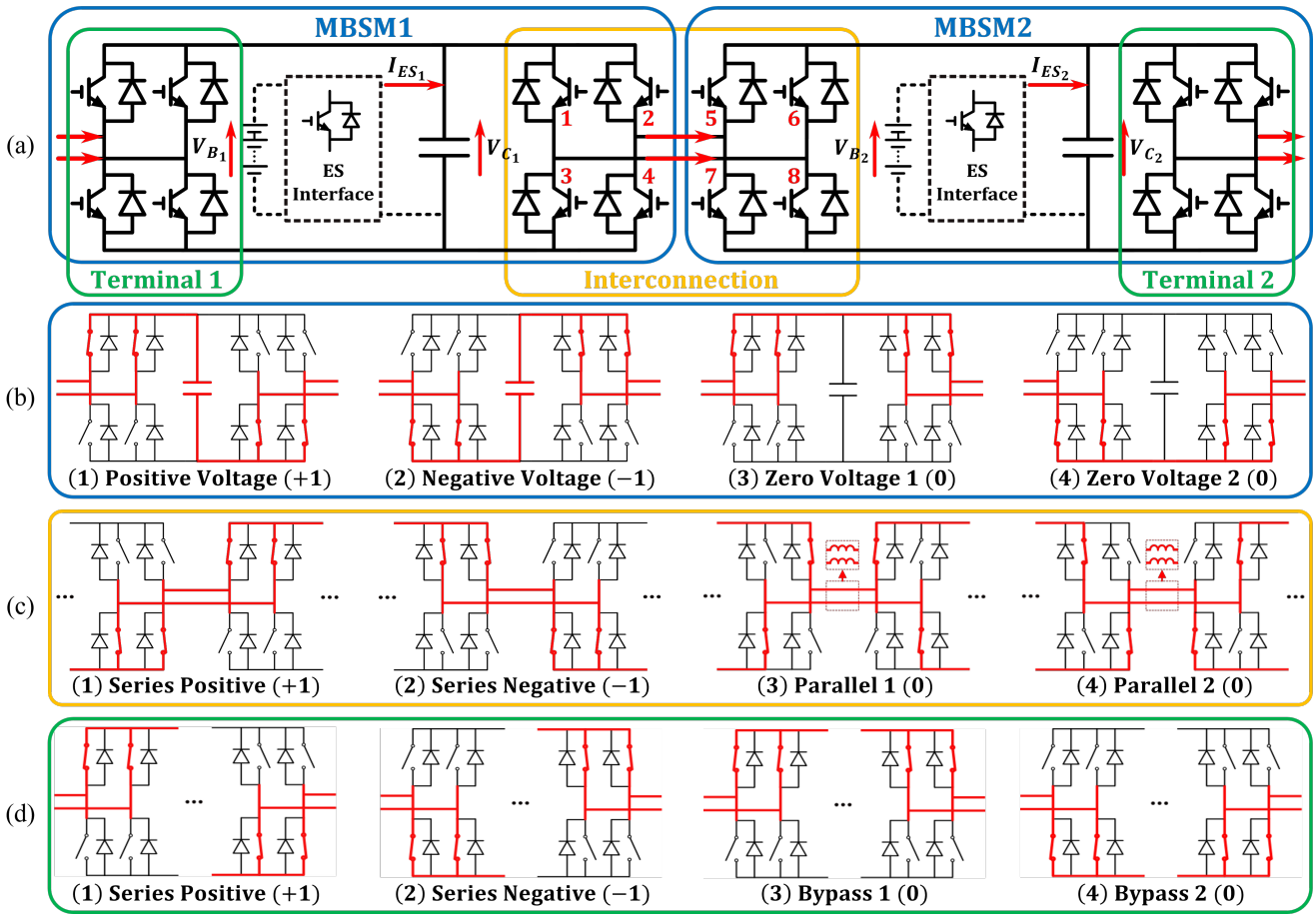

Fig. 2: Structure and states of MBSMs (a) A stack consisting of two MBSMs, (b) MBSM states in the conventional FBSM based mode, (c) Interconnection states in the soft-parallel based mode (showing where inductors were previously inserted in [16], [17], [18], (d) Terminal states in the soft-parallel based mode.

limited in the envelope formed by the stack current I_S, but also the direct parallel connection of capacitors is avoided. The activation of specific soft-parallel states is determined by the instantaneous stack current. In order to compensate the current measurement error and potential delay resulted by communications, a positive value I_{Thr} is set as the current threshold to provide the margin for states transition. Bypass states, as are shown in Fig. 3 (c1) and (c2), will replace soft-parallel states if $|I_S| \leq I_{Thr}$.

In Fig. 3 (a1)-(b2), $I_S > I_{Thr}$ and $I_S < -I_{Thr}$ represent stack current flows from left to right and the opposite direction, respectively. Capacitor voltages of C_1 and C_2 are denoted as V_{C_1} and V_{C_2}. Take the soft-paralleling state 1 when $I_S > I_{Thr}$, as is shown in Fig. 3 (a1), as an example, semiconductors S_2 and S_8 are switched on. If $V_{C_1} > V_{C_2}$, stack current will flow via S_2, D_5 and charge into C_2 as the anode of D_5 is positive relative to its cathode. While $V_{C_1} < V_{C_2}$, D_3 will be activated and the actual current path becomes $C_1 \rightarrow D_3 \rightarrow S_8$. C_1 are charged to reduce the voltage difference. Notice that semiconductor states in Fig. 3 (a1) and in Fig. 3 (a2) are different yet the same effect can be achieved. Similar performance can be found in Fig. 3 (b1) and in Fig. 3 (b2). By alternating between the equivalent states, average current, losses, and junction temperature rise are distributed to different semiconductors within a MBSM evenly.

All semiconductor states and the conditions to determine them in the soft parallel based mode are listed in Table I. In all soft-parallel states, characters with $*$ represent current flowing through the corresponding semiconductor, either diode or IGBT; characters without $*$ represent the semiconductor is activated to form parallel path but no current is passing through. Take the states in Fig. 3 (a1) and Fig. 3 (b1) as examples, the equivalent simplified circuit when $V_{C_1} > V_{C_2}$ are shown in Fig. 4 (a) and Fig. 4 (b), respectively. In Fig. 4 (a), stack current flows through D_5 while D_3 is reverse blocked so no current is passing. The reverse voltage of D_3 can be described by: $V_{Blk} = V_{C_1} - V_{C_2} - V_F$, in which V_F is the diode forward voltage. The capacitor charging current is equal to the stack current and no inrush current or capacitor parallel loss is generated as the capacitor voltage difference is clamped by D_3. Similar analysis can be conducted to the circuit shown in Fig. 4 (b), where D_2 is reverse blocked and stack current flows through D_8 to the cathode of C_1, reducing the voltage difference by discharging the capacitor with higher voltage.

The direction of the stack current changes in a whole cycle of STATCOM operation. Whenever the current direction or the relative magnitude of capacitor voltages is changed, the

TABLE I: Semiconductor states in the soft-parallel based mode

Desired States	Measured Conditions	Interconnection States	Naturally Conditions	Semiconductor state							
				1	2	3	4	5	6	7	8
Soft-parallel (0)	$I_S > I_{Thr}$	Fig. 3(a1)	$V_{C1} > V_{C2}$	0	S_2*	D_3	0	D_5*	0	0	S_8
			$V_{C1} < V_{C2}$	0	S_2	D_3*	0	D_5	0	0	S_8*
		Fig. 3(a2)	$V_{C1} > V_{C2}$	S_1*	0	0	D_4	0	D_6*	S_7	0
			$V_{C1} < V_{C2}$	S_1	0	0	D_4*	0	D_6	S_7*	0
	$I_S < -I_{Thr}$	Fig. 3(b1)	$V_{C1} > V_{C2}$	0	D_2	S_3*	0	S_5	0	0	D_8*
			$V_{C1} < V_{C2}$	0	D_2*	S_3	0	S_5*	0	0	D_8
		Fig. 3(b2)	$V_{C1} > V_{C2}$	D_1	0	0	S_4*	0	S_6	D_7*	0
			$V_{C1} < V_{C2}$	D_1*	0	0	S_4	0	S_6*	D_7	0
Bypass (0)	$\|I_S\| \le I_{Thr}$	Fig. 3(c1)	$I_S > 0$	S_1	S_2	0	0	D_5	D_6	0	0
			$I_S < 0$	D_1	D_2	0	0	S_5	S_6	0	0
		Fig. 3(c2)	$I_S > 0$	0	0	D_3	D_4	0	0	S_7	S_8
			$I_S < 0$	0	0	S_3	S_4	0	0	D_7	D_8
Series Positive (+1)		Fig. 2(c)(1)	$I_S > 0$	0	0	D_3	D_4	D_5	D_6	0	0
			$I_S < 0$	0	0	S_3	S_4	S_5	S_6	0	0
Series Negative (-1)		Fig. 2(c)(2)	$I_S > 0$	S_1	S_2	0	0	0	0	S_7	S_8
			$I_S < 0$	D_1	D_2	0	0	0	0	D_7	D_8

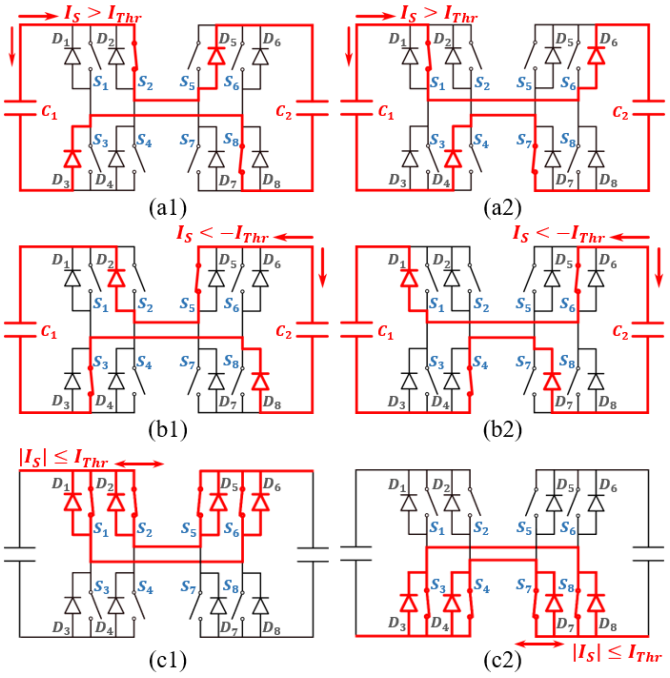

Fig. 3: States of the interconnection, semiconductors, and corresponding current paths in: (a1) soft-parallel state 1 when $I_S > I_{Thr}$, (a2) soft-parallel state 2 when $I_S > I_{Thr}$, (b1) soft-parallel state 1 when $I_S < -I_{Thr}$, (b2) soft-parallel state 2 when $I_S < -I_{Thr}$, (c1) bypass state 1 when $|I_S| \le I_{Thr}$, (c2) bypass state 2 when $|I_S| \le I_{Thr}$.

conducting semiconductor device changes, as indicated by Table I. As a result, semiconductors in different busbars take turns conducting current whether the relative magnitude of V_{C_1} and V_{C_2} changes or not in a cycle. So, the RMS current passing through a semiconductor is half of that in a single busbar SM when observing a whole cycle though the semiconductor should tolerate the whole instantaneous current. The reduction of RMS current leads to a reduction in power losses and temperature rises.

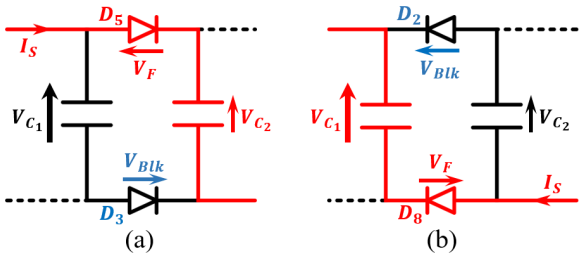

Fig. 4: Equivalent circuit when $V_{C1} > V_{C2}$ of: (a) soft-parallel state in Fig. 3 (a1), (b) soft-parallel state in Fig. 3 (b1).

III. Control Framework

A. Hierarchical Control System

The overall control system of the MBSM STATCOM can be divided into three layers, as is presented in Fig. 5. In Layer 1, energy management takes SM voltages as inputs and calculate the power correction command to ensure the total energy stored in three stacks is balanced through zero sequence circulating current I_0. The inputs of the power controller also include AC voltages, stack currents, and the operation point command: the expected active power output (P_{ref}) and reactive power output (Q_{ref}), based on which the current reference $I_{ES_{ref}}$ for all ES interfaces are calculated. As P_{ref}

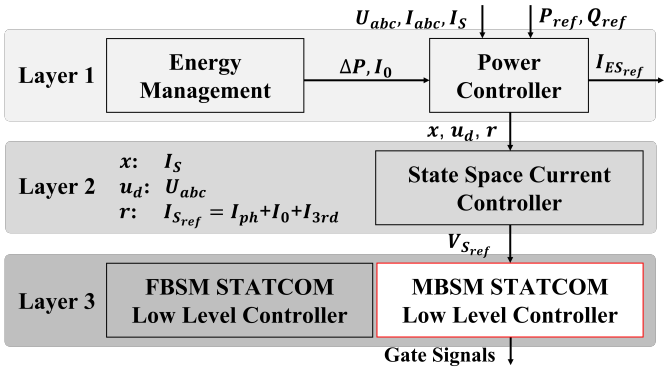

Fig. 5: Overall control system of the MBSM STATCOM.

increases, so will $I_{ES_{ref}}$, implying that more current will be injected into the capacitors in ES-MBSMs. The capacitor voltage deviation will also be increased accordingly since capacitors in normal MBSMs are not affected by the ES current raise. A normally used solution for reducing the voltage deviation is injecting additional third harmonic circulating current I_{3rd} [13], [14]. The total stack current reference $I_{S_{ref}}$ is calculated by the sum of phase current that contribute to AC output I_{ph}, I_0, and I_{3rd}. In Layer 2, the dynamics of the STATCOM are described by a set of loop voltage and node current differential equations, which can be rearranged and reduced to a base state space model with independent states [23] and regulated by Linear quadratic regulator (LQR) [24]. Then stack voltages references $V_{S_{ref}}$ are processed to Layer 3 to manage the switching states of all MBSMs, and finally the gate signals of semiconductors are generated. Compared with conventional FBSM STATCOM, MBSM STATCOM is only different inside the stack. Therefore, only the low level controller is different in their hierarchical control systems.

B. Low Level Controller

The flowchart in Fig.6 summarizes the proposed low level control system. The initialization involves importing the stack voltage reference $V_{S_{ref}}$, capacitor voltages V_C, stack current I_S and the counter value t. The first step is dynamically selecting the operation mode of the MBSM STATCOM to maintain voltage balancing and meanwhile lower down the power losses to the greatest extent. The mode selection follows a hysteresis manner: The conventional FBSM based mode is selected if $\overline{V_{ES}} - \overline{V_{cap}} > V_{Thr}$ until the difference decreases to zero, where $\overline{V_{ES}}$ represents the average voltage of ES-MBSMs, $\overline{V_{cap}}$ is the average voltage of normal MBSMs, and V_{Thr} is the voltage threshold, to bring MBSMs back to balance as soon as possible. Or, the STATCOM will stay in the soft-parallel based mode. For a stack consisting of N_{SM} MBSMs in soft-parallel based mode, N_{SM} triangular Phase Shift Carrier (PSC) [25] waves, in which the phase shift value is $2\pi/N_{SM}$, are assigned to a pair of stack terminals and $N_{SM}-1$ interconnections. The expected states are determined by the size of N_{ref} $(= V_{S_{ref}}/\sum V_C)$ and the carriers $C(i)$:

$$State(i) = \begin{cases} +1, & if \quad N_{ref} > C(i) \\ 0, & if \quad C(i) \geq N_{ref} > -C(i) \\ -1, & if \quad N_{ref} \leq -C(i) \end{cases} \tag{1}$$

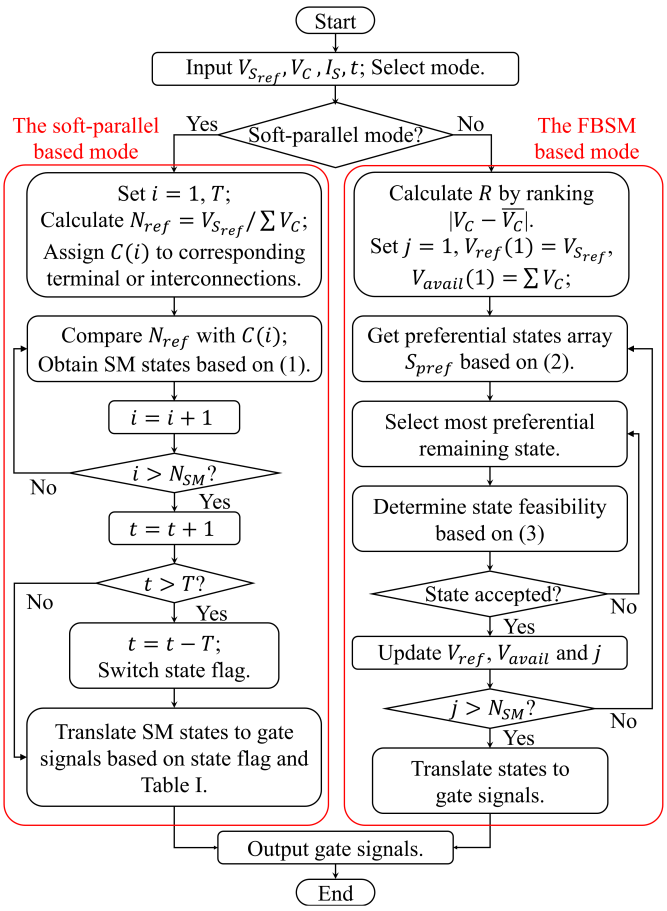

Fig. 6: The proposed low level control system.

For interconnections, state = +1, 0, -1 represent Series Positive, Zero Voltage Output (soft parallel state or bypass state as illustrated in Fig. 3) and Series Negative, respectively. The specific states is determined by the stack current based on Table I. The counter t is used to switch states between Fig. 3(a,b,c)(1) and Fig. 3(a,b,c)(2) after a fixed number of controller steps (T). t keeps track of how long either of these two group of soft-parallel states are used and swap them over several cycles to spread the load between all the semiconductor devices. Such arrangement can avoid excessive switching of semiconductors at specific positions, helping on reducing the risk of wear out failure.

In conventional FBSM based mode, the MBSM is regarded as a whole to define states positive inserted (1), bypassed (0) and negative inserted (-1). At first the sorted index R is obtained by ranking all MBSMs by their absolute deviation from the average capacitor voltage $\overline{V_C}$. The initial value of iterations are set as $V_{ref}(1) = V_{S_{ref}}$ and $V_{avail}(1) = \sum V_C$. Eq. (2) summarizes the criteria of preferential states, where the MBSM whose voltage $> \overline{V_C}$ is discharged and those whose voltage$\leq \overline{V_C}$ is charged with I_S.

$$S_{pref}(j) = \begin{cases} [1, 0, -1], \ if \ (V_C(R(j)) - \overline{V_C}) \cdot I_S \leq 0 \\ [-1, 0, 1], \ if \ (V_C(R(j)) - \overline{V_C}) \cdot I_S > 0 \end{cases} \tag{2}$$

The feasibility of the most preferential state, determined by Eq. (3), will be certificated if no potential voltage limit

violation is found. Or the state will be discarded and the subsequent remaining state in the array is tested. The parameters V_{ref}, V_{avail} and j are then updated and processed to the next iteration until states of all MBSMs are assigned. The semiconductor states are consequently obtained based on the MBSM state and state shown in Fig. 2(b).

$$\begin{cases} 1, & if \ \ |V_{ref} - V_C(R(j))| \leq V_{avail} - V_C(R(j))/2 \\ 0, & if \ \ |V_{ref}| \leq V_{avail} - V_C(R(j))/2 \\ -1, & if \ \ |V_{ref} + V_C(R(j))| \leq V_{avail} - V_C(R(j))/2 \end{cases} \tag{3}$$

IV. Analytical Analysis

A. Optimal Phase Angle of the Additional Circulating Current

Generally, MBSMs can operate in either soft-parallel based mode or conventional FBSM based mode. When injecting active power from the ES-STATCOM to the external grid, the ES interfaces always charge the capacitor in ES-MBSMs. It should be ensured that the ES-SM outputs the same amount of active power as it received from the ES interface at the end of each cycle to maintain voltage balancing. Additional third harmonic circulating current (I_{3rd}) is injected in the delta-configured loop to improve the capability of MBSMs for active power exchanging. I_{3rd} will not change the AC current or cause any interference to the overall energy balance of the converter as it does not contain any fundamental component. Fig. 7 illustrates the equivalent circuit for current analysis. The overall stack current reference involves: (1) Phase current I_{ph} (i_{ab}, i_{bc}, i_{ca}) that contribute to the AC output, (2) Zero sequence circulating current I_0 for energy balancing between different stacks, and (3) Additional third harmonic circulating current I_{3rd} for maintaining voltage balancing between ES-MBSMs and normal MBSMs in one stack. The stack current reference is:

$$I_{S_{ref}} = I_{ph} + I_0 + I_{3rd} \tag{4}$$

I_0 is only used during transients, and disappears during steady state operation where energy is distributed evenly among three stacks. As a result, when analysing the optimal phase angle of I_{3rd}, I_0 becomes negligible. Define the phase of I_{ph} and the phase of I_{3rd} as $\phi_{I_{ph}}$ and $\phi_{I_{3rd}}$, respectively. The overall stack current reference becomes:

$$I_{S_{ref}} = \hat{I_{ph}} \cdot sin\,(wt + \phi_{I_{ph}}) + \hat{I_{3rd}} \cdot sin\,(3wt + \phi_{I_{3rd}}) \tag{5}$$

Apply $\theta = wt + \phi_{I_{ph}}$, and $\Delta\varphi = \dfrac{\phi_{I_{3rd}}}{3} - \phi_{I_{ph}}$, Eq. (5) becomes:

$$I_{S_{ref}} = \hat{I_{ph}} \cdot sin\,\theta + \hat{I_{3rd}} \cdot sin\,3(\theta + \Delta\varphi) \tag{6}$$

In a whole cycle, the SM capacitor voltage variation should be zero. SM capacitor voltage variation is resultant of both energy storage current I_{ES} and overall stack current $I_{S_{ref}}$. Applying superposition theorem here, I_{ES} and $I_{S_{ref}}$ are seen as two independent current source. Their influence on SM capacitor voltage variation are analysed separately. Denote the capacitor voltage variation resulted by I_{ES} as $\Delta V_{C_{ES}}$, $\Delta V_{C_{ES}}$ is:

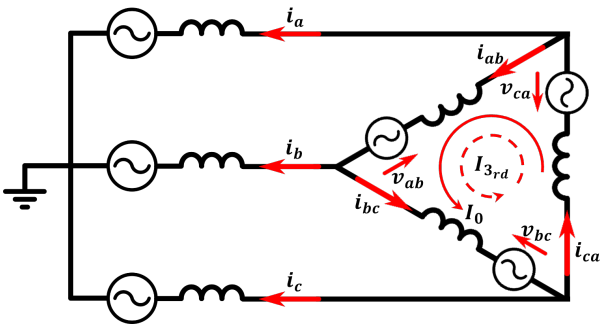

Fig. 7: Equivalent circuit for current analysis

$$\Delta V_{C_{ES}} = \frac{1}{C}\int_0^{2\pi} \overline{I_{ES}}\, d\theta = \frac{2\pi \cdot \overline{I_{ES}}}{C} \tag{7}$$

where $\overline{I_{ES}}$ is the average of I_{ES}. I_{ES} only contains DC current, and charges to the capacitor. So, capacitors in ES-MBSMs have higher voltage than those in normal MBSMs. As presented in Fig. 4, whatever the stack current direction is, stack current always flows into the cathode of the capacitor with higher voltage and discharge it. According to Eq. (6), stack current is composed of a sine wave in fundamental frequency and a sine wave in the third harmonics. The positive half cycle of the stack current is symmetrical to the negative half cycle. Denote the SM voltage variation caused by overall stack current in the positive half cycle as ΔV_{C_p}, and denote the voltage the SM voltage variation caused by overall stack current in the negative half cycle as ΔV_{C_n}. The following equations hold:

$$\Delta V_{C_p} = |\frac{1}{C}\int_0^{\pi} \hat{I_{ph}} \cdot sin\,\theta + \hat{I_{3rd}} \cdot sin\,3(\theta + \Delta\varphi)\, d\theta| \tag{8}$$

$$\Delta V_{C_n} = |\frac{1}{C}\int_{\pi}^{2\pi} \hat{I_{ph}} \cdot sin\,\theta + \hat{I_{3rd}} \cdot sin\,3(\theta + \Delta\varphi)\, d\theta| \tag{9}$$

Extend Eq. (8) and Eq. (9), we have:

$$\Delta V_{C_p} = \Delta V_{C_n} = \frac{2}{C} \cdot \hat{I_{ph}} + \frac{2}{3C} \cdot \hat{I_{3rd}} \cdot cos\,(3\Delta\varphi) \tag{10}$$

It should be ensured that the capacitor voltage at the start of each cycle is equal to the capacitor voltage at the end of the same cycle to maintain voltage balancing, which means the voltage deviation caused by ES current should be offset by voltage deviation caused by stack current:

$$\Delta V_{C_{ES}} = \Delta V_{C_p} + \Delta V_{C_n} \tag{11}$$

Combine Eq. (7), Eq. (10), and Eq. (11), we have:

$$\Delta V_{C_p} = \Delta V_{C_n} = \frac{\Delta V_{C_{ES}}}{2} = \frac{\pi \cdot \overline{I_{ES}}}{C} \tag{12}$$

The higher active power the STATCOM output, the larger the ES current will be. Therefore, the optimal phase angle should maximize the capability of the phase current to offset the voltage deviation caused by ES current in a whole cycle, which means ΔV_{C_p} and ΔV_{C_n} should be maximized. According

to Eq. (10), and Eq. (12), the optimum is obtained when $cos\,(3\Delta\varphi) = 1$, as a result:

$$\Delta\varphi = \frac{\phi_{I_{3rd}}}{3} - \phi_{I_{ph}} = 0 \tag{13}$$

The STATCOM operating point describes how much active power and reactive power are released by the converter, represented by p.u. value P_{ref} and Q_{ref}, respectively. Denote the phase angle of stack voltage as $\phi_{U_{ph}}$, the operating point is described as:

$$\begin{cases} P_{ref} = cos\,(\phi_{U_{ph}} - \phi_{I_{ph}}) \\ Q_{ref} = sin\,(\phi_{U_{ph}} - \phi_{I_{ph}}) \end{cases} \tag{14}$$

So, $\phi_{I_{ph}}$ can be represented with converter operating point and $\phi_{U_{ph}}$:

$$\phi_{I_{ph}} = \phi_{U_{ph}} - \arctan\,(\frac{Q_{ref}}{P_{ref}}) \tag{15}$$

The derivation of $\phi_{U_{ph}}$ can be found in ref. [26]. Notice that the reference direction of stack voltage applied in this paper, as shown in Fig. 1 and Fig. 7, is opposite to that in the literature. So we have:

$$\phi_{U_{ph}} = \frac{2\pi(m-1)}{3} - \frac{\pi}{6} \tag{16}$$

where m = 1, 2, 3 representing the sequence of three phase. Combine Eq. (13), Eq. (15), and Eq. (16), the optimal phase angle of I_{3rd} is:

$$\phi_{I_{3rd}} = 3 \cdot \phi_{I_{ph}}\ mod\ 2\pi = \frac{3}{2}\pi - 3\arctan\,(\frac{Q_{ref}}{P_{ref}}) \tag{17}$$

B. Comparison of Different Operation Modes

Depending on the MBSM states, ES-MBSM capacitor charging current has three cases: (1) $I_{ES} + |I_S|$ when I_S flow into the anode of the capacitor, (2) $I_{ES} - |I_S|$ when I_S flow into the cathode of the capacitor and (3) I_{ES} when the capacitor is bypassed. In comparison, the charge current of capacitor in normal MBSMs is $|I_S|$, $-|I_S|$ or 0. Soft-parallel mode enables I_S to flow into the capacitors with lower voltage than their neighbours. The energy management controller keeps the total energy stored in the stack balanced during operation, so in most cases the voltage of ES-MBSM tends to be greater than the rated value, while voltage of capacitor in normal MBSM deviates to a lower value. I_{ES} and I_S flowing through a ES-MBSM and a normal MBSM next to it in soft-parallel mode are shown in Fig. 8 (a). I_{ES} is all injected to C_1 because of the diodes and consequently $V_{C_1} > V_{C_2}$, resulting in I_S flowing in C_2. Then the voltage difference decreasing speed is:

$$\frac{d\Delta u}{dt} = \frac{1}{C_{SM}}\,(I_{ES} - |I_S|) \tag{18}$$

The absolute value of the stack current needs to be larger than I_{ES} to reduce the voltage difference.

When the MBSMs operate in conventional FBSM based mode, I_S tends to charge the capacitor whose voltage is higher than average value, while discharge those whose voltage is lower, to accelerate the SM voltage balancing. The current state is shown in Fig. 8 (b). The voltage difference can be reduced as long as $|I_S| > I_{ES}/2$ according to the voltage difference decreasing speed calculated in (19):

$$\frac{d\Delta u}{dt} = \frac{1}{C_{SM}}\,(I_{ES} - 2\,|I_S|) \tag{19}$$

Less stack current is required for voltage balancing than the former mode. Consequently, the conventional FBSM based mode is more powerful than the soft-parallel based mode in terms of reducing the voltage deviation while the same amount of circulating current is injected.

While operating in the soft-parallel based mode, the interconnection states of the MBSMs are obtained by compare the modulation index with PWM carriers. Based on the semiconductor states summarized in Table I, at most four semiconductors (out of eight semiconductors in an interconnection) change their states in each SM state transition, so the average semiconductors switching frequency is less than the PWM frequency. In contrast, in the FBSM based mode the gate signals are updated after every controller step. The switching loss when operating at the soft-parallel based mode is consequently lower than that in the FBSM based mode.

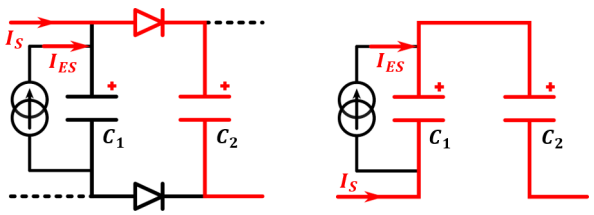

Fig. 8: ES current and stack current flowing through a ES-MBSM and a normal MBSM in (a) Soft-paralleling based mode, (b) FBSM based mode.

TABLE II: System Parameters

Parameters	Value	Parameters	Value
Nominal Power	30 MVA	N_{sm} per Stack	15
AC Voltage (RMS)	18 kV	Nominal V_{sm}	2000V
AC Frequency	50 Hz	MBSM Capacitance	2.5 mF
Phase Inductance	0.1 pu	Sampling Time	5 μs
Stack Inductance	0.1 pu	PWM Frequency	1 kHz

V. Simulation Results and Discussion

Simulation models of partially rated ES STATCOMs in three different configurations are built in MATLAB/Simulink to evaluate the converter performances and the proposed control system. The system parameters are summarized in Table II. The quantity ratio of ES-MBSMs to total MBSMs in a stack is $9/15$ (60%). ES-MBSMs are distributed evenly in the stack. V_{Thr} is set at 2.5% of the nominal capacitor voltage (50V) to determine the operation mode. I_{Thr} is determined by the current measurement resolution and communication bandwidth, and is set as 50A in simulation. In all simulations, the STATCOM output 1 p.u. apparent power while only the power factor (PF) changes.

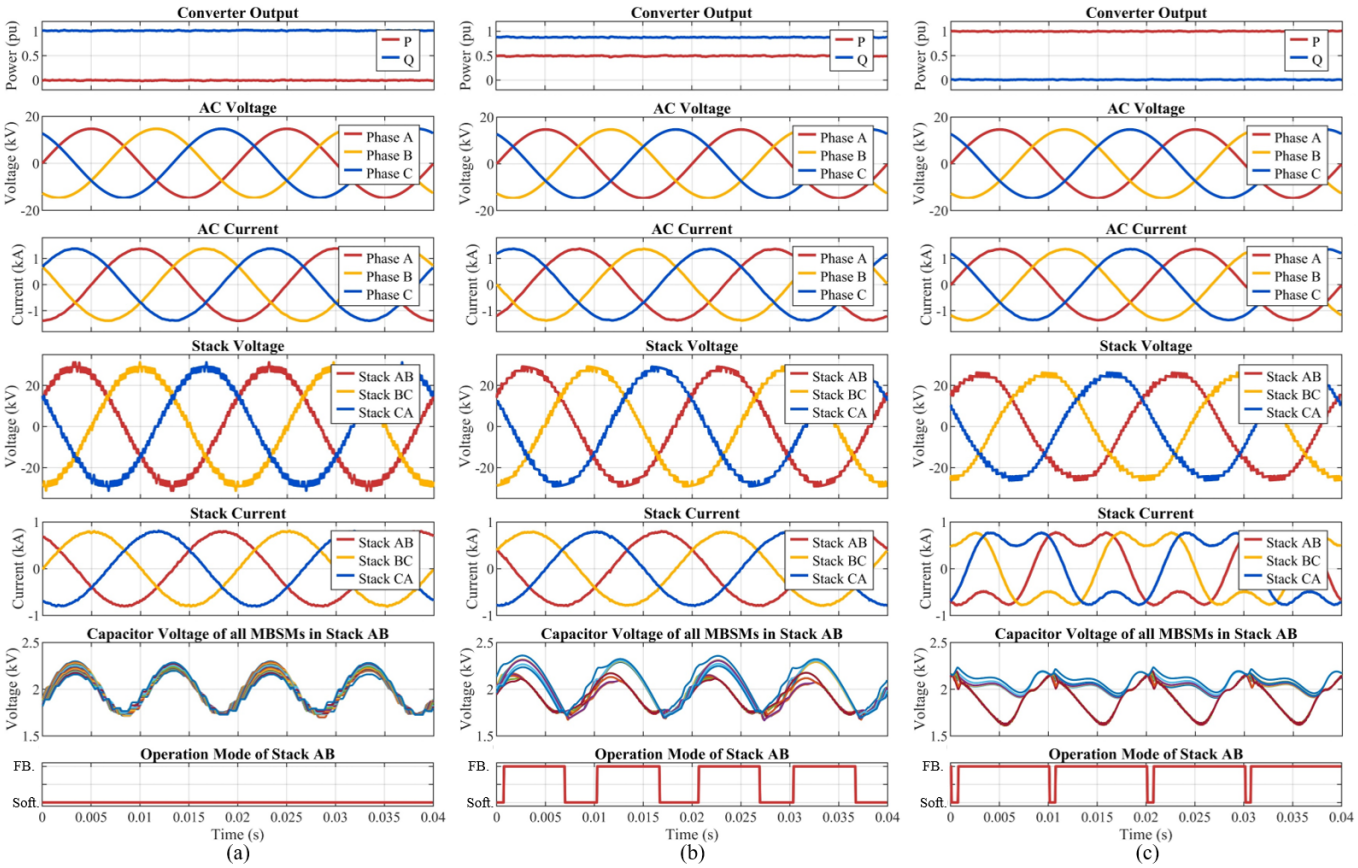

Fig. 9: Converter performances in different operation points:(a) PF = 0, (b) PF = 0.5, (c) PF = 1.

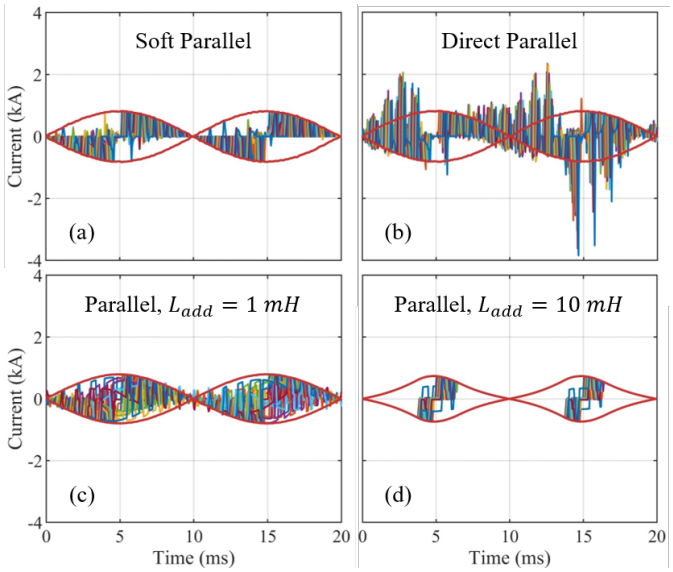

Fig. 10: Instantaneous capacitor currents with different parallel mechanism: (a) Soft parallel; (b) Direct parallel; (c) Parallel through 1 mH inductors; (d) Parallel through 10 mH inductors. Red lines represent the envelop of stack current.

A. Normal Operation

The converter ability of reactive power compensating as well as providing active power for frequency support, are verified by simulation results in Fig. 9. Three different operating points are investigated: (1) PF = 0 as in Fig. 9 (a); (2) PF = 0.5 as in Fig. 9 (b); (3) PF = 1 as in Fig. 9 (c). Results show the power outputs are well tracked, and the AC currents have low total harmonic distortion (THD) in different set-points. Capacitor voltages stay balanced and the upper bound of the deviation stays in the safe margin (20% of the rates SM voltage). I_{3rd} with the optimal phase angle derived by Eq. (17) and an amplitude of 300A is injected to maintain the voltage balancing when PF = 1, so third harmonics current exists in the stack current in Fig. 9 (c). The ratio of soft-paralleling based mode decreases as the increase of power factors. The PRES MBSM STATCOM is verified to be capable to output 1 p.u. active power with the proposed low level controller applied.

TABLE III: ΔV_{SM} and I_{cap} in MMSPC versus L_{add} when PF = 0

L_{add} (H)	10^{-8}	10^{-7}	10^{-6}	10^{-5}	10^{-4}	10^{-3}
ΔV_{sm} (V)	137	142	222	338	480	671
I_{cap} (A)	3775	3296	2337	1936	1241	835

TABLE IV: ΔV_{SM} in MBSM and in MMSPC versus PFs

Power Factor		0	0.1	0.2	0.3
ΔV_{sm} (V)	MBSM, Soft parallel	159	172	276	402
	MMSPC[20], L_{add} = 1mH	671	692	745	890

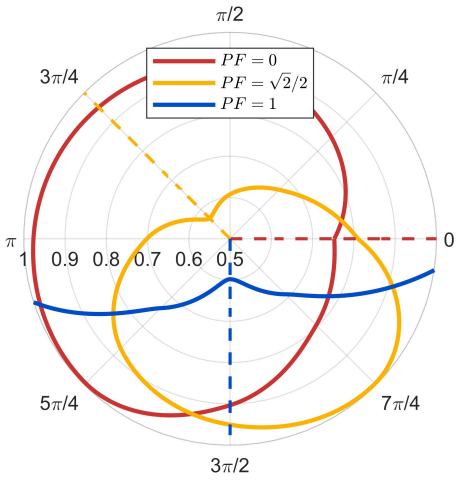

Fig. 11: Normalized maximum SM voltage deviation versus phase angle of circulating current at three different set-points. Dashed lines are optimal value from Eq. (17).

B. Effectiveness of the Soft-parallel mechanism

The fundamental benefit of the soft-parallel over MMSPC [20], [21] is to suppress the inrush current resulted by capacitor parallel without the requirement of using additional inductors. Instantaneous capacitor currents (I_{cap}) with different parallel mechanism when the STATCOM operating at PF = 0 output are investigated. As has been explained in Section II, with soft-parallel I_{cap} is restricted by the envelop of stack current as the capacitor voltage difference is clamped by the reverse blocked diodes, as is shown in Fig. 10 (a). Direct parallel leads to large inrush current, the amplitude of which is about four times of the stack current, as in Fig. 10 (b). Fig. 10 (c) and (d) demonstrate the effect of different inductance to inrush current in MMSPC. Similar I_{cap} suppression performance as the soft-parallel mechanism can be achieved with L_{add} = 1 mH. However, large harmonics occurs in the stack current when L_{add} = 10 mH.

SM voltage deviation (ΔV_{SM}) is also of great interest and is suggested to be kept lower than 20% of the rated SM voltage [27] as it determines the AC output quality as well as the volume and cost of SM capacitors. ΔV_{SM} and I_{cap} in MMSPC versus different L_{add} are listed in Table III. It can be summarised that as the applied inductance increases, so does ΔV_{SM}, while I_{cap} decreases. $L_{add} < 1$ mH can't effectively suppress I_{cap}. In the simulation of MMSPC, $L_{add} = 1$ mH to fairly compare ΔV_{SM} versus different power factors with the soft-parallel method, as listed in Table IV. The result indicates MMSPC may not capable enough for a PRES STATCOM as the ΔV_{SM} is already larger than 20% of the rated SM voltage when PF = 0.3.

C. Optimal Phase Angle of Additional Circulating Current

Fig. 11 illustrates the effect of circulating current phase angles to the normalized maximum ΔV_{SM} within a stack at three different operation points with the same circulating current amplitude. The presented data is obtained through dividing the measured ΔV_{SM} by the maximum deviation versus phase angle in each operation point (195V for PF = 0, 815V for PF = $\sqrt{2}/2$, and 900V for PF = 1). When PF = 0 the minimum deviation is obtained when $\phi_{I_{3rd}} = 0$. The optimum $\phi_{I_{3rd}}$ becomes $3/4\pi$ when the active power output is equal to reactive power (PF = $\sqrt{2}/2$), while it is $3/2\pi$ at PF = 1. The performances verify the analytical result from Eq. (17). It could also be concluded from Fig. 11 that the more active power released from the converter, the larger deviation is seen by the SM voltages. The system becomes unstable when the converter generating full active power if $\phi_{I_{3rd}} \notin [5/4\pi, 7/4\pi]$ as ΔV_{SM} is too large.

TABLE V: Different STATCOM Configurations

Label	SM Type	Low level Control Scheme
Conf. 1	MBSM	The controller as is shown in Fig.6
Conf. 2	FBSM	Conventional SM sorting controller [11]
Conf. 3	FBSM	VBA controller proposed in [13]

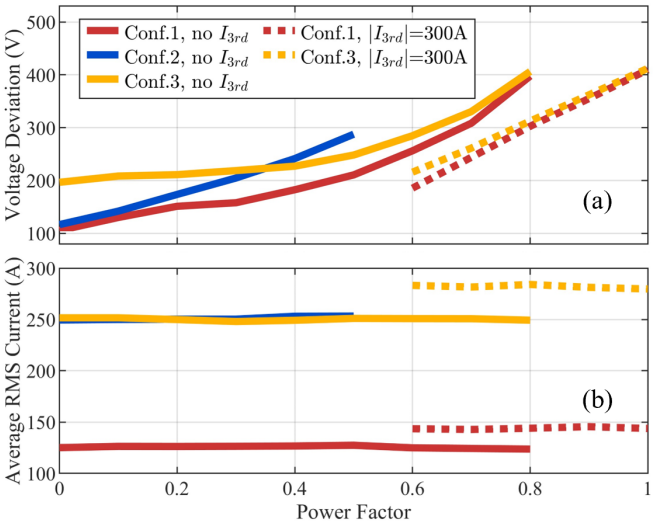

Fig. 12: (a) Maximum ΔV_{SM}, and (b) Average RMS currents of all semiconductors in a stack versus PF.

D. Active power capability and losses

The power capability and efficiency of the MBSM STATCOM are further investigated and compared with its single bus FBSM counterparts, as listed in Table V. The PWM frequencies of Conf. 1 and Conf. 2 are both 1000 Hz, while the sorting frequency in the iteration based controller of Conf. 3 is set as 10kHz as a trade-off between tracking accuracy and power efficiency. In Fig. 12, the solid lines show the results with no I_{3rd}, whereas the dashed lines represent results under the same I_{3rd} with the optimal phase angle and an amplitude of 300A. Higher PF represents larger I_{ES} charges capacitors in ES-MBSM. Hence, capacitor voltages are more likely to deviate from each other. Overall, the maximum ΔV_{SM} increases in all STATCOMs as the PF increasing. Conf. 1 has the best performances in all set-points whether the additional circulating current is injected or not. Conf. 2 has lower ΔV_{SM} than Conf. 3 when PF $\leq$ 0.4, however will become unstable if PF $>$ 0.5. The active power capability of Conf. 1 and Conf. 3

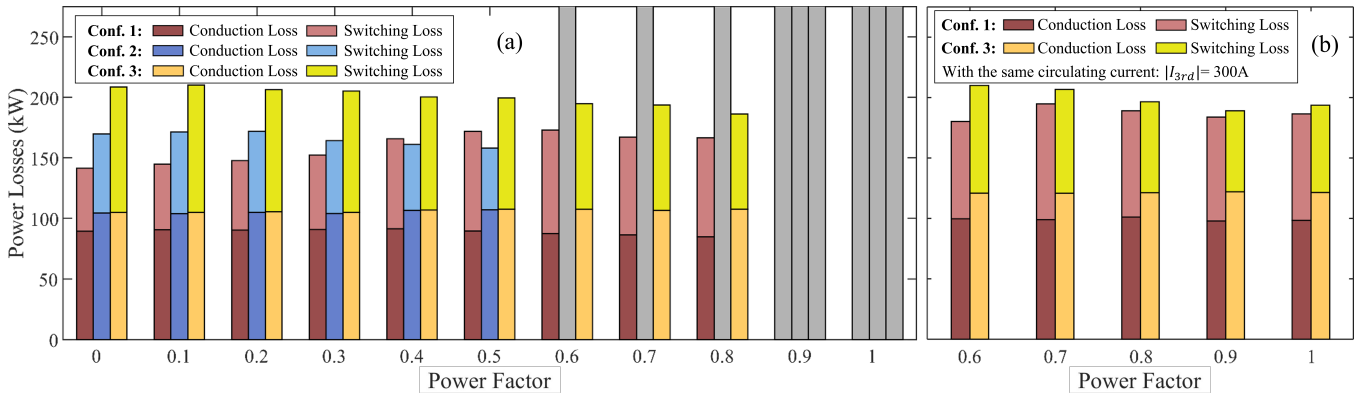

Fig. 13: Semiconductor losses of different STATCOMs versus PF: (a) with no I_{3rd}; (b) $|I_{3rd}|$ = 300A.

are both up to 0.8 p.u. if no I_{3rd} applied. While comparing the solid and dashed lines, it can be concluded that not only will the maximum ΔV_{SM} be reduced but also the active power capability can be further pushed to 1 p.u. with I_{3rd} applied. Moreover, the average RMS currents of all semiconductors in a stack in the Conf. 1 is approximately halved in all set-points, as in Fig. 12 (b).

The losses analysis are conducted based on the IGBT module FZ1200R33HE3 produced by Infineon from which the losses curves have been extracted to compute the energy lost through conduction and switching at every simulation time step ($5\mu s$). The power losses of three different STATCOMs are summarized in Fig. 13. When the active power output is greater than a certain value, the SM voltages will be imbalanced and the whole converter cannot normally operate any more. Losses for an unstable STATCOM are not applicable and are presented as grey columns. Fig. 13 (a) presents losses of all three configurations when no I_{3rd} is applied. Conf. 1 has the lowest conduction losses in all set-points. With the increase of PF, the switching losses are also increasing as Conf. 1 operates less frequently in the soft-paralleling based mode. Notice that even though Conf. 2 has lower total losses when PF $\in [0.4, 0.5]$, it has much larger SM voltage deviation and distortions compared with Conf. 1. Additional I_{3rd} is inserted to output 1 p.u. active power as introduced before. The amplitude of I_{3rd} should also ensure that the peak stack current does not exceed 1 p.u., as suggested in [13], [28]. With the system parameters listed in Table II, the maximum amplitude of total stack current is 962A, and the maximum amplitude of I_{3rd} can be injected is 394A. Different circulating current amplitudes are investigated in the simulation model, and the results show 300A is the minimum circulating current amplitude that ensure the studied STATCOM (Conf. 1, 60% ES-MBSMs) can output 1p.u. active power while the maximum SM voltage deviation is still within the normal range (20% of the nominal SM voltage). Fig. 13 (b) presents the power losses of Conf. 1 and Conf. 3 when the same I_{3rd} with the optimal phase angle and an amplitude of 300A applied. Even when the maximum circulating current amplitude (394A) is applied in Conf. 2, the maximum power factor is 0.5, the same as when no circulating current is injected, as in Fig. 13 (a). The active power output capability of Conf. 2 does not perform as well as Conf. 1 and Conf. 3. So, the results of Conf. 2 is excluded in Fig. 13 (b). Conf. 1 almost fully operates in conventional FBSM based mode, as illustrated in the last figure of Fig. 9(c), and its losses are very close to that of the Conf. 3. The MBSM implementation is more stable at higher PF – as demonstrated in Fig. 12 and Fig. 13 – whereas the FBSM implementation loses stability around the PF = 0.5 (Conf. 2) or at the penalty of large additional circulating current (Conf. 3). The PRS MBSM STATCOM is a potential solution for fast frequency response in the first few seconds of a major grid disturbance. As part of the ancillary service, fully active power operation mode takes up a comparatively small portion of a STATCOM's lifetime compared to its major job, reactive power support. Consequently, the proposed MBSM STATCOM and the corresponding control system is able to effectively improve the power efficiency, especially in long term operation.

VI. Conclusion

The MBSM STATCOM utilizes twice the number of semiconductors in exchange of better power efficiency and lower semiconductor current. The directional conduction of diodes leads to the soft parallel mechanism, which improves the SM sorting performance. The soft parallel of MBSM is however more effective in reactive power mode than active power mode due to the location of ES, which see their current circulation limited to their own SM capacitor. The proposed controller for the MBSM STATCOM dynamically switches between two operation modes to reduce the converter losses over the extended range of active power, in line with the state-of-the-art papers. Simulation results confirm the earlier point, in that PRES-MBSM-STATCOM performs better at pure reactive power set-points and marginally better at high active power. This is explained by the fact that MBSM operates more frequently in soft-paralleling mode when the ES are released less power, i.e. reactive power set-points. Future work could focus on: (1) Different capacitor sizing in MBSMs with and without ES interfaces for better voltage balancing; (2) Examining other structural configuration of the ES interfaces in the MBSM STATCOM, e.g. placing ES interfaces on the busbars connecting two adjacent MBSMs; (3) The performances with different ES-SM ratios.

ACKNOWLEDGMENT

This work is supported by the joint scholarship of China Scholarship Council (CSC) and the University of Edinburgh.

REFERENCES

[1] F. Z. Peng, "Flexible ac transmission systems (facts) and resilient ac distribution systems (racds) in smart grid," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2099–2115, 2017.

[2] S. Schneider, H. G. Platz *et al.*, "Compensation of the voltage fluctuations in the distribution network of london underground using the svc plus®," in *15th IET International Conference on AC and DC Power Transmission (ACDC 2019)*, 2019, pp. 1–8.

[3] M. Pereira, D. Retzmann *et al.*, "Svc plus: An mmc statcom for network and grid access applications," in *2011 IEEE Trondheim PowerTech*, 2011, pp. 1–5.

[4] M. N. Slepchenkov, K. M. Smedley, and J. Wen, "Hexagram-converter-based statcom for voltage support in fixed-speed wind turbine generation systems," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1120–1131, 2011.

[5] T. Lüth, M. M. C. Merlin *et al.*, "High-frequency operation of a dc/ac/dc system for hvdc applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4107–4115, 2014.

[6] M. M. C. Merlin, T. C. Green *et al.*, "The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310–317, 2014.

[7] B. Wang, X. Wang *et al.*, "Reliability model of mmc considering periodic preventive maintenance," *IEEE Transactions on Power Delivery*, vol. 32, no. 3, pp. 1535–1544, 2017.

[8] M. M. C. Merlin, D. Soto-Sanchez *et al.*, "The extended overlap alternate arm converter: A voltage-source converter with dc fault ride-through capability and a compact design," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3898–3910, 2018.

[9] P. D. Judge, M. M. C. Merlin *et al.*, "Thyristor/diode-bypassed submodule power groups for improved efficiency in modular multilevel converters," *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 84–94, 2019.

[10] J. A. Barrado, R. Grino, and H. Valderrama-Blavi, "Power-quality improvement of a stand-alone induction generator using a statcom with battery energy storage system," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2734–2741, 2010.

[11] M. Vasiladiotis and A. Rufer, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 163–175, 2015.

[12] P. D. Judge and T. C. Green, "Modular multilevel converter with partially rated integrated energy storage suitable for frequency support and ancillary service provision," *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 208–219, 2019.

[20] S. M. Goetz, Z. Li *et al.*, "Control of modular multilevel converter with parallel connectivity—application to battery systems," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8381–8392, 2017.

[13] S. Mian, P. Judge *et al.*, "A delta-connected modular multilevel statcom with partially-rated energy storage for provision of ancillary services," *IEEE Transactions on Power Delivery*, pp. 1–1, 2020.

[14] Z. Li, R. Lizana *et al.*, "Current injection methods for ripple-current suppression in delta-configured split-battery energy storage," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7411–7421, 2019.

[15] E. Wiesner, K. Masuda, and M. Joko, "New 1200v full sic module with 800a rated current," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1–9.

[16] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular multilevel converter with series and parallel module connectivity: Topology and control," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 203–215, 2015.

[17] Z. Li, R. Lizana F. *et al.*, "A modular multilevel series/parallel converter for a wide frequency range operation," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9854–9865, 2019.

[18] Z. Li, R. Lizana F. *et al.*, "Module implementation and modulation strategy for sensorless balancing in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8405–8416, 2019.

[19] K. Ilves, F. Taffner *et al.*, "A submodule implementation for parallel connection of capacitors in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3518–3527, 2015.

[21] K. Ilves, Y. Okazaki *et al.*, "Capacitor voltage balancing in semi-full-bridge submodule with differential-mode choke : (invitedpaper)," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018, pp. 2335–2342.

[22] M. Glinka and R. Marquardt, "A new ac/ac multilevel converter family," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 662–669, 2005.

[23] C. Hao and M. Merlin, "Automatic derivation of state-space model from linear electrical circuits with dependent variables using modified nodal analysis," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, pp. 1–6.

[24] P. Münch, D. Görges *et al.*, "Integrated current control, energy control and energy balancing of modular multilevel converters," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 150–155.

[25] S. Lu, L. Yuan *et al.*, "An improved phase-shifted carrier modulation scheme for a hybrid modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 81–97, 2017.

[26] M. Vasiladiotis and A. Rufer, "Balancing control actions for cascaded h-bridge converters with integrated battery energy storage," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10.

[27] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *IET Power Electronics*, vol. 8, no. 3, pp. 350–360, 2015.

[28] E. Spahic, C. P. Susai Sakkanna Reddy *et al.*, "Multilevel statcom with power intensive energy storage for dynamic grid stability - frequency and voltage support," in *2015 IEEE Electrical Power and Energy Conference (EPEC)*, 2015, pp. 73–80.