Towards Development of Flexible Sensor Systems Based on Organic Thin-film Transistors

By

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Declaration of Authenticity and Author's Rights

This thesis is the result of the author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

Amayikai Ajibauka Ishaku

Date: November 2021

This thesis is dedicated to my loving family, caring friends, and supportive supervisors

Author's Declaration

I declare that the work presented in this thesis has been carried out by me, unless otherwise acknowledged.

Amayikai Ajibauka Ishaku

Date: November 2021

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Abstract

To date, significant progress has been made to advance the performance of organic thin-film transistors (OTFTs). These included new materials and structures and innovative fabrication methods to yield properties such as light-weight, mechanical flexibility, and low-temperature fabrication. Yet, many OTFTs still suffer from low on-state drain current and electrical instability seen as a hysteresis or a shift in the transistor transfer characteristics, thus hindering wider OTFT applications. This thesis aims to tackle these issues by presenting low-voltage OTFTs based on air-stable dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) and hydrophobic bi-layer dielectric made of aluminium oxide and octadecyl phosphonic acid ($AlO_x/C_{18}PA$) on PEN substrates. The fabricated transistors are approximately hysteresis-free and exhibit on-state drain current approaching 100 µA at gate-source and drain-source voltages of –2 V. This is a notable advancement compared to the performance of similar devices reported in the literature and indicative of a robust design and fabrication. High on-state drain current was enabled by ultra-thin gate dielectric and interdigitated source/drain contacts leading to high channel width-to-length ratio and small transistor area.

The electrical stability was studied in the above transistors, both fresh and aged. AC square pulses with constant bias time of 1 second and varying pulse period were simultaneously applied to gate and drain of the transistor to simulate the recurrent turn-on/turn-off transistor operation. OTFT performance marginally degraded under AC pulses, with the exception of field-effect mobility that improved. Degradation

proceeded faster in aged OTFTs stored in dark ambient environment but the on-state drain current stabilised after ~500 pulses. The stabilisation resulted from the rising field-effect mobility compensating the threshold voltage increase. Finally, the inclusion of the above OTFT as a voltage amplifier in a temperature sensor system raised the temperature sensitivity by a factor of ~5, thus laying foundation for future flexible sensors and circuit applications.

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List of symbols and acronyms

Acronyms

AC	Alternating current
a-IGZO	Amorphous indium gallium zinc oxide
BGTC	Bottom gate top contact
C-f	Capacitance vs frequency
C-V	Capacitance vs voltage
D	Drain
DC	Direct current
DI	Deionized
DNTT	Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene
FET	Field-effect transistor
G	Gate
HOMO	Highest occupied molecular orbital
I-V	Current vs voltage
LUMO	Lowest unoccupied molecular orbital
MIM	Metal insulator metal
NTC	Negative temperature coefficient
OLED	Organic light-emitting diode
OTFT	Organic thin-film transistor
PMMA	Polymethyl methacrylate
PDQT	Diketopyrrolopyrrole–thiophene

PEN	Polyethylene naphthalate
PI	Polyimide
ppm	Particle per million
PS	Polystyrene
PUT	Putrescine
PVA	Polyvinyl alcohol
PVC	Polyvinyl chloride
PVP	Polyvinyl phenol
PW	Pulse width
RFID	Radio frequency identification
RTD	Resistance temperature detector
S	Source
SAM	Self-assembled monolayer
SGOTFT	Suspended gate organic thin-film transistor
SPGU	Semiconductor pulse generator unit
TC	Transfer characteristic
TCR	Temperature coefficient of resistance
TGBC	Top gate bottom contact
UV	Ultraviolet
UVOCS	Ultraviolet ozone cleaning system
WF	Work function

Symbols

$\Delta L/L$	Channel length modulation

ΔV_{TH}	Threshold voltage shift (V)
μ	Field-effect mobility (cm^2/Vs)
μ_0	Low-field mobility (cm^2/Vs)
A	Cross-sectional area (cm^2)
Al	Aluminium
Al_2O_3	Aluminium oxide
AlO_x	Aluminium oxide
Au	Gold
$BaZrTiO_3$	Barium zirconium titanate
C	Capacitance (F)
$C_{18}PA$	Octadecyl phosphonic acid
C_{AlOx}	Capacitance of aluminium oxide (F/cm^2)
C_{C18PA}	Capacitance of octadecyl phosphonic acid (F/cm^2)
C_{diel}	Gate dielectric capacitance per unit area (F/cm^2)
CeO_2	Ceric oxide
Cr	Chromium
d	Thickness of the dielectric layer (mm)
d_1	Thickness of the AlO_x layer (mm)
d_2	Thickness of the $C_{18}PA$ layer (mm)
$E(x)$	Electric field (V/m)
f	Frequency (Hz)
g_m	Transconductance (S)
H_2O	Water
HfO_2	Hafnium oxide

I_D	Drain current (A)
i_d	Drain-to-source current (peak-peak) (A_{PP})
I_G	Gate leakage current (A)
I_{OFF}	Off-state drain current (A)
I_{OFF}*L/W	Normalised off-state drain current (A)
I_{ON}	On-state drain current (A)
I_{ON}*L/W	Normalised on-state drain current (A)
I_{ON}/I_{OFF}	On/off current ratio
J	Current density (A/cm^2)
k	Dielectric constant or relative permittivity
L	Channel length (µm)
L_p	MIM structure electrode length (µm)
n	Number of MIM structures
N_2	Nitrogen
O_2	Oxygen
P(VDF-TrFE)	Poly(vinylidene fluoride-trifluoroethylene)
P(VDF-TrFE-CFE)	Poly(vinylidene fluoride-trifluoroethylene-chlorofluroethylene)
Q	Accumulated charge (C)
q	Charge of an electron (C)
Q(x)	Charge density at point x in the channel (C/m)
R_C	Contact resistance (Ω/cm^2)
R_{CH}	Channel resistance (Ω/cm^2)
R_D	Drain resistance (Ω)
R_G	Gate resistance (Ω)

R_T	Thermistor resistance (Ω)
S	Subthreshold slope (mV/decade)
t	Time (s)
T	Pulse period (s)
Ta_2O_5	Tantalum pentoxide
t_c	Channel thickness (nm)
TiO_2	Titanium oxide
TiO_x	Titanium oxide
V	External voltage (V)
$V(0)$	Voltage at the source side of the channel (V)
$V(L)$	Voltage at the drain side of the channel (V)
$V(x)$	Voltage at point x in the channel (V)
V_D	Drain voltage (V)
V_{DD}	Supply voltage (V)
VD_{EODR}	Effective overdrive drain voltage (V)
V_{DS}	Drain-to-source voltage (V)
V_G	Gate voltage (V)
V_{GS}	Gate-to-source voltage (V)
v_{gs}	Gate-to-source voltage (peak-peak) (V_{PP})
V_{IN}	Input voltage (V)
V_{OUT}	Output voltage (V)
V_{PP}	Peak- to-peak voltage (V)
V_S	Source voltage (V)
VS_{EODR}	Effective overdrive source voltage (V)

V_{SS}	Subthreshold slope voltage (V)
V_{TH}	Threshold voltage (V)
W	Channel width (mm)
W_p	MIM structure electrode width (mm)
x	Point located along the channel length between drain and source
ZrO_2	Zirconium dioxide
α	Steady state value at infinity
β	Stretching parameter
γ	Mobility enhancement factor
δ_{VT}	Threshold voltage bias sensitivity
ε	Permittivity
ε_0	Permittivity of vacuum (F/m)
ε_r	Relative permittivity
λ	Channel modulation factor
p	Hole carrier density (/cm^2)
σ	Electrical conductivity (S/m)
τ	Time constant (s)

List of publications

Journal papers

1. Amayikai A. Ishaku and Helena Gleskova. "Potential of low-voltage organic transistors with high on-state drain current for temperature sensor development." *Organic Electronics*, vol. 93, 2021, p. 106152.

2. Afra Al Ruzaiqi, Amayikai A. Ishaku, and Helena Gleskova. "Organic thin film transistors with multi-finger contacts as voltage amplifiers." *IEEE Access*, vol. 6, 2018, p. 43770-43775.

Conference papers

1. Amayikai A. Ishaku, Afra Al Ruzaiqi, and Helena Gleskova. "Low-Voltage High-Transconductance Dinaphtho-[2, 3-b: 2', 3'-f] thieno [3, 2-b] thiophene (DNTT) Transistors on Polyethylene Naphthalate (PEN) Foils." *IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*. IEEE, 7th – 10th July 2019, Glasgow, UK.

2. Amayikai A. Ishaku, Aris Tranganidas, Slavomír Matúška, Róbert Hudec, Graeme McCutcheon, Lina Stankovic, Helena Gleskova. "Flexible force sensors embedded in office chair for monitoring of sitting postures." *2019 IEEE International Conference on Flexible and Printable Sensors and Systems (FLEPS)*. IEEE, 7th – 10th July 2019, Glasgow, UK.

Chapter 1

Introduction

1.1 Organic semiconductors in electronics

The introduction of organic semiconductors and the subsequent development of various organic devices has transformed the field of flexible and wearable electronics. The term ‘organic’ refers to material compounds composed of primarily carbon and hydrogen, while ‘semiconductor’ refers to materials with electrical conductivity which lies between a conductor with high conductivity and insulator with low conductivity. Organic semiconductors for organic transistors are based on polymers or small molecules [1.1, 1.2]. Their molecular properties make them insulators until becoming semiconducting as a result of charge injection, optical excitation, or thermal activation [1.3]. Their electrical conductivity and formation of electric current depends on the charge carrier transport in the highest occupied

molecular orbital (HOMO) or lowest unoccupied molecular orbital (LUMO), also referred to as the valence and conduction bands in inorganic semiconductors, respectively [1.4]. Low-lying HOMO energy levels have been shown to promote air and thermal stability and high carrier mobility in small molecule organic semiconductors such as dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT), [1.1] making them favourable organic semiconductor material for transistor research.

The advantage of organic semiconductors lies in their chemistry. Organic semiconductors can be modified at the molecular level to provide wide variety of customisation to meet design requirements [1.5]. Therefore, organic semiconductors can have molecular properties allowing them to flex, stretch or print on flexible substrates [1.6], with minimal or reversible effect on performance or stability [1.7]. Additionally, self-healing properties have also been explored for electronic skin applications [1.8]. Such use of organic semiconductors in organic thin-film transistors has fuelled the rapid progress of flexible and wearable devices, thus altering the way technology is implemented and used. With potential for scalability, integration of electronics onto flexible substrates, and inexpensive large-area roll-to-roll manufacturing compatible with printing technology, it is no surprise that innovative applications including flexible organic light emitting diode (OLED) displays and lighting, and large-area printed organic solar cells [1.9-1.12] are becoming increasingly popular, see Figure 1.1.

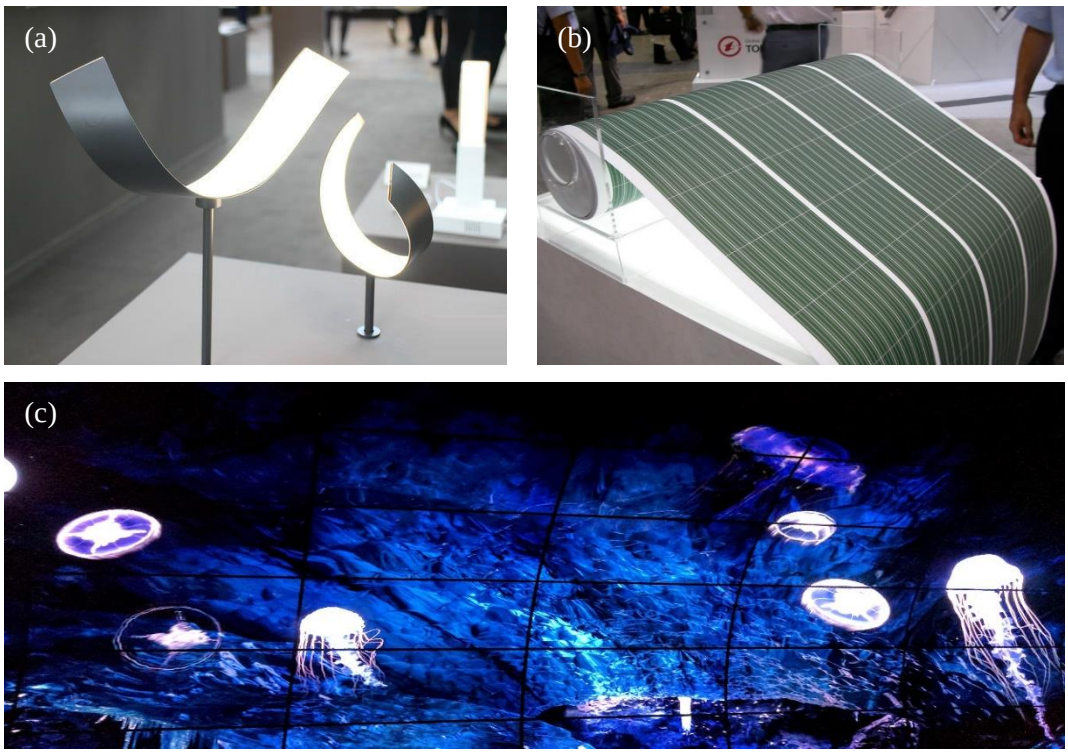

Figure 1.1: OLED ultra-thin panel for lighting [1.13] (a), large area printed organic photovoltaic [1.14] (b), and flexible display [1.15] (c)

1.2 Thesis motivation

The current state of flexible and wearable electronics demands inexpensive materials and simple low-temperature fabrication techniques married with devices that deliver high performance at low-voltages, while enabling mechanical flexibility. Organic thin-film transistors (OTFTs) are ideal candidates offering great potential through careful selection of materials, downscaling in size for increased integration density [1.16], and diverse range of flexible and stretchable substrate solutions. This is in contrast to traditionally rigid, bulky, and fragile inorganic devices. In addition, OTFT-based sensors could provide initial stage amplification and on-site transducing of physical stimulus into electrical signal in miniaturised sensors. Yet, OTFTs have some drawbacks. Current state-of-the-art solutions address their performance, low-

voltage operation, short-channel downscaling effects, hysteresis, and electrical or atmospheric instabilities. Some of the developed solutions are not adopted, typically because of cost, obtainability of material and/or equipment, complexity of procedures, or trade-off between enhancement of a target parameter and degradation in other parameters. For example, downscaling transistor size and channel length for increased integration density, enhanced operating speed and reduced cost is met with short channel and contact resistance effects.

This thesis discusses the fabrication, optimisation, analysis, and sensor demonstration of a low-voltage, hysteresis-free DNTT organic thin-film transistor that is optimised using simple approach to meet its integration in flexible analogue circuits and sensors. It aims to fabricate OTFTs on polyethylene naphthalate (PEN) plastic substrate to enable mechanical flexibility and to employ ultra-thin gate dielectric of medium-k material functionalised with a self-assembled monolayer (SAM) to achieve high capacitance (C_{diel}), low leakage current (I_G), and low-voltage transistor operation. Finally, enhancement of the on-state drain current (I_{ON}) and transconductance (g_m) for voltage gain amplification relies on modification of the transistor channel with interdigitated source/drain contacts based on the work previously conducted in [1.17].

OTFT stability is crucial throughout its lifetime of usage and storage. Therefore, understanding the effects of electrical and environmental factors on the OTFT performance and the origin of any transistor deterioration are essential for predicting the device behaviour over time, particularly after integration. Consequently, investigation of the bias stress effect and ambient storage is performed on fresh and aged transistors, then a stretch-exponential model is fitted to examine the degradation

in the performance parameters. Finally, integration of the OTFT in an analogue temperature sensor system is presented. Here, the transistor performs the task of transducing temperature stimuli into electrical signal and provides initial amplification.

1.3 Thesis objectives

This thesis builds on the previous development and optimisation of low-voltage OTFTs on glass substrate based on DNTT organic semiconductor and bi-layer gate dielectric made of ozone-oxidised Al functionalised with octadecyl phosphonic acid at Strathclyde University [1.17]. The following objectives were set to advance the research towards flexible analogue circuit and sensors:

- **OTFT fabrication on PEN** – Fabrication of DNTT OTFTs on PEN substrates. This should involve employment of interdigitated source/drain contacts to maximise the channel width (W) to length (L) ratio and achieve increased drain current and transconductance. The transistors should maintain the low-voltage operation, low gate-leakage current, and hysteresis-free behaviour.
- **OTFT stability** – Study of a bias stress effect under AC conditions. The AC bias stress should mimic the recurrent turn-on/turn-off of the transistors, as such approach may be implemented in sensors with infrequent data collection [1.18].
- **OTFT-based sensor** – Design of a temperature sensor based on the OTFT transistor amplifier. The experimental sensor data should be accompanied by a model that reproduces and allows prediction of the sensor behaviour in future sensor designs.

1.4 Thesis outline

This thesis is organised into 7 chapters and focuses on the fabrication, development, analysis, and sensor demonstration of low-voltage, high transconductance organic thin-film transistors based on DNTT and fabricated on PEN foils.

Chapter 2 looks at the background literature and discusses the transistor structures, materials, parameters, and regimes of operations. Furthermore, it reflects on state-of-the-art employed towards development of analogue circuits and applications. Chapter 3 describes all fabrication procedures, measurements, OTFT parameter extraction and evaluation of the metal-insulator-metal (MIM) structures. It also describes the experimental setup and measurement techniques used in the investigation of the OTFT bias stress instability, followed by the design, measurement, and analysis of OTFT-based temperature sensor system. Chapter 4 presents and discusses the effectiveness of interdigitated source/drain contact geometry and gate-width variations employed in two different OTFT designs for increasing the channel width to length ratio (*W/L*) and enhancing transistor performance. Finally, it confirms the effect of *W/L* on AC drain current and transconductance. Chapter 5 provides a study of AC bias stress on low-voltage, high drain current OTFTs and highlights the impact of ageing and pulse period (*T*) on the stability of the transistors. Chapter 6 investigates the design, construction, and full system analysis of a temperature sensor system based on high-transconductance OTFT. A DC compact model of the transistor's transfer characteristic (TC) is included in the sensor model, and a

comparison between the theory and experiment is given. Finally, chapter 7 presents the key conclusions and suggests potential future work.

1.5 Thesis contributions

This thesis details the fabrication, evaluation, and integration of low-voltage, high-transconductance DNTT OTFTs on plastic substrate into analogue sensors. The principal contributions are summarised below.

The adoption of interdigitated source/drain contacts significantly increased the drain current and transconductance of the OTFTs on PEN substrate. While the DNTT-based OTFTs with similar cross-section and standard layout of the source/drain contacts previously achieved drain current of ~1 μA at $V_{DS} = V_{GS} = –2$ V [1.19], the OTFTs on PEN foils achieved drain current of up to ~120 μA.

Next, investigation of the transistor stability under AC conditions was performed. For the first time, square AC pulses with varied pulse period were simultaneously applied to the drain and gate electrodes, causing the transistor to turn on and off repeatedly. The turn-on and turn-off voltages were −2 and 0 V respectively and four different pulse periods were used: T of 5, 20, 40 and 60 s. For each T, 1000 pulses with turn-on time of 1 s and varying turn-off times were applied to the transistors, leading to the aggregate net stress time of 1000 s in all cases. The reduction in the on-state drain current did not exceed 17% and stabilization was observed after only 500 cycles in some cases. This stabilisation is believed to result from the simultaneous increase in field-effect mobility and threshold voltage. The maximum

degradation in the on-state drain current occurred for medium *T*, thus making *T* = 60 s a favourable condition for sensor systems.

Finally, the above transistors were investigated for sensor development. To demonstrate the voltage-amplifying ability of such transistors for raising the sensitivity of a sensor, the OTFT was used to increase the response to the temperature ordinarily achieved with a thermistor. Two transistors with on-state drain current of ~60 and ~120 μA were tested, leading to voltage gain of −2.8 and −4.9 V/V, respectively, thus increasing the sensor sensitivity by a factor of up to 5.

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Chapter 2

Research background

In this thesis the OTFT has been optimised to function as a voltage amplifier in a proposed analogue sensor. This development, aimed towards integration into flexible analogue circuits, prioritises advances in low-voltage OTFTs, i.e. it implements structure, materials, and channel geometry to effectively enhance the on-state drain current and transconductance.

This chapter looks at OTFT structures, materials, principles of operation and measured parameters and explores various techniques employed to enhance OTFT performance. It begins with a brief introduction of the organic thin-film transistors and transistor materials and structures in Section 2.1, followed by the background theory and OTFT operation in section 2.2. Section 2.3 discusses various transistor parameters used in the characterisation of transistor performance. Sections 2.4 reflects on state-

of-the-art development and OTFT applications towards organic analogue circuits. Section 2.5 summarises the chapter.

2.1 Organic thin-film transistors (OTFT)

The history of the transistor can be traced back to the late 1940's when the first ever transistor was reported [2.1-2.3]. Described as a dual functioning device, the transistor was the first and only device to function both as a signal amplifier and an electronic signal control switch. Successful implementation of thin-films in transistors in the early 1960's saw the innovation of depositing thin-films of the active layers, dielectrics, metal contacts/electrodes in the first thin-film transistor [2.4]. Two decades later, in the mid 1980's, the implementation of organic semiconductor in the first organic field-effect transistor was reported [2.5].

Today, decades later, the breakthroughs in the organic materials have paved the way towards the commercialisation of organic thin-film transistors. The pursuit of OTFTs in recent years has stemmed from the unique properties offered by the organic materials when compared to their inorganic counterparts. Low-cost, large area fabrication processes replaced complex, expensive and sophisticated vacuum growth techniques combined with photolithography, as required by silicon technology [2.6]. The compatibility of organic materials with low temperature fabrication processes benefited from the introduction of a wide variety of conventional and unconventional substrate materials including glass [2.7], paper [2.8], plastic [2.9] and textile [2.10], making this technology well-suited for wearables and flexible electronics. Notable applications include flexible displays [2.11], bio-sensors [2.12, 2.13], pressure sensors

[2.14], radio frequency identification (RFID) tags [2.15], e-paper [2.16], and wearable cloth [2.17].

2.1.1 Metal-insulator-metal structure

A metal-insulator-metal or MIM structure is a two-terminal system defined by two parallel metal layers separated by a dielectric (see Figure 2.1). Also called a parallel-plate capacitor, the MIM structure shares similarities with the field-effect transistor (FET); however, the FET contains an additional semiconductor layer. The MIM structure is particularly useful for determining the capacitance of the transistor gate dielectric and thus the accumulated charge (Q) in the channel of the FET.

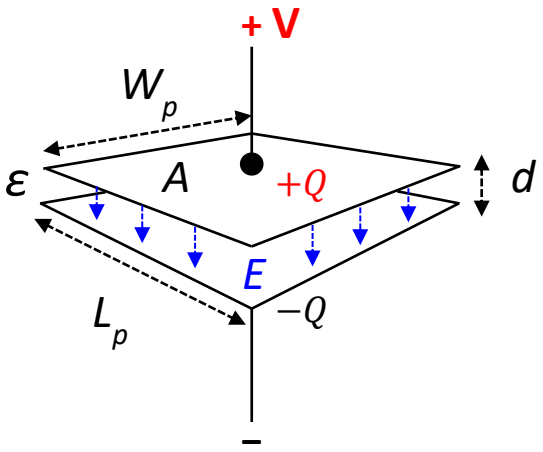

Figure 2.1: Schematic diagram of MIM structure.

The dielectric within the MIM structure becomes polarised in the presence of an electric field (E). Polarisation occurs when a voltage-induced electric field forces the 'separation and alignment' of positive and negative charges, i.e. polarisation, within the dielectric. The degree of polarisation depends on the strength of the electric field and the relative permittivity or dielectric constant (ε_r) of the given dielectric

material. The relative permittivity of all dielectric materials (other than vacuum) is ε_r > 1 and it is a characteristic material property.

As shown in Figure 2.1 and described by Equation 2.2, the MIM structure is fundamentally a parallel-plate capacitor characterised by the electrode area ($A = W_p$ x L_p), where W_p and L_p are the length and width of one electrode. The charge Q is given by the product of the MIM structure capacitance (C) and the externally applied voltage (V), as described by Equation 2.1. The dielectric capacitance per unit area (C_{diel}) is given by Equation 2.2.

$$Q = CV \tag{2.1}$$

$$C_{\text{diel}} = \frac{C}{A} = \frac{\varepsilon_0 \varepsilon_r}{d} \tag{2.2}$$

where C is the capacitance of the MIM structure, d is the thickness of the dielectric, and $\varepsilon = \varepsilon_0 \varepsilon_r$ is the permittivity, where ε_0 is 8.854x10^{-12} F·m^{-1}.

The dielectric capacitance C_{diel} is an important parameter when designing and evaluating transistors. Higher capacitance leads to higher drain current and transconductance and low-voltage operation. While higher capacitance can be achieved by reducing the thickness of the gate dielectric, very thin inorganic dielectrics lead to increased leakage current. Consequently, MIM structure with bi-layer gate dielectric consisting of aluminium oxide (AlO_x) and octadecyl phosphonic acid ($C_{18}PA$), with an average area of 2.45x10^{-3} cm^2 and C_{diel} = 0.3±0.029 μF/cm^2 is used in this thesis.

2.1.2 OTFT structures and materials

Transistors are multi-layered devices and the OTFT is no exception. Their various structural configurations depend on the arrangement of the transistor layers in relation to the position of the organic semiconductor. As such, OTFTs can take up various forms, two of which are described in this section.

In staggered OTFTs, also referred to as top-gate bottom-contact (TGBC) structure, the placement of the gate electrode sits higher than the organic semiconductor and the source and drain electrodes. The order of deposition from bottom to top is as follows: source/drain electrodes, organic semiconductor, gate dielectric and gate electrode (see Figure 2.2(a)). In inverted-staggered or bottom-gate top-contact (BGTC) configuration the gate electrode is positioned below the semiconductor layer with the source and drain electrodes placed above as shown in Figure 2.2(b). The order of deposition is as follows: gate electrode, gate dielectric, organic semiconductor and source/drain contacts.

It has been shown that the device performance can be greatly affected by the chosen structure/configuration of the OTFT [2.18-2.22]. This thesis adapts the wildly used inverted-staggered BGTC configuration for the following reasons: (a) larger saturation current [2.20] associated with staggered configurations, (b) increased mobility, and (c) reduced source/drain contact resistance [2.19-2.21].

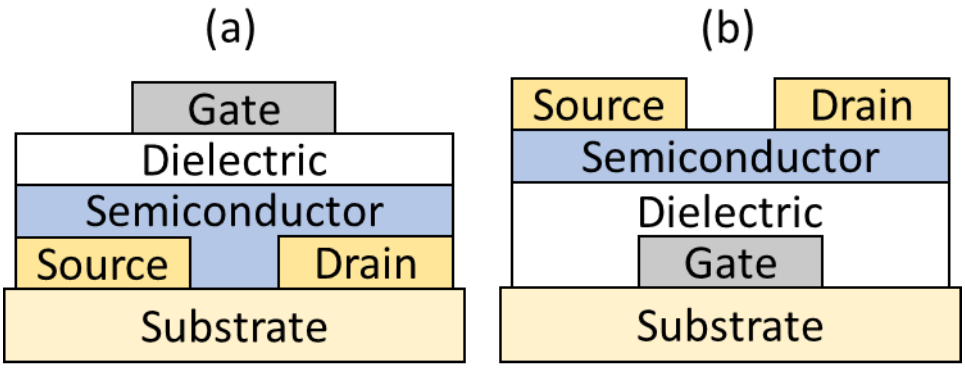

Figure 2.2: OTFT structures: TGBC (a) and BGTC (b).

In addition to the selected OTFT structure, the choice of material for each layer plays a crucial role in OTFT performance. OTFTs have three main groups of materials – metals, insulators, and semiconductors. The most wildly used metals are pliable precious metals such as gold (Au), typically used for their high conductivity and work function that matches the energy levels of the organic semiconductor, although aluminium (Al) and chromium (Cr) are also desirable and cost effective. When choosing the insulating materials, high relative permittivity and extremely low DC conductivity are desirable. Aluminium oxide (AlO_x) treated with octadecyl phosphonic acid ($C_{18}PA$) has been shown to exhibit reduced gate leakage current and low surface energy [2.23, 2.24]. Other high-k materials such as hafnium oxide (HfO_2) and titanium oxide (TiO_x) are also popular choices.

Organic semiconducting materials based on thiophenes exhibit much better air stability when compared to the previously used pentacene [1.1]. Among them the commercially-available, small-molecule, dinaphtho-[2,3-b:2’,3’-f]thieno[3,2-b] thiophene (DNTT) shows good reproducibility, low-voltage operation, and high field-

effect mobility and drain current. Consequently, thiophenes remain the popular choice of p-type semiconductor in organic transistors [2.25].

Organic transistors enable incorporation of a wide range of substrates which can provide added functionality in areas typically not suited for conventional inorganic electronics. This attribute has become the driving force behind flexibility, stretchability, and conformability centred around OTFTs. This thesis uses polyethylene naphthalate (PEN) (Optfine PQA1, DuPont Teijin) to achieve mechanically flexible OTFTs for flexible and wearable electronics. PEN is a lightweight, heat resistant polymer with low-permeability to oxygen and water and bending radius up to 1 mm [2.26].

2.2 OTFT Operation

The operation of an OTFT can be thought of as a voltage-driven current source [2.27], i.e. the application of a small voltage bias on the gate and drain terminals, with source typically grounded, creates a conduction channel allowing current to flow from drain to source, identified as drain current (I_D). The current is proportional to the gate bias, i.e. an increase in gate bias causes an increase in the accumulated charge in the channel which results in increased drain current. However, the regime of operation varies with the drain bias. Specifically speaking, the gate controls the channel formation while the drain and source electrodes act as charge carrier injection and extraction terminals.

OTFTs operate on the principles of charge carrier accumulation at the semiconductor/dielectric interface. When a gate-to-source voltage (V_{GS}) greater than

threshold voltage (V_{TH}) is applied, where V_{TH} is the minimum V_{GS} required to start the charge accumulation process, a conduction channel is formed. The accumulation of charge carriers results in high charge carrier density, thus significantly lowering the resistance between the source and drain and allowing the current to flow. In a p-channel (or n-channel) device a negative (positive) V_{GS} triggers the accumulations of holes (electrons) and subsequent channel formation. Applying voltage between drain and source (V_{DS}) results in the movement of charge carriers and drain current I_D appears. This implies that if V_{GS} is sufficiently high to form the channel, V_{DS} is still needed for I_D to flow. Figure 2.3 illustrates the formation of the conduction channel in an OTFT for various voltages applied on the transistor terminals.

During the steady-state operation of the transistor, a small portion of the charges transported along the channel penetrates through the gate dielectric into the gate and leads to an unwanted gate leakage current I_G. This results from the V_{GS} voltage that leads to vertical electric field that is much larger than the horizontal electric field resulting from V_{DS}. Therefore, the gate dielectric has two main functions: (a) to provide a high capacitance per unit area C_{diel} and (b) to minimise the gate leakage current I_G. In an ideal transistor all carriers are transported along the channel, i.e. I_G is zero and I_D is maximum. However, in practice, charges become trapped into states in the semiconductor and/or gate dielectric/semiconductor interface resulting in reduction of the accumulated charge density. These trapped charges are accounted for by the threshold voltage V_{TH} [2.28]. The charge per unit area accumulated in the transistor channel Q is therefore given as

$$Q = C_{\mathrm{diel}}(V_{\mathrm{GS}} - V_{\mathrm{TH}}) \tag{2.3}$$

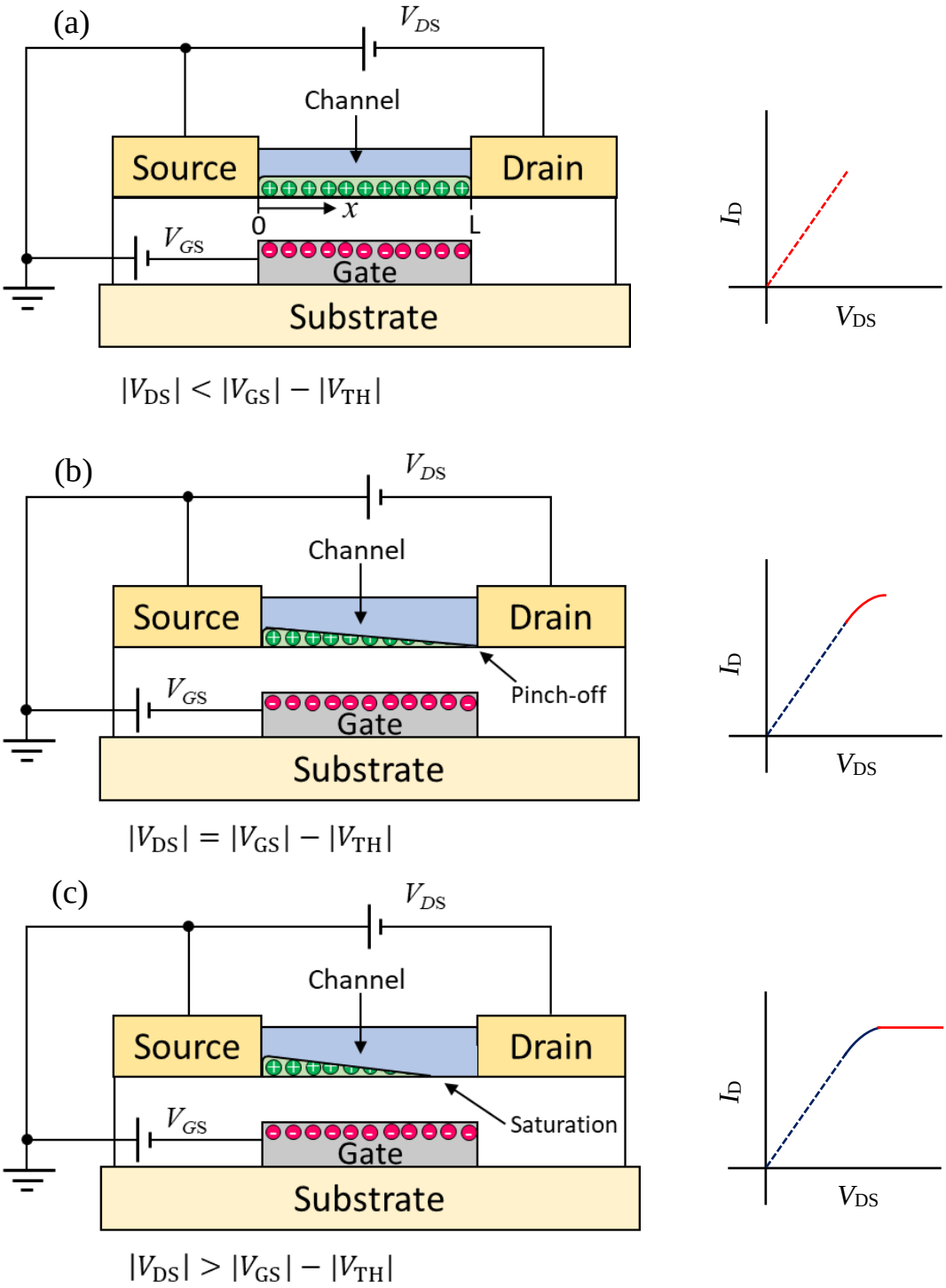

Figure 2.3: OTFT channel formation. Linear regime ($|V_{DS}| < |V_{GS}| - |V_{TH}|$) (a), pinch-off ($|V_{DS}| = |V_{GS}| - |V_{TH}|$) (b), and saturation regime ($|V_{DS}| > |V_{GS}| - |V_{TH}|$) (c).

2.2.1 Linear regime ($|V_{DS}| < |V_{GS}| - |V_{TH}|$) and $|V_{GS}| > |V_{TH}|$

An OTFT is known to operate in one of three regimes (linear, saturation and subthreshold) based on the voltages applied on its terminals. The transistor operates in the linear regime, when $|V_{DS}| < |V_{GS}| - |V_{TH}|$ and $|V_{GS}| > |V_{TH}|$. Derivation of the drain current in the linear regime follows.

Point x positioned in the given channel (Figure 2.3(a)) with length L so that $0 \leq x \leq L$, has the potential $V(x)$. Therefore, the charge density $Q(x)$ at point x is expressed as:

$$Q(x) = C_{\text{diel}} [V_{GS} - V_{TH} - V(x)] \tag{2.4}$$

Using Equation (2.5), the drain current (I_D) is given as the product of current density (J) and cross-sectional area (A). At the same time, the current density J is proportional to the product of the electrical conductivity (σ) and electric field ($E(x)$) given by Equations (2.5) – (2.7) respectively. Substituting Equations (2.6) and (2.7) into (2.5) leads to (2.8). Considering only the magnitude:

$$J = \sigma E = \frac{I_D}{A} \tag{2.5}$$

$$\sigma = qp\mu \tag{2.6}$$

$$E(x) = -\frac{dV(x)}{dx} \tag{2.7}$$

$$J = qp\mu \frac{dV(x)}{dx} \tag{2.8}$$

Here q is 1.602 x10^{-19} C, p is the hole carrier density and μ is the hole mobility. I_D = $J \cdot A$, where the cross-sectional area A is a product of channel width (W) and channel thickness (t_c). Therefore substituting Equation (2.8) into (2.5) and taking $A = W \cdot t_c$ and $q \cdot p = Q/t_c$, where Q is given by Equation (2.4), gives I_D as:

$$I_D = \mu W C_{\text{diel}}[V_{GS} - V_{TH} - V(x)]\frac{dV(x)}{dx} \tag{2.9}$$

Integrating I_D over the length of the channel in terms of voltages from source ($x = 0 \therefore V(0) = 0$) to drain ($x = L \therefore V(L) = V_{DS}$) for a constant current gives:

$$\int_0^L I_D\, dx = \mu W C_{\text{diel}} \int_0^{V_{DS}} [V_{GS} - V_{TH} - V(x)]\, dV(x) \tag{2.10}$$

$$I_D = \mu C_{\text{diel}} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right] \tag{2.11}$$

Very small values of V_{DS} in the linear regime, i.e. $|V_{DS}| < |V_{GS}| - |V_{TH}|$, implies that (2.11) can be simplified to (2.12) since the last term $\frac{{V_{DS}}^2}{2}$ is negligible:

$$I_D = \mu C_{\text{diel}} \frac{W}{L}(V_{GS} - V_{TH})V_{DS} \tag{2.12}$$

Equation (2.12) shows a linear increase in I_D with V_{DS}. $V_{GS} - V_{TH}$, known as the overdrive voltage, also affects I_D.

2.2.2 Saturation regime $(|V_{DS}| \geq |V_{GS}| - |V_{TH}|)$ and $|V_{GS}| > |V_{TH}|$

The saturation operation of an OTFT is realised when $|V_{DS}| \geq |V_{GS}| - |V_{TH}|$ and $|V_{GS}| > |V_{TH}|$. Setting $|V_{DS}| = |V_{GS}| - |V_{TH}|$, the voltage on the drain at point $x = L$ gives $V(L) = V_{DS}$. Thus, the effective potential on the drain channel side becomes $V_{GS} - V_{TH} - V_{DS}$, and since $|V_{DS}| = |V_{GS}| - |V_{TH}|$ the potential is effectively zero on the drain side. Yet the potential at the source side remains $V_{GS} - V_{TH}$. Therefore, the estimated Q at the drain end of the channel is zero (see Figure 2.3(b)) and is commonly referred to as pinch-off and marks the start of the saturation regime [2.29]. Substituting $|V_{DS}| = |V_{GS}| - |V_{TH}|$ into Equation (2.11) gives I_D in the saturation regime as (2.13) which simplifies to (2.14). Setting $|V_{DS}| > |V_{GS}| - |V_{TH}|$ results in a shift of the pinch-off point towards the source ($x < L$) with no further increase in I_D. I_D is said to be saturated and is independent of V_{DS}, as shown in Figure 2.3(c).

$$I_D = \mu C_{\text{diel}} \frac{W}{L} \left[(V_{GS} - V_{TH})(V_{GS} - V_{TH}) - \frac{(V_{GS} - V_{TH})^2}{2} \right] \tag{2.13}$$

$$I_D = \mu C_{\text{diel}} \frac{W}{2L} (V_{GS} - V_{TH})^2 \tag{2.14}$$

2.2.3 Subthreshold regime $(|V_{GS}| < |V_{TH}|)$

The drain current in a transistor is known to exist even for $|V_{GS}| < |V_{TH}|$. This regime of operation below the threshold region is known as the subthreshold regime and is characterised by the so-called subthreshold slope (S). The current in this region of operation is orders of magnitude less than the maximum drain current when $|V_{GS}| >$

$|V_{TH}|$ and increases exponentially with V_{GS}. Therefore, the subthreshold slope is particularly important in device characterisation where switching speed during transitions between on- and off-states are essential.

2.3 OTFT Parameters

Organic thin-film transistors use various parameters to evaluate their performance. These parameters are highly sensitive to a number of factors including device fabrication procedures, transistor structure, selection of materials and layer thicknesses, and are determined from current-voltage (I-V) measurements, namely the transistor output and transfer characteristics.

The field-effect mobility (μ) is considered one of the most significant OTFT parameters. The field-effect mobility is a measure of the average charge carrier drift velocity in the presence of applied electric field. In other words, it represents the movement efficiency of the accumulated charge carriers along the conduction channel. The field-effect mobility is a good method for evaluating the suitability of an OTFT for the required application.

The threshold voltage (V_{TH}) is described as the minimum V_{GS} required to satisfy the condition for the accumulation of charge carriers and the forming of a conduction channel. To ensure proper transistor operation, the threshold voltage needs to be controlled. Low threshold voltages are typically preferred for reducing power consumption and are desirable in low-voltage applications. Under prolonged application of gate bias, this parameter is known to experience a shift in the direction of the applied gate bias, a phenomenon known as threshold voltage shift. The transistor

behaviour becomes altered under such conditions. Additionally, the channel length and thicknesses of the semiconductor and dielectric can influence the threshold voltage.

When biased with voltage higher than the minimum voltage required for accumulation ($V_{GS} > V_{TH}$), an OTFT is said to operate in the on-state. The accumulation of mobile charge carriers leads to a drain current to flow from the drain to the source terminal. In this thesis, the maximum value of the drain current while the transistor operates in saturation is referred to as the on-state drain current (I_{ON}). Similarly, the minimum drain current while operating in the off-state ($V_{GS} < V_{TH}$) is referred as the off-state drain current (I_{OFF}). The ratio between the on-state and off-state currents is expressed as I_{ON}/I_{OFF}. High current ratio I_{ON}/I_{OFF} represent transistors with lower losses in the form of gate leakage current.

The gate leakage current is the unwanted current flowing from the channel through the dielectric into the gate. Ideally, the gate leakage current should be zero; however, values up to 1 nA can be observed. The gate leakage current has been shown to be controlled by the thickness of the dielectric and dielectric constant, annealing, overlap between the gate-source and gate-drain electrodes and gate/drain bias [2.30-2.32].

Transconductance (g_m) is another important transistor parameter. The transconductance describes transistor's efficiency relating the output to the input. It is defined as the ratio of change in the output I_D due to a change in the input V_{GS}.

When metals and semiconductors are joined together, the interface connecting the two materials is subjected to a 'resistance' generally termed as the contact resistance (R_c). The contact resistance is the result of the energy mismatch between the

metal work function (WF) and the HOMO of the organic semiconductor at their interface, leading to a potential barrier known as a Schottky barrier [2.33, 2.34]. In organic transistors, R_c exists at the metal-semiconductor interface between the organic semiconductor and the source/drain contacts. Therefore, the ease of charge carrier transfer across the metal/organic semiconductor interface determines the contact resistance. Minimizing the contact resistance is particularly important when the channel resistance (R_{ch}) is small. R_{ch} is the resistance along the semiconductor region where the conduction channel is formed. Since an OTFT's total resistance is a sum of its contact and channel resistances (R_c and R_{ch}, where R_{ch} is proportional to the channel length), the contact resistance becomes dominant in short channel transistors where $R_c >> R_{ch}$, thus limiting I_D, μ and cut-off frequency.

Neglecting large R_C or inaccurate measurements can lead to false extraction of transistor parameters and inefficient performance. As a result, several methods exist for lowering the contact resistance by tuning the interface and lowering the Schottky barrier. Proper selection of electrode material, self-assembled monolayers, inter-layers, and doping techniques are effective methods for controlling the contact resistance [2.34]. In this thesis the Femi level of Au (source/drain electrodes) aligns with the HOMO energy level of p-type DNTT organic semiconductor to minimise contact resistance.

2.4 Towards integration in analogue circuits

Advancement of the OTFT performance can take various forms depending on the desired functionality. However, regardless of the functionality, repeatable and

reversible responses are required. Additionally, mechanical flexibility, large on-state drain current, low-voltage operation, and sufficient voltage gain are among properties desired for flexible or wearable analogue circuits and/or sensor applications. This section explores the current state-of-the-art of OTFTs (some of which have been employed in this research) with the aim to address some of their limitations in relation to flexible analogue sensors applications. It also presents notable applications of such OTFTs in novel analogue circuits.

2.4.1 OTFT performance improvement

The use of organic transistors in analogue circuits is rapidly gaining popularity, yet the challenges they often present limit their rapid progression. Low field-effect mobility combined with electrical and environmental instabilities, or challenging device uniformity and impurities introduced during fabrication processes have remained the common problem areas. Many recent advances in OTFTs have led to significant improvement in their performance. Today, OTFTs are comparable, or in some cases outmatch, amorphous silicon technology. Field-effect mobility beyond 40 cm^2/Vs has been reported in [2.35] and an ultralow leakage current below 10^{-17} A/μm was demonstrated in [2.36]. MHz operation, high on-currents and low-voltage operation have also been presented in [2.37-2.40].

Most developments follow the optimisation of the gate dielectric for enhanced performance and low-voltage operation. The gate dielectric controls various parameters such as C_{diel}, I_D, I_G, μ, V_{GS}, V_{TH}, and also the interfacial defects and surface roughness that affect device stability. State-of-the-art OTFTs employ various

strategies for combating such limitations and improving transistor performance. A number of advances have been attributed to the optimisation of the gate dielectric, yielding high capacitance.

Following the charge density equation $Q = CV$ (corresponding to $Q = C_{diel}(V_{GS} - V_{TH})$ in the transistor), increasing Q while keeping $(V_{GS} - V_{TH})$ small for low voltage applications in wearable battery-powered electronics can be realised through the dielectric capacitance C. High relative permittivity (high-k) leads to high capacitance of the gate dielectric $(C_{\mathrm{diel}} = \varepsilon_r \cdot \varepsilon_0/d)$, crucial for increasing the drain current and the transconductance. Reduction in V_{TH}, improved field-effect mobility, and reduction in the gate leakage current were also demonstrated, such improvements resulting from the appropriate choice of dielectric material, its thickness and/or the use of dielectric multilayers or self-assembled monolayers (SAM).

Among high-k dielectric materials Al_2O_3, Ta_2O_5, HfO_2, BaZrTiO3 [2.39-2.41] yield high charge carrier mobility. These high-k oxides possess larger band gaps with fewer interface defects. They are compatible with organic semiconductors and lead to reduced gate leakage current, all while increasing the gate dielectric capacitance [2.41]. OTFTs with such dielectrics have been reported with 1 V operations [2.38] and in some cases dielectrics as thin as ~ 4 nm have been used [2.42]. Table 1 shows various high-k materials for low voltage, high capacitance OTFTs.

Table 1. Gate dielectrics for high OTFT capacitance [2.43, 2.44]

Inorganic material	***k constant***	**Organic material**	***k constant***
Al_2O_3	8 to 9	PMMA	3.9
Ta_2O_5	20 to 27	PVC	4.6
TiO_x	40	PS	2.6
TiO_2	80	PI	2.6
HfO_2	25	PVA	7.8
$BaZrTiO_3$	17	PVP	
ZrO_2	25		
a-$LaAlO_3$	30		
CeO_2	20		
P(VDF-TrFE-CFE)	60		

Increased dielectric capacitance, reduced gate leakage current and low voltage operation can be further enhanced by reducing the dielectric thickness, or with the aid of SAMs. SAMs are molecular nanoscale surface treatments that control the surface properties by converting arrangements of disordered molecules into functional organised complex structures without external input [2.45-2.47]. Titanium oxide (TiO_x) treated with phosphonic acid SAM; TiO_x/SAM, produced near zero V_{TH} = −0.09 V and high μ of 1.2 cm^2/Vs when operated at 1 V [2.48]. AlO_x modified with octadecyl phosphonic acid $AlO_x/C_{18}PA$ also showed low-voltage operation with V_{TH} = –0.33 V, μ of ~0.3 cm^2/Vs, and I_G and I_{OFF} of ~ 10^{-10} A and 10^{-11} A respectively [2.23]. Further advancement in AlO_x functionalisation (AlO_x/SAM) has demonstrated 1 V operation in ring oscillators [2.49]. Aghamohammadi *et al*. [2.50] investigated the dependence of dielectric thickness and the use of alkyl or fluoroalkyl SAMs on the

threshold voltage in DNTT transistors. Al_2O_3 with thickness from 5 nm to 200 nm was functionalised with SAMs of alkyl or fluoroalkyl octadecyl phosphonic acid. Results showed the threshold voltage to be dependent on gate dielectric capacitance only when fluoroalkyl SAMs are used, in which a linear but inverse dependence on the gate dielectric capacitance ($V_{TH} \propto 1/C_{diel}$) was observed. The threshold voltage in transistors with alkyl octadecyl phosphonic acid did not depend on gate dielectric capacitance. The dipoles introduced by various SAMs on the surface of the dielectric played a role.

Interdigitated electrodes with 'multi-finger' geometry significantly increase the *W/L* ratio through a reduction in the *L* and/or increase in *W* and are also a viable method to enhance transistor drain current while maintaining small transistor size. The channel geometry that determines *W/L* controls the drain current and the transconductance ($W/L \propto I_D$ and g_m) as inferred from Equations (2.12) and (3.7). Therefore, the physical manipulation of the channel area that increases *W/L* ratio could be used to enhance I_D, g_m and in turn the voltage gain. In [2.51], an increase in the number of interdigitated source-drain 'fingers' from 0 to 4 led to an increase in I_D, enhanced μ and reduction in both I_G and total contact resistance, improved carrier transport and increased lateral electric field along the channel towards the drain. Results presented in the subsequent Chapters of this thesis also focused on analysing transistor performance as a function of various geometries of interdigitated source/drain contact, demonstrating drain current as high as 126 μA, g_m ~ 60 μS and voltage gains between ~4.9 and ~8.4 V/V using L = 20 to 50 μm and W = 18.23 mm.

The presence of hysteresis in organic transistors is another obstacle in their wider implementation. Hysteresis is known to exist in the presence of humidity, oxygen, or any contamination/defects at the dielectric/semiconductor interface, particularly in devices with hydrophilic dielectric [2.52]. The hysteresis has been observed in more than 90% of published research, making it a major problem in organic transistors. The hysteresis depends on interfacial trap density, molecular structure, surface energy, charge transport, etc [2.51-2.56]. The transistors with negligible or hysteresis-free behaviour include the superhydrophobic dielectric materials such as C_{18}PA and hexamethyldisilazane [2.23, 2.26-2.58]. Annealing the dielectric before the deposition of the semiconductor also eliminated the hysteresis [2.52, 2.59].

In this thesis, dielectric bi-layer of AlO_x treated with octadecyl phosphonic acid (C_{18}PA) SAM with total thicknesses of ~ 17 nm (to minimise gate leakage current), combined with DNTT organic semiconductor and the use of interdigitated source/drain contacts is investigated. Octadecyl phosphonic acid has led to hysteresis-free behaviour and has shown to improve the environmental stability of transistors due to hydrophobic properties of C_{18}PA resulting from its mesoporous nature (materials with pores diameter between 2 and 50 nm) and thermal stability [2.56-2.58]. Excellent thermal stability of AlOx/octadecyl phosphonic acid bilayer was reported in [2.60]. The capacitance did not change during annealing up to 150°C for 30 mins and slight degradation after 30 mins at 160°C was observed. DNTT is also credited with long-term environmental stability in the presence of ambient light and air, high charge carrier mobility, and small contact resistance compared to other materials like pentacene [2.61-2.63].

2.4.2 Analogue circuit applications

Analogue circuits and sensors are increasingly integrating OTFTs into their designs. OTFTs can operate in transducer circuits converting physical/chemical stimuli into electrical signals, and/or in amplifier circuits to boost weak signals and enhance sensitivity. This is no different from the traditional use of silicon transistors; the OTFTs however can offer desirable form factors and mechanical flexibility via the use of plastic substrates.

In [2.64], a suspended-gate OTFT (SGOTFT) as a pressure sensing device was reported. In the proposed device the gate of the OTFT was suspended, i.e. an air gap was created with the help of flexible laminated support layer that deformed when subjected to pressure. Ultra-low capacitance of 0.01 nF/cm^2 and drain current less than 10^{-8} A were measured for the unloaded OTFT, and mobility of 0.34 cm^2/Vs and I_{ON}/I_{OFF} of 10^4 A were achieved under a constant pressure of 1 kPa. The device exhibited maximum sensitivity >190 kPa^{-1} at V_{DS} = −60 V and responded to pressure as low as 3 Pa (~0.23 kPa^{-1}) at V_{GS} of 6 V when implemented in a battery-powered wrist-attached pulse measurement device. An 8x8 tactile pressure sensing array was also demonstrated.

OTFT-based e-skin for robotic arms implementing tactile sensing was also reported [2.65-2.67]. The ultra-thin resistive tactile sensor was ultra-light, weighing only 3 g/m^2. The OTFT active-matrix array was fabricated on a 1-µm-thick polyethylene naphthalate (PEN) foil with aluminium electrodes, DNTT as the organic active layer, and dielectric bi-layer composed of anodic aluminium oxide and phosphonic acid self-assembled monolayer.

Successful implementation of a multifunctional sensor based on organic field-effect transistor was recently reported in [2.68]. A 2.5-μm-thick ferroelectric poly(vinylidene fluoride trifluoroethylene) (P(VDF-TrFE)) capacitor was connected to the gate of DNTT OTFT to take advantage of the piezoelectric (force stimulus) and pyroelectric (temperature stimulus) properties of P(VDF-TrFE). The transistors with μ as high as 0.56 cm^2/Vs and V_{TH} between −0.19 and −0.68 V functioned as transducers for converting the stimuli into useful voltage signals. A sensitivity of ~ 65 mV/N and ~ 3.9 mV/N were observed for applied forces of less than 0.1 N and between 0.1 and 1 N, respectively. The response to temperature was linear, the sensitivity varied from 3.8 mV/°C to 17.2 mV/°C for temperatures from 20 to 25°C, depending on the OTFT parameters.

[2.69] demonstrated the detection of highly toxic putrescine (PUT) vapour in air using OTFT based on diketopyrrolopyrrole–thiophene polymer (PDQT). The response as a function of the concentration of PUT vapour was characterised with a real-time measurement of transistor current versus time at $V_{GS} = V_{DS} = -100$ V. After exposure to PUT vapour for 10 s (using concentrations from 0 to 100 ppb) the devices displayed a reduction in OTFT drain current within average response time of 2 s. Recovery to 80% of the original current was observed 30 minutes after the exposure was stopped. Exposure to PUT also led to a significant reduction in field-effect mobility over the course of 8 weeks.

2.5 Summary

The discovery of organic semiconductors has paved the way for organic transistors. Although still riddled with challenges in their electrical performance, fabrication reproducibility, and electrical and environmental instabilities, significant progress has been made to date that will lay the foundation for the wide-spread use of organic transistors in the foreseeable future. In this chapter, a range of such improvements relating to the research presented in this thesis have been introduced and discussed.

The research presented in the following chapters builds on prior advancements and focuses on the implementation of organic transistors into analogue sensors. The OTFTs are fabricated on plastic substrates and are optimised for low-voltage operation and high on-state drain current, achieved through the judicious choice of materials, transistor structure, and manipulation of the channel geometry. An unconventional approach to study the bias stress instability in such transistors is then developed. Finally, the voltage-amplifying ability of the transistors is demonstrated through a temperature sensor.

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Chapter 3

Methodology

This chapter introduces the fabrication process of low-voltage, high transconductance organic thin-film transistors and associated MIM structures on PEN substrate. Furthermore, it describes the OTFT operation, characterisation and measurement techniques used to evaluate the electrical performance and elaborates on the development of temperature sensors based on such OTFTs. A brief overview of the MIM structures and complete vacuum-evaporated OTFT fabrication process is described in Section 3.1. Section 3.2 describes the measurement process of MIM structures and OTFT. Section 3.3 discusses the transistor parameter extraction techniques. Section 3.4 describes the measurement procedures for investigating the instability of organic transistors under a pulsed bias stress. Section 3.5 and 3.6 details the construction and measurement of OTFT-based temperature sensor, respectively. Finally, Section 3.7 summarizes the Chapter.

3.1 Fabrication on PEN: MIM and OTFT structures

A typical OTFT consist of three electrodes for gate, drain and source, a gate dielectric, and an organic semiconductor, all layered on a substrate. The MIM structures and OTFT fabrication process are identical except the organic semiconductor layer is excluded in the MIM structure. The MIM structure can be described as two parallel layers of metal separated by a layer of dielectric and is necessary for determining the gate dielectric capacitance and in turn the transistor performance. OTFTs and MIM structures are fabricated side-by-side on the same PEN substrate and the dielectric layer of the MIM structure is identical to the gate dielectric within the transistor.

The MIM structure and OTFT cross-sections and fabrication stages are shown in Figure 3.1 and 3.2 respectively. MIM and OTFTs are fabricated on polyethylene naphthalate (PEN) (Optfine PQA1, DuPont Teijin) substrate. Dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) acts as the organic semiconductor. The gate is made of aluminium (Al) and drain/source electrode are made of gold (Au). The thin gate dielectric bi-layer consists of aluminium oxide (AlO_x) and octadecyl phosphonic acid ($C_{18}PA$). Fabrication took place inside a cleanroom with yellow lighting. Except for the aluminium oxide formation, all layers were deposited by thermal evaporation in a Mini-Spectros (Kurt J. Lesker, UK) vacuum system enclosed in a nitrogen filled glovebox (Jacomex, France) to reduce contamination, moisture, and oxidation. The Mini-Spectros vacuum chamber had base pressure of ~ 10^{-7} mbar and the glove box had O_2 and H_2O content of ~ 1 and ~ 0.3 particle per million (ppm) respectively. The thermal evaporations were controlled via Mini-Spectros software. The software comes

equipped with customisable recipes for various metals and organic materials and real-time control for managing the substrate temperature, substrate rotation, position of various shutters, deposition rates, and layer thicknesses.

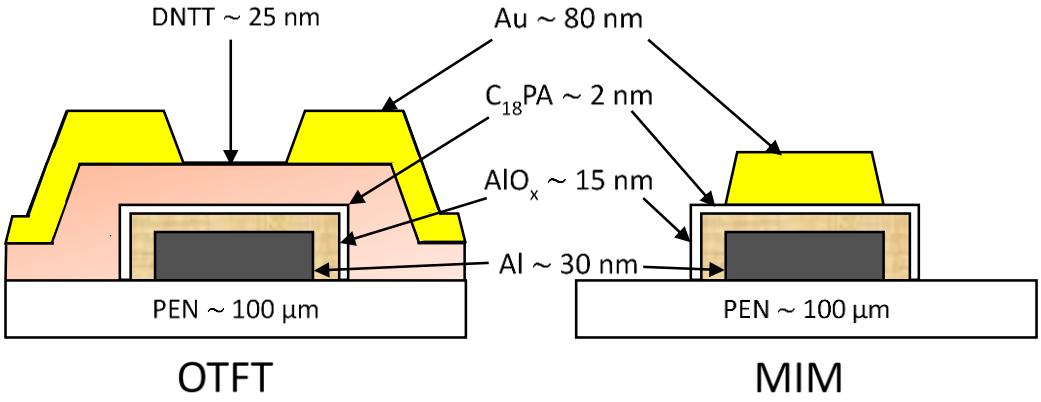

Figure 3.1: OTFT and MIM structure cross-sectional view.

Tungsten boats/crucibles were used for the evaporation of metals, while 1-cm^3 alumina crucibles were used for organic materials. To achieve Al or Au evaporation, the source metals had to be melted. Contrary to that, the organic materials were sublimed at much lower temperatures, typically around 200 ºC. A mechanical shutter

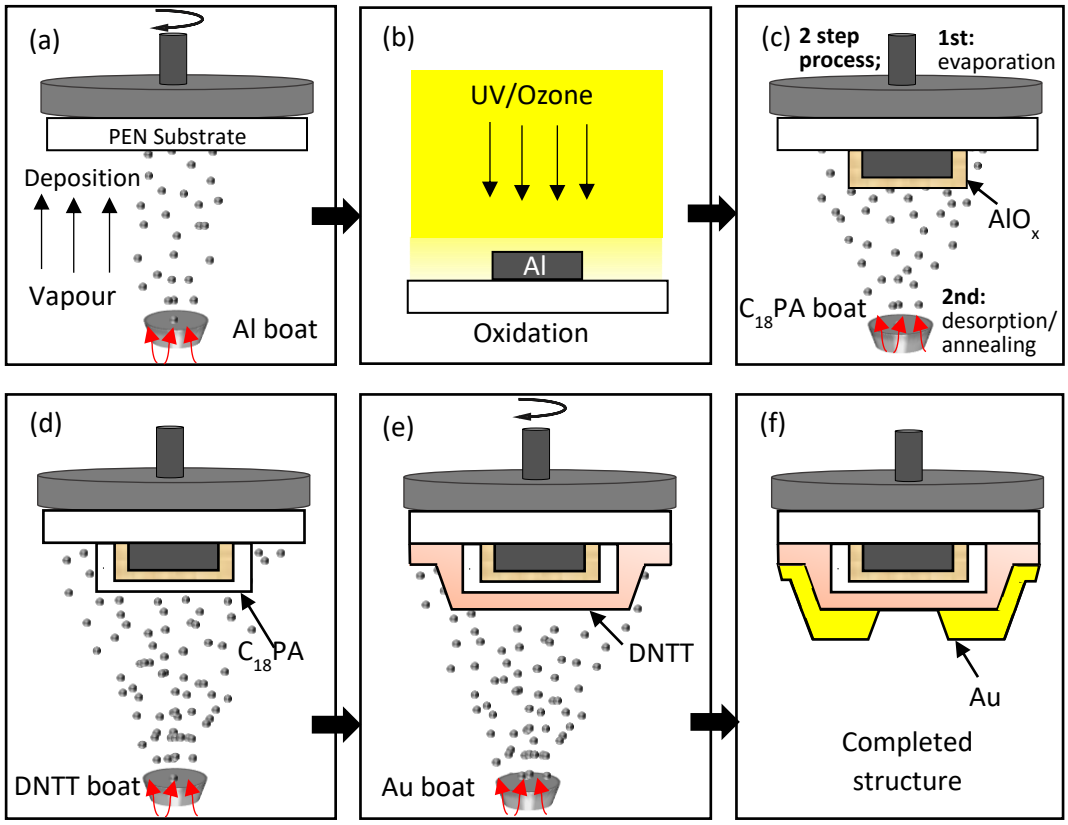

Figure 3.2: Flow diagram of MIM structure and OTFT fabrication stages. Note, DNTT (stage d) is omitted during MIM structure fabrication.

and a thickness monitor positioned above each source material controlled the evaporation rate and the deposited thickness. Simultaneously, substrate rotation was used to create uniform metal coatings. All thermal evaporations were performed at room temperature, making it suitable for plastic substrates. The only high-temperature step during the fabrication is the C_{18}PA desorption to create a monolayer. In this case the substrates were heated to 160 ºC for 2.5 hours. Subsequent deposition of each new layer of material was formed using alignment of steel shadow masks over the previous layers. The quality of stencil mask, pattern, size, and edge roughness are critical for the device performance. Consequently, steel stencil masks were selected for this study for their stiffness and mechanical stability.

The aluminium oxide (AlO_x) layer results from the oxidation of aluminium when exposed to ozone. The oxidation was performed in an ultraviolet (UV)/ozone cleaner (UVOCS, USA) enclosed under a Hepa filter. Wavelengths of ~185 and ~ 254 nm emitted from the mercury lamp led to the generation of ozone and formation of the aluminium oxide (AlO_x) on the surface of aluminium gate electrodes.

Fabrication begins with cleansing of the 100-µm-thick PEN substrates. The substrates are placed in a hot, soapy DI water and sonicated in an ultrasonic bath for 1 hour. Afterwards they are 'rinsed' by sonication in a hot, clean DI water and dried with a nitrogen gun. The gate electrodes are made of a 5-nm-thick chromium (Cr) serving as an adhesion layer to PEN and a 30-nm-thick Al deposited at a rate of ~ 2 Å/s. Sections of the gate electrodes were then coated with 40-nm-thick Au layer to prevent their oxidation during UV/ozone exposure and to allow measurement of the completed transistors by forming a metal contact to the gate.

The aluminium oxide (AlO_x) layer was then prepared by exposing the surface of the Al gate electrode to UV/ozone in ambient atmosphere for 60 minutes, oxidising the surface of the Al producing AlO_x. The thickness of the formed AlO_x depends on the intensity of the UV light and the exposure time. 60 minutes of exposure forms ~ 7-nm-thick AlO_x layer. Experimentation has shown that thicker AlO_x layer > 10 nm is needed to supress the gate dielectric leakage current. Instead of using long oxidation times of up to 10 hours, a 15 Å-thick-layer of Al is evaporated on top of AlO_x and exposed to UV/ozone. Consequently, the desired oxide thickness is achieved by using 1 to 3 thin Al coats and subsequent exposure to UV/ozone. [3.1] The aluminium oxide (~ 15 nm thickness) forms the bottom layer of the gate dielectric bi-layer.

Next, ~ 9 monolayers of octadecyl phosphonic acid ($C_{18}PA$) were thermally evaporated at a rate of 3 Å/s at room temperature, resulting in a 20-nm-thick $C_{18}PA$. The substrate temperature was then raised to 160 °C for 2.5 hours to remove all physisorbed $C_{18}PA$ molecules and to anneal the formed monolayer. The annealing process completes the gate dielectric $AlO_x/C_{18}PA$ bi-layer. The typical total bi-layer thickness was 17 nm and consisted of ~15 nm of AlO_x and ~2 nm of $C_{18}PA$.

The final stages of the OTFT fabrication involve the deposition of the organic semiconductor and the deposition of drain and source electrodes. The process begins with the thermal evaporation of a 25-nm-thick DNTT (Sigma Aldrich, U.K) at the rate of 0.5 Å/s over the gate dielectric bi-layer at room temperature. During DNTT evaporation, the MIM structures were fully masked to omit deposition. Finally, 80-nm-thick gold (Au) was thermally evaporated at the rate of 3 Å/s to form the drain and source contacts and complete OTFTs and MIM structures. Table 2 compares the fabrication properties of MIM structures and OTFTs.

Based on the prior research at University of Strathclyde, materials, evaporation rates, oxidation time and thicknesses of Table 1 were chosen for high performance OTFTs with good electrical and environmental stability, low-voltage operation, and hysteresis-free characteristics [3.2, 3.3].

3.2 Measurement: MIM structures

All MIM measurements were performed with an Agilent B1500A semiconductor device parameter analyser (Keysight Technologies) running EasyEXPERT characterisation software. Connections to the MIM structure were made

Table 2. Comparison of MIM structure and OTFT fabrication properties.

MIM structure	OTFT	Material layer	Evaporation rate (Å/s)	Thickness (nm)	UV/Ozone oxidation (mins)
✓	✓	PEN	N/A	100,000	N/A
✓	✓	Al	2	30	N/A
✓	✓	AlO_x	N/A	15	60
✓	✓	$C_{18}PA$	3	2	N/A
N/A	✓	DNTT	0.5	25	N/A
✓	✓	Au	3	80	N/A

using a Signatone probe station coupled to the B1500A unit. Figure 3.3 shows the equipment setup used for measurements of the MIM structures. The Agilent EasyEXPERT software facilitates multiple measurements and analysis including capacitance-frequency (C-f), capacitance-voltage (C-V) and current-voltage (I-V) measurements. The MIM structures were evaluated using the C-f tool described in Sections 3.2.1 and 3.2.2 while Section 3.2.3 describes the process of calculating the thickness of the $C_{18}PA$ layer.

3.2.1 Capacitance of MIM structures

The capacitance (C) was obtained by applying a 100 mV peak-to-peak sinusoidal voltage and sweeping the frequency (f) from 1 kHz to 1 MHz. An example of the capacitance measurement as a function of frequency is illustrated in Figure 3.4. For this study C is extracted at f = 10 kHz on the C-f response curve.

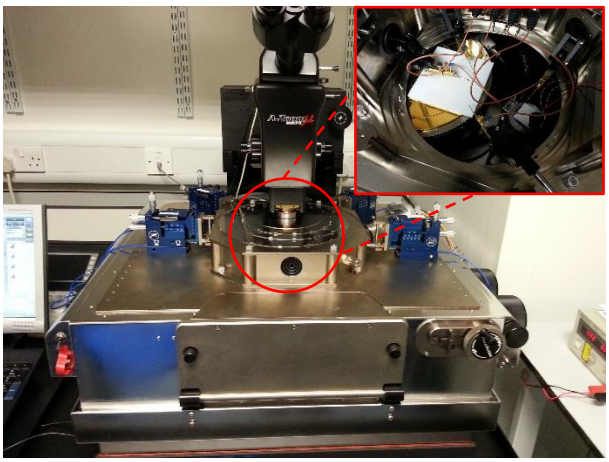

Figure 3.3: Agilent B1500A and probe station for device characterisation.

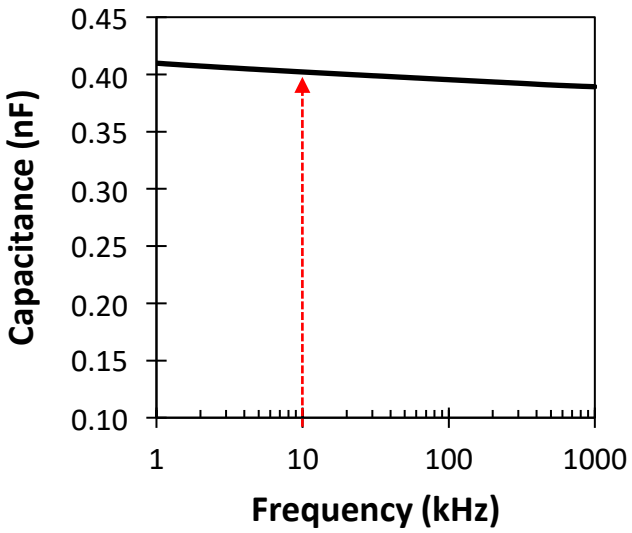

Figure 3.4: MIM capacitance as a function of AC frequency.

3.2.2 Gate dielectric capacitance per unit area

The capacitance of $AlO_x/C_{18}PA$ gate dielectric (C_{diel}) can be modelled as two capacitors in series, as shown in Figure 3.5. The same is true for the capacitance per unit area which is the quantity desired for the transistor evaluation. Consequently, the mean dielectric capacitance per unit area is calculated by measuring capacitance (at 10

kHz) of various MIM structures and dividing it by their respective area. The gate dielectric capacitance is expressed in Equation 3.1, where *n* is the total number of MIM structures, and *A* is the $AlO_x/C_{18}PA$ capacitor area.

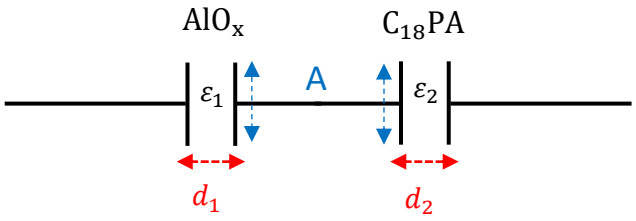

Figure 3.5: Gate dielectric bi-layer, where *A* is the contact area (identical for AlO_x and $C_{18}PA$), $\boldsymbol{\varepsilon_1}$, $\boldsymbol{\varepsilon_2}$ and $\boldsymbol{d_1}$, $\boldsymbol{d_2}$ are the permittivity and thicknesses of AlO_x and $C_{18}PA$ respectively.

$$C_{diel} = \frac{\sum_{i=1}^{n}\left(\frac{C_i}{A_i}\right)}{n} \tag{3.1}$$

During the transistor fabrication process, two types of MIM structures and transistors were prepared. Some contained bi-layer of $AlO_x/C_{18}PA$, while the others contained only AlO_x. If C_{AlOx} is the capacitance of the AlO_x layer and C_{diel} the capacitance of the $AlO_x/C_{18}PA$ bi-layer, then the capacitance of the phosphonic acid monolayer C_{C18PA} can be calculated from the Equation 3.2.

$$\frac{1}{C_{diel}} = \frac{1}{C_{AlOx}} + \frac{1}{C_{C18PA}} \tag{3.2}$$

3.2.3 AlO_x and $C_{18}PA$ thicknesses

The thickness of AlO_x can be calculated from the measured C_{AlOx} using the relative permittivity of ~6.8 [3.4]. C_{C18PA} is obtained from C_{AlOx} and C_{diel} using

Equation (3.2). The thickness of $C_{18}PA$ was calculated from C_{C18PA} using Equation 3.3, where d_2 and ε_2 are the thickness and permittivity of $C_{18}PA$ respectively. $C_{18}PA$ has relative and free space permittivity of ~2.1 [3.5] and 8.85 x 10^{-12} F/m respectively.

$$d_2 = \frac{\varepsilon_2}{C_{C_{18}PA}} \tag{3.3}$$

3.3 Measurement: OTFT

As with the MIM structures, connections to and measurements of the OTFT were carried out with Agilent B1500A semiconductor device parameter analyser and Signatone probe station. The measurement was setup under dark ambient environment to measure the OTFT transfer and output characteristics and subsequent extraction of OTFT parameters described in Sections 3.3.1 and 3.3.2. The OTFT hysteresis behaviour is introduced in Section 3.3.3 and Section 3.3.4 explains the determination of the OTFT AC transconductance.

3.3.1 Transfer characteristics

The OTFT's transfer characteristics show the behaviour of the drain current (I_D) and the gate leakage current (I_G) as a function of the gate-to-source voltage (V_{GS}) swept from 0 to −2 V. The fixed drain-to-source voltage (V_{DS}) corresponds to the OTFT's operation in the linear (V_{DS} = −0.1 V) and saturation (V_{DS} = −2 V) regimes. Note that negative voltages are required for the p-type transistors. Figure 3.6 shows typical OTFT transfer characteristics. The transfer characteristics are necessary for extracting OTFT parameters including the threshold voltage (V_{TH}), field-effect

mobility (μ), subthreshold slope (S), on-state drain current (I_{ON}), off-state drain current (I_{OFF}) and current ratio (I_{ON}/I_{OFF}). OTFT parameters are extracted from both linear and saturation regimes, however, for this study only parameters in saturation regime are used. The linear regime is used for verification purposes since the linear and saturation regime only differ by approx. ±10 %. All parameter are determined using MATLAB programming software.

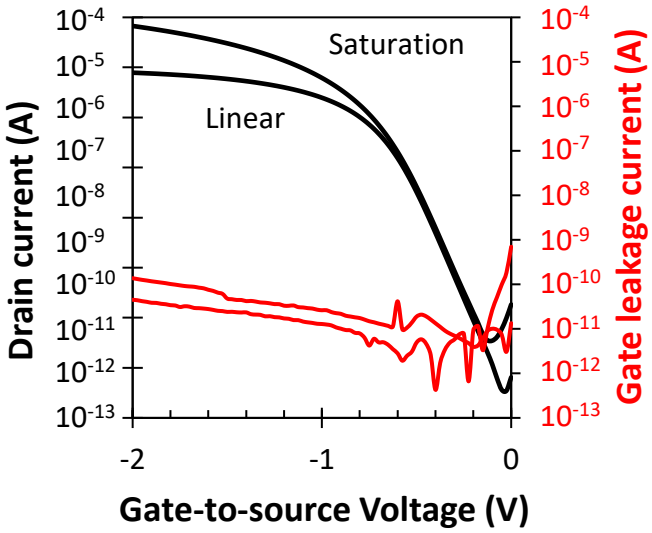

Figure 3.6: Transfer characteristics in linear (V_{DS} = −0.1 V) and saturation regime (V_{DS} = −2 V) for V_{GS} sweep from 0 to −2 V.

3.3.1.1 Threshold voltage

The threshold voltage can be extracted from both the linear and saturation transfer characteristics. In the linear regime, the threshold voltage V_{TH} can be defined as the voltage on the x-axis at the point where a tangent line projecting from the point of steepest slope on the I_D vs. V_{GS} curve intercepts the x-axis. Figure 3.7 demonstrates the procedure. The same procedure is true for the saturation regime, however the $\sqrt{I_D}$

vs. V_{GS} curve is used. The point of steepest decent was found by the derivatives $\frac{\partial I_D}{\partial V_{GS}}$ and $\frac{\partial \sqrt{I_D}}{\partial V_{GS}}$ of the respective curve.

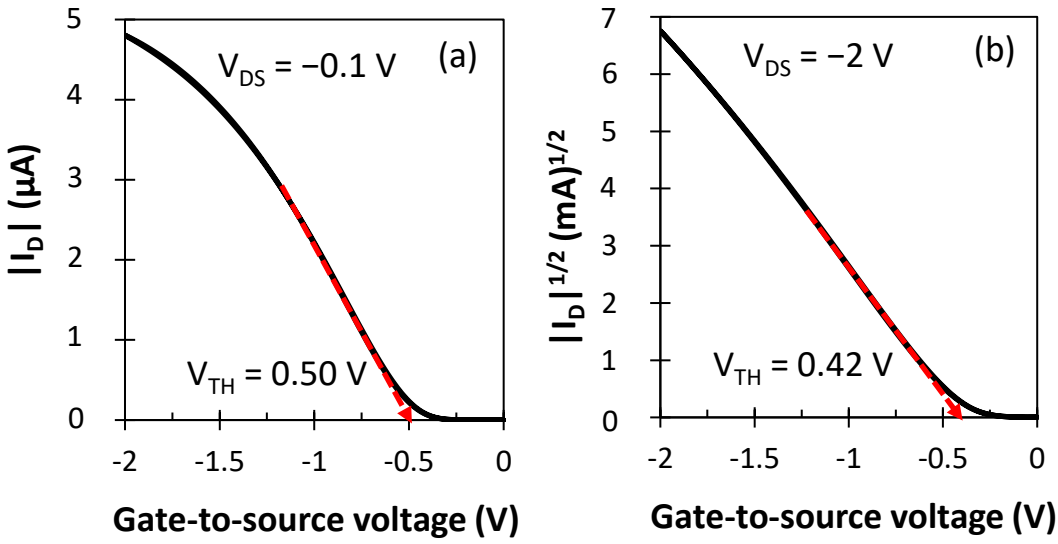

Figure 3.7: Threshold voltage extraction from slopes of $\boldsymbol{I_D}$ and $\sqrt{\boldsymbol{I_D}}$ as functions of $\boldsymbol{V_{GS}}$ in linear (V_{DS} = −0.1 V) (a) and saturation (V_{DS} = −2 V) (b) regimes.

3.3.1.2 Field-effect mobility

The linear and saturation field-effect mobilities μ_{lin} and μ_{sat} (cm^2/V·s) were determined by rearranging Equations 2.12 and 2.14 into Equations 3.4 and 3.5 respectively, where $\frac{\partial I_D}{\partial V_{GS}}$ and $\frac{\partial \sqrt{I_D}}{\partial V_{GS}}$ are the gradient of steepest decent extracted from the derivatives of I_D vs. V_{GS} and $\sqrt{I_D}$ vs. V_{GS} curves respectively. L and W represent the transistor channel length and channel width respectively. C_{diel} is the gate dielectric capacitance per unit area and V_{DS} is the drain-to-source voltage.

$$\mu_{lin} = \frac{L}{C_{diel}\, W\, V_{DS}} \left(\frac{\partial I_D}{\partial V_{GS}}\right) \tag{3.4}$$

$$\mu_{sat} = \frac{2\ L}{C_{diel}\ W}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2 \tag{3.5}$$

3.3.1.3 Subthreshold slope

The subthreshold slope S (mV/decade) is described as the inverse of the point of steepest slope on the transfer characteristics curve, where the behaviour of the drain current (in logarithmic scale) $log_{10}(|I_D|)$ is shown to rise exponentially as a function of the gate-to-source voltage V_{GS}. The region is referred to as the subthreshold region and is extracted from the saturation regime (V_{DS} = −2 V) by Equation 3.6. Figure 3.8 demonstrates the subthreshold slope extraction method.

$$S = \left[\frac{\partial(\log_{10}(|I_D|))}{\partial V_{GS}}\right]^{-1} \tag{3.6}$$

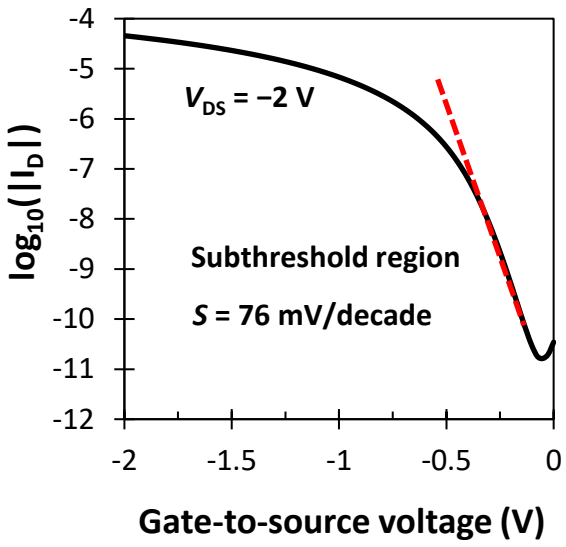

Figure 3.8: Subthreshold slope extraction from the subthreshold region.

3.3.1.4 On-state and off-state drain currents

The on-state drain current (I_{ON}) and off-state drain current (I_{OFF}) are defined as the maximum and minimum drain currents on the transfer characteristics curve when the transistor is in the on-state and off-state respectively. Typically, extractions are performed from the saturation regime (V_{DS} = −2 V). The current ratio I_{ON}/I_{OFF} is the ratio of the on-state drain current to off-state drain current and is found by the division of I_{ON} over I_{OFF}.

3.3.2 Output characteristics

The output characteristic is a plot of drain current (I_D) as a function of drain-to-source voltage (V_{DS}) at a fixed gate-to-source voltage (V_{GS}). Each output characteristic captures the behaviour of the drain current in both the linear and saturation regimes. At small V_{DS} i.e. ($|V_{DS}| < |V_{GS}| - |V_{TH}|$) the drain current shows a linear increase and for larger V_{DS} i.e. ($|V_{DS}| \geq |V_{GS}| - |V_{TH}|$) the drain current is at saturation. For $V_{DS} < V_{TH}$, the drain current is effectively zero. The output characteristic is essential for visualising the regime of operation with respect to V_{GS} and V_{DS}, i.e. it is crucial for determining suitable voltages for operation in the desired regime. Figure 3.9 shows typical output characteristics of the OTFTs used in this thesis, showing V_{DS} sweep (0 to −2 V) and V_{GS} step (−0.5 V to −2 V, −0.25 V increments). For the chosen low-voltage V_{GS} = −2 V (black curve), the output characteristic validates operation in the linear regime with V_{DS} = −0.1 V and operation in the saturation regime with V_{DS} = −2 V.

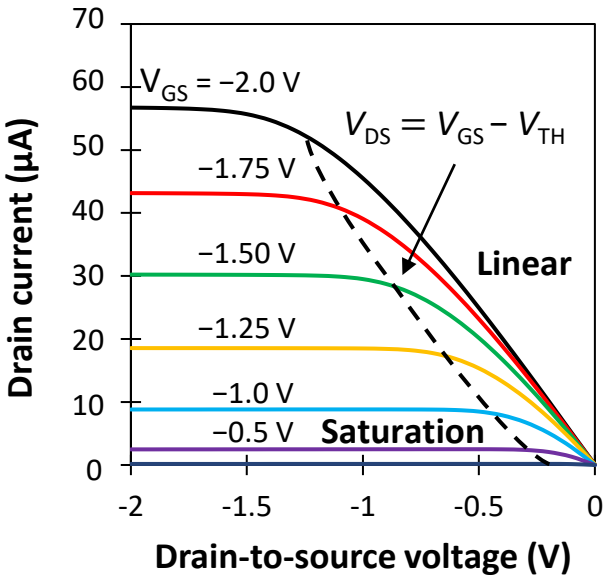

Figure 3.9: Output characteristics, plot of drain current as a function of drain-to-source voltage from 0 to −2 V and gate-to-source voltage at −0.25 V increments. Dashed line divides the linear and saturation regimes.

3.3.3 OTFT hysteresis

A transistor is said to have hysteresis when the drain current exhibits a delay during the reversed transition of the applied gate-to-source voltage. The hysteresis is measured by taking a forward (V_{GS} = 0 to −2 V) and reverse (V_{GS} = −2 to 0 V) sweep of the transfer characteristics. While a transistor with hysteresis displays different values of I_D during the forward and reversed measurements (the two curves are shifted), an ideal transistor with no hysteresis shows identical measurements as shown in Figure 3.10. All OTFTs presented in this thesis displayed hysteresis-free behaviour as a result of interface between environmentally stable DNTT and hydrophobic $C_{18}PA$ that suppresses moisture/humidity. Annealing of $AlO_x/C_{18}PA$ dielectric in vacuum was the last step in its preparation and annealing was reported to reduce surface roughness and remove moisture, thus minimising the hysteresis [2.51, 2.58, 2.59].

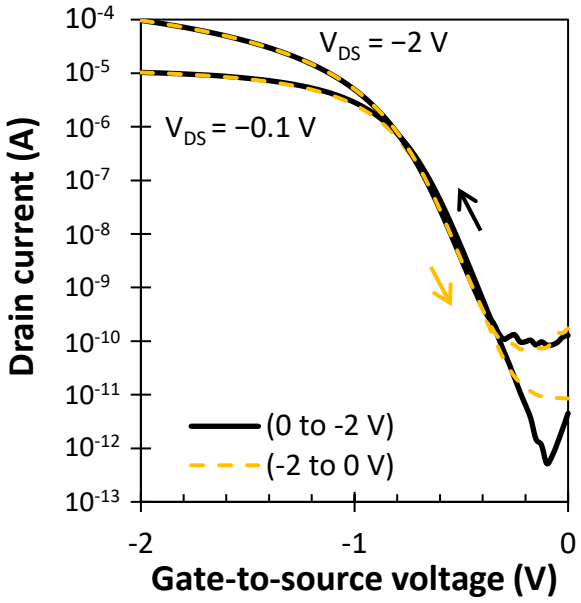

Figure 3.10: OTFT hysteresis measurement, forward (V_{GS} = 0 to −2 V) and reverse (V_{GS} −2 to 0 V) sweep (arrows show the direction of sweep) in linear (V_{DS} = −0.1 V) and saturation (V_{DS} = −2 V) regimes.

3.3.4 OTFT with high transconductance on PEN

The AC transconductance (g_m) refers to the ratio of change in the drain current with respect to changes in the gate-to-source voltage for a constant drain-to-source voltage. The AC transconductance measurement, described by Equation 3.7 and illustrated by Figure 3.11, was determined by, firstly applying a sinusoidal signal of 1 Hz generated from an arbitrary waveform generator at a magnitude of 0.2 V peak-to-peak to the transistor gate. The drain-to-source voltage and source voltage (V_S) are fixed at −2 V and 0 V respectively. Next, the sinusoidal drain current was measured using an Agilent B1500A semiconductor parameter analyser. Calculation of the AC transconductance was carried out using Equation 3.7, where i_d and v_{gs} are the peak-to-peak sinusoidal drain current and gate voltage at the drain and gate terminals of the transistor, respectively.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{i_{\mathrm{d}}}{v_{\mathrm{gs}}} = \frac{W}{L}\mu_{sat}C_{diel}(V_{GS} - V_{TH}) \tag{3.7}$$

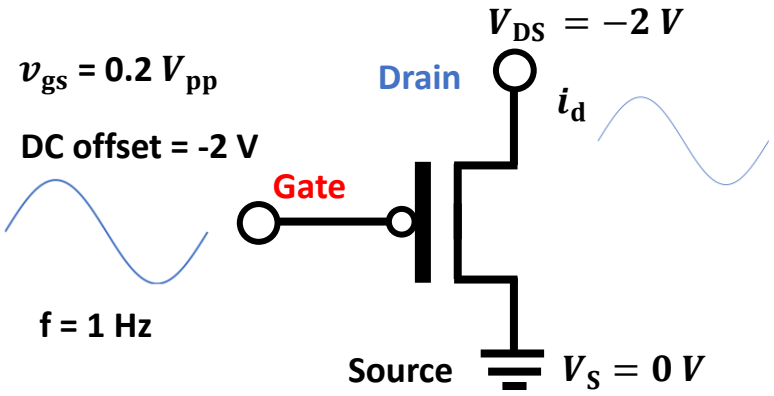

Figure 3.11: AC transconductance measurement setup.

The measurement was performed on a set of transistors with interdigitated source/drain contacts. Their channel length and width varied between 20 to 50 µm and 12 to 18.23 mm respectively.

3.3.5 Transistor channel dimension

The OTFTs used in this thesis employ the interdigitated source/drain contacts depicted in Figure 3.12. The transistor channel length (*L*) is defined as the gap distance between the drain and source electrodes in µm, while the transistor channel width (*W*) is the total length of the meandering channel between the drain and source electrodes in mm. Measurement of *L* and *W* were performed using a microscope with a camera attachment and a stage micrometer. The microscope/camera displayed the magnified transistor channel image on the computer screen so that the *L* and *W* can be measured. The stage micrometer (placed next to the transistor) was used for scale conversion.

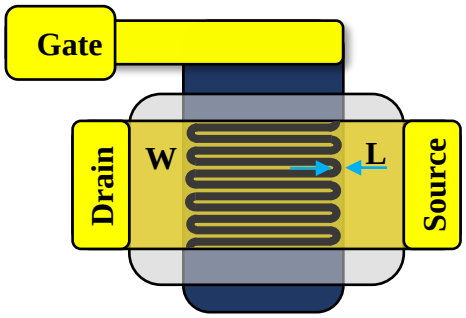

Figure 3.12: Top view of an organic thin-film transistor with interdigitated source/drain contacts.

3.4 Measurement: OTFT response to pulsed bias stress

Bias stress refers to the process of introducing stress to the transistor in the form of voltage on the gate and drain terminals for a prolonged period. It is well documented that under such conditions, transistors undergo charge trapping at the semiconductor/gate dielectric interface [3.6]. Consequently, the bias stress produces a threshold voltage shift in the direction of the applied voltage depending on the extent of continuous bias stressing.

This section presents the measurement procedure of a low voltage, high transconductance OTFT fabricated on flexible PEN foil. Contrary to previously documented pulsed bias stress studies where the degree of instability is measured through the application of short gate pulses varied by the duty cycle [3.7-3.9], this thesis focuses on square AC waveforms with long periods (T) between 5 and 60 s, i.e. fixed on-time of 1 s and varied off-time from 4 to 59 s. These were chosen to suit low sample rate sensor applications (< 1 Hz) that do not require continues monitoring and therefore benefit from reduced data volume while maintaining adequate and accurate

sensor information. A DC bias stress measurement was also performed on some transistors for reference.

The bias stress measurement procedure begins with an initial transfer characteristics measurement taken before stressing. Next, the device stability was evaluated by biasing the gate and drain terminals of eight transistors with four AC square waveforms and one DC bias (V_{GS} = V_{DS} = −2 V). Figure 3.13 depicts the bias stress setup. The source terminal was grounded (V_S = 0 V). Regardless of the pulse period *T*, each transistor was stressed with 1000 pulses. The DC measurement corresponds to ≈ 17 minutes of actual measurement time, while T = 60 s corresponds to ≈ 17 hours or 60,000 s of actual measurement time with 1000 s of net stress time. The bias stress was briefly interrupted after each 100 pulses to measure transfer characteristic in saturation. Measurements were performed on a set of transistors with similar V_{TH} ~ –0.5 V, I_{ON} ~5×10^5 A and channel width W ~ 18.23 mm. Pulse generation and bias stress measurements were performed with Agilent B1500A semiconductor device parameter analyser and semiconductor pulse generator unit (SPGU). Unipolar pulse generation was achieved through continuous switching between the ON (−2 V) and OFF states (0 V). Detailed pulse diagram can be found in Figure 5.1 of Chapter 5.

The time dependent changes in OTFT parameters for the normalised on-state drain current, threshold voltage shift and normalised field-effect mobility were fitted using stretched-exponential functions described by Equations 3.7, 3.8 and 3.9 respectively.

$$\frac{I_{ON}(t)}{I_{ON}(0)} = \alpha_{I_{ON}} + \left[1 - \alpha_{I_{ON}}\right] e^{-\left(t/\tau_{I_{ON}}\right)^{\beta_{I_{ON}}}} \tag{3.7}$$

$$\Delta V_{TH} = \alpha_{V_{TH}} \left[1 - e^{-\left(t/\tau_{V_{TH}}\right)^{\beta_{V_{TH}}}} \right] \tag{3.8}$$

$$\frac{\mu(t)}{\mu(0)} = \alpha_{\mu} + \left[1 - \alpha_{\mu} \right] e^{-\left(t/\tau_{\mu}\right)^{\beta_{\mu}}} \tag{3.9}$$

where, $\boldsymbol{I_{ON}(t)}$ and $\boldsymbol{\mu(t)}$ are the on-state drain current and field-effect mobility at time *t* of the bias stress. $\boldsymbol{I_{ON}(0)}$ and $\boldsymbol{\mu(0)}$ are the initial on-state drain current and field-effect mobility at time $t = 0$, $\boldsymbol{\Delta V_{TH}}$ is the threshold voltage shift. $\alpha_{\boldsymbol{I_{ON}}}$, $\alpha_{\boldsymbol{V_{TH}}}$, $\alpha_{\boldsymbol{\mu}}$ are the steady state values at infinity, $\boldsymbol{\tau_{I_{ON}}}$, $\boldsymbol{\tau_{V_{TH}}}$, $\boldsymbol{\tau_{\mu}}$ are the time constants and $\boldsymbol{\beta_{I_{ON}}}$, $\boldsymbol{\beta_{V_{TH}}}$, and $\boldsymbol{\beta_{\mu}}$ are stretching parameters corresponding to the normalised on-state drain current, threshold voltage shift and the normalised field-effect mobility.

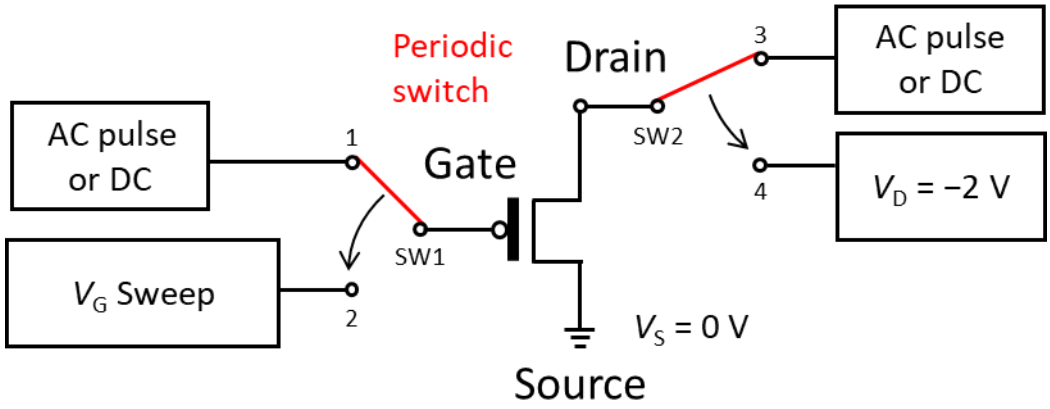

Figure 3.13: Bias stress setup. The same AC pulse or DC bias were applied to gate and drain (switch positions 1 and 3 respectively). Transfer characteristics were measurement by sweeping V_{GS} from 0 to −2 V and V_{DS} = −2 V (saturation) and V_S = 0 V (synchronised switch to positions 2 and 4 respectively).

3.5 Construction: OTFT-based temperature sensor system

The fabrication process of a temperature sensor system based on OTFT fabricated on PEN foil and commercially available thermistor (Farnell,

NTCLE100E3104J) is discussed. The sensor system design consists of a NTC thermistor (R_T) with nominal resistance of 100 kΩ at 25°C attached to the gate of a high-transconductance OTFT configured as a common-source transistor amplifier. The thermistor is chosen for its high sensitivity at low temperature range between 20 and 50°C, suitable for body and office temperature monitoring, while the transistor has sufficiently high on-state drain current and high transconductance for signal amplification. When the circuit is biased and the thermistor is heated, the thermistor acts as a transducer which induces electrical changes to the OTFT gate voltage based on the applied temperature, while the OTFT functions as an active amplifier of the induced signal. Two resistors connected to the gate (R_G) and drain (R_D) terminals are used to divide voltages and adjust signal levels of the gate and output voltages. Figure.14 depicts the OTFT-based temperature sensor schematic.

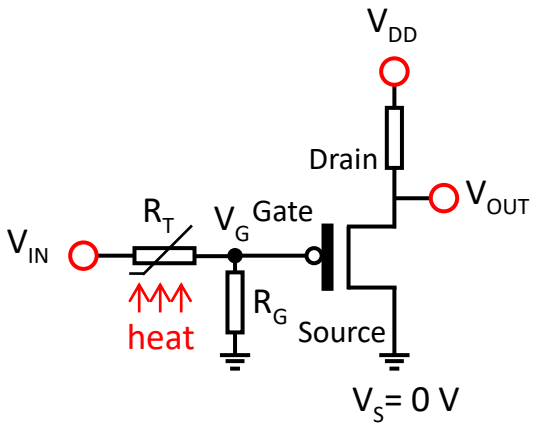

Figure 3.14: OTFT-based temperature sensor schematic.

The assembly process is as follows; the temperature sensor circuit was assembled on a piece of stripboard for connections between the resistors and thermistor. The thermistor and resistors were soldered directly on to the stripboard,

while connections to the OTFT required the use of a gold wire and silver conductive paste due to the small scale of the OTFT. The gold wire was attached to the OTFT using silver paste and provided an electrical connection between the drain and gate terminals of the OTFT and the discrete components, see Figure 3.15.

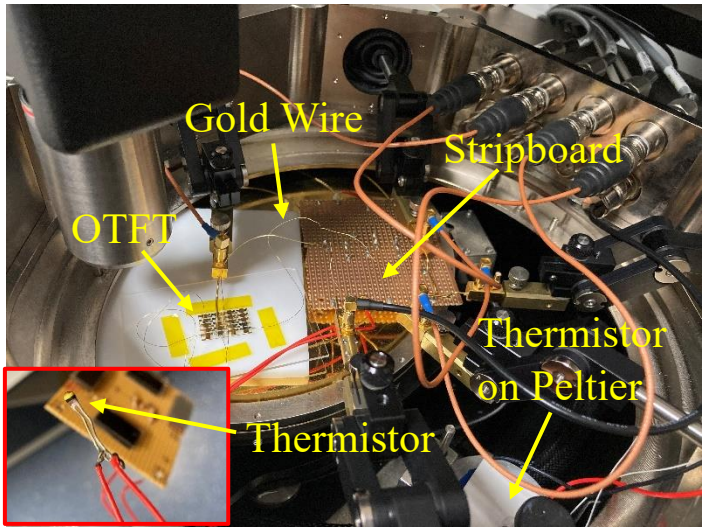

Figure 3.15: Temperature sensor measurement setup

3.6 Measurement: OTFT-based temperature sensor system

This section describes the equipment setup and measurement techniques employed to monitor the OTFT-based temperature sensor's response to temperature in the predetermined range between 20 °C and 50 °C, input voltage (V_{IN}) of −4 V and supply voltages (V_{DD}) from 0 to −8 V. Section 3.6.1 details the measurement process utilized to determine the temperature vs. resistance response of the thermistor. Section 3.6.2 describes the calculation to obtain a value of resistance for the resistor R_G used in series with the thermistor. Lastly, Section 3.6.3 reports on the measurement

technique used to measure the response of the whole OTFT-based temperature sensor system.

Measurement of the sensor was performed with an Agilent B1500A semiconductor device parameter analyser. A Signatone probe station ensured secure electrical connections to the sensor while housed inside the probe station. The thermistor was mounted (with thermally-conductive paste) directly to the surface of a Peltier element for heating and cooling. The Peltier is connected in a feedback loop to a temperature controller linked to a desktop computer for remote temperature control. A heat sink, mounted to the Peltier, absorbs and disperses heat away when needed. The combined Peltier and heatsink system were placed inside the probe station when measurements was taken. Figure 3.16 illustrates the thermistor temperature control system.

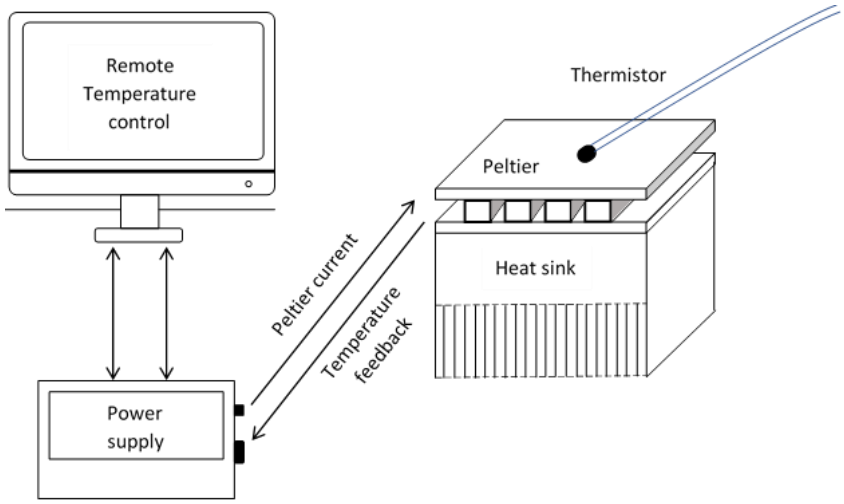

Figure 3.16: Thermistor temperature control system setup.

3.6.1 Temperature vs. thermistor response

To understand the behaviour of the 100 kΩ nominal resistance thermistor, the negative temperature coefficient (NTC) characteristic curve was measured in the temperature range between 20° C and 50 °C at 5°C increments suitable for low-voltage low temperature monitoring applications. The NTC characteristics curve was obtained by heating the thermistor to each temperature and subsequent measurement of the corresponding thermistor resistance was obtained using a digital multimeter.

3.6.2 Effect of resistor R_G on gate voltage

The process of finding the value of resistance for the resistor R_G in Figure 3.14 uses a simple approach. The left-hand side of the temperature sensor circuit forms a series connection between the resistor R_G and the thermistor resistance R_T. Therefore, it plays an important role in optimizing the gate voltage V_G and ultimately sensor sensitivity. When the circuit is biased with an input voltage (V_{IN}), current flows through the series resistors R_T and R_G to ground. Negligible current is observed at the transistor gate due to the high impedance of the gate dielectric. Therefore, the principles of voltage division described by Equation 3.10 can be utilized to find the resistance of R_G.

$$V_G = \frac{R_G}{R_T + R_G} \cdot V_{IN} \tag{3.10}$$

Setting V_{IN} to −4 V, R_T to the predetermined values at increments of 5°C from 20° C to 50 °C and increasing R_G from 10 kΩ and 100 kΩ at 10 kΩ increments, the optimal value of R_G is the resistance which produces the largest change in V_G across the temperature range of R_T, while keeping the gate voltage in the desired range, typically between –1 and –2 V.

With the optimal value of R_G implemented into the sensor circuit design, an investigation was conducted to confirm the response of V_G due to R_G for R_T between 20 °C and 50 °C at 5°C increments. The thermistor was heated to the respective temperatures using the temperature setup in Figure 3.16 and an Agilent B1500A semiconductor device analyser was used to evaluate the sensor.

3.6.3 Effect of temperature and supply voltage on OTFT based temperature sensor

The effect of temperature and supply voltage V_{DD} on the gate and output voltages of the temperature sensor were investigated. The process begins by heating the thermistor to seven predefined temperatures between 20 °C and 50 °C at 5 °C increments. Note, in all experiments, only the thermistor is heated. At each temperature, V_{DD} is ramped from 0 to – 8 V for V_{IN} = −4 V, V_S = 0 V and R_D = 47 kΩ and the gate and output voltage as functions of both temperature and V_{DD} are monitored using the Agilent B1500A.

3.7 Summary

This chapter presented the fabrication process of MIM structures and low-voltage, hysteresis-free OTFTs based on DNTT on PEN substrate. It described the electrical and structural measurements on such devices and introduced interdigitated source/drain electrodes to optimise the transistor performance. Furthermore, a novel approach for pulse bias stress based on off-time duty cycle was introduced to study the electrical and environmental stability of the transistors. Finally, a temperature sensor system based on a thermistor and OTFT was demonstrated, thus paving a way toward fully flexible sensor on plastic substrate.

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Chapter 4

High transconductance OTFTs with interdigitated source/drain contact on PEN foils

In the methodology Chapter, the fabrication of organic thin-film transistors with interdigitated source/drain contacts was described. This chapter reports on the effectiveness of interdigitated source/drain contact geometry in optimizing transistor performance, particularly the drain current and AC transconductance. Section 4.1 introduces the interdigitated source/drain contacts for optimizing transistor channel geometry, drain current and transconductance. Section 4.2 describes the experiments and measurements conducted to evaluate the effects of interdigitated contacts on transistor performance. Sections 4.3 and 4.4 presents the result of narrow-gate and wide-gate transistors with interdigitated source/drain contacts and their effect on

transistor parameters, respectively. Section 4.5 reports on the effect of channel dimensions on the AC transconductance. Section 4.6 discusses results. Finally, a summary of the work is detailed in Section 4.7.

4.1 Introduction

The transconductance (g_{m}) of a transistor is used to evaluate its performance. While field-effect mobility has a direct effect on the transconductance, parameters such as channel length [4.1], contact resistance [4.2], material and thickness of the semiconductor [4.3], and surface roughness of the gate dielectric [4.4] have been shown to affect the mobility and therefore the transconductance. Consequently, these must be successfully addressed for applications where high transconductance is crucial.

This study introduces an approach to increase the transistor transconductance by utilizing interdigitated source/drain contacts. Previously, low-voltage OTFTs with a "standard" channel geometry, also described as a rectangular channel separating the drain and source electrodes, have shown a transconductance of 12 µS [4.5]. The increase in transconductance was achieved through downscaling the channel length [4.6]. This chapter investigates the concept of improving the transconductance of a transistor by upscaling the channel width *W* while downscaling the channel length *L*, thus optimizing the channel width-to-length ratio *W/L*. Based on equations for the drain current $I_{\mathrm{D,sat}} = \frac{W}{2L}\mu_{\mathrm{sat}}C_{\mathrm{diel}}(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2$ and transconductance $\mathrm{g_{m,sat}} = \frac{W}{L}\mu_{\mathrm{sat}}C_{\mathrm{diel}}(V_{\mathrm{GS}} - V_{\mathrm{TH}})$ in saturation, the modulation of *W/L* has a direct impact on

transistor parameters such as on-state drain current and transconductance. To achieve this, interdigitated source/drain contacts are employed.

Interdigitated source/drain contacts represent an arrangement of the source and drain electrodes formed by multi-finger structures interlocked to create a long, meandering transistor channel. This configuration increases *W*, resulting in the upscaling of *W/L* by an order of a magnitude, or more, while maintaining a small transistor area. Such an approach could provide low-voltage transistors with sufficient transconductance for amplification [2.23] as well as play an important role in downscaling field-effect transistors [4.7]. Figure 4.1 demonstrates the interdigitated channel configuration in comparison to its standard counterpart.

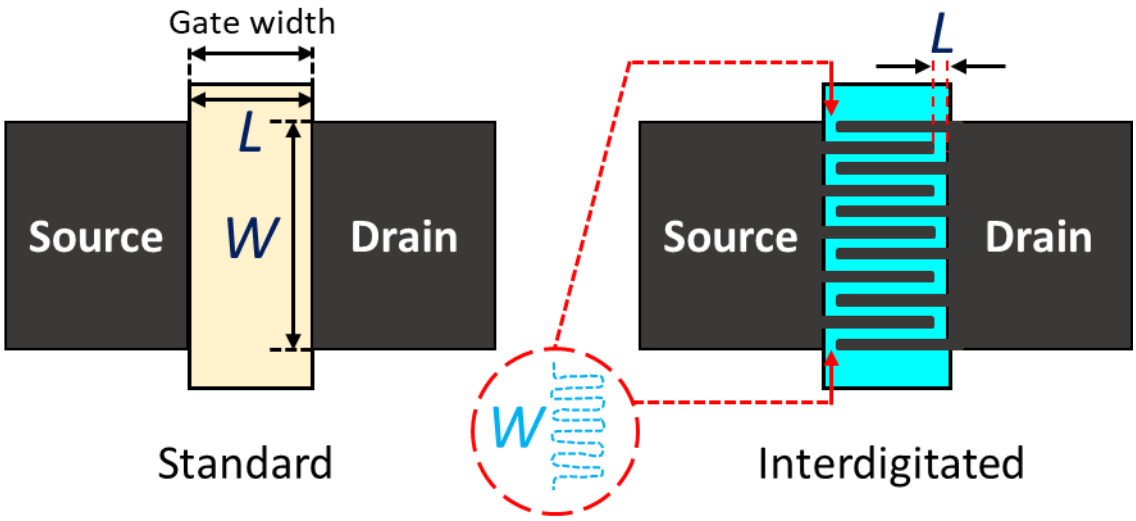

Figure 4.1: Standard rectangular and interdigitated source/drain contacts.

4.2 Experimental details

This section outlines the experimental procedures carried out to study the effects of interdigitated source/drain contacts, i.e. increased channel width-to-length

ratio (*W/L*), on the electrical performance of low-voltage DNTT transistors on PEN substrate.

4.2.1 Interdigitated source/drain contacts

The effect of interdigitated source/drain contact channel geometry on the electrical performance of OTFTs was investigated. Two batches of transistors were fabricated following the fabrication process described in Chapter 3. The first batch consisted of 44 wide-gate OTFTs with varying channel dimensions; *L* from ~20 to ~50 μm and *W* from ~12 to ~18 mm. The second batch that was fabricated together with the wide-gate OTFTs consisted of 14 narrow-gate OTFTs with *L* ~ 5 to 20 μm and *W* ~ 3.7 to 4.03 mm.

The terms narrow- and wide-gate OTFT refers to the scale of the transistor channel controlled by variations in the width of the gate electrode (gate width), see Figure 4.2.

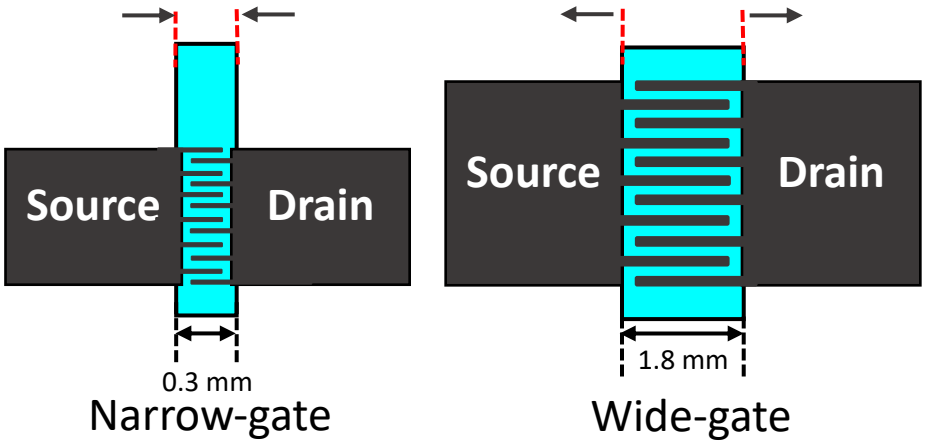

Figure 4.2: Schematic of narrow gate and wide-gate OTFTs.

The material and thickness of each OTFT layer from bottom to top is as follows: the gate electrode is made of 30-nm-thick Al, the gate dielectric is ~17-nm-thick bi-layer of AlO_x coated with a monolayer of octadecyl phosphonic acid $C_{18}PA$, the organic semiconductor is a 20-nm-thick DNTT and the source/drain contacts are made of 50-nm-thick Au.

For the purpose of analysis, the transistors were divided into two main groups based on channel width *W* (narrow- and wide-gate), and 5 subgroups based on their channel lengths. The narrow-gate subgroups ($W < 4.03$ mm) consisted of transistors with a) channel length $L < 10$ μm and b) $L \sim 10$ to 20 μm. The wide-gate subgroups (W ~ 12 to 18.23 mm) consisted of OTFTs with c) $L = 20$ to 30 μm, d) $L = 30$ to 40 μm and e) $L = 40$ to 50 μm.

The electrical performance of the devices was measured following the transfer characteristics parameter extraction method outlined in Chapter 3. Here, only the saturation regime ($V_{GS} = V_{DS} = -2$ V) is used. Measurements were performed using an Agilent B1500A semiconductor device parameter analyser. Device parameters including the on-state (I_{ON}) and off-state (I_{OFF}) drain currents, field-effect mobility (μ), threshold voltage (V_{TH}), and subthreshold slope (S) were studied as a function of *W/L* ratio.

4.2.2 Drain current and AC transconductance

Device transconductance measurements were conducted on three wide-gate and three narrow-gate transistors. Devices with similar electrical performance and varied *W/L* ratios between 202 and 524 were chosen to observe the effect of relatively

high *W/L* ratio on the transconductance. Next, an AC waveform of −0.2 V_{pp} (−2 V offset) at 1 Hz was applied to the gate terminal of each transistor (see Figure 3.11). Drain and source terminals were biased with DC voltages of −2 V and 0 V respectively. Measurements of the peak-to-peak sinusoidal drain current were extracted as a function of time and subsequently used in the AC transconductance calculations.

4.3 Interdigitated source/drain contact in narrow-gate OTFTs

This section reports on the measurements and findings associated with the narrow-gate OTFTs with interdigitated source/drain contacts. Narrow-gate transistors were fabricated with *W/L* ratios between 202 and 655. Variations in *W/L* were achieved through variation in *L* (*L* ≤ 20 μm) while *W* ~ 4.03 mm. Figure 4.3 shows a top-view of a narrow-gate OTFT with gate width of 0.3 mm.

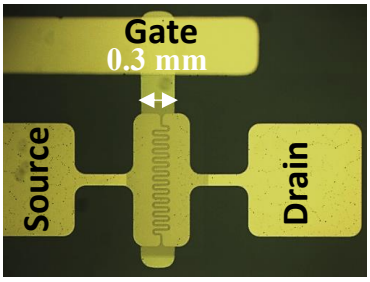

Figure 4.3: Top-view of narrow-gate width OTFT with *L* = 17 μm and *W* = 4.03 mm.

The subsequent subsections describe the impact of varying *W/L* ratio on the electrical performance of DNTT OTFTs on PEN substrates.

4.3.1 Transfer and output characteristics

Figure 4.4 (a) and (b) show the transfer characteristics of OTFTs with the wide-gate and narrow-gate, respectively. The output characteristics are shown in Figure 4.4 (c) and (d) respectively. Detailed analysis into the effect of interdigitated source/drain contacts on OTFTs parameters is presented in the following sub-sections.

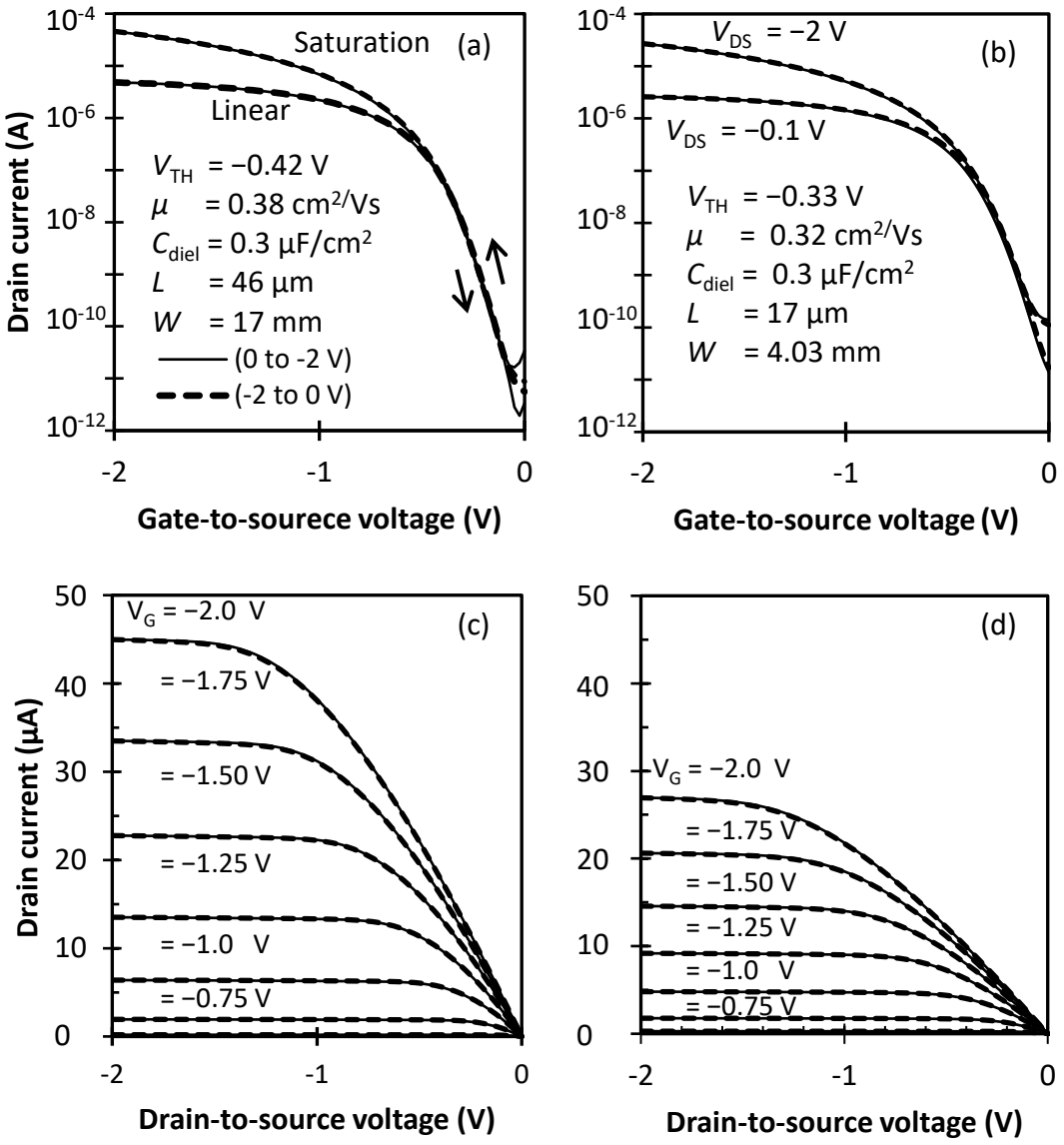

Figure 4.4: Transfer (a, b) and output (c, d) characteristics for wide-gate (a, c) and narrow-gate (b, d) OTFTs on PEN. Each curve shows hysteresis measurement from 0 to –2 V (solid line) and back (dash lines).

The result of Figure 4.4 showcases the OTFTs presented in this thesis. While fabricated on flexible PEN substrate, the devices showed comparable results with similar DNTT OTFTs on glass substrates [1.17, 2.23]. Low-voltage operation of V_{GS} = –2 V was achieved with V_{TH} ~ –0.3 to ~ –0.4 V, while large number of devices reported in literature require much higher voltages between 10 V to 100 V [4.8-4.10]. Hysteresis-free behaviour was confirmed through the forward and reverse V_{GS} sweeps, indicating good dielectric/semiconductor interface between AlO_x/C_{18}PA and DNTT. In addition, high on/off current ratio in excess of 10^6 and field-effect mobility of 0.3 to 0.4 cm^2/Vs were achieved.

4.3.2 Field-effect mobility and threshold voltage

Figure 4.5 shows the field-effect mobility μ of narrow-gate OTFTs with interdigitated source/drain contacts as a function of *W/L* ratio. Transistors with the smallest channel length (L < 10 μm; *W/L* = 437 to 655) showed the lowest mobility of 0.23±0.04 cm^2/V·s. Transistors with higher channel lengths (L = 10 to 20; *W/L* = 202 to 276) exhibited mobility of 0.31±0.03 cm^2/V·s. As *W/L* is increased, μ decreased from 0.35 to 0.17 cm^2/V·s.

Figure 4.6 depicts the threshold voltage V_{TH} of narrow-gate OTFTs as functions of *W/L*. The threshold voltage increased from 0.3 to 0.47 V with increasing *W/L* as the channel length is reduced. Transistors with L < 10 μm experience a consistent threshold voltage of 0.43±0.02 V, while L = 10 and 20 μm showed a wider spread between 0.3 and 0.42 V with average and deviation of 0.35±0.04 V. The trend suggests

better threshold voltage stability at shorter channel lengths and larger variation for OTFT with larger channel lengths.

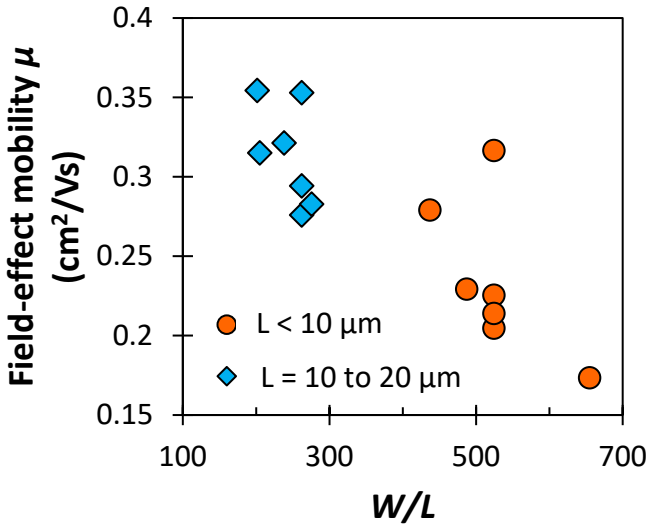

Figure 4.5: Field-effect mobility as a function of *W/L* for narrow-gate OTFTs with interdigitated source/drain contacts and L < 10 μm (circles) or L = 10 to 20 μm (diamonds).

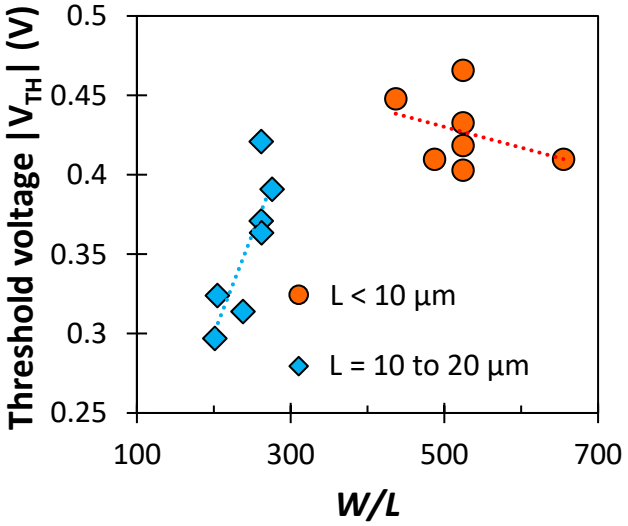

Figure 4.6: Threshold voltage as a function of *W/L* for narrow-gate OTFTs with interdigitated source/drain contacts and L < 10 μm (circles) or L = 10 to 20 μm (diamonds).

4.3.3 On-state and off-state drain currents

Figure 4.7 shows on-state drain current I_{ON} as a function of *W/L*. The result shows a positive correlation between the on-state current and channel length as *W/L* is increased. Transistors with increased channel length *L* = 10 to 20 μm displayed lower on-state drain current of 27±1.9 μA when *W/L* is varied from 202 to 276. Shorter channel transistors with *L* < 10 μm displayed current of 39±5 μA for an increased *W/L* between 437 and 655. Since the drain current increases with *W/L*, an improvement in the drain current for *L* < 10 μm would be expected.

While an improvement in the on-state drain current at shorter channel lengths is apparent, normalisation of the on-state drain current (I_{ON}**L/W*) removes its dependence on *W/L*, i.e. the on-state drain current is no longer influenced by channel dimension *L* and *W*. Such normalisation revealed a new observation, shown in Figure 4.8. Transistors with *L* = 10 to 20 μm displayed an average normalised on-state drain current of 1.1×10^{-7} A; transistors with *L* < 10 μm displayed reduced average current of 7.5×10^{-8} A. The observation also revealed a gradual decreasing dependence as *W/L* is increased and *L* decreased. Since this effect is more pronounced at shorter channel lengths, it is assumed that the contact resistance dominates at reduced channel length.

Figure 4.9 shows the off-state drain current I_{OFF} as a function of *W/L*. As *W/L* is increased so does the off-state drain current. Shorter channel OTFTs with *L* < 10 μm showed averages and standard deviation of 280±260 pA, while longer channel lengths *L* = 10 to 20 μm showed values of 120±60 pA. *W/L* from ~202 to ~654 showed a total increase of ~36 pA; however, minimum and maximum I_{OFF} located at *W/L* ~276 and

~524 respectively showed a total change of ~887 pA. Normalising the off-state drain current (I_{OFF}*L/W) and plotting it as a function of W revealed no dependence on L (see Figure 4.10).

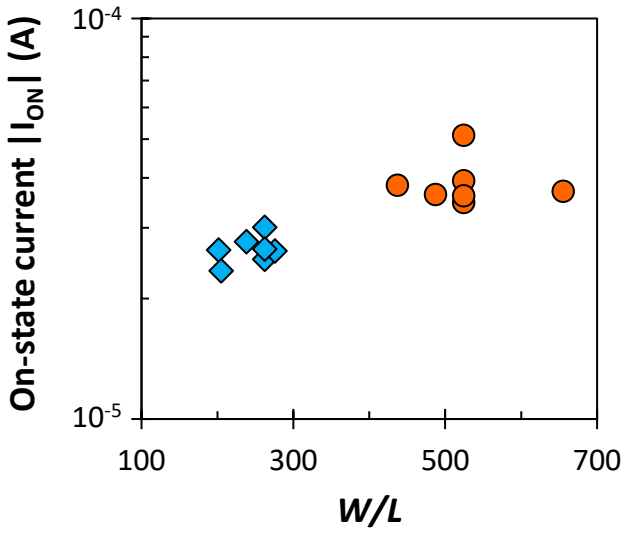

Figure 4.7: On-state drain current as a function of W/L for narrow-gate OTFTs with interdigitated source/drain contacts and L < 10 μm (circles) or L = 10 to 20 μm (diamonds).

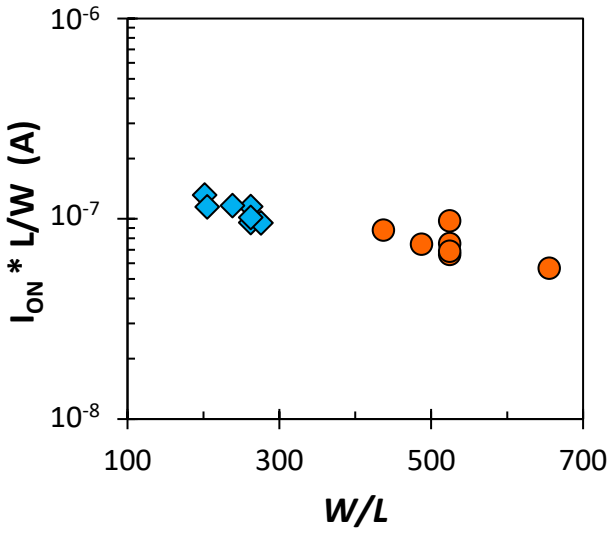

Figure 4 8: Normalised on-state drain current as a function of W/L for narrow-gate OTFTs with interdigitated source/drain contacts and L < 10 μm (circles) and L = 10 to 20 μm (diamonds).

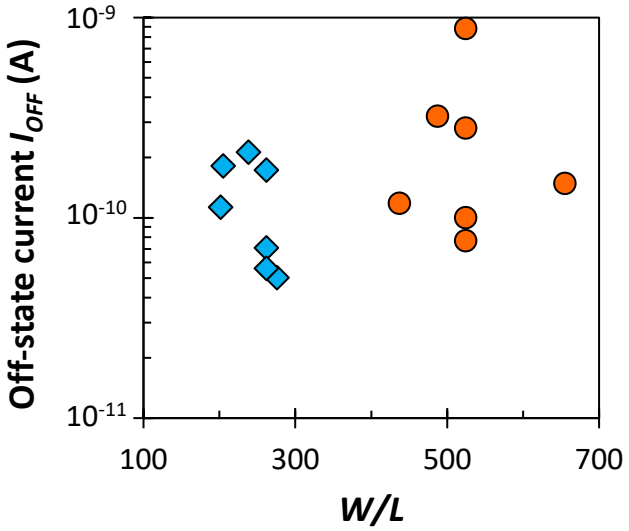

Figure 4.9: Off-state drain current as a function of *W/L* for narrow-gate OTFTs with interdigitated source/drain contacts and $L < 10$ μm (circles) or $L = 10$ to 20 μm (diamonds).

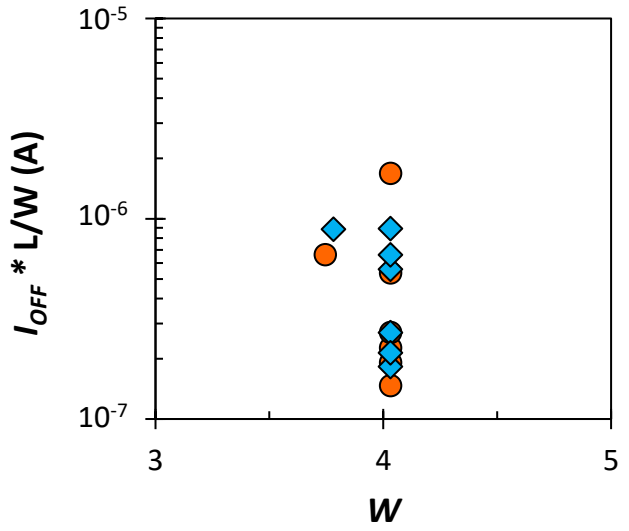

Figure 4.10: Normalised off-state drain current as a function of *W* for narrow-gate OTFTs with interdigitated source/drain contacts and $L < 10$ μm (circles) or $L = 10$ to 20 μm (diamonds).

4.3.4 Subthreshold slope

Figure 4.11 (a) shows the transistor subthreshold slope as a function of *W/L*; the slope increases as *W/L* is increased. Transistors with shorter channel lengths L < 10 μm display averages of 128±15 mV/decade and 102±4 mV/decade for L = 10 to 20 μm, suggesting that at short channel lengths the subthreshold slope is larger than for longer channel lengths. Additionally, when plotted as a function of the threshold voltage, an increase is observed; transistors with larger L show lower threshold voltage and values approaching ideal subthreshold slopes, as demonstrated by Figure 4.11 (b).

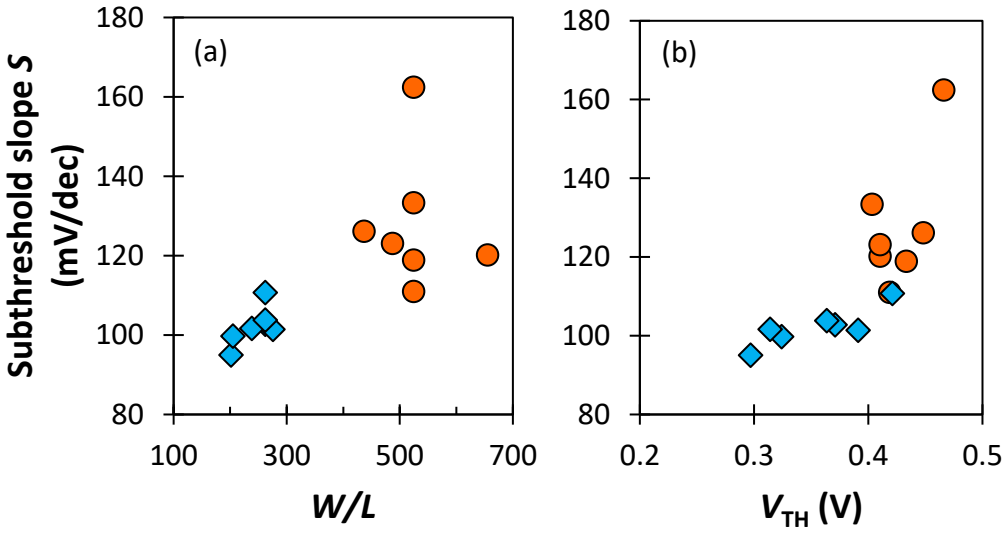

Figure 4.11: Subthreshold slope as a function of *W/L* (a) and V_{TH} (b) for narrow-gate OTFTs with interdigitated source/drain contacts and L < 10 μm (circles) or L = 10 to 20 μm (diamonds).

4.3.5 Gate leakage current

Figure 4.12 shows the gate leakage current I_G of narrow-gate transistors as a function of *W/L*. Results show that the transistor gate leakage current is not influenced by the channel dimension W or L. As *W/L* is increased, the change in I_G is negligible.

Transistors with L < 10 μm displayed average I_G of 1.1x10^{-11} A, while L = 20 to 30 μm displayed average of 1.5x10^{-11} A.

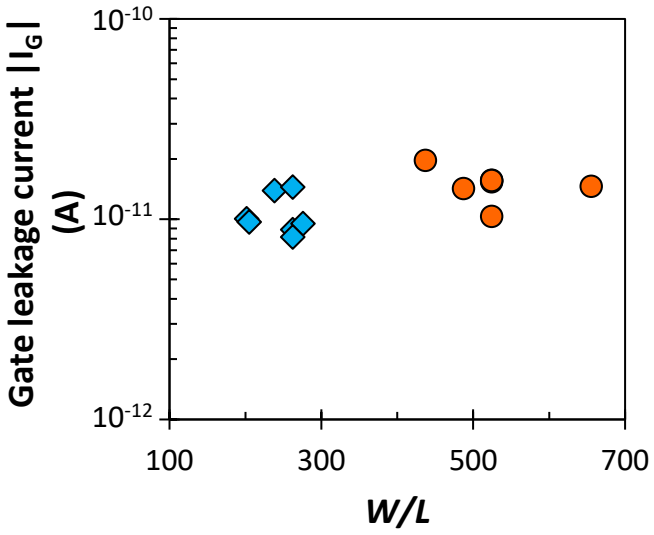

Figure 4.12: Gate leakage current as a function of *W/L* for narrow-gate OTFTs with interdigitated source/drain contacts and L < 10 μm (circles) or L = 10 to 20 μm (diamonds).

4.4 Interdigitated source/drain contact in wide-gate OTFTs

This section reveals the impact of interdigitated source/drain contact on transistor parameters with wide gates. Variation in *W/L* between 210 and 910 was achieved by manipulating the gate width (1.8, 1.6, 1.4, and 1.2 mm), resulting in W values between ~12 and 18.23 mm and L values between 20 and 50 μm. Figure 4.13 shows a top-view of two OTFTs with gate width of 1.4 mm (a) and 1.8 mm (b) with W =15.40 mm and W = 18.23 mm respectively.

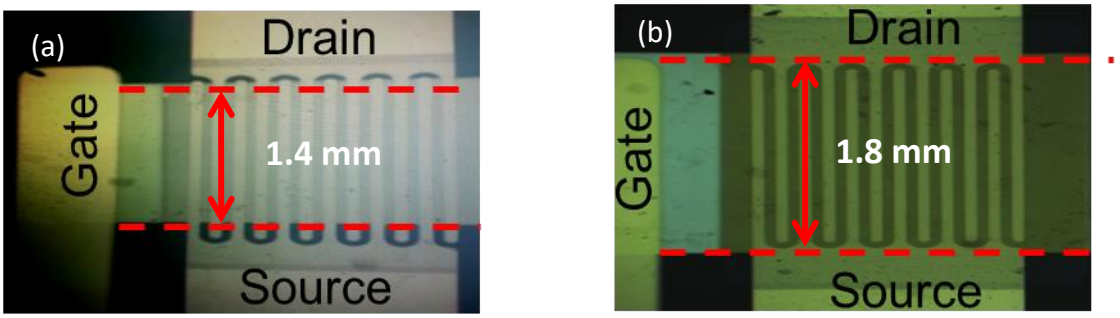

Figure 4.13: Gate width manipulation in wide-gate OTFTs resulting in reduced gate width of 1.4 mm and W =15.40 mm (a) and full gate width of 1.8 mm and W = 18.23 mm (b). Dashed horizontal lines show the gate width boundaries.

4.4.1 Field-effect mobility and threshold voltage

Figure 4.14 shows the field-effect mobility of wide-gate transistors as a function of channel width-to-length ratio W/L. A decreasing trend in field-effect mobility μ is observed as W/L increases. Transistors with the highest channel lengths L = 40 to 50 µm (W/L = 290 to 440) displayed the highest mobility of 0.35±0.03 $cm^2/V{\cdot}s$. OTFTs with medium channel lengths L = 30 to 40 µm (W/L = 380 to 590) displayed reduced values of 0.30±0.02 $cm^2/V{\cdot}s$. Finally, OTFTs with the shortest channel lengths L = 20 to 30 µm (W/L = 620 to 910) displayed the lowest mobility of 0.25±0.06 $cm^2/V{\cdot}s$.

Figure 4.15 shows the effect of W/L on the threshold voltage V_{TH} at various channel lengths. The extracted V_{TH} increases with W/L from −0.33 to −0.74 V as the channel length decreases, showing a dependence on W/L ratio. Results showed that transistors with L = 40 to 50 µm displayed the lowest threshold voltages of −0.52±0.08 V. Transistors with medium channel lengths of L = 30 to 40 µm, exhibited increased V_{TH} of 0.57±0.06 V. Transistors with shortest channel lengths of L = 20 to 30 µm

displayed values of 0.6±0.06 V. Following the trend shown, the wide-gate transistors also show less variation in the threshold voltage for large *W/L*.

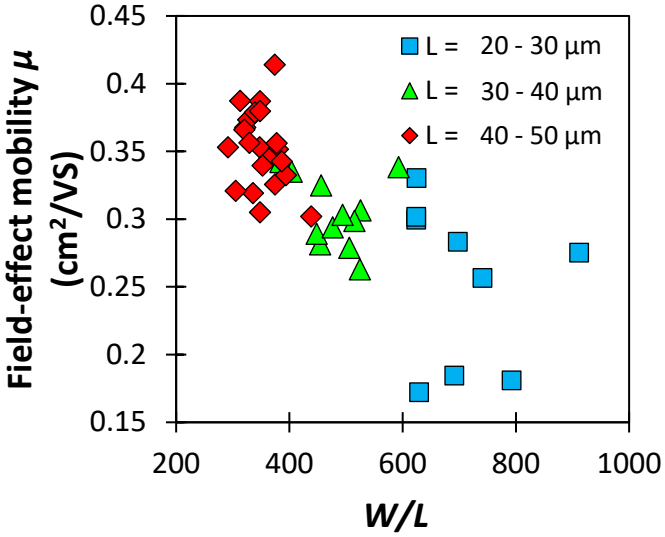

Figure 4.14: Field-effect mobility as a function of *W/L* for wide-gate OTFTs with interdigitated source/drain contacts and *L* = 20 to 30 μm (square), *L* = 30 to 40 μm (triangles), or *L* = 40 to 50 μm (diamonds).

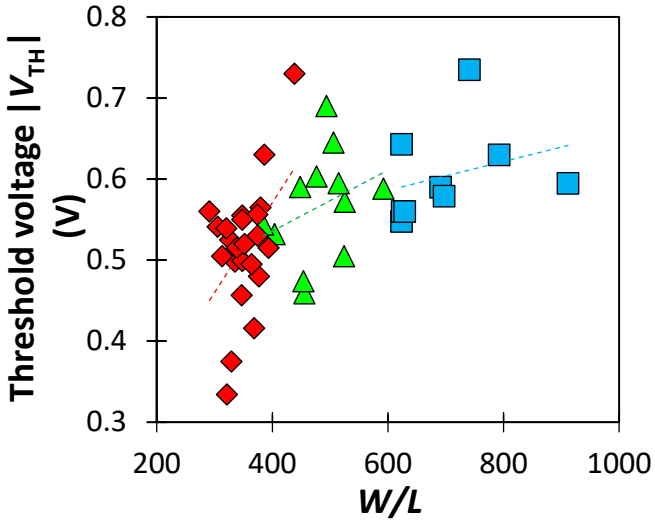

Figure 4.15: Threshold voltage as a function of *W/L* for wide-gate OTFTs with interdigitated source/drain contacts and *L* = 20 to 30 μm (square), *L* = 30 to 40 μm (triangles), or *L* = 40 to 50 μm (diamonds).

4.4.2 On-state and off-state drain currents

Figure 4.16 (a) shows the on-state drain current I_{ON} as a function of *W/L*. The on-state current increases with rising *W/L* and decreasing channel length. OTFTs with the shortest channel lengths between 20 and 30 µm displayed the highest current with an average of 49 µA; channel lengths between 30 and 40 µm showed an average of 40 µA; and channel lengths between 40 and 50 µm yielded the lowest current of 39 µA.

Results for normalised (I_{ON} * *L/W*) shown in Figure 4.16 (b) showed a reduction of 93 nA between $1.4x10^{-7}$ A and $4.7x10^{-8}$ A as *W/L* is increased. Contextually the drain current should remain constant when normalised. OTFTs with *L* = 20 to 30 µm showed average normalised on-state current $7x10^{-8}$ A. Channel lengths *L* = 30 to 40 µm and *L* = 40 to 50 µm display averages of $8.5x10^{-8}$ A and $1.0x10^{-7}$ A respectively.

For off-state drain current I_{OFF} shown in Figure 4.17 (a), the current is split into two regions regardless of channel lengths. The upper region accounts for the majority of OTFTs with mid to high channel lengths between 30 and 50 µm and an average current of $2.6x10^{-8}$ A, while the majority of the lower region is accounted for by OTFTs with channel lengths between 20 and 30 µm and average current of $3.1x10^{-11}$ A.

The behaviour of the off-state drain current would be explained further with additional analysis of normalising the off-state drain current (I_{OFF} * *L/W*) with respect to the channel dimension and displaying it as a function of the channel width *W*, see Figure 4.17(b). When normalised, a new separation of the transistors results. This separation is however governed by the channel width *W*. Transistors with *W* < 18.23 mm displayed an average off-state current of $6.6x10^{-11}$ A, while transistors with *W* =

18.23 mm displayed up to ~3.3 orders of magnitude reduction at an average of 3.5×10^{-14} A. Based on this finding, a low off-state drain current is consistently achieved for transistors with the gate width of 18.23 mm. In such a case the entire transistor channel is located above the gate electrode and thus fully controlled by the applied gate voltage.

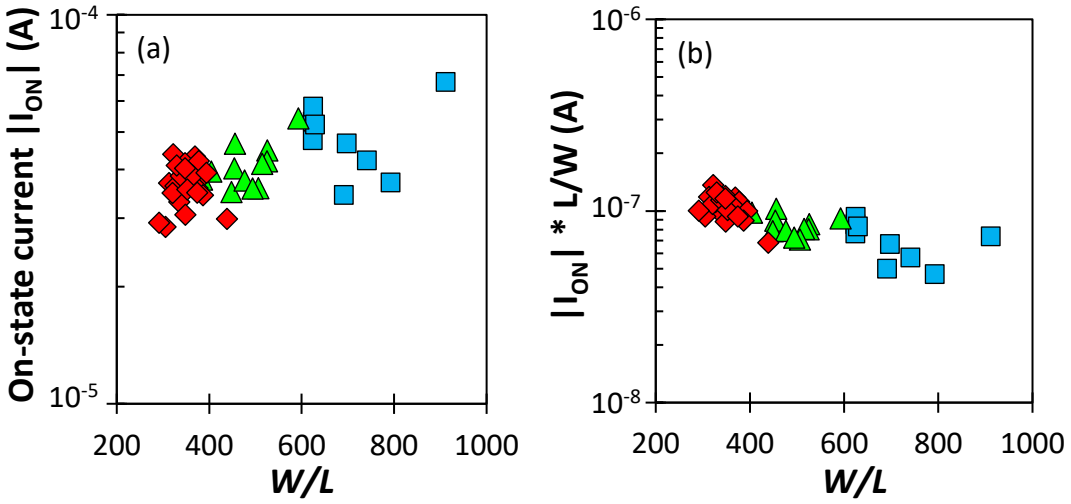

Figure 4.16: On-state drain current (a) and normalised on-state drain current (b) as functions of *W/L* and channel lengths *L* = 20 to 30 µm (squares), 30 to 40 µm (triangles) and 40 to 50 µm (diamonds).

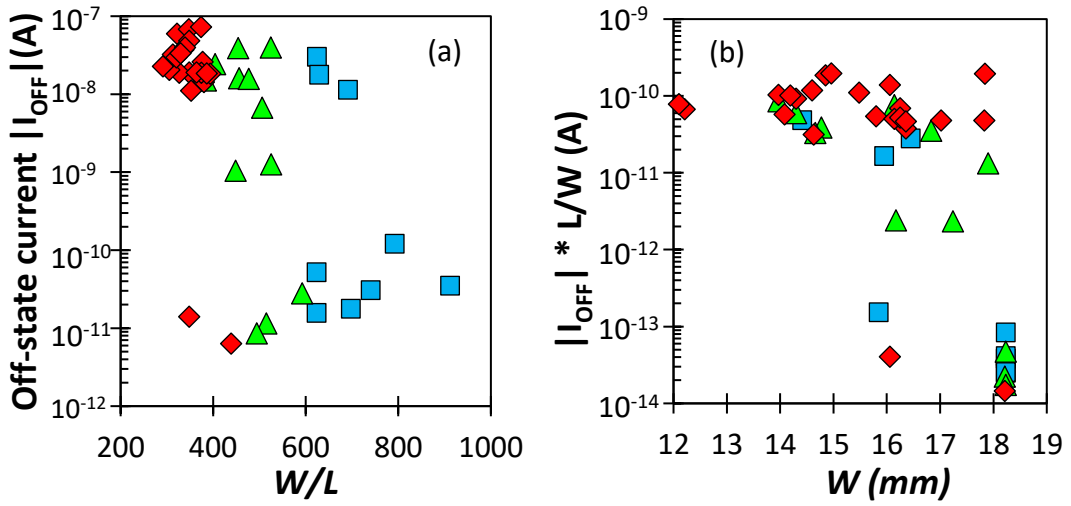

Figure 4.17: Off-state drain current (a) and normalised off-state drain current (b) as functions of *W/L* and width *W* respectively, for channel length *L* = 20 to 30 µm (squares), 30 to 40 µm (triangles) and 40 to 50 µm (diamonds).

4.4.3 Subthreshold slope

Figure 4.18 (a) shows the changes in sub-threshold slope *S* of wide-gate OTFTs, with increasing *W/L* and decreasing channel length *L*. The result shows a spread distribution with a reduction in the slope as channel length is decreased and *W/L* is increased. Transistors with channel lengths between 40 to 50 µm displayed values of 198±49 mV/decade; transistors with channel lengths between 30 to 40 µm and 20 to 30 µm displayed 147±57 mV/decade and 125±48 mV/decade, respectively.

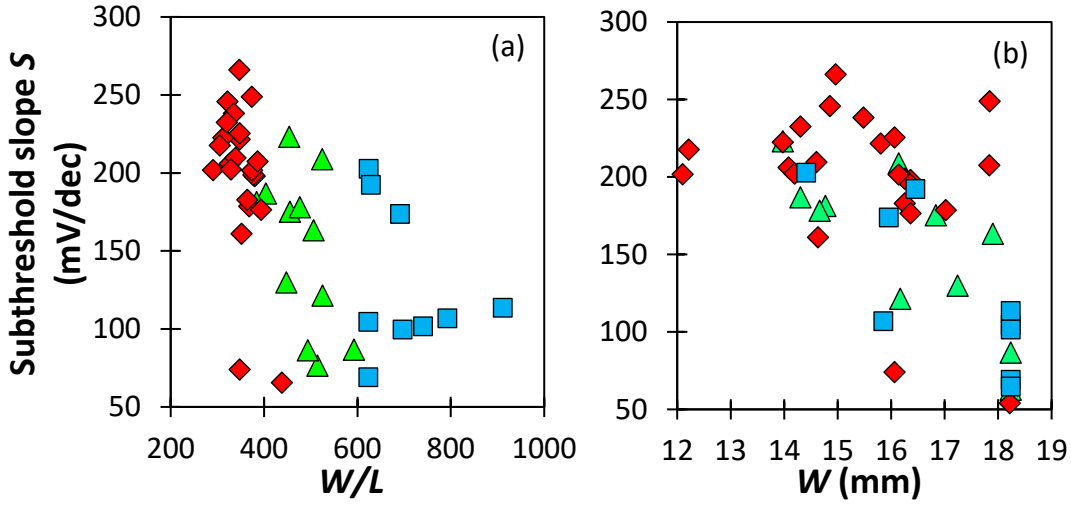

Figure 4.18: Subthreshold slope as a function of *W/L* (a) and *W* (b) for wide-gate OTFTs with interdigitated source/drain contacts and *L* = 20 to 30 µm (square), *L* = 30 to 40 µm (triangles), or *L* = 40 to 50 µm (diamonds).

When plotted as a function of channel width, the result in Figure 4.18 (b) indicates a consistently reduced subthreshold slope for OTFTs with *W* = 18.23 mm displaying values between 54 and 114 mV/decade. However, OTFTs with reduced channel width *W* < 18.23 mm experience varying distributions between 74 and 266 mV/decade with no clear dependence on channel length or width, suggesting a partial dependence on not only channel width but more importantly on the position of the gate

relative to the channel. i.e. the placement of the full channel above the gate also has an effect on the sub-threshold slope.

4.4.4 Gate leakage current

Figure 4.19 displays the gate leakage current of wide-gate transistors as a function of *W/L*. Results suggest no direct dependence on channel length although a few transistors with *L* = 20 to 30 µm experienced raised gate leakage current compared to other channel lengths.

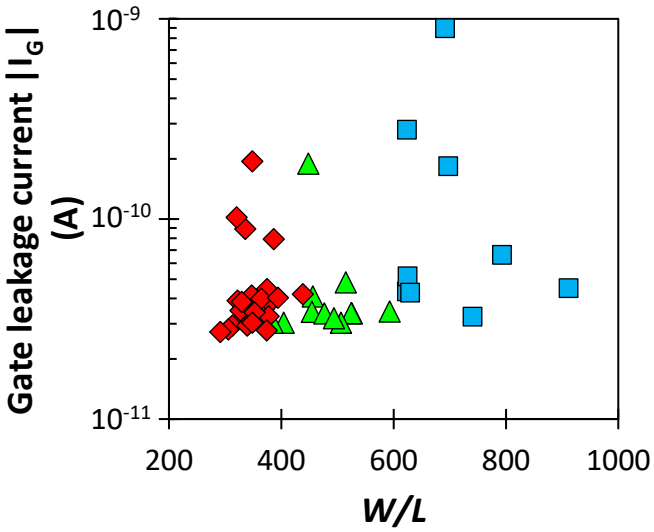

Figure 4.19: Gate leakage current as a function of *W/L* for wide-gate OTFTs with interdigitated source/drain contacts and *L* = 20 to 30 µm (square), *L* = 30 to 40 µm (triangles), or *L* = 40 to 50 µm (diamonds).

4.5 AC transconductance in narrow- and wide-gate OTFTs

The sinusoidal drain currents and AC transconductance measurements performed on a sample of transistors with varying *W/L* are detailed in this section.

4.5.1 Drain current

Figure 4.20 shows the sinusoidal drain current waveforms of three narrow gate (T1, T5 and T6) and wide-gate (T2, T3 and T4) OTFTs with varied *W/L* as functions of time. Results reveal a larger increase in the rate of change of drain current as *W/L* is increased for a constant input gate voltage. This correlation is true regardless of gate width employed (narrow or wide), the drain current increased linearly with an increase in *W/L*. OTFT with the largest *W/L* ratio, T1, experienced the largest change in drain current, while equally, OTFT with the least *W/L*, T6, experienced the least drain current. Results are summarised in Table 3.

Table 3. Dependence of AC drain current and transconductance on *W/L* ratio.

Transistor	***W/L***	i_d **(µA) peak-peak**	g_m **(µS)**
T1	524 (4.03mm/7.7µm)	11.1	56
T2	494 (18.23 mm/37 µm)	10.6	53
T3	408 (12.54 mm/30.77 µm)	8.3	41
T4	371 (17.13 mm/46 µm)	7.6	38
T5	262 (4.03 mm/15.38 µm)	6.4	32
T6	202 (4.03 mm/20 µm)	5.1	26

The change in drain current increased linearly with *W/L* in agreement with the drain current equation, proving the hypothesis that the drain current improves by increasing the channel *W/L* dimensions. Generally, wide-gate OTFTs possess larger *W/L* ratios as an advantage of having larger *W* of up to 18.23 mm compared to 4.03 mm for narrow gate equivalents therefore leading to larger drain current. However, narrow-gate transistor T1 displayed the largest drain current of all transistors. This exception is the result of the very short channel length of $L \sim 7.7$ µm achieved as a result of a small separation between the substrate and the mask during the vacuum evaporation.

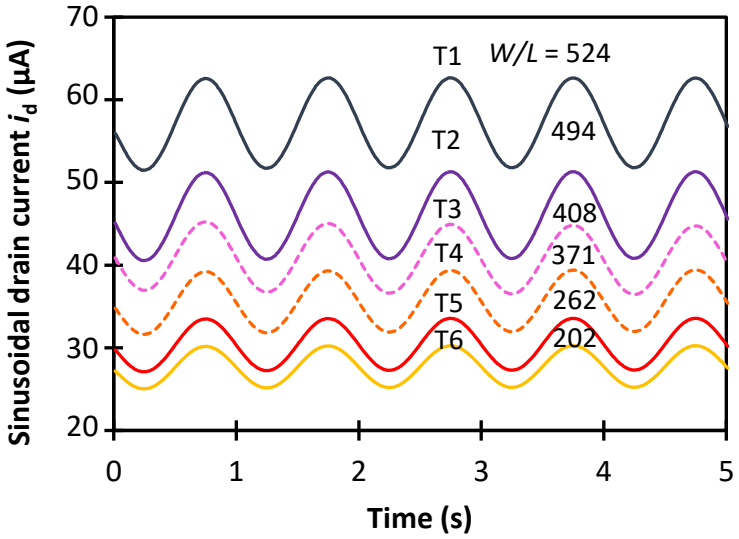

Figure 4.20: Sinusoidal drain current as a function of time (for $\boldsymbol{v_{gs}}$ of $-0.2V_{pp}$, and V_{DS} and V_S of −2 V and 0 V respectively. The solid and dashed lines correspond to narrow- and wide-gate transistors, respectively.

4.5.2 AC transconductance

Figure 4.21 shows the calculated AC transconductance g_m of transistors T1 – T6 obtained from the sinusoidal drain current measurement and plotted as a function

of their respective *W/L* ratio. Results summary is shown in Table 3. Results show a linear relationship with *W/L* when all transistors are compared. The larger the *W/L* ratio, the greater the transconductance. However, when narrow gate and wide-gate transistors are compared, the rate of increase (trendline) is shown to be steeper for the latter devices. The same observation is also true for the sinusoidal drain current.

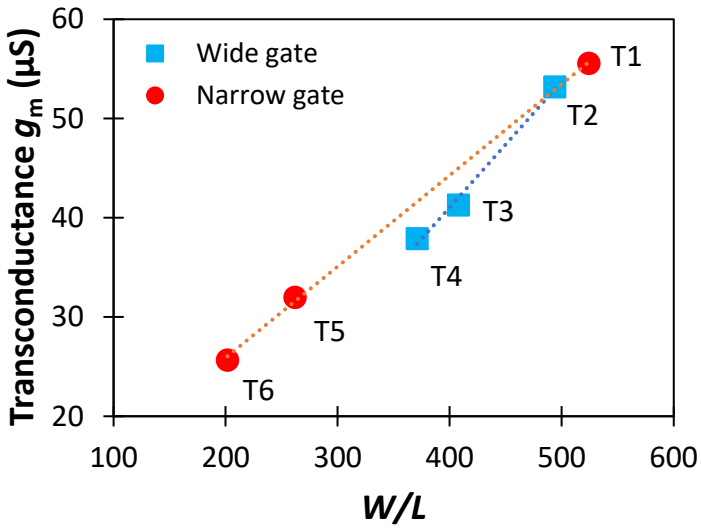

Figure 4.21: AC transconductance g_m as a function of *W/L* for narrow-gate (circles) and wide-gate (squares) OTFTs.

4.6 Discussion

The effect of modulating channel dimensions to achieve enhancement in the drain current and AC transconductance of DNTT based OTFTs on PEN has been characterised. Based on theory, the channel geometry of a transistor can be utilised to improve key parameters; however, this research has shown that in addition to improving the drain current and AC transconductance, other parameters of the transistor could also benefit or suffer as a result. Furthermore, all devices displayed impressive low-voltage operation at $V_{GS} = V_{DS} = -2$ V regardless of channel ratio.

In the first instance, employment of interdigitated source/drain contacts in place of the standard "rectangular" drain/source contacts makes efficient use of the channel area while maintaining a small transistor form factor. The use of interdigitated source/drain contacts to increase channel width yielded significant improvement in the *W/L* ratio in excess of 900 in wide-gate and over 600 in narrow-gate devices.

The drain current of an OTFT is a function of the channel width and varies inversely with channel length ($1/L$). Therefore, up-scaling of channel width to length ratio *W/L* has a direct influence on the on-state drain current. Analysis of the on-state drain current proved the dependence on channel ratio. The results showed that the on-state drain current is dependent on the channel length and *W/L* ratio. Transistors with the smallest channel lengths showed the highest on-state current and vice-versa. Principally, the resistance of a conductor is proportional to its length. Similarly, in OTFTs, the channel resistance is proportional to the channel length, therefore decreasing the length reduces channel resistance, resulting in an increase in drain current flow. Narrow- and wide-gate devices saw a total increase of 118 % and 136 % respectively, over twice their initial values. Wide-gate transistors displayed the highest increase due to larger *W/L* ratio. The on-state drain current however exhibited a gradual reduction (where a constant dependence is expected) when its dependence on channel dimensions was removed. In this scenario, the presence of contact resistance between the source/drain contacts and DNTT semiconductor may explain the reduction in on-state drain current. Shorter channel lengths are prone to dominant contact resistance as a result of significantly reduced channel resistance. Therefore, the current decreases as a result of a dominant contact resistance.

The field-effect mobility displayed a reduction as *W/L* was increased and the channel length was decreased. In narrow-gate devices, the mobility decreased by a total of ~ 51 % from the initial value of 0.35 $cm^2/V{\cdot}s$. Similarly, wide-gate transistors saw a reduction of ~ 58 % from the initial value of 0.41 $cm^2/V{\cdot}s$. The mobility of a device can be influenced by a number of variables including thermal effects, choice of semiconductor material, defects, impurity, channel length and the fabrication techniques. Here, the reduction in both groups of devices is attributed to the variation in channel dimensions. In short channel devices, the channel resistance R_{CH} is significantly reduced proportionally to channel length, therefore the contact resistance R_C at the drain and source interfaces becomes dominant ($R_{CH} < R_C$), in turn hindering mobility. In long channel transistors, the channel resistance dominates the contact resistance and consequently the latter can be often neglected due to minor influence on performance. The results shown are consistent with other published findings on mobility behaviour due to contact resistance [4.11,4.12].

Regarding the threshold voltage, V_{TH} rises with decreasing *L* to a total increase of 36 % and 55 % for narrow- and wide-gate devices, respectively. The trend observed in both narrow- and wide-gate devices suggest the effect of threshold voltage roll-off. Threshold roll-off is a short channel effect where a decrease in threshold voltage is observed for a decrease in channel length due to reduction of charges as a result of reduced channel length [4.13-4.15]. However, the results reported here contradict the reviewed literature. In agreement with our results, [4.12] reported an increase in threshold voltage from ~ 0.5 to ~ 1.5 V as channel length decreased from 100 to 5 μm in pentacene thin-film transistor. The results obtained here indicate that for a constant voltage bias, transistors with smaller dimensions experience significantly greater

charge trapping, therefore requiring larger voltage to turn on the devices, i.e., larger threshold voltage is needed. [4.16] reported an increased threshold voltage at shorter channel lengths in amorphous-indium-gallium-zinc-oxide thin-film transistors, attributing the effect on carrier diffusion from the n^+ doped source and drain a-IGZO regions to the intrinsic a-IGZO channel.

The off-state drain current results showed no dependence on channel length for wide-gate devices but exhibited a gradual increase in narrow-gate transistors. At shorter channel lengths the effect is due to short channel effects such as drain-induced barrier lowering [4.17]. Shorter channel lengths result in a reduced channel resistance and therefore increased off-state current. Subsequent investigation revealed a valuable dependence on channel width for wide-gate transistors. Transistors with full gate width i.e., W = 18.23 mm, displayed significantly reduced off-state drain current as low as 1.45×10^{-14} A when normalised with transistor channel dimensions. This is significant and implies better device control through reduced power loss due to reduced leakage when the device is in the off-state.

The sub-threshold slope followed different trends for narrow-gate and wide-gate devices. In narrow-gate OTFTs (L < 20 μm), the subthreshold slope increased with decreasing channel length. However, wide-gate OTFTs (L = 20 to 50 μm) displayed the opposite effects of a decreasing dependence on channel length. Narrow-gate transistor with L = 10 and 20 μm showed a consistently reduced average subthreshold slope of 102±4 mV/decade compared to other channel lengths with considerably higher and more spread distributions.

The use of interdigitated source/drain contacts to increase *W/L* ratio on six devices saw an increase from 202 to 524 and resulted in AC transconductance from 26 to 56 μS, respectively. As expected, the AC transconductance was also shown to directly depend on $1/L$. Narrow-gate transistors displayed lower g_m with the exception of one device which displayed the highest overall g_m due to its very short channel length. Wide-gate devices displayed a higher g_m and were also shown to have a steeper rise compared to narrow-gate transistors.

4.7 Summary

The behaviour of DNTT based organic thin-film transistor on PEN when channel dimensions are altered was studied. The study revealed that almost all transistor parameters are influenced by either the channel length or channel width. Therefore, great consideration should be taken when deciding suitable channel dimensions. In this study, the *W/L* ratio was increased by a few orders of magnitude while maintaining similar transistors dimension. As a result, improvement in the on-state drain current lead to significant improvement in the AC transconductance. Transistor parameters such as field-effect mobility and threshold voltage were shown to be negatively affected with decreasing channel lengths, while parameters such as gate leakage current saw no dependence on channel length or channel width. Narrow-gate OTFTs with channel lengths between 10 and 20 μm experienced the best subthreshold slope.

For future sensor development, the wide-gate transistors with transistor channel placed fully above the gate line are the best option. Consequently, the following chapters investigate these transistors further.

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Chapter 5

Bias stress effect in DNTT organic thin-film transistors

It is well-known that organic thin-film transistors under prolonged application of voltages are likely to change their performance, i.e. they suffer from bias stress instability. This Chapter investigates the effect of bias stress on low-voltage, high drain current organic thin-film transistors on polyethylene naphthalate foils. Section 5.1 reviews the literature with respect to bias stress and describes the purpose of the investigation. Section 5.2 outlines the experimental details used in investigating the bias stress effect on DNTT OTFTs. Sections 5.3 details the results and Section 5.4 discusses the experimental observations and their significance for flexible sensor development. Section 5.5 summarises the investigations and observations.

5.1 Introduction to bias stress effects

Many reports on OTFT bias stress instability have been published in the past two decades. Much of the early research focused on instabilities caused by environments that led to degradation in OTFT performance. Oxygen, moisture, illumination, temperature, and humidity were the main causes of such environmental degradation [5.1-5.3].

Kim *et al*. reported successful suppression of moisture and oxygen adsorption in pentacene OTFTs encapsulated with transparent SnO_2. The protected devices showed retention of 0.5 cm^2/Vs field-effect mobility sustained for 1 month before gradually degrading to 0.35 cm^2/Vs after 100 days of aging in ambient air. In addition, their on/off current ratio was in excess of 10^5. The field-effect mobility of the non-encapsulated transistors was three times lower and their on/off current ratio was ~10^4 [5.4].

Environmental instability caused by the choice of material and thickness of the active semiconductor layer has also been reported. Choi *et al*. reported significant degradation in the drain current and field-effect mobility of a printed pentacene OTFT when the thickness of the active layer was decreased from 1 μm to 50 nm and the transistors were exposed to ambient air for 1,400 hours. Their investigation concluded that the thicker active layer protected the channel against H_2O and O_2 diffusion, thus preventing the creation of new charge carrier trapping sites and consequently slowing down the environmental degradation [5.5].

The use of non-polar and/or hydrophobic dielectrics materials has also led to transistors with improved environmental stability. Baek *et al*. studied fluorinated polyimide as the gate dielectric material in pentacene OTFTs. Such OTFTs showed better crystallinity of the organic semiconductor preventing the creation of trapping sites at the semiconductor/dielectric interface, and thus leading to improved electrical stability, when compared to transistors with non-fluorinated polyimide in N_2 and ambient air [5.6]. Wei *et al*. reported similar enhanced surface hydrophobicity using fluorinated polyimides which prevented charge trapping [5.7].

As the OTFT performance improved and the transistors became viable for new, applications, the focus shifted from the environmental to the electrical stability of OTFTs. Viz., operational degradation that occurred while the transistors were turned on. This operational instability is known as the "bias-stress effect".

OTFTs exhibit bias-stress while under voltage, i.e. bias, conditions for prolonged time, i.e. their performance changes when voltages are applied on their terminals. The mechanism of the bias-stress in OTFTs has been linked to charge trapping in the organic semiconductor, gate dielectric or at the gate dielectric/semiconductor interface [5.8]. This charge trapping causes a reduction in the drain current and a time-dependent shift of the threshold voltage [5.9]. A stretched-exponential function is often used to describe the kinetics of these changes [5.10]. Common findings show correlation with the magnitude and polarity of V_{GS} and V_{DS}, stress time, choice of semiconductor and gate dielectric.

Fukuda *et al*. reported a reversal in the threshold voltage under DC bias stress in OTFTs using polychloro-p-xylylene as the gate dielectric, i.e. a positive threshold

voltage shift under a negative DC gate-source voltage. They found that the degree of positive shift during bias stress was proportional to the annealing temperature of the polychloro-p-xylylene. Higher temperatures led to higher positive shift and vice versa [5.11].

Bias-stress instability has been linked to contact resistance in pentacene OTFTs [5.12]. The contact resistance was found to increase continuously with increasing stress time.

AC bias stress was reported for poly(quarterthiophene) organic transistors using square pulses with repetition time of up to 100 ms and varied duty cycle [3.7]. The authors observed that the transistor recovery exhibited short- (charge carriers trapped in shallow traps) and long-lived (charge carriers trapped in deep traps) components.

To date, researchers continue to explore the changes associated with OTFTs under bias stress, though most studies are conducted under fixed (DC) V_{GS} and V_{DS} voltages and the application of alternating voltages (AC) is under-reported. The work presented in the Chapter investigates the bias stress effect of DNTT OTFTs under a range of AC pulse. The focus is on low-voltage pulses with low repetition rate, applicable to flexible sensors that do not demand continues data collection i.e. it examines the effect of spending less time in the on-state and more time in the off-state. The effect of long-term storage of the transistors in dark ambient atmosphere is also investigated.

5.2 Experimental details

Following the fabrication procedure prescribed in Chapter 3, five transistors composed of 30-nm thick Al (gate electrode), bi-layer of 15-nm thick AlO_x and 2-nm $C_{18}PA$ (insulating gate dielectric), 25-nm-thick DNTT (organic semiconductor) and 50-nm thick Au (drain and source electrodes) were selected for the bias stress characterisation. Four additional transistors (stored in dark ambient atmosphere for 5-6 months) were selected to investigate the impact of aging on the bias stress instability compared to freshly fabricated devices. A source-drain mask with interdigitated contacts (see Figure 3.12 and 4.1) was used to provide transistors with high on-state drain current. The transistors possess a low turn-on voltage, high transconductance and hysteresis-free characteristics (see Chapter 4) making them suitable for the bias stress experiments.

Investigation of bias stress was performed using Agilent B1500A semiconductor device parameter analyser and semiconductor pulse generator unit (SPGU). Five waveforms for biasing the transistors were generated including four unipolar AC pulses and one DC bias. The OTFT on-state drain current (at $V_{GS} = V_{DS} = -2$ V) was continuously monitored, while the remaining transistor parameters were extracted from the OTFT transfer characteristics measured at $V_{DS} = -2$ V. The initial transfer characteristic was measured before the bias stress commenced. Each bias stress consisted of 1000 pulses and the bias stress was periodically interrupted after every 100 pulses to re-measure the OTFT transfer characteristic. All pulses have a fixed transistor turn-on time of 1s and varied turn-off time from 0 s to 59 s, corresponding to pulse periods T from 5 to 60 s. Therefore, the only difference is the

length of time the transistor is turned off, while all transistors underwent the same net stress time of 1000 s. In addition, one transistor was subjected to a DC bias stress for comparison. DC bias stress was performed at V_{GS} = V_{DS} = −2 V (the source was grounded) for 1000 s, equivalent to a 'pulsed' bias stress with T = 1 s with turn-on time of 1 s and turn-off time of zero. The turn-on and turn-off times are defined as the times the transistor spends in either the on- or off-state respectively. Net bias stress time refers to the total, accumulated turn-on time, i.e. the time spent by the OTFT in the on-state. Figure 5.1 shows the applied AC pulses.

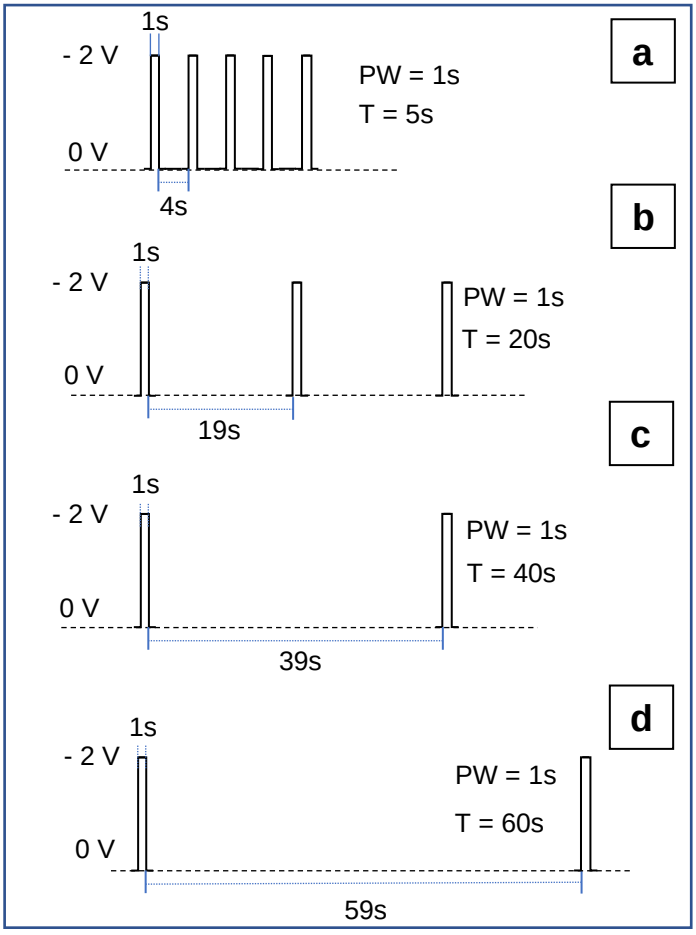

Figure 5.1: AC pulse signals with 1-s-pulse width (PW), on-state and off-state voltages of −2 V and 0 V, and period (T) of 5s (a), 20s (b), 40s (c) and 60s (d). During the bias stress the same pulse was applied to the gate and drain of the transistor.

5.3 Bias stress effect in fresh and aged transistors

The degradation of transistor parameters due to bias stress is detailed in this section. Various transistor parameters are investigated as a function of net bias stress time for different pulse periods T and fitted with stretched-exponential functions described by Equations (3.7)-(3.9). Sections 5.3.1-5.3.6 discusses the standard and normalised on-state drain current, threshold voltage shift and the field-effect mobility in freshly fabricated transistors. Section 5.3.7 explores the impact of long-term aging of the transistors in a dark ambient atmosphere and the effect on such aging on the AC bias stress.

Figures 5.2, 5.3 and 5.4 show data from freshly fabricated transistors measured with T = DC, 5 s, 20 s and 60 s as a function of the net bias stress time. Figures 5.5, 5.6 and 5.7 show the normalised data from Figures 5.2-5.4, showing the measured data (symbols) with the solid lines as the stretched-exponential fits with fitting parameters of β and τ. The stretched-exponential fitting was applied to normalised data only. Figures 5.8, 5.9, and 5.10 correspond to OTFTs aged for 5-6 months in dark ambient atmosphere and bias stressed with T = 20, 40 and 60 s.

5.3.1 On-state drain current

Figure 5.2 shows the transistor on-state drain current I_{ON} as a function of net bias stress time. A decrease in I_{ON} is observed as bias stress time is increased. The rate of decrease is observed to vary with T, although DC bias stress shows a slightly different behaviour. In the first instance, an initial increase of ~ 1.6% is observed in the early stages of bias stressing, then followed by a decrease of ~ 3.2% from its initial

value. For T = 5 s and 60 s a reduction in drain current of approximately 6-7% is shown, followed by ~11% drop for T = 20 s.

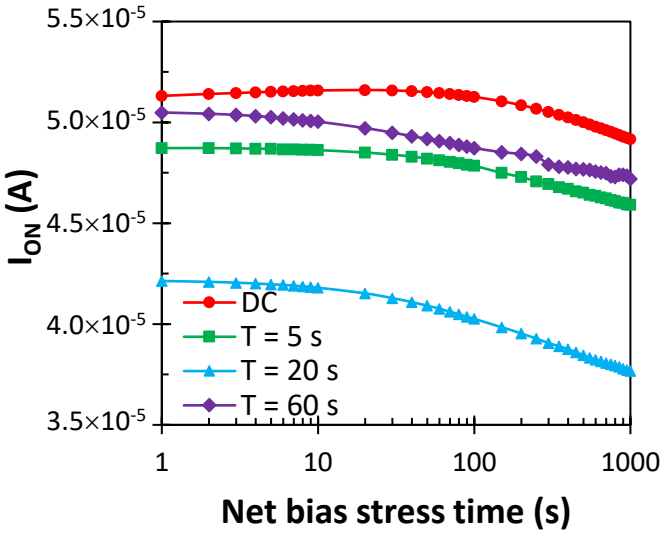

Figure 5.2: On-state drain current I_{ON} as a function of net bias stress time for DC (circles), and AC pulse periods with 1 s on-time and periods; T = 5 s (square), 20 s (triangles) and 60 s (diamonds).

5.3.2 Threshold voltage

Figure 5.3 shows an increase in the threshold voltage with increasing bias stress time for all stress conditions. For pulse periods T = 5 to 60 s, the largest change is observed in the first 100 s of stressing, followed by a gradual increase to 1000 s. Under DC bias a total increase of 10% is observed, T = 5 s displayed an increase of ~ 9%, followed by T = 20 s with an increase of 19% and lastly 17% for T = 60s. Noticeably, the threshold voltage at the final bias stress period shows similar shifts for both T = 5 s and 20 s.

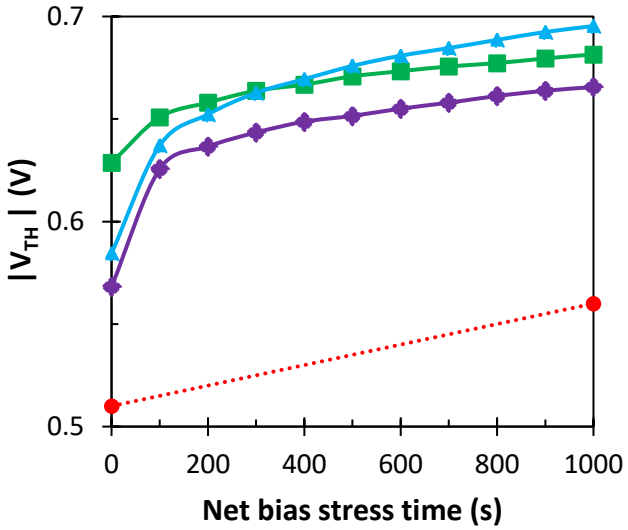

Figure 5.3: Threshold voltage V_{TH} as a function of net bias stress time. The legend of Figure 5.2 applies.

5.3.3 Field-effect mobility

Figure 5.4 shows the field-effect mobility as a function of net bias stress time. The field-effect mobility shows almost no change for bias stress with T = 5 s. T = 20 s and 60 s show an increase in the field-effect mobility of 3.4% and 6.6%, respectively. In these cases, a rapid increase for short stress time is followed by a slower increase for longer times. Contrary to this, the DC bias stress produces a reduction in the mobility of about 4%.

5.3.4 Normalised on-state drain current $\frac{I_{ON}(t)}{I_{ON}(0)}$

Figure 5.5 shows the normalised on-state drain current of freshly fabricated OTFTs fitted to Equation 3.7 and plotted as a function of net bias stress time lasting

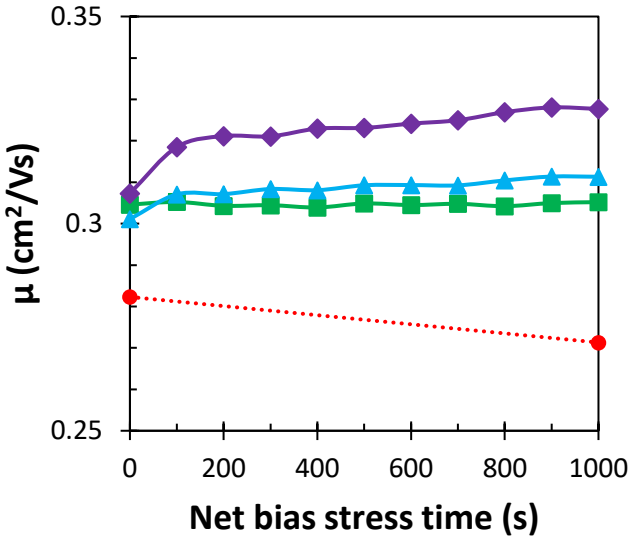

Figure 5.4: Field-effect mobility μ as a function of net bias stress time. The legend of Fig. 5.2 applies.

for 1000 s. OTFT under DC bias stress experienced an initial increase of 1.6% in the on-state drain current, followed by a 3.2% decrease from its initial value. The stretched-exponential function of Equation 3.7 cannot model this behaviour and the stretching parameter $\beta_{I_{ON}}$ was set to 1, the maximum value. For the bias stress under square pulses, from T = 5 s to 60 s, the steady-state values for $t \rightarrow \infty$ were 0.93, 0.87 and 0.92 respectively and reductions in $\tau_{I_{ON}}$ and $\beta_{I_{ON}}$ were observed. The time constant decreased from 394 to 338 to 202 s and the stretching parameter from 0.74 to 0.60 to 0.45. The final steady-state values corresponding to DC and T = 60 s bias stress showed a difference of only 7% even though the DC bias stress corresponds to real-time measurement of 1000 s (≈ 17 minutes) and the pulsed bias stress with T = 60 s is equivalent to the total measurement time of 60000 s (≈ 17 hours).

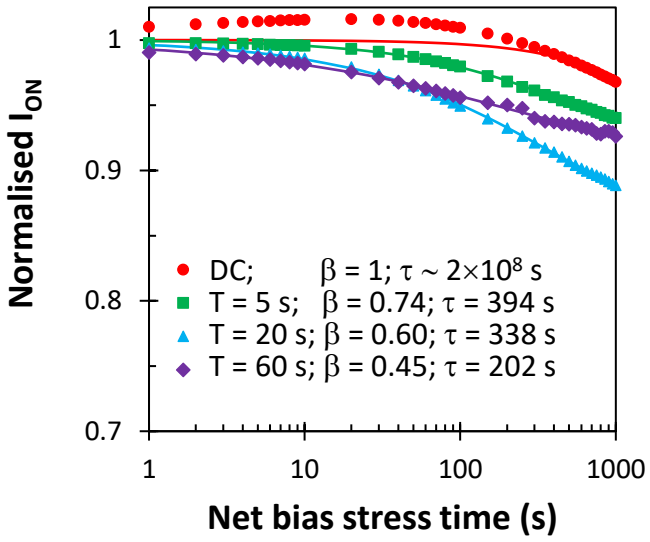

Figure 5.5: Normalised on-state drain current of freshly fabricated OTFTs as a function of net bias stress time. Points (symbols) represent measured data and lines are the stretched exponential fits with fitting parameters of β and τ.

5.3.5 Threshold voltage shift $|\Delta V_{TH}|$

Figure 5.6 shows the measured threshold voltage shift $|\Delta V_{TH}|$ and the corresponding stretched exponential fit using Equation 3.8, as a function of the net bias stress time for T = 5, 20, 60 s. The initial and final values of the DC bias stress are also shown for comparison. The threshold voltage increases in all cases. A short net bias stress time displayed the quickest increase in the threshold voltage, with higher T displaying larger shifts. The shift in the threshold voltage slows down for longer stress times. After 1000 s of net bias stress, the pulses with T = 5 s lead to an increase in $|V_{TH}|$ of about 50 mV (similar to DC bias stress), followed by T = 60 s bias stress with $|\Delta V_{TH}|$ of ~ 100 mV, and T = 20 s with $|\Delta V_{TH}|$ of ~ 110 mV. The corresponding steady-state values at $t \rightarrow \infty$ are 86, 164 and 144 mV, with increasing T. Both the τ_{V_T} and β_{V_T}

decrease with increasing T. The τ_{V_T} decreased from 1140 to 780 to 732 and β_{V_T} from 0.50 to 0.46 to 0.34.

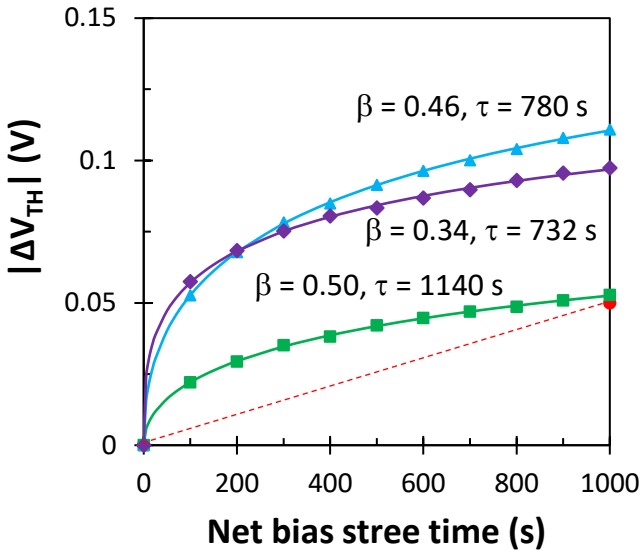

Figure 5.6: Threshold voltage shift of freshly fabricated OTFTs as a function of net bias stress time. The legend of Fig. 5.5 applies.

5.3.6 Normalised field-effect mobility $\frac{\mu(\mathbf{t})}{\mu(\mathbf{0})}$

Figure 5.7 shows the normalised field-effect mobility as a function of net bias stress time and the stretched-exponential fits using Equation 3.9. For the DC bias stress the starting and final values are shown for comparison. The DC bias shows a reduction of about 4% in the normalised mobility when compared to the pulsed bias stress. All AC bias stress conditions led to an increase in the mobility and this increase was higher for larger T. T = 5 s led to no change in the mobility. Increase in the pulse period to T = 20 s and then T = 60 s showed an increase of 3.4% and 6.6%, respectively. As T increased from 5 to 60 s, the normalised steady-state value for $t \rightarrow \infty$ increased from 1.00 to 1.10 and 1.46, respectively. At the same time τ_{μ} increased from 2.88 x 10^3 to

5.76 x 10^5, while β_μ decreased from 0.76 to 0.29. Longer off-state times exhibited larger increase in the field-effect mobility.

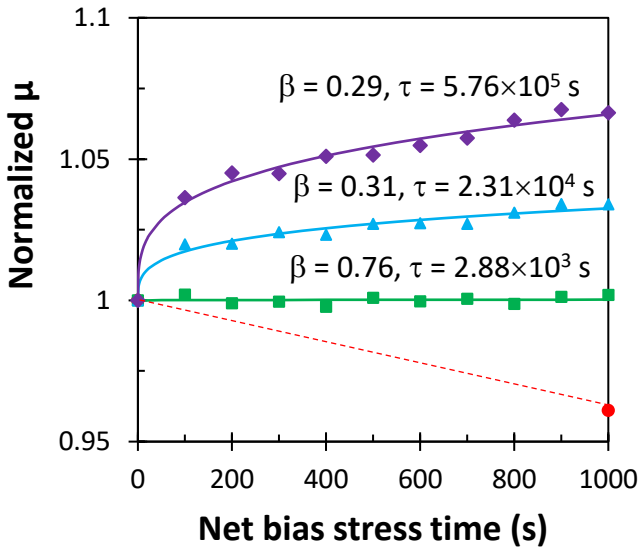

Figure 5.7: Normalised filed-effect mobility of freshly fabricated OTFTs as a function of net bias stress time. The legend of Fig. 5.5 applies.

5.3.7 Effect of environmental aging

Figures 5.8, 5.9 and 5.10 show the normalised on-state drain current, threshold voltage shift and normalised field-effect mobility for transistors 'aged' for 5-6 months in dark ambient air and then measured with pulse periods of 20, 40 and 60 s. Two transistors were bias stressed for T = 40 s to check the reproducibility. The stretched-exponential functions were again fitted to the data; however, the mobility fits should be regarded with caution due to the larger scatter in the measured data.

Results show that the degradation of the on-state drain current proceeds faster; yet, there is a clear sign that the drain current reaches a steady-state value within ~ 500 s. These values are 0.90 for T = 20 s, 0.84 for both measurements at T = 40 s and 0.87

for T = 60 s. These values are up to 6% smaller than those of fresh transistors. In addition, all time constants are reduced, and the stretching parameters increased.

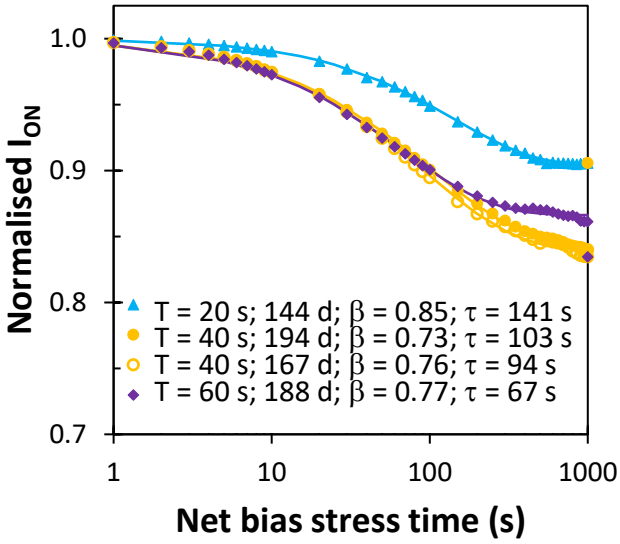

Figure 5.8: Normalised on-state drain current of 5-6 months aged OTFTs as a function of net bias stress time.

Figure 5.9 shows an increase in the threshold voltage for all bias pulses. Again, T = 60 s shows smaller $|\Delta V_{TH}|$ when compared to T = 40 s. The steady-state values at $t \rightarrow \infty$ are 0.11 for T = 20 s, 0.17/0.19 for T = 40 s, and 0.16 for T = 60 s, all slightly higher when compared to the data of Figure 5.6. Furthermore, all time constants are reduced and stretching parameters increased when compared to fresh OTFTs stressed with similar bias pulses.

Finally, Figure 5.10 shows an increase in normalized mobility for all pulses. The total increase in the mobility is somewhat similar to that of Figure 5.7 and larger T led to a bigger increase. Also, there is an indication that the stretching parameters are bigger than 0.5.

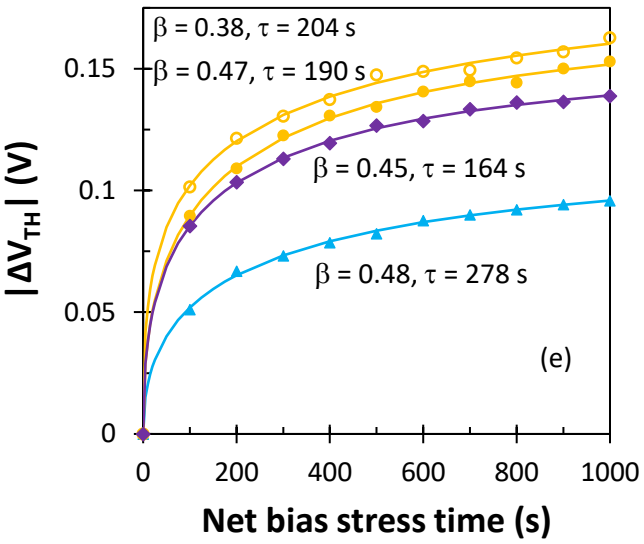

Figure 5.9: Threshold voltage shift of 5-6 months aged OTFTs as a function of net bias stress time. The legend of Fig. 5.8 applies.

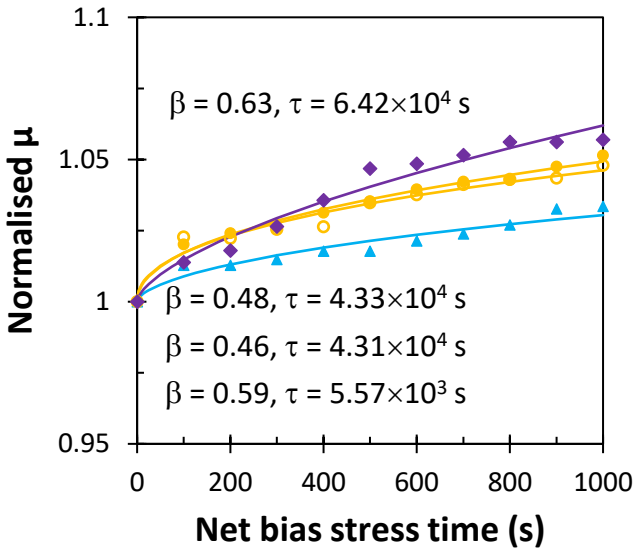

Figure 5.10: Normalised field-effect mobility of 5-6 months aged OTFTs as a function of net bias stress time. The legend of Fig. 5.8 applies.

5.4 Discussion

Degradation in the transistor's drain current occurs regardless of the pulsed bias stress condition or transistor age. However, the rate of decay was shown to be

slower in newly fabricated transistors compared to aged transistors. However, aged transistors reach stabilisation faster, at approximately half of the bias stress time. The kinetics of the drain current decay clearly depends on the bias stress pulse period and transistor history (fresh versus the aged transistors).

The change in the drain current originates from the combined effects of changes in the threshold voltage and field-effect mobility. Figure 5.11 shows the changes in the normalised on-state drain current, threshold voltage shift and normalized field-effect mobility after 1000 stress pulses as a function of the pulse period T or measurement/lapsed time. The reference points are the corresponding values before the bias stress. The pink symbol in Figure 5.11(a) is an exception and represents the change in the drain current from its maximum value for DC bias stress. For shorter measurement time (smaller T) the value of the normalized on-state drain current after 1000 cycles decreases linearly with T, and stabilized/reduced for T = 60 s. The value of the threshold voltage shift after 1000 cycles increased linearly with T and reduced/stabilized for T = 60 s. However, the normalized drain current and $|\Delta V_T|$ at T = 60 s depended on the age of the transistors, leading to bigger changes for aged transistors. Finally, the value of the field-effect mobility after 1000 cycles increased logarithmically with the measurement time and all transistors followed the same behaviour regardless of their age. Consequently, the mobility improvement is associated with the measurement time and T = 60 s leads to the biggest improvement regardless of the transistor age.

The charge carrier accumulation in p-channel thin-film transistors (on application of a negative gate bias) leads to conduction channel formation. Prolonged

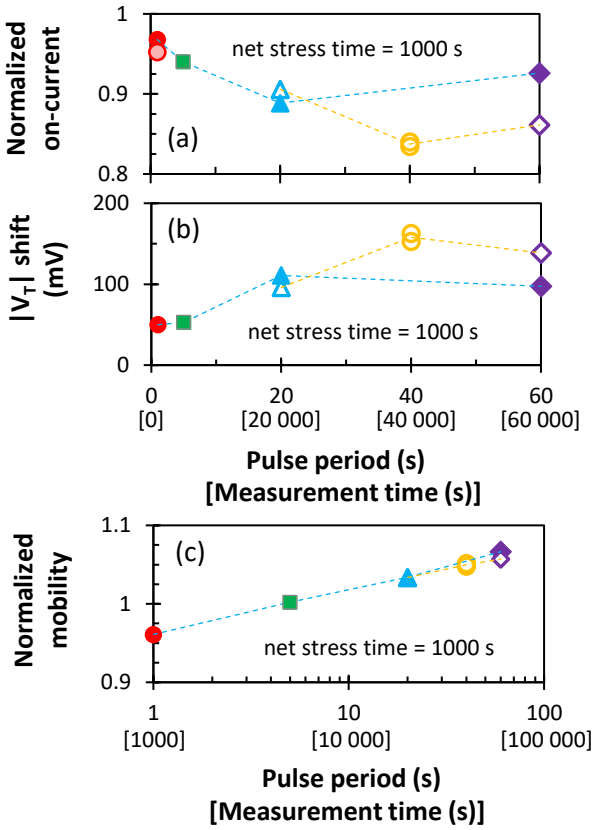

Figure 5.11: Normalized on-state drain current (a), threshold voltage shift (b) and normalized field-effect mobility (c) versus the pulse period T or measurement/lapsed time, for net bias stress of 1000 s. DC bias stress is represented as T = 1 s. Full and empty symbols correspond to the fresh and aged transistors. The light and dark blue dashed lines connect the measurements from fresh and aged transistors respectively. The pink symbol in (a) shows the change in drain current from its maximum value for DC bias stress.

application of the gate bias results in the increased trapping of charge carriers into localised states (at the semiconductor/dielectric interface) and thus causes the increase or shift in the threshold voltage away from 0 V, i.e. towards more negative values [5.13]. If the bias stress does not cause additional change in the field-effect mobility and subthreshold, this threshold voltage shift would result in a reduced on-state drain current (in this case $V_{GS} = V_{DS} = -2$ V). However, the concurrent increase in the field-effect mobility, would manifest itself as an increase in the on-state drain current, thus counteracting the effect of the threshold voltage. Therefore, if the field-effect mobility

increases faster than the threshold voltage, an increase in the on-state drain current may be observed. For the reversed situation, i.e. the threshold voltage increases faster than the field-effect mobility, a decrease in the on-state drain current results. However, if the rise in field-effect mobility 'compensates' the rise in the threshold voltage, a stable on-state drain current may result. To date, all three cases of the on-state drain current behaviour have been observed, although no explanation was offered. Figure 5.8 shows that the on-state drain current of the aged transistors stabilises after 500 s of net bias stress time, while the field-effect mobility and threshold voltage continue to increase (although at a slowing rate), suggesting that the observed steady on-state drain current is the outcome of the field-effect mobility 'compensating' the threshold voltage shift.

For all transistors the improvement in the field-effect mobility is related to T, i.e. a larger increase in the mobility is observed for longer T. The initial stages of the DC bias stress was accompanied by an increase in the on-state drain current (the first ~ 200 seconds of net bias stress time). However, the comparison of the before- and after-stress transfer characteristics shows an overall decrease in mobility and thus the mobility cannot offset the increase in $|V_{TH}|$. Similar behaviour of the on-state drain current under DC bias stress was previously reported for OTFTs based on DNTT and DNTT-derivatives and the initial increase in the drain current was attributed to a decrease in the contact resistance [5.9]. For T = 5 s the on-state drain current is more or less constant for about 10 seconds and then decreases by 6.0% in 20000 seconds (1000 s of net bias stress), resulting from a relatively slow and minor increase in $|V_{TH}|$ and no change in the field-effect mobility. The biggest overall drop of 11.1% in the on-state drain current in 40000 seconds (1000 s of net bias stress) is observed for T =

20 s as a consequence of the largest increase in $|V_{TH}|$ offset by a small increase in the mobility. When T reaches 60 s, the increase in $|V_{TH}|$ becomes smaller and the increase in the mobility becomes more significant, leading to a 7.4% drop in the on-state drain current after 60000 seconds (1000 s of net bias stress). This decrease in the drain current is comparable to that obtained for T = 5 s; yet the overall measurement time has increased by a factor of 12. This qualitative behaviour is replicated for the aged transistors, except in this case, the data was also collected for T = 40 s at which value the threshold voltage shift reaches its maximum.

T = 60 s bias stress represents a favourable stress condition shown by a reduction in threshold voltage shift and largest field-effect mobility improvement in both fresh and aged transistors, thus leading to less degradation in the on-state drain current. Additionally, for 'fresh' transistors, T = 60 s is the only bias stress condition that shows signs of on-state drain current stabilisation when the net stress time approaches 1000 s. Consequently, T = 60 s may be a suitable measurement regime for sensor systems within infrequent data collection applications.

5.5 Summary

The electrical stability of low-voltage DNTT transistors with high on-state drain current under DC and AC (on/off square pulses) bias stress was investigated. The chosen bias stress conditions forced the transistor either to operate in the saturation regime (desirable for the sensor) or be turned off. During each AC bias stress the transistor was repeatedly turned on for 1 s while the turn-off time was either 4, 19, 39 or 59 s, providing 4 different AC waveforms with T = 5 s, 20 s, 40 s and 60 s. The on-

state drain current of the transistor was measured; as were the changes in the threshold voltage, field-effect mobility, and subthreshold slope. The total net stress time was 1000 s for the DC and all AC bias stresses. Under the DC bias stress, an initial increase in the on-state drain current was followed by a gradual decrease, leading to an overall drop of 3.2%. The $|V_T|$ exhibited a small increase and the mobility a small decrease. The net stress time of 1000 s led to a somewhat larger degradation of the on-state drain current for all AC pulses and the degradation proceeded faster and stabilized after 500 s of net bias stress for aged transistors. For all transistors, the drop in the on-state drain current and the shift in the threshold voltage reached maxima for medium values of T (T = 20 s and 40 s), thus leading to slightly reduced degradation for T = 60 s. Finally, the field-effect mobility gradually increased with T, leading to the largest enhancement for T = 60 s regardless of the transistor age. The value of the normalized field-effect mobility after 1000 cycles increased logarithmically with the measurement time. The improvement in mobility is dependent on the measurement time and the application of the intermittent voltages is beneficial.

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Chapter 6

Temperature sensor based on OTFT

OTFTs have found many uses to date due to their unique material properties. The Chapter explores a temperature sensor with an OTFT configured as a common source amplifier for signal conversion and amplification and a thermistor as the temperature sensing element. Introduction to the temperature sensor, the role and benefits of organic electronics in temperature sensing for medical monitoring is detailed in Section 6.1. The circuit design and experimental procedure performed to investigate the temperature sensor performance are discussed in Section 6.2. Section 6.3 describes the results obtained and Section 6.3 demonstrates a DC compact model of the transistor and the sensor. Section 6.4 discusses results and, finally, Section 6.5 summarises the main findings.

6.1 Introduction

Unique properties of organic electronics has stimulated attention amongst researchers over the last few decades. Recent developments and commercial applications emerging from such research take advantage of attributes such as compatibility with plastics and even fabric substrates, low-cost, low-temperature and large-area fabrication, material application via printing, and adaptability to new form factors. Consequently, organic electronics is becoming an enabler for wearable applications and robotic skin [6.1-6.4]. While most inorganic state-of-the-art devices have limited flexibility and biocompatibility, much of the growing attention has been focused on the adaptation of organic devices in fitness and healthcare [6.5, 6.6] where such devices have been shown to provide bio-sensing solutions in real-time point-of-care environments [6.7].

The maturity level of organic transistors based on several conjugated organics materials has spurred sensor developments [6.8-6.10]. Successful implementation of organic transistors in sensors have stimulated demands for automobile and smart devices. Among various sensing applications, temperature monitoring using organic electronics is lagging. To date, much of the attention has focused on sensing of touch, pressure, or force for robotic applications and health monitoring [6.10-6.13], although several temperature monitoring approaches have been reported. These include formation of organic diodes [6.8], operation of the organic transistors in the subthreshold regime [6.14], and development of temperature-sensitive transistors [6.15-6.18].

Temperature sensors are required in various sectors, for example in industrial and commercial control systems in oil and gas explorations, in meteorology for weather and climate change, in healthcare for body temperature monitoring, and home/office radiators for air temperature control. Depending on the end-application, commercially available thermometers, thermistors, thermocouples and RTDs as well as unconventional sensors based on piezoelectrics, fibre-optics, infrared or wearable organic electronics have been used [6.19-6.24].

The implementation of the organic transistors for temperature sensing primarily focuses on body temperature monitoring. When implemented as a stand-alone sensor, the role of the transistor is to respond to changes in physical stimuli [2.13]. Alternatively, when embedded as part of the sensor, the OTFT would respond to electrical stimuli and operate as a signal amplifier for strengthening weak signals produced by physical stimuli. The aforementioned OTFT attributes, particularly small dimensions, mechanical flexibility and low-voltage operation are advantageous in this context.

The work presented in the Chapter focuses on the demonstration of a temperature sensor where a low-voltage organic transistor provides signal amplification. Utilising the OTFTs presented in previous chapters which show high on-state drain current and low-voltage and hysteresis-free operation that many existing OTFTs struggle to achieve as a result of thick gate dielectric, low carrier mobility, high threshold voltage and interfacial defects.

This Chapter evaluates a simple application of such OTFTs for sensing body or ambient office temperature. The proposed sensor has the potential of full integration

on the same flexible PEN substrate, although that is not demonstrated. The work however lays the foundation for future developments of fully flexible sensors based on organic transistors. The organic transistor acts as a first stage of signal processing by amplifying the signal from a commercial thermistor and providing an output voltage signal in preparation for the next stages of signal processing. The proposed application is just one way of implementing the OTFTs reported in the thesis. A similar approach can be used with other sensors where amplification of the signal resulting from a physical stimuli may be required directly at the sensing site.

6.2 Experimental details

This section describes the construction, experimental setup, measurement methods and evaluation of the temperature sensor system by calculation, testing and simulation.

6.2.1 Transistor fabrication

Two organic transistors with high on-state drain current at gate and drain voltages of −2 V fabricated on polyethylene naphthalate foils were selected to respond to changes in temperature and raise the sensitivity of the sensor. To achieve voltage-amplification, two low-voltage bottom-gate top-contact p-type organic thin-film transistors based on DNTT were prepared following the fabrication procedure outlined in Chapter 3. Low-voltage operation was achieved using a thin, bi-layer gate dielectric (total thickness of 17 nm) consisting of aluminium oxide AlO_x prepared by UV/ozone oxidation [6.25] and an octadecyl phosphonic acid $C_{18}PA$ monolayer prepared in

vacuum [3.2]. Transistors with W = 18.23 mm were used to obtain the best parameters. In addition, a thicker Au layer of 80 nm was used for the source/drain contacts to reduce the contact resistance, V_{TH}, and provide a durable contact to circuit components.

6.2.2 Sensor circuit design and experimental setup

The temperature sensor system consists of two sections comprising a thermistor as the sensing element and an OTFT for signal amplification. The commercially-available thermistor with negative temperature coefficient (NTC) and nominal resistance of 100 kΩ at 25°C (Farnell, NTCLE100E3104J) responded to changes in temperature between 20 and 50°C. The organic transistor, having qualities of low-voltage operation and high on-state drain current, resulting from the ultra-thin gate dielectric and interdigitated source/drain electrode configuration [2.24], amplifies the changes in the thermistor resistance owing to the changing temperature.

The sensor schematic is shown in Figure 6.1. All resistive components and the thermistor were soldered onto a stripboard. Connections to the transistor terminals were subsequently formed via gold wires attached using conductive silver paste. The employment of a strip board meant that the sensor was not integrated; however, the physical separation of the transistor from the thermistor allowed exclusive heating of the thermistor, thus simplifying the analysis of the sensor data. The thermistor was placed on a Peltier element for temperature control via LabVIEW software. To provide optimum heat transfer, the thermistor was ‘embedded’ in thermally conductive paste. Operation of the sensor was analysed by applying a range of input voltages (V_{IN}) and supply voltages (V_{DD}) and monitoring the voltages on the gate and drain of the

transistor while simultaneously varying the temperature of the thermistor from 20 to 50°C in 5°C increments.

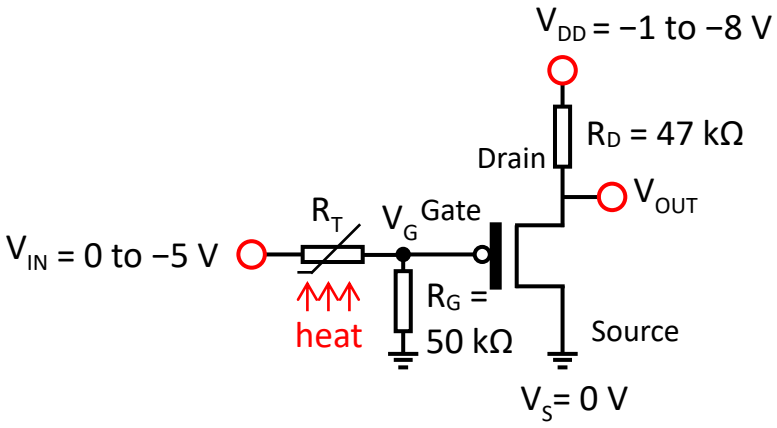

Figure 6.1: OTFT based temperature sensor. V_{IN} = 0 to −5 V, V_{DD} = −1 to −8 V, V_S = 0 V. R_T has nominal resistance of 100 kΩ at 25° C and R_D = 47 kΩ.

On the sensor, an input voltage V_{IN} (swept from 0 to −5 V) supplies the series connection of R_T and R_G. V_G drives the transistor with a fraction of V_{IN} on the gate terminal from the voltage division between R_T and R_G. The resistor (R_D) connects the drain terminal to the supply voltage V_{DD} (swept from−1 to −8 V) and the source terminal V_S is grounded (0 V).

V_{IN} and R_G determine the OTFT gate voltage V_G, which should be higher than the OTFT threshold voltage but sufficiently low to enable the saturation operation of the transistor without the need for excessive V_D = V_{OUT}. V_D is restricted by the breakdown voltage of the OTFT gate dielectric; the transistor bias stress instability has been observed to increase with rising V_G and lower V_G can accomplish stable sensor operation more easily; R_D controls the voltage gain of the transistor, i.e. the sensitivity of the sensor – a lower R_D leads to lower voltage gain but requires lower V_{DD} while a

higher R_D leads to higher gain but requires higher V_{DD}. A trade-off exists between the gain and the supply voltage V_{DD}.

Values of resistors R_G and R_D were obtained following an investigation to optimise the change in the resistance of the thermistor within the required temperature range. The resistance of R_G was calculated from extracting the resistance of R_T after subjecting the thermistor to a range of temperatures between 20 and 50°C (at 5°C increments). R_G was investigated in the range between 10 kΩ and 100 kΩ (in 10 kΩ increments), the aim being to produce the largest change in V_G while keeping it between −1 to −2 V. The value of R_D was selected to give sufficiently high output voltage V_{OUT} on the drain terminal, while keeping V_{DD} relatively low.

6.3 Results

This section reports on the results obtained following investigations of the proposed organic transistor-based temperature sensor. Investigations focused on obtaining the temperature-resistance response at a range of the transistor gate and drain voltages, detailed in Section 6.3.1. Section 6.3.2 focuses on the development of a DC compact transistor model, the basis for an overall sensor model.

6.3.1 Temperature sensor

6.3.1.1 Transistor transfer characteristics

Two transistors with different on-state drain current were tested in the temperature sensor; Figure 6.2 shows the transfer characteristics of the organic

transistors operating in both the linear (V_{DS} = 0.1 V) and saturation (V_{DS} = −2 V) regimes for V_{GS} ramped from 0 to −2 V and back and V_S = 0 V. The transistor in Figure 6.2(a) displayed a drain current of 61 μA at V_{DS} = V_{GS} = −2 V; the transistor in Figure 6.2(b) showed a higher drain current of 126 μA, owing to shorter L. The transistor parameters extracted from the transfer characteristics are shown in their respective

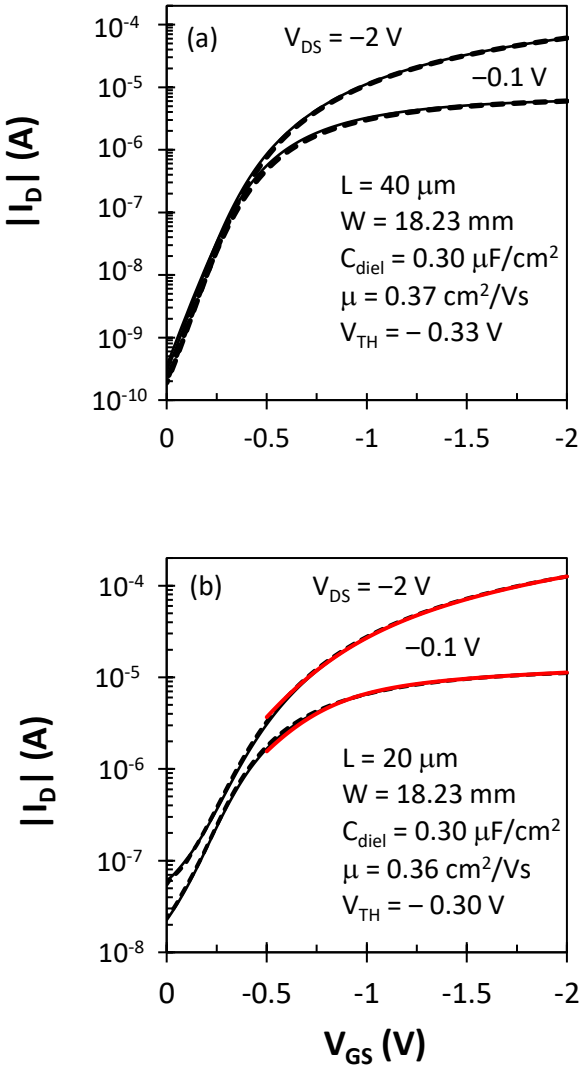

Figure 6.2: Transfer characteristics of OTFTs used in the temperature sensor and verification model. Solid black lines and dotted lines represent hysteresis for V_{GS} ramped in forward direction (0 to −2 V) and reverse (−2 to 0 V) respectively. Solid red lines represents the transistor model.

figures. The transfer characteristics show little-to-no hysteresis confirmed by the overlap between the solid and dashed lines. The solid red lines represent the simulated transistor drain current model discussed in the subsequent subsections.

6.3.1.2 Thermistor response

Figure 6.3 shows the thermistor response when subject to temperature changes between 20 and 50°C, showing that the thermistor resistance decreased non-linearly with increasing temperature. At 20°C, the thermistor displayed a resistance of 128 kΩ and ~34 kΩ at 50°C, a total change of ~94 kΩ. The result shows good agreement between the measured and calculated data obtained from the manufacturer's data sheet.

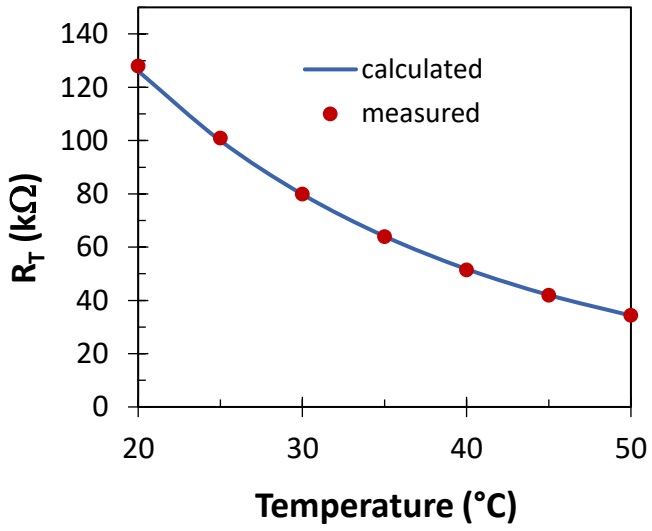

Figure 6.3: Temperature response of a thermistor having a nominal resistance of 100 kΩ at 25°C.

6.3.1.3 Effect of resistor R_G

Figure 6.4 shows the effects of resistor R_G on the gate voltage V_G for temperatures between 0 and 100°C. Keeping the transistor V_G voltage in the range

between –1 and –2 V (suitable for transistors with threshold voltage ~ –0.3 V), The relationship between R_G and the suitable temperature range can be inferred. Lower values of R_G are better suited for higher temperatures while higher values of R_G are needed for lower temperatures. For temperatures between 20 and 40°C, an R_G between 50 and 60 kΩ is desirable, taking advantage of the full range of acceptable V_G values. In addition, the change in V_G with temperature is linear; consequently, an R_G of 50 kΩ was selected for the sensor.

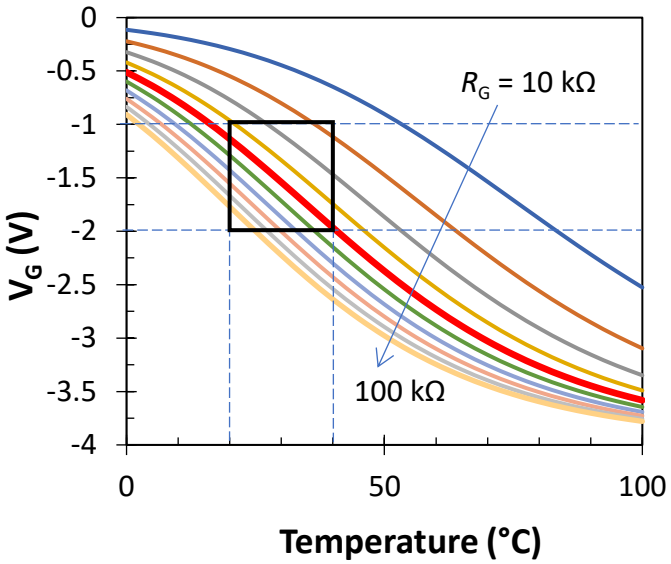

Figure 6.4: Effects of resistor R_G (10 k to 100 kΩ) on V_G as a function of temperature. The desirable temperature and voltage range for V_G are indicated by the black rectangle. The red thick curve corresponds to R_G = 50 kΩ. The results correspond to V_{IN} = −4 V.

6.3.1.4 Impact of temperature and V_{IN} on V_G

Figure 6.5 demonstrates the effect of V_{IN} and thermistor temperature on the transistor gate voltage V_G. V_{IN} was swept from 0 to −5 V while the thermistor was held at a constant temperature and V_G was monitored. The temperature of the thermistor was gradually increased in 5°C increments from 20 to 50°C, for each V_{IN} sweep. As

expected, the results reveal a linear dependence of V_G on V_{IN} for each temperature. Higher temperature resulted in a stronger response of V_G to changes in V_{IN}. At 20°C the overall change in V_G is ~1.4 V while at 50°C the change is ~3 V.

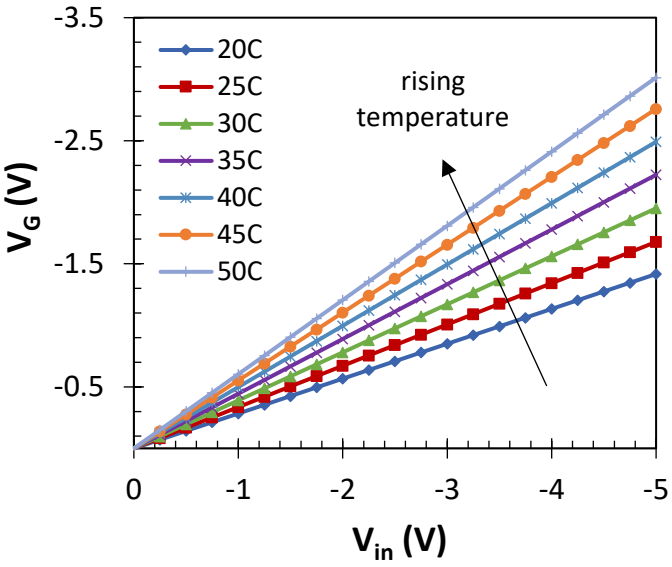

Figure 6.5: V_G as a function of V_{IN} for temperatures ranging from 20 to 50°C and R_G = 50 kΩ.

Table 4 compares the gate voltage V_G (a) calculated using Eq. (3.10), (b) measured on the output of the voltage divider (transistor is disconnected) and (c) measured on the gate of the transistor in the fully-assembled sensor using the following parameters R_G = 50 kΩ, R_D = 47 k kΩ, V_{IN} = V_{DD} = –4 V. The obtained values are very similar, indicating that the transistor does not load the left side of the circuit due to its high input impedance.

Figure 6.6 shows the transistor gate voltage V_G as a function of supply voltage V_{DD} at various temperature settings of the thermistor. As expected, the value of V_{DD} has no effect on the transistor V_G. The graph clearly illustrates the linear increase in V_G with rising temperature, in agreement with data of Figure 6.5 and Table 4.

Table 4. Gate voltage of the transistor.

	Eq. (1) [a]	voltage divider [b]	full sensor [c]
T (°C)	V_G (V)	V_G (V)	V_G (V)
20	-1.136	-1.133	-1.132
25	-1.333	-1.342	-1.331
30	-1.541	-1.561	-1.548
35	-1.753	-1.778	-1.764
40	-1.966	-1.993	-1.987
45	-2.173	-2.207	-2.194
50	-2.372	-2.411	-2.394

[a] V_G voltage calculated using Eq. (1)
[b] V_G measured on the output of the voltage divider (transistor is disconnected)
[c] V_G measured on the gate of the transistor in the fully-assembled sensor. (R_G = 50 kΩ, R_D = 47 kΩ, V_{IN} = V_{DD} = –4 V)

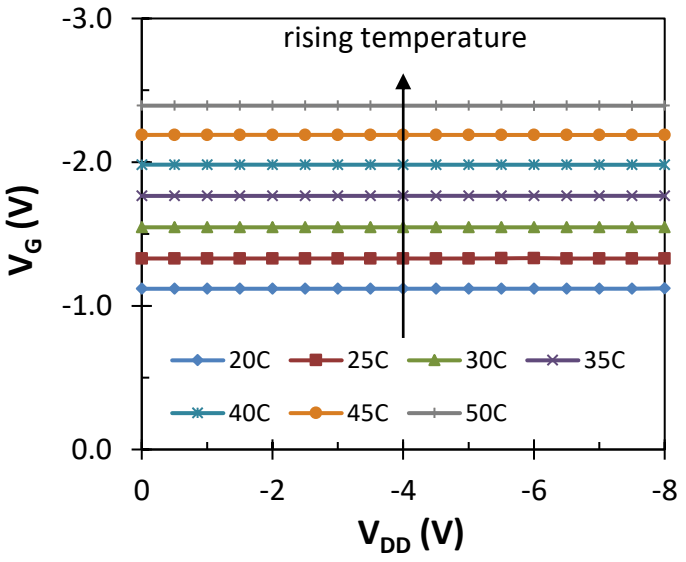

Figure 6.6: V_G as a function of V_{DD} for temperatures between 20 and 50°C, R_G = 50 kΩ, R_D = 47 kΩ and V_{IN} = −4V. V_G is referenced to ground.

Figure 6.7 shows V_{OUT} as a function of V_{DD} at varying temperatures. V_{DD} shows an increase with the rising output voltage V_{OUT} (= V_{DS}). For lower values of V_{DD}, the output voltage V_{OUT} increased linearly with a slope of about 0.18, observed for V_{OUT} less than ~ −1.2 V, corresponding to the transistor operating in the linear regime ($|V_{DS}| < |V_{GS}| - |V_{TH}|$). When the supply voltage V_{DD} is sufficiently high to place the transistor into saturation ($|V_{DS}| \geq |V_{GS}| - |V_{TH}|$), the slope of V_{OUT} becomes ~1.

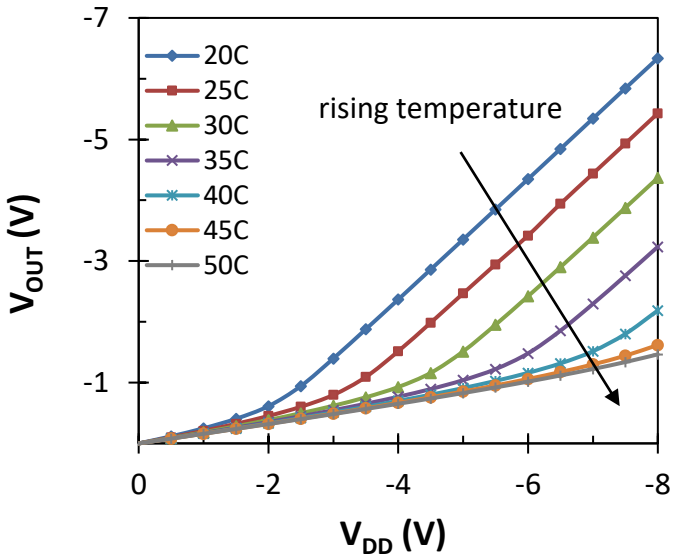

Figure 6.7: V_{OUT} as a function of V_{DD} for temperatures between 20 and 50°C, R_G = 50 kΩ, R_D = 47 kΩ and V_{IN} = −4V.

Figure 6.8 shows V_{OUT} as a function of temperature at various V_{DD}. V_{OUT} decreases with rising temperature regardless of the supply voltage V_{DD}. When the transistor operates in saturation, the change in V_{OUT} is ~ –200 mV/°C and the decrease is approximately linear. The response to temperature becomes substantially weaker at higher temperatures when the voltages on the terminals of the transistor drive it into the linear regime. In such a case V_{OUT} responds to the changing temperature at a rate of ~ –1.3 mV/°C and the decrease is again linear.

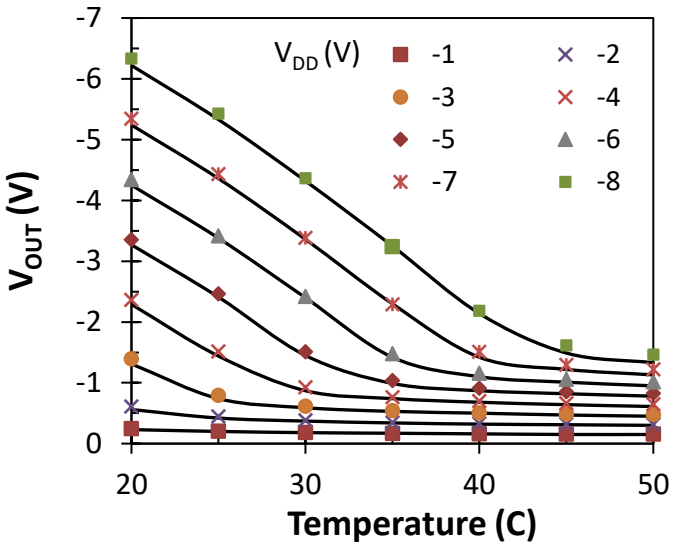

Figure 6.8: V_{OUT} of temperature sensor as a function of temperature between 20 and 50°C for R_G = 50 kΩ, R_D = 47 kΩ, and V_{IN} = –4 V. The solid black lines in (c) correspond to the sensor model.

Figure 6.9 shows repeated measurements of V_{OUT} as a function of V_G for the two OTFTs in Figure 6.2. V_{OUT} shows an almost linear decrease with rising V_G as the temperature T is raised from 20 to 50°C (rising T) and back down to 20°C (falling T). V_{OUT} levels off for high values of V_G, resulting from the transistor being operated in the linear regime. OTFT with higher drain current (Figure 6.2 (b)) exhibits a steeper decline and levels out at ~ −2 V. The transistor with lower drain current (Figure 6.2(a)) exhibits a slightly weaker response to the temperature with signs of levelling beginning at ~ −2.4 V. Both transistors show good repeatability; however, OTFT of Figure 6.2(b) with higher drain current exhibits about a factor of two stronger response when compared OTFT in Figure 6.2(a). By taking the slope of V_{OUT}/V_{IN}, the voltage gain of both transistors can be calculated, leading to the maximum value of 4.94 V/V for the OTFT of Figure 6.2(b) and 2.79 V/V for the OTFT of Figure 6.2(a). Consequently, the voltage gain of the transistor scales approximately linearly with the OTFT on-state

drain current that must exceed ~ 20 μA at $V_{GS} = V_{DS} = -2$ V for the transistor to provide amplification of the sensor signal.

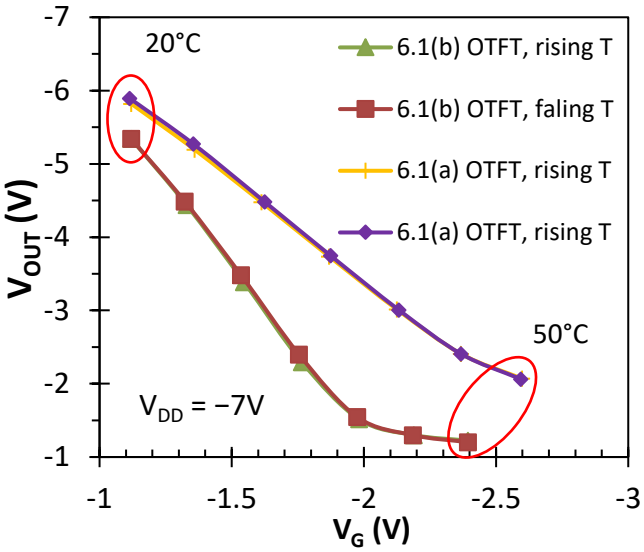

Figure 6.9: Repeated measurements of V_{OUT} as a function of V_G for $V_{IN} = -4$ V, $V_{DD} = -7$ V, $R_D = 47$ kΩ, $R_G = 50$ kΩ and OTFTs of Figure 6.2(a) and (b). Rising and falling T represent ramping temperature from 20 to 50°C and from 50 to 20°C respectively.

6.3.2 Temperature sensor model

The behaviour of the sensor depends on the operation of the transistor in the linear and saturation regimes as a consequence of the relationship between V_G and $V_D = V_{OUT}$. Therefore, the behaviour of the transistor and thus the sensor can be modelled based on the relationship of the drain current I_D and V_{OUT} respectively, where I_D represents the transistor current and V_{OUT} represents the sensor output, i.e. the voltage on the drain of the transistor. The drain current model has previously been demonstrated in [6.26] derived from the TFT DC compact model [6.27]. A simplified form of the equation has been adapted as in Equation (6.1) to capture the full behaviour

of the transistor and thus sensor. The single analytical expression for I_D is modelled as:

$$I_D = \frac{W}{L\left(1-\frac{\Delta L}{L}\right)} \cdot \frac{\mu_O}{\left(\frac{V_{SS}}{\gamma+2}\right)^{\gamma}} \cdot C_{diel} \cdot \left[\frac{(VS_{EODR})^{(\gamma+2)}}{\gamma+2} - \frac{(VD_{EODR})^{(\gamma+2)}}{\gamma+2}\right] \quad (6.1)$$

where VS_{EODR} and VD_{EODR} are the effective voltage overdrive on source and drain side of the transistor, respectively. If the source/drain contact resistance is neglected, they are:

$$VS_{EODR} = V_{SS} \ln\left\{1 + \exp\left[\frac{V_G - V_{TH} - V_S - (V_G - V_S)\delta_{VT}}{V_{SS}}\right]\right\} \quad (6.2)$$

$$VD_{EODR} = V_{SS} \ln\left\{1 + \exp\left[\frac{V_G - V_{TH} - V_{OUT} - (V_G - V_{OUT})\delta_{VT}}{V_{SS}}\right]\right\} \quad (6.3)$$

$\Delta L/L$ represents the channel length modulation. When the transistor is turned on, which is the case of the temperature sensor, it can be expressed as:

$$\frac{\Delta L}{L} = \lambda(V_{OUT} - V_S) \cdot \frac{(V_{OUT} - V_S) + (V_G - V_{TH})}{2(V_{OUT} - V_S) + (V_G - V_{TH})} \geq 0 \quad (6.4)$$

The remaining parameters, so called ‘fitting parameters’, are the subthreshold slope V_{SS}, mobility enhancement factor γ, low-field mobility μ_o, and the threshold voltage bias sensitivity δ_{VT}. They are determined by obtaining a least-square fit of Equation (6.1) to the data of Figure 6.2(b). Furthermore, the channel modulation factor is $\lambda = 0.02$.

The result of such fitting is demonstrated by the red lines in Figure 6.2(b). The result shows that Equation (6.1) reproduces the transistor transfer characteristics well and thus enables calculation of V_{OUT} of the sensor. The advantage of using Equation (6.1) is that the same four fitting parameters reproduce the transistor behaviour both in the linear and saturation regime.

The behaviour of V_{OUT} is related to I_D and consequently temperature variations in the form of V_G. Based on the above equations, V_{OUT} as a function of temperature can be expressed as follows:

$$V_{OUT} = V_{DD} - I_D \cdot R_D \tag{6.5}$$

The black lines in Figure 6.8 show the calculated V_{OUT} for the transistor of Figure 6.2(b).

6.4 Discussion

A highly sensitive temperature sensor based on a low-voltage high-transconductance OTFT and thermistor was demonstrated and characterised, including a sensor model based on the compact model of the transistor. The purpose of the investigation was to demonstrate the OTFT as an amplifier of the changing transistor gate voltage, all while within a simple temperature sensor application. The change in the gate voltage was induced by a thermistor, the resistance of which changed with temperature. The performance of the temperature sensor was assessed by heating the thermistor through a range of temperatures and monitoring the transistor input and sensor output.

The temperature sensor evaluation revealed 5 parameters which impact its behaviour via V_{IN}, R_T, R_G, V_G and V_{DD}. These parameters influence the performance of the organic transistor by impacting the gate and drain voltages. These voltages have been shown to play a crucial role in the temperature sensor sensitivity. The parameters of the temperature sensor govern the sensor sensitivity within the desired temperature range. Analysis of the thermistor resistance to temperature revealed larger changes in R_T at lower temperatures and a non-linear decrease in resistance at high temperatures, the behaviour is related with the beta (β) constant of the NTC thermistor [6.28]. Variations from 128 kΩ to ~34 kΩ were observed when the thermistor was heated from 20 to 50°C. The change in the resistance manifested as a change in the gate voltage of the transistor. The larger the change in R_T with temperature, the larger the change in V_G, providing a higher sensor sensitivity V_{OUT}.

Evaluations of resistor R_G revealed 50 kΩ as the optimal choice of resistance for the intended temperature range between 20 and 40°C. i.e. for body temperature monitoring. A lower R_G widens and shifts the temperature band to higher temperatures. Similarly, a higher R_G narrows and shifts the temperature band to lower temperatures. Therefore, the midpoint of 50 kΩ results in the largest variation in V_G of approximately 1 V. In addition, it is well suited for operating the transistor between $V_G = -1$ to -2 V, i.e. well above its threshold voltage.

Analysis of V_{IN} found evidence of a linear dependence with V_G as well as increased sensitivity at higher temperatures. V_G is observed to experience a ramp dependence with V_{IN} where larger V_{IN} produced larger V_G and higher temperatures significantly increase V_G. The significance of this finding lies within the operating

principles of a transistor. As previously mentioned, the gate voltage of a transistor controls the formation of a conduction channel. In addition, larger values with respect to V_D result in the linear operation of the transistor. Lower values of V_G with respect to V_D result in the OTFT operating in the saturation regime, i.e. the transistor can be forced to operate in the linear or saturation regime based on the V_G, i.e the temperature. Changing the temperature from 20 to 50°C typically resulted in a transition of the OTFT from the saturation to the linear regime of operation, as a consequence of the response to temperature becoming substantially weaker at higher temperatures, driving the transistor to operate in the linear regime. The choice of V_{DD} offers the possibility to keep the OTFT in saturation throughout the desired temperature range. To achieve this, higher values of V_{DD} are required but at the expense of a higher power consumption.

For the given transistor, the sensor displays the strongest response for V_{DD} between −7 and −8V when operating in the temperature range from 20 to 40°C. This mode of operation yields the largest sensor sensitivity of 204 mV/°C; while the transistor amplifies the signal by a factor of ~ 5 when the OTFT is at V_{IN} = −4V and R_G = 50 kΩ. The temperature sensor without the transistor results in a lower voltage variation of approximately 0.86 V and sensitivity of 43 mV/°C.

The mathematical model of the organic transistor was used to explain the observed measurements and effectively predict the performance of such a temperature sensor. The agreement between the model and the measured data is excellent. The transfer characteristics of the transistor when simulated with four fitting parameters under the same conditions as the measured data sufficiently and accurately predicted

the linear and saturation regimes. The four fitting parameters; subthreshold slope V_{SS}, mobility enhancement factor γ, low-field mobility μ_o, and the threshold voltage bias sensitivity δ_{VT} (with set channel modulation factor λ) were able to fit both OTFT transfer characteristics. The use of the same fitting parameters has the advantage of reproducing the transistor behaviour in both linear and saturation regimes, thus reducing the number of equations for I_D from two to one.

Finally, full sensor integration on plastic substrate can be achieved. In the current temperature sensor prototype, fabrication of the OTFT was performed on PEN substrate, therefore, integration routes exist. For example, the thermistor used in the current model having temperature coefficient of resistance (TCR) of ~ −4 %/K could be replaced with a thin-film thermistor based on pentacene with Ag nanoparticles that was reported to exhibit TCR of ~ −4.4 %/K [6.16].

6.5 Summary

A thorough investigation of a temperature sensor with low-voltage, high on-state drain current transistor based on DNTT was demonstrated. The sensor uses an NTC thermistor with nominal resistance of 100 kΩ that responds to temperature changes in the range from 20 to 50°C, i.e. is suitable for body temperature monitoring. An OTFT configured as a common source amplifier with a high transconductance of 0.11 mS strengthened the input signal. Experimental observations surrounding the behaviour and functionality of the sensor were fully supported through a DC compact model of the transistor. The temperature sensor displayed a linear response to temperature changes with an average sensitivity of −204 mV/°C, ~ a 5 time increase

as a result of the transistor amplifier. Temperatures beyond 40°C exhibits a significant reduction in sensitivity down to ~ 1.3mV/°C, making the sensor ideally suited for the temperature range from 20 to 40°C. Furthermore, a voltage gain of up to 4.94 V/V was achieved when transistor with on-state drain current of 126 μA at $V_{GS} = V_{DS} = -2$ V was used. The linear dependence between the voltage gain and on-state drain current means that the current sensor configuration can achieve voltage amplification only for OTFTs with on-state drain current higher than 20 μA. Future development of the temperature sensor may lead to a fully-integrated, flexible sensor for wearable health monitoring applications.

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Chapter 7

Conclusions and future work

This thesis presents low-voltage organic thin-film transistors based on DNTT on PEN substrate with the aim (a) to raise the on-state drain current of such devices using channel geometry manipulation, (b) to investigate the behavioural instabilities of such devices due to DC or AC bias stress, and (c) to demonstrate the application of such transistors in an analogue temperature sensor system designed for body or ambient office monitoring.

7.1 Conclusions

This thesis presented OTFTs on PEN with high on-state drain current, low-voltage operation, and hysteresis-free characteristics, demonstrating the transistor's

voltage amplifying properties in a temperature sensor system. The work advances the previously developed OTFTs on glass substrate at the University of Strathclyde. Transfer of fabrication process from glass to PEN substrate enabled mechanical flexibility, while maintaining comparable performance. Interdigitated source/drain contacts leading to channel width-to-length ratio of up to 900 were coupled with ultra-thin dielectric bi-layer of aluminium oxide (AlO_x) and octadecyl phosphonic acid ($C_{18}PA$) and provided significant improvement in the on-state drain current (over 120 µA) and transconductance (beyond 50 µS), essential for the transistor as voltage amplifier. $AlO_x/C_{18}PA$ gate dielectric led to capacitance of 0.3 µF/cm^2 and provided low gate leakage current and hydrophobic surface properties that resulted in negligible hysteresis. A summary of the electrical performance for narrow- and wide-gate OTFTs are shown in Table 5.

Table 5. Electrical characteristics of OTFTs with interdigitated electrodes in narrow- and wide-gate configurations.

	Narrow-gate OTFT with W/L ~ 524	Wide-gate OTFT with W/L ~ 494
I_{ON} (µA)	51	36
I_{OFF} (pA)	887	8.6
V_{TH} (V)	0.47	0.69
μ (cm^2/Vs)	0.32	0.30
I_G (pA)	15.6	31.8
S (mV/dec)	162	86.3
i_d (µA)	11.1	10.6
g_m (µS)	56	53

Fresh and aged (5-6 months) transistors were subjected to AC bias stress to study their operational stability. AC square pulses with the on-time of 1 s and off-time of 4, 19, 39 or 59 s were applied to the gate and drain terminals, to turn the transistors on and off repeatedly. OTFTs exhibited degradation in V_{TH} and I_{ON}, and improvement in μ regardless of pulse period or their age. Since the net stress time of 1000 s was equal for all stress conditions, the changes in the transistor parameters were attributed to the varied turn-off time of the transistor. Overall, the changes in the transistor parameters were small ($\leq$ 19%) for stress up to ~ 17 hours and the on-state drain current of the 'aged' transistors degraded faster and stabilised after ~ 500 pulses. The bias degradations is typically associated with the charge trapping controlled by surface roughness, interfacial defects, choice of dielectric/semiconductor materials, and channel length. The small changes reported in this thesis suggest positive impact of DNTT and $C_{18}PA/AlO_x$ interface. Results also showed T = 60 s as favourable operating condition for sensors systems based on such OTFTs.

The temperature sensor system demonstrates one of many potential applications of OTFTs configured as common-source transistor amplifiers. In the presented application, two transistors with on-state drain current of 61 and 126 µA respectively provided sufficient voltage gain of ~3 and ~5 V/V, while an NTC thermistor with nominal resistance of 100 kΩ responded to temperature changes from 20 and 50 °C. Low supply voltage of −7 V kept the transistor in saturation operation for temperatures between 20 to 40 °C and the sensor output V_{OUT} showed linear response to temperature with sensitivity of ~ −204 mV/°C. A DC compact model of the transistor was implemented to model the sensor system and validate the sensor measurements.

7.2 Future work

Future directions of the work could vary from further transistor development to full sensor integration. As demonstrated, the sensor response depends greatly on the transistor performance and scales linearly with the on-state drain current. The thesis focused on improvement in the on-state drain current and transconductance by changing the channel geometry. However, the field-effect mobility of the presented transistors is 0.3 – 0.4 cm^2/Vs and that does not represent the highest mobility achieved for $AlO_x/C_{18}PA$/DNTT OTFTs [2.52].

As discussed in Chapter 4, the contact resistance may be the cause of the decreasing normalised on-state drain current with increasing W/L. Since the contact resistance starts to dominate in short channel length devices, it must be addressed when L is reduced. The contact resistance causes reduction in the applied voltage and therefore a reduction in the effective voltage across the channel, resulting in insufficient charge injection, hereby causing a reduction in drain current [2.25]. [2.18] investigated the effect of contact resistance in devices with channel length from 2 to 100µm, and reported a significant reduction in the effective mobility and limitation in performance when the channel length was reduced to less than 10 µm. Similarly, [2.19] described that the contact resistance substantially decreased the effective mobility when the channel length was reduced to less than 1 µm. Therefore, extraction and evaluation of the contact resistance of the narrow-gate devices with $L < 20$ would provide useful insights on the degree of degradation caused by contact resistance. In addition, understanding and addressing the contact resistance in the current OTFT

provides an additional route for a reduction in L and for increasing the on-state drain current.

The bias stress investigation revealed a dependence between the transistor turn-off time and the change in transistor parameters under bias. A longer turn-off time resulted in the lesser bias-induced degradation. Therefore, this creates an opportunity for applications that do not require continuous OTFT operation. In such cases, intermittent biasing of the OTFT would lessen the bias stress effect.

The research presented has also laid the foundation for full sensor integration on plastic substrate. In the temperature sensor prototype, fabrication of the OTFT was performed on PEN substrate. The thermistor used in the current sensor has temperature coefficient of resistance (TCR) of ~ −4 %/K and could be replaced with a thin-film thermistor based on pentacene with Ag nanoparticles that reported to exhibit TCR of ~ −4.4 %/K [6.16]. Once integrated, an analysis of the full system can be performed. In addition, the output from the sensor system can feed into a microcontroller for data processing and wireless transfer.