University of Strathclyde

Large Step Down Voltage Converters for Desalination

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This thesis is the result of author's original research. It has been composed by the author and has not been previously submitted for examination which has led to the award of a degree.

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Abstract

One percent of the world's drinking water is currently desalinated, and this will have to increase to 14% by 2025. Desalination is energy intensive, having significant commercial and ecological implications.

One of the most promising methods of desalination is capacitive deionisation which only uses 1kWh/m^3 but requires a voltage of less than 1.8V at currents of up to 1000A

This thesis produced hardware capable of creating 550A at a voltage of 1.8V, giving over a 1kW power rating, with an input voltage of 340V dc. The converter designed was a bidirectional asymmetrical half-bridge flyback converter allowing for isolation at these high step down ratios. The converter was used to charge a bank of 17,000F supercapacitors from 0V to 1.8V, with an initial charging step down ratio in excess of 340:1 falling to 190:1 as the load charged.

A novel Asymmetrical Half-Bridge Coupled-Inductor Buck converter is presented as the ideal solution for large step-down ratios with analysis comparing the ability to efficiently step down a voltage with other common converters, the buck and flyback converters.

A comparison between a single-ended coupled-inductor buck converter employing a buck-boost voltage clamp and the novel asymmetrical half-bridge coupled-inductor buck converter circuit shows that the asymmetrical half-bridge converter is a more efficient circuit as leakage energy is recovered; the switch voltages are clamped to within the dc voltage rating of the bridge and the control strategy is simple.

Passive and active snubbers are reviewed for efficiency, switch ratings and management of the effects of leakage inductance and compared against the novel designs presented.

In the desalination application isolation is required so the flyback circuit is used. An isolated three switch bidirectional converter is constructed using silicon carbide MOSFETs and diodes switching at 40kHz. The converter uses novel current measuring techniques, an on-board microprocessor and closed loop control designed into the final DC-DC converter.

List of Symbols

Symbol	Term	Unit
A	Area	m^2
B_s	Magnetic Flux Density	T
C	Capacitance	F
δ	Duty Cycle	
δ_b	Buck Duty Cycle	
δ_{ci}	Coupled-Inductor Buck converter Duty Cycle	
δ_{fb}	Flyback Duty Cycle	
f	Frequency	Hz
H	Applied Magnetic Field	A/m
I_{load}	Load Current	A
I_{max}	Maximum Current	A
I_{min}	Minimum Current	A
I_1	Current flowing in inductor L1	A
I_2	Current flowing in inductor L2	A
l	Length	m
L	Inductance	H
L_t	Total inductance of coupled inductor	H
MMF_{ci}	Magneto Motive Force Coupled-Inductor Buck Converter	A
MMF_{fb}	Magneto Motive Force Flyback Converter	A
μ_0	Permeability of a Vacuum	H/m
μ_r	Relative Permeability	H/m
N	Number of inductor turns	
N_1	Number of turns in inductor L1	
N_2	Number of turns in inductor L2	
n	Number of transformer turns	
SDR	Step Down Ratio	
T_s	Switching Time Period	s
R	Electrical Resistance	Ω
V_{in}	Input Voltage	V
V_{out}	Output Voltage	V

List of Abbreviations

Abbreviation	Term
AC	Alternating Current
CCM	Continuous Conduction Mode
CDI	Capacitive Deionisation
DC	Direct Current
DCDL	Diode Capacitor Diode Inductor
DCM	Discontinuous Conduction Mode
EMI	Electromagnetic Interference
IGBT	Insulated Gate Bipolar Transistor
LED	Light Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PI	Proportional Integral
PID	Proportional Integral Derivative
PWM	Pulse Width Modulation
RCD	Resistor Capacitor Diode
RMS	Root Mean Square
SiC	Silicon Carbide
SMPS	Switched Mode Power Supply
ZRC	Zener Resistor Capacitor

Chapter 1 Introduction

This thesis presents comparative analysis of DC-DC converters with large step-down voltage ratios. This research analysis includes detailed evaluation of the potential use of large step-down ratio converters in water desalination. There are many single stage DC-DC converter topologies, whence analysis of both isolated and non-isolated versions are presented. Also, the main limitation of large step-down DC-DC converters, namely switch over-voltage due to leakage inductance, is evaluated.

1.1 Water Desalination Background

This research investigates power electronics' suitability for application in water desalination (process of salt removal) through *Capacitive Deionisation* [1]. Water scarcity is thought to be one of the biggest challenges facing our generation. About 4 billion people, representing nearly two-thirds of the world population, experience severe water scarcity during at least one month of the year and this could increase to some 4.8-5.7 billion people in 2050. [2], [3]. Turning sea or waste water into drinking water is vital for continued life, growth and prosperity globally. Fresh water is also a fundamental resource for non-anthropological applications, steam turbines in power stations and farming irrigation for example, therefore for arid or semi-arid geographical regions, desalination is an evident solution. In such regions of low precipitation, a high UV Index is common. When coupled with investment in solar driven power, an electrical method of desalination holds great potential. This thesis will outline said process and a viable circuit topology for the application.

70% of the world's surface is covered by water, however only 2% of this water is fresh water and of this, only one third is readily accessible – with the inclusion of polluted water, this number again falls. Perhaps the fact that we should be teaching future generations is "how much of the world is made up of usable drinking water?" and its startling response, 0.205%, Fig. 1.1.

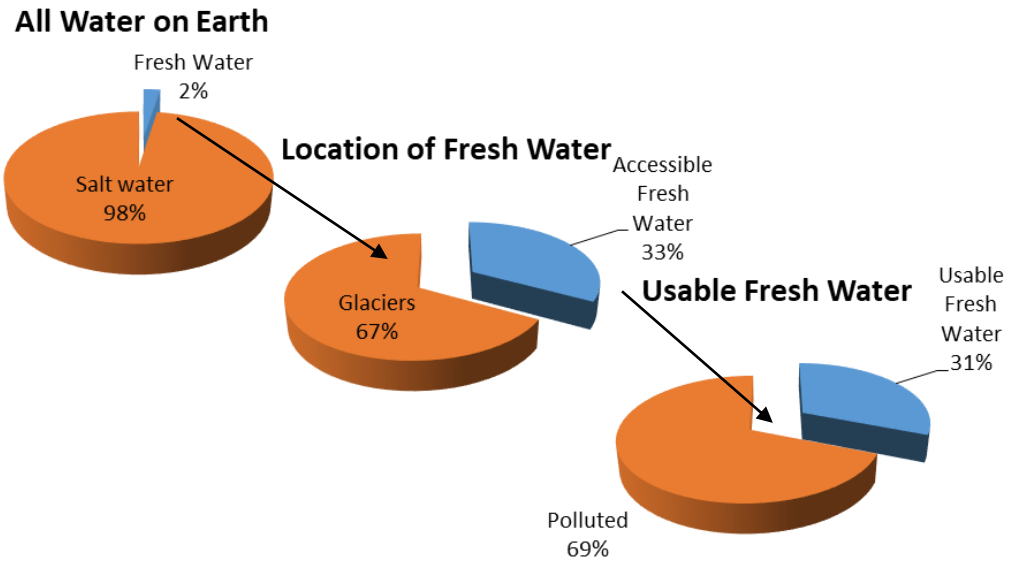


Fig. 1.1 Percentage of fresh water on Earth

Global water consumption is rising annually by about 1% [4], however the amount of readily available freshwater is not rising. Concurrently, an increasing world population is resulting in a mounting demand for fresh water.

Agriculture accounts for ~70% of global freshwater usage [5] and with an unyielding demand. According to [6], the Earth's population is predicted to increase by 1.5 billion to a global population of 9.7 billion by 2050 [7], with this, a predicted increase in food demand of 70% by 2050.

Remarkably, the second largest demand on our fresh water resource is generated by the electricity sector [8]. An estimated 1.1 billion [9] people at present, do not have access to electricity. An estimated increase in global energy consumption is in the region of ~49% from 2007 to 2035 with current thermal power plants and their water intensive requirements account for 78% of world electricity production. [10]–[12] As such, if current modes of electricity production are maintained, the volume of fresh water required will increase by 11.2%.[13] The culmination of these factors are leading to a global fresh water shortage and unless a financially viable and environmentally sustainable solution can be found, could prove cataclysmic .

One potential solution to fresh water shortage is the exploitation of wastewater or seawater. Desalination is the process of removing salt from saline solutions. Currently one percent of the world's drinking water is desalinated, and this is expected to increase to 14% by 2025. [4] However, desalination inherently is energy intensive, posing significant commercial and ecologic implications.

1.2 Energy Economics of Desalination

Various methods of desalination are currently performed to deionise and thus remove salt from a solution.

The primary variants in water desalination regarding economics are sea water desalination and brackish water desalination. The key difference is the concentration of salt in the solutions. Sea water is around 35,000 ppm whereas brackish water is ~4000 ppm (variable depending on the sample's source). [14]

The minimum energy required to separate salt ions from a solution is about 1.1kWhm^{-3} for average sea water samples and 0.12 kWhm^{-3} for typical brackish water. [14] Energy versus ppm is a linear relationship however achieving these values is complex and expensive. [15] [16]

The significance of dissimilar salt concentration lies in the effect on desalination process efficiencies. However, processes that desalinate via heat are almost independent of concentration as this functions to remove the water from solution (via evaporation) as opposed to salt, therefore the energy is close to a constant. There is some variation in boiling point for different solution concentrations but this energy increase is minimal. As such when it comes to efficiencies, thermal methods can be far more viable for seawater desalination.

Other methods including reverse osmosis and electrochemical methods are more dependent on salt concentration. There is still scope for them to compete with thermal methods in sea water desalination and their efficiencies can be far better than the thermal techniques, particularly for brackish water desalination.

1.3 Methods of Desalination

There are three fundamental processes used in water desalination: thermal, pressure, and electrical. [17]

The thermal process, distillation, is perhaps the most widespread application for seawater at present. *Multistage flash distillation* is the evaporation and consequent condensation of a liquid. When applied to salt water, the condensed fluid is free from salt.

Pressure driven salt removal via *reverse osmosis* is a cost-effective desalination technique applicable to both sea and brackish water whereby water is pushed through a semi-permeable membrane partitioning salt molecules and pure water on opposite membrane sides.

Electrical desalination involves electric field generation and the use of a semi-permeable membrane. When electric voltage is applied to a solution an electric field is produced, this causes ions present to disassociate and removed using a semi-permeable membrane.

The energy used in both the electrical and pressure process depends on the initial concentration of salt with 90% of current desalination plants employing reverse osmosis or multistage flash distillation. Both methods are highly energy-intensive but at present, shortage of drinking water outweighs this energy expenditure. Further methods include electrodialysis, multiple effect distillation, mechanical vapour compression, and capacitive deionisation.

Capacitive deionisation [1], [18], [19] is an auxiliary electrical desalination method comprised of two stages: the adsorption stage, where desalination of feed water occurs, and the desorption stage, where the electrons are recuperated. CDI applies an electrical potential over parallel anodic and cathodic electrodes, commonly porous carbon, to form an electrolytic cell. In salt solution, the presence of sodium and chloride ions (Na^+ and Cl^- respectively) enhances water conductivity and reduces the solution's resistance to electron flow. Anions, negatively charged chlorine ions, are removed from solution via assimilation onto the positively charged electrode. A simultaneous movement of positively charged sodium cations, supplement the cathode; the negatively polarised electrode. As the ions undergo electrosorption, this process renders the salt-water solution salt free, Fig. 1.2.

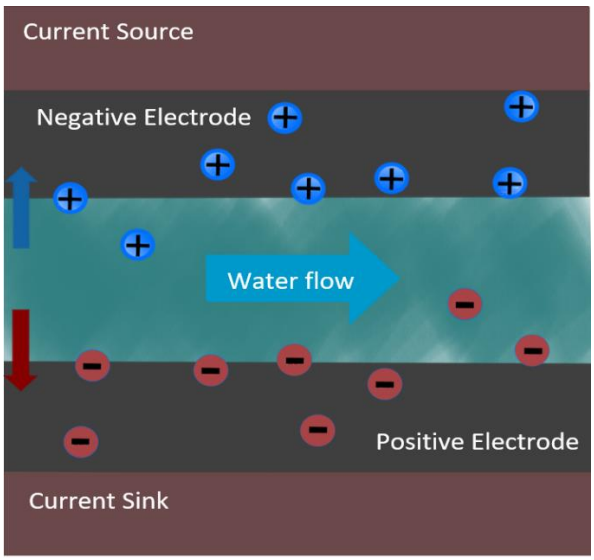


Fig. 1.2 Capacitive deionisation electrode cross section

The desorption phase is initiated when the electrodes reach saturation point and the electrodes are discharged. When discharging the cell, the ions migrate back into the water stream increasing the waste solution salinity. Cell discharging can recover up to 60% of the initial energy used to remove the ions. The highly saline water stream created is then returned to the sea as waste water. The process can be likened to that of charging and discharging a super capacitor due to the linear charge/discharge cycles and process repeatability.

Presently, the predominant use for CDI is desalination of low to moderate salt concentration (~10gL^{-1}) water (brackish). [20]–[22] This owes to CDI efficiently removing salt ions from water in contrast to other methods which remove water from the saline solution. In CDI, the energy consumption per unit volume of salt water is proportionate to the amount of removed salt. This contrasts with the previously presented desalination methods, such as RO, where the energy use and water volume feed water is less proportional.

Membrane CDI (MCDI) is a variant of CDI which involves the insertion of ion-exchange membranes in front of the electrodes. This adjustment enhances the CDI unit by numerous means: MCDI requires less energy input than CDI [1], and the presence of a membrane ensures that ions remain in the electrode pores. This concurrently results in enhanced

migration of the remaining ions in solution through the membrane, and overall increased salt-adsorption efficiency, Fig. 1.3.

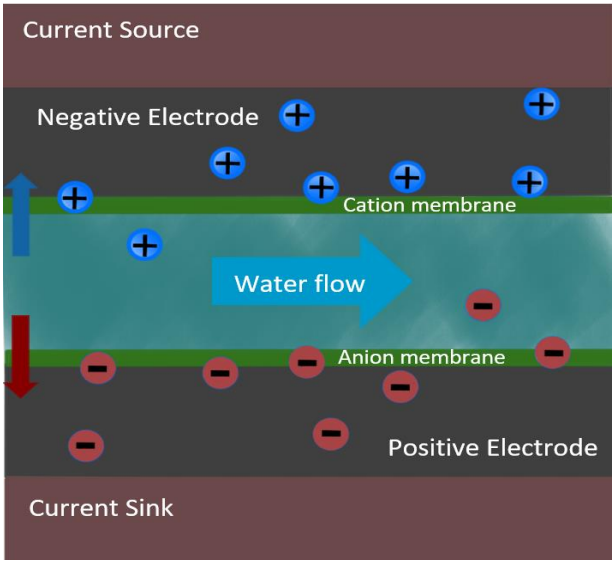


Fig. 1.3 Membrane Capacitive Deionisation cross section

For elevated CDI performance, electrode material selection is important and is undergoing continuing research. The most elementary electrode material is porous carbon. In deionisation, high electrosorption capacity is paramount - this is achieved via optimal transfer of ions through a highly conductive medium. To increase percentage time of desalination against time required to reset the cell, the pore size distribution must consist of large pores with a high specific surface area. Also, through chemical stability, the porous material used should have low degeneracy rates in the functioning voltage range.

Recently hydrogels, known as Aerogels and Xerogels, have gained interest [23]–[25]. The gels have extremely low density and electrical resistivity, and are consequently of interest within optimising electrode functionality research.

1.4 Summary of Techniques

Table 1.1 Summary of desalination techniques.

Process	Power consumption	Water Impurity
Reverse Osmosis	2.9–3.7 $kWhm^{-3}$	Sea/Brackish Water
Multistage Flash Distillation	13.5 $kWhm^{-3}$	Sea Water
Electrodialysis	1.7 $kWhm^{-3}$	Brackish Water
Multiple-Effect Distillation	6 $kWhm^{-3}$	Sea Water
Mechanical Vapour Compression	6 $kWhm^{-3}$	Sea Water
Capacitive Deionisation	1 $kWhm^{-3}$	Brackish Water

The electrochemical processes, *capacitive deionisation* (CDI) and *electrodialysis*, are areas out with this project that require most investigation; with both methods presenting energy saving potential in contrast to current methods of desalination. CDI is particularly attractive. By recouping the energy from the separated ions, the net energy required for the process is reduced to a value correlated with system losses, so could be adopted for affordable desalination. Both electrochemical process requires further filtration to remove bacteria and potentially any pollutants as the process only removes ionic salts from the water.

1.5 Requirements of Electrochemical Methods of Desalination

Both discussed electrochemical water desalination processes, CDI and EDI, theoretically operate at under 1.23V DC (Nernst Voltage). The Nernst Voltage is the voltage at which the hydrogen bonds between H and O break in a water molecule (H_2O); above this point, electrolysis occurs and requires surplus energy. However, this critical voltage must be applied directly across the water molecule, and to mitigate the voltage drop effects of impurities and resistance of the solution, voltages between 1.23 to 1.8V DC are commonly used.

The methods to produce the input of 1.8V are important. A simple configuration would be an in-series cell arrangement to summate smaller voltages to achieve a large input voltage. The cells have capacitive properties as they are effectively charge ions being stored on parallel electrodes so cell balancing circuits must be fitted to ensure even distribution of current and voltage.

The difficulty of creating a 1.8V supply voltage depends upon the voltage input, as the power source for the desalination process dictates the electronics required for the given application, be it AC or DC.

The energy required for desalination can be as low as $1kWhm^{-3}$ for 4,000ppm. The voltage required for CDI must be less than 1.8V to stop hydrogenisation (formation of hydrochloric acid and sodium hydroxide). This low voltage present challenges for the electronics to achieve the required power levels into the electrodes; high currents are required potentially in excess of 1000A per cell [19].

The three most probable inputs - are: three phase AC supply, single phase AC supply, or a solar panel array.

A three-phase AC supply: Three sinusoidal voltages at (conventionally) 50Hz and 120º out of phase. Such supply requires rectification (conversion from AC to DC) to provide a 600V DC input. As any input must be reduced, a 600V input is the weakest aspect for the application as the voltage step-down ratio has a maximum of 600:1. Such a large step down would normally create high peak currents or large over-voltages due to leakage inductance of a wound magnetic component. The use of a three-phase step-down transformer adds cost, volume, and reduced efficiency, but does afford isolation.

The single-phase AC supply: would also need to be rectified from 240V AC to 340V DC. This is a lesser, and consequently easier step-down ratio. However, the single phase supply is primarily reserved for domestic or small-scale plant use, therefore for the vast quantities involved in water desalination its preference is diminished.

A *solar panel array* of photovoltaic cells exhibits potential, primarily areas where desalination is necessary; low precipitation rate is associated with areas that have a high UV index. A solar panel is comprised of photovoltaic cells which utilise UV light energy to produce DC voltage. This voltage output is variable but 48V is a widely used standard. A 48V input voltage battery would necessitate a smaller step down ratio, however this

generates a higher current draw from the supply than a larger step down ratio would for the same output current. Current draw is critical in battery supplies as high current over prolonged time periods reduces the lifecycle of a battery bank therefore this aspect should be considered in input selection.

The primary argument for a solar panel array is its environmental sustainability. Firstly, the source of electrical supply has a comparatively low carbon footprint. To ensure maximal symbiosis, the panels could be installed on the roof of the desalination facility, reducing the travel of electricity and subsequent losses of energy, as well as the installation foot print.

Following comparative analysis, the 600V input circuit topology was deemed to be of most value to investigate due to its complexity. So if such technology could function from 600V, the resultant equipment could cater for lower voltage levels.

When approaching the problem of capacitive deionisation, both small-scale and large-scale industrial plants must be considered to fashion the most efficient design of both desalination cells and their electronics.

In water desalination, cells can be in both parallel or series physical arrangement. In series, water flows from one cell into the next and in parallel, water is forced through one cell or another but not both. Connecting the cells in series allows for greater ion removal from the water stream at a constant flow rate. A parallel cell arrangement allows for a greater volume of water to be desalinated but does not change the amount of salt removed from a given volume of water as this is proportional to the current flowing into the cells.

As well as the physical layout, cells can be electrically connected either in series, parallel, or under individual control.

In a series array, the voltage across the cells is summated and the operating output voltage required can be increased to reduce the step-down ratio of the converter. However, when electrically connected in series, the characteristic of each cell will determine the amount of voltage each cell experiences and imbalanced energy distribution can result.

In parallel electrical connection, voltages are not summated, so the 1.8V input voltage requirement is fixed. This presents the benefit that one DC-DC converter can be used for all cells connected in parallel with no additional electronics, with the consequences of

ease of control. When the cell layout is series in physicality and parallel electrically Fig. 1.4, the amount of salt removed can be calculated using the total current from the single converter.

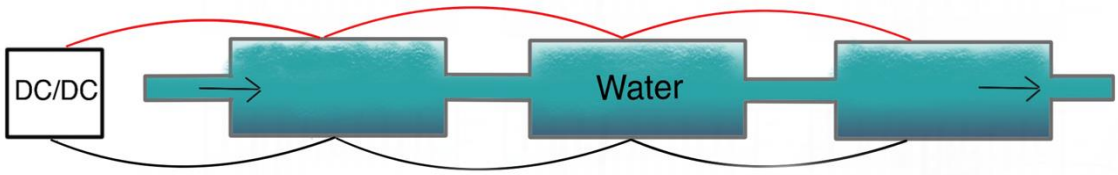


Fig. 1.4 Water desalination cells arranged in series electrically connected in parallel

For increased flow rate additional sets of cells can be physically added in parallel to the previous arrangement Fig. 1.5. This gives more area for the water to flow over and if the electrical current supply is doubled then the rate of water desalinated per time will double.

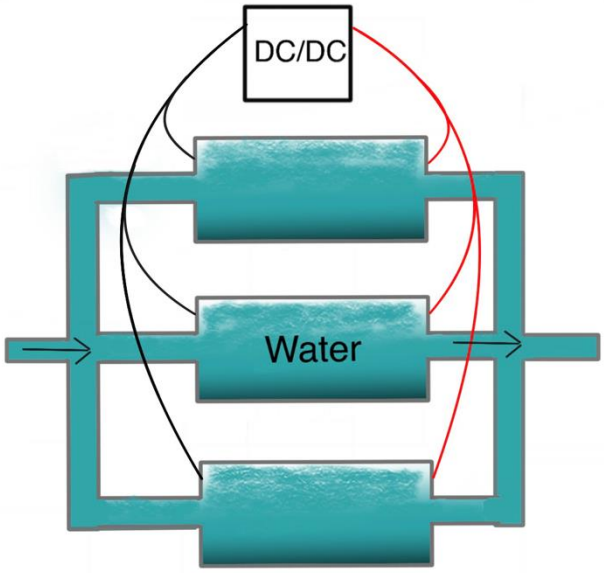


Fig. 1.5 Water desalination cells connected in parallel, electrically connected in parallel

For both layouts, if the currents became too large an additional DC-DC converter could be used to control this additional water stream and effectively create a stand-alone desalination unit. This would also allow for greater control in the case where the water flowing through each unit begins to differ.

Aside from cell layout and electronics, the energy path must also be considered. Energy is converted from the input voltage down to the required 1.8V in all arrangements. This can be achieved via a single, high-powered circuit or separately within each individual circuit responsible for cell block control. Once the cell is held at the correct voltage level desalination then occurs.

However, a major component of the electrosorption process is the 'flushing' or discharging of the electrodes. This discharge can be achieved in two ways: energy is either transferred from one discharging cell into a charging cell with any loss replenished by the grid or the energy is stepped back up to the input voltage to be absorbed by the supply.

This research considers multiple series-connected cells (as in Fig. 1.4) under singular circuit control utilising grid charging-discharging. Such circuit design is entirely modular, for a given increase in volume, flowrate and concentration, an additional module (block of cells and circuit) is connected in parallel. These can all operate individually or as a combined system.

1.6 Summary

Fresh water paucity is a significant issue facing our generation. Water desalination is a viable solution to this problem. Following evaluation of existing methods of water desalination, it is evident that capacitive deionisation offers promise and further investigation is of consequence. As this is an electrochemical method, operational efficiency relies upon efficient, reliable electronics. In the most extreme scenario, a water sample may require a capacitive deionisation circuit to function with a 600:1 step-down ratio. Electrically, a voltage less than 1.8V is required and large currents in excess of 500A allow for a higher rate of desalination. The input voltage is likely to be either 600V DC from three phase AC rectified or 340V DC (single phase AC rectified). Chapter 2 will consider various DC-DC converters with such a step-down capability.

1.7 Converter Parameter Specification

Throughout the thesis the overarching electrical aim is to step down a high voltage to 1.8V. Initially 600V dc is the target input and as such is investigated as this is seen as the worst case scenario where a three phase AC supply is used. Throughout the thesis however this target is altered for various tests and experiments due to the hardware capabilities of the initial prototypes.

In Chapter 3 a step down ratio of smaller than 100:1 is investigated as this was noted to be the most significant point when comparing the three converters discussed. Above this point no significant change is seen compared to the results of 100:1.

In Chapter 4 an input voltage of 150V is used for the hardware testing and simulations as this is the maximum possible with the given hardware due to large leakage inductance. To achieve a circuit higher power through put, an output voltage of both 1.8V and later 2.6V are tested as the 2.6V allows for a higher current draw and thus higher power testing.

Chapter 5 again uses the same 150V input voltage but achieved a higher power through put to step down to the 1.8V.

Chapter 6 presents the final experimental setup which is designed to extend the power and step down ratio as high as possible. A 340V dc input voltage is reached, with a 550A output. This demonstrates a step down of 340V-1.8V dc which is seen as a significant step. Future iterations should allow for the full 600V-1.8V dc set out in the initial scope.

1.8 Thesis Structure

This thesis includes an introduction to water desalination, comparative review of DC-DC converter topologies, switch voltage protection circuits and experimental assessment of a high current output DC-DC converter tested on a supercapacitive load, with the aim of determining the most appropriate circuit for capacitive deionisation.

- **Chapter 1**- Outlines the contained research of the thesis and its structure. And provides a brief introduction to, and methods of, water desalination, and an overview of the electrical requirements for the application.
- **Chapter 2** reviews DC-DC step-down converters from literature. Cursory analysis of each circuit is presented to determine the most befitting circuits for

application to water desalination. The chapter contains a review of passive snubber circuits suitable for protecting a switch against over-voltage.

- **Chapter 3** presents a detailed comparison of the most viable circuit configurations (buck converter, coupled-inductor buck converter and flyback converter) for large voltage step-down ratio application. Initially, circuit duty cycles and consequential peak currents are compared, followed by examination of circuit performance at various turns ratios.
- **Chapter 4** investigates active snubbers; their efficiency enhancement, control benefits and ability to suppress the adverse effects of leakage inductance inherent with large step-down magnetically coupled converters.
- **Chapter 5** introduces the asymmetrical half-bridge coupled-inductor buck converter; a novel converter topology that offers an aside solution to leakage inductance with cost and potential efficiency savings over active snubbers.
- **Chapter 6** discusses the experimental equipment used in circuit testing throughout this research. The chapter discusses the evolution of the initial capacitive deionisation test rig to the final super capacitor load used.
- **Chapter 7** presents conclusions, the author's contribution, and suggestions for future research

Chapter 2 DC-DC Converters for Voltage Step-Down Applications

Chapter 1 introduced water desalination and its applications. From this, the method of capacitive deionisation was selected for further investigation. Chapter 2 details analysis of capacitive deionisation, (CDI), electrical requirements. and introduces and evaluates a range of converter topologies that are suited to capacitive deionisation.

2.1 Circuit Design Scope

In addition to water desalination, there are many power conversion applications that require significant voltage step-down ratios, such as LED lighting or battery chargers. Such circuits require step-down ratios greater than 10:1. For example, if the circuitry is supplied from a rectified 230V single-phase AC to DC stage, the input voltage is 340V DC and the output voltage must be stepped down to 30V. Water desalination requires even greater step-down ratios due to typically low output voltage stipulations. For example, a step-down ratio of 190:1 is necessary to achieve the 1.8V output required for capacitive deionisation desalination from a single phase AC supply. [1] Conventionally, a flyback or multiple-stage buck converter [26] would be used to achieve such ratios. However a coupled-inductor buck circuit [27]–[29] or a dual active bridge may be considered as a more efficient voltage step-down circuit for a given turns ratio of N_1:N_2 [30]–[32]. Other less conventional DC-DC step-down converters are also considered and evaluated.

2.2 DC-DC Converters

A DC-DC converter is a circuit that transforms direct current, DC, from one voltage level to another whilst concurrently changing the current by the inverse of the same ratio. DC-DC converter circuits function through the switching of a semiconductor switch. The ratio

of switch on time to the switching period is used to determine the output voltage. Whether the input voltage is increased or decreased depends on the circuit arrangement. DC-DC converters can be evaluated by their power density, complexity, efficiency and resultant cost and reliability.

2.2.1 Comparison and Simulation of Converters

Being able to compare existing converters relies on defining the criteria to compare them against and describing the simulation so that it can be recreated and repeated.

The circuits are simulated using the software Pspice which allowed for accurate simulations of a variety of circuits using the same components thus allowing fair comparison.

The fundamental design parameters of all converters are stated in Table 2.1, unless stated otherwise. Individual component values are stated under each simulation. These apply to all the fundamental converters simulated in Chapter 2.

Table 2.1 Fundamental converter simulation parameters

Variable	Value
Coupling Factor	0.95
Frequency	40kHz
Duty Cycle	24%
Input Voltage	300V

2.2.2 Buck Converter

The simplest step-down converter is the buck converter, Fig. 2.1(a), which comprises three components: a semi-conductor switch, diode and an inductor and can be arranged in three forms: buck, boost, buck-boost. The buck circuit is a popular solution for applications with small voltage step-down ratios.

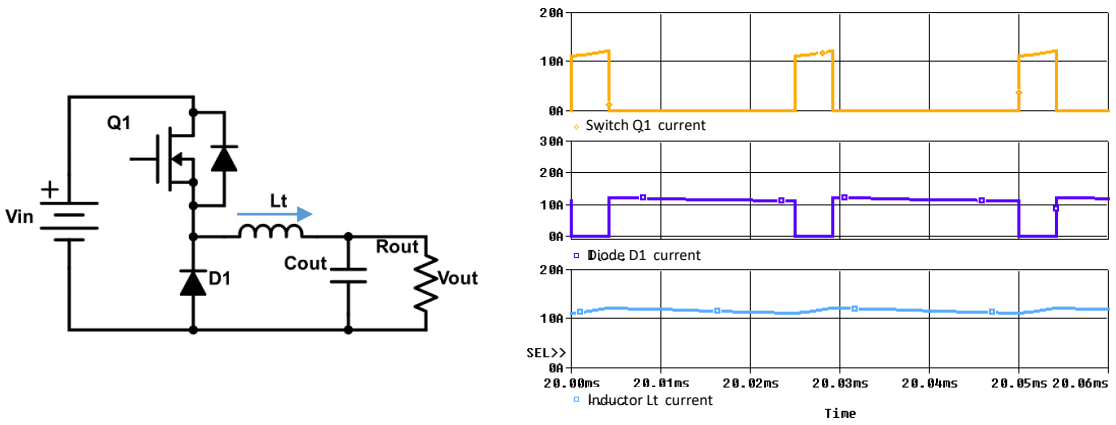
When the main switch Q1 is turned on (for period t_{on}), current flows through it from Vin (input voltage), through the inductor Lt to the output capacitor C1 to support the output voltage (Vout). During this switch on-time (conduction time), energy is delivered from

the input to the inductor. As the current in the inductor increases linearly during the on-time, additional energy is stored in the inductor core.

When Q1 turns off (for period t_{off}), current flow through the inductor cannot step change instantaneously, it can only change continuously due to flux within the core. The inductor voltage can change instantaneously in order to maintain the current continuous. During the off-time, the voltage at the diode's cathode falls until the diode becomes forward-biased. The forward-biased diode conducts the current flowing through Lt thereby providing a continuous current path for the inductor current flow to the output capacitor and the load, R1. Typical waveforms of various circuit elements are shown in Fig. 2.1b.

Continuous conduction is a mode of operation where the inductor current never drops to zero for any period of time. In continuous conduction, the ratio of output to input voltage is the '*duty cycle'*, $\frac{V_{out}}{V_{in}} = \delta = \frac{t_{on}}{t_{on}+t_{off}}$, where δ is the switch on-state duty cycle. It is the percentage of time the switch is turned on during the cycle time period. Buck converters are used extensively in low voltage DC-DC power supplies and LED drivers due to their low cost and simplicity. In LED drivers, both the output voltage and continuous current in the output inductor are controlled by this topology. However, the current drawn from the supply is always discontinuous due to the main switch being connected to the input, so when the switch turns off, no input current can flow.

The buck converter [33] is conventionally limited to a duty cycle in the region of 10% to 90% of the switching period. Below 10%, the primary switch on-time is small, so the peak currents in Q1 become large compared to the average input current, while at the other duty cycle extreme, the peak diode current is large compared to the average output current, rendering the circuit inefficient.



(i) (ii)

Fig. 2.1 Conventional buck converter: (i) Schematic and (ii) simulated currents of Q1, D1 and Lt.

Table 2.2 Buck converter simulation parameters

Component		
Primary Inductor	Lt	484µH
Load	Rout	2Ω
Output Capacitor	Cout	6.8µF
MOSFET RDSon	Q1	1µΩ (assumed ideal)

2.2.3 Buck-Boost Converter

The buck-boost converter is shown in Fig. 2.2. The circuit can provide both boost and buck functions. That is, it can both step-up and step-down. When the switch Q1 is on, the diode D1 is reverse biased and current flows from the supply Vin, storing energy in the inductor Lt. When the switch Q1 turns off the diode becomes forward biased and the inductor current then flows into the output capacitor C1 and load. In the buck-boost converter even when the inductor current is continuous, the current in both the supply side and output side is discontinuous. While operating with continuous current in the inductor $\frac{V_{out}}{V_{in}} = \frac{-\delta}{1-\delta}$, noting that the output is referred in the opposite direction (inverted). If the duty cycle less than 50% the converter will step down (in magnitude) the input voltage, whereas if the duty cycle is above 50% the converter acts as a voltage step-up converter. Since the output voltage in the buck-boost converter is inverted its application is limited. Also, both Q1 and D1 have to be rated to support $V_{in}+|V_{out}|$, whereas in the buck converter Q1 and D1 only have to support Vin.

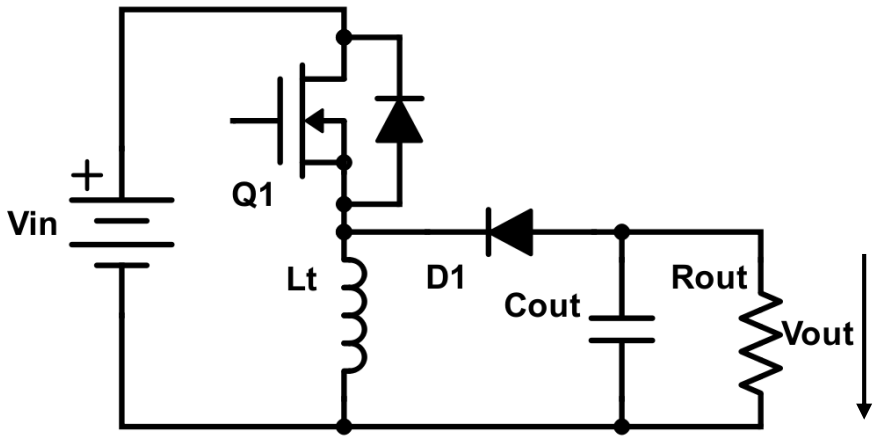


Fig. 2.2 Buck-boost converter

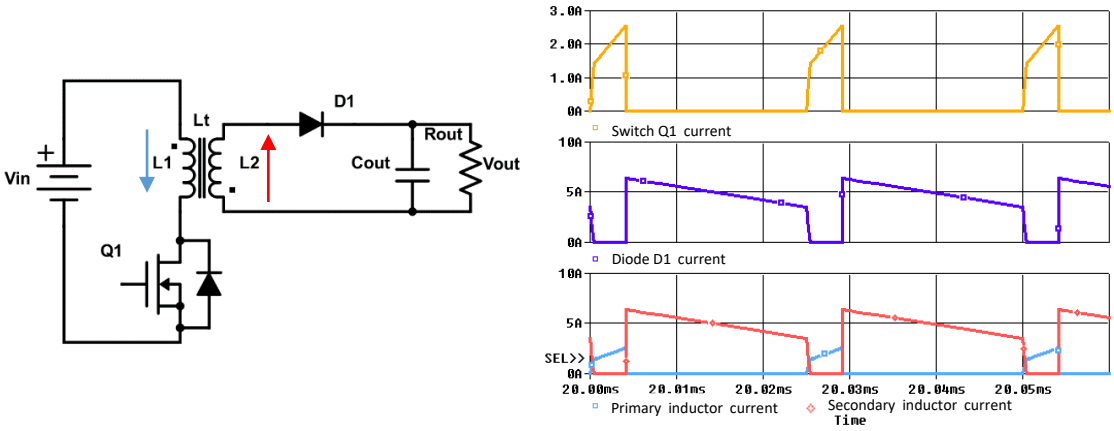
2.2.4 Flyback Converter

The flyback converter [34] is an isolated (coupled circuit) variant of the buck-boost converter. The inductor Lt in Fig. 2.3(a) is a pair of inductors wound on the same core forming an isolated coupled-inductor. The flyback converter can both step up and step down depending on the duty cycle. The coupled inductors both link the same core flux and therefore when Q1 is turned off the current which was flowing in the first inductor is replaced by a current in the second inductor. At any one time current only flows in one winding of the coupled pair of inductors. The energy stored in the core increases during the on-time of Q1 and decreases during its off-time. Fig. 2.3b shows typical circuit waveforms. The flyback converter is one of the most commonly used converters as it provides a wide range of output voltages by variation of the turns ratio of the coupled inductor.

When the flux in the core does not drop to zero $\frac{V_{out}}{V_{in}} = \frac{N2}{N1}\frac{\delta}{1-\delta} = \sqrt{\frac{L2}{L1}}\frac{\delta}{1-\delta}$, where N2 is the turns on L2, the secondary and N_1 is the primary turns, forming L1. The maximum energy that can be transferred is limited by the maximum energy that can be stored in the core volume, viz. $½BH \times Volume$.

The current delivered to the output capacitor of the flyback converter is always discontinuous. Although the flyback converter does not have a continuous current path to

the load when the main switch is on, it does offer the isolation afforded by the magnetic component. A switch clamp circuit is advisable for efficiency and to protect the switches from over-voltages resulting from leakage inductance due to imperfect magnetic coupling [35], [36].



(a) (ii)

Fig. 2.3 Single switch flyback converter: (i) schematic and (ii) simulation currents for switch Q1, diode D1 and the primary and secondary of Lt.

Table 2.3 Flyback converter simulation parameters

Component		
Primary Inductor	L1	484µH
Secondary Inductor	L2	70µH
Load	Rout	2Ω
Output Capacitor	Cout	6.8µF
MOSFET RDSon	Q1	1µΩ (assumed ideal)

2.2.5 Cuk Converter

The Cuk converter [37] uses a coupled-inductor (L1 and L2) (coupling is optional), as shown in Fig. 2.4, and a capacitor C1 to provide a path for continuous input and output currents in both states of the switch Q1. The voltage transfer function of the Cuk converter is the same as the buck-boost converter $\frac{V_{out}}{V_{in}} = \frac{-\delta}{1-\delta}$ with the output also inverted.

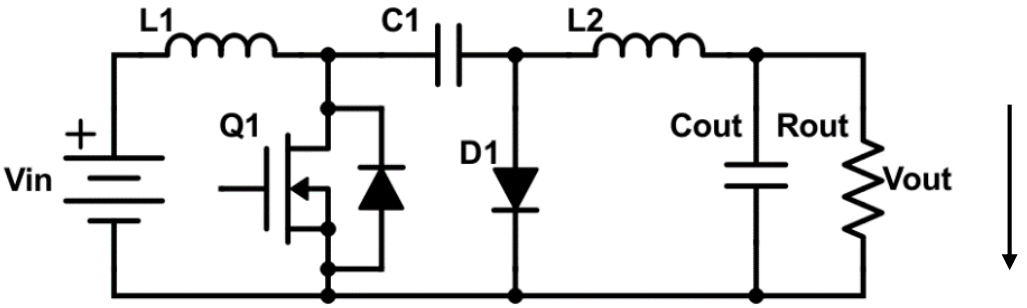


Fig. 2.4 Cuk converter

Fig. 2.5 shows an extension of the basic Cuk converter with the addition of a multistage capacitor [38] and [39], with the addition of a switch and diode to give a larger step-down ratio [40]. Reference [40] reports efficiencies of 77% and 71% at frequencies of 500kHz and 1MHz respectively. The circuit is simple and the control is the same as for a standard Cuk converter, so only requires one control signal as all switches are referenced to a common ground and can be controlled from the same gate driver. However, to obtain the higher efficiencies desired, and the step-down ratio required for desalination, would be a difficult challenge. Additionally, the circuit is not readily reversible. Both this circuit and the basic Cuk converter do however have transformer isolation versions.

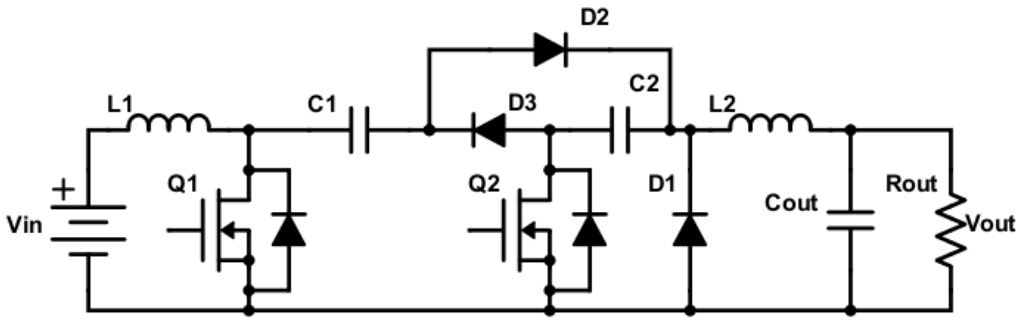


Fig. 2.5 Multi-stage Cuk converter.

2.2.6 Dual Active Bridge Converter

The dual active bridge [30], Fig. 2.6, has been proposed as an isolated and reversible DC-DC converter. With full bridges, one high voltage and one low voltage (for a step-down application) it offers complete control of the power flow in either direction. This flexibility comes at a price with a large number of devices and gate drive circuits. The step-down ratio of the dual active bridge is directly proportional to the turns ratio of the rectangular AC driven transformer. Therefore, for a large step-down ratio, a large turns ratio may impact on coupling factor, hence efficiency.

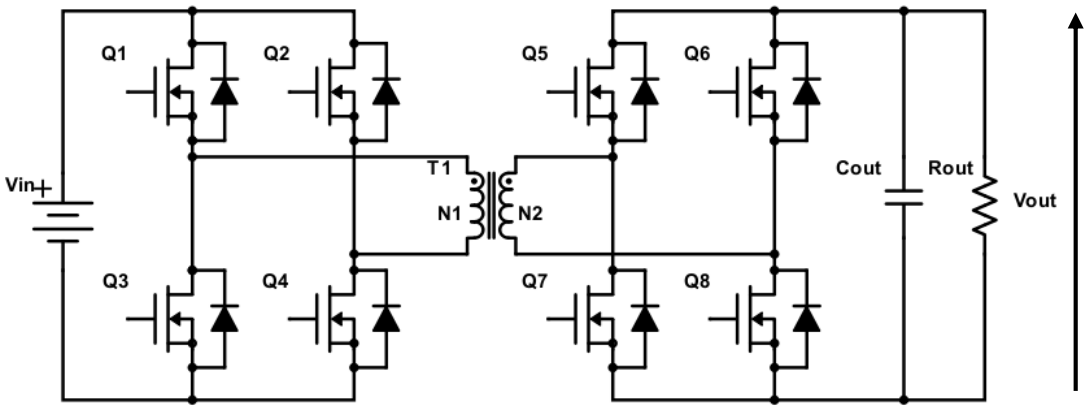


Fig. 2.6 Dual active bridge converter

2.3 Tapped Inductor Topologies

Utilising a coupled or tapped-inductor is a method to achieve large step down ratios. There are many variants of a coupled-inductor topology and these are presented in [41]. In total, 27 single switch/diode/inductor coupled (tapped) inductor buck, boost and buck-boost topologies are described. Each design is suited to different applications. The circuits were all considered to find the most suitable for the water desalination application. The boost topologies within the presented circuits are eliminated from further analysis as voltage step down is required. Equally the buck-boost topologies can step down but

employ some of their dynamic duty cycle range on boost, so only buck tapped inductor topologies need to be considered.

Within the remaining proposed topologies, the windings can either be arranged opposing or in concurrence. Windings arranged in opposition are not considered because they are less efficient due to a coupled current flowing in the opposite direction to the required output current [41]. So every cycle the current in the winding with the lowest number of turns of the two opposing windings must reverse. Although theoretical this is not an issue, this non-productive energy reversal transfer reduces the efficiency due to practical losses in the involved elements. This leaves four buck converters (in [41], termed T1b+, S1+/-, T1+ and S5+/-) in the four parts of Fig 3.7.

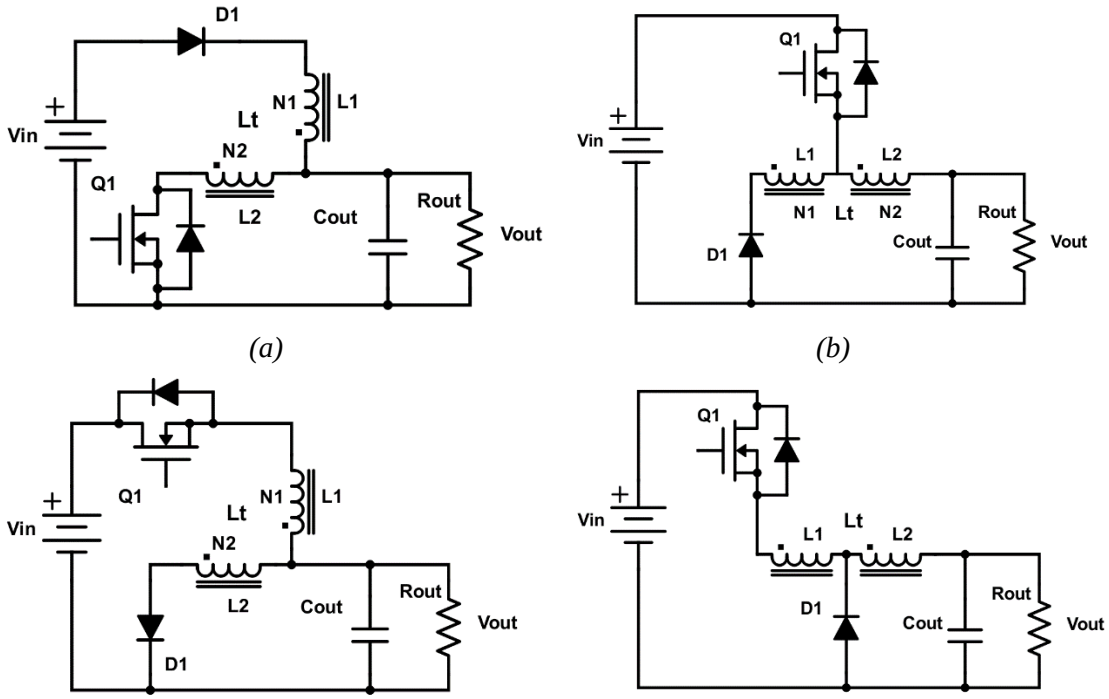


Fig. 2.7 four buck function circuits: (a) T1b+ output tap, (b) S1+/- switch tap, (c) T1+ output tap, (d) S5+/- diode tap [41]

The voltage transfer functions of the four tapped buck converters are [41]:

T1b+:

$$\frac{V_{out}}{V_{in}} = \frac{N(1-\delta)}{N(1-\delta)-\delta(1-N)} \tag{2.1}$$

S1+/-:

$$\frac{V_{out}}{V_{in}} = \frac{\delta}{\delta + N(1-\delta)} \tag{2.2}$$

T1 +/-:

$$\frac{V_{out}}{V_{in}} = -\frac{\delta(1-N)}{N(1-\delta) + \delta(1-N)} \tag{2.3}$$

S5 +/-:

$$\frac{V_{out}}{V_{in}} = \frac{\delta N}{\delta N + (1-\delta)} \tag{2.4}$$

The four transfer functions are plotted in Fig. 2.8. All are a modification to the standard buck converter transfer function, δ. The feature sought for high step down levels is reduced output sensitivity to wide duty cycle variation at low duty cycles. Converters that have the lowest gain at high turns ratio and low duty cycle are candidates, viz. only S5+/-.

Additionally, T1+ can be eliminated because the output is inverted, which creates added complications but no additional benefits. Similarly, T1b+ is removed from consideration due to the switch not isolating the input from the output, so the output voltage is the input voltage when the power is first applied. This would create load cell safety issues as it removes a key fail safe aspect from the process.

For a given step down ratio S1+/- has a much higher output voltage than S5+/-. As a large step down ratio is desired S5+/- should be investigated further as a wide δ range for a low, slow changing output voltage is optimal.

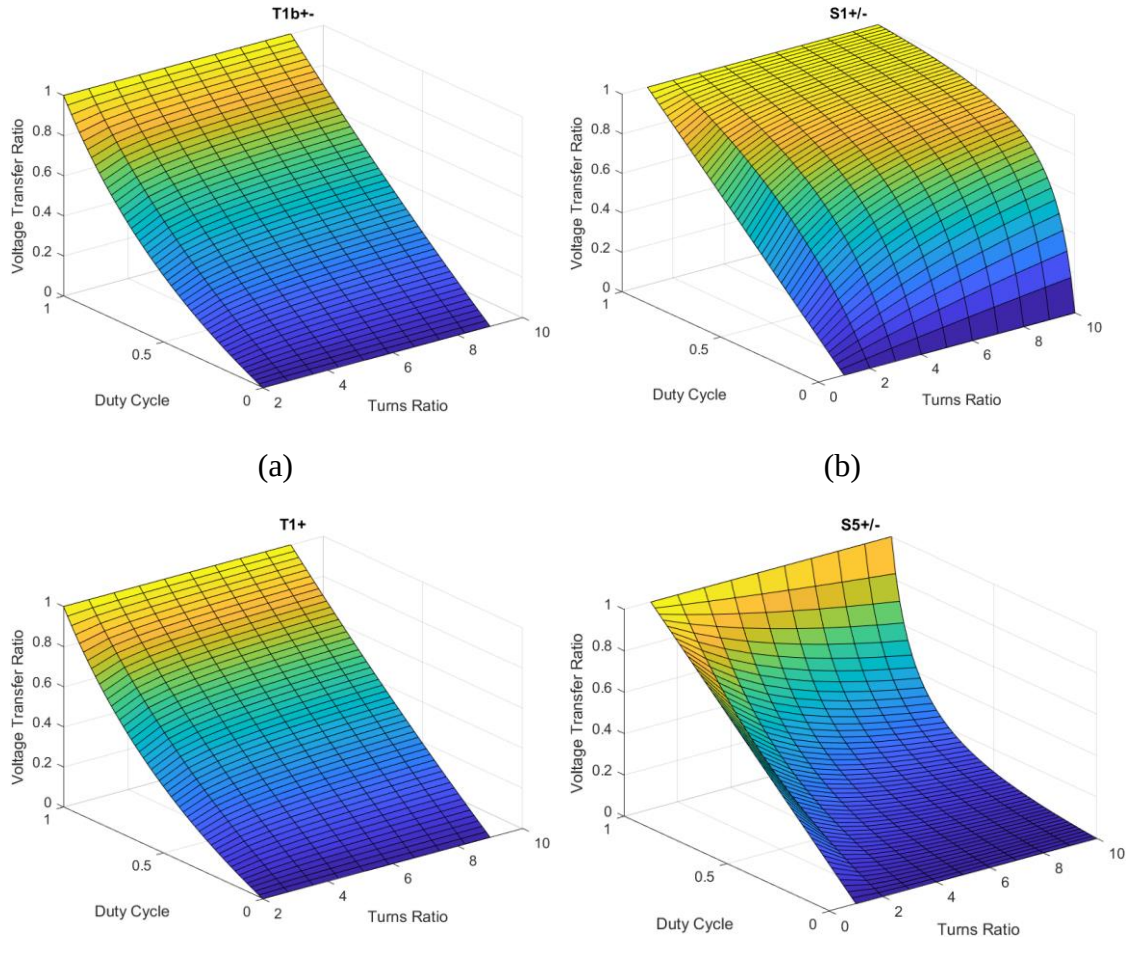
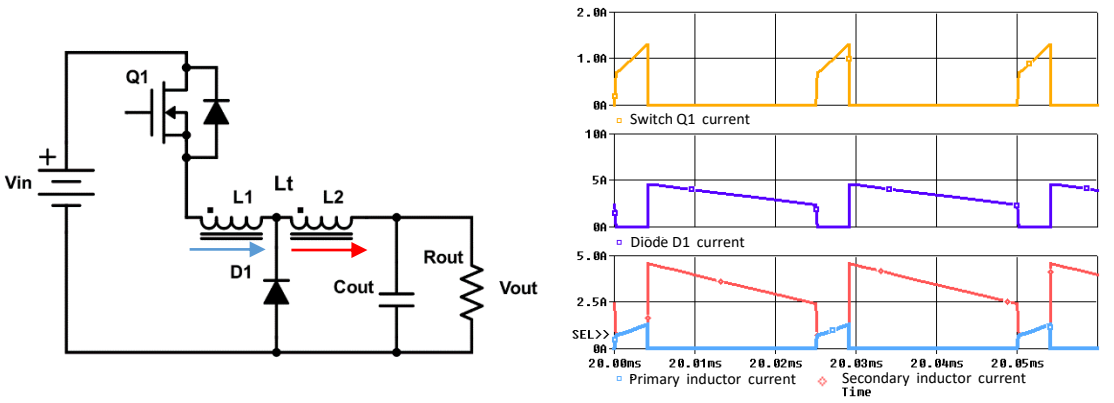


Fig. 2.8 Step down ratio versus duty cycle and turns ratio (a) T1b+/-,(b) S1+/-,(c) T1+,and (d) S5+/-.

2.3.1 Coupled-Inductor Buck Converter

Fig. 3.9(a) (Fig. 3.7(d), S5+/-) shows a coupled-inductor version of the buck converter [42]–[45] in which the single inductor is split into two inductors wound on a single core. The freewheel diode is connected to a common node between the two inductors. This connection of inductors is also referred to as a tapped inductor. [46]

When switch Q1 in Fig. 2.9(a) is on, the current can flow from the input supply through Q1 and Lt (comprising N_1+N_2 turns on a single core) to the output capacitor C1 and load R1. In this state the circuit functions like a standard buck converter with energy building up in the inductor Lt as the current increases. Typical circuit waveforms are shown in Fig. 2.9(b).



(i) (ii)

Fig. 2.9. Coupled-inductor buck converter S5+/- [46]*: (i) Schematic and (ii) simulated currents for switch Q1, diode D1 and the primary and secondary of Lt.*

Table 2.4 Coupled-inductor buck converter simulation parameters

Component		
Primary Inductor	L1	484µH
Secondary Inductor	L2	70µH
Load	Rout	2Ω
Output Capacitor	Cout	6.8µF
MOSFET RDSon	Q1	1µΩ (assumed ideal)

When Q1 is turned off, the diode D1 provides a freewheel path for the current in L2. At the point of switching the flux or MMF in the core must be maintained. The current in L2 increases to a higher value consistent with the terminated current in L1, thereby maintain the same core flux.

$$I_2\ after\ \text{Q1}\ switch\ off = \frac{N1 + N2}{N2} I_1\ before\ Q1\ switching \tag{2.5}$$

With an appropriate choice of turns for L1 and L2, the current which can be delivered to the load during the switch off-time can be significantly higher than the current in the switch while it was conducting. Q1 in Fig. 2.9(a) is therefore rated for a current which can be significantly less than the current in the load.

The diode D1 must be rated to carry the high load current but unlike the buck converter the diode D1 is not rated at the output voltage. When Q1 is on, the supply voltage (minus the small output voltage) is dropped across the series combination of L1 and L2, thereby increasing the voltage rating of D1 in the coupled-inductor buck converter to Vout+V_{L2}.

As with the conventional buck converter in Fig. 2.1, an inductor combines with the output capacitance to create a low-pass output filter. The coupled inductors enable the voltage step-down ratio at a given duty cycle to be greater than that of the conventional variant, as the turns-ratio of the coupled inductor contributes to the overall step-down ratio of the circuit.A feature of the coupled-inductor buck converter is that energy is transferred into the output during both the switch on and off times, due to the output being continuous compared to the flyback converter which has discontinuous output current, but provides isolation. Both the flyback and tapped inductor converters are reversible, once a second switch is utilised across the output diode (both reversibility and synchronous rectification result).

2.4 The Need for Switch Protection

There are two main causes for overvoltage on the primary side of either the coupled-inductor buck or the flyback converter. Either transformer action referring the voltage across the secondary back to the primary or the leakage inductance on the primary winding. The flyback is easier to comprehend so is analysed below.

2.4.1 Transformer Action

To analyse the voltage referred back to the primary side, the total voltage on the secondary side should be evaluated.

Using the arrow directions of Fig. 2.10 (arrow head is positive), the voltage across the secondary winding is

$$V_{L_2} = V_{out} + V_{D1} + V_{Lstray2a} + V_{Lstray2b} + V_{LeakL2} + I_2 R_{L_2}$$

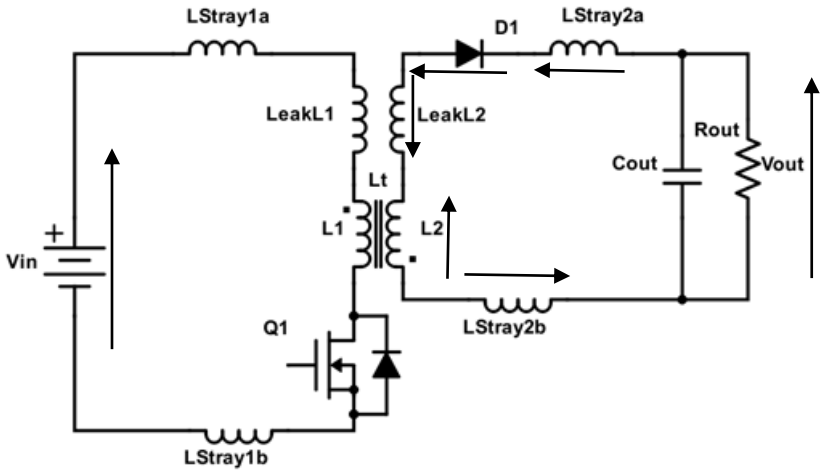


Fig. 2.10 Non ideal voltages seen by flyback converter

During the off time of the switch Q1 there are two situations:

1. The initial transition when there is a large di/dt which develops significant voltages on the leakage inductance of L2 and the stray inductances of the secondary loop. The voltage across the ideal part of the coupled flyback inductor is:

$$V_{L_2} = V_{out} + V_{D1} + V_{Lstray2a} + V_{Lstray2b} + V_{LeakL2} + I_2 R_{L_2}$$

2. The steady state when current has transferred to the secondary, the di/dt is relatively small. The voltage across the ideal part of the coupled flyback inductor is

$$V_{L_2} = V_{out} + V_{D1} + I_2 R_{L_2}$$

In the case of a large step down converter with a very high secondary current and low output voltage, the voltage across the diode and the voltage across the winding resistance of L_2 will be significant. The winding resistance must be minimised and the diode will need to be a synchronous diode function with low channel resistance.

In both these cases the voltage referred back to the primary winding will be in the direction shown in Fig. 2.11 which can then be used to calculate the voltage seen across the main switch Q1.

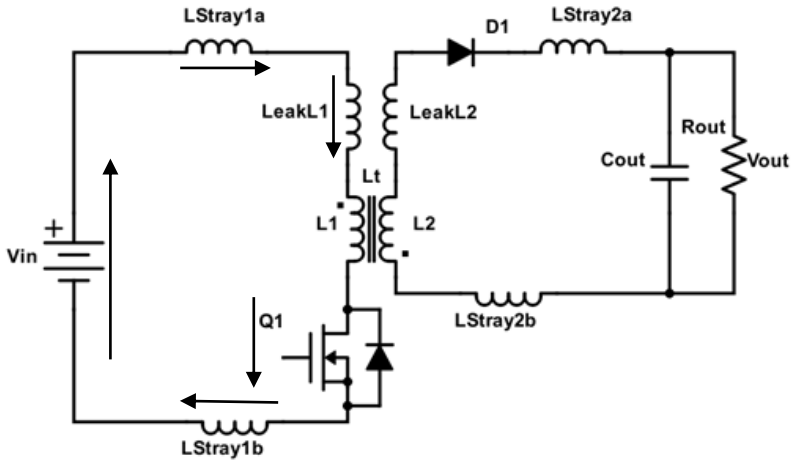


Fig. 2.11 Non idealities on primary side of flyback converter, referred back from the secondary

The referred voltage is givens by

$$V_{L_1} = \frac{N_1}{N_2} V_{L_2} = \frac{N_1}{N_2} \left[V_{out} + V_{D1} + V_{Lstray2a} + V_{Lstray2b} + V_{LeakL2} + I_2 R_{L_2} \right]$$

During the primary to secondary transfer of energy, the primary side di/dt is large and negative, inducing voltages in the direction shown across the primary side stray inductances and the primary side leakage inductance.

However once the energy transfer is complete the di/dt on the primary side disappears but a referred voltage from the secondary to primary remains. The steady state voltage across Q1 during its off condition is therefore

$$V_{Q_{1off}} = V_{in} + \frac{N_1}{N_2} \left[V_{out} + V_{D1} + I_2 R_{L_2} \right]$$

It is vital therefore that the switch protection circuit should avoid clamping the voltage across the switch to lower than this, which would prevent the complete transfer of energy from the primary to secondary. This voltage is shown in the simulations to follow where an ideal inductor is used in series with the load and the diode.

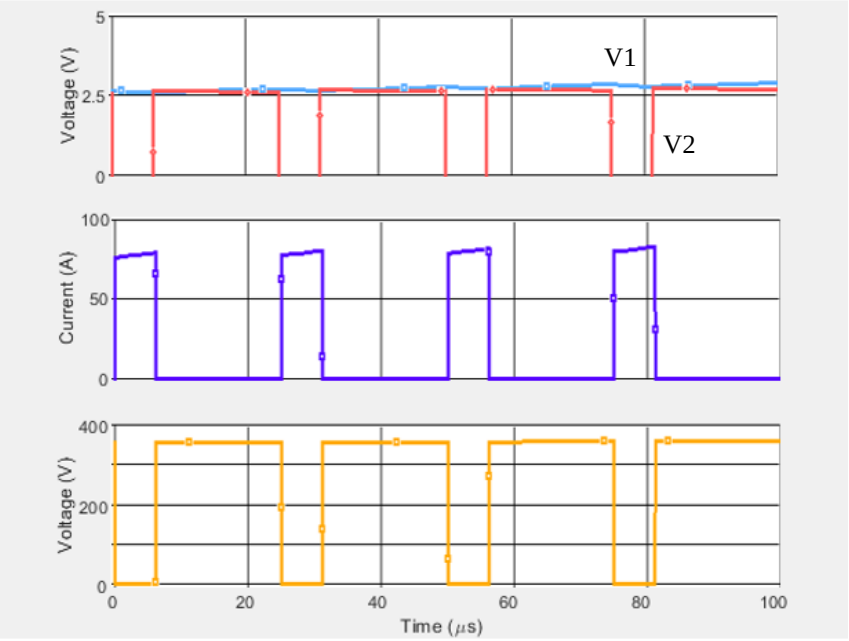


Fig. 2.12 simulation showing referred voltage (a)(V1) Output Voltage (Vout), (a)(V2) Diode Voltage (VD1), (b) Primary (L1) inductor current, (c) Q1 Switch Voltage (Vds)

In the case in Fig. 2.12, with a turns ratio of 10:1, an output voltage of 2.5V and diode loss of 2.5V creating a total of 5V at the output side which referred back through the inductor; creates an additional 50V across the main device. With an input of 300V this explains the 350V seen across the main device during its off time.

2.4.2 Leakage Inductance

Using such an inductor allows for the main switch in the converter to have lower peak and average current. However, the winding of this inductor produces a leakage inductance (the windings are not perfectly coupled) which appears in series with any coupled turns. During the transfer of current from the primary winding to the secondary winding an additional voltage is developed across the leakage inductance; this adds to the voltage across the main switch during the switch off process. This voltage could be in excess of double the input voltage depending on the size of the leakage inductance. For example, for a 600V input the voltage across the switch could be over 1700V for a poorly coupled inductor. An in-depth look at the snubber circuits [47]–[49] used to protect switching devices in coupled-inductor circuits is introduced.

2.4.3 Solutions

A snubber is a circuit that is added to a switching circuit to provide device protection from over-voltage. It limits and modifies the switch VI trajectory and by limiting the sharp rise of voltage across a current switching device in an inductive system; by providing an alternative current path for the device current while the voltage across the device rises. This soft switching characteristic reduces the *dv/dt* causing the over-voltage. Another method of protecting a switch against over-voltage is by adding some form of voltage clamping. These circuits provide switch protection by providing an alternative current path but only when a certain voltage is reached and so the current from the leakage inductance will only flow into a voltage clamp when the voltage has risen above the voltage level of the clamp. This can be achieved by using a diode back to the supply rail or by creating an additional rail voltage. Circuits which provide protection using additional active components are described in Chapter 4. This section concentrates on snubbers which use passive energy management [44] during the switching transition.

2.5 Large Step-Down Voltage Ratio Coupled-Inductor Buck Topology Circuit – snubber and clamping circuits

The circuits in Section 2.2 are common but not necessarily used for high step-down ratios. Various papers have been written adapting some of these circuits to enable large step-down ratios. Some of their findings, concerning snubbers, are outlined in this section. Simulations and experimental results of the proposed tapped inductor topology, S5+/-, and possible switch protection circuits are presented.

Fig. 2.13 (Fig. 2.9(a)) shows the simplest form of the coupled-inductor buck circuit, S5+/-, where Q1 is the main switching device and D1 is the freewheel diode. The coupled inductor Lt with primary L1 and L2 and output capacitor C1 and load R1. The leakage inductance energy causes voltage overshoot on the semiconductors, but that same inductance functions as a turn-on snubber, that is, switch turn-on stressing is not a significant problem.

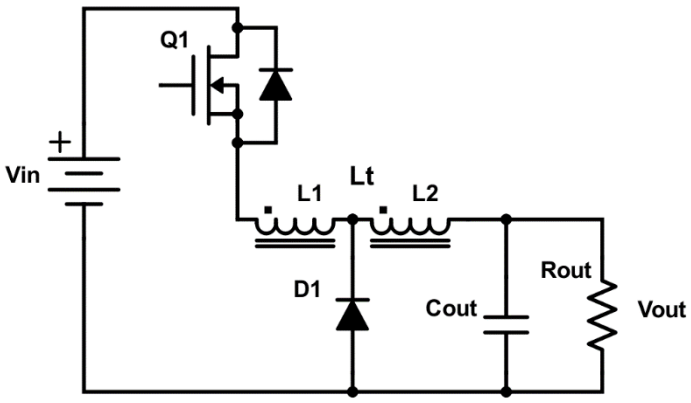


Fig. 2.13 Coupled-inductor buck converter, S5+/-

2.5.1 Ultrahigh Step-Down Converter [50]

A novel design (Fig. 2.14) using a coupled inductor is presented in [50], where the circuit utilises an energy transferring capacitor which purportedly acts as a snubber capacitor. The main switch Q1 and synchronous rectifier Q2 have the same function as Q1 and D1 in Fig. 2.9. The capacitor C1 charges during the on-time of Q1, as shown in the waveform Fig. 2.15 and Fig. 2.16. When Q1 turns off an additional switch and diode conduct while the current in the primary leakage inductance drops to zero. At this point the current in the primary winding reverses and the capacitor partially discharges through Q2 and Q3. Q2 and Q3 turn off and Q1 turns back on for the next cycle. The use of the capacitor, switch Q3 and complementary switch Q2 in this circuit provides clamping of the voltage across the main switch Q1 while providing the path for the current in the leakage inductance. However, the reverse current which flows in the primary winding is detrimental to the overall energy flow and leads to an efficiency reduction.

Although the converter utilises the capacitor in series with the switch and coupled inductor to ensure switch protection, the capacitor is also used for the energy transfer. The significant disadvantage of this converter is this method of switch protection. The switch is clamped using the supply rails to V_{in}, whence the switch is always protected. However, this is also the maximum voltage that is applied across the coupled inductor. A lower voltage across the inductor during the transition increases the time it takes for the transition from the primary to the secondary. In the simulation of this circuit, (Fig. 2.15

and Fig. 2.16) the energy does not finish coupling before the next transition. Various component values were assessed and due to limiting voltage, V_{in}, across the inductor, no improvement was gained. The circuit continues to function with switch protection.

The authors derive an expression for the output voltage, which increases linearly with the main switch duty ratio. According to the simulations this is incorrect as at higher duty ratios the capacitor C1, charges so as to oppose the supply voltage. Thus reducing the voltage applied to the coupled inductor. When the duty ratio is one, the output voltage is zero. The limited operating range and negative primary currents outweigh the main switch snubbering benefits of this circuit.

The desalination application requires the circuit to reverse the power flow to clean and flush the electrodes. Any snubber on the main switch would need to be replicated on the high current low voltage side when the circuit is used to reverse the power flow.

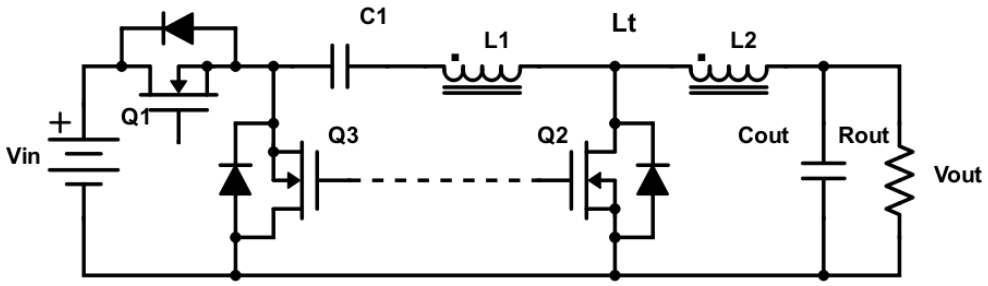


Fig. 2.14 Ultra high step-down ratio converter [50]

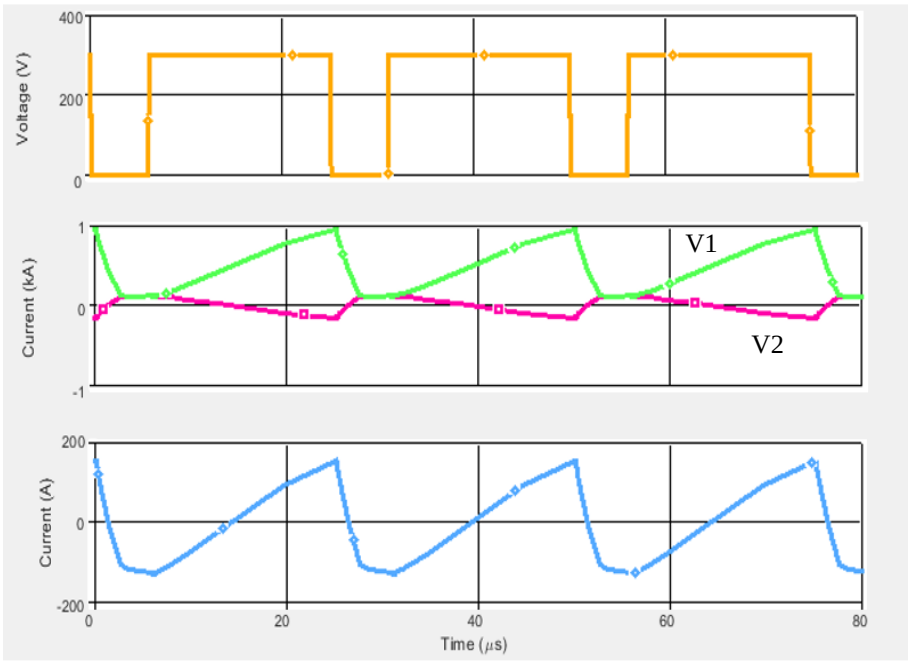


Fig. 2.15 Ultra high stepdown converter simulated with 3:1 turns ratio. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber capacitor (Cs) current

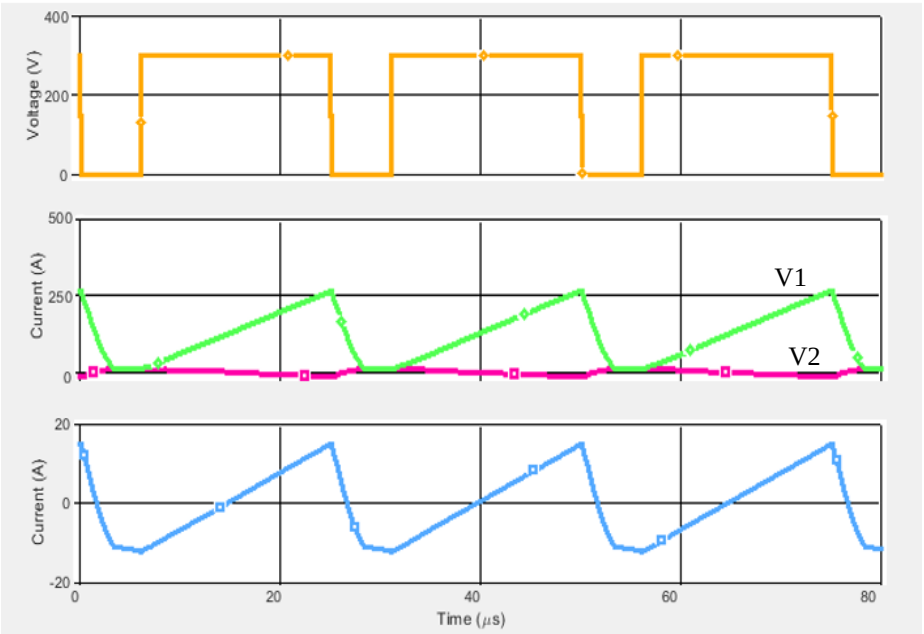


Fig. 2.16 Ultra high stepdown converter simulated with 10:1 turns ratio. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber capacitor (Cs) current

Table 2.5 Ultra high step-down converter simulation parameters

Component		
Primary Inductor	L1	470µH
Secondary Inductor	L2	4.7µH
Snubber Capacitor	C1	
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1/Q2/Q3	1µΩ (assumed ideal)

2.5.2 High Voltage Tapped-inductor Buck Converter – shunt capacitors

Fig. 2.17, [51] is a coupled-inductor buck for a 3kV to 100V step-down converter. Two resonant capacitors C1 and C2 around the high voltage switch and across the low voltage switch allow zero voltage turn-off. However, the capacitor charging time delays the transfer of energy to the secondary of the coupled inductor, making energy transfer less efficient. As a result of these limitations the switching frequency of the converter in [51] was restricted to less than 20kHz.

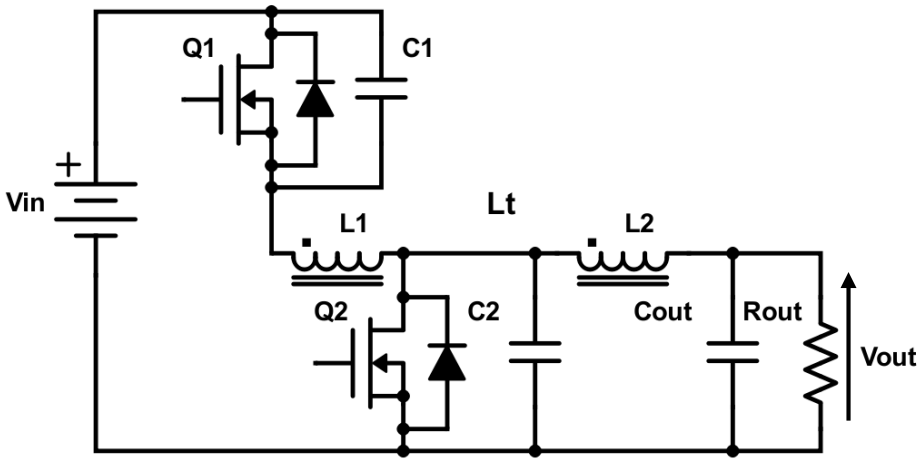


Fig. 2.17 High Voltage coupled-inductor buck converter *S5+/-* with additional shunt capacitors [51]

Circuit topology improvements are suggested in [52], where the gate drive to the high voltage switch can be made autonomous. The high voltage switch is made up of series connected low voltage MOSFETs, each having an autonomous gate driver which makes

it possible to series connect the MOSFETs to make the high voltage switch, each MOSFET having its own self powered and self-timed gate driver. The paper acknowledges that the autonomous gate drive does not provide the accurate timing required for high frequency operation. High frequency operation is advantageous in the coupled-inductor circuits as the inductor physical size and inductance decrease with a higher frequency.

Reference [52] acknowledges the main issue with coupled-inductor circuits which is the over-voltage on the main switch caused by leakage inductance and investigates a different method of minimising the voltage across the high side. It presents the idea of cascading multiple switches. This does not remove the voltage across the switch but simply shares the voltage across the switches. This technique is adequate if it can be assured that the switches turn on and off at the same time otherwise one switch will quickly take the full voltage and fail. It is also less fault tolerant, since if one switch fails it is likely all the switches will then fail.

2.5.3 Tapped-Inductor Buck Converter for High-Step-Down Ratio dc-dc Conversion

In [44] the authors describe how the coupled-inductor buck extends the duty ratio of the main switch when a high step-down ratio is required but highlights that the coupled-inductor buck suffers from two major problems. Firstly, a large voltage overshoot occurs at turn off of the main high voltage switch due to the leakage inductance between the coupled inductor primary and secondary. Secondly, the gate driver of the high voltage switch requires a floating source which means that low cost bootstrap gate drive ICs cannot be used due to the source of the device being connected directly to an inductor. [44] presents a rearranged coupled-inductor circuit topology which allows the uses of a bootstrap gate drive IC. With the rearranged coupled-inductor buck topology a simple lossless snubber is proposed which clamps the turn off voltage spike and recovers the leakage energy.

The proposed circuitry interchanges the inductor and main switch (compare Fig. 2.17 and Fig. 2.18, (Fig. 4 in [44])) which then allows for a diode capacitor diode snubber to be

implemented. The circuit still operates as a conventional coupled-inductor buck converter with the turns ratio of the inductors L1 and L2 still being used in combination with the duty cycle of the converter to step down the input voltage by a large ratio. The issue of leakage inductance is most significant when the primary side switch is turned off as that is when the stored energy associated with the leakage energy is maximum. The proposed snubber uses a capacitor C2 and two diodes, D2 and D3. The capacitor is used to both indirectly protect the device and then to increase the switch on-time current flowing through L2 and the load.

With the primary winding L1 moved to the DC power supply side, the source of Q1 is now connected to the drain of Q2. This means that a conventional bootstrap gate drive IC can be used. Diodes D2 and D3 are added with a voltage clamping capacitor C2 to provide a lossless clamp circuit.

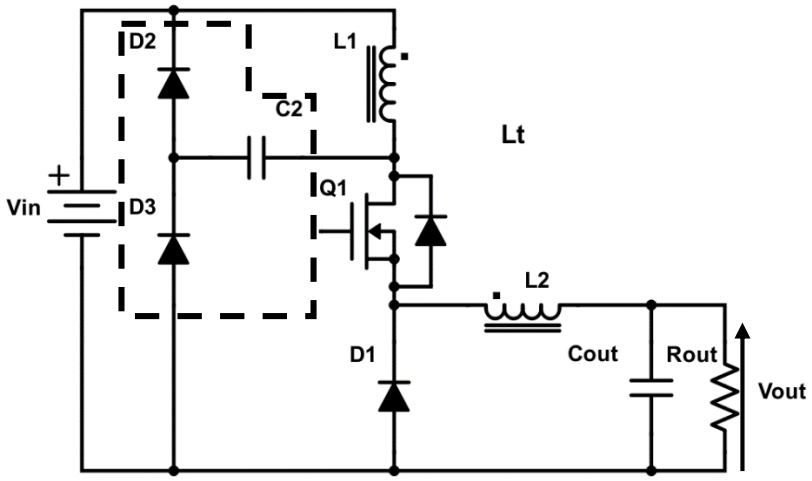


Fig. 2.18 Coupled-inductor buck converter S5+/- with DCD snubber,(Fig. 4 in [44]*).*

The built experimental 12V to 1.5V/50A circuit [44] for desalination showed that the coupled-inductor circuit with the lossless voltage clamp was more efficient than the coupled-inductor buck without voltage clamp and significantly more efficient than the standard buck converter. Also their coupled-inductor design used planar tracks on the PCB with an E-core and I-core ferrite completing the magnetic path. An interleaved control strategy for a four phase converter was used, and two pairs of coupled inductors share the same core.

Although the snubber is effective, the simulations in Fig. 2.19 and Fig. 2.20 show high switch current flowing in Q1 when Q1 is turned on. The snubber capacitor has been charged after the previous turn off action. When Q1 is turned back on the current in inductor L2 flows from the capacitor Cs until the current builds (due to leakage) up in L1. In the case of using this circuit for a large step-down ratio, the discharge current flowing through Q1 during the initial part of the switch on time can reach the high load current level, specifically the current level in L2. This is a significant disadvantage as one of the key features of the coupled-inductor buck circuit is the ability for the primary switch to only see low currents and high voltage and similarly the secondary switch Q2 to only experiences high currents and low voltages. With this circuit the primary switch Q1 would have to be rated to both the maximum voltage and the maximum load current which would significantly increase in cost and decrease efficiency due to the higher $R_{DS(on)}$ associated with higher voltage rated devices.

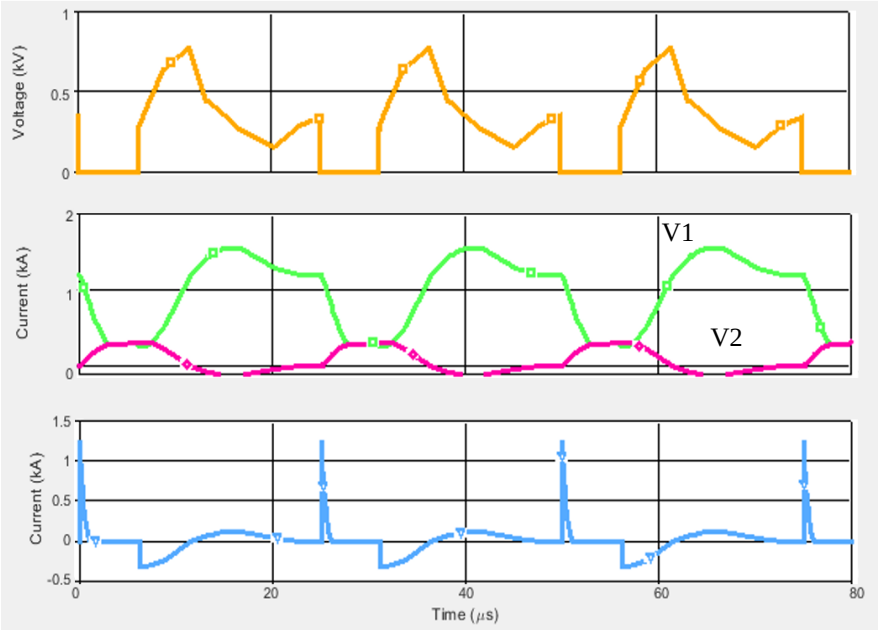


Fig. 2.19 Coupled-inductor buck converter simulated with 3:1 turns ratio in N1:N2. A 1000A capacitor current flows through Q1. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber capacitor (Cs) current

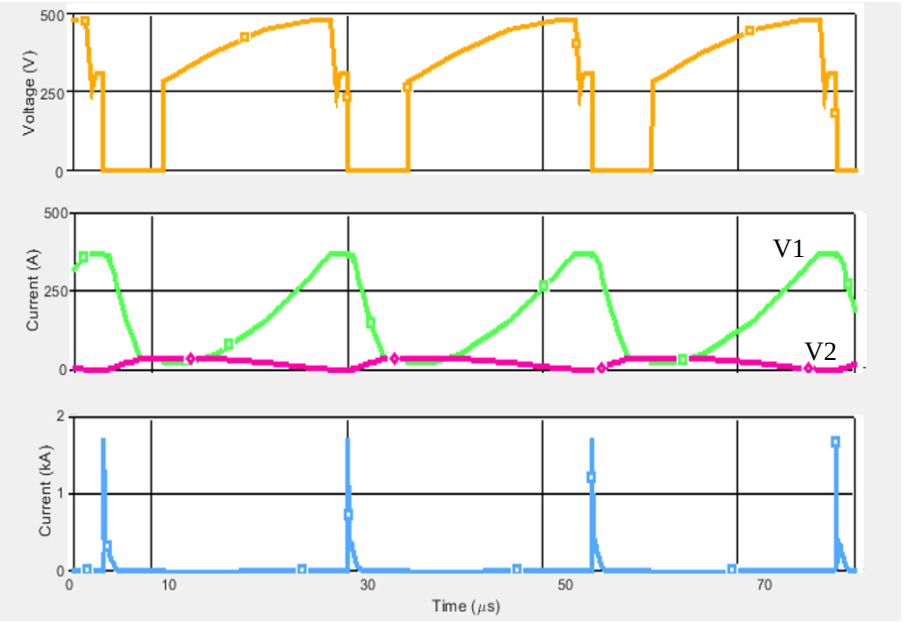


Fig. 2.20 Coupled inductor buck converter simulated with 10:1 turns ratio in N1:N2. A 1500A current pulse flows through Q1. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber capacitor (Cs) current

Table 2.6 DCD snubbered converter simulation parameters

Component		
Primary Inductor	L1	470µH
Secondary Inductor	L2	4.7µH
Snubber Capacitor	C2	2µF
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1/Q2/Q3	1µΩ (assumed ideal)

2.5.4 DCDL Coupled-Inductor Buck

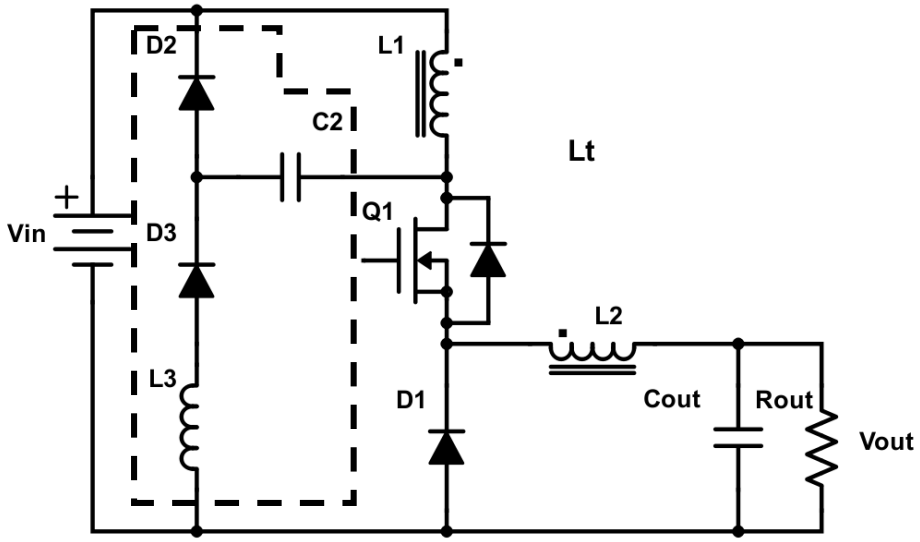


Fig. 2.21 Inductor added to DCD snubber for controlled discharge current

The addition of an inductor in series with D3 allows for the discharging current through Q1 to be controlled. The DCDL snubber is a viable method of controlling the over-voltage on the switch. The snubber is effective, simple, passive, and low-cost. However, the resonant version which is 100% efficient has a minimum on time and results in higher peak currents in the output. Fig. 2.23. Alternatively, the circuit in Fig. 2.21, uses the capacitor as a clamp across the switch by using a larger capacitance value, this creates a more continuous output current however requires the initial energy to charge the capacitor to the desired voltage.

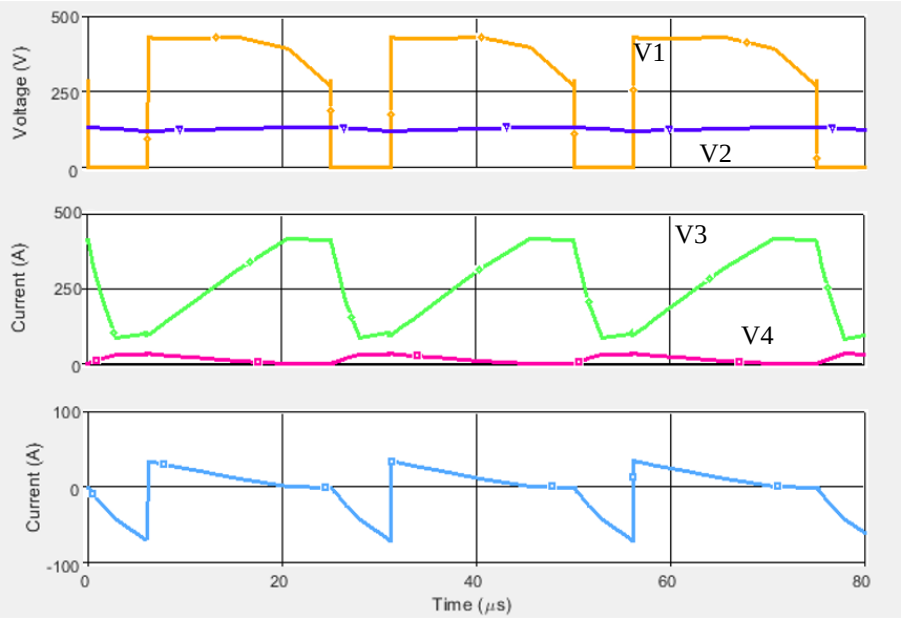


Fig. 2.22 DCDL snubber using 20μF capacitor and 10μH inductor to create clamp operation. (a)(V1) Q1 Switch Voltage (Vds), (a)(V2) Capacitor Voltage (Vcap), (b)(V3) Secondary (L2) inductor current, (b)(V4) Primary (L1) inductor current, (c) Snubber capacitor (C2) current

Table 2.7 DCDL snubbered converter simulation parameters(tank capacitor)

Component		
Primary Inductor	L1	470μH
Secondary Inductor	L2	4.7μH
Snubber Capacitor	C2	20μF
Snubber Inductor	L3	10μH
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1	1μΩ (assumed ideal)

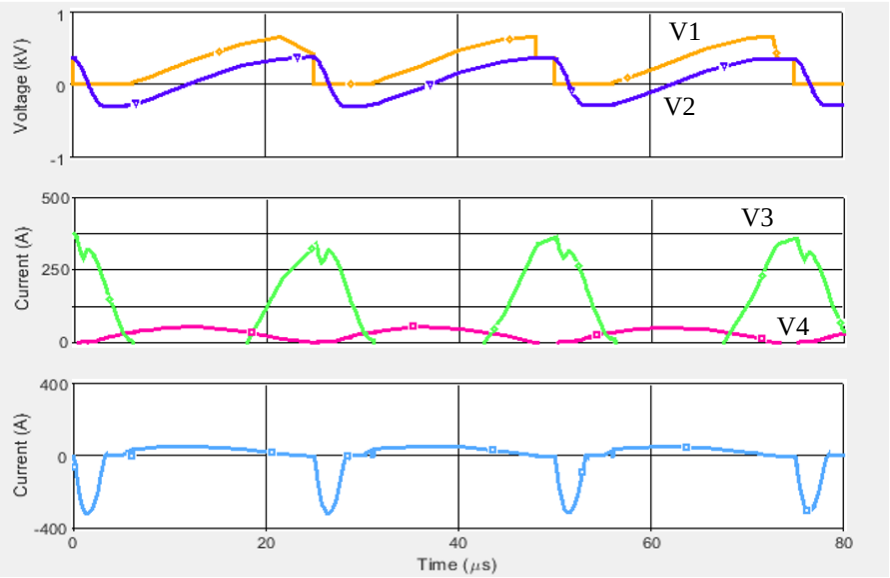


Fig. 2.23 DCDL snubber using 2μF capacitor and 1μH inductor to create resonant operation. (a)(V1) Q1 Switch Voltage (Vds), (a)(V2) Capacitor Voltage (Vcap), (b)(V3) Secondary (L2) inductor current, (b)(V4) Primary (L1) inductor current, (c) Snubber capacitor (C2) current

Table 2.8 DCDL snubbered converter simulation parameters(resonant capacitor)

Component		
Primary Inductor	L1	470μH
Secondary Inductor	L2	4.7μH
Snubber Capacitor	C2	2μF
Snubber Inductor	L3	1μH
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1	1μΩ (assumed ideal)

Various passive lossy snubbers are now presented that can offer protection from switch over-voltage. These are simulated when acting on the main switch of the coupled-inductor buck converter. Results and analysis are detailed.

2.5.5 RC Snubber

An RC snubber, Fig. 2.24, uses the series combination of a resistor and capacitor to damp the over-voltage seen by a device. The capacitor C1 charges with the current caused by the leakage inductance. The voltage drop across resistor R1 creates a larger voltage at the switch node than at the capacitor which reduces the amount of current flowing into (and

out) the snubber. The current flowing into the capacitor increases its voltage thus increases the voltage at the switch node. When the switch is turned back on the current discharges from the snubber back into the same node so depending on the switch position this could simply send the current to ground or be reused in the circuit. The circuit serves its purpose but the snubber is inefficient due to current passing through the resistor.

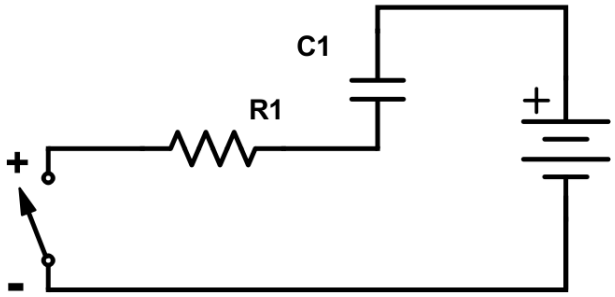


Fig. 2.24 RC Snubber

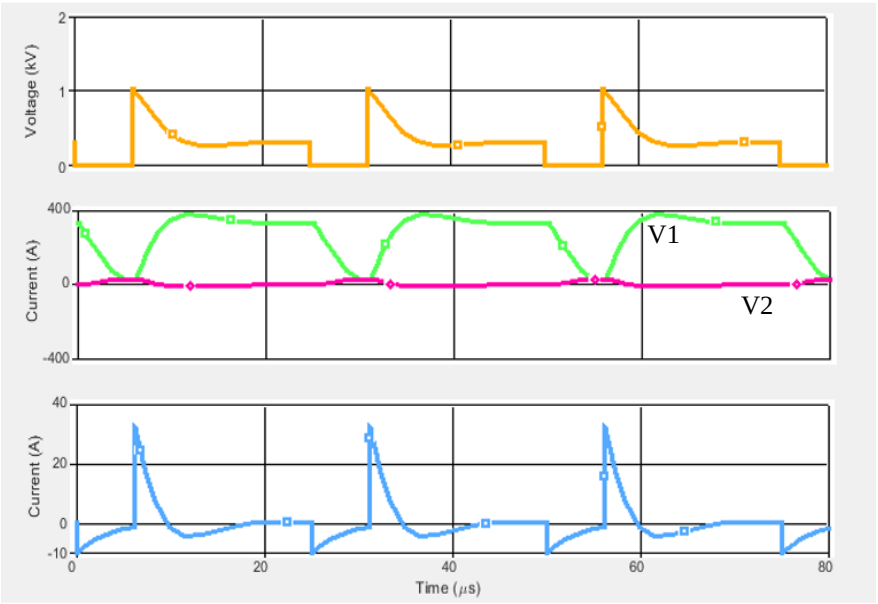


Fig. 2.25 RC Snubber simulation. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber capacitor (C1) current

Table 2.9 RC snubbered coupled-inductor buck converter simulation parameters

Component		
Primary Inductor	L1	490µH
Secondary Inductor	L2	4.9 µH
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1/Q2	1µΩ (assumed ideal)
Snubber Resistor	R1	20Ω
Snubber Capacitor	C1	100nF

2.5.6 RCD Snubber

The RCD snubber [53], Fig. 2.26, is similar to the RC snubber, but with a diode in parallel with the resistor. The diode ensures a low resistance current path from the switch to the capacitor. The losses are halved, being reduces from CV^2 for the RC to $½CV^2$ for the RCD snubber.

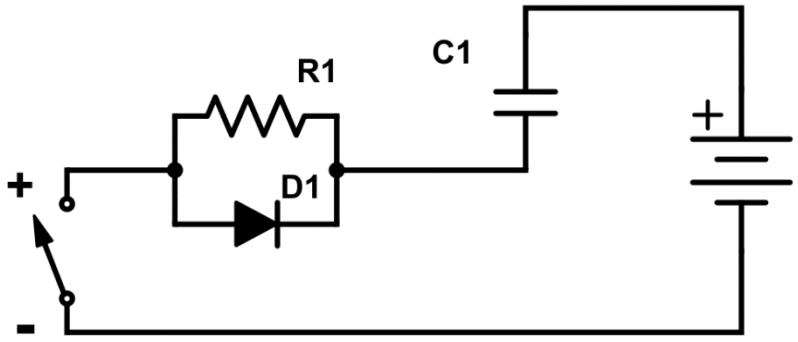


Fig. 2.26 RCD Snubber

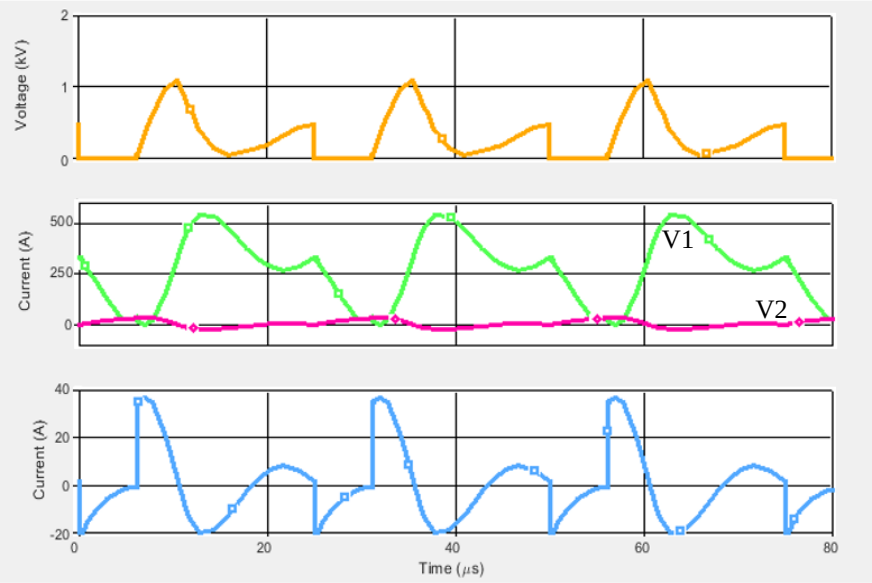


Fig. 2.27 RCD Snubber 10:1. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber capacitor (C1) current

Table 2.10 RCD snubbered coupled-inductor buck converter simulation parameters

Component		
Primary Inductor	L1	490µH
Secondary Inductor	L2	4.9 µH
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1/Q2	1µΩ (assumed ideal)
Snubber Resistor	R1	20Ω
Snubber Capacitor	C1	100nF

2.5.7 RCD Clamp (Pre-charged)

This second RCD arrangement allows the snubber to remain pre-charged to the rail voltage and behave more like a clamp. The voltage at the cathode of the diode will never fall below the supply rail. When the voltage across the switch rises above the supply rail current begins to flow into the snubber capacitor. At switch turn-on the capacitor discharges back to the supply rail through the resistor. This snubber R creates a less resonant response. But in all passive snubbers involving resistance, the losses are related to the leakage inductance, $\frac{1}{2}L_\ell I^2$.

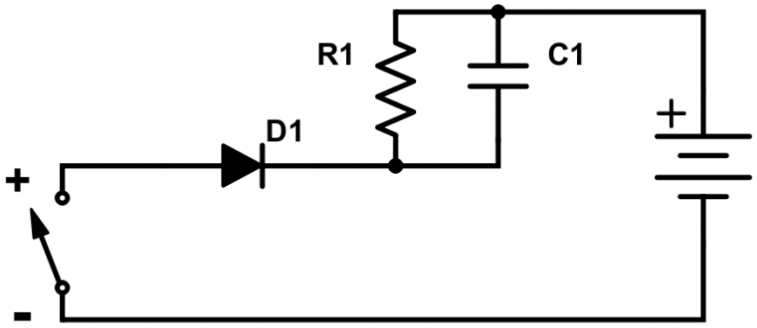


Fig. 2.28 RCD Snubber

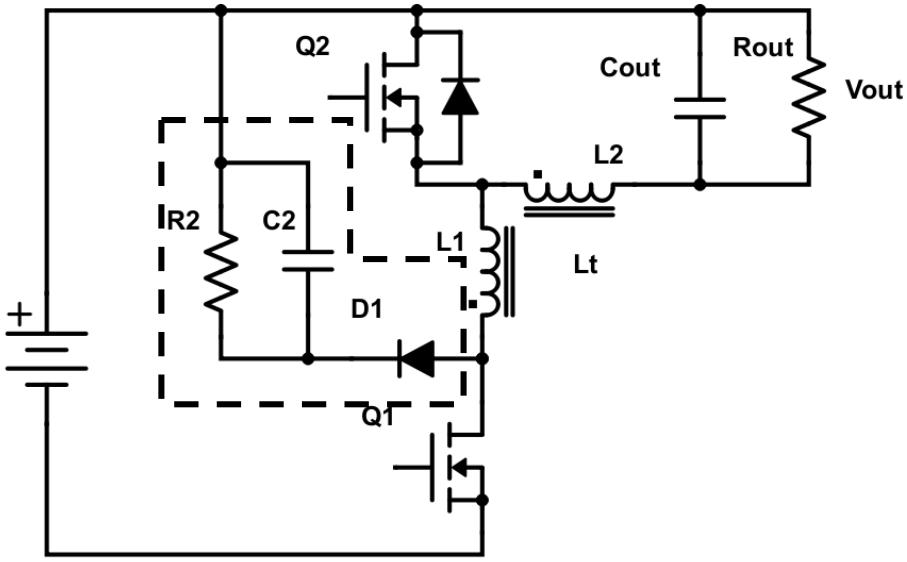


Fig. 2.29 Passive snubber implementation. The S5+/- circuit, but with the topology rearranged so the main switch is referenced to 0V.

The RCD snubber was simulated to be compared against the other switch protection circuits. The simulation used a tapped inductor turns ratio of both 3:1 (Fig. 2.30) and 10:1 (Fig. 2.31) with the secondary winding in both cases having an inductance of 4.7 µH. The simulations show the voltage across the main device Q1, the primary and secondary currents, and the snubber current. The RCD snubber voltage is also shown overlaid on the switch voltage to show that the voltage drops to zero each cycle and is acting as a snubber and not a clamp.

The RCD snubber negatively affects the transition time between the primary and secondary as the capacitor allows a path for the current in the primary to continue flowing and as such the desired high current is flowing through the output for less time.

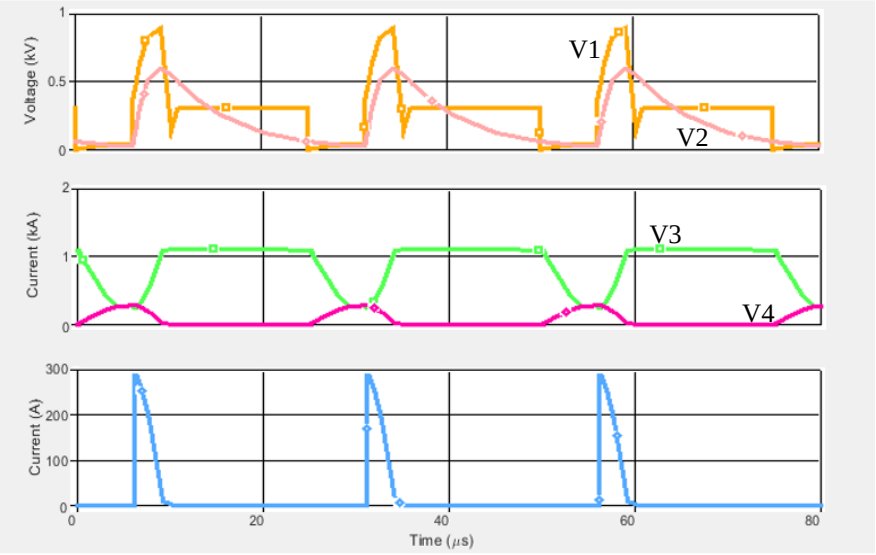


Fig. 2.30 RC snubber simulation with 3:1 turns ratio, C2=700nF, R2=10ohm. (a)(V1) Q1 Switch Voltage (Vds), (a)(V2) C2 Voltage, (b)(V3) Secondary (L2) inductor current, (b)(V4) Primary (L1) inductor current, (c) Snubber Diode (D1) current

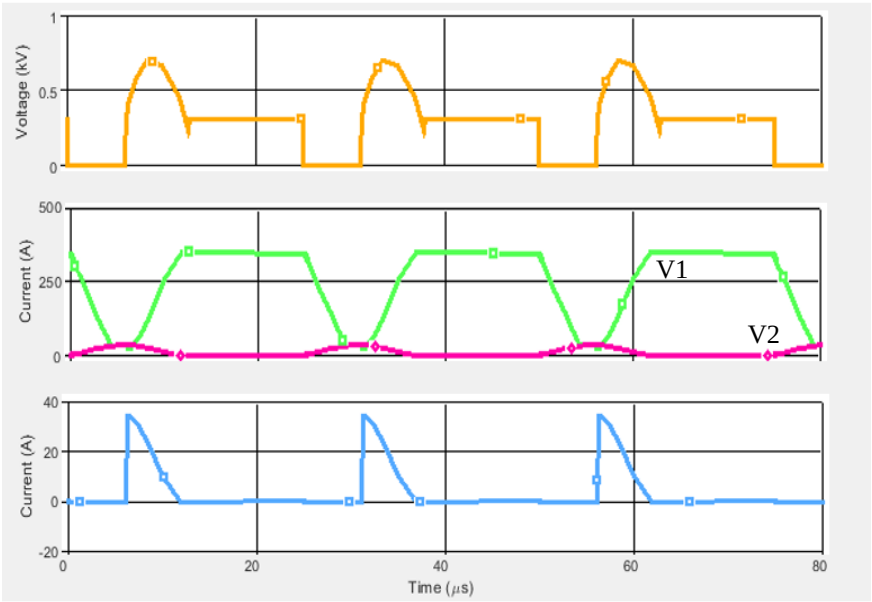


Fig. 2.31 RC snubber simulation with 10:1 turns ratio, C2=700nF, R2=10Ω. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber Diode (D1) current

Table 2.11 RCD (precharged) snubbered coupled-inductor buck converter simulation parameters

Component		
Primary Inductor	L1	490µH
Secondary Inductor	L2	4.9 µH
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1/Q2	1µΩ (assumed ideal)
Snubber Resistor	R1	10Ω
Snubber Capacitor	C1	700nF

Fig. 2.32 illustrates the practical operation of the passive snubber in Fig. 2.29. Fig. 2.32 shows the currents in the coupled inductor L1 and shows that the voltage across Q1, is limited to twice the input voltage (288V in this case).

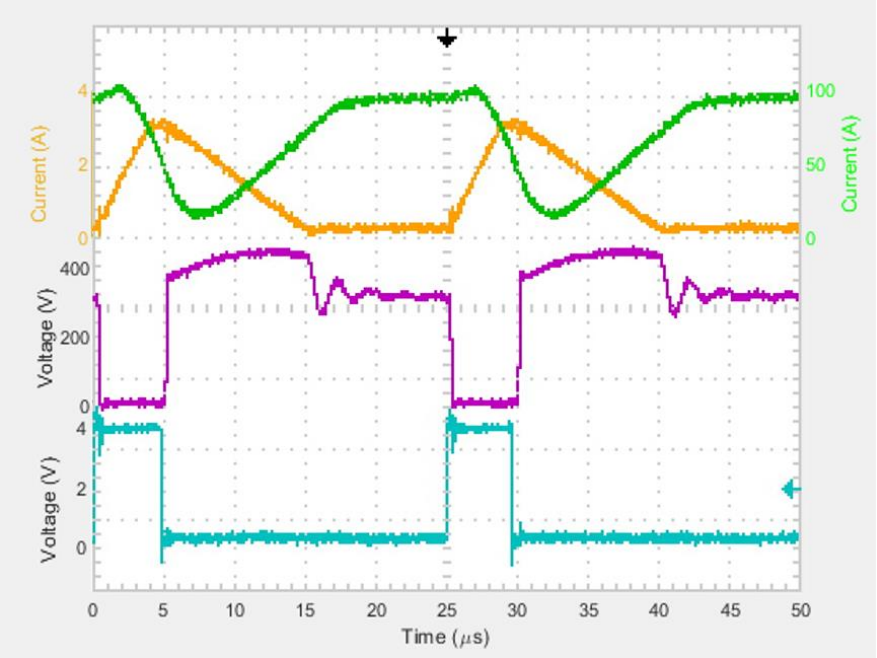


Fig. 2.32 Passive RC snubber experimental testing (hardware details described in Section 4.5, Table 3.4) (a) Secondary (L2) inductor current, (b) Primary (L1) inductor current, (c) Q1 Switch Voltage (Vds), (d) Q1 Gate Signal (Vgs)

2.5.8 ZRC Snubber

A Zener diode snubber circuit, Fig. 2.33, uses the diode's Zener threshold voltage V_Z to limit the maximum voltage across the main switch Q1. When V_Z is reached due to current

flowing in the leakage inductance, current begins to flow through the Zener diode back into the input supply rail. The Zener diode is a diode that acts like an ordinary diode unless the diode is reversed biased by a voltage greater than its reverse breakdown threshold voltage. At this point the Zener can conduct in reverse against the direction of a conventional diode. V_Z is a set variable depending on the Zener and so a large range of voltages can be chosen. For high voltages multiple Zener diodes can be put in series to increase the effective V_Z. This proposed design would be a cheap and simple way to implement a clamp. However, it offers decreased efficiency in comparison to some of the alternatives presented later in this thesis. For a large threshold voltage, the power could exceed the power ratings of available Zener diodes. This snubber offers a low-cost solution for applications where efficiency is not the primary objective.

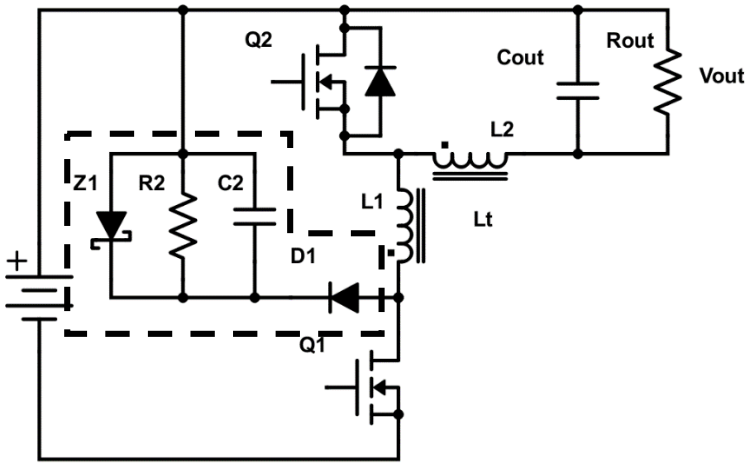


Fig. 2.33 ZRC snubber circuit

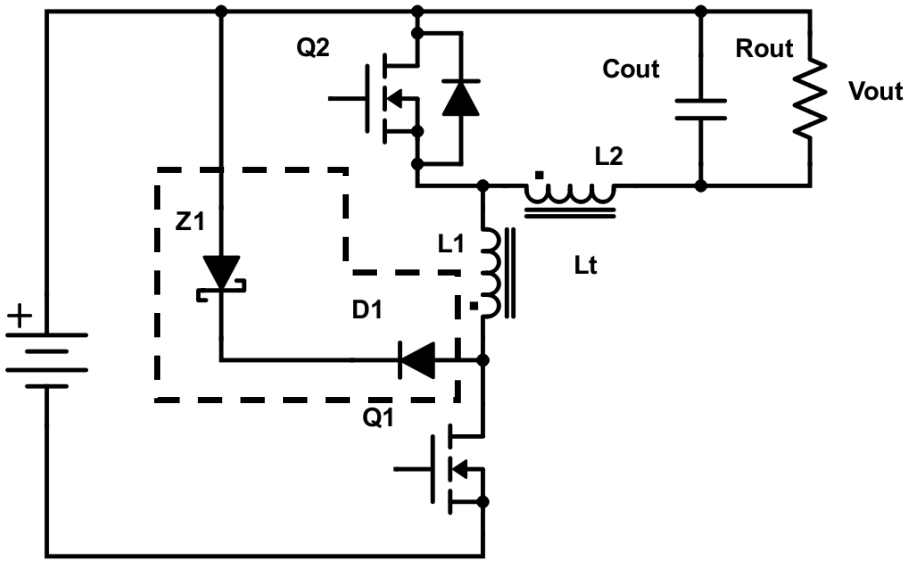


Fig. 2.34 Zener diode snubber circuit

The Zener diode snubber circuit was simulated with identical conditions to the RCD snubber. The Zener diode with a threshold voltage of 600V with a 3:1 turns ratio, and 400V for the 10:1 turns ratio, to demonstrate how variation changes circuit conditions. The Zener threshold voltage is added to V_{in} (300V in this case) to give the peak voltage across Q1.

The difference between 3:1 Fig. 2.35 and 10:1 Fig. 2.36 plots, apart from the turns ratio, is the different peak voltage across Q1. Setting this to a lower voltage creates a slower transition of current from the primary into the secondary. This slower transition time, similarly to the RCD snubber, means a high secondary current is flowing through the load for less time.

The difference between the RCD snubber and the Zener diode snubber is the additional energy that is absorbed by the RCD snubber. The RCD snubber discharges to zero volts across the capacitor every cycle and has to be charged from zero up to the voltage point above the switch. This means that additional energy flows into the RCD snubber compared to the Zener diode snubber which is effectively inactive until the voltage of the node above Q1 is greater than the zener threshold voltage.

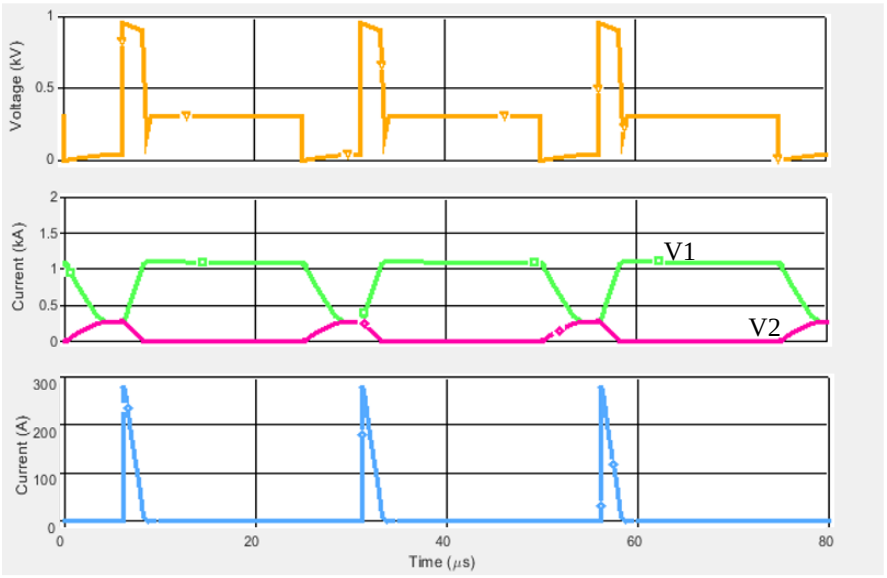


Fig. 2.35 Zener snubber simulation with 3:1 turns ratio and 600V Zener diode threshold voltage. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber Diode (D1) current

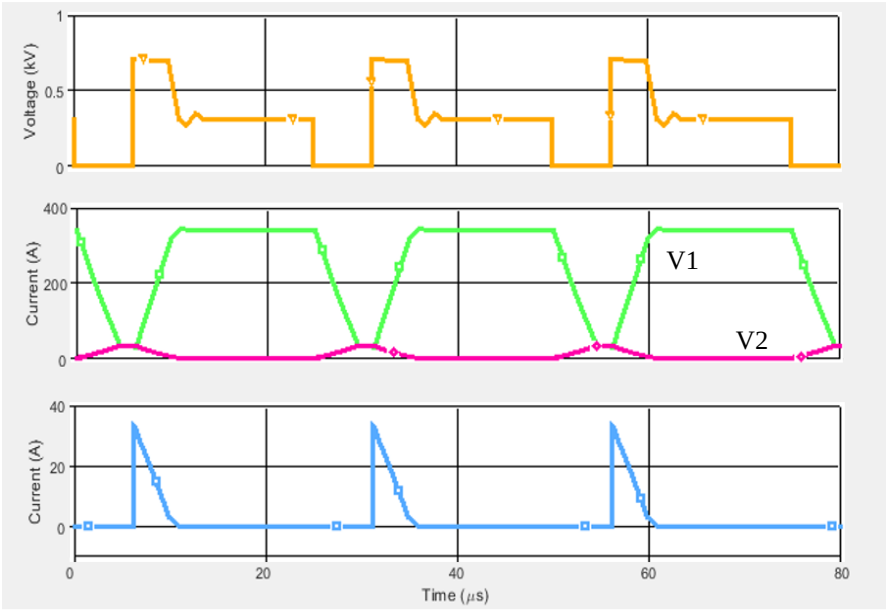


Fig. 2.36 Zener snubber simulation with 10:1 turns ratio and 400V Zener snubber threshold voltage. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber Diode (D1) current

Table 2.12 Zener snubbered coupled-inductor buck converter simulation parameters

Component		
Primary Inductor	L1	490µH
Secondary Inductor	L2	4.9 µH
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1/Q2	1µΩ (assumed ideal)
Zener Threshold Voltage	Z1	600V/400V

A range of snubbers and clamping circuits have been presented in this section. Snubbers offer a current path at all points in the switching cycle whereas clamps only allow current to flow above a certain voltage. Snubbers reduce the *dv/dt* or slope of turn off whereas a clamp does not until the clamp voltage level is reached. For circuits where coupled-inductors are utilised it is worth considering that reducing the *dv/dt* will then increase the amount of time for the energy to transfer from one winding to the other, which decreases the efficiency.

2.6 Summary

The design of a power supply with 600:1 step down ratio is a challenge. Prior art circuits would typically achieve this with multiple stages, each stage introducing losses. For this project a single stage, reversible coupled-inductor circuit will be investigated, since basic simulation indicates the viability of achieving a step-down ratio of 600V to 1V with the one power conversion stage. One objective of the research is to achieve the voltage step-down in one stage.

There is significant research on the coupled-inductor buck converter. However, nobody pushes the circuit to the step down ratio of 600:1. The over voltage across the main switching device has attracted research involving snubbers and leakage inductance minimisation. Leakage inductance minimisation research produced good results but not at the proposed high ratio. As such a combination of good winding practice and a novel snubber design will be required.

This chapter presented and analysed several passive switch protection circuits. These circuits can be readily added to any circuit and can offer significant benefit to the circuit.

In each circuit the turn-off snubber capacitor can either be referred to the supply rail or to the ground rail. The circuits presented are all shown with the capacitor connected to the supply rail as this enables the capacitor rating to be significantly low in this application (voltage rating reduced by the rail voltage magnitude). The main issue with all of passive snubber circuits is the voltage at which the snubber becomes active and the efficiency.

Chapter 4 will investigate the use of active snubbers as an alternative to passive snubbers. These have the potential to have a higher efficiency but with the possible drawbacks of extra cost and complexity.

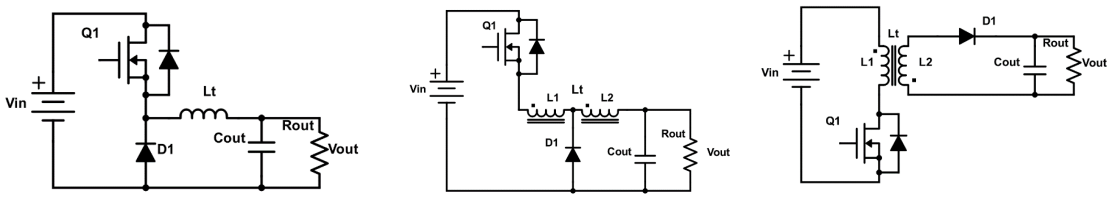
Chapter 3 Flyback and Buck Circuit Alternatives for High Step-Down Voltage Ratios

This chapter compares three step-down converters, viz., the buck, coupled (tapped) inductor buck and flyback converters, to investigate the use cases for when each of these common step-down converters should be utilised, and whether there could be advantages to utilising one over the others. [54]

3.1 Comparison of Buck Circuits

Chapters 1 and 2 presented the task to be addressed and the possible circuits and topologies that could be utilised. Most papers discussing large step-down ratio circuits use the coupled-inductor buck converter. However, at which step-down ratio it is advisable to switch from the buck converter to the coupled-inductor buck converter? The flyback converter can also compete with the coupled-inductor buck converter with specific advantages and disadvantages. This chapter aims to quantify the applications and step down ratios where each converter would be best suited.

This chapter compares the performance of three single stage circuit topologies that can be used to achieve a wide range of step-down ratios, and makes recommendations with regards to the most appropriate topology for a given application. The flyback converter (an isolated version of the buck-boost converter), coupled-inductor buck converter, and buck converter are analysed. The flyback converter and coupled-inductor buck converter are then evaluated using simulation and experimental studies to investigate the effect of turns ratio on circuit performance.



(a) *(b)* *(c)*

Fig. 3.1 Circuit schematics of (a) Buck converter, (b) Coupled-inductor buck converter, (c) Flyback converter

In order to compare the circuits and develop selection criteria for a given application the circuits must be analysed to highlight their advantages and disadvantages. Table 3.1 summarises the comparison between the buck, coupled-inductor buck, and flyback converters. Dual-switch versions of the flyback and coupled-inductor converters may be realised to eliminate the problem of over-voltage on the main switch due to the leakage inductance, [55]–[58]. However, this investigation is restricted to single-switch variants.

Table 3.1 Summary of main properties of buck, coupled-inductor buck, and flyback converters

Feature	Buck Converter	Coupled-inductor Buck Converter	Flyback Converter
Minimum number of devices	One main switch and one freewheel device		
Magnetics			
Connections to wound inductor	2 connections, one winding	3 connections, two windings	4 connections, two windings
Isolation	No		Yes
Energy storage	Some energy is delivered to the load during on-time so energy storage requirement in the magnetic field is less.		Magnetic field must store all energy transferred in each switching period
Magnetic gap	No, continuous amp-turn cancellation, therefore all require distributed air-gap material		
Energy Flow			
Energy drawn from supply	Only when switch is On		
Energy delivered to load	When switch is On and Off		When switch is Off
Ratings			
Primary switch peak voltage	Greater than V_{in}	Input voltage + referred load voltage	
Primary switch peak current	Peak current into load and output capacitor	Peak switch current is less than peak current into load and output capacitor	
Primary switch average current	The same		
RMS current of primary switch	Minimised by low peak current and high switch duty cycle		
Voltage of freewheel device	Just over V_{in}	Output voltage + referred primary voltage	
Current of freewheel device	Peak current into load and output capacitor		
Snubber circuit	Not necessarily required	Protection against leakage inductance over-voltage required	
Control			
Primary switch	Open-loop or closed-loop as voltage is limited even at no-load		Must be closed-loop
Secondary Switch (if synchronous rectification)	Complementary with dead-time	Complementary with leakage inductance providing some protection against shoot-through	
Losses			
Conduction loss	Average current × on-state voltage	Average current × higher on-state voltage due to higher voltage rating of device	
Switching loss	Peak current × V_{in}	Lower peak current × (V_{in} + referred V_{out}) Could be lower than buck if peak current is reduced sufficiently	
Performance and EMC			
Output voltage ripple	Lower for a given capacitance		Higher for a given capacitance
Input current ripple	High at low duty cycle	Potential for increased duty cycle allows lower input current filtering	

3.2 Equations of Buck Type Circuits

In this section circuit equations are used as the basis of comparison of the buck, coupled-inductor buck and flyback converters. Analysis of switch currents, output currents and relative duty cycles for a given step-down ratio are investigated. The circuits are analysed for continuous conduction mode (CCM) operation and the following definitions are used.

Table 3.2 Defined variables

Switch duty cycle	Duty cycle of main switch Q1 $t_{on}/(t_{on}+t_{off}) = t_{on}/T_s$; $T_s = t_{on}+t_{off}$	δ
Voltage transfer (function)	Output Voltage/Input Voltage TF	V_{out}/V_{in}
Voltage step-down ratio	Input Voltage/Output Voltage 1/TF, SDR	V_{in}/V_{out}
Coupled turns ratio	Primary Turns/Secondary Turns TR	N_1/N_2

3.2.1 Flyback Converter

When the main switch (Q1 in Fig. 3.1(c)) is on, the supply voltage V_{in} is applied across the inductance L_1. The current i_1 in L_1 increases from I_{1min} to I_{1max} (peak current) according to

$$V_{in} = \frac{L_1}{\delta T_s}\left(I_{1_{max}} - I_{1_{min}}\right) \tag{3.1}$$

where δ is the duty cycle of Q1 and T_s is the switching period. I_1 refers to the current in L_1 and I_2 refers to the current in L_2. V_{out} is given by:

$$V_{out} = \frac{L_2}{(1-\delta)T_s}\left(I_{2_{max}} - I_{2_{min}}\right) \tag{3.2}$$

Since the inductances of the primary and secondary windings are related by the squares of the number of turns, N_1 and N_2 then

$$L_2 = \left(\frac{N_2}{N_1}\right)^2 L_1. \tag{3.3}$$

At the switching instants, the ampere-turns balance is maintained, so that

$$N_1 I_1 = N_2 I_2. \tag{3.4}$$

Combining (3.1), (3.2), (3.3) and (3.4), and eliminating currents and T_s, gives the voltage transfer function of the flyback converter.

$$\frac{V_{out}}{V_{in}} = \frac{N_2}{N_1}\frac{\delta}{1-\delta}. \tag{3.5}$$

3.2.2 Coupled-Inductor Buck Converter

Similar analysis applies for the coupled-inductor buck converter. When Q1 is turned on, the inductance L_T of the circuit is the sum of inductances L_1 and L_2, plus $2\sqrt{L_1 L_2}$, which is proportional to $(N_1+N_2)^2$.

$$V_{in} - V_{out} = \frac{L_t}{\delta T_s}\left(I_{1_{max}} - I_{1_{min}}\right) \tag{3.6}$$

When Q1 is off, the circuit inductance is L_2, and V_{out} can be calculated from

$$V_{out} = \frac{L_2}{(1-\delta)T_s}\left(I_{2_{max}} - I_{2_{min}}\right). \tag{3.7}$$

L_2 can be expressed as

$$L_2 = \left(\frac{N_2}{N_1 + N_2}\right)^2 L_t. \tag{3.8}$$

At the switching instants $(N_1 + N_2)I_1 = N_2 I_2$, so the result from (3.8) into (3.7) yields

$$V_{out} = \frac{\left(\frac{N_2}{N_1 + N_2}\right)^2 L_t}{(1-\delta)T_s}\frac{N_1 + N_2}{N_2}\left(I_{1_{max}} - I_{1_{min}}\right). \tag{3.9}$$

(3.9) reduces to

$$V_{out} = \frac{\frac{N_2}{N_1 + N_2} L_t}{(1-\delta)T_s}\left(I_{1_{max}} - I_{1_{min}}\right) \tag{3.10}$$

Combining (3.6) and (3.10), and eliminating the currents and period T_s yields

$$\frac{V_{out}}{V_{in}} = \frac{\delta N_2}{N_1 + N_2 - \delta N_1} \tag{3.11}$$

Comparing (3.5) and (3.11), the coupled-inductor buck converter has a lower output voltage than the flyback circuit for a given switch duty cycle and given turns ratio.

3.2.3 Comparison of Voltage Transfer Ratios Against Main Switch Duty Cycle

Using the equations in Section 3.2, the three circuits can be compared for different turns ratios. Fig. 3.2 shows the voltage transfer ratios of the buck, coupled-inductor buck and the flyback circuits versus switch duty cycle. The voltage transfer ratio of the buck converter increases linearly from 0 to 1 as the switch duty cycle increases from 0 to 1. The voltage transfer ratios of the coupled-inductor buck and flyback converters are non-linear. In Fig. 3.2, with turns ratio of 1:1 the coupled-inductor buck circuit delivers a lower output voltage at all switch duty cycles but the flyback circuit delivers a higher output voltage than the buck converter at all switch duty cycles. With a turns ratio of 3:1, the coupled-inductor buck converter delivers a significantly lower output voltage at all duty cycles and the flyback circuit delivers a lower output voltage than the buck converter up to 65% switch duty cycle. The voltage transfer ratios of the coupled-inductor buck and flyback converters both follow a similar trajectory, significantly lower than that of the buck converter. The voltage transfer ratio of the flyback converter is always greater than unity at high switch duty cycles.

In Fig. 3.2 the coupled-inductor buck converter offers a lower output voltage and a greater voltage step-down ratio while maintaining a higher switch duty cycle. At a given voltage step-down ratio, the on-time of the switch in the coupled-inductor buck converter will be a higher percentage of the switching period.

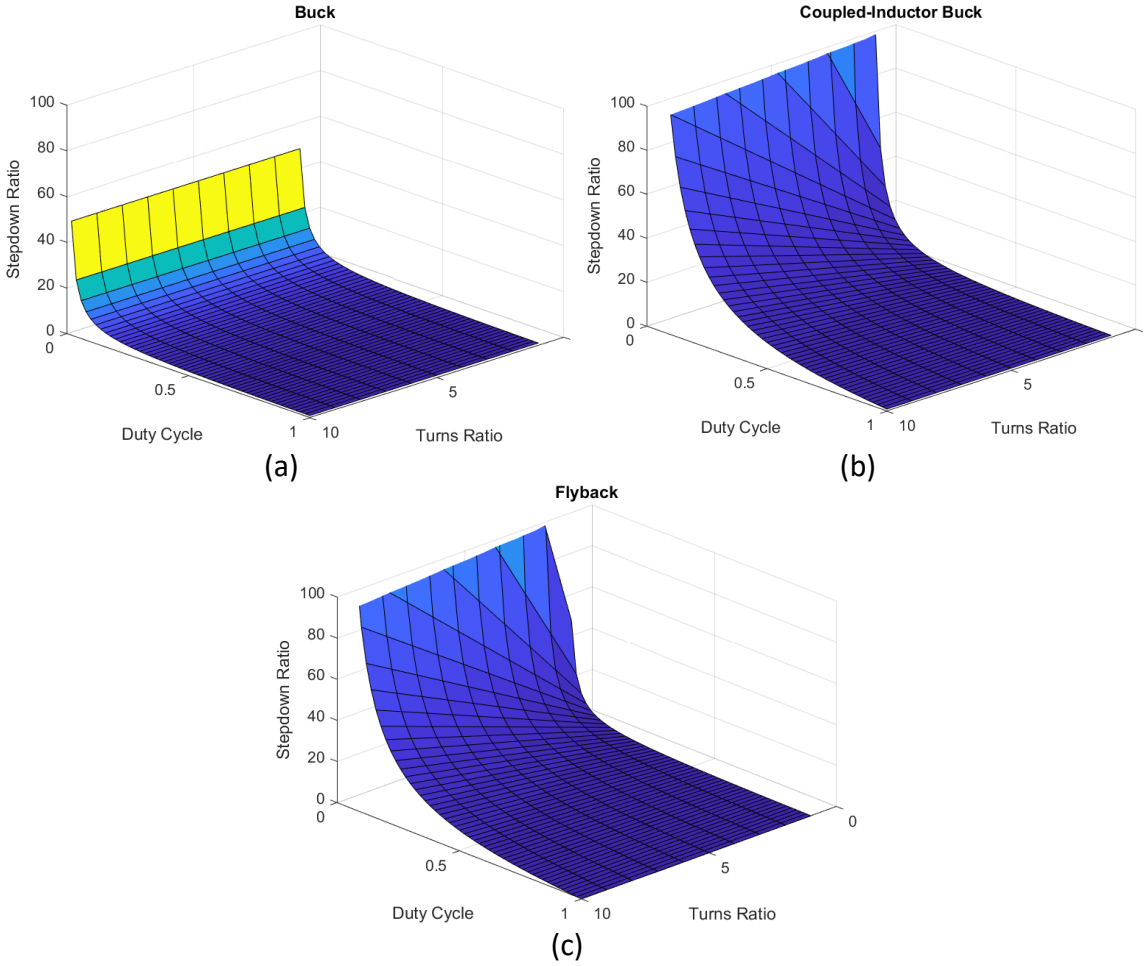


Fig. 3.2 Voltage transfer ratio versus turns ratio, (a) buck, (b) coupled-inductor buck and (c) flyback.

In all three topologies the supply voltage is V_{in}. For a given power input, the average current in Q1 will therefore be the same, thus the difference in switch ratings will be dependent on the switching voltage and the peak switched current. Sections 3.2.4 to 3.2.6 develop mathematical expressions for each converter which enable comparison of the peak currents as a function of step down ratio. A circuit offering a higher switch duty cycle will have a lower peak current. However, both the coupled-inductor circuit of Fig. 3.1(b) and the flyback circuit of Fig. 3.1(c) require switch voltage ratings which must support the referred output voltage in addition to the input voltage during the primary switch off-time. The performance of the three circuits and their component rating requirements can be compared based on the peak current in the switch at the point of switch turn off.

3.2.4 **Peak Current in the Buck Converter**

The average load current is given by (without two windings, effectively I_1=I_2):

$$I_{load_{b\_av}} = \frac{I_{1_{b\_max}} + I_{1_{b\_min}}}{2} \tag{3.12}$$

$$I_{1_{b\_max}} + I_{1_{b\_min}} = 2\, I_{load_{b\_av}} \tag{3.13}$$

The peak current ($I_{1_{b\_max}}$) can also be calculated from the ripple current by considering the duty cycle δ_b and inductance L_T:

$$I_{1_{b\_max}} - I_{1_{b\_min}} = \frac{\delta_b V_{in} T_s}{L_T} \tag{3.14}$$

Adding (3.13) and (3.14) cancels the minimum currents giving:

$$I_{1_{b\_max}} = I_{load_{b\_av}} + \tfrac{1}{2}\frac{\delta_b V_{in} T_s}{L_T} \tag{3.15}$$

In the buck circuit, L_T can be calculated according to its physical parameters:

$$L_T = (N_1 + N_2)^2 \frac{\mu_0\, \mu_r A}{l} \tag{3.16}$$

Substituting (3.16) into (3.15) gives (3.17) where k_L is a constant as defined in (3.18).

$$I_{1_{b\_max}} = I_{load_{b\_av}} + \frac{\delta_b}{k_L\,(N_1 + N_2)^2} \tag{3.17}$$

$$k_L = \frac{2}{V_{in} T_s} \frac{\mu_0\, \mu_r A}{l} \tag{3.18}$$

Representing step down ratio in terms of duty cycle as shown in (3.19), (3.17) can now be expressed as (3.20), which defines the peak current in the buck converter in terms of voltage step down ratio.

$$\text{Step down ratio (SDR)} = \frac{V_{in}}{V_{out}} = \frac{1}{\delta_b} \tag{3.19}$$

$$I_{1_{b\_max}} = I_{load_{b\_av}} + \frac{1}{k_L\,(N_1 + N_2)^2 SDR} \tag{3.20}$$

3.2.5 Peak Current in the Coupled-Inductor Buck Converter

$$I_{load_{ci_{av}}} = (1-\delta_{ci})\frac{\frac{N_1+N_2}{N_2}}{N_2}\frac{I_{1_{ci\_max}}+I_{1_{ci\_min}}}{2} + \delta_{ci}\frac{I_{1_{ci\_max}}+I_{1_{ci\_min}}}{2} \quad (3.21)$$

where δ_{ci} is the duty cycle in the coupled-inductor circuit.

$$I_{load_{ci\_av}} = \frac{(1-\delta_{ci})N_1+N_2}{N_2}\frac{I_{1_{ci\_max}}+I_{1_{ci\_min}}}{2} \quad (3.22)$$

(3.22) can be rearranged to give:

$$I_{1_{ci\_max}} + I_{1_{ci\_min}} = \frac{2\,N_2\,I_{load_{ci\_av}}}{(1-\delta_{ci})N_1+N_2} \quad (3.23)$$

The ripple current is given by

$$I_{1_{ci\_max}} - I_{1_{ci\_min}} = \frac{\delta_{ci}V_{in}T_s}{L_T} \quad (3.24)$$

Adding (3.23) and (3.24) gives

$$I_{1_{ci\_max}} = \frac{N_2\,I_{load_{ci\_av}}}{(1-\delta_{ci})N_1+N_2} + ½\,\frac{\delta_{ci}V_{in}T_s}{L_T} \quad (3.25)$$

In the coupled-inductor buck converter, L_T is the inductance presented by the series primary and secondary turns:

$$L_T = (N_1+N_2)^2\frac{\mu_0\,\mu_r A}{l} \quad (3.26)$$

Substituting (3.26) into the second term of (3.25) in gives (3.26)

$$I_{1_{ci\_max}} = \frac{N_2\,I_{load_{ci\_av}}}{(1-\delta_{ci})N_1+N_2} + \frac{\delta_{ci}}{k_L\,(N_1+N_2)^2} \quad (3.27)$$

The coupled-inductor buck converter step-down ratio is the inverse of the voltage gain calculated in (3.11):

$$\text{Step down ratio (SDR)} = \frac{V_{in}}{V_{out}} = \frac{N_1+N_2-\delta_{ci}N_1}{\delta_{ci}N_2} \quad (3.28)$$

Rearranging (3.28) gives:

$$\delta_{ci} = \frac{N_1 + N_2}{N_2 SDR + N_1} \tag{3.29}$$

Substituting into (3.27) to eliminate δ_{ci}:

$$I_{1_{ci\_max}} = I_{load_{ci\_av}} \frac{N_2}{\left(1 - \frac{N_1 + N_2}{N_1 + N_2 SDR}\right) N_1 + N_2} + \frac{1}{k_L (N_1 + N_2 SDR)(N_1 + N_2)} \tag{3.30}$$

3.2.6 Peak Current in the Flyback Converter

The average load current of the flyback converter (referred to the input side) is given as

$$I_{load_{fb\_av}} = \left(1 - \delta_{fb}\right) \frac{N_1}{N_2} \frac{I_{1_{fb\_max}} + I_{1_{fb\_min}}}{2} \tag{3.31}$$

where δ_{fb} is the switch duty cycle. Rearranging (3.31) gives

$$I_{1_{fb\_max}} + I_{1_{fb\_min}} = \frac{2\, I_{load_{fb\_av}}}{\left(1 - \delta_{fb}\right)} \frac{N_2}{N_1} \tag{3.32}$$

The inductor ripple current during the switch on-time is:

$$I_{1_{fb\_max}} - I_{1_{fb\_min}} = \frac{\delta_{fb} V_{in} T_s}{L_1} \tag{3.33}$$

Adding (3.32) and (3.33) eliminates the minimum current

$$I_{1_{fb\_max}} = \frac{I_{load_{fb\_av}}}{\left(1 - \delta_{fb}\right)} \frac{N_2}{N_1} + \frac{\delta_{fb} V_{in} T_s}{2\, L_1} \tag{3.34}$$

When Q1 is on in the flyback converter, the inductance of primary is L_1.

$$L_1 = {N_1}^2 \frac{\mu_0\, \mu_r A}{l} \tag{3.35}$$

Replacing L_1 in (3.34) with (3.35) gives (3.36) where k_L is (3.18), which is common to each circuit:

$$I_{1_{fb\_max}} = \frac{I_{load_{fb\_av}}}{\left(1 - \delta_{fb}\right)} \frac{N_2}{N_1} + \frac{\delta_{fb}}{k_L\, {N_1}^2} \tag{3.36}$$

The flyback converter voltage step down ratio *SDR* is the inverse of the voltage gain given by (3.5):

$$\text{Voltage Step down Ratio (SDR)} = \frac{V_{in}}{V_{out}} = \frac{N_1}{N_2}\frac{1-\delta_{fb}}{\delta_{fb}} \tag{3.37}$$

Rearranging (3.37) gives:

$$\delta_{fb} = \frac{N_1}{N_1 + N_2 SDR} \tag{3.38}$$

The result from (3.38) is substituted into (3.36) to eliminate δ_{fb}:

$$I_{1_{fb\_max}} = I_{load_{fb\_av}} \frac{N_2}{\left(1 - \frac{N_1}{N_1 + N_2 SDR}\right) N_1} + \frac{1}{k_L\,(N_1 + N_2 SDR) N_1} \tag{3.39}$$

3.3 Benefit of Higher Duty Cycle Operation

Equations (3.20), (3.30) and (3.39) can be used to plot the peak primary currents for each converter as a function of step down ratio. For each converter constant k_L (with the experimental values from Chapter 4 & 5) is defined according to:

$$k_L = \frac{2}{V_{in} T_s}\frac{\mu_0\,\mu_r A}{l} = \frac{2}{150 \times 25\mu s}\frac{4\pi \times 10^{-7} \times 300 \times \pi \times (12.5 \times 10^{-3})^2}{\pi \times 150 \times 10^{-3}} \tag{3.40}$$

Average load current $I_{load_{fb\_av}} = I_{load_{ci\_av}} = I_{load_{b\_av}}$ is 100A and the turns ratios examined are range from 3:3 - 30:3, with N_1 varied and N_2=3.

The plots in Fig. 3.3 show the variation in the peak switch current with step down ratio (SDR) and number of primary turns. The plots for the buck converter, coupled inductor buck and flyback show peak switch currents with 100A of average load current and fixed three turns in the secondary winding. In the buck converter in Fig. 3.3(a) the peak switch current is always more than 100A independent of the step down ratio. The highest switch current occurs when the circuit inductance has the fewest turns and when the step down ratio is small. In contrast the peak switch current in the coupled inductor buck (Fig. 3.3(b)) is under 100A except for the lowest step down ratio and low number of primary turns. Fig. 3.3(c) shows that the peak switch current in a flyback is significantly lower than the buck but not as low as the coupled buck converter. At higher step down ratios

and higher primary turns, the flyback and coupled-inductor buck converge to similar low values for primary switch currents.

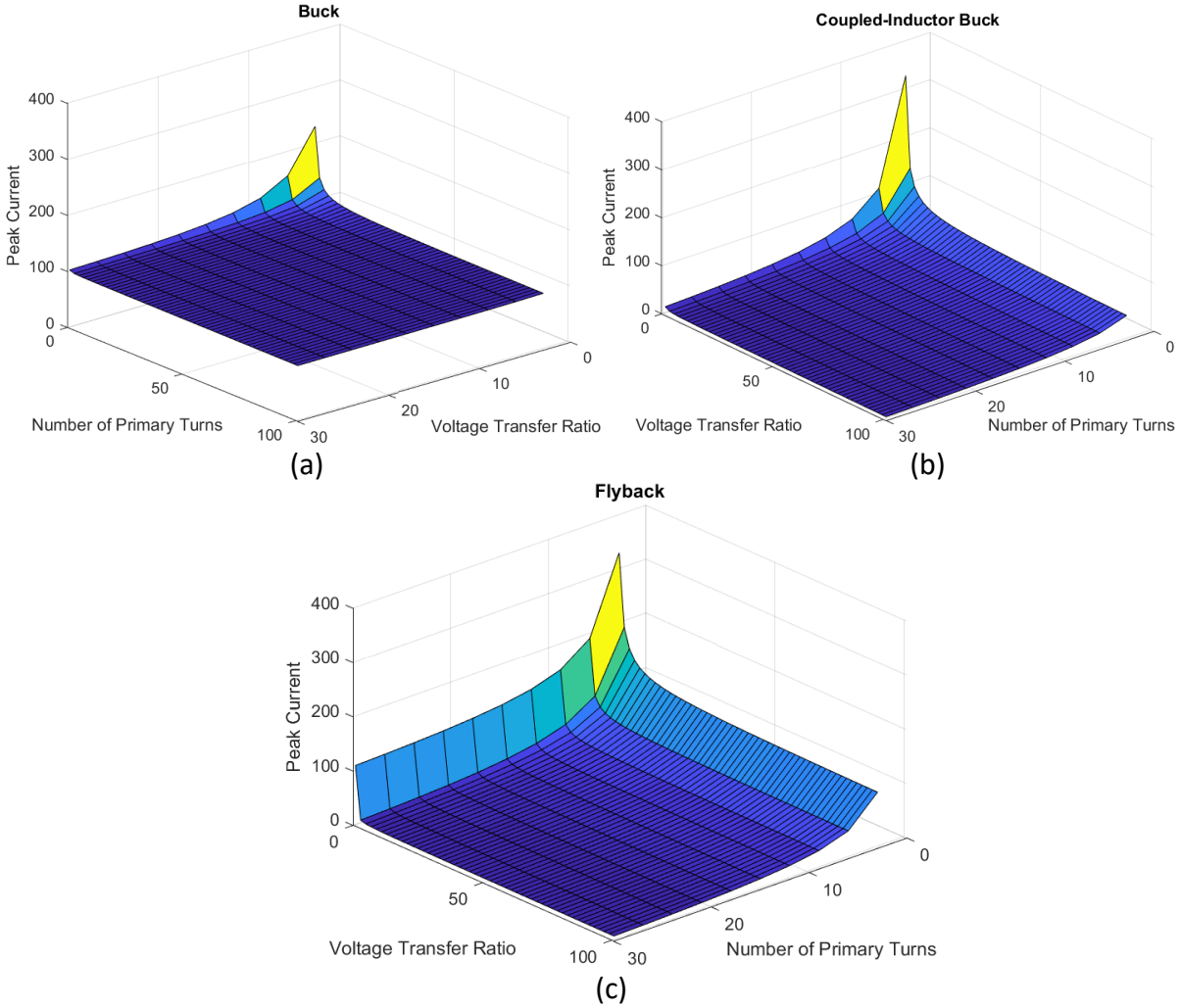


Fig. 3.3 Maximum switch current for 100A load current versus voltage step-down ratio for each circuit against an increasing No. Primary Turns and (Fixed secondary turns = 3) (a) Buck converter (total turns = No. Primary Turns + 3) (b) Coupled-inductor buck converter (c) Flyback converter

3.3.1 Switch and Diode Voltage Ratings

Additionally, the ratings on the devices

The switch and diode voltage ratings for each of the three circuits are given below:

Buck converter switch rating:

$$V_{off} = V_{in} \tag{3.41}$$

Flyback converter switch rating:

$$V_{off} = V_{in} + \frac{N1}{N2} V_{out} \tag{3.42}$$

Coupled-Inductor Buck converter switch rating:

$$V_{off} = V_{in} + \frac{N1}{N2} V_{out} \tag{3.43}$$

Buck converter diode rating:

$$V_{off} = V_{in} \tag{3.44}$$

Flyback converter diode rating:

$$V_{off} = V_{out} + \frac{N2}{N1} V_{in} \tag{3.45}$$

Coupled-Inductor Buck converter diode rating:

$$V_{off} = V_{in} - \left(\frac{N1}{N2 + N1}\right)(V_{in} - V_{out}) \tag{3.46}$$

The coupled-inductor buck converter and the flyback converter have the same main switch rating which is larger than that of the buck converter. The diode ratings however differ significantly; the significance of the diode rating difference arises when the converter operates bidirectionally as the diode will be the location of the main switch for reverse operation.

Table 3.3 compares the normalized losses for the buck and coupled buck converters over a range of voltage step-down ratios and coupled turns-ratios of 3:1 and 10:1.

Table 3.3: Estimated switching losses in the coupled buck converter as a percentage of buck converter switching losses, as shown in Fig. 3.2 & Fig. 3.3.

	Buck Converter				*Coupled-Inductor buck converter, Turns 3:1*					*Coupled-Inductor buck converter Turns 10:1*				
SDR	δ	I_{max_Q1}	V_{Q1}	P_{sw_b}	δ	I_{max_Q1}	V_{Q1}	P_{sw_ci}	$\frac{P_{sw\_ci}}{P_{sw\_b}}$%	δ	I_{max_Q1}	V_{Q1}	P_{sw_ci}	$\frac{P_{sw\_ci}}{P_{sw\_b}}$%
5:1	0.2	1.08	1	1.08	0.5	0.4	1.6	0.64	59 %	0.73	0.06	3.0	0.18	16.7 %
10:1	0.1	1.05	1	1.05	0.32	0.33	1.3	0.43	41 %	0.55	0.05	2.0	0.1	10 %
20:1	0.05	1.02	1	1.02	0.2	0.24	1.15	0.28	27 %	0.3	0.05	1.5	0.075	7 %

From the plots in Fig. 3.3, the peak currents in the coupled-inductor buck and flyback converters tend to converge at higher turns ratios (and SDR). The buck converter can be seen to have far higher peak currents at larger step-down ratios but further investigation is required to distinguish between the two magnetically coupled converters at these step down ratios. The two circuits were therefore simulated and constructed to examine the extent to which they differ.

3.4 Magnetic Component Considerations

This section compares the magnetic component requirement for two converters.

3.4.1 Magnetic Core Comparison

Equation (3.30) defines the peak primary (switch) current in the coupled-inductor buck converter.

$$I_{1_{ci\_max}} = \frac{N_2\, I_{load_{ci\_av}}}{\left(1 - \frac{N_1 + N_2}{N_2 SDR + N_1}\right) N_1 + N_2} + \frac{1}{(N_2 SDR + N_1) k_L (N_1 + N_2)} \qquad (3.47)$$

In the coupled-inductor buck converter the peak switch current flows simultaneously in N_1+N_2 turns so that the peak MMF within the magnetic core is $(N_1 + N_2) \times I_{1_{ci\_max}}$. The MMF in the coupled inductor core is therefore given by

$$MMF_{ci} = \frac{N_2\, I_{load_{ci\_av}}}{1 - \frac{N_1}{N_2 SDR + N_1}} + \frac{1}{k_L(N_1 + N_2 SDR)}. \quad (3.48)$$

Repeating the same process for the flyback converter results in a peak current given by (3.49).

$$I_{1_{fb\_max}} = \frac{N_2\, I_{load_{fb\_av}}}{\left(1 - \frac{N_1}{N_2 SDR + N_1}\right) N_1} + \frac{1}{k_L\,(N_1 + N_2 SDR) N_1} \quad (3.49)$$

At the instant of switch turn off in the flyback converter the peak current flows through only the primary (L_1). The MMF within the magnetic core is $N_1 \times I_{1_{fb\_max}}$ and is given by (3.50).

$$MMF_{fb} = \frac{N_2\, I_{load_{fb\_av}}}{1 - \frac{N_1}{N_2 SDR + N_1}} + \frac{1}{k_L\,(N_1 + N_2 SDR)} \quad (3.50)$$

Equations (3.48) and (3.50) are identical showing that the magnetic component is not a key design factor that distinguishes between the two circuits.

3.4.2 Leakage Inductance Considerations

The leakage inductance, which generally increases with larger turns ratio, can cause undesirable over-voltages across the switches. If these over-voltages are detrimental to circuit operation they may be controlled, at the expense of the inclusion of additional components, for example, by employing two-switch variants of the converters, as in Chapter 5 & 6. These 'asymmetrical-half bridge' two-switch variants achieve switch protection by clamping the maximum voltage across each switch to the supply rail.

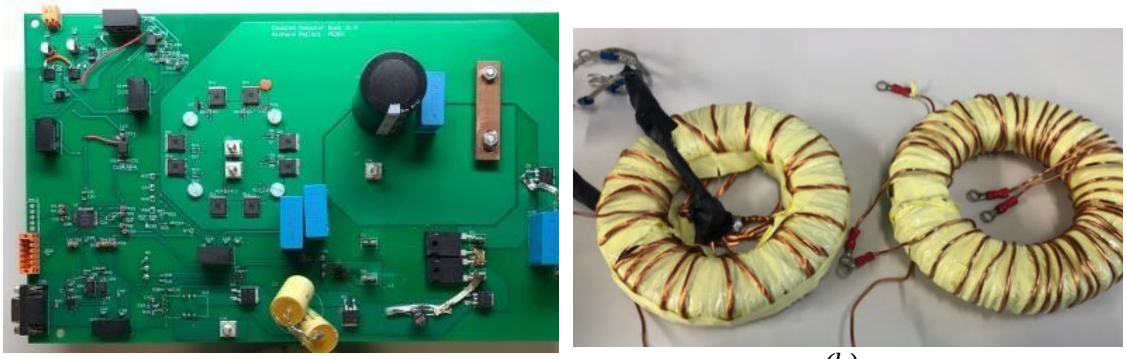
3.5 Simulation supported Experimental Comparison of the Flyback and Coupled-Inductor Buck Converters

The analysis in Section 3.2 highlighted the benefit of the coupled-inductor circuit over a range of primary to secondary turns ratios. The analysis also shows that the coupled-inductor buck converter always has a lower peak current than the flyback circuit. The

circuits also differ in their ratio of primary side current to output current. Having a higher output current for a given primary current allows for a lower rated switch (Q1) to be used for a specific load. In order to confirm the lower switch rating for a given output current, the circuits were realised, using components specified in Table 3.4, to enable experimental comparison of their operation. The experimental circuits were also compared with PSpice time-domain simulations in order to validate the simulation model and to confirm that it accurately predicts the performance of the two circuits. Having confidence in the model enables it to be used in the design of higher power implementations and investigation of closed-loop controller design and behaviour under dynamic conditions. Results shown in Section 3.2 show that the performance of the two selected circuits tends to converge at a voltage step-down ratio in the region of 50:1. The aim of the following study therefore is to achieve a voltage step down ratio in excess of 50:1, whilst delivering current into a load resistance of a few milli-ohms from a 30V supply voltage.

Table 3.4 Experimental component values.

Component	Part number/Value
Primary Side Switch Q1	Infineon MOSFET IGW15N120H3
Synchronous Rectifier on Load Side	Parallel connected Infineon OptiMOS IPB100N
Output Capacitance	6800 µF
Load Resistance	Copper bar, resistance 4 mΩ
Transformer 1 wound on T520-52 iron powder Core	Primary inductance = 490 µH Secondary inductance = 70 µH Inductance ratio, L_1:L_2 = 7:1 Turns ratio, N_1:N_2 = 2.65:1 Coupling coefficient = 0.975
Transformer 2 wound on T520-52 iron powder Core	Primary inductance = 490 µH Secondary inductance = 4.7 µH Inductance ratio, L_1:L_2 = 104:1 Turns ratio, N_1:N_2 =10.2:1 Coupling coefficient = 0.958
Primary Side Snubber	An energy recovery voltage clamp snubber (see Chapter 4 & 5) protects the primary side switch and returns the leakage energy to the input supply.



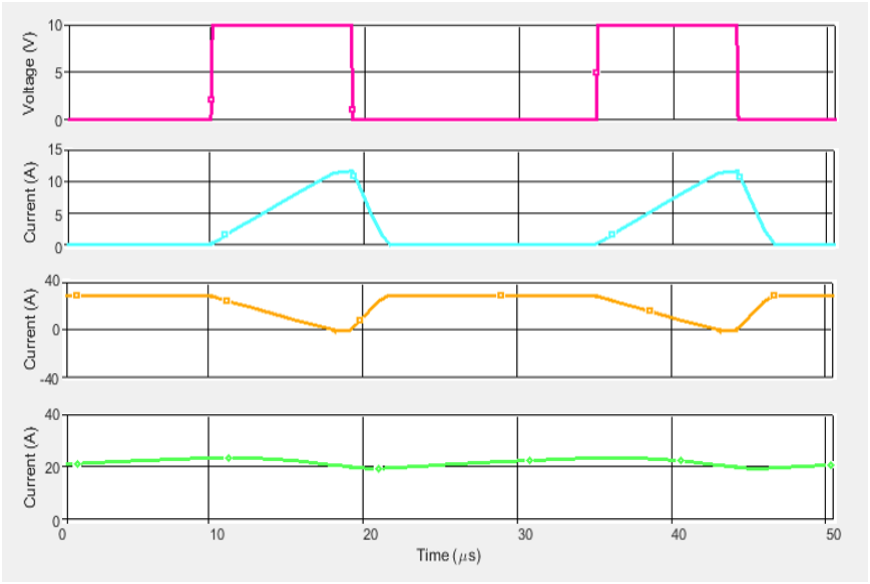
(a) *(b)*

Fig. 3.4 (a) Experimental circuit for testing flyback and coupled-inductor converters and (b) wound coupled inductors N_1:N_2=2.65:1 and 10.2:1 used for both circuits.

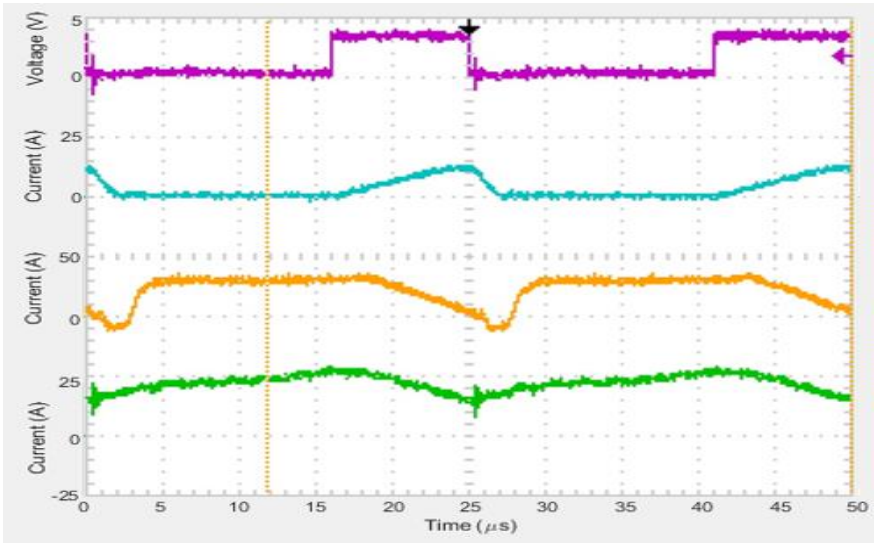
The aim was to use the two transformer turns ratios within the range specified in Section 3.2. The practical inductors resulted in turns ratios of 2.65:1 and 10.2:1, and these are considered to be suitably close to the target values to provide meaningful experimental results. These practical turns ratios were used in the PSpice simulation to ensure meaningful comparison.

3.5.1 Experimental and Simulated Waveforms

The experimental and PSpice simulated waveforms for the flyback and coupled-inductor buck converters using the 2.65:1 transformer and 'continuous conduction' are shown in Fig. 3.5 and Fig. 3.6, while Fig. 3.7 and Fig. 3.8 show the corresponding results when the second transformer with a 10.2:1 turns ratio, is used. The figures demonstrate the agreement between the simulated and practical results, verifying the accuracy of the PSpice model. The results also highlight that the main difference between the two circuits being the secondary current which is discontinuous in the flyback converter but continuous in the coupled-inductor converter. The continuity of the secondary current in the coupled-inductor buck converter is more apparent in Fig. 4.8 as a lower turns ratio is used. Having a continuous secondary current means that for a given output voltage the same power throughput can be achieved with a lower peak output current. This enables reduced output switch and capacitor ratings, and reduced peak and average input currents. Consequently, the coupled-inductor buck converter offers improved efficiency resulting from the use of lower rated (viz. lower $R_{DS(on)}$) devices. This efficiency advantage over the flyback converter diminishes at higher turns ratios. For larger turns ratios the ratio of the output current to the input current is also increased, that is, the turns ratio and current ratio are proportional for the same duty cycle. As the turns ratio is increased, switch Q1 on-time current, which also flows in the secondary, is a smaller proportion of switch Q1 off-time current in the secondary. For increasing turns ratio this proportion approaches zero resulting in discontinuous secondary (output) current, which is a characteristic of the flyback converter and which reinforces the similarity between the two circuits at high turns ratio.

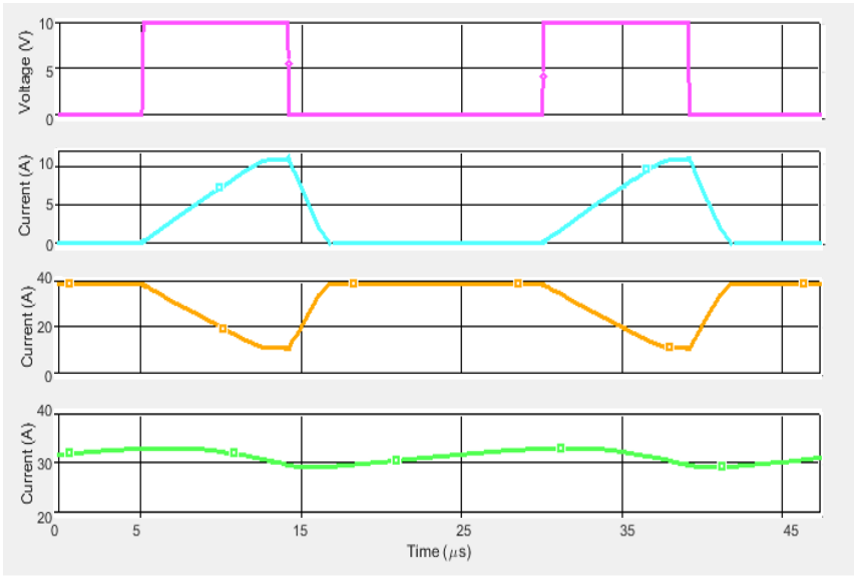


(i)

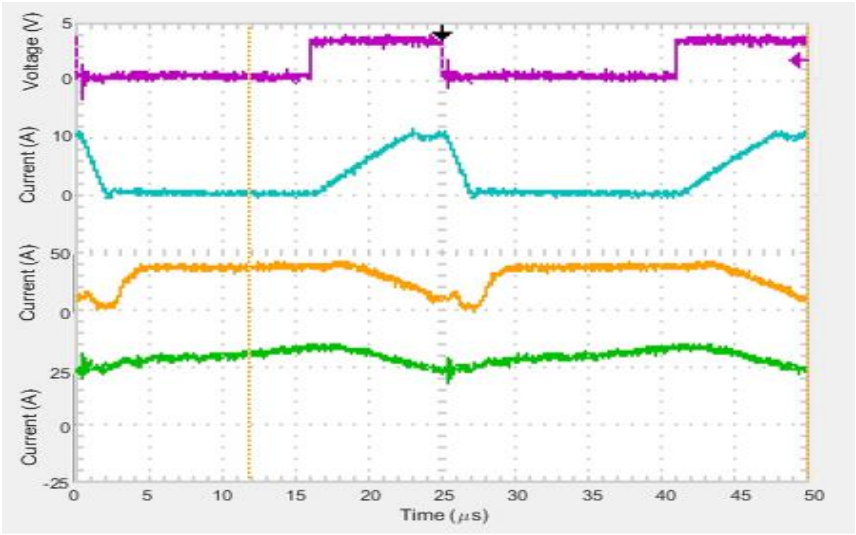


(ii)

Fig. 3.5 Flyback circuit waveforms with 2.65:1 turns ratio at a 36% duty cycle: (i) simulated and (ii) experimental. (a) Q1 Gate Signal (Vgs), (b) Primary (L1) inductor current, (c) Secondary (L2) inductor current, (d) Load Voltage R1

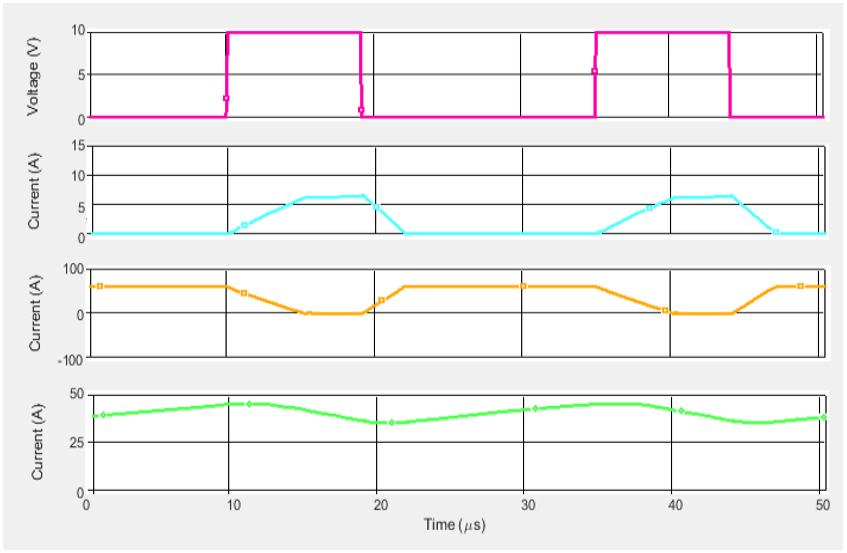


(i)



(ii)

Fig. 3.6 Coupled-inductor buck converter waveforms with a 2.65:1 turns ratio at a 36% duty cycle: (i) simulated and (ii) experimental. (a) Q1 Gate Signal (Vgs), (b) Primary (L1) inductor current, (c) Secondary (L2) inductor current, (d) Load Voltage R1



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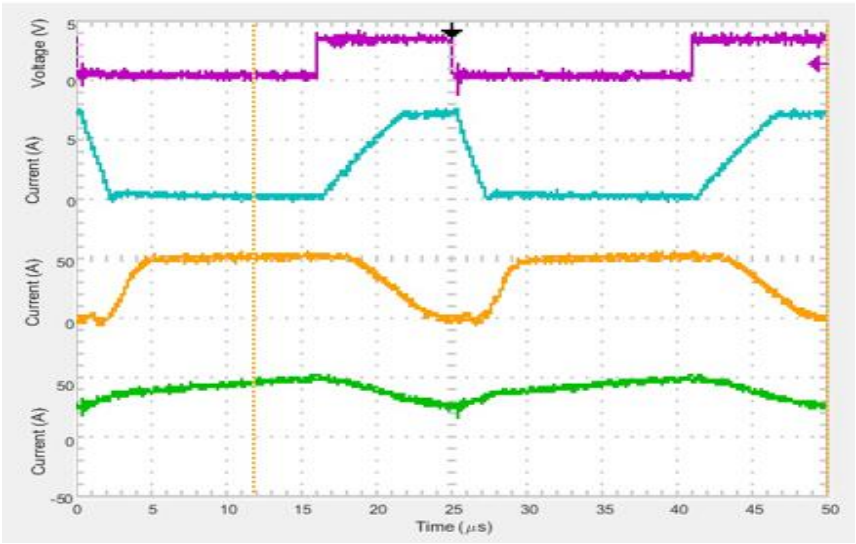
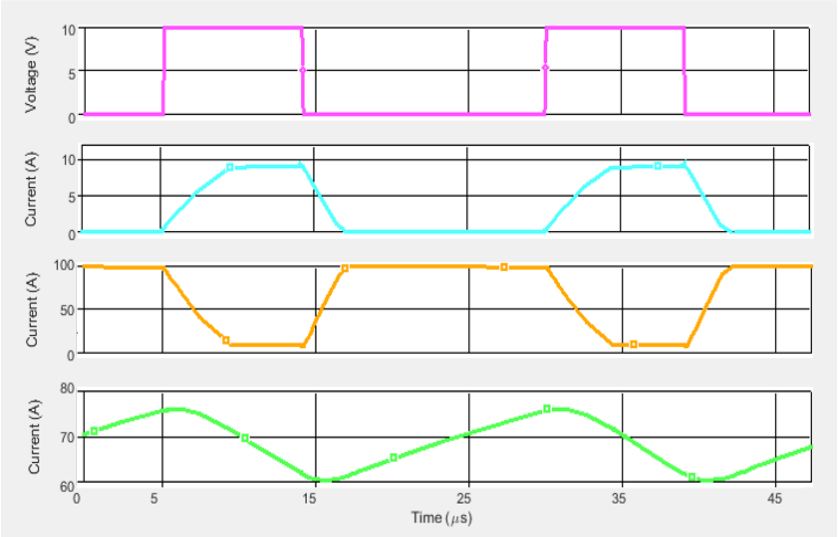


(ii)

Fig. 3.7 Flyback circuit waveforms with 10.2:1 turns ratio at a 36% duty cycle: (i) simulated and (ii) experimental. (a) Q1 Gate Signal (Vgs), (b) Primary (L1) inductor current, (c) Secondary (L2) inductor current, (d) Load Voltage R1



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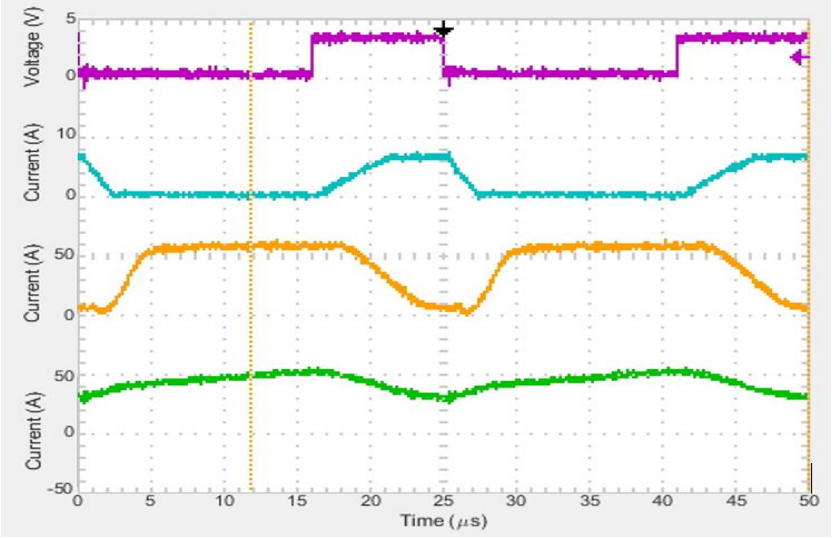


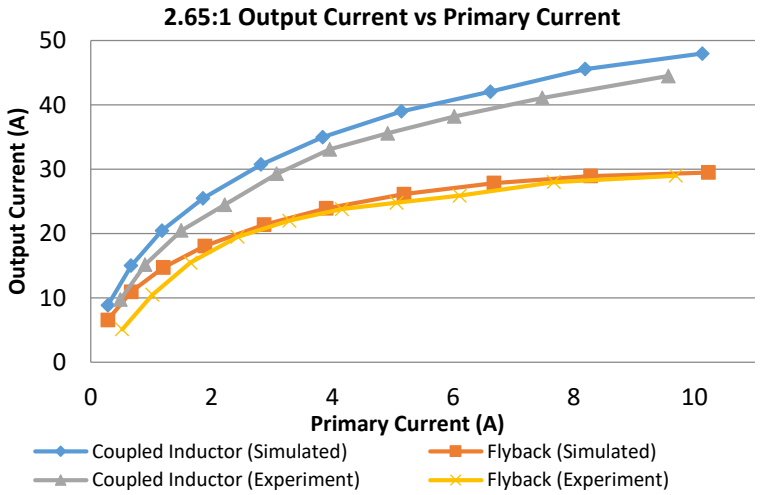
(ii)

Fig. 3.8 Coupled-inductor converter waveforms with a 10.2:1 turns ratio at a 36% duty cycle: (i) simulated and (ii) experimental. (a) Q1 Gate Signal (Vgs), (b)Primary (L1) inductor current, (c) Secondary (L2) inductor current, (d) Load Voltage R1

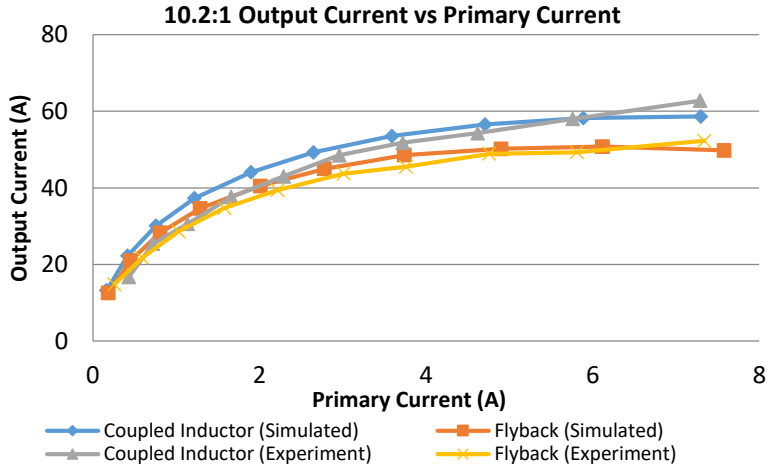
3.5.2 Comparison of Flyback and Coupled-Inductor Buck Converters

Fig. 3.9 shows the simulated and experimental current values for the two converters over a range of duty cycles. The figures show that there is agreement between the experimental and PSpice simulation results. The figures confirm that the coupled-inductor circuit has a lower average primary current and thus a lower current rating for a given output current

when compared to the flyback converter. The transformer copper losses and the primary switch conduction losses will therefore be lower for the coupled-inductor buck converter, as identified in the mathematical analysis of Section 3.2. This saving is significant at lower turns ratios and diminishes as the turns ratio increases.



(a)

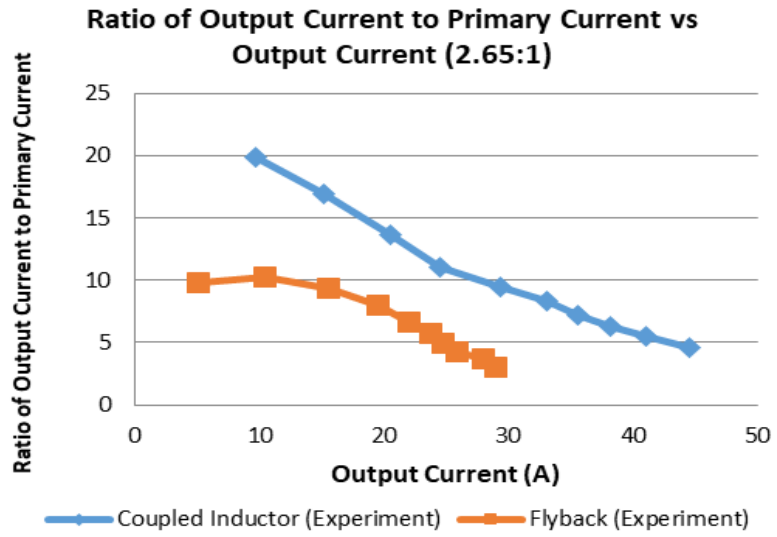


(b)

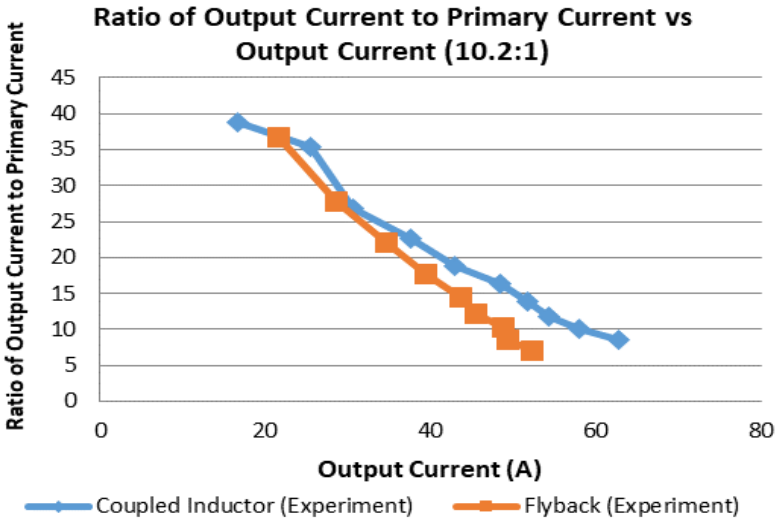
Fig. 3.9 Output current versus average primary current by varying duty cycle, turns ratio of: (a) 2.65:1 and (b) 10.2:1.

The experimental results in Fig. 3.9 show the coupled-inductor converter has a higher current gain for a given output current and will therefore have a lower average primary

side (switch) current. Thus, if using a 3:1 turns ratio, a lower rated switch could be used in the coupled-inductor buck converter than in the flyback converter.



(a)



(b)

Fig. 3.10 Ratio of output current to primary current plotted against output current by varying duty cycle, for a turns ratio of: (a) 2.65:1 and (b) 10.2:1.

The results confirm that the coupled-inductor buck converter has lower primary current for a given output current, and therefore lower switch and inductor losses, when compared to the flyback converter. The coupled-inductor buck converter has the potential to be a lower cost alternative to the flyback converter in applications where isolation is not required.

3.6 Summary

The buck converter conventionally is used with step-down ratios up to 10:1. This investigation highlights the advantage of utilising a coupled-inductor buck converter for all step-down ratios since it offers lower peak primary switch current than the buck converter. This is however at the expense of increased magnetic component complexity (tap, creating three terminals).

The flyback converter outperforms the buck converter in terms of peak switch current only when the wound magnetic component turns ratio becomes large. The additional complexity of the magnetic component in the flyback converter, which exceeds that of the magnetic component coupled-inductor buck converter, may be justified if isolation is required.

As the step-down ratio is increased, the coupled-inductor buck converter continues to outperform both the buck and flyback converters. As the step-down ratio is further increased the primary switch current requirements of the coupled-inductor and flyback converters converge. The coupled-inductor buck converter still offers the best performance and lowest cost but the advantage of isolation offered by the flyback converter may be traded for its marginally reduced performance.

The coupled-inductor buck converter offers an alternative to the buck converter in applications where switching losses need to be minimised which is particularly beneficial at large step-down ratios where the losses can be reduced by more than 50% compared to the buck converter.

At large turns ratios it is desirable to minimise leakage inductance to ensure reliable operation. Snubber circuits provide a solution to switch over-voltage resulting from this leakage inductance at low power levels whilst ‘asymmetrical-half bridge’ or two-switch

variants may be required in high power applications. Chapter 4 will investigate possible active recovery snubber circuits for use with the coupled-inductor buck converter to protect the main switch from over-voltage.

Chapter 4 Active Switch Protection Circuits for Large Step-Down Voltage Coupled-Inductor Converters

Chapter 3 highlighted the problems created by the leakage energy in the coupled-inductor buck (and flyback) converter. This chapter presents active switch protection circuits which can absorb, and in some cases recover, the energy associated with the leakage inductance and therefore protect the switching devices against over-voltages. Active switch protection involves the addition of one or more semiconductor switches to control or reduce the over-voltage seen on the switch needing protection. An active switch protection circuit can have an increased efficiency over a passive variant and can offer greater control. However, it is often more expensive and complex.

Firstly, a regenerative flyback snubber is presented, analysed, simulated and experimental results presented. Secondly, the buck-boost clamp snubber is analysed, simulated, and experimentally assessed.

4.1 Novel Fly-forward Regenerative Snubber

The proposed regenerative snubber, Fig. 5.1, offers a way for an active switch to recirculate the energy back to the input supply.

Q1 turn-on Whilst the main switch Q1 is on, Q3 is also on to reset the snubber, as both are controlled by the same gating signal. As shown in Fig 5.2(a), snubber capacitor C2 resonantly discharges through transformer T1 primary (dashed, orange) during ‘on’ period of switches Q1 and Q3. Resonant current flows in the primary of T1 provided the reflect input voltage V_{in} n1/n2 is exceed by the voltage on C2. Current flows in the secondary of T1, n2 and through D4, recovering energy in C2 back into the input source Vin (sparse dotted, green).

Q1 turn-off When Q1 switches off, turn-off snubber capacitor C2 charges, clamping the switch Q1, voltage. C2 functions as a turn-off snubber capacitor [46], storing the main circuit leakage energy.

The energy recovery circuit is adaptive: when the load current increases (and leakage energy increases), snubber action occurs at a lower voltage level, giving better switch protection whilst recovering snubber energy. This adaptation is achieved by fixing the turns ratio of T1 so that the reflected circuit voltage across n1 of T1 is greater than half the dc-link voltage. Under light load, the snubber capacitor cannot fully discharge. As the load current increases there is more leakage energy (which is proportional to the current squared) in the coupled inductor Lt, the bypass diode D2 conducts, clamping the snubber capacitor voltage to zero, thereby allowing the voltage transients to be suppressed.

Since Q1 and Q3 utilise the same drive signal, a simple control structure results. The leakage inductance associated with the recovery transformer T1 may be sufficient for the desired resonance properties, to avoid the need for added discrete inductance (L3) in series with D3.

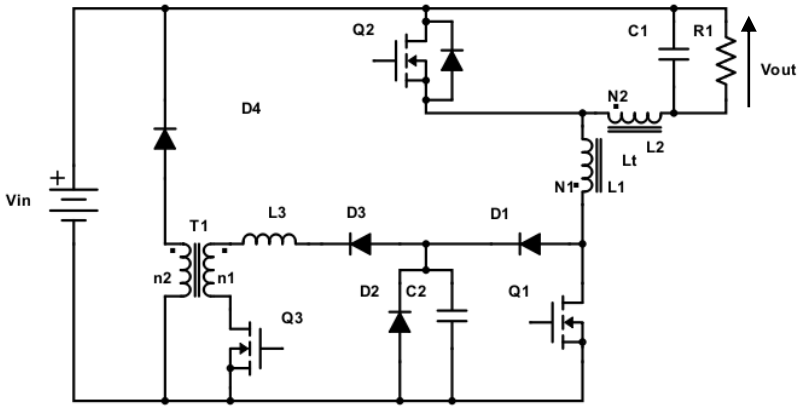
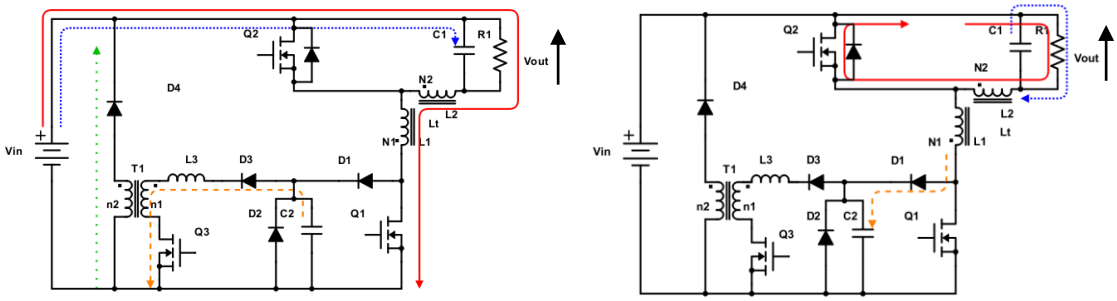


Fig. 4.1. Novel regenerative flyforward snubber.



(a) (b)

Fig. 4.2 (a)Mode 1 - energising coupled inductor Lt, (b) Q1 turned off discharging Lt.

4.1.1 Regenerative snubber Simulation

Fig. 4.3 shows simulation results for an output current of 350A at 1V, derived from a 300V DC supply. In Fig. 4.3, the voltage across the main switch Q1 is limited to a peak of approximately 1kV by the fly-forward snubber C2, allowing a 1.7kV rated device to be used. The voltage across the snubber capacitor C2 is reset by Q3, and energy is recovered back into the DC supply. The interchange of current in the primary (L1) and secondary (L2) windings of coupled inductor Lt, with the turns ratio of 10:1 delivering 350A to the load with only 20A in Q1.

Fig. 4.4 shows in more detail the currents and voltages within the snubber. The capacitor C2 can be seen to charge up to the clamp voltage and then discharge. The snubber input current flowing through D1 is shown to increase when the main switch is turned off. The last plot in the figure shows the current transferring from the primary n1 of T1 into the secondary n2 and returning to the input of the converter.

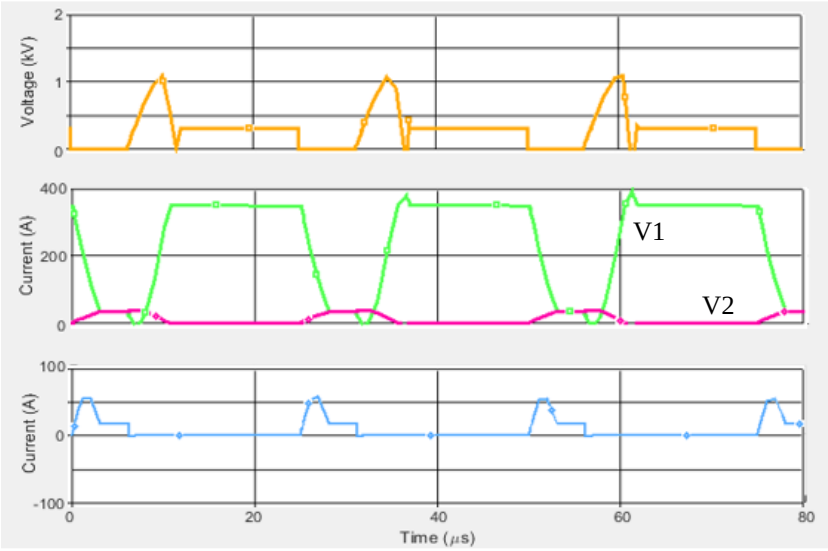


Fig. 4.3 Simulation of regenerative snubber, voltage across Q1 and primary and secondary currents showing conventional operation. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) T1 primary current (n1)

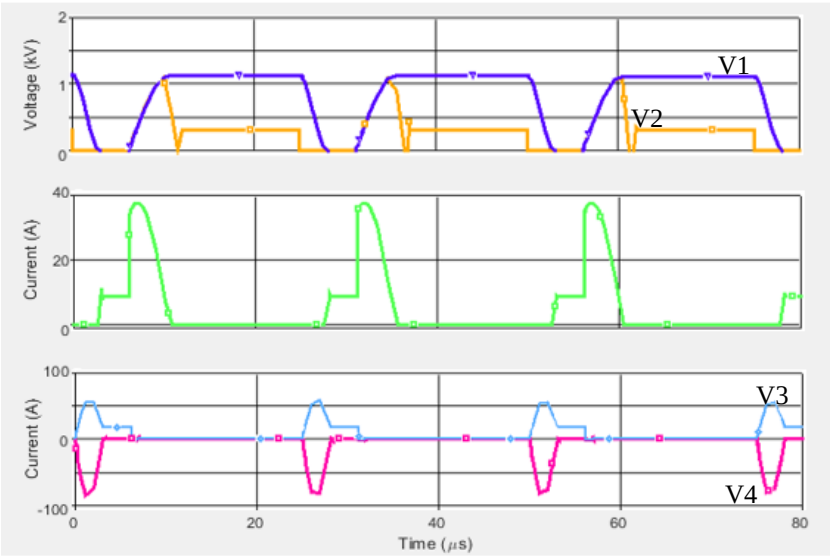


Fig. 4.4 Regenerative snubber operation (a)(V1) C2 Capacitor Voltage, (a)(V2) Q1 Switch Voltage (Vds), (b) Snubber current (D1), (c)(V3) T1 Primary current, (c)(V4) T1 Secondary current

Component		
Primary Inductor	L1	470µH
Secondary Inductor	L2	4.7µH
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1/Q2/Q3	1µΩ (assumed ideal)

4.1.2 Coupled-Inductor Calculations

Ampere-turn balance dictates that the magneto-motive forces (MMFs) in the main coupled inductor Lt must be equal before and after transitions between Mode 1 (on-state) and Mode 2 (off-state). The current I_1 in L1 and the current I_2 in L2 are therefore related by:

$$I_2(off)N_2 + I_1(off)N_1 = I_2(on)N_2 + I_1(on)N_1 \quad (4.1)$$

Since $I_1(off) = 0$ and $I_2(on) = I_1(on)$ then

$$I_2(off)N_2 = I_2(on)N_2 + I_2(on)N_1. \quad (4.2)$$

Rearranging (4.2) gives

$$\frac{I_2(off)}{I_2(on)} = \frac{N_1 + N_2}{N_2}. \tag{4.3}$$

The average current in N_2 is

$$I_{ave} = \delta I_2(on) + (1 - \delta) I_2(off) \tag{4.4}$$

Substituting for $I_2(off)$ gives

$$I_{ave} = \delta I_2(on) + (1 - \delta) I_2(on) \frac{N_1 + N_2}{N_2} \tag{4.5}$$

Rearranging (4.5) gives:

$$I_2(on) = \frac{I_{ave}}{\delta + (1 - \delta) \frac{N_1 + N_2}{N_2}} \tag{4.6}$$

$I_2(off)$ is then calculated as:

$$I_2(off) = \frac{I_{ave}}{\delta + (1 - \delta) \frac{N_1 + N_2}{N_2}} \times \frac{N_1 + N_2}{N_2} = \frac{I_{ave}}{\delta \frac{N_1 + N_2}{N_2} + (1 - \delta)} \tag{4.7}$$

Rearranging (4.7) to give I_{ave} and taking the square root to calculate $I_2(RMS)$ gives:

$$I_2(RMS) = \sqrt{\delta I_2(on)^2 + (1 - \delta) I_2(off)^2} \tag{4.8}$$

This is the relationship between RMS current and duty cycle. The RMS current in conjunction with the number of turns required determines the wire gauge required to realise coupled inductor L1.

In any given inductor *L* with *N* turns, the flux ∅ and current *I* are related by

$$L \frac{di}{dt} = N \frac{d\emptyset}{dt} \rightarrow Ldi = Nd\emptyset. \tag{4.9}$$

Integrating (4.9) to obtain inductance *L* gives

$$L = \frac{NAB}{i}. \tag{4.10}$$

Expressing *B* in terms of the physical properties of the core gives

$$L = \frac{NA\mu_o\mu_r\, Ni}{l\, i} = \frac{A\mu_o\mu_r N^2}{l} \tag{4.11}$$

Rearranging (4.11) in terms of *N* gives

$$N = \sqrt{\frac{L \times l}{A \times \mu_0 \times \mu_r}} \tag{4.12}$$

where l is the magnetic path length and *A* is the cross sectional area of the core.

$$N = \sqrt{\frac{5 \times 10^{-3} \times 310.9 \times 10^{-3}}{796.1 \times 10^{-6} \times 1.2566 \times 10^{-6}}} \times 100 = 124.7 \text{ turns} \tag{4.13}$$

If a turns ratio of 1:100 is used, based on (4.13) N2 = 1.24 turns which is impractical. Peak saturation current occurs at the beginning of Mode 2 when only N2 carries current. This can be calculated from (4.14)-(4.17):

$$H = \frac{I_{peak} \times N}{l} \tag{4.14}$$

$$I_{peak} = \frac{B_s \times l}{\mu_0\mu_r N} \tag{4.15}$$

Where *H* is the applied external magnetic field and B_s is the saturation flux density in the core

The relative permeability of the core, μ_r, can be derived from the A_L values from the manufacturer's data sheet and using (5.11) and $L=N^2 A_L$.

Inserting the design values into (4.15) gives:

$$I_{peak} = \frac{B_s \times A}{A_L N} \tag{4.16}$$

$$I_{peak} = \frac{0.5 \times 5.24 \times 10^{-4}}{1.37 \times 10^{-7} \times 1.25} = 1529A \tag{4.17}$$

4.1.3 Regenerative Snubber Experimentation

The experimental system consists of the proposed DC-DC converter and a microcontroller which can be interfaced in real time through a CAN (controlled area network). The microcontroller samples current and voltage measurements at 40kHz, and records real-time temperature measurements for device protection. The PCB was designed to minimise resistances of current paths (thick, short tracks) and to ensure balanced signal impedances which is especially important as if the paralleled devices turn on at different times the current would be shared unequally and could result in a device failure. Switch Q2 is used as a synchronous rectifier and comprises eight parallel-connected MOSFETs, switched at the same time to ensure equal current sharing. The main components used in the DC-DC converter are summarised in Table 4.1, and the circuit is shown in Fig. 4.5.

Simulation show that poor inductor coupling causes switching voltages that potentially exceed device ratings. To minimise leakage inductance [46], the coupled inductor L1 was densely wound to ensure maximum coupling. An iron powder T520-52 core was used. The L1 winding consisted of 125 turns of single core copper wire. The secondary winding L2 was formed from twelve parallel-connected coils, each having two turns. The resulting N_1:N_2 turns ratio was 62:1. This was not the targeted ratio (100:1) but was the maximum that could be achieved with the core whilst maintaining minimal leakage inductance.

Table 4.1 Principle components of the DC-DC converter

Name	Component	Model	Rating
Q1	MOS Power Transistor	IPB100N	30V
Q2	Power IGBT	IGW15N120H3	1700V
D2-5	Diode D2PAK	ISL9R18120S3ST	1700V
C1	Electrolytic Capacitor	ELH689M016AT6AA	68000µF

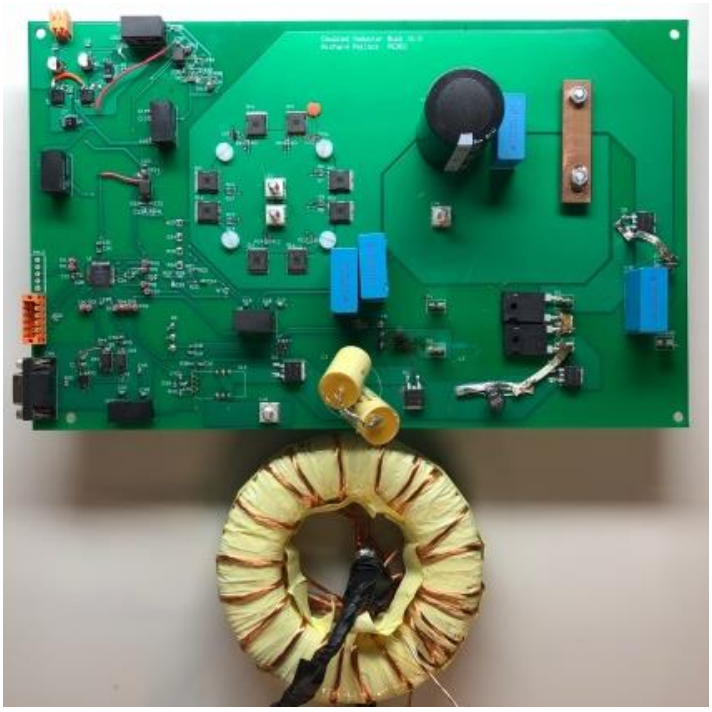


Fig. 4.5 Coupled-inductor circuit prototype

4.1.4 Snubber Testing

The DC-DC converter was initially operated at low power with a coupled-inductor L1 turns ratio N_1:N_2 of 1:16. This is to show that the design operates as intended and would highlight any practical issues.

If the current in the secondary inductor N2 drops to 0A, highlighted by the discontinuous operation shown in Fig. 4.6, current can flow in the reverse direction via the synchronous switch Q2 to the output. When the main switch Q1 turns back on, the voltage across Q2 rises rapidly due to the flux in the core of L1 having to be reversed before current can flow through Q1. This would not usually be an issue as the voltage spike is only around 30V. Due to the need to use a low $R_{DS(on)}$ device, however, a 30V spike would be detrimental to the circuit. As such it was important to initially turn on the circuit without the synchronous switch at this low power just to ensure that the current was flowing in the correct path.

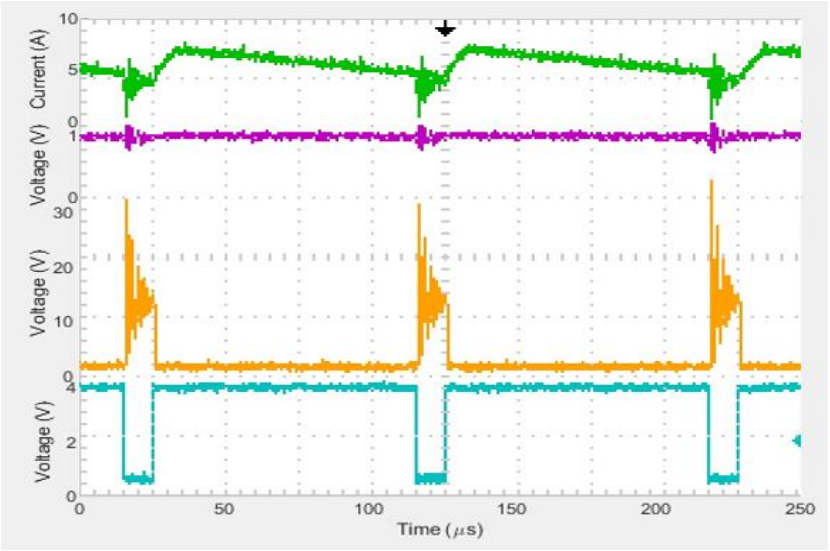


Fig. 4.6 Discontinuous operation with reverse current flow. (a) Secondary (L2) inductor current, (b) Load Voltage R1, (c) Q2 Switch voltage (Vds), (d) Q1 Gate Signal (Vgs)

Once continuous inductor current operation is reached, this is no longer an issue. As shown in Fig. 4.7, Q1 turns on and current in L1 rises rapidly. This is due to existing current flowing in L2 coupling back into L1. The point at which the currents in L1 and L2 become equal is highlighted in Fig. 4.7 by a change in current gradient. At this point, L1 and L2 effectively become series connected. Q1 is then turned off and the energy couples back into L2.

Fig. 4.7(a) shows the voltage across Q1, which drops to zero when Q1 is turned on and rises to the snubber voltage at turn off, preventing an over-voltage. The snubber capacitor is discharged by Q3 when it and Q1 are switched on. The voltage across Q3 at turn off may be large due to the absence of a freewheel path for the energy recovery inductor. A flyback snubber is also possible by interchanging the connections on the secondary inductor, Fig. 4.8. The current which has built up in n1 of T1 is transferred to the n2 of T1 when Q3 is switched off, as shown in Fig. 4.9. Whereas T1 acts as a transformer in the forward converter case, in the flyback case it acts as a coupled circuit that stores energy, then releases that energy. The current in n2 is stepped down due to the 2:1 turns ratio of T1.

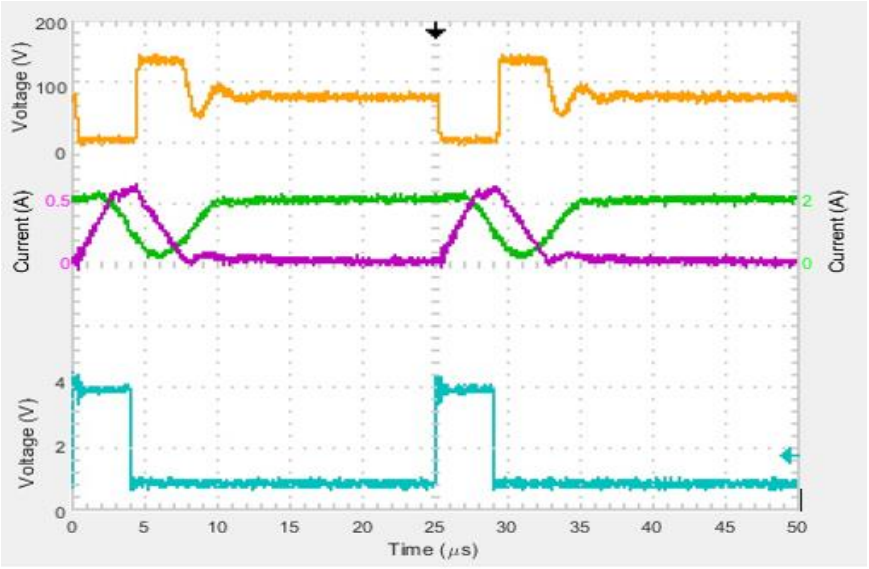


Fig. 4.7 Continuous operation and coupled inductor current transferring from L1 to L2. (a) Q1 Switch Voltage (Vds), (b) Secondary (L2) inductor current, (c) Primary (L1) inductor current, (d) Q1 Gate Signal (Vgs)

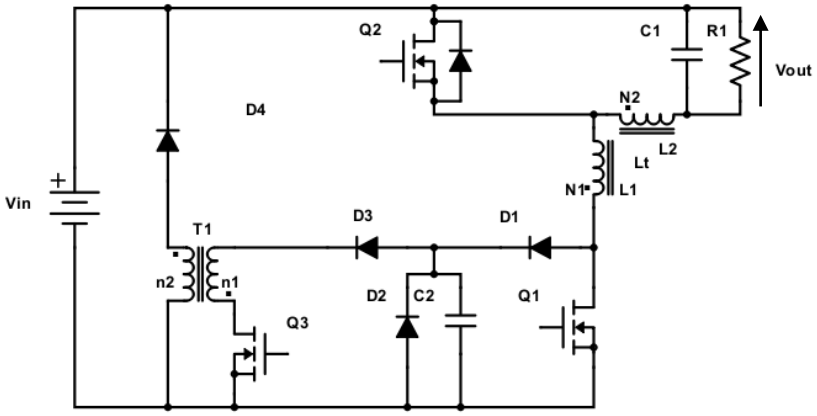


Fig. 4.8. Snubber circuit modified to a flyback configuration (note change in dot convention of T1).

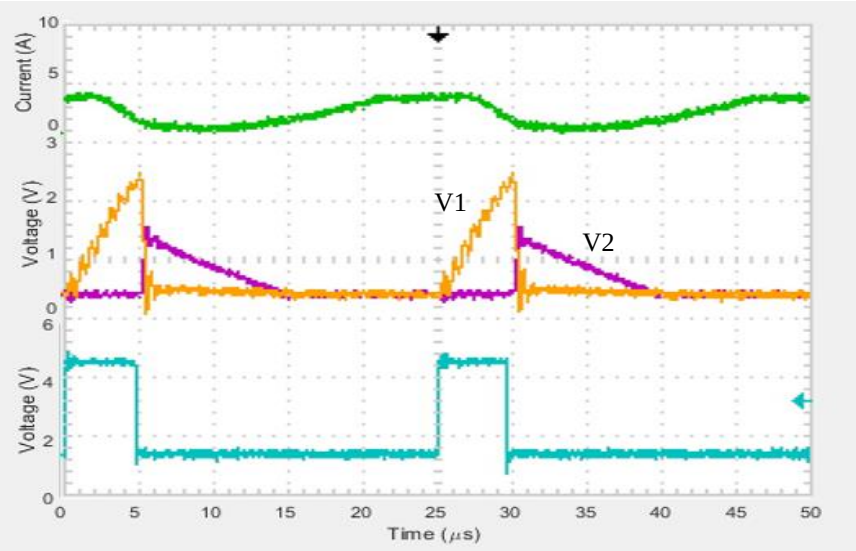


Fig. 4.9 Flyback snubber with N_1:N_2=2:1 turns ratio. (a) Secondary (L2) inductor current, (b)(V1) T1 Primary current, (b)(V2) T1 Secondary current, (c) Q1 Gate Signal (Vgs)

However, limited energy is coupled from the primary L1 into the secondary L2 in the main coupled-inductor circuit. This is due to the regenerative snubber preventing the voltage across Q1 rising above the rail voltage. For energy transfer from the primary to the secondary winding, a voltage difference is required. The voltage across Q1 must be above the input voltage, and the greater this difference the faster the energy transfer. Due to the snubber only allowing a voltage slightly above the input voltage, the energy takes too long to transfer from the primary into the secondary, so is not able to transfer within the oscillatory period. This however can be altered with smaller snubber capacitance which must be designed in accordance to the leakage of each coupled inductor and making the turns ratio of T1 closer to 1:1.

4.1.5 Regenerative Snubber Summary

The proposed snubber provides a route for excess energy to be returned to the input of the converter with no additional control, however also has several challenges. The capacitor must be chosen for a specific inductor leakage inductance which varies from circuit to circuit. Additionally, the snubber switch Q2 must has the same rating as Q1 plus the over-voltage caused by any leakage inductance of the transformer T1. The snubber

inductance and capacitance can be designed so that the current falls to zero before the switch turns off. This will remove the issue of an over-voltage due to the T1 leakage current as the current will be zero. The disadvantage however will be the large peak currents as the current conducts for a shorter period so as to ensure it is zero before the switch transition.

4.2 Buck-boost Clamp Snubber

A clamp snubber presented in [59] protects a main switching device from over-voltage by connecting it via a diode and snubber capacitor, to a supply rail. This supply rail could be the input, output, ground or an intermediary rail. Fig. 4.10 shows a circuit that creates an intermediary rail to act as a clamp snubber. This is achieved by effectively having a buck-boost circuit with the output connected back to the supply. As the supply voltage is fixed this means that the voltage across the input of the buck-boost converter which is supported by C1 can be determined by the duty cycle of Q1 thus creating an intermediary supply rail which the switch is connected to via a diode.

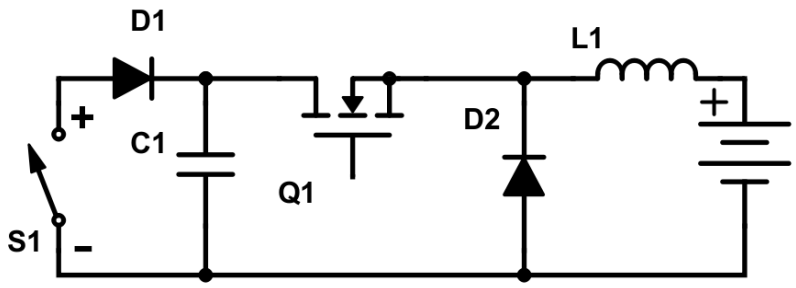


Fig. 4.10 SMPS regenerative snubber, using a buck-boost topology.

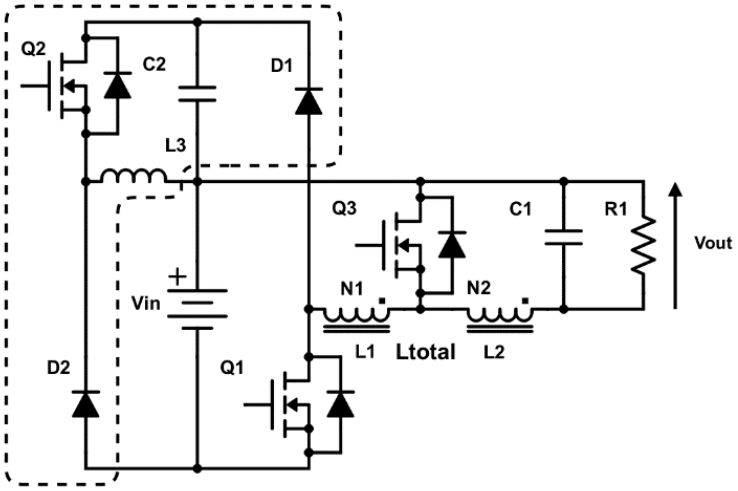


Fig. 4.11. Voltage clamp circuit for single-ended coupled-inductor circuit. The dotted line shows the added buck-boost converter with capacitor C2 referenced to V_{in}.

The circuit in Fig. 4.11 is similar to that in a previously proposed design [59], but in Fig. 4.11 C2 is referenced to the supply voltage which can significantly reduce the required capacitor voltage rating, which should result in circuit cost-savings. Alternatively, the energy can be recovered into the output by reconnecting the anode of D2 to the zero-volt output rail. Such a recovery configuration is not applicable in this application since the necessary recovery switch duty cycle would be very small due to the very low output voltage.

In simulation the capacitor voltage is maintained at 1.5kV by the controlled step up/down SMPS circuit. If only steady-state operation is required, the step up/down SMPS converter can operate with a constant duty cycle. The snubber would be inactive until diode D2 becomes forward biased. Controlling the voltage across C2 limits the voltage across Q1. The SMPS snubber gives the same results as the passive RC variant but is more efficient as energy is recovered back into the supply. Diode D1 may be required to prevent a return path for the capacitor current due to the resonant LC circuit (depending on the values of LC).

The buck-boost clamp was simulated under the same conditions as the snubbers examined in Chapter 2, to ensure a valid test. Similar to the Zener diode snubber, the voltage set point was varied between the two turns ratio voltages. This clamp offers an ideal rail voltage that is controllable by varying the duty cycle of the PWM however possibly fixed

once the circuit design is complete. The circuit produces almost identical results to the Zener snubber for the same turns ratio when the duty cycle is 32% for Fig. 4.12 and 40% for Fig. 4.13. These give a switch voltage of 900V and 700V respectively which is the same as the Zener diode snubber.

The main difference between the Zener diode snubber and the buck-boost clamp is the cost and efficiency of the two circuits. The Zener diode is low-cost, but careful consideration of Zener diode power dissipation is necessary. For example, a 200V 1N3350 stud mounted Zener diode is available but only 10 to 20W of its 50W power rating is usable due to operating temperature limits. This is not a significant issue with series connection of lower voltage Zener diodes, as Zener diodes are cheap but for larger voltages or power dissipation, this solution may become untenable. This should be compared against the component costs of the buck-boost snubber which are modest but in the majority of applications will be more expensive than the Zener diode snubber. The other significant difference is the efficiency of the two switch protection circuits. The buck-boost clamp is simply a buck which can have high efficiencies when returning the energy back to the input whereas the Zener diode creates the threshold voltage by dropping the voltage across it. This energy is lost as heat and so is inefficient. Effectively the two circuits perform the same but for two different commercial cases. The Zener snubber is suitable for a cheap inefficient solution at low powers, and the buck-boost clamp for a more expensive efficient solution for higher power converters.

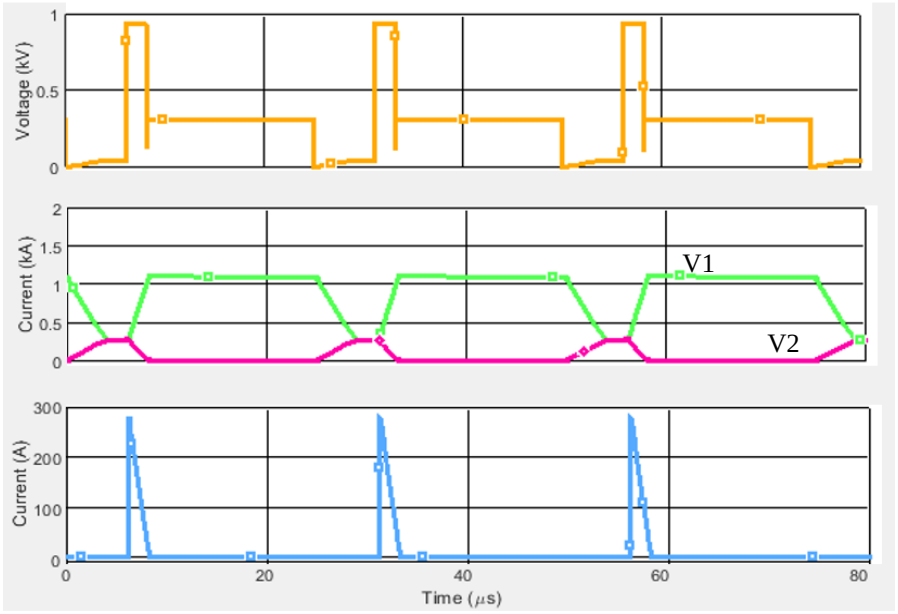


Fig. 4.12 Buck-boost clamp snubber 3:1 turns ratio with 32% snubber switch duty cycle. (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber diode current (D1)

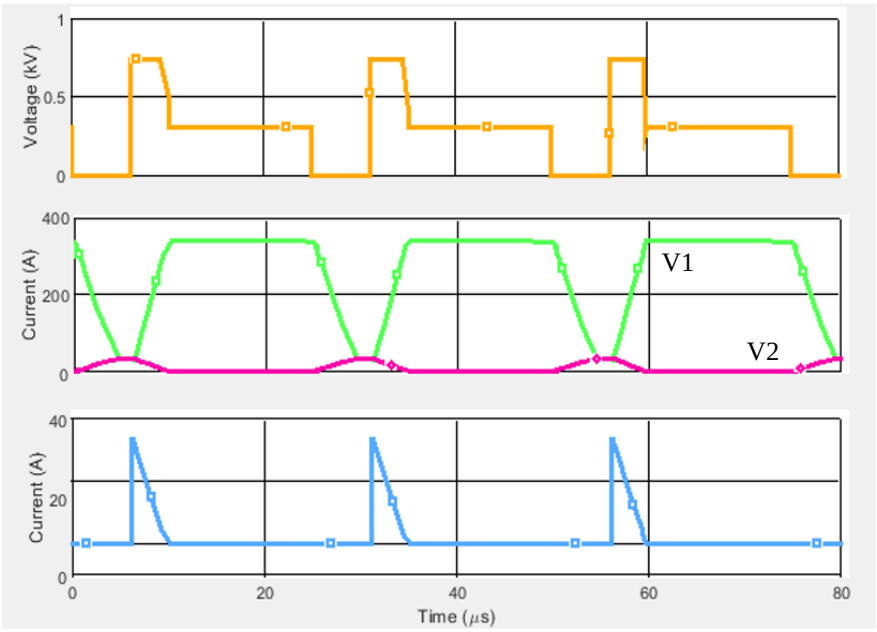


Fig. 4.13 Buck-boost clamp snubber 10:1 turns ratio with 40% snubber switch duty cycle (a) Q1 Switch Voltage (Vds), (b)(V1) Secondary (L2) inductor current, (b)(V2) Primary (L1) inductor current, (c) Snubber diode current (D1)

4.2.1 Investigating the Effect of the Clamping Voltage

One additional feature of the buck-boost clamp is the ability to vary the voltage across the switch. The voltage across C2 must be high enough to force the primary current in L1 to zero. At the end of the switching transition the current $I_{2_{max}}$ in L2 is given by (4.17). The time, t_{tr}, taken for the transfer of energy from the primary N1 turns to the secondary N2 turns is given by:

$$t_{tr} = \frac{L_{leakage} I_{1_{max}}}{V_{C_2} - \frac{N_1}{N_2} V_{out}} \tag{5.17}$$

In order for the energy to transfer from the primary L1 to the secondary L2, the voltage across C2 must be greater than the referred secondary voltage, $V_{out}\ N_1/N_2$. A higher voltage across C2 leads to a shorter transfer time and reduces losses in the windings L1 and L2 as there will be lower peak currents for a given average current. A higher voltage leads to higher switching losses in the main switch. There may therefore be an optimum value for the voltage across capacitor C2 which minimises the losses on the primary side. This will be investigated in Section 4.2.3.

The voltage VC2 across C2 is controlled by the energy recovery switch Q2 in Fig. 4.11. Q2 provides a path to transfer capacitor energy to the input supply via inductor L3. An advantage of the voltage clamp is that it only activates at the controlled voltage level ($V_{in}+V_{C2}$) to protect the switching devices, and at that level, recycles excess energy back to supply Vin.

An advantage of using a clamp is that current only flows into the clamp when its threshold voltage is exceeded. This contrasts with an RC snubber [53], [60] which draws current under all operating conditions, and therefore reduces circuit efficiency. Additionally, a benefit of the voltage clamp circuit is that the voltage across switch Q1 will not rise above the designed clamp voltage regardless of the load, thus ensuring the device is always safe from over-voltage. The voltage clamp is set at a voltage which is appropriate for the switch rating.

The voltage clamp circuit maintains a constant clamp voltage regardless of load, provided the energy recovery circuit is in continuous conduction. However, the clamp voltage will drop at lower loads when the energy recovery circuit enters discontinuous conduction.

4.2.2 Practical Single-Ended Converter

In comparison with a passive snubber, such as RC snubber, the voltage clamp proposed and illustrated in Fig. 4.11 offers switch protection and improved efficiency in a single-ended coupled-inductor converter. The voltage clamp can be controlled using the duty cycle of switch Q2 to determine the voltage of the clamp depending on the switch rating and application. The clamp circuit was tested at different voltages (250V and 385V) to assess its effect on performance and efficiency of the coupled-inductor buck converter. The main input voltage to the converter was 150V which was the maximum possible with the experimental setup.

Fig. 4.14 shows the waveforms for the coupled-inductor buck converter at a clamp voltage of 250 V, and Fig. 4.15 shows the same plots but for a clamp voltage of 385 V. By increasing the clamp voltage from 250V to 385V, achieved by varying the duty cycle of the clamp switch Q2, the rise time of the current in the secondary decreases from 5.6 μs to 2 μs. Thus the circuit has the advantage of output current flowing in the output R1 for a larger percentage of the switching cycle. In each case, the voltage across Q1 is clamped to the chosen clamp voltage and the switch is protected from over-voltage. During this period current flows into the clamp circuit. The experimental plots in Fig. 4.15 confirm the simulation results in Fig. 4.12 and Fig. 4.13.

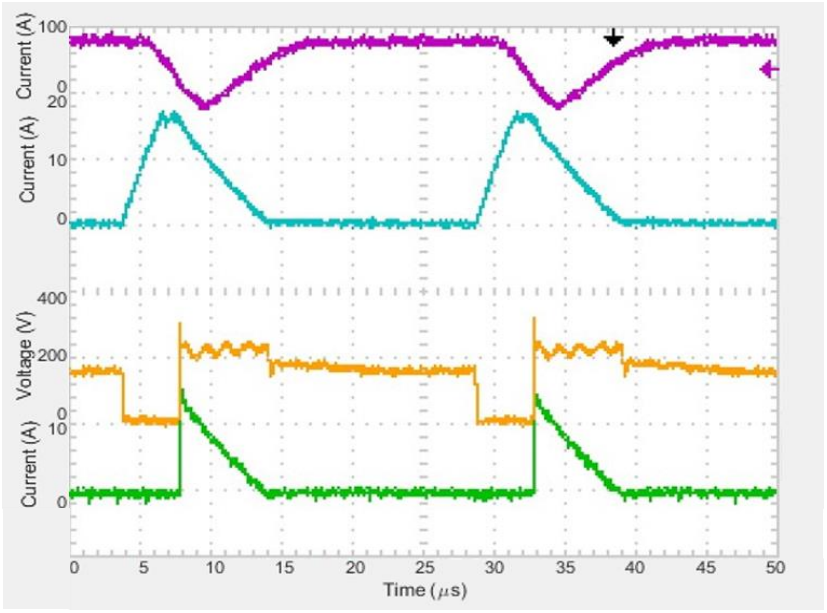


Fig. 4.14 Circuit waveforms at clamp voltage of 250V. (a) Secondary (L2) inductor current, (b) Primary (L1) inductor current, (c) Q1 Switch Voltage (Vds), (d) Snubber diode current (D1)

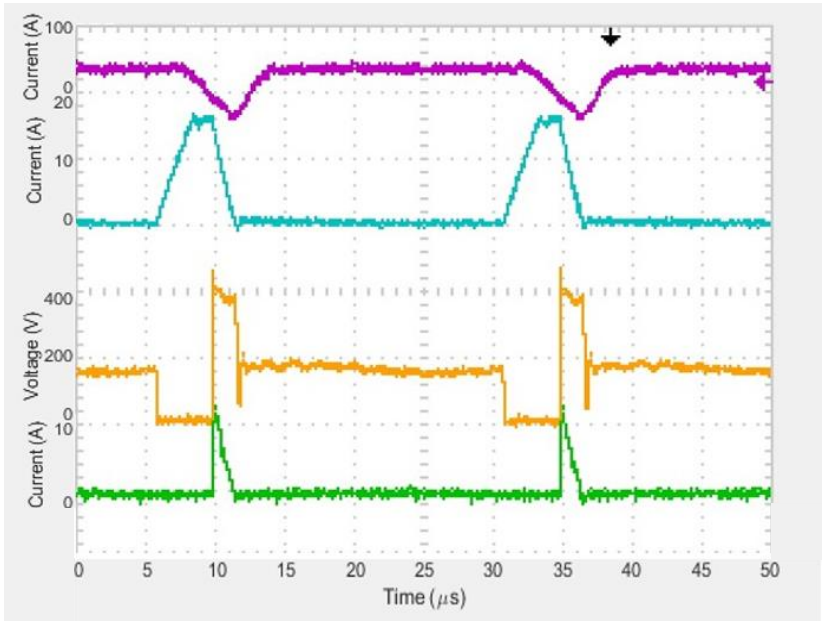


Fig. 4.15 Circuit waveforms at clamp voltage of 385V. (a) Secondary (L2) inductor current, (b) Primary (L1) inductor current, (c) Q1 Switch Voltage (Vds), (d) Snubber diode current (D1)

Fig. 4.16 and Fig. 4.17 show detailed versions of Fig. 4.14 and Fig. 4.15, focused on the on to off transition of the main switch Q1. These are used to calculate switching losses.

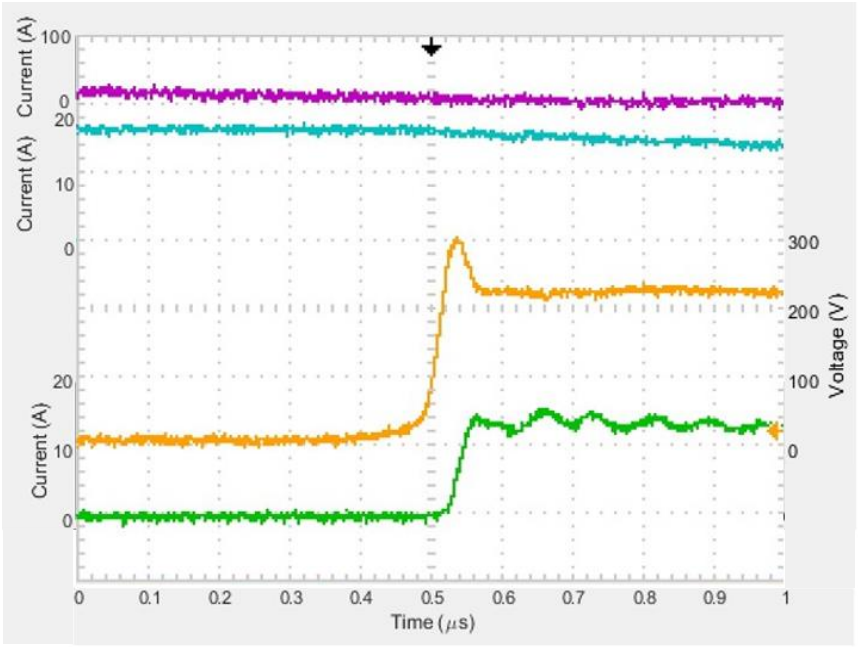


Fig. 4.16. Detailed view of circuit waveforms at clamp voltage of 250V. (a) Secondary (L2) inductor current, (b) Primary (L1) inductor current, (c) Q1 Switch Voltage (Vds), (d) Snubber diode current (D1)

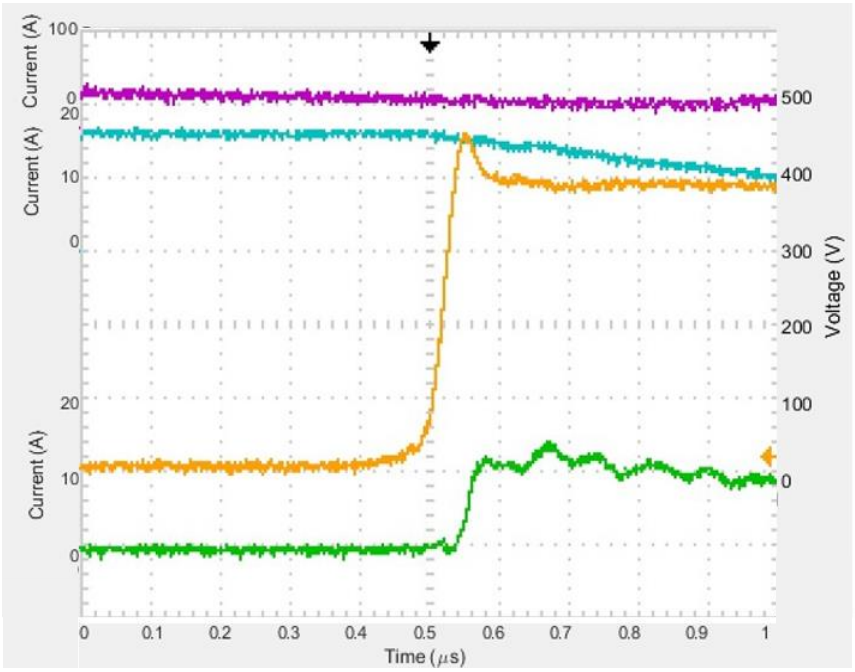


Fig. 4.17. Detailed view of circuit waveforms at clamp voltage of 385V. (a) Secondary (L2) inductor current, (b) Primary (L1) inductor current, (c) Q1 Switch Voltage (Vds), (d) Snubber diode current (D1)

4.2.3 Data Analysis

The clamp on the single-ended converter protects the switch from over-voltage, as is shown in Fig. 4.14 and Fig. 4.15 where the voltage across the switch is controlled to a predefined value. Data was collected to investigate the effect of clamp voltage variation on circuit efficiency. Fig. 4.18 and Fig. 4.19 show the clamp current and voltage respectively, which are used to calculate the instantaneous switching power loss shown in Fig. 4.20.

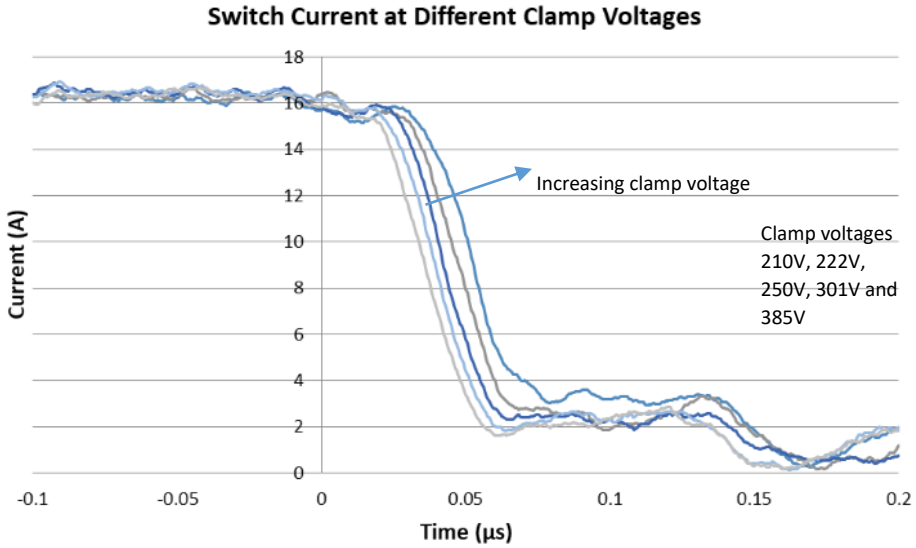


Fig. 4.18 Q1 turn off transition currents at different clamp voltages.

In Fig. 4.18 the highest clamp voltage of 385V creates a current that is slowest to fall whereas the lowest clamp voltage produces the quickest fall. In Fig. 4.19, the largest clamp voltage is 385V which produces the highest voltage across the switch and a clamp voltage of 210V produces the smallest voltage.

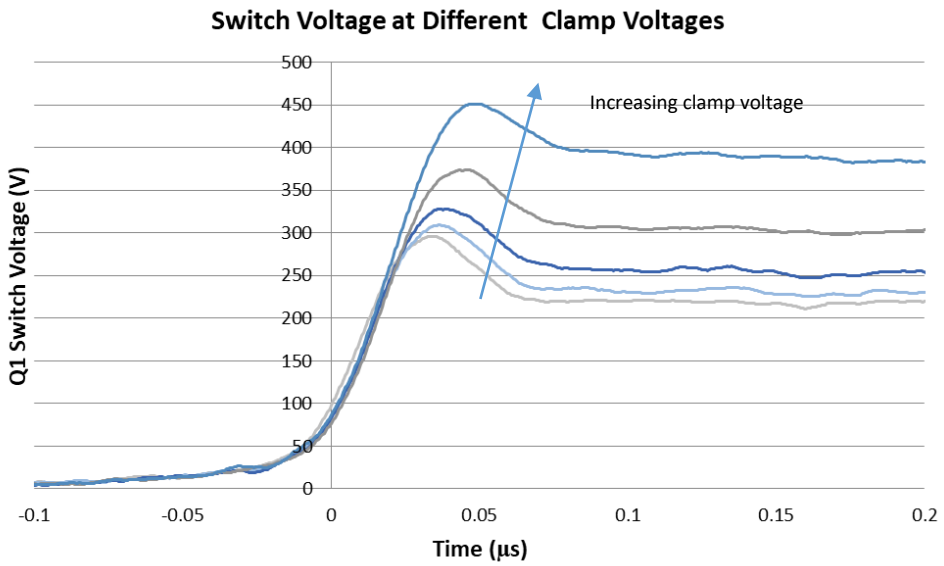


Fig. 4.19 Voltage across main switch Q1 at the turn off transition.

The results in Fig. 4.20 are calculated from the product of the switch voltage and current at a given time instant, for a given clamp voltage. The switching losses increase as clamp voltage is increased. This is due to the increase in current decay time as clamp voltage is increased. The area under each plot gives the total switching loss for one transition.

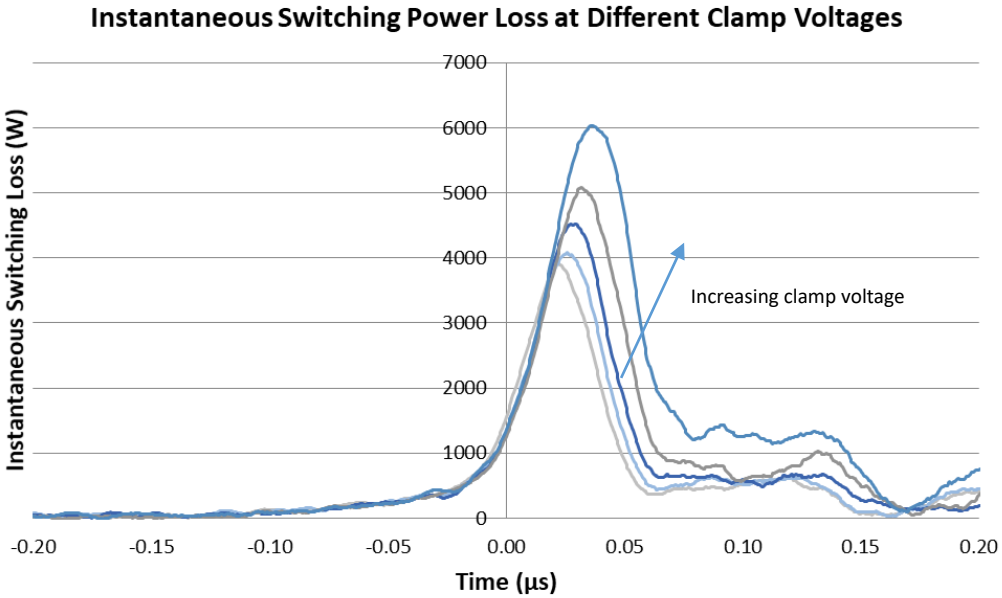


Fig. 4.20 Switching loss dependence on clamping voltage.

Fig. 4.21 presents a summary of all losses in the circuit and shows how they are affected by the clamp voltage. The primary side conduction losses are significantly less than those in the secondary side due to there being significantly more current in the secondary N2 and the primary duty ratio being only 15%. The switching loss on the primary side increases by 15 W (or 5% of input power) when the clamp voltage increases from 210 V to 385 V, while the conduction losses show minimal decrease. The switching losses therefore dominate the overall efficiency. More efficient modes of operation therefore occur at lower clamp voltages.

The losses shown in Fig. 4.21, however, do not account for the losses within the clamp itself. A lower clamp voltage means a higher current flow through the clamp. This introduces additional losses as the clamp switch will also have switching and conduction losses. These however were not analysed in this investigation.

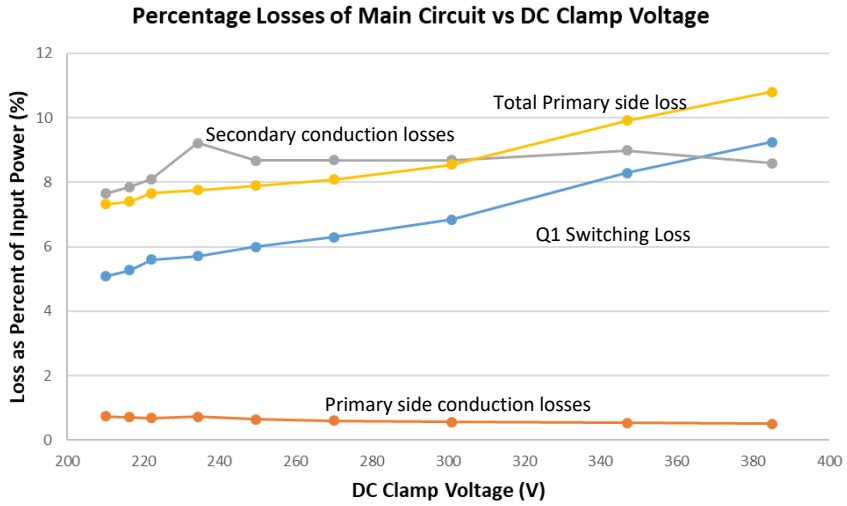


Fig. 4.21 Summary of switching and conduction losses.

4.3 Summary

Two switch protection circuits were presented and analysed in this chapter. First the fly-forward regenerative snubber and then the buck-boost clamp snubber. Both snubbers where proven to function as expected however both have their disadvantages. The switch protection circuits are complicated and require additional design considerations. The fly-forward snubber has the additional complexity of a transformer and the buck-boost requires a separate control signal for the additional switch. The ability to control the

voltage level of the snubbering is possible with both the switch protection circuits. The buck-boost clamp snubber is thought to be most promising of the two due to the ability to actively control the clamping level. The results from this converter will be compared against the novel Asymmetrical Half-Bridge Coupled inductor buck presented in chapter 5.

Chapter 5 Asymmetrical Half-Bridge Coupled-Inductor Buck Converter

Chapter 4 discussed active snubber clamping circuits that protected a main switching device from over voltage. Each of the circuits presented offered advantages and disadvantages. The buck-boost clamp snubber offered the best solution as it was controllable and guarantees switch protection with no drawbacks other than the cost of implementing it.

In this chapter a final snubber clamping topology is presented and compared to the buck-boost clamp snubber. The asymmetrical half-bridge coupled-inductor buck is presented as a novel circuit that offers switch protection with no additional control.

5.1 Asymmetrical Half-Bridge Coupled-Inductor Converter

The converter shown in Fig. 5.1 is the asymmetrical half-bridge coupled-inductor buck converter. Two switches, Q1 and Q2, are used to apply the input voltage to the coupled inductor and output circuit. When Q1 and Q2 turn off, the current transfers into clamping diodes D1 and D2. This effectively changes the potential difference across the coupled inductor from V_{in} to $-V_{in}$ which creates an effective voltage swing of $2V_{in}$. Thus, the current transfer time is quicker than for the conventional coupled-inductor buck converter. The current in primary winding L1 is forced to zero and the secondary current can flow in the synchronous rectifier Q3. Both switches Q1 and Q2 are protected from the effects of leakage inductance by their associated diodes, D1 and D2, which clamp them to V_{in} for Q1 and *GND* for Q2.

A coupled-inductor circuit driven by an asymmetrical half-bridge uses the supply to protect the main switching devices from over-voltage. Although the clamping circuit uses two switches and two diodes, the devices are all rated just above the input supply voltage as the voltage cannot rise above this. This type of switch protection is found in two switch flyback converters, [55], [56] but this is its novel use with the coupled-inductor buck converter.

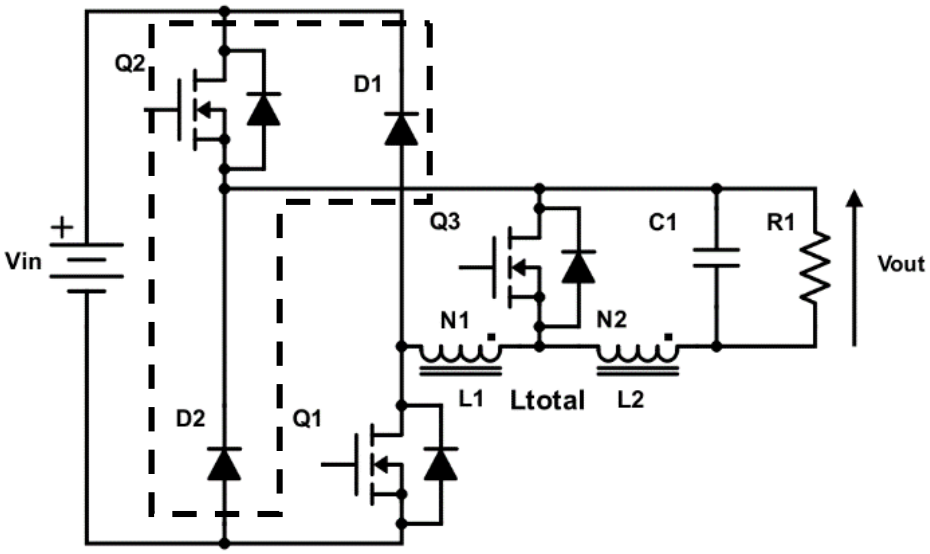


Fig. 5.1 Asymmetrical half-bridge coupled-inductor circuit.

5.1.1 Simulation of the Asymmetrical Half-Bridge

Fig. 5.2 shows simulation results for the asymmetrical half-bridge coupled-inductor circuit in Fig. 5.1, where V_{in}=200V, δ=16%, N_1:N_2=10:1, R_1=4mΩ and C_1=6.8mF. Hard rail clamping of a bridge switch and diode is seen in Fig. 5.2.

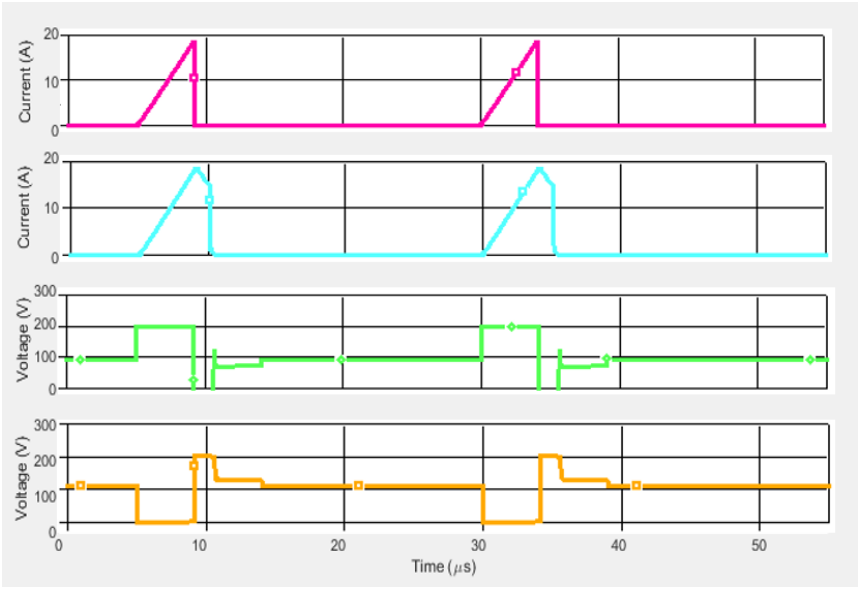


Fig. 5.2 Simulated switching waveforms of the asymmetrical half-bridge coupled-inductor buck converter. (a) Q1 source current, (b) Primary (L1) inductor currnet, (c) D2 Voltage, (d) Q1 Switch Voltage (Vds)

Table 5.1 Component values for Asymmetrical Half-Bridge simulation

Component		
Primary Inductor	L1	470µH
Secondary Inductor	L2	4.7µH
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1/Q2/Q3	1µΩ (assumed ideal)

5.1.2 Experimental Results

The main objective of the experimental aspects of this thesis is to demonstrate practical circuits can achieve high voltage step down in a single stage. In order to ascertain practically circuit properties and limitations of the asymmetrical half bridge and the single ended buck clamp snubber circuits, the following operating conditions were used: 150 V input voltage, 16% duty cycle, 2.6V output voltage, 10:1 coupled inductor turns ratio, and 300W (115A) power throughput. Both converters were experimentally tested to evaluate switching losses and conduction losses with the fixed input voltage, duty cycle, and coupled inductor turns ratio.

The switches were controlled via a board-mounted microcontroller to ensure minimal noise on the gates of the devices. The same PCB output stage consisting of C1, R1, Q3 and the coupled inductor L1 and L2, was used for both the asymmetrical half bridge and the buck-boost clamp snubber circuits to ensure a valid comparison between the two circuits. The experimental components are detailed in Table 5.2.

Table 5.2 Component for experimental hardware, used for both the asymmetrical half-bridge and single-ended converter.

Name	Component	Model	Values	Rating
Q3	MOS Power Transistor	IPB100N		30V
Q1, Q2	Power IGBT	IGW15N120H3		1700V
D1, D2	TO-247 Diode	VS-40EPS12-M3		1200V
L1	Iron Powder Inductor	T520-52 core (10:1 turns ratio)	60.8mΩ 497µH	
L2	Iron Powder Inductor	Shared core with L1	2.6mΩ 4.7µH	

5.1.3 Asymmetrical Half-Bridge Testing

The asymmetrical half-bridge coupled-inductor buck converter with an input voltage of 150V gives a total change of 300V (or $2V_{in}$) across the coupled inductor during the switching transition of the main switch Q1. To enable a comparison, the single-ended converter also requires 300V across the coupled inductor and so is controlled to have a clamp voltage of 300V, that is, V_{C2}=150V. The conduction losses in the diodes are ignored as they only conduct for a short period. The switching losses in the diodes are zero due to the fact the diode current falls to zero before the switch turns back on and a voltage is applied across the diode.

Fig. 5.3 presents results from the practical half-bridge circuit configured and controlled to give an output voltage of 2.6V.

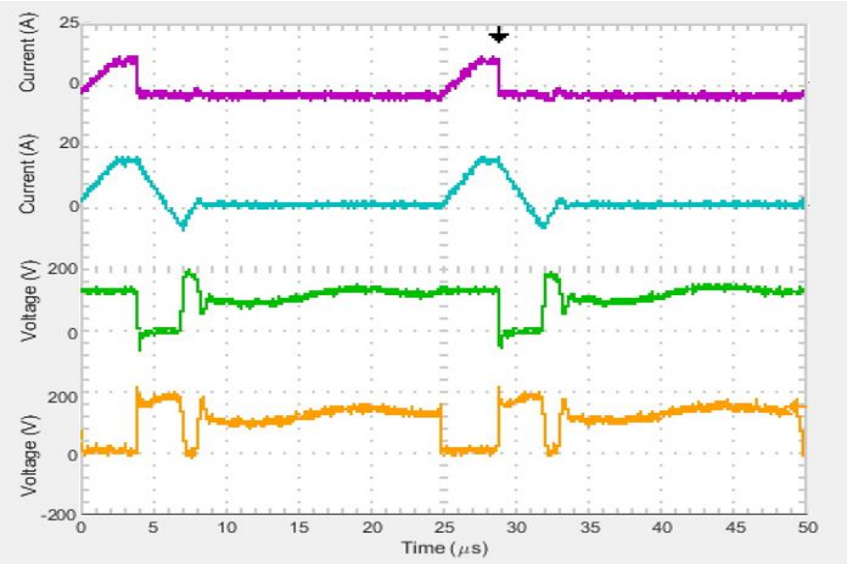


Fig. 5.3 Switching waveforms of the asymmetrical half-bridge coupled-inductor buck converter. (a) Q1 source current, (b) Primary (L1) inductor current, (c) D2 Voltage, (d) Q1 Switch Voltage (Vds)

From Fig. 5.3, as Q1 turns off, its voltage rises from zero to 150 V whilst the diode voltage simultaneously falls from 150 V to zero and begins conducting. The voltage across the coupled inductor is the difference between the voltages across diode D2 and switch Q1. This demonstrates the 300V potential that is created across the coupled inductor in the

transition period. The switch current (top trace) shows that when the switch Q1 is on all of the primary current flows through Q1. Q2 conducts the same current. When switch Q1 turns off the primary current does not fall to zero instantaneously but finds a current path through D1 and falls to zero over time. The experimental results follow those simulated in Fig. 5.2.

Fig. 5.4 shows the detailed view of the turn-off waveform of Q1. This can be used to calculate the switching losses of switches Q1 and Q2. The switching losses are the product of the voltage across the switch multiplied by the current through it.

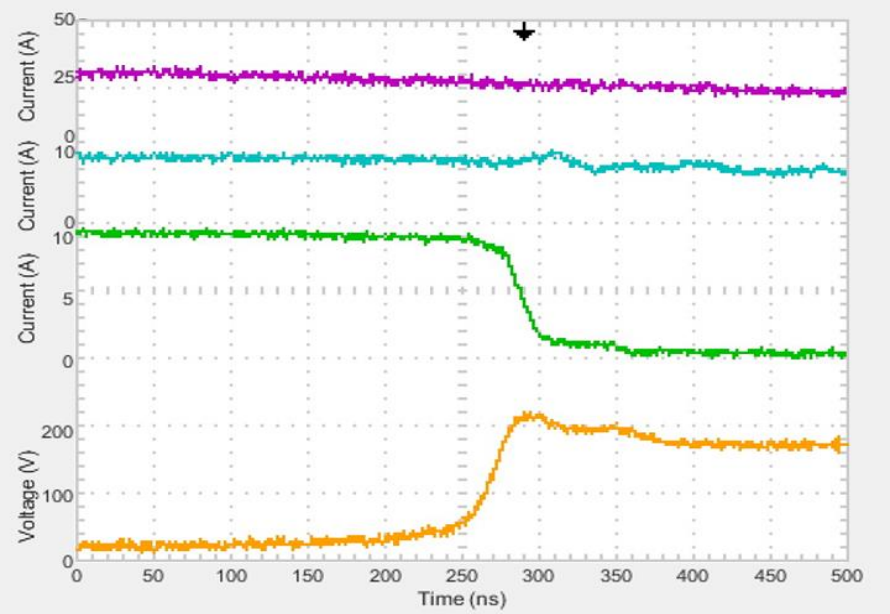


Fig. 5.4 Detailed switching waveforms of the asymmetrical half-bridge coupled-inductor buck converter. (a) Secondary (L2) inductor current, (b) Primary (L1) inductor current, (c) Q1 source current, (d) Q1 Switch Voltage (Vds)

Table 5.3 presents loss information for the asymmetrical half-bridge coupled-inductor buck converter operated with output voltages of 1.5V (δ=10%) and 2.6V (δ=16). The results show that efficiency increases with power. This is due to the switching losses increasing by a smaller proportion than the increase in power. The secondary conduction loss increases approximately linearly with power and the primary loss increases fourfold.

Table 5.3 Asymmetrical half-bridge power loss and efficiency at 120W and 300W output.

	120W (1.5V)	**300W (2.6V)**
Switching Loss	10.73W	11.87W
Primary Loss	0.43W	1.64W
Secondary Loss	12.17W	21.30W
One Switch Conduction Loss	3.32W	3.32W
Total Losses	29.98W	41.46W
Percentage Efficiency	74.05%	84.39%

5.1.4 Results Comparison

Once the asymmetrical half-bridge coupled-inductor buck converter had been tested the results were compared to that of the buck-boost clamp snubber presented in chapter 4. Both circuits used the same input voltage, turns ratio, duty cycle. To be able to quantify a comparison of the efficiency of an asymmetrical half-bridge converter, Fig. 5.1, to the buck-boost voltage clamped coupled-inductor converter, (Chapter 4, Fig. 4.10), a supply voltage of 150V and a clamp voltage of 300V were chosen to give the same 300V potential difference across the coupled inductor in both circuits during Q1 transitions. The asymmetrical half-bridge main switches (Q1 and Q2) are rated to at least V_{in} whereas switch ratings of at least $V_{in}+V_{C2}$ are required for the single-ended converter. This advantage of the asymmetrical half-bridge was not utilised in these tests as the same devices were used for both to enable a fair comparison of the losses.

As shown in Fig. 5.5, for a 300V inductor potential difference, the asymmetrical half-bridge offers higher efficiencies. The comparison between the two converters does not account for the losses in the buck-boost clamp switch Q2. These losses could however become significant at lower clamp voltages due to the increase in clamp current flowing, and if they were included in the comparison the buck-boost clamp circuit efficiency would be further reduced. The comparison at 300V therefore shows that the asymmetrical half-bridge circuit offers better efficiency and lower rated devices.

Fig. 5.5 also shows that the clamp circuit efficiency is higher for clamp voltages of 210V and 216V. At these lower clamp voltages however it is likely that the clamp losses, which are neglected here, would be proportionally greater due to a higher clamp current. Additionally, the comparatively lower rated MOSFET devices that can be deployed in the asymmetrical half-bridge converter offer lower conduction losses. In combination these two effects suggest that the asymmetrical half-bridge converter will exhibit an efficiency advantage under all operating conditions.

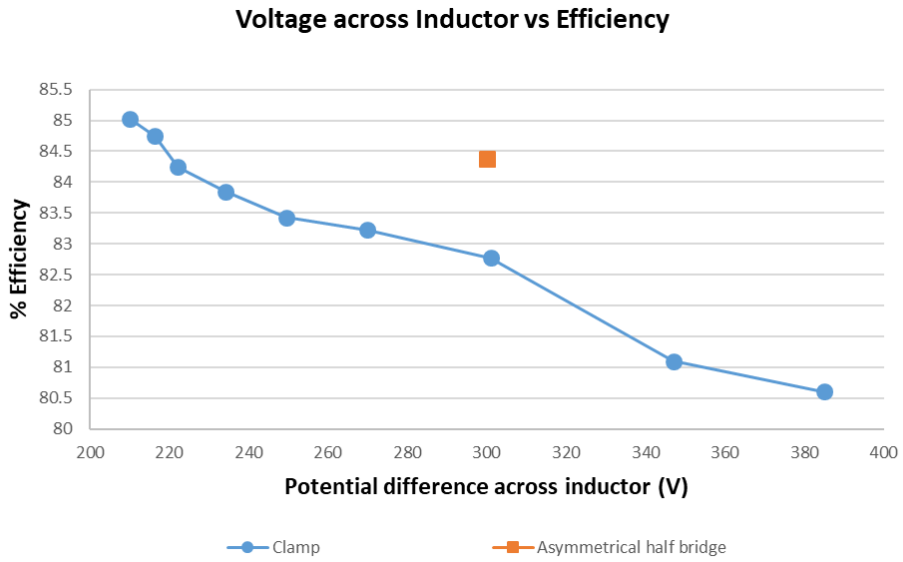


Fig. 5.5 Asymmetrical half-bridge and single-ended voltage clamped, coupled-inductor converter efficiencies versus inductor potential difference.

The asymmetrical half-bridge requires no additional control to operate, as the additional switch is controlled from the same gate signal as switch Q1 although an isolated gate driver is required for Q2. Both topologies require two switches.

As already highlighted, a further benefit of the asymmetrical half-bridge is that the four power devices in the bridge only need to be rated at V_{in} whereas in the clamp both switches and additional diodes should be rated above the clamp voltage ($V_{in}+V_{C2}$). The asymmetrical half-bridge coupled-inductor converter utilises diode clamping to protect the switches and create the required voltage across the coupled inductor.

A desalination plant would be powered from a rectified three-phase AC supply creating a DC supply voltage V_{in} of just under 600V. The asymmetrical half-bridge converter can therefore utilise 800V devices whereas the single-ended converter would require 1200V,

or even 1700V, rated devices. The additional cost of the asymmetrical half bridge components is not a significant amount given the benefits they offer.

Another benefit is the ability to use a conventional bootstrap gate driver on both primary side devices. This is normally a drawback on the conventional coupled-inductor buck converter.

5.2 Summary

A novel asymmetrical half-bridge coupled-inductor buck converter circuit was presented and compared with a single-ended coupled-inductor buck converter with a buck-boost voltage clamp. The results show that the asymmetrical half-bridge converter provides an efficient circuit to drive the coupled-inductor buck converter. The problematic leakage energy of the primary winding was managed within the bridge avoiding the need for a snubber circuit. The two switches are rated at just above the input supply voltage. Using the asymmetrical half-bridge to drive a coupled-inductor buck converter requires only one control signal as both switches on the primary side are switched simultaneously.

The single-switch coupled-inductor converter has the benefit of a single switch in the main forward path but needs an additional clamp circuit to control the voltage induced by the leakage energy of the coupled inductor. This introduces the comparative disadvantage of requiring separate control for the duty cycle of the clamp switch.

Whilst the investigation has shown that lower clamp voltages can offer an efficiency advantage when compared to the asymmetrical half-bridge circuit, full consideration of the clamp losses together with the efficiency advantages offered by lower rated MOSFET devices suggest that the asymmetrical half-bridge circuit will tend exhibit better efficiency.

In the desalination application, the high turns ratio between primary and secondary increases the leakage inductance. The asymmetrical half-bridge offers the most robust solution and highest efficiency because the leakage energy is recovered, and the switch voltages are clamped to within the voltage rating of the bridge.

Chapter 6 Experimental Results – Asymmetrical Half-bridge Flyback

The previous chapters investigated various circuits and topologies that combined could be used for the desired water desalination application. Chapter 3 showed the comparison of the coupled-inductor buck the flyback and the buck circuit and concluded that both the flyback and coupled-inductor buck converter offered significant benefits over the buck converter especially for large voltage step down ratios. The analysis showed that for small step down ratios, the coupled-inductor buck offered an added advantage over the flyback circuit with far lower peak currents for a given turns ratio. With a large step-down ratio, the coupled-inductor buck converter has little advantage over the flyback converter. The flyback converter however offers the additional bonus of isolation which for such a large voltage difference and a load that involves water is advised. The flyback still has the issue of leakage energy and similarly needs a snubber or clamp snubber to protect the main switch from over voltage. From chapters 2, 4, 5 various snubbers and clamp snubbers were proposed and investigated for the coupled-inductor buck converter, and these are all applicable to the flyback converter. Passive snubbers were ruled out due to their inefficiency. Chapter 4 and 5 described various active voltage clamping methods. The two most efficient and promising were the buck clamp snubber and the asymmetrical half-bridge. These were analysed and due to the simplicity of design and the ability to derate the components, the asymmetrical half-bridge is seen as a better option even though the buck clamp snubber has the possibility to offer marginally better efficiencies in certain conditions.

Assimilating all these characteristics and factors, the asymmetrical half bridge flyback converter in Fig. 6.1 is chosen as the circuit to fulfil the application requirements. A summary of the experimental test performed appears in Table 6.3 at end of this chapter.

6.1 Asymmetrical Half-bridge Flyback Circuit Topology

The half-bridge flyback converter in Fig. 6.2 is to operate at 40kHz, from an input voltage of 340V DC (rectified 230V AC). The specification is a step-down ratio of 340:1 at its

maximum, falling to 190:1 with a power rating of 720W, producing an output current of at least 400A.

Basic simulations, Fig. 6.2. established the expected viability of the asymmetrical half bridge flyback concept being purported. All semiconductor voltages are clamped, confirming successful managing of transformer leakage inductance energy.

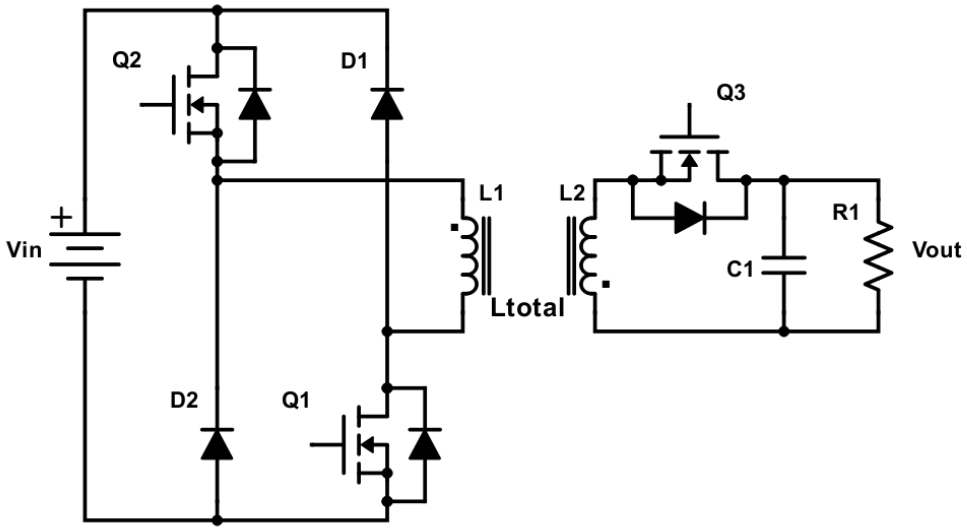


Fig. 6.1 Asymmetrical half-bridge flyback converter

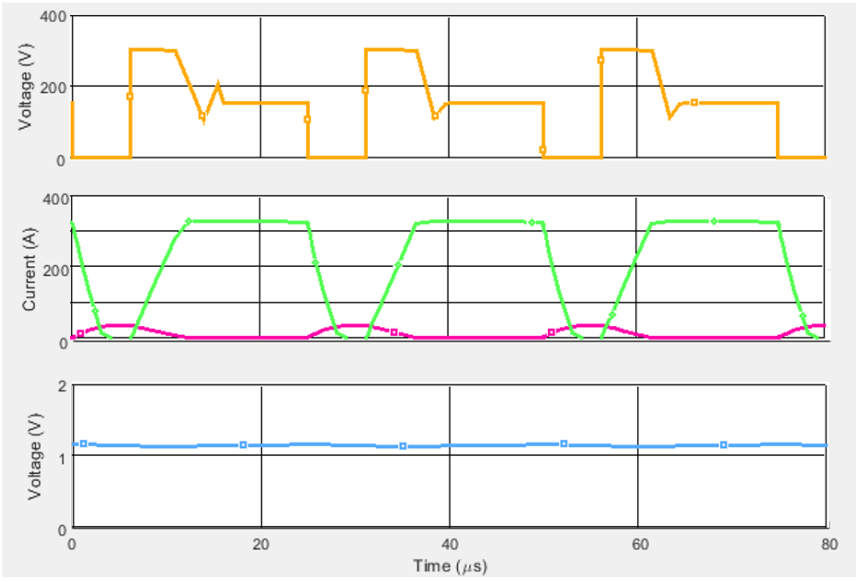


Fig. 6.2 Affirmation simulations of the asymmetrical half-bridge flyback converter.
(a) Q1 Switch Voltage (Vds), (b) Secondary (L2) inductor current, (c) Primary (L1) inductor current, (d) Output Voltage (Vout)

Table 6.1 Component values for Asymmetrical Half-Bridge Flyback simulation

Component		
Primary Inductor	L1	470µH
Secondary Inductor	L2	4.7µH
Load	Rout	0.005Ω
Output Capacitor	Cout	50mF
MOSFET RDSon	Q1/Q2/Q3	1µΩ (assumed ideal)

6.2 Implementation of Flyback Converter

Constructing the final prototype consisted of two main parts the software and the hardware.

Silicon Carbide devices (MOSFETs and diodes) were used for the asymmetrical half-bridge of the flyback converter. Silicon Carbide devices are relatively new to commercial uses in power electronics but exhibit reduced switching losses. At 40kHz, the inductor physical size can be reduced as less inductance is required for a given ripple current.

The hardware layout was designed on Altium PCB designer and consisted of a two-layer board with the majority of the components on the top side for easier debugging and thermal testing. The PCB model is shown in Fig. 6.3. The main circuit components are listed in Table 6.2:

Table 6.2 Experimental Component Choices

Component	Part Number
Microcontroller	dsPIC33EP128MC504-IPT
Primary SiC MOSFETs	C3M0120090D
Primary Diodes	IDH02G120C5
Secondary MOSFETs	IPB100N
Isolated Power supplies	MGJ2D151505SC
Gate Drivers	1EDI60N12AF

Circuit diagrams, PCB layout, and design criteria and constraints are presented in Appendix A. Details of the software are given in Appendix B.

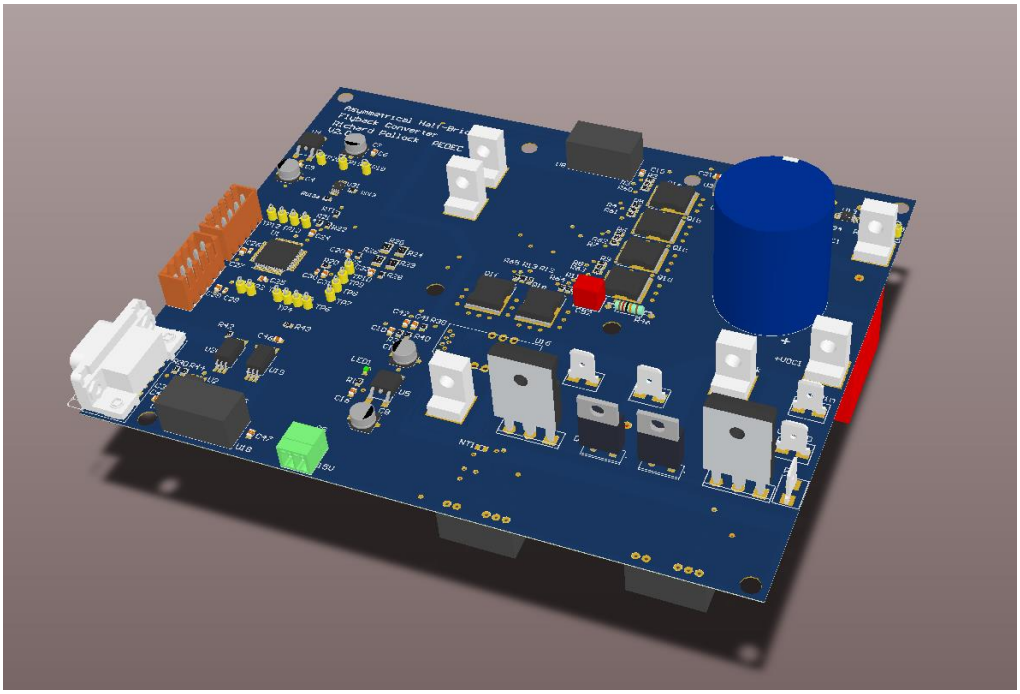


Fig. 6.3 3D model of final PCB design

Constructing the final prototype consisted of two main parts the software and the hardware.

6.2.1 Hardware Design

The hardware was designed on Altium PCB designer and consisted of a two-layer board with the majority of the components on the top side for easier debugging and thermal testing. The PCB schematics are shown below detailing the Microcontroller used and the measurement and isolation chips in Fig. 6.4 and the main power circuit and gate drivers in Fig. 6.5.

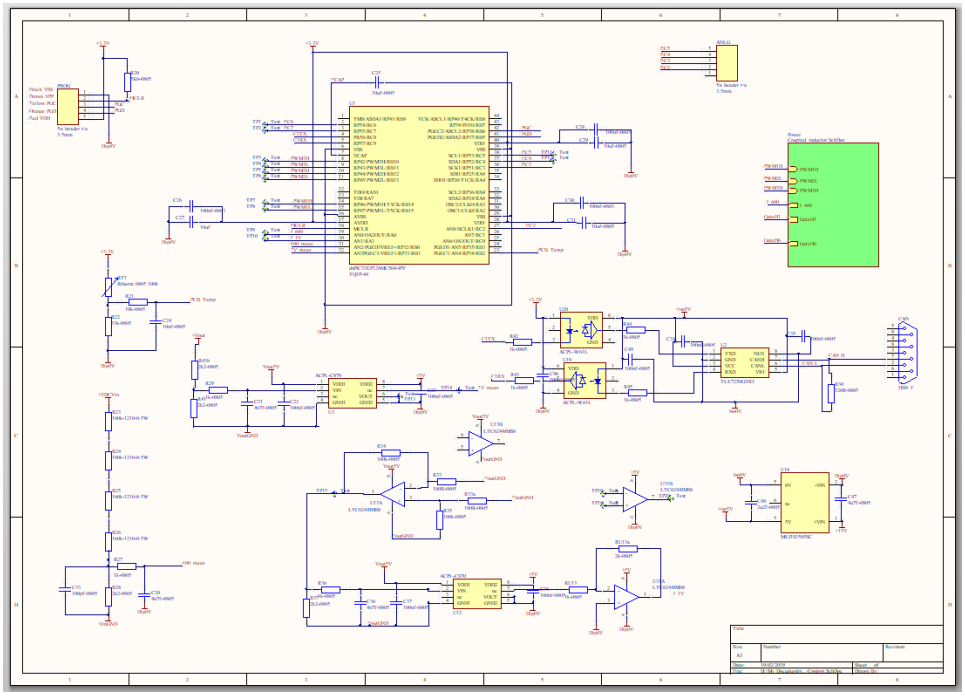


Fig. 6.4 Control and measurements Altium schematic

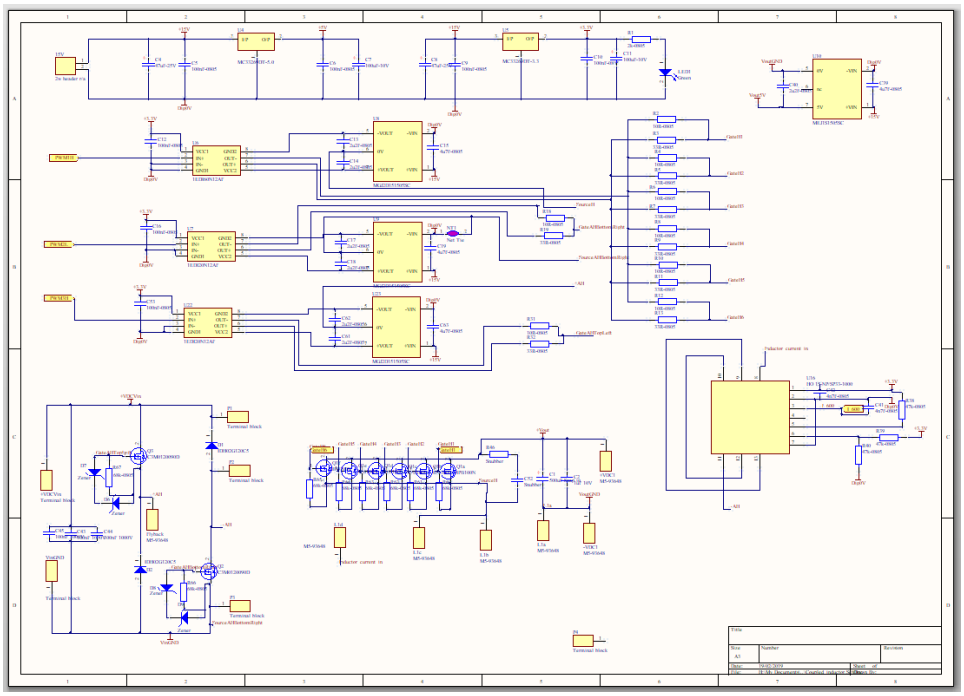


Fig. 6.5 Power and gate driver Altium schematic

The board was designed in two halves with the logic and measurements isolated from the main power stage. The main current path was split into two parts the high current and low voltage path and the low current and high voltage side. The high current side can be seen to have a far greater copper trach width for the current to flow through Fig. 6.6. In the top

right corner of Fig. 6.6 a large C shaped track can be seen. The design of this was to allow measurement of the high output current. It is difficult to measure a current in excess of 200A. The method utilised instead was to measure the voltage drop across a track of known resistance and this could be used to calculate the current. The track has low resistance but due to the large current there is a measurable meaningful voltage drop. The C shape track comes about from ensuring that the voltage drop measured is just that of the DC current and so the AC currents are absorbed by the capacitors on a different branch of the track.

Another carefully designed part of the PCB was the gate signals to the six parallel secondary MOSFETs. It is paramount that these turn on at the same time to ensure they share the current evenly and so that they each experience an equal loading. To do this each device has a turn on and turn off resistor, this resistance dominates the track resistance and creates a largely equal resistance. In addition to this the distance of each gate signal was matched as far as possible.

As well as the secondary switches needing careful design, the gate signals to the primary switches were carefully considered. The primary MOSFETs were chosen to be silicon carbide devices. These are very fast and efficient switches however can cause EMI problems if not carefully considered. To deal with this the gate signals to the gate and returning from the source were kept as short as possible to minimise any ringing.

The second half to the PCB design is simpler with the main design consideration of trying to keep all of the logic and measurements as far from the noisy primary MOSFETs as possible.

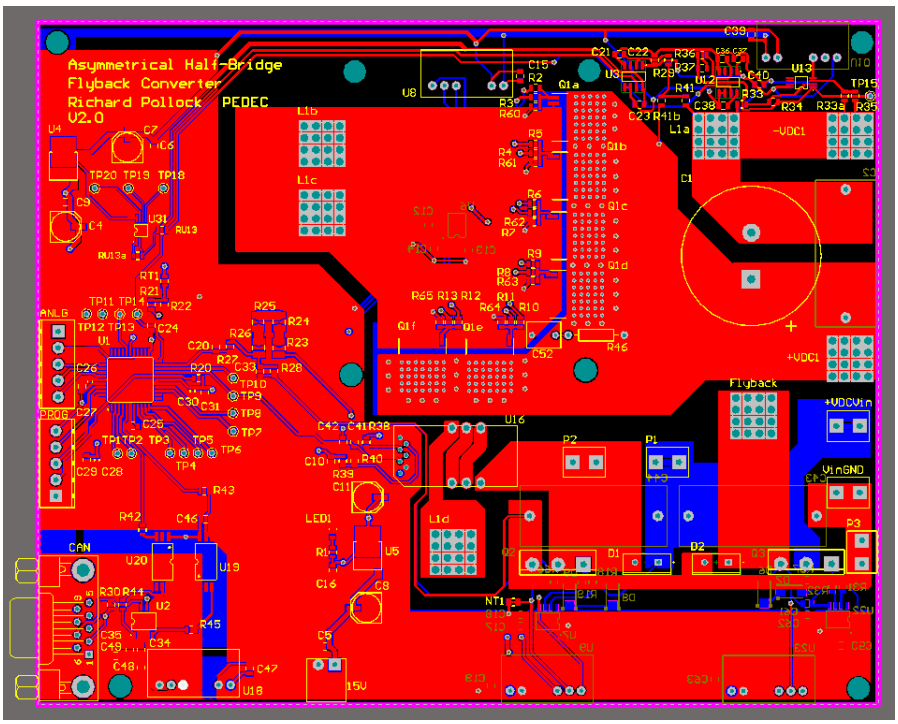


Fig. 6.6 Altium PCB layout

6.2.2 Software Design

The converter was controlled by software created for the on-board microprocessor. The board facilities could then be controlled in real-time through the external *can* connection enabling live data recording or for manual control of the current targets or the mode of operation. The converter was setup to run with the control loop shown in Fig. 6.7, which incorporates a PI controller acting on the primary side current which ensures the power flow through the converter is controlled.

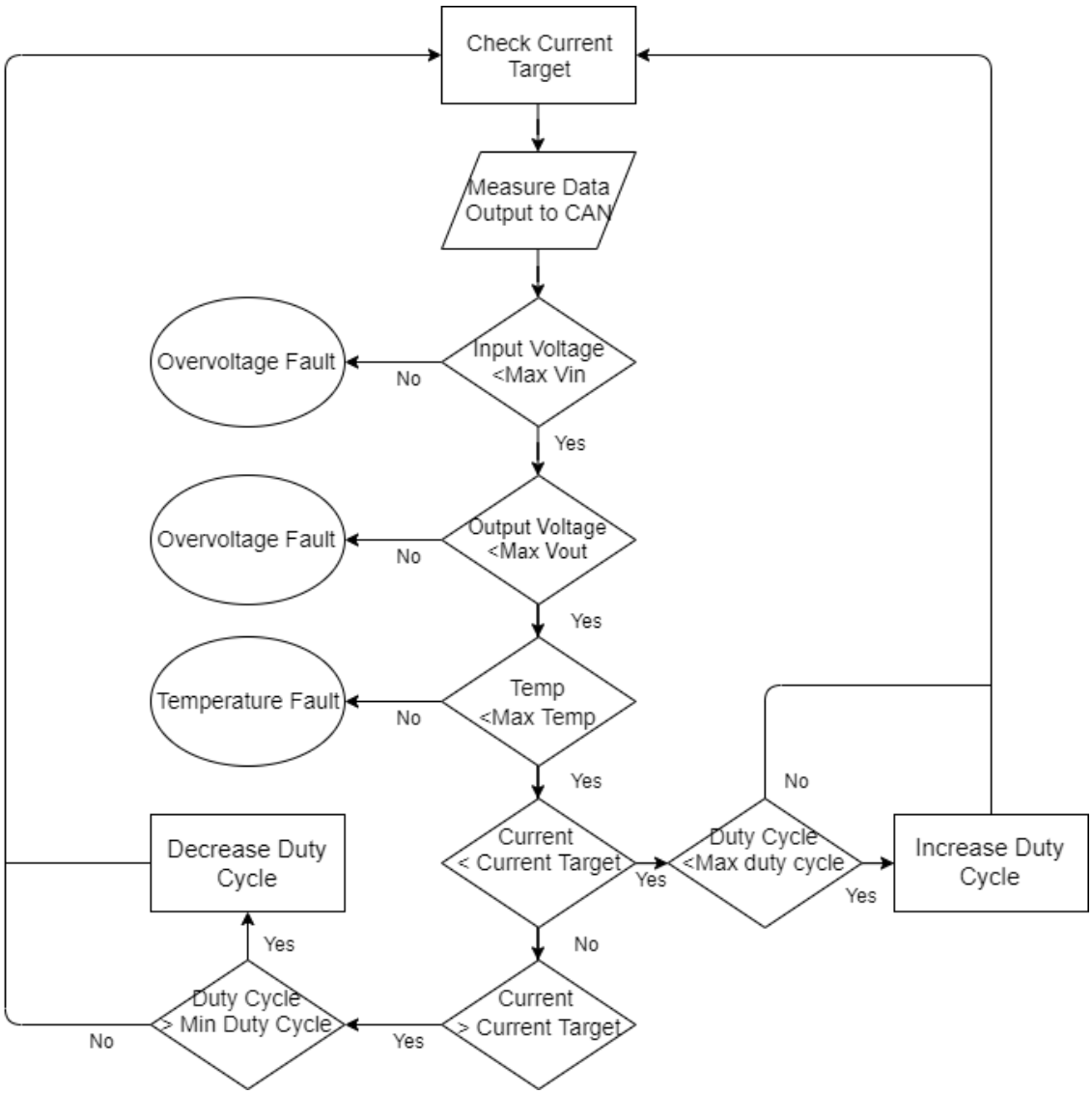
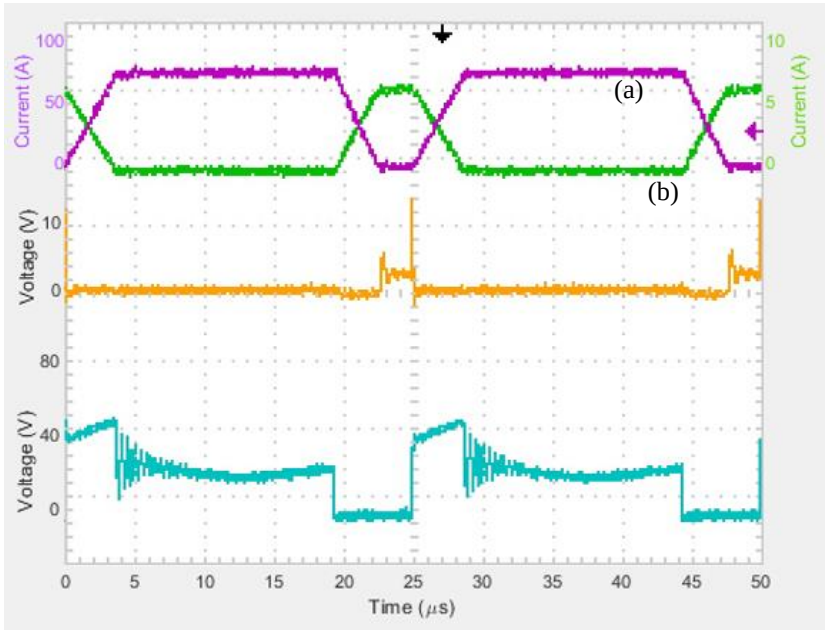


Fig. 6.7 Simplified Software Flowchart

6.3 Initial Testing

The first step was to investigate the primary over-voltage and ensure it was correctly clamped to protect the main primary switches. The over-voltage on these switches was well clamped however the ringing caused by these switches was transferring into the low voltage secondary where the ringing had the potential to cause an over-voltage across the secondary MOSFETs as shown in Fig. 6.8. With an input voltage of 50V DC, the voltage across these switches was reached 15V. So if the circuit were to run at 340V DC input it can be assumed this would cause a significant over-voltage on the 30V rated secondary MOSFETs.



(a)

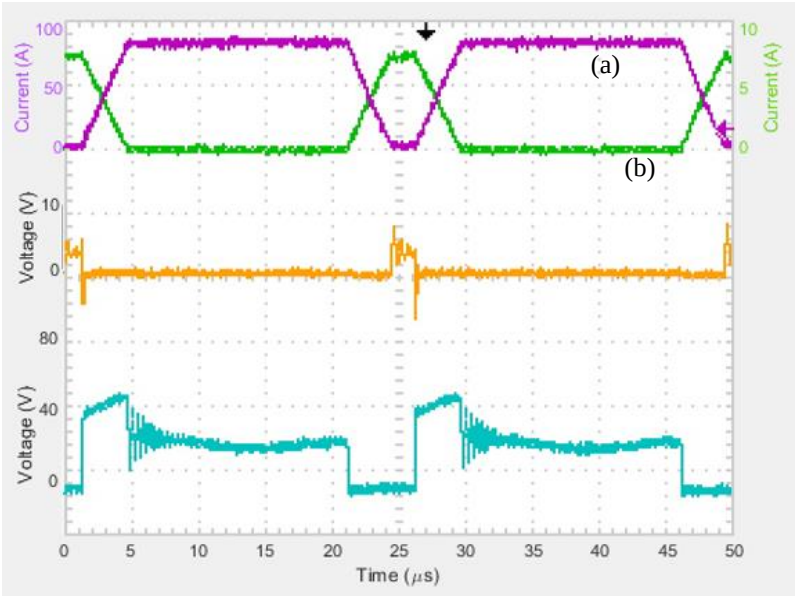
(b)

(c)

(d)

Fig. 6.8 Initial testing of Asymmetrical half-bridge flyback converter. (a) Secondary (L2) inductor current, (b) Primary (L1) inductor current, (c) Q3 Switch Voltage (Vds), (d) Q1 Switch Voltage (Vds)

Ideally if the ringing could be removed through the control this would be easier than adding aditional circuitry. Slightly delaying one of the two primary switches by half the resonance period, antiphases, hence partially cancels the induced ringing, giving the open loop results as shown in Fig. 6.9.



(a)

(b)

(c)

(d)

Fig. 6.9 Delayed primary switches reducing secondary switch voltage. (a) Secondary (L2) inductor current, (b) Primary (L1) inductor current, (c) Q3 Switch Voltage (Vds), (d) Q1 Switch Voltage (Vds)

6.3.1 Closed Loop Operation

For closed loop operation there are five feedback sensors monitored by the microcontroller, viz. input current, input voltage, output current, output voltage, and PCB temperature. Closed loop operation is based on the primary current as this is controllable, along with the PWM duty cycle, and will enable the rate of charging of the desalination cell to be controlled. The output current could also be used, however due to its large value, it is hard to accurately measure at reasonable cost and bandwidth, so the primary side current is a related and more viable control variable. The output voltage was used to measure when the target voltage was reached. The maximum output voltage was set to 1.8V and if reached, would trigger a fault in the code and turn off the converter. In future iterations this could be used to then discharge the capacitors back into the supply. The final sensor is a fault sensor, specifically the PCB temperature sensor, used to shut down the converter if overheated. Also two key values, minimum and maximum values for each of the sensors, were set and if any of these are surpassed, the converter would return a fault code which could then be used diagnose the fault and necessary remedial action.

The sample rate was 20kHz, half the switching frequency 40kHz, thus enabling enough time for the calculations to be carried out. The primary current measurement was taken at the falling edge of the primary side switches PWM control signal to ensure that even as the duty cycle is changed by the closed loop controller, the measurement appears independent of the duty cycle.

The control loop based on the primary side current used a PI controller where a current target was set by the user through the CAN interface and a maximum and minimum duty cycle as well as the integral and proportional factors were fixed through programming.

6.3.2 Maximum Power Operation - Short Circuit Tests

Initially the circuit was run with a turns ratio of 10:1 using the inductor wound for the experimental testing in Chapters 4 and 5. For the desired ratio for the higher power testing, stepping down from 340V to 1.8V or lower, a larger turns ratio was required. The cross sectional area of copper was increased to decrease the resistance.

It was found that low stray and leakage inductance were critical to minimise circuit injection noise interfering with the controller, and to reduce over voltage on the secondary devices. A smaller more compact magnetic circuit enabled operation at 300V DC input with 400A output current., as shown in the waveforms to follow. The new core, a T300-40D was a significant reduction in size. The smaller size and as such will saturate at a lower current but would allow for shorter connection to the PCB and therefore less stray and leakage which is vital to reliable circuit operation. An additional factor is the resistance was decreased as 10 secondary windings were used in parallel and the windings themselves are significantly shorter as the core area is smaller thus allowing lower resistance again.

The plots below show various different measurements taken at 300V with the output short circuited. Fig. 6.10 shows the primary and secondary currents, the voltage across Q1 and the voltage across Q3 (which can be seen to be at 29V). Unless the scope trigger is set carefully the ringing on the secondary switch is not always visible, as in Fig. 6.11 and Fig. 6.12.

Fig. 6.13 shows the delay created between the two primary switches turning off and utilising a zero-volt loop until the second switch turned off, this initially solved the issue of ringing in the secondary switch but is insufficient to prevent the high voltage ringing.

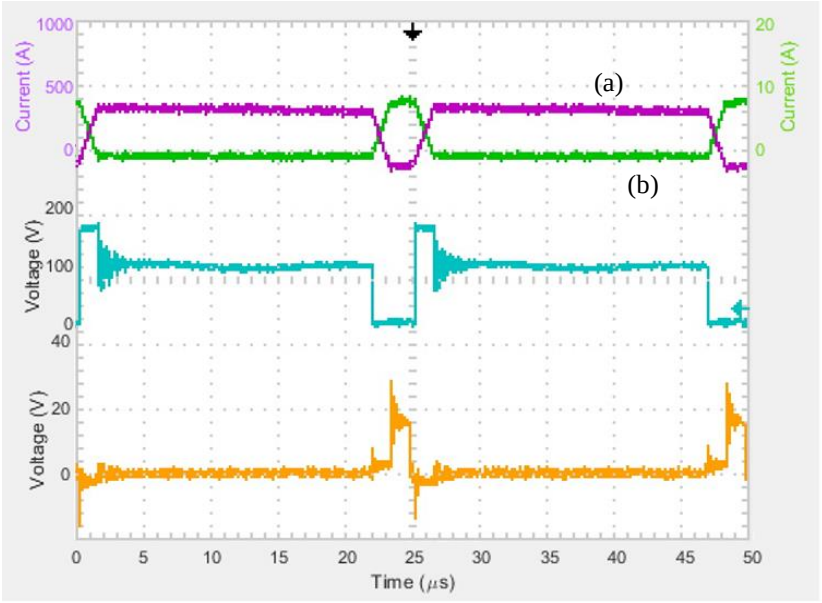


Fig. 6.10 Maximum operation with secondary switch voltage at 29V. (a) Secondary (L2) inductor current, (b) Primary (L1) inductor current, (c) Q1 Switch Voltage (Vds), (d) Q3 Switch Voltage (Vds)

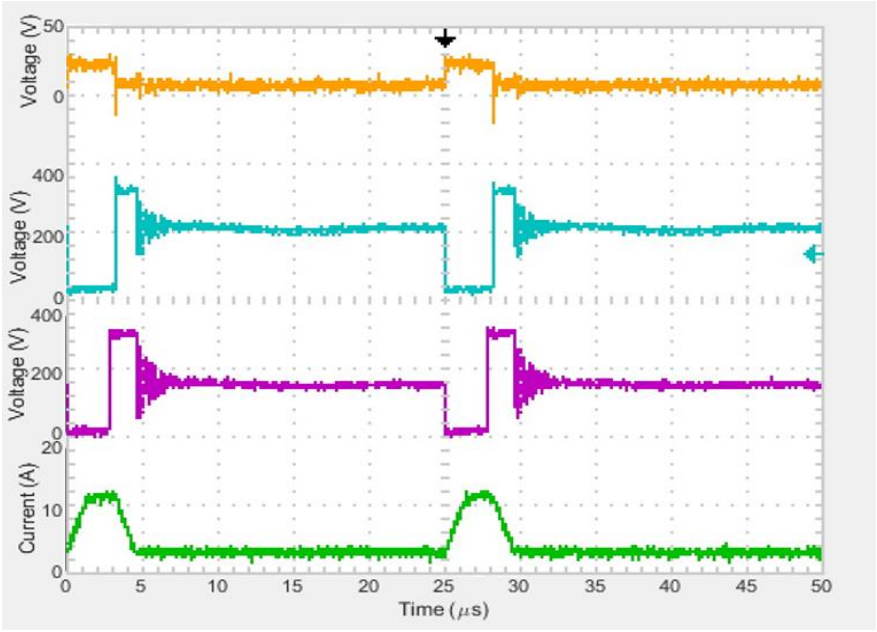


Fig. 6.11 Three switch voltages and Primary current. (a) Q3 Switch Voltage (Vds), (b) Q1 Switch Voltage (Vds), (c) Q2 Switch Voltage (Vds), (d) Primary (L1) inductor current

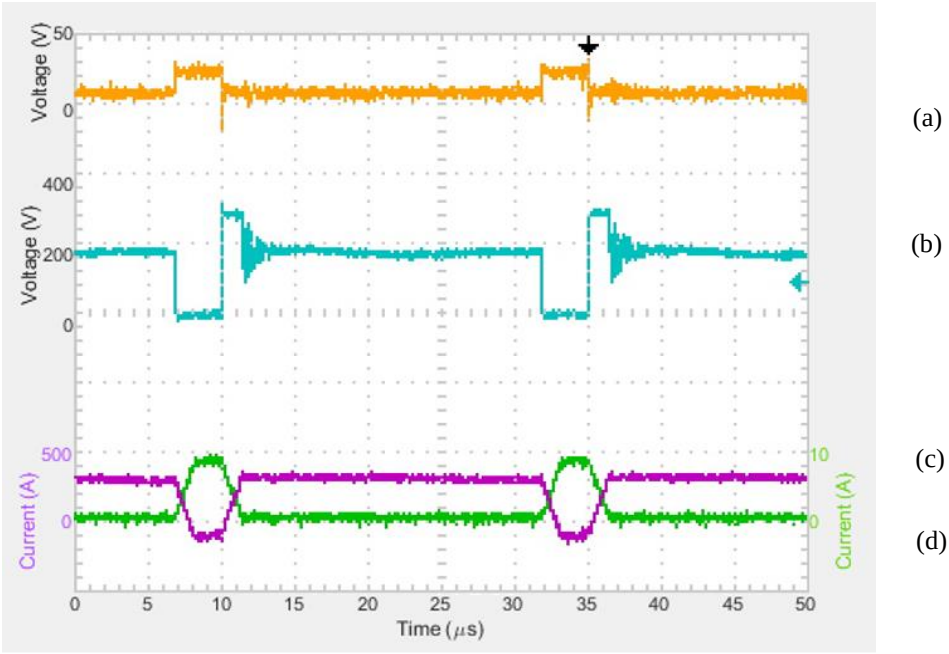


Fig. 6.12 Switch Q2 and Q3 and primary and secondary currents. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

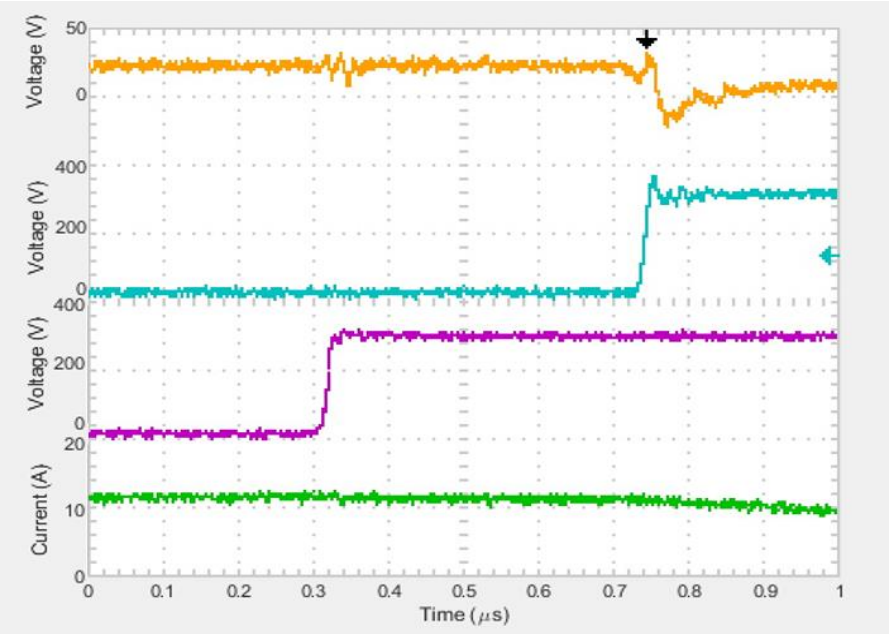


Fig. 6.13 Rising edge showing the delay of the second switch. (a) Q3 Switch Voltage (Vds), (b) Q1 Switch Voltage (Vds), (c) Q2 Switch Voltage (Vds), (d) Primary (L1) inductor current

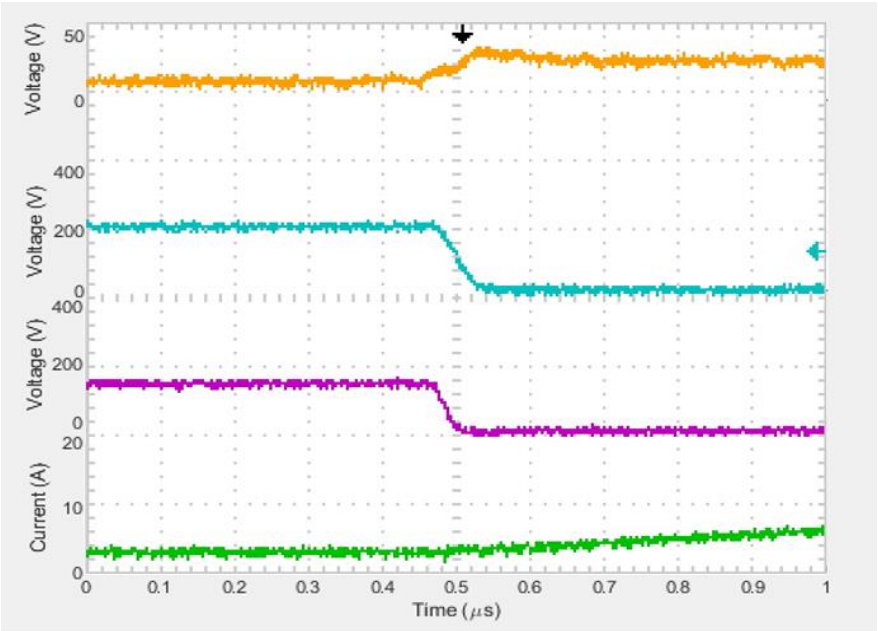


Fig. 6.14 Falling edge. (a) Q3 Switch Voltage (Vds), (b) Q1 Switch Voltage (Vds), (c) Q2 Switch Voltage (Vds), (d) Primary (L1) inductor current

6.4 Test Rigs

After the short circuit testing, for more application focused circuit testing, performance on more realistic loads was assessed.

6.4.1 Desalination Test Rig

To fully test these circuits for their water desalination application, a scaled down capacitive deionisation demonstration unit was designed and built. Suitable commercial desalination units were not available. Appendix C shows more details of the demonstration unit built. It proved that CDI was possible and the electrical characteristics, however a large enough surface area and low resistance were not possible. Alternative electrical testing loads were therefore investigated.

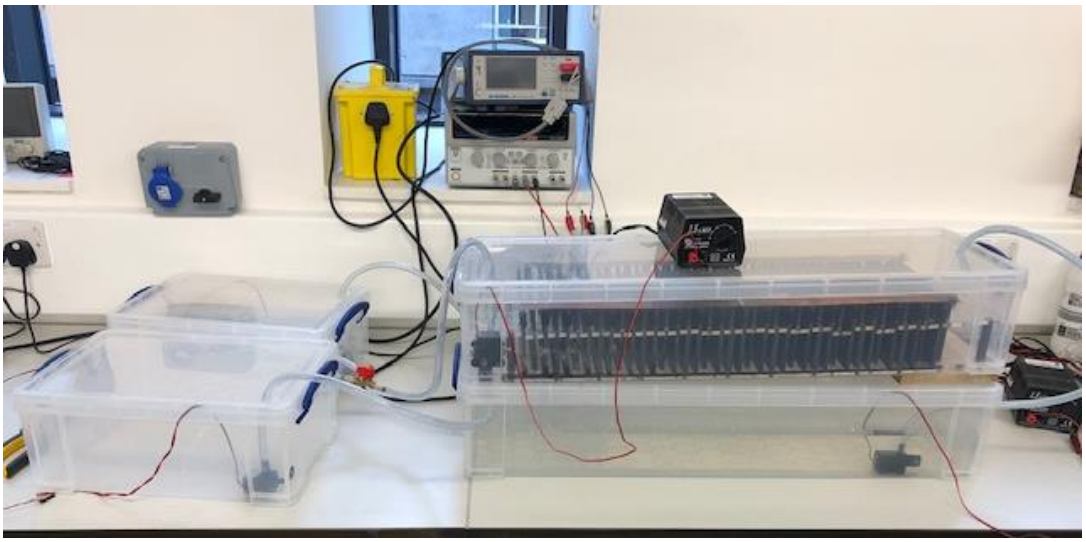


Fig. 6.15 Water desalination test rig

6.4.2 Super Capacitor Test Rig

The desalination test rig allowed for the confirmation that the process of desalination was viable and the electrical properties of such a unit, however the resistance and surface area of the unit were not a true representation of a commercial module. A desalination unit is a collection of parallel connected plates; this creates electrical properties similar to

capacitor. The larger the surface area, the larger the effective capacitance, and the more plates in parallel, the lower the resistance [20]. The high resistance of the test unit built meant that only a fraction of the desired power would be consumed by the unit at 1.8V. As an alternative super-capacitors offer a suitable likeness to a CDI unit. A bank of twenty, 850F super-capacitors were connected in parallel to represent a CDI unit with capacitance of 17kF. This unit would provide a suitable load that could take the minimum of 200A for 153s which is a long enough to obtain and measure stable circuit conditions.

For safe testing to ensure the capacitors were always discharged safely a resistor bank with resistance of 0.1Ω was connected in parallel with the capacitor bank. This resistance allows for an 18A current to flow through the bank at a voltage of 1.8V.

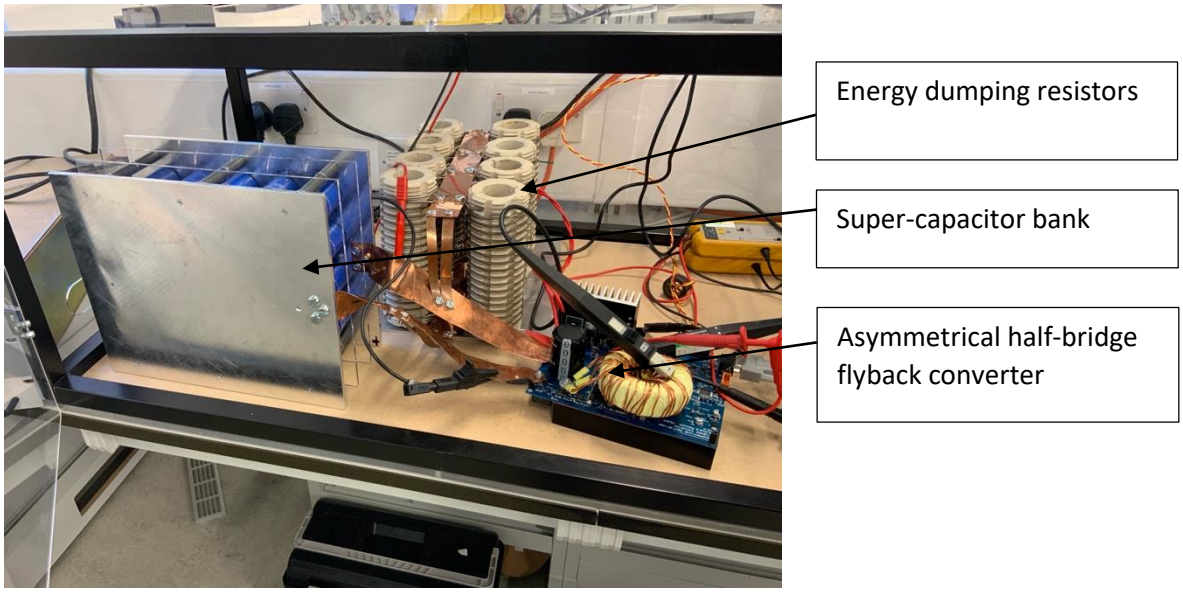


Fig. 6.16 Complete super-capacitor test setup

Although the circuit will only be operating at a maximum of 400W a 200A output current is a significant test for the circuit.

6.4.3 Super Capacitor Charging with Asymmetrical Half-Bridge Flyback Converter

The target for the test was to again run the circuit from 340V and charge the super-capacitors however with the addition of the load, the voltage across the secondary

switch was no longer 0V. The additional voltage meant that the test had to be run at 200V to ensure that the secondary switches were again within their rated voltages. The circuit was tested by charging the capacitors from 0V up to 1.8V. Waveforms were captured at the minimum output voltage, a mid point of the charging cycle, and the maximum output voltage of 1.8V. The minimum output voltage was actually 0.8V as the super-capacitors almost immediately jumped to this voltage as such a large current was flowing. At each voltage level three waveforms were captured. The turn on of the primary switches, the turn off of the primary switches and two switching cycles to show the wider operation and minimum and maximum currents. Test circuit waveforms are shown in Fig. 6.17 to Fig. 6.25.

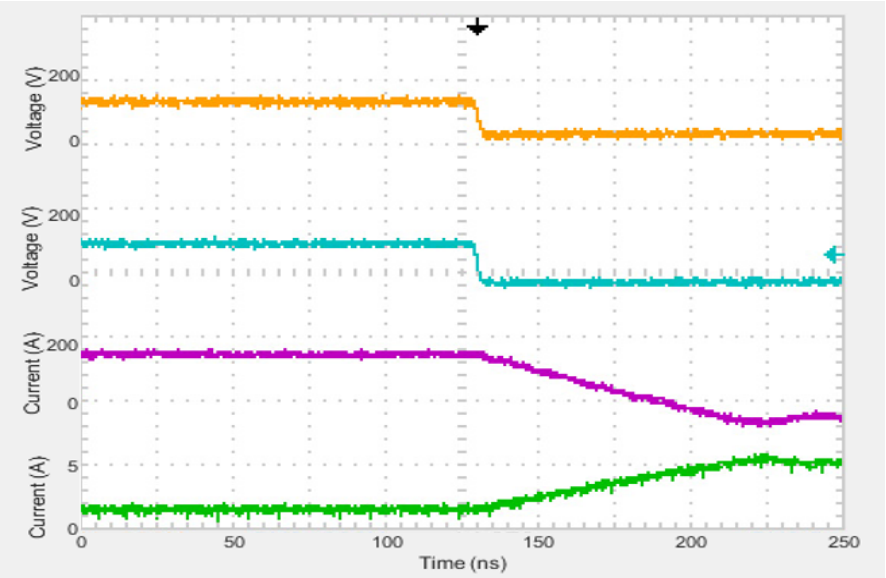


Fig. 6.17 Primary switch turn on transition 0.8V. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

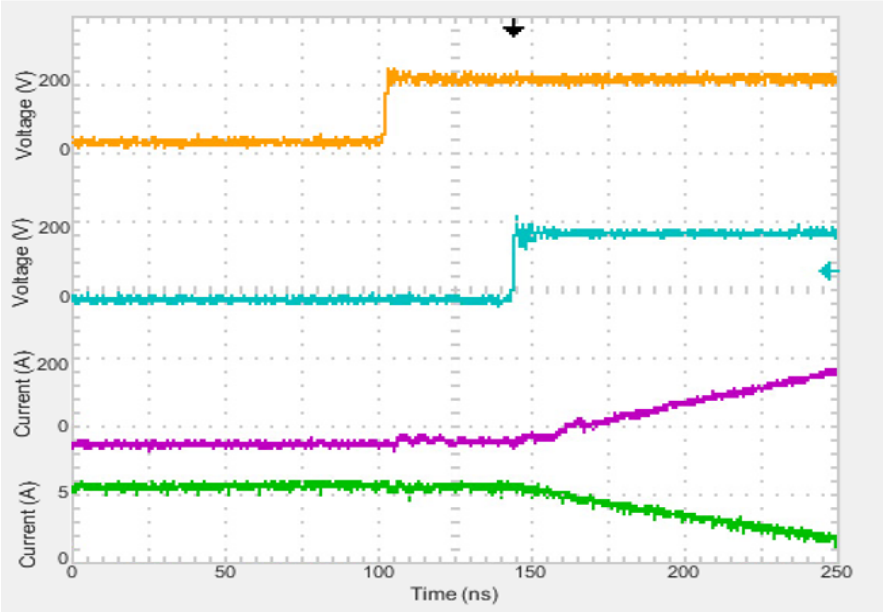


Fig. 6.18 Primary switch turn off showing delay to reduce zero volt ringing at 0.8V. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

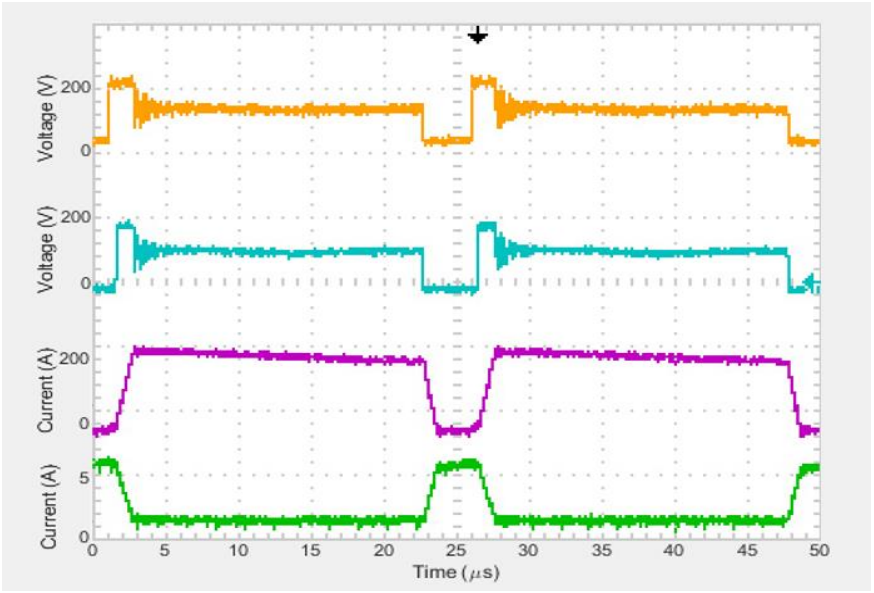


Fig. 6.19 Two full switching waveforms at minimum capacitor voltage of 0.8V. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

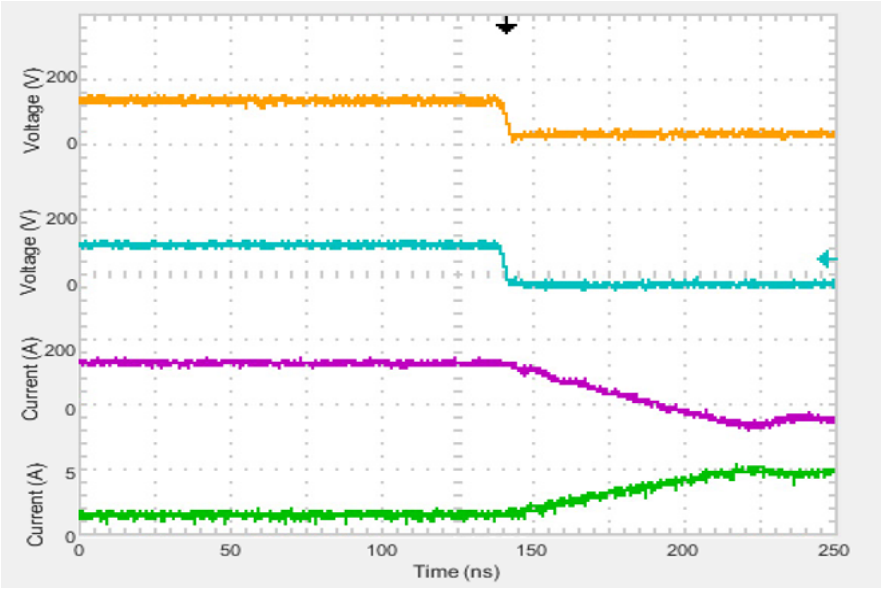


Fig. 6.20 Primary switch turn on for 1.3V super-capacitors. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

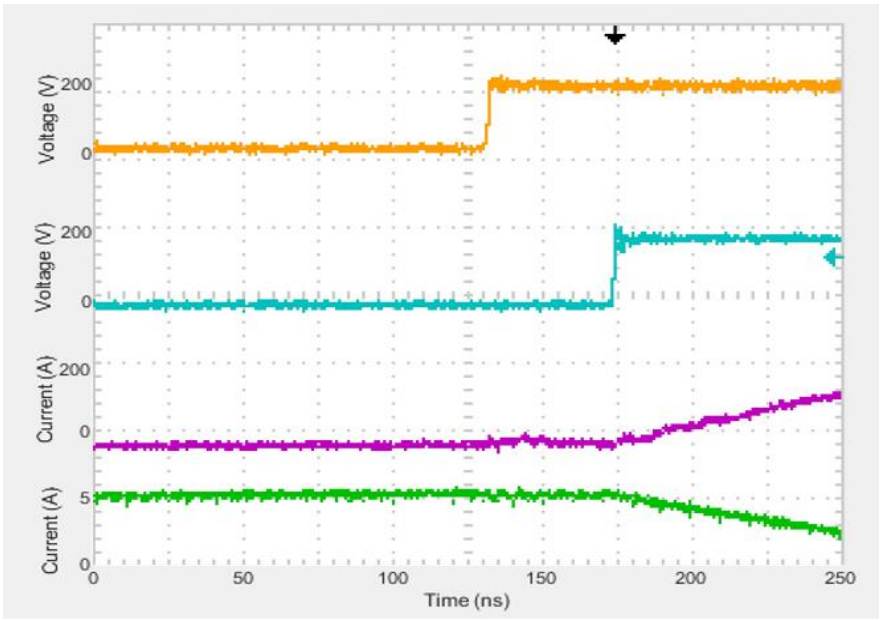


Fig. 6.21 Primary switch turn off for 1.3V super-capacitors. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

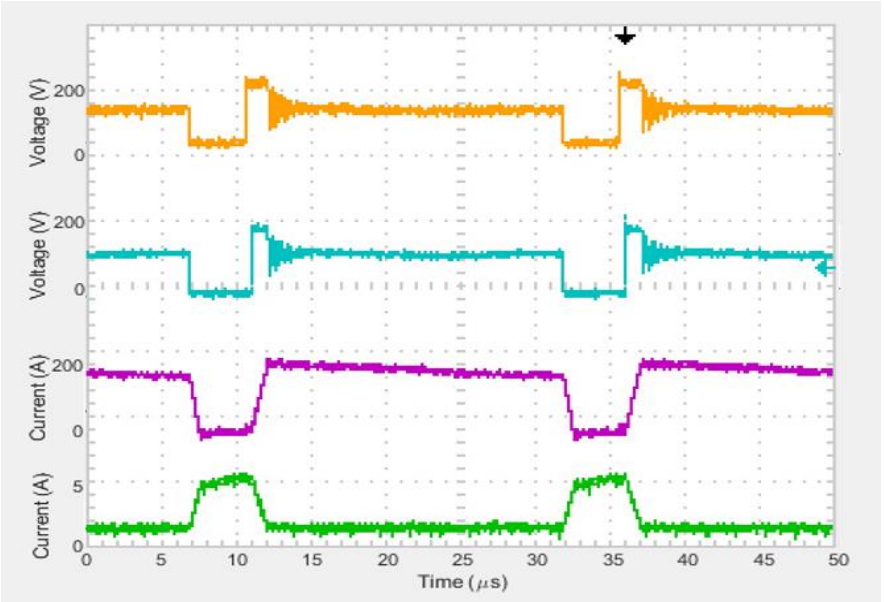


Fig. 6.22 Two full charging waveforms for 1.3V super-capacitors. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

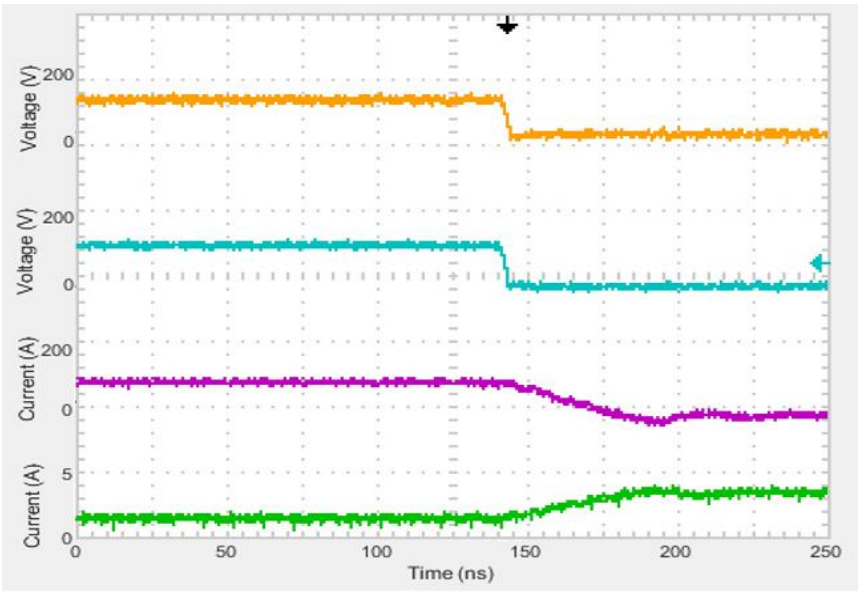


Fig. 6.23 Primary switch turn on for 1.8V super-capacitors. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

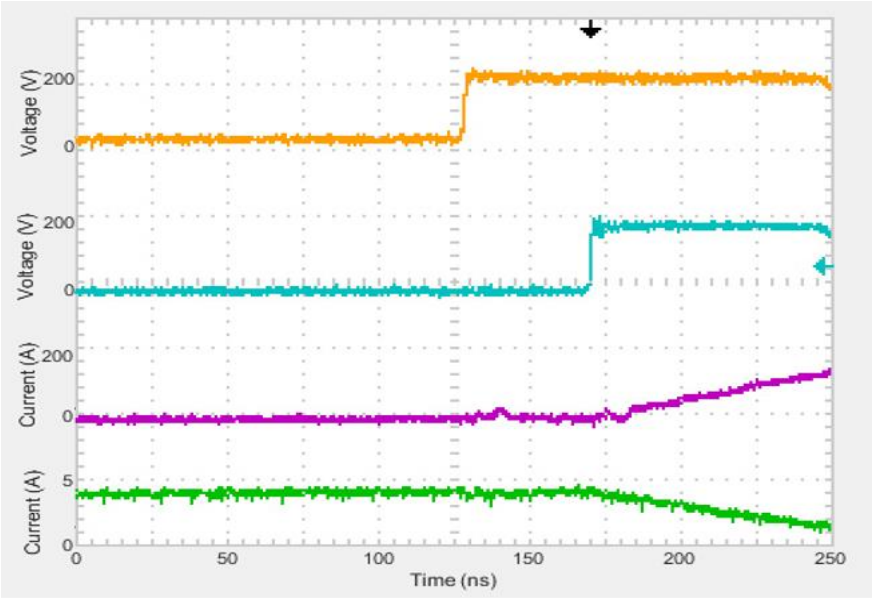


Fig. 6.24 Primary switch turn off for 1.8V super-capacitors. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

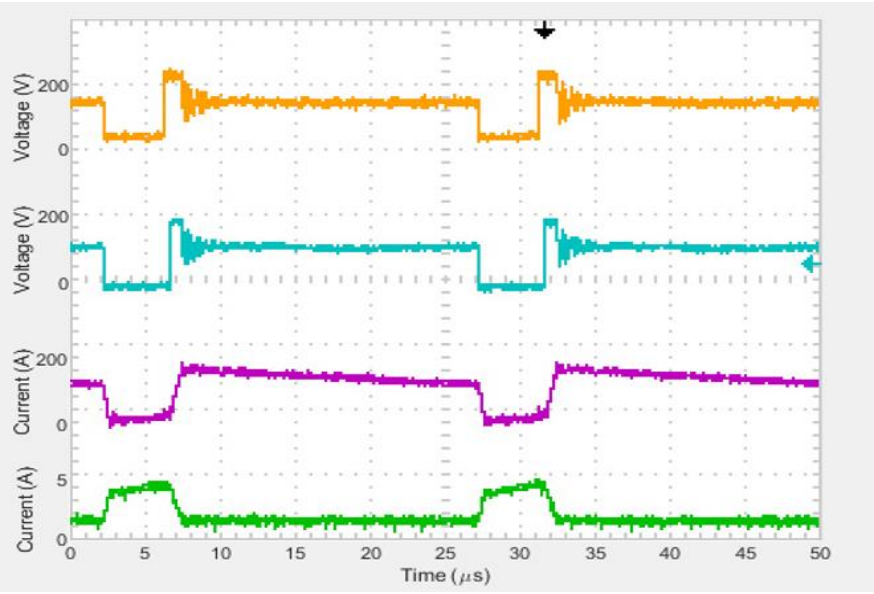


Fig. 6.25 Two full switching cycles for 1.8V super-capacitors. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

6.4.4 340V Input Voltage

To achieve a 340V DC input, the secondary MOSFETs were changed from 30V to 80V rated device to cater for over-voltages. Performance at 340V input achieved a stepped down to 1V and charged the super-capacitors up to 1.8V, that is a step-down ratio of

340:1 was achieved. The super-capacitors were initially charged with a current of 550A which due to the current control on the primary slowly decreases. This can be changed in the software if needed as the input voltage and input current are held constant as the output voltage increases, the output current must decrease. These waveforms in Fig. 6.26 show minimal ringing across the circuit components, even at the extreme 340:1 stepdown ratio.

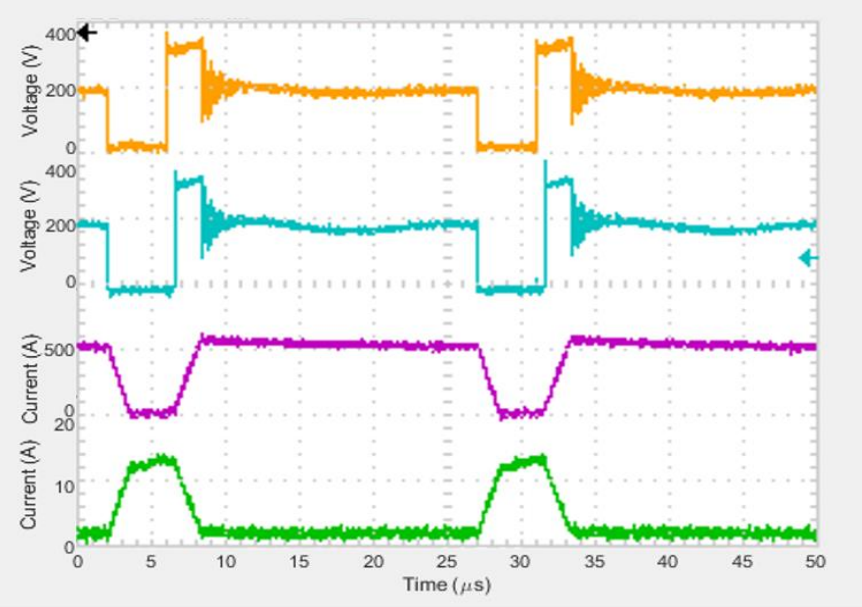


Fig. 6.26 340V input voltage with 550A output current. (a) Q1 Switch Voltage (Vds), (b) Q2 Switch Voltage (Vds), (c) Secondary (L2) inductor current, (d) Primary (L1) inductor current

The current and voltage charging trends are shown in Fig. 6.27 and Fig. 6.28 starting at over 550A and decreasing. This data was captured using the CAN connection and recording the output current. The accuracy of the scaling of the data could be questioned as at these high currents the temperature of the board can change quickly. An increase in temperature can vastly change the apparent measured current which is measured by a voltage drop. However, the values to align with the oscilloscope waveforms gathered.

The voltage similarly can be seen to increase with the increase rate slowing as would be expected for a capacitor.

These waveforms give insight into the data that the micro controller actually receives but potentially the resolution is too high for showing the more general trend.

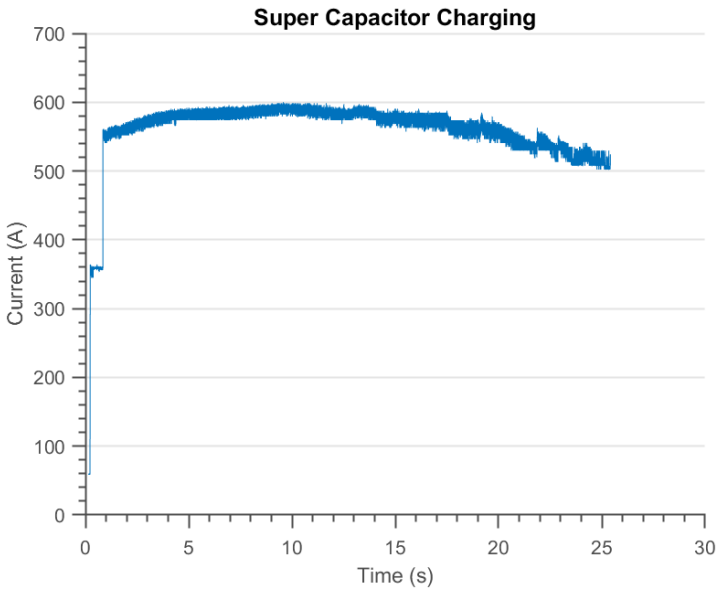


Fig. 6.27 Capacitor charging current (Approx)

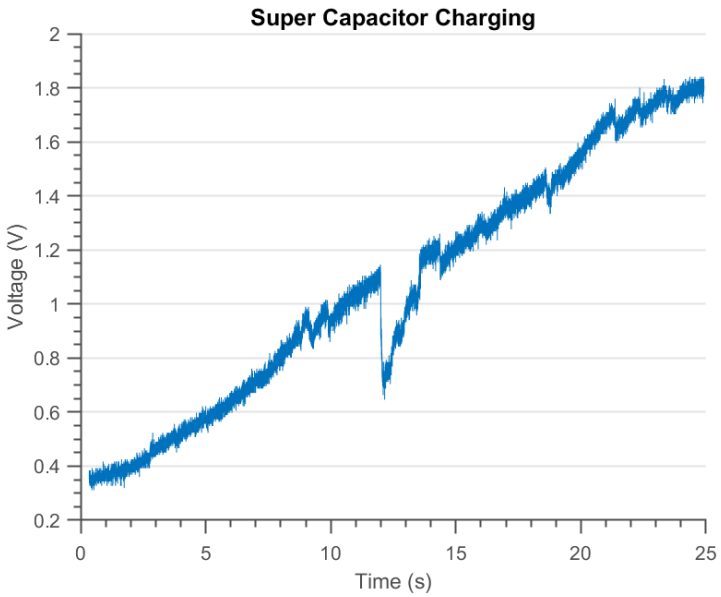


Fig. 6.28 capacitor voltage (charging) 550A

The charging profile of the super-capacitors shows a near consistent charge from 0.3V up to 1.8V. The voltage appears to fluctuate more readily at lower voltages and then settle down as the voltage increases.

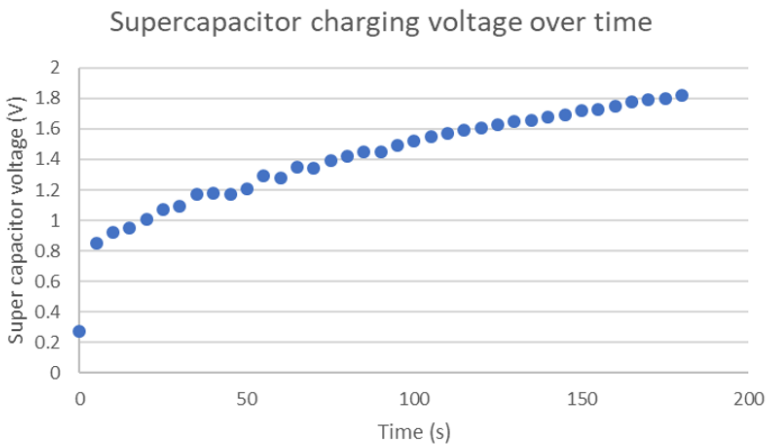


Fig. 6.29 capacitor voltage (charging) 350A

From the experimental data, the topology, control, measurement, thermal management and operation of the circuit have been established.

The flyback converter control charged super capacitors. Since the input supply was unidirectional, boost (inverse of buck) converter discharge of the super capacitors was not possible.

6.5 Summary

This chapter presented and tested the final suggested topology. The final build achieved the goal that was set out of 340V to 1.8V and achieved an output current of 550A.

This circuit offers an isolated 3 switch bidirectional converter that can step voltages from 340V to less than 1V. The converter is capable 600:1 step-down ratio, for three phase rectified applications again as long as layout of the converter was carefully considered.

The addition of silicon carbide devices in the primary side increased the efficiency but may create additional ringing, however the benefit of utilising these devices to achieve a higher switching frequency allowing for a physically smaller coupled-inductor is a significant benefit.

Table 6.3 Summary of completed testing

	Test 1	**Test 2**	**Test 3**	**Test 4**
Load	Short Circuit	Short Circuit	Super-capacitors	Super-capacitors
Input Voltage	30V	300V	200V	340V
Output current	N/A	400A	350A	550A
Q3 Device Rating	30V	30V	30V	80V
Figures	Fig. 6.8-Fig. 6.9	Fig. 6.10-Fig. 6.14	Fig. 6.17-Fig. 6.25	Fig. 6.26-Fig. 6.28
Section	Section 6.3	Section 6.3.2	Section 6.4.2	Section 6.4.4

Chapter 7 Conclusion

7.1 Summary and General Conclusions

The presented research has proposed capacitive deionisation as a method of water desalination and investigated the necessary electronics. From the background research, it was identified that deionisation required a voltage of up to 1.8V applied across the electrodes within a stream of the salt water. The actual voltage depended on the ionisation levels in the water and the build-up of the salt ions on the electrodes. Initially a fresh set of electrodes within a high concentration of salt ions required a low potential difference across the electrodes. As deionisation progressed, the salt ions built up on the surface of the electrodes and the potential difference must increase in a similar way to a capacitor charging, hence the term capacitive deionisation. It was established that the potential difference across the electrodes should not exceed 1.8V in order to avoid hydrogeniseation (the unwanted formation of hydrochloric acid and sodium hydroxide). To have a significant impact on the supply of fresh water, a capacitive deionisation cell operating at a power level of approximately 1kW would take 1 hour to desalinate $1m^3$ of brackish water, equating to energy of 1kWhr. Delivering this power level into a pair of low voltage electrodes requires a large current. At 1.8V this would be 555A but earlier in the process the current would need to be higher. At an output voltage of 1V the current would need to be 1000A to achieve 1kW into the electrodes. The technical challenge, forming the design focus for this research, was therefore the design of a DC/DC converter operating from an input voltage of 340V DC (rectified voltage from 230V ac) which delivers 1 kW at output voltages less than 1.8V. This required a DC/DC converter with a step down ratio of 200:1 (at 1.8V) and output current between 500 and 1000A.

Additionally, the converter used for capacitive deionisation should be reversible since the electrodes can be ‘cleaned’ by reversing the current direction and extracting the energy stored in the charged ions as they are washed away into already salted discharge water. The research therefore focussed on the selection of power supply topologies which could offer large step down ratios of up to 340:1 (at 1V) and be reversible in operation.

Achieving such a large DC:DC step down ratio is challenging, but such a circuit would have a many applications. These applications would have varying desired step-down ratios. For example, LED lighting is often powered from single phase AC supplies and depending on the number of LEDs would require output voltages as low as a few volts.

Electric vehicles are becoming increasingly prominent. To enable faster charging and higher power within vehicles, the voltage chosen for the main DC battery is increasing. Many manufactures are considering 800V (Formula E) as an achievable target voltage. However, this increasing DC bus voltage creates a problem for the vehicle low voltage 12V battery distribution system. A reversible converter that could achieve a step down ratio of 800:12 would have commercial use.

7.1.1 Existing literature

Numerous converters were surveyed from the literature in Chapter 2, with three highlighted for investigated in subsequent chapters.

(1) The buck converter seen as the main converter for non-isolated step down voltages but conventionally is not used above a step down ratio of 10:1. For a larger step down ratio, stacking multiple buck converters in series should be considered, giving a step down ratio of up to 100:1. However there is a large number of modular parts and additional switching losses in a multiple stage converter.

(2) The coupled-inductor buck converter was introduced as an alternative, and is similar to a buck converter with the addition of a tapped or coupled inductor. This converter offers the ability to have a turns ratio associated with the construction of the coupled inductor. The tap turns ratio provides an additional factor besides the duty cycle, thereby creating an increased step down ratio. This coupled-inductor buck converter topology allows for a variable step down ratio for any large step down ratio application.

(3) The final converter topology investigated was the flyback converter. The flyback converter is the isolated version of the buck-boost converter. With the

addition of the turns ratio in the transfer function, the flyback converter is closely aligned with the coupled-inductor buck converter at large turns ratios.

The flyback converter is an alternative to the coupled-inductor buck converter for applications where isolation is required. Chapter 3 analysed these two converters in detail and showed the coupled-inductor buck converter is more efficient at smaller step down ratios, where isolation is not required.

The major drawback of the coupled-inductor and flyback topologies is over-voltages created by the leakage inductance of the coupled-inductor. This leakage inductance increases with turns ratio, with the effects requiring mitigation.

The first method is in the construction of the inductors: with careful printed circuit board layout and winding of the inductors, the leakage inductance can be reduced. However, this is still not sufficient in most cases and switch/diode protection circuits are required.

Passive switch protection methods were investigated (Chapter 2). These are additional circuits to protect the switches and they use no additional active switches so ideally only diodes, capacitors, inductors and resistors are employed. Whilst these circuits are simple to implement they offer limited flexibility to varying loads and are inefficient as the leakage energy is dissipated after each switching operation. By simulating various circuits, it was assessed desirable that the circuits act as a clamp and thus only be active above a set voltage. This then meant that the snubber losses were less, since they do not discharge to 0V and recharge from 0V each switching cycle.

Switch protection circuitry employing additional active switches were investigated in Chapter 4. The addition of an active switch allows for greater control and increased efficiency. The additional switch can be used in a variety of ways. One method discussed has the input to a buck-boost converter connected to the node above the switch. If the voltage at this node rises above the duty cycle multiplied by the input voltage, then current will begin to flow. For example, for a 600V dc input and 50% duty cycle, this would set the clamping voltage to 1200V. This would create adequate switch protection whilst being efficient and not affect operation of the circuit below 1200V across the main switch. The circuits discussed in Chapter 4 are effective but typically require that the extra active switch be rated at the full current and full voltage. It was therefore appropriate to consider

DC/DC converters in which two converter switches be utilised in an asymmetrical half bridge.

The asymmetrical half-bridge coupled-inductor buck converter uses two switches but offers switch clamping with complex additional control. The circuit facilitates that the switches and diodes are clamped to the input voltage. This allows for lower rated devices, which are cheaper and offer greater efficiency. This asymmetrical half bridge coupled-inductor buck converter circuit is novel and was presented in Chapter 5.

The asymmetrical half-bridge coupled-inductor buck converter was tested and compared to the buck clamp snubber. The efficiency of the asymmetrical half-bridge was better than that of the buck clamp snubber. With simpler control and lower rated devices, it was found that the half-bridge is the best way to deal with the leakage energy.

7.1.2 Experimental Assessment

Chapter 6 described the application testing of the circuits developed for desalination water. The construction of a small scale test tank for desalination was described. For this application and for such a large step down ratio, isolation is a must, and although the most of the research was based around the coupled-inductor buck converter, the flyback converter offers the isolation required and as Chapter 3 showed is similar to the coupled-inductor buck converter at large step down ratios. The coupled-inductor buck converter remains the preferred option for applications where isolation is not required.

The asymmetrical half-bridge flyback converter was tested charging a 17,000 F bank of super-capacitors, as this is a similar loading requirement to a commercial capacitive deionisation unit. Test results were for delivering hundreds of amps and fully charging the capacitor bank up to the 1.8V required. An input voltage of 340V was used while delivering controllable output voltages of 0 to 1.8V, confirming that a step down ratio of 340:1 was achievable with a single switching stage. The circuit was tested with short circuit load and used to charge the capacitor bank from 0V. The final prototype used SiC MOSFETs and diodes on the input side allowing a high switching frequency of 40kHz whilst minimising switching losses. SiC devices switch faster than traditional silicon components; such faster switching speeds result in ringing readily transmitting

throughout the circuit. SiC devices however, allowed for switching frequencies of 40kHz to be readily achieved which allowed for a compact coupled-inductor design. Investigating methods to limit EMI produced by SiC devices would be worthwhile as the benefit they offer makes them ideal in this application, if the large *di/dt* can be controlled.

The topology achieved a 340:1 step down ratio and with further coupled inductor redesigns could reach the 600:1, for 3 phase rectified voltage sources.

This research has shown such large step down ratios are viable, although some additional design requirements should be considered.

Large step-down ratio converters have an increasing number of applications and this research established that there are various options as to how to achieve this. Step down ratios of 600:1 are achievable and show promise to solve problems across various areas of power electronics.

7.2 Author's Contribution

An outline of the novel research conducted is as follows:

Chapter 2 - comparison of multiple coupled-inductor topologies to find the converter best suited for a large step down ratio

Chapter 3 - comparison of a flyback converter, a coupled-inductor buck converter, and a buck converter.

Chapter 4 - a comparison of a novel regenerative snubber and a buck-clamp snubber with modified capacitor placement allowing for capacitor derating.

Chapter 5 - the design and testing of a novel asymmetrical half-bridge coupled-inductor buck converter.

Chapter 6 - fabrication of a desalination test rig. Super capacitor charging from input voltage 340V to an output of 1.8V in a single switching stage at over 550A output. Over 1kW for a 340:1 step down ratio.

Appendix D - published papers from this body of research

7.3 Future Research

- The coupled inductor construction, which has leakage inductance could be improved, using the PCB as the secondary, could improve circuit performance. Higher voltage 80V switches were used on the secondary and the circuit operated without issue. Another method to tackle the over-voltage problem would be to use a snubber or switch protection on the low voltage secondary switches. Due to the high current, this snubber would be costly in terms of physical size and monetary cost. The addition of a snubber on this switch would be more expensive and complex, whilst rating the secondary to a higher voltage would be an easy solution, if clamping is required.
- Future research would entail testing the converter on a commercial desalination unit.
- Refining the bidirectional nature of the converter and doing tests on the control required for the flushing stage of the desalination unit.
- Achieving 550A was the step towards 1000A by extending the presented design.
- Possible publications on the final results and the high current nature and successful step down ratio of 340V to 1V.
- Investigation into additional uses of the converter for charging and discharging of super capacitors for grid smoothing or high current battery applications where super capacitors are used in parallel.

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Appendix A PCB Control Software

The three core functions within the converter code are shown below. The converter initialisation, the main current control loop (as such the main converter control) and the converter fault cases for over current voltage and temperature.

Converter Initialisation

```
static void Start_Inverter (void)
{
        PDC1=period_sw;
        PDC2=period_sw;
        PDC3=period_sw;

//Initial PWM set to the constant period_sw, this allows the converter to start correctly with no input from the user
        IOCON1bits.OVRENH=0;
        IOCON2bits.OVRENH=0;
        IOCON3bits.OVRENH=0;

        current_target_600_sw=550;
        pwmvalue_delay_sw=50;

//Initial current target set to 550, this again ensures safe operation with no input from the user
//PWM delay is the value that the two primary switches are delayed by to reduce the ringing

}
```

Current Control Loop

```
void Control_Current_600V(void)
{
	current_value_sw=current_measure_600V_sw;

	CURRENT_PROP_GAIN_sw = 2;
	CURRENT_INT_GAIN_sw=5;

// The proportional and integral gain are set as to determine the converters response to a changing current

	current_pwm_max_sw =900;
	current_pwm_min_sw = 450;

// Maximum and minimum duty cycles are set to ensure the converter stays within operational limits

	current_error_sw = current_target_600_sw - current_value_sw;

// The current error is used to calculate how far away the current is from the desired current

	loc_result1_slw = ((signed long)current_pwm_max_sw);
	loc_result2_slw = (loc_result1_slw)<<CURRENT_INT_GAIN_sw;
	loc_result3_slw = ((signed long)current_pwm_min_sw);
	loc_result4_slw = (loc_result3_slw)<<CURRENT_INT_GAIN_sw;

	current_integral_slw = current_integral_slw + (signed long)current_error_sw;

	if ((current_integral_slw > loc_result2_slw)){
		current_integral_slw = loc_result2_slw;
	}

	if ((current_integral_slw < loc_result4_slw)){
		current_integral_slw = loc_result4_slw;
	}
// The integral gain is capped at the values stored in loc_result2 and 4

	loc_result5_slw = ((current_integral_slw>>CURRENT_INT_GAIN_sw)
		+(((signed long)CURRENT_PROP_GAIN_sw *(signed long)current_error_sw)>>2));

// Implementing the integral and proportional gain to calculate the response

	if (loc_result5_slw > 0x7FFF){
		loc_result5_slw = 0x7FFF;
	}
// Ensuring the resultant does not overflow and create an error
	pwmvalue_primary_sw = (signed int)loc_result5_slw;

	if (pwmvalue_primary_sw > current_pwm_max_sw){
		pwmvalue_primary_sw = current_pwm_max_sw;
	}

	else if (pwmvalue_primary_sw < current_pwm_min_sw){
		pwmvalue_primary_sw = current_pwm_min_sw;
	}
// Assigning the new PWM value whilst ensuring it is within the minimum and maximum values set
}
```

Voltage, Current and Temperature Fault Function

```
static void OverCurrent_OverVoltage_OverTemperature(void)
{
	if (current_measure_600V_sw>max_current_600V_sw || current_measure_600V_sw<0){
		fault_code_sw=0xFA;
		fault_value_sw=current_measure_600V_sw;
		inverter_run_sw=0x0F;
	}
// If the primary current measured exceeds the maximum or the minimum values return a fault code to the user and turn off the converter.


	else if (current_measure_1V_sw>max_current_1V_sw || current_measure_1V_sw <0){
		fault_value_sw=current_measure_1V_sw;
		fault_code_sw=0xFB;
		inverter_run_sw=0x0F;
	}
// If the output current measured exceeds the maximum or the minimum values return a fault code to the user and turn off the converter.

	else if (vdc_measured_600V_sw>max_vdc_600V_sw || vdc_measured_600V_sw <0){
		fault_value_sw=vdc_measured_600V_sw;
		fault_code_sw=0xFC;
		inverter_run_sw=0x0F;
	}
// If the input voltage measured exceeds the maximum or the minimum values return a fault code to the user and turn off the converter.

	else if (vdc_measured_1V_sw>max_vdc_1V_sw || vdc_measured_1V_sw <0){
		fault_value_sw=vdc_measured_1V_sw;
		fault_code_sw=0xFD;
		inverter_run_sw=0x0F;
	}
// If the output voltage measured exceeds the maximum or the minimum values return a fault code to the user and turn off the converter. This was also used to detect when the super-capacitors were charged to 1.8V.

	if (pcb_av_sw>max_pcb_temp_sw){
		fault_value_sw=pcb_av_sw;
		fault_code_sw=0xF8;
		inverter_run_sw=0x0F;
	}
// If the temperature measured exceeds the maximum or the minimum values return a fault code to the user and turn off the converter. This protects the converter from damage quicker than the user could react.

}
```

Appendix B Desalination Cell Design

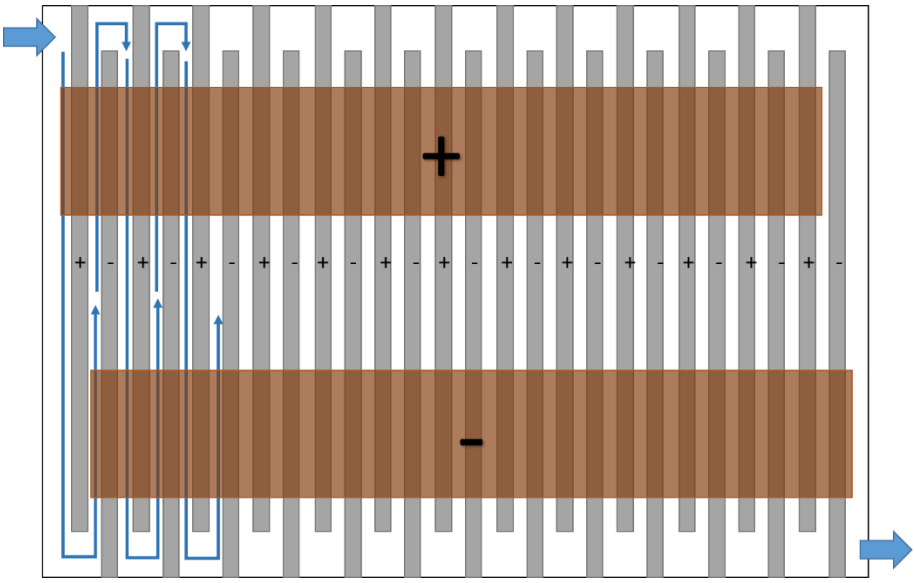

Fig. i Top down view of desalination test rig

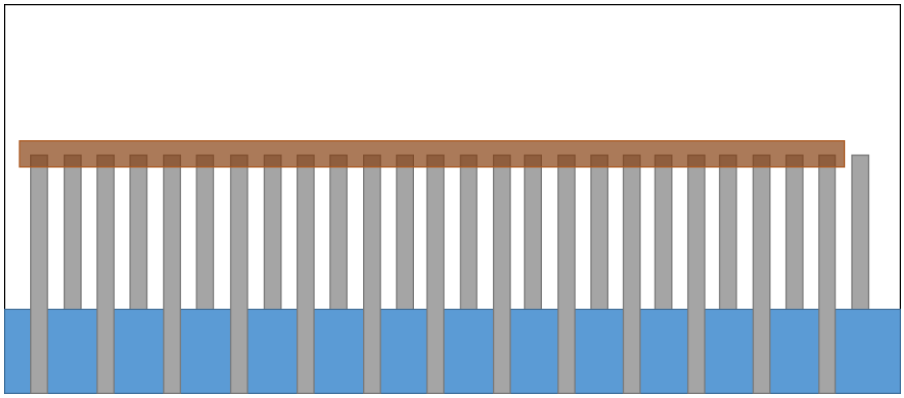

Fig. ii side view of desalination test rig

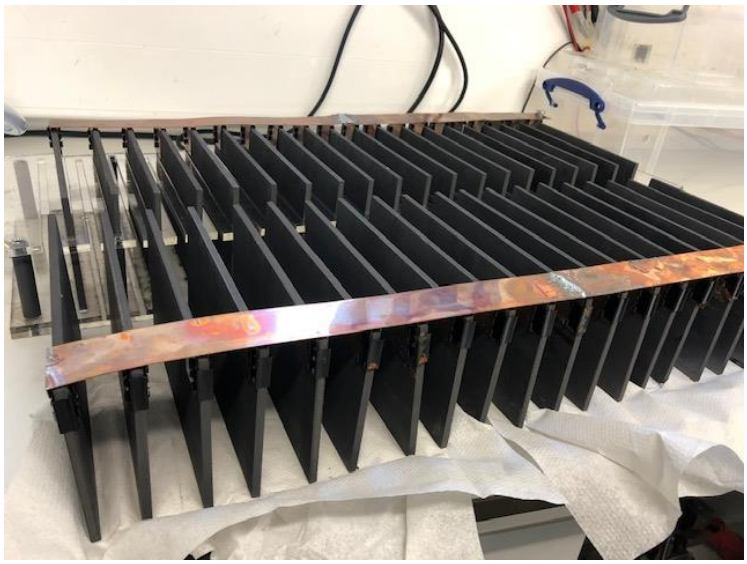

Fig. iii Construction of desalination test rig

Fig. iv Assembled desalination cell desalination test tank

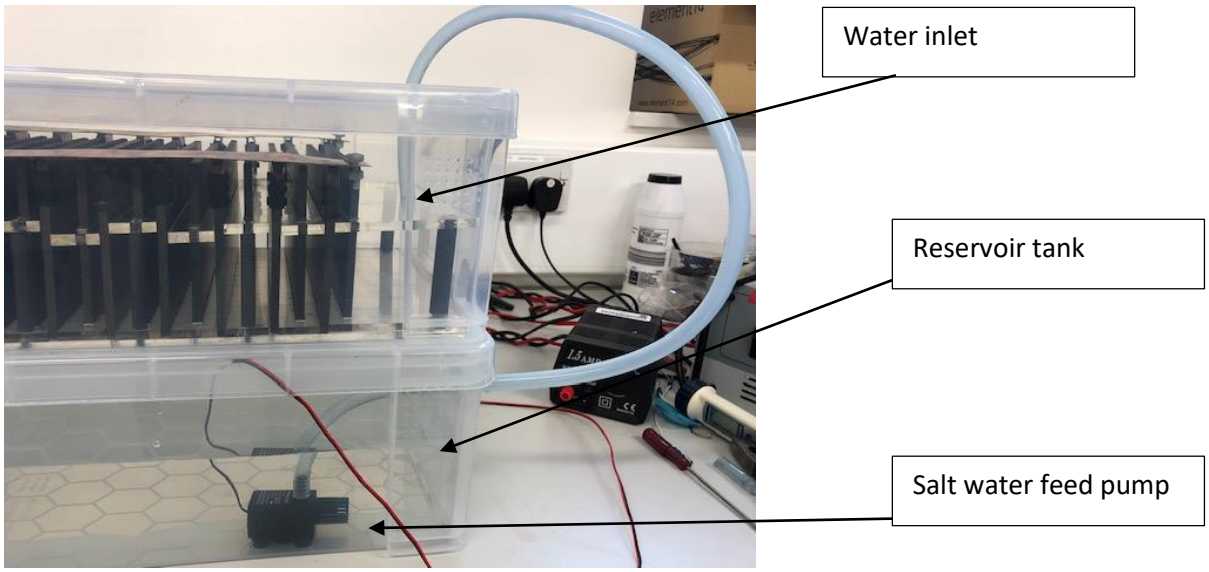

Fig. v Use of water pumps within the test rig

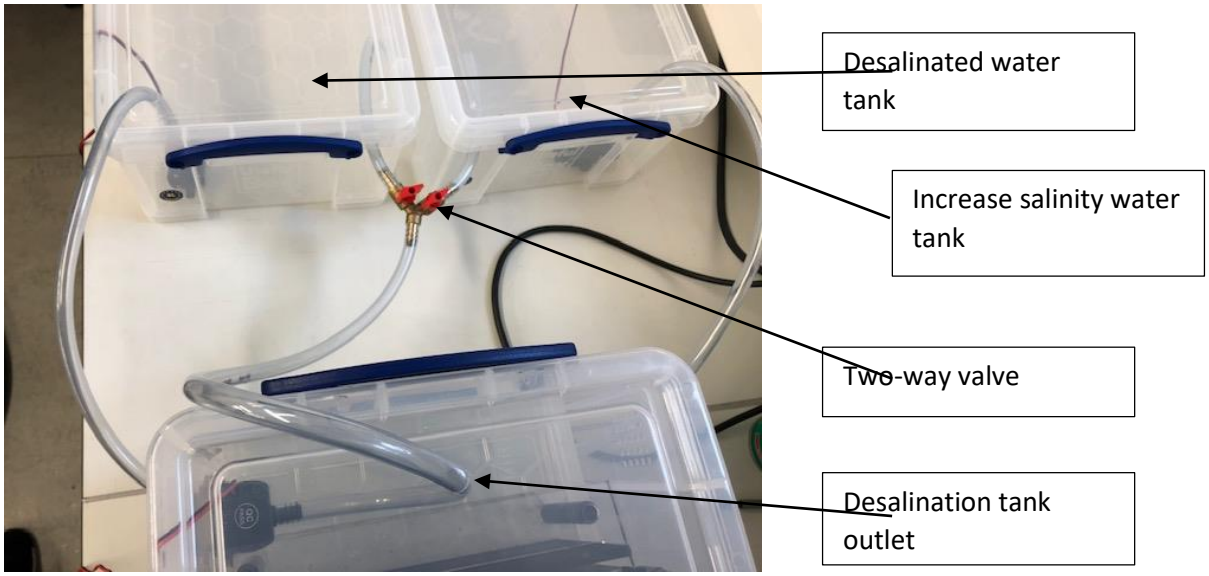

Fig. vi Tubing to determine the path of the flow at the output of the cell.

Appendix C List of Figures and Tables

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Appendix D List of Author's Publications

Conference Papers

R. C. Pollock, N. McNeill, D. Holliday, and B. W. Williams, "DC-DC converter with a high step-down ratio for water desalination applications," in *IET PEMD Power Electronics Machines & Drives, Liverpool*, UK, 2018.

Journal Papers

R. C. Pollock, N. McNeill, D. Holliday, and B. W. Williams, "DC–DC converter with a high step-down ratio for water desalination applications," *J. Eng.*, vol. 2019, no. 17, pp. 4545–4549, 2019.

R. Pollock, "Voltage Clamping Circuits for Large Voltage Step-Down Coupled Inductor Converters," *Renew. Energy Sustain. Dev.*, vol. 5, no. 1, pp. 23–32, 2019.