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NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF PHYSICS

PEDRO CARVALHO RODRIGUES
Bachelor of Science in Biomedical Engineering

FABRICATION OF FLEXIBLE HYBRID CIRCUITS IN PARYLENE

MASTER IN BIOMEDICAL ENGINEERING

NOVA University Lisbon
September, 2022

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Para a minha família.

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" Happiness can be found even in the darkest of times, if one only remembers to turn on the light "
(Albus Dumbledore)

Abstract

In recent years, with the increasing research interest in personalized medicine, new and disruptive technologies such as the Internet of Things (IoT) and flexible wearable electronics have emerged and have become trending topics in the scientific community. Despite consistent progress in the area of fully flexible electronics, these continue to reveal some restrictions, which can be overcome by traditional silicon integrated circuits (ICs). The combination between these technologies generated the new concept of flexible hybrid electronics (FHE) igniting a new generation of wearable health monitoring systems.

This thesis reports a new way to the use parylene C as substrate, dielectric and encapsulation layers to accommodate silicon ICs, surface mounted devices (SMDs) and thin metal layers, in order to create flexible and conformable double layered hybrid sensing membranes for body temperature monitoring, one of the most relevant physiological parameters upon a medical diagnosis, since it's among the main indicators for inflammation and infection. To achieve the thin metal and parylene C layers, thin-film microfabrication techniques were employed and corroborated by superficial, electrical and structural characterization techniques. In addition the establishment of an electrical connection by the integration of silicon ICs and SMDs onto the thin metal layer was successfully tested using a low-temperature solder paste and a reflow oven, which reproduced a previously inputted time-temperature profile. Furthermore, this thesis analyses the repercussions of this integration procedure on the peel off process.

Throughout this work, commercial body temperature measuring circuits were used as inspiration for the temperature sensing circuits developed. The interface between the produced membranes and their respective microcontrollers was also tested, although no temperature measurements were obtained due to parylene's performance as a dielectric.

The successful production of a fully functional flexible and conformable double layered hybrid sensing membrane could propel the adaptation of other rigid health monitoring electronics to FHE membranes, further engraving this technology into people's daily lives.

Keywords: Flexible Hybrid Electronics, Double Layer, Parylene C, Silicon Integrated Circuit, Temperature Sensing

Resumo

Com o crescente interesse na pesquisa em medicina personalizada, novas tecnologias como a *Internet of Things (IoT)* e a eletrónica flexível, surgiram e tornaram-se tópicos de tendência na comunidade científica. Apesar dos progressos na área da eletrónica totalmente flexível, continuam a existir algumas restrições, que podem ser superadas pelos circuitos integrados de silício *(ICs)* tradicionais. A junção entre estas tecnologias gerou um novo conceito de eletrónica híbrida flexível *(FHE)* dando início a uma nova geração de sistemas de monitorização de saúde.

Esta tese aborda uma forma inovadora de usar parileno C como substrato, dielétrico e camada de encapsulamento para acomodar *ICs* de silício, *surface mounted devices (SMDs)* e camadas metálicas finas, a fim de criar circuitos em membranas híbridas de dupla camada flexíveis e conformáveis para monitorização da temperatura corporal, um dos parâmetros fisiológicos com maior relevância aquando do diagnóstico, uma vez que é um dos principais indicadores de infeções e inflamações. Para obter as camadas finas de metal e parileno C, foram empregues técnicas de microfabricação de filmes finos, corroboradas por caracterizações superficiais, elétricas e estruturais. Utilizando uma pasta de solda de baixa temperatura e um forno de refluxo, reproduzindo um perfil de tempo-temperatura, foi desenvolvido um protocolo para a conexão e integração de *ICs* na fina camada de metal. São ainda apresentados resultados relativos às implicações deste processo no método do *peel off*.

Os circuitos desenvolvidos durante esta tese tiveram por base circuitos comerciais que medem a temperamtura corporal. Apesar da interface entre as membranas produzidas e os seus respetivos microcontroladores ter sido testada, não foi possível medir a temperatura com os circuitos desenvolvidos devido à performance do parileno como dielétrico.

A produção bem-sucedida de uma membrana híbrida de dupla camada, flexível e conformável, totalmente funcional pode impulsionar a adaptação de outros equipamentos rígidos de monitorização de saúde para membranas híbridas flexíveis, inserindo ainda mais esta tecnologia na vida quotidiana.

Palavras-chave: Eletrónica Híbrida Flexível, Dupla Camada, Parileno C, Circuito Integrado de Silício, Monitorização de Temperatura

Contents

List of Figures xvii

List of Tables xxi

Abbreviations/Acronyms xxiii

1 Introduction 1

1.1 Motivation and Context 1
1.2 Goals 2
1.3 Thesis Overview 3

2 Theoretical Concepts 5

2.1 Parylene 5
2.2 Thin Film Microfabrication Techniques 6
2.2.1 Chemical Vapour Deposition 7
2.2.2 Electron Beam Evaporation Method 8
2.2.3 Photolithography 9
2.2.4 Reactive Ion Etching 10
2.3 Surface Mount Assembly Process 11
2.4 Rigid Circuits for Temperature Measuring 13

3 Flexible Electronics: State of the Art 17

3.1 Fully Flexible Electronics 17
3.1.1 Temperature Sensors 18
3.2 Flexible Hybrid Electronics 20

4 Materials and Methods 25

4.1 Electrical Circuit Design (Photomasks) 25
4.2 Assembling Flexible Hybrid Electronics 26
4.2.1 Microfabrication Steps 26
4.2.2 IC Integration 36

4.2.3 Peel Off . . . 38
4.3 Other Production Techniques . . . 39
4.4 Characterization Techniques . . . 42
4.4.1 Superficial Characterization . . . 42
4.4.2 Electrical Characterization . . . 43
4.4.3 Structural Characterization . . . 44

5 Results and Discussion **47**
5.1 Circuit and Photomask Design . . . 47
5.2 Manual Mask Alignment System Development . . . 50
5.3 Parylene Deposition . . . 51
5.4 Copper Deposition and Patterning . . . 53
5.5 Wet and Dry Etching . . . 56
5.6 Soldering Process . . . 60
5.7 Peel Off . . . 62
5.8 Final Prototypes and Testing . . . 66

6 Conclusion **71**
6.1 Future Perspectives . . . 73

Bibliography **75**

Appendices

A Schematics and Circuits **87**

B Photomasks **91**

C Arduino Codes **95**

Annexes

I Laser Power and Speed Conversion Charts **99**

List of Figures

2.1 Chemical structures of the three main commercially viable parylene variants. 5
2.2 Parylene deposition process. 7
2.3 Experimental setup of the electron beam (e-beam) evaporation method. . . 8
2.4 Spin Coating process. 9
2.5 Positive and negative masks. 10
2.6 Simplified reactive ion etching (RIE) system, composed of plasma to etch thin films. 11
2.7 Example of a commonly used reflow profile. 12
2.8 Process steps for printing and assembling flexible hybrid electronics (FHE) systems. 13
2.9 MAX30205 Human Body Temperature Sensor Evaluation Kit. 14
2.10 Adafruit MAX31865 resistive temperature detector (RTD) PT100 Amplifier. . 15

3.1 Overview of electronic skin (e-skin) component and technological requirements. 18
3.2 Flexible membrane RTDs for skin temperature measuring. 20
3.3 Research works mentioned above relevant to this dissertation. 23
3.4 Self-alignment of rigid silicon integrated circuits (ICs) and surface mounted devices (SMDs) following the reflow process, from [8]. 24

4.1 Steps involved in the production of photomasks. 25
4.2 Example of a glass carrier. 26
4.3 Departamento de Ciência dos Materias (DCM)'s spin coater equipment. . . 27
4.4 Glass carrier with the spin coated polyvinyl alcohol (PVA) layer. 28
4.5 chemical vapour deposition (CVD) system responsible for the deposition of parylene. 28
4.6 Deposition of a parylene layer to act as a substrate. 29
4.7 Center of Excellence in Microelectronics Optoelectronics and Processes (CEMOP)'s e-beam evaporation system. 30
4.8 Deposition of the copper layer onto the untreated a parylene layer. 31

4.9 Equipment used during the photolithography process. 31
4.10 Photoresist layer spin-coated onto the metal layer. 32
4.11 Patterned photoresist succeeding the development step. 32
4.12 Patterned copper layer succeeding the wet etching step. 33
4.13 Deposition of the second parylene layer for dielectric purposes. 33
4.14 CEMOP's dry etching equipment. 34
4.15 Etching of the parylene layer in specific areas. 35
4.16 Membrane status after all microfabrication processes and prior to the soldering phase. 35
4.17 Solder paste deposition on the parylene areas opened by dry etching. 36
4.18 DCM's pick and place system in use. 37
4.19 Placement of rigid ICs and SMDs over the solder paste. 37
4.20 DCM's reflow oven with the time-temperature reflow profile used on screen. 38
4.21 Final produced membrane without the glass carrier. 39
4.22 Centro de Investigação de Materiais (CENIMAT)'s commercial laser. 39
4.23 Example of a laser design used in this project. 40
4.24 DCM's 3D printer. 41
4.25 Steps involved in the production the 3D carrier support. 41
4.26 Profilometers used throughout the superficial characterizations. 42
4.27 CENIMAT's Olympus BX51 optical microscope. 43
4.28 Representation of the four-point-probe method. 44
4.29 CENIMAT's X'Pert PRO MRD system responsible for the X-ray diffraction (XRD) method. 44

5.1 MAXIM prototype's circuit design. 48
5.2 Photomasks used for the light emitting diode (LED) prototype. 49
5.3 Final result of the carrier support manufactured via laser technology. 50
5.4 Final result of the carrier support manufactured via 3D printing. 51
5.5 Thickness measurement of the parylene substrate layer, using the profilometry method. 52
5.6 PT100's electrical circuit etched onto the copper layer. 53
5.7 Comparison between the diffractogram from XRD analysis of the prototype's substrate and the reference diffractogram for copper. 54
5.8 Examples of the by-products of the wet etching method. 56
5.9 Unwanted metal removal due to the over-etching of the copper layer. 56
5.10 Noticed pads and viae detached from the main circuit. 57
5.11 Schematic of the possible explanations for the detached pads and viae. . . . 58
5.12 First step in the solution for the detached pads and viae. 58
5.13 LED prototype's circuits after the deposition of the silver paint on the required areas. 59
5.14 Size comparison between components of different size codes. 60

5.15 Solder paste appearance before and after being submitted to a temperature reflow profile. 61
5.16 Size comparison between the zero insertion force (ZIF) connector and 0402 size code components. 62
5.17 Comparison between the first and second iteration MAXIM prototype. . . . 63
5.18 Diffractograms from a XRD analysis of parylene C at different temperatures. 64
5.19 Inversion boards created. 65
5.20 Mechanical fragilities among prototypes. 65
5.21 Communication enabling devices, based on ZIF connector and their final purpose. 66
5.22 Prototypes which were submitted to the testing phase. 67
5.23 Tests performed to the MAXIM prototype and the warning message displayed in Maxim Evaluation kit's program succeeding each test. 67
5.24 Debugging of the MAXIM prototype, including its interface with the Arduino and the confirmation that no sensor was detected. 68
5.25 Example of overlapping circuit threads. 69
5.26 LED activation. 69

A.1 Schematic diagrams and circuit designs for the LED prototype. 88
A.2 Schematic diagram and circuit design for the MAXIM prototype. 89
A.3 Schematic diagram and circuit design for the PT100 prototype. 90

B.1 Photomasks used for the LED prototype. 92
B.2 Photomasks used for the MAXIM prototype. 93
B.3 Photomasks used for the PT100 prototype. 94

C.1 Arduino code created for the LED prototype. 96
C.2 Arduino code for the MAXIM prototype. 97
C.3 Arduino code for the PT100 prototype. 98

I.1 Laser speed and power percentage conversion to standard units for the VLS 3.50 desktop laser by Universal Laser Systems. 100

List of Tables

3.1 Summary of the presented FHE research work, including their references. . 24

4.1 Temperature and Process Low Alarm values used for parylene deposition. . 29
4.2 Parameters used during the e-beam evaporation method. 30
4.3 RIE parameters used during the dry etching process of the parylene films. . 34
4.4 Profilometer parameters. 42

5.1 Thickness measurements of the several parylene deposited layers. 53
5.2 Component's viability for the soldering process. 60

Abbreviations / Acronyms

ADC	analog-to-digital converter
BLE	bluetooth low energy
CEMOP	Center of Excellence in Microelectronics Optoelectronics and Processes
CENIMAT	Centro de Investigação de Materiais
CNT	carbon nanotube
CVD	chemical vapour deposition
DC	direct current
DCM	Departamento de Ciência dos Materias
e-beam	electron beam
e-skin	electronic skin
ECG	electrocardiography
EEG	electroencephalography
EMG	electromyography
FHE	flexible hybrid electronics
GUI	graphic user interface
I^2C	inter-integrated circuit
IC	integrated circuit
IoT	internet of things
IPA	isopropyl alcohol
LED	light emitting diode

MEMS	microelectromechanical system
NFC	near-field communication
PCB	printed circuit board
PDMS	polydimethylsiloxane
PE	polyethylene
PEN	polyethylene naphthalate
PEO	polyethylene oxide
PET	polyethylene terephthalate
PI	polyimide
PVA	polyvinyl alcohol
PVD	physical vapour deposition
RF	radiofrequency
RFID	radio frequency identification
RIE	reactive ion etching
RTD	resistive temperature detector
SMD	surface mounted device
ULP	user language program
UV	ultra-violet
XRD	X-ray diffraction
ZIF	zero insertion force

1
Introduction

1.1 Motivation and Context

In recent years, with the increasing research interest in personalized medicine, which harnesses biomedical devices to provide tailored diagnostics according to the individual characteristics of each patient. And with the rapid development of modern society, new and disruptive technologies such as the internet of things (IoT) and flexible wearable electronics have emerged and have become trending topics in the scientific community [2]–[4].

Owing to their stretchability, soft nature, flexibility, lightweight and other unique properties, flexible electronics, unlike rigid silicon-based electronic devices, can be conformally attached to the human body, achieving both measurement fidelity and wearing comfort, enabling new applications in the fields of biomedical engineering and continuous wearable health monitoring [2], [5], [6].

Despite consistent progress in the area of fully flexible electronics, these continue to reveal some constraints. Among them, low performance and high-power consumption. In opposition, silicon integrated circuits (ICs) do not report such limitations, providing unparalleled performance at low power consumption for years. As a result, over the past few years, the new concept of flexible hybrid electronics (FHE) emerged, opening new avenues for research, as well as suggesting broader impacts on human life [6], [7]. The market research agency, IDTechEx, finds that by the year 2030, the global demand for FHE will reach a value of over $ 3 billion [8], [9].

FHE combines traditional silicon ICs with flexible and printed electronics leveraging the strengths of these two dissimilar technologies, using flexible electronics to produce devices that can conform to the irregular topographies associated with its deployment and silicon ICs for computation and communication purposes [6], [10].

The development of FHE is enabling a new generation of wearable health monitoring systems, providing user comfort, compliant mechanics and soft integration [2], [5], [10]–[12]. These new devices are being developed in order to perform continuous physiological

monitoring via real-time measurements of body motion, blood pressure, body temperature, heart rate, glucose and lactate content in sweat, as well as electrophysiological activities including electroencephalography (EEG), electrocardiography (ECG) and electromyography (EMG) [2], [5], [12]. They can also be used in the form of human-machine interface and in electronic skin (e-skin) applications [3], [13]. By attaching these devices to the body surface and combining them with wireless communication protocols, such as near-field communication (NFC), allows a real-time and easy way of obtaining data from the previously mentioned health measurements [8], [14].

This long-term monitoring of vital signals provides critical information to establish an individual's health baseline, alerting users and healthcare professionals when abnormalities are detected, indicating if further medical attention is necessary [15]. One of the most significant factors associated with human health and physical activity is body temperature. Since an elevated body temperature can be an indication of infection, inflammation, or fever, on the contrary, a degraded body temperature may signify low blood flow due to circulatory shock [11], [15]. For the mentioned reasons temperature sensors have been developed for applications in healthcare and medical diagnosis devices.

Therefore, in order to produce scalable, cost-effective designs for reliable temperature monitoring on dynamically moving human subjects, the combination of flexible electronics with rigid silicon ICs, such as temperature sensors, is vital to withstand the complex mechanical deformation of the human skin and at the same time provide accurate temperature data. [6], [8], [16].

1.2 Goals

This master thesis's main goal is the creation of FHE membranes for body temperature monitoring. To achieve this goal ultra-thin and conformable double layered hybrid sensing membranes, based on rigid silicon ICs and surface mounted devices (SMDs) over flexible metal and parylene layers, will be developed and used.

To accomplish this project's proposition, various necessary steps need to take place:

- **Study the individual response of two commercial rigid temperature measuring circuits**. The FHE membranes produced in this project will be based on circuits such as, the MAX30205 Human Body Temperature Sensor Evaluation Kit and the Adafruit MAX31865 resistive temperature detector (RTD) PT100 Amplifier.

- **Produce the flexible element of the FHE membrane, comprised of parylene films and metallic thin films**. This step will require the application of thin-film microfabrication techniques, in a clean-room environment.

- **Assemble rigid and silicon-encapsulated electronics (ICs and SMDs) onto the flexible substrate**. This will include the use of low-temperature solder paste and

reflow soldering. In addition, to determine the smallest size code components viable for soldering on the flexible substrates, various soldering tests will be performed.

- **Interface the sensing membrane with a microcontroller.** During this stage, a way to make contact between the conductive pattern developed to either the microcontroller present in the MAX30205 Evaluation Kit or an Arduino will be created in order to access the temperature values.

1.3 Thesis Overview

To help follow up this work, it is essential to outline the adopted thesis structure and summarize the content of each chapter. This thesis is divided into six chapters.

In this chapter, the context and motivation for the development of this work are explained, and the objectives are defined.

The theoretical concepts necessary to understand and support the work developed throughout this thesis are introduced in Chapter 2, among them the microfabrication techniques employed to produce the flexible membrane along with the assembly process of the FHE membrane. Furthermore the rigid printed circuit boards (PCBs) in which the FHE membranes are modeled after are presented.

In Chapter 3, the use of parylene in areas related to this thesis is analysed and existent flexible hybrid wearables used for medical applications are highlighted. The methodologies and equipment used throughout this project are sequentially described in Chapter 4.

Chapter 5 details the optimizations performed and results obtained from the previously disclosed chapter, as well as, addresses the developed prototype's achievements and failures. The last two chapters are image heavy allowing for an easier and better understanding.

Finally, Chapter 6 summarizes the most relevant conclusions and achievements of this dissertation and provides suggestions for future work to enhance this study.

2

Theoretical Concepts

This chapter presents the theoretical basis for the production of a flexible hybrid sensing membrane. Among other concepts, the thin-film fabrication techniques used as well as methods for the surface mount assembly of ICs are described. Followed by a brief overview on the rigid circuits in which the sensing membranes were modeled after.

2.1 Parylene

Parylene is the trade name for poly(para-xylylenes) polymers, a family of semi-crystalline thermoplastic polymers [17]. Typically, suited for flexible and bio-friendly substrates in implantable or wearable applications [18], [19].

This unique polymer consists of a linear chain of benzene rings with two methylene groups replacing two hydrogen atoms on opposite sides of the benzene ring serving as coupling links for the polymer [8], [20], [21]. Currently, there are over twenty different types of parylene, however, from these twenty, only three are considered commercially viable: parylene N, which does not have chlorines on the benzene ring, parylene C and D, with one and two chlorines on the benzene ring respectively [17], as demonstrated in Figure 2.1.

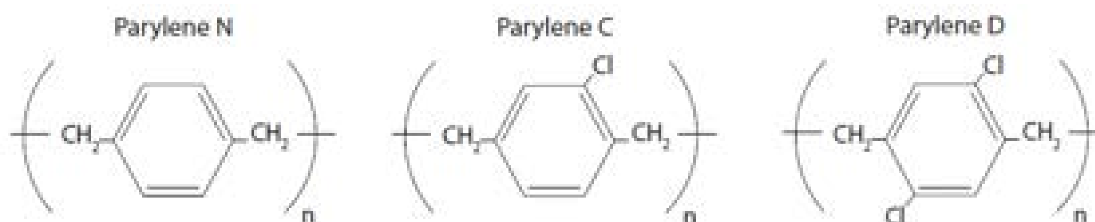

Figure 2.1: Chemical structures of the three main commercially viable parylene variants. Adapted from [8].

Depending on the type of parylene, their properties and uses also differ. Parylene N is primarily used as a dielectric, and when the prevention of crevice penetration is crucial. On the other hand, parylene C because of its low permeability to moisture and corrosive gases is able to repulse any aqueous solution that it comes in contact with. Parylene D is

used when mechanical strength is necessary [17], [22]. Given the imperviousness to water, a parylene C film enables the protection of devices from environmental deterioration when used as an encapsulation layer [20].

William Gorham devised a method for parylene deposition, involving the pyrolysis of a dimerized form of the material di-para-xylylene or paracyclophane, known as the Gorham vapour-deposition process. In this process the thickness of parylene films is very repeatable, well-controlled, and it can be determined by the mass of dimer placed in the vaporizer [8], [17].

When compared with other materials such as polydimethylsiloxane (PDMS) and polyimide (PI), the use of parylene C as a structural material presents several advantages including a pinhole-free conformability, [23], due to its room-temperature chemical vapour deposition (CVD) process, low water permeability, intermediate flexibility, and mechanical strength (Young's modulus of 4 GPa), and its good purity without solvent contamination [11], [18]. Moreover, parylene is process-compatible with the standard thin-film microfabrication techniques, which include metal deposition, photolithography, and etching, [19], and since is deposited at room-temperature the coating process is post-IC compatible [17].

Parylene C is also optically transparent, and it has good chemical stability, as well as excellent encapsulating properties [23]. Not only is approved by the Food and Drug Administration (FDA) but also has the highest biocompatibility rating for plastics in the United States, by being a US Pharmacopeia Class VI material, proving its capability to be safely applied in electronic skin (e-skin) wearable devices [17], [18]. Being biocompatible led parylene C to be widely used as a biocompatible encapsulant of implantable microdevices, such as pacemakers or WLAN antennas [8], [23], [24]. In addition, Jung et al. demonstrated that ultrathin parylene C membranes show negligible effects on the loss of energy originated from a radiofrequency signal reflected by an antenna (return loss) [24], [25].

Despite, the previously mentioned advantages, as temperature increases to the annealing temperature, crystallization of the parylene polymer occurs, hindering its flexibility and elasticity [25], [26]. In addition parylene C has a relatively low glass-transition temperature, T_g, of approximately 50 °C.

Considering all the information previously stated, parylene C will be used in this work as a substrate, dielectric and encapsulating layer. The following section will focus on techniques used to deposit parylene C and thin metal films.

2.2 Thin Film Microfabrication Techniques

In this section, the operating principles of the standard thin-film microfabrication techniques used to manufacture flexible constituents of a flexible hybrid electronics (FHE) membrane are explored. These include CVD to deposit the parylene, electron beam

(e-beam) for the deposition of metal films, photolithography and reactive ion etching (RIE) to pattern parylene, [8], [27].

2.2.1 Chemical Vapour Deposition

Generally, parylene thin film deposition is done using the CVD technique. In this technique, the polymerization of parylene occurs in a rarefied atmosphere in a vacuum chamber. The monomer uniformly polymerises at room temperature and covers all available surfaces [8]. The parylene deposition process consists of three main steps: vaporization, pyrolysis, and polymerization, illustrated in Figure 2.2 [28].

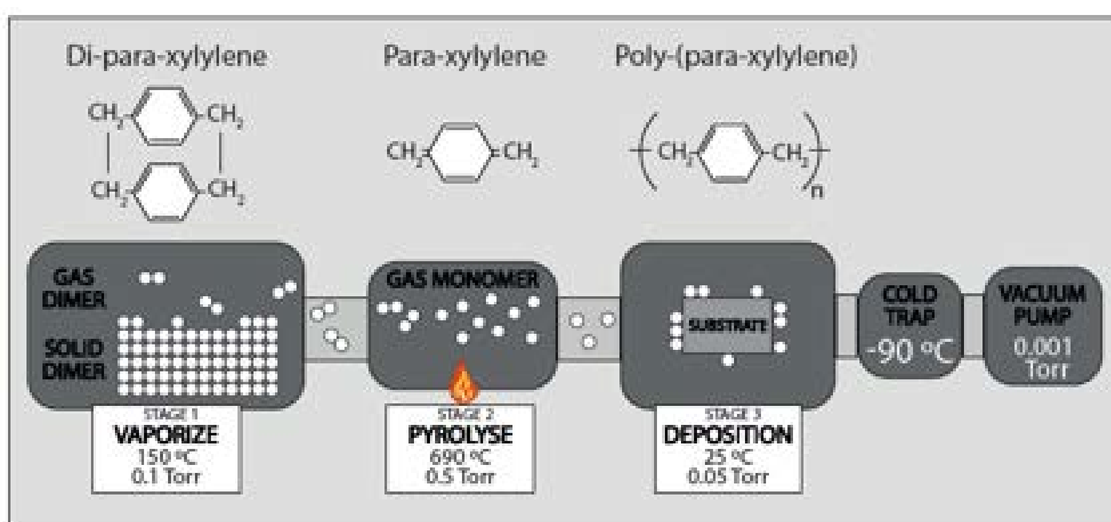

Figure 2.2: Parylene deposition process. Adapted from [8].

In the first step, after adding the required parylene dimer amount, [21], to the vaporizer chamber which varies depending on the pretended film thickness, the parylene is sublimated from its solid dimer form (di-para-xylylene), [8], [20], when heat is applied at 13.3 Pa.

Afterwards, the gaseous dimer is cleaved into a monomer (para-xylylene), using a high-temperature pyrolizer furnace, capable of achieving temperatures of 690 °C. The final step takes place in the deposition chamber, here the polymerization of the gaseous monomer occurs at room temperature with a pressure of 6.67 Pa, allowing the coating of the substrate [8], [28], [29].

A vacuum system ensures vacuum during the polymerization/deposition process and a cold trap prevents contamination of the pump by trapping the parylene molecules [21].

Following the parylene, metal deposition is one of the next possible steps and is achieved by physical vapor deposition methods such as e-beam evaporation.

2.2.2 Electron Beam Evaporation Method

Physical vapour deposition (PVD) includes several deposition techniques, and the e-beam evaporation method is one of them. Frequently, these physical deposition methods require a physical transformation from a solid or liquid state to vapour without undergoing chemical changes.

E-beam evaporation offers a simple deposition process, large-area deposition, convenient replacement of source targets, and controllability of deposition rates. Moreover, this deposition method holds a high material utilization efficiency along with structural and morphological control of films. E-beam evaporation also allows the deposition of a broad range of thin-film materials (e.g. Au, Cu, Ti and Pt) which were unlikely to deposit with other techniques such as thermal evaporation, where the temperature of the evaporant material is raised by resistive heating [30], [31]. Another advantage of this technique is its ability to produce thin films with low levels of impurities, [25], since in the resistive heating method besides the material, its crucible is also heated, risking the contamination of the material with the crucible's constituents.

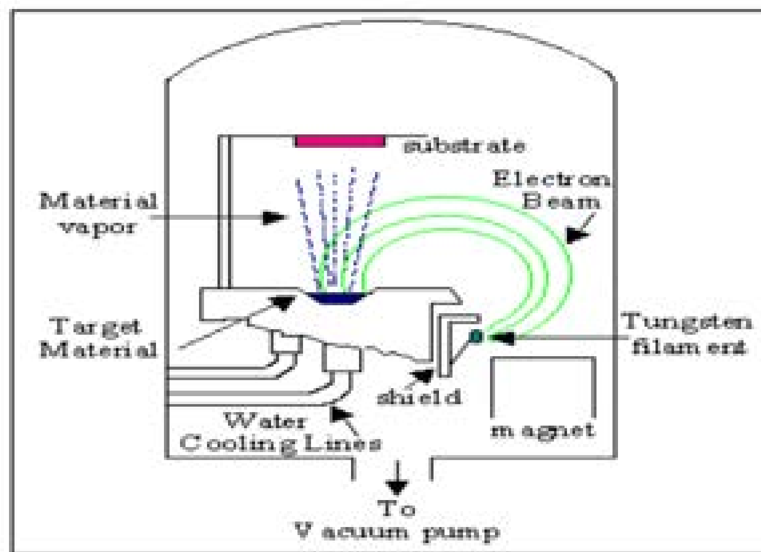

Figure 2.3: Experimental setup of the e-beam evaporation method. Adapted from [31].

The process of e-beam evaporation, depicted in Figure 2.3 begins under a vacuum of 10^{-5} mbar (10^{-3} Pa) or less. Then by applying a high voltage to the filament, high currents are created originating electron emissions. After the initial electron emissions, a magnet is used to deflect and accelerate the e-beam towards the target material placed in a crucible, where temperatures could reach up to 3000 °C [8], [31], [32].

The heating process is accomplished by transforming kinetic energy into thermal energy by virtue of the large number of electrons hitting the evaporant's surface, vaporizing the target material. The vaporized material will then coat a substrate positioned above the crucible [8].

When the desired thickness is achieved, the deposition is complete. In order to verify

in-situ the thickness of the deposited thin film, a thin-film thickness monitor composed of a quartz crystal microbalance, is used [8], [33].

Photolithography is the next step, so the deposited metal layer could be patterned.

2.2.3 Photolithography

Photolithography is a fundamental patterning process in microfabrication [25]. This technique consists of the formation of a pattern in a layer of a photosensitive polymer (photoresist) when exposed to ultra-violet (UV) light through a mask. The obtained pattern in the polymer can then be selectively dissolved so the user can access the specific pattern in the underlying substrate [8], [34].

To carry out its primary goal, photolithography involves several steps. Afore initializing this process, the substrate must be subdued to rigorous cleaning [25]. Following this step, the deposition of the photoresists is performed, during which, a thin layer of this organic photosensitive polymer is deposited. Generally, this deposition is performed by spin coating, represented in Figure 2.4. Here a vacuum chuck is responsible for holding the substrate in place, so the photoresist is spread over it, due to centrifugal forces, spreading the solution over the substrate's surface. The combination of spin speed and its duration is what determines the film's final thickness [8], [33], [35].

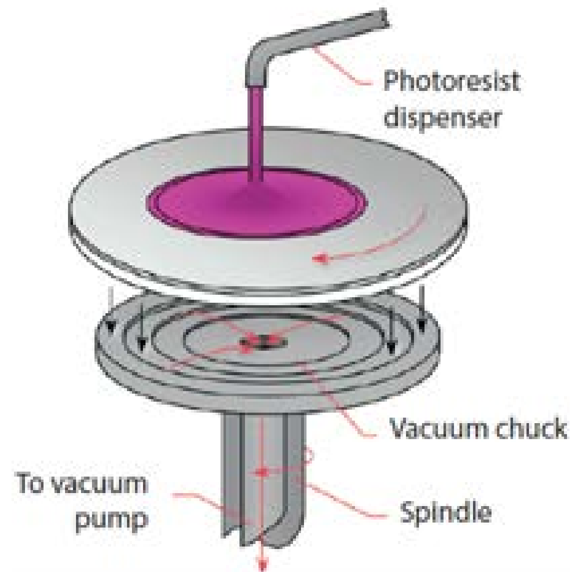

Figure 2.4: Spin Coating process, adapted from [8].

Since the organic polymer, after the coating, may still contain up to 15% of solvent and may also contain built-in stresses, the substrate is soft baked at 90 °C, to remove the solvents and stresses as well as to promote adhesion of the photoresist layer [8], [33], [35].

In a subsequent step, the photoresist-coated substrate is relocated to a mask aligner, consisting of a UV lamp aligned with the mask. Allowing a perfect transfer of the mask's pattern onto the light-receiving substrate in the form of a latent image. This is a result

of modifications to the solubility of the photoresist, ascribed to chemical reactions in the radiation-exposed areas of this layer [8], [33], [35].

Masks can either be negative or positive, as seen in Figure 2.5. When the pattern is transparent with a black background, the mask is called a positive or dark field. If the pattern is dark and the background transparent it's called a negative or clear field mask. Regularly these masks can be made of a flat glass, a quartz plate or photolith film [8], [33], [35].

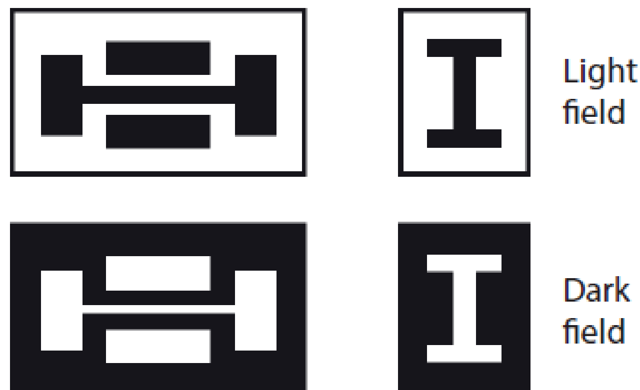

Figure 2.5: Positive and negative masks. Adapted from [35].

Photoresists are composed of three main components: a polymer (base resin), a sensitiser, and a casting solvent. When exposed to a certain intensity of radiation during a period of time, the polymer changes its structure. One of the main features of the photoresists is the resist tone, dividing photoresists into positive and negative. If positive, the polymer is weakened by photochemical reactions, which scission of the main and side polymer chains, during radiation exposure, this makes the photoresist more soluble in developing solutions. In the opposite case, the photoresist becomes less soluble, due to the strengthening of the polymer by random cross-linkage of the main and pendant side chains [8], [33], [35].

The final step is called development and it is necessary to dissolve the unpolymerized photoresist, forming a latent image that will serve as a mask for further steps. There are two main technologies applicable after the development: wet and dry development. Predominantly wet development is used over dry, however, the aforementioned is starting to replace the wet development for some line-width resolution applications [8], [33], [35].

2.2.4 Reactive Ion Etching

RIE, otherwise known as dry etching, is a process where physical and chemical effects are combined to remove material from a subject's surface. It uses radiofrequency (RF) discharge-excited species (radicals, ions) to etch unmasked substrates or thin films in a low-pressure chamber. This process is essential not only if there is a need for narrow lines

or channels but also when high aspect ratio structures need to be fabricated [8], [33], [36], [37].

Several materials, such as oxides, metals and polymers, can be etched through RIE using different reactive atmospheres. Different parameters can used to optimize the etching time and anisotropy such as the RF power, the pressure inside the chamber as well as, the type and flow rate of the etching gas [36], [38]. Among the gases used in this process are tetrafluoro-methane (CF_4), oxygen (O_2), and sulfur hexafluoride (SF_6) [8], [33], [36], [37].

A typical RIE equipment, as seen in Figure 2.6, consists of a vacuum chamber with two electrodes that create an electric field that ionizes the gas molecules, creating the plasma. As soon as the plasma is established, the direct current (DC) bias voltage extracts ions from it and energizes them, accelerating them towards the substrate, contributing to the directionality of etching and consequently to the desorption of reaction byproducts from the substrate [8], [39].

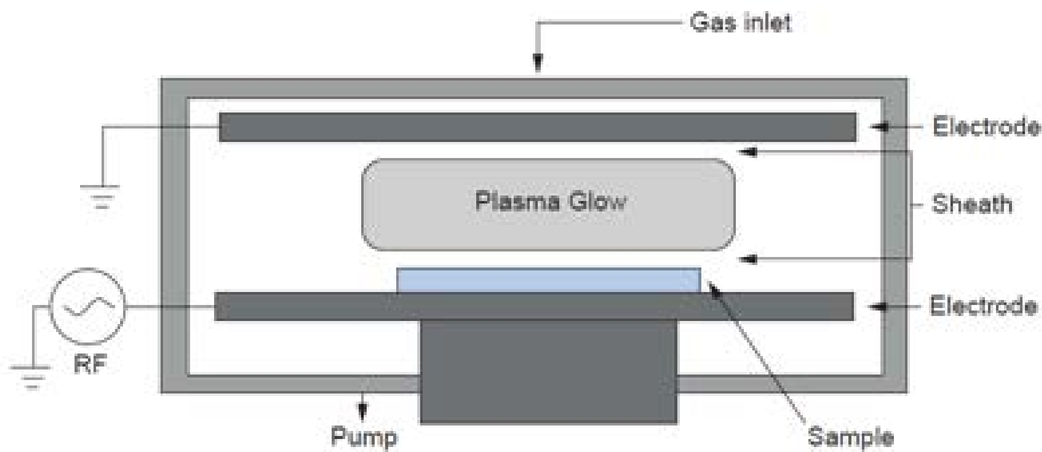

Figure 2.6: Simplified RIE system, composed of plasma to etch thin films. Adapted from [8].

2.3 Surface Mount Assembly Process

After the fabrication of the flexible components present in the final membrane, the integration of silicon integrated circuits (ICs) and surface mounted devices (SMDs) onto this membrane is the next step in order to build a fully functional sensing membrane.

Surface mount assembly is a process which enables the integration of ICs and SMDs in printed circuit boards (PCBs) which is also suitable for FHEs. Primarily this technique is a process of reflow soldering, that involves firstly the deposition of solder paste, then the component placement and finally the reflow [8], [40].

A mixture of solder beads and flux is what comprises solder paste. The flux besides allowing the coalescence of soldering beads, also serves as a medium for them, providing stable soldering [8], [40].

Following the completion of the paste's deposition and the IC's placement, the PCB is prepared for reflow. This method includes infrared reflow, forced convection reflow, vapour phase reflow, and in-line-conduction reflow. From these, the infrared and convection reflow are very effective in heating and transferring heat, respectively, making them the prevailing methods used [8], [40]. A commonly used reflow profile can be seen in Figure 2.7.

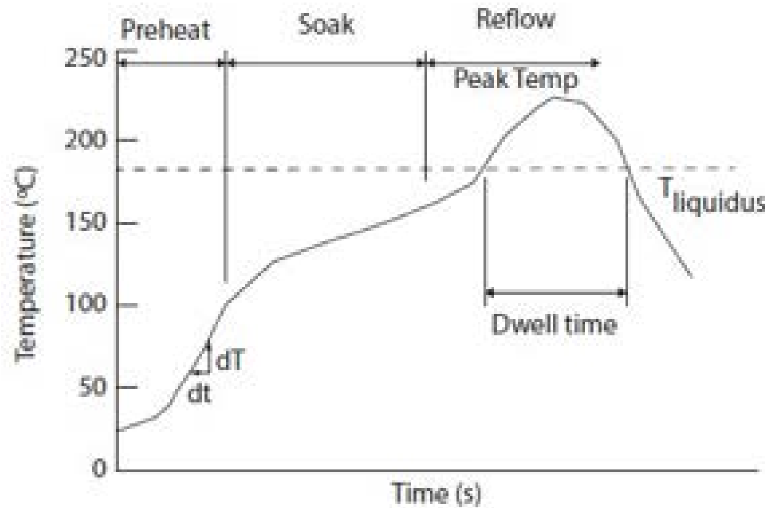

Figure 2.7: Example of a commonly used reflow profile. Adapted from [40].

Several component manufacturers specify a maximum temperature rate rise of 4 °C per second, as can be expressed by dT/dt. Due to thermal stress build-up increases, caused by temperature gradient formation, moisture entrapment or even mismatch in thermal expansion coefficients of component materials. When regarding solder paste, an accelerated temperature increase may aggravate slump behaviour primarily due to a rapid drop in viscosity before the solvent is dried thoroughly [8], [40].

Therefore, the reflow profile may significantly vary from paste to paste, depending on the solvent used. Consequently, it is crucial that the temperature reflow profile, established by the producer of the solder paste is followed. Moreover the reflow profile can be broken down into several phases, namely, preheat, soak, reflow and cooling, as depicted in Figure 2.7 [8], [40].

In a typical FHE assembly process, the printed circuits are fabricated first, soon after, the rigid components are mounted. As depicted in Figure 2.8, the substrate is drilled, and the metal layer is printed on both sides of the substrate, if needed. After that, top and bottom encapsulations are printed, and the silicon ICs are bonded to the substrate [6].

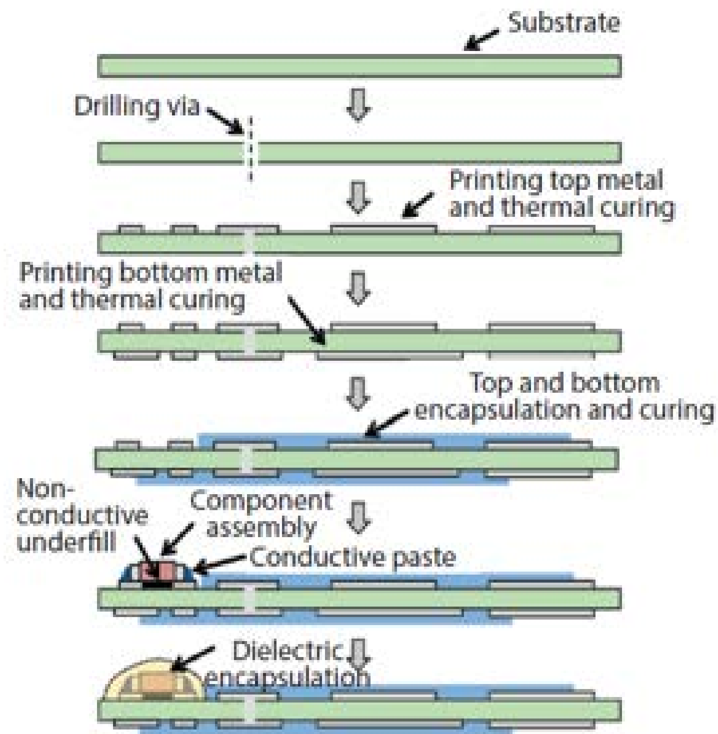

Figure 2.8: Process steps for printing and assembling FHE systems. Adapted from [6].

The next section, will give some insights on the rigid circuits in which the developed FHE prototypes will be based on.

2.4 Rigid Circuits for Temperature Measuring

In order to achieve viable and functional FHE systems comprised of several microscopic components, microcontrollers, more than one layer and different kinds of communication protocols, a prior assortment of tests and prototypes need to take place. As a starting point in this investigation it was proposed the conversion of commonly used and widely known circuits for temperature monitoring from their rigid PCB format to a flexible hybrid membrane.

As such the chosen circuits were the MAX30205 Human Body Temperature Sensor Evaluation Kit and the Adafruit MAX31865 resistive temperature detector (RTD) PT100 Amplifier. Preceding the fabrication of the membranes the specifications and characteristics of these devices require further investigating.

MAX30205 Human Body Temperature Sensor Evaluation Kit

The MAX30205 Human Body Temperature Sensor Evaluation Kit, from Maxim Integrated provides a convenient way to access the MAX30205 human body temperature sensor. This evaluation kit incorporates a few elements, including a temperature sensor PCB, a USBDTMB PCB, a 10-pin flex cable, a MICRO-USB cable and a graphic user interface (GUI) program. All these parts are illustrated in Figure 2.9 [41], [42].

Figure 2.9: MAX30205 Human Body Temperature Sensor Evaluation Kit. A - Temperature Sensor PCB with the MAX30205 human body temperature sensor. B - USBDTMB PCB, which controls the communication of the raw temperature data to the computer. C - GUI program supplied by Maxim Integrated.

The temperature sensor PCB, represented in Figure 2.9 A, contains as previously mentioned, a MAX30205 human body temperature sensor (MAX30205MTA+), available in an 8-pin TDFN package, which operates over the 0 °C to +50 °C temperature range, accurately measuring temperature with a 0.1 °C accuracy in a range from 37 °C to 39 °C while also providing an over-temperature alarm [41], [42].

The MAX30205 converts temperature measurements to digital form using a high-resolution, sigma-delta, analog-to-digital converter (ADC). It communicates via a inter-integrated circuit (I^2C)-compatible, 2-wire serial interface accepting standard write, read, send, and receive byte commands to read the temperature data and configure the behavior of the open-drain over-temperature shutdown output, allowing for temperature data to be sampled and transferred to the GUI [41], [42].

Furthermore the sensor features a 2.7 V to 3.3 V voltage range, low 600 μA supply current and a lockup-protected I^2C-compatible interface making it ideal for wearable fitness and medical applications [41], [42].

The USBDTMB PCB, represented in Figure 2.9 B, is used to do I^2C to HID transaction translation, transporting the raw temperature data to the computer through the USB and

displaying it on the GUI program, represented in Figure 2.9 C, [41], [42].

Taking into account the time period of this master's thesis project and the complexity of both PCBs only the sensor PCB (Figure 2.9 A) is eligible to be converted into a flexible hybrid membrane, leaving all communication and processing to the rigid USBDTMB PCB.

Adafruit MAX31865 RTD PT100 Amplifier

The Adafruit MAX31865 RTD PT100 Amplifier, depicted in Figure 2.10 A, employs a 100 Ω platinum RTD (PT100), represented in Figure 2.10 B, which is commonly used to measure temperatures in laboratory, industrial and medical settings because of its accuracy, repeatability and stability [43], [44].

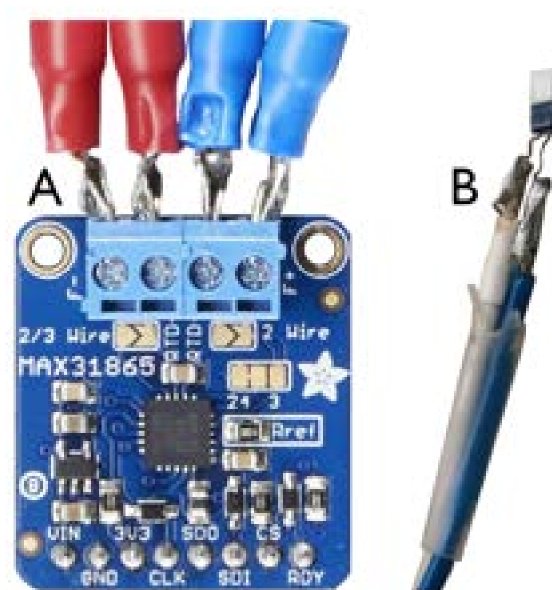

Figure 2.10: Adafruit MAX31865 RTD PT100 Amplifier. A - Amplifier board which includes the MAX31865 sensor, [43]. B - 100 Ω platinum RTD.

However, in order to take full advantage of the PT100's accuracy and precision an amplifier must be used, and that is where the MAX31865 sensor, from Maxim Integrated, comes into play. This sensor is a resistance-to-digital converter optimized for platinum RTDs, whose sensitivity is set by an external resistor, which in PT100's case is a 430 Ω resistance. This amplifier not only allows the reading of low resistance but also adapts automatically to the resistance of the connecting wires which can go up to four [43], [44].

The breakout of this device can be wired to any microcontroller, being Arduino the favoured microcontroller, the whole of the Adafruit MAX31865 RTD PT100 Amplifier is qualified to be converted into a flexible hybrid membrane, leaving all communication and processing to the Arduino.

3

Flexible Electronics: State of the Art

This chapter highlights several research projects in the field of flexible electronics by firstly, providing the state of the art of entirely flexible sensing membranes. The continuous development of these technologies led to the birth of e-skins, which mimic the properties of human sensing by using electronic methods.

However, the need for more accurate and reliable temperature measurements impelled the incorporation of ICs and SMDs into flexible membranes giving rise to FHE, the topic of the second part.

3.1 Fully Flexible Electronics

The concept of flexible electronics has been around for several decades, [45], one of its first references in literature being of a solar cell fabricated in a silicon wafer, which was then thinned to $\sim 100\mu$m and transferred to a flexible substrate [21], [46]. These days there is great interest in new materials and fabrication techniques that allow the manufacturing of high-performance scalable electronic devices directly onto flexible substrates. This interest extends beyond flexibility including properties such as stretchability, heal-ability, [47], [48], biocompatibility and biodegradability [49]–[51].

A common electronic structure is composed of 4 elements: a substrate, back-plane electronics, a front-plane, and encapsulation. In order for this structure to be flexible all components must comply with some degree of bending, maintaining the device's performance and reliability [52].

Therefore, flexible electronics are commonly used as standalone solutions in applications which do not require high computation power or being robust to deformation, [4], [45]. The previously mentioned characteristics enable flexible and wearable electronics to be used in a wide range of applications. In particular, the development of flexible and wearable medical devices for regular and continuous health monitoring, in addition to, their usage in the emerging field of skin-inspired electronics, e-skins [4], [13], [53].

Skin is the largest organ in the human body and functions as the physical interface between the body and the environment, providing the nervous system with sensory

input from external thermal and mechanical stimuli, resulting in a regulated physiological response allowing a safe and rapid interaction with the person's surroundings [54]–[56].

The pursuit of these e-skin devices is motivated by their possible application on functional prosthetic devices, [57], humanoid robotics, [58], and human health monitoring, where they could play a key role [59]–[61].

Figure 3.1 illustrates some examples of e-skin applications. In order to accurately measure and quantify the signals derived from human activities, physical and biochemical sensors have been developed and are integrated into these e-skins. These sensors include, for example, tissue pressure, [61]–[69], electrocardiographys (ECGs), [70]–[72], body temperature, [33], [54], [62], [73]–[75], metabolite levels, [76], UV levels, [77], electrolyte balance, [78], and biomarkers for some diseases [55], [79].

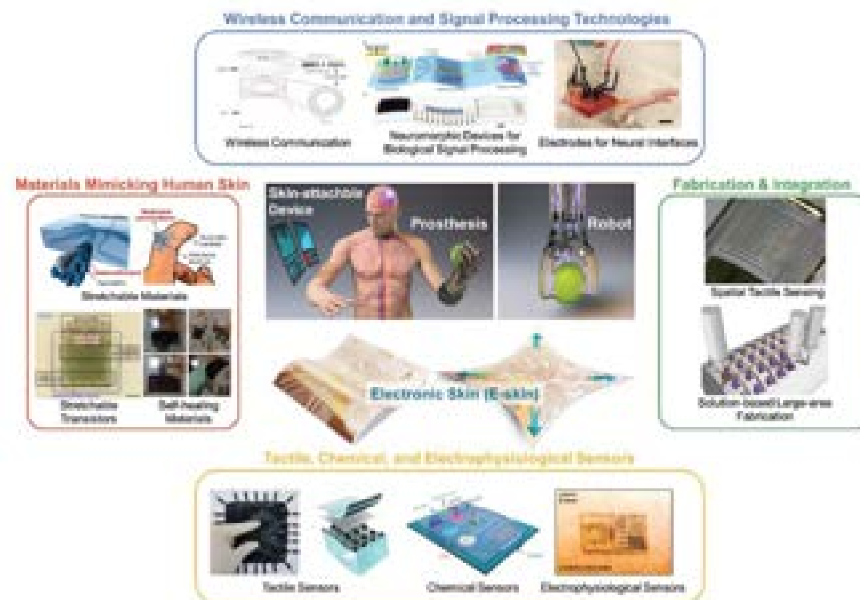

Figure 3.1: Overview of e-skin component and technological requirements. Adapted from [57].

3.1.1 Temperature Sensors

Temperature is one of the basic physiological parameters when detecting human activities and determining critical and abnormal body conditions such as infections, inflammation, hypothermia, and others. As they are closely related to the environment and human life, temperature sensors have been studied extensively in multiple applications.

When it comes to these sensors, several methods can be used to manufacture them, and they can be separated into different types depending on how they are able to detect temperature. These include RTDs, thermally sensitive resistors (thermistors), and pyroelectric temperature detectors [4], [11], [80].

From the specified types of temperature sensors, the most used are the RTDs for their high accuracy, fast response, physiological stability, simplicity of fabrication and ease of

mass production [11], [33], [80]. By using pure metals (Pt, Au, Cu), metal oxide particles, carbon nanotube (CNT) polymer composites, or graphene as the resistive material, the sensor's temperature detection mechanism can be explained according to the following equation,

$$R = R_0[1 + \alpha(T - T_0)] \tag{3.1}$$

where R is the resistance of the sensor at temperature, T, R_0 is the resistance of the sensor at the reference temperature T_0, usually 20 °C, α is the temperature coefficient of resistance. The equation establishes that the resistance of metal increases as the temperature also increases [4], [8], [11].

Initially, Kim et al. presented surgical suture strips that had serpentine-structured platinum temperature sensors with Si diodes for a diagnostic system. Via an in vivo experiment demonstrated scalability, biocompatibility, and stable measurements of the local temperature [11], [81].

Webb et al., in 2013, with the purpose of providing continuous and accurate thermal characterization of the human skin's surface, in an intimately and non-invasive manner, introduced an ultra-thin and compliant skin-like temperature sensor array with a thin (50 nm), narrow (20 μm), Au, 4×4 serpentine-structured, RTD dependent film prepared by microlithographic techniques (Figure 3.2 A). This stretchable electronic system was capable of non-invasive mapping of skin temperature with millikelvin accuracy [75].

However, in the matter of wearable applications, because these normally monitor temperatures within the range of $30 - 40$ °C, metal-based RTDs have a low-temperature resolution. Contrarily to metal-based RTDs, the resistance of thermistor-type temperature sensors changes non-linearly as the temperature increases. This feature makes it possible for these sensors to measure temperature much more precisely than RTDs, even though the temperature range is smaller. The thermistor's resistance varies according to the following equation,

$$R = R_0 \times e^{B\left(\frac{1}{T} - \frac{1}{T_0}\right)} \tag{3.2}$$

where R is the resistance of the sensor at temperature T, R_0 is the resistance of the sensor at $T = \infty$ and B is the thermal index [8], [11].

Jeon et al., also in 2013, developed a flexible wireless temperature sensor based on Ni microparticle-filled binary polymer composites with polyethylene (PE) and polyethylene oxide (PEO) as the matrix, in an effort to monitor human body temperature. As the operating principle when the material's temperature equals the composites melting point, the distance between Ni microparticle increases due to volume expansion of the composites, increasing the thermistor's resistance. In addition, a passive radio frequency identification (RFID) antenna was integrated with the temperature sensor on a plastic substrate, enabling wireless communication [8], [33], [74].

In a study carried out by Yan et al., a stretchable graphene thermistor with a tunable thermal index by mechanical strain was produced using graphene and silver nanowires,

fully embedded in an elastomer matrix composed of PDMS, as thermal detection channels and electrodes. This graphene thermistor not only was capable to be stretched up to 50% but could also be twisted up to 360°. Although it was observed a tendency for the offset resistance of the graphene thermal channel to increase upon stretching [8], [11], [15], [33], [82].

More recently Marquês, in her master thesis work, reported a flexible and conformable temperature sensor, for biomedical devices shown in Figure 3.2 B, demonstrating a new way of using parylene-C as a substrate and encapsulating layer via the application of multiple thin-film microfabrication techniques [33].

Figure 3.2: Flexible membrane RTDs for skin temperature measuring. A - 4x4 temperature sensor array before and after the twisting motion. Adapted from [75]. B - Flexible temperature sensor in parylene C, after peel-off. Adapted from [33].

Overall, despite promising advances made in wearable temperature sensing, a few impediments still affect accurate temperature measurements. One of those is the strain dependency of entirely flexible membranes, evidenced by Yan et al. in their work. This is not ideal for wearable sensing because flexing and twisting the sensor can alter the resistance of thermistors and RTDs, adding an error factor to the measurement [8], [15].

3.2 Flexible Hybrid Electronics

Considering all the challenges, mentioned above, related to entirely flexible electronics, FHE began to appear as an alternative over the past years, combining silicon ICs, flexible substrates, and printing functionalities, leveraging high-performance and low power computing capabilities.

FHE systems integrate functional material/components in traditional and unusual electronic architectures on flexible substrates to yield systems that have unique properties such as lightweight construction, conformable mechanics, functional reconfigurability, self-healing constitution, and others [7]. These systems bring together "soft" and "hard" electronics into a single platform where the "soft" devices are used in conformable sensor interfaces and are manufactured in soft substrates. On the other hand, "hard" silicon-based devices provide the computational backbone and compatibility with existing communication and computation standards for processing and transmitting data. Therefore, playing complementary roles in FHE [6], [8], [72], [83].

Wen et al. in 2016 presented a wireless wearable battery-free RFID temperature sensor patch in a flexible PI substrate (Figure 3.3 A). This research group not only reported a strain independent antenna during bending but also stated that the degradation of performance was nearly nonexistent [84].

Also in 2016, Khan et al. used FHE technology to develop a wearable ECG and skin temperature monitor, over a flexible Kapton/PI substrate that hosts the silicon ICs and rigid passive components (Figure 3.3 B). The ECG electrodes were inkjet-printed using gold nanoparticle ink and the skin temperature was recorded via a stencil-printed Ni oxide, negative temperature coefficient thermistor. To assemble the silicon ICs to the substrate a solder paste composed of Sn-Pb was applied followed by a solder reflow step, where the solder paste is subjected to a temperature profile [70], [72].

In 2018, Lee et al. introduced an ultrathin, low-profile, stretchable hybrid electronic system with ICs, embedded in breathable elastomeric membranes, for intraoral application, enabling real-time, long-range wireless assessment of Na^+ intake. The detection of Na^+ ions is possible due to a microstructured, ion-selective Na^+ sensor with functioning polymer membranes [85].

Tree years later, in 2021, Zhao et al. developed an on-skin FHE system that integrated electrophysiology electrodes as well as an accelerometer collecting both ECG and acceleration data, wirelessly transmitting, and displaying it in real-time on a mobile phone application through Bluetooth communication (Figure 3.3 C). This system uses PDMS as the substrate, therefore the research team used silane, a coupling agent, as a pre-treatment method to enhance the bonding strength between the rigid ICs and the flexible substrate [5].

In 2017, Escobedo et al. presented a full-passive multi-gas sensing tag, based on near-field communication (NFC) technology for energy harvesting and data transmission, including temperature, to a smartphone (Figure 3.3 D). In order for the silicon ICs to be assembled to the device's PEN substrate, conductive resin was used [86].

In the following year, Han et al. reported a battery-free wireless sensor for full-body pressure and temperature mapping, encapsulated on both sides with PDMS, using thin films of PI as electrical isolators [87].

In 2021, Rachim et al. introduced a new type of epidermal electronics designed for cuffless blood pressure monitoring, named "multiPANI". All of PANI's ICs were bonded to its polyethylene terephthalate (PET) film substrate [88].

Most of the existing FHE devices do not incorporate parylene C as a substrate. However, over the years, there has been an increase in the number of research papers mentioning this polymer not only as a substrate but also as an encapsulating layer [8].

In 2011, Li et al. presented a fully implantable, flexible, parylene-enable neurostimulator comprised of an antenna for wireless and data transmission, a BION stimulator IC and, other passive components. The system assembly was achieved by interconnecting individual components together on the carrier substrate with a biocompatible Ag epoxy [89], [90].

In the same year Ledochowitsch et al. reported the design, microfabrication and testing of a flexible 256-electrode array for micro-electrocorticography, comprised of a flexible five-layer microelectromechanical system (MEMS) device [91].

Chang et al., in 2013 designed a system capable of packing a 512-channel intraocular epiretinal implant. To integrate the several ICs onto the parylene membrane, Ag conductive epoxy was used [92].

Two years later in 2015, Maeng et al. exhibited integrated micro-supercapacitors on an ultrathin and highly flexible parylene film, with an RF rectifier circuit for energy harvesting purposes. Ag conductive epoxy was used to assemble all of its components to the device's substrate [19].

Later in 2017, Lin et al. demonstrated a flexible device, based on parylene C, with temperature sensing functionalities, depicted in Figure 3.3 E [18].

In 2019, Duarte developed a passive radio frequency antenna, able to obtain energy when a radio frequency transmitter is approached (converting its signal into current), using parylene C as a substrate and encapsulating layer. Proving that these ultra-thin parylene membranes are compatible with commonly used microelectronic production techniques and as such, it is possible to standardize thin films under their surface, presented in Figure 3.3 F [25].

More recently in 2021, Chong in his dissertation conceived a fully integrated, wireless, flexible pulsation sensor for real-time monitoring of blood pressure in vascular grafts using a piezoresistive PDMS composite for the strain sensing element. The application of a solder paste, followed by component placement and reflow soldering were the methods used as a means to assemble the electronic components to the PDMS flexible circuit board [10].

Also in 2021, Selbmann et al. presented an avant-garde approach for the fabrication of a ultra-thin and extremely flexible parylene based PCB, featuring multiple metallic layers (Figure 3.3 G). The production of this device had personalised medicine and medical wearables in focus, allowing it to be attached to a patient, acting as an e-skin, measuring vital signals while simultaneously using biocompatible materials [93].

In the same year, Santos reported an innovative way of using parylene C as substrate and encapsulating layers to accommodate silicon ICs and SMDs for the purpose of monitoring skin temperature, resulting in the production of a sensing membrane, seen in Figure 3.3 H. The integration of silicon ICs and SMDs was tested using a lead-free low-temperature solder paste and reflow oven allowing the establishment of an electrical connection between the thin metal pattern and the silicon ICs. In addition, an NFC data transfer was established between the sensing membrane and a mobile device [8].

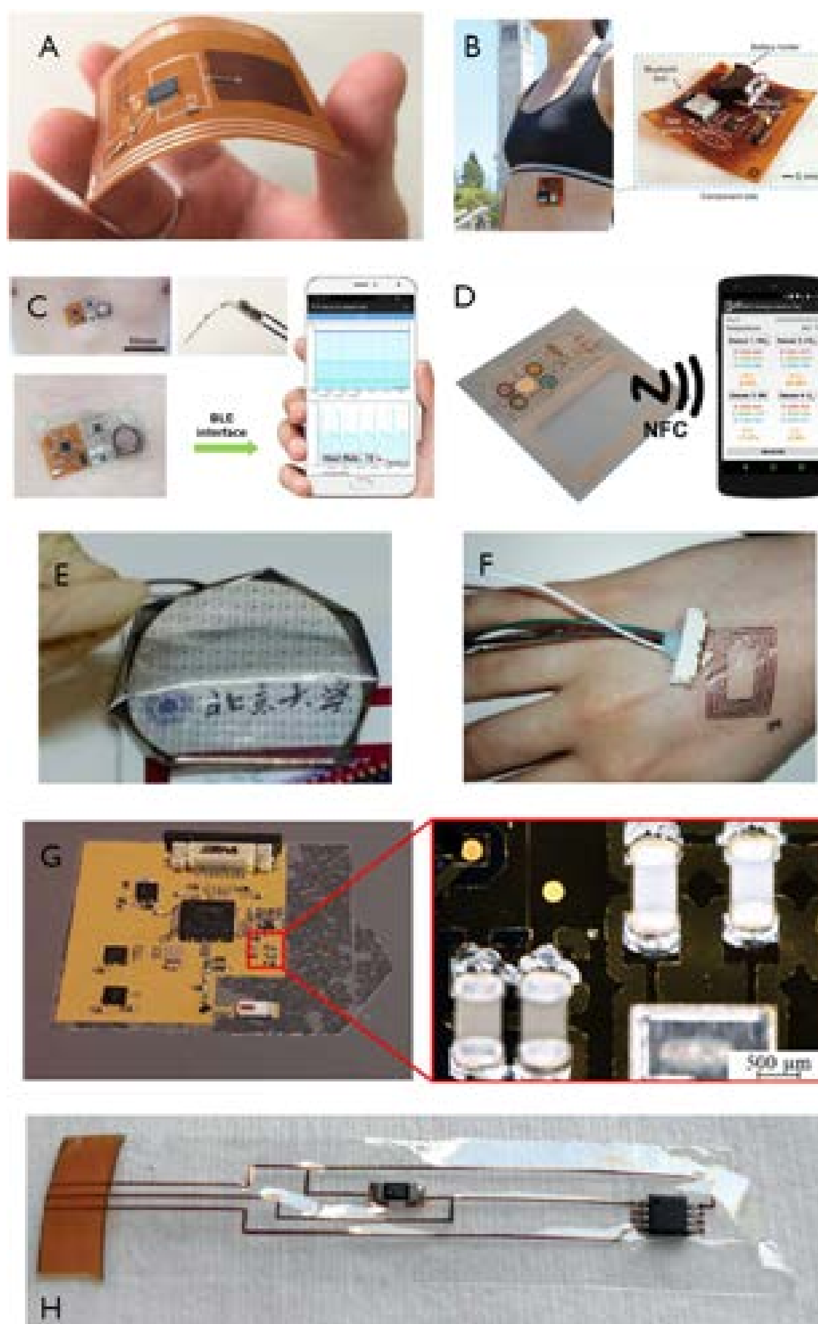

Figure 3.3: Research works mentioned above relevant to this dissertation. A - Fabricated RFID temperature sensor on a bendable PI substrate, adapted from [84]. B - Flexible hybrid PI membrane composed of ECG electrodes and a thermistor, adapted from [72]. C - On-skin FHE system collecting both ECG and acceleration data while wirelessly transmitting it. Adapted from [5]. D - Multi-gas sensing NFC tag printed on flexible polyethylene naphthalate (PEN) substrate. Adapted from [86]. E - Flexible device, based on parylene C as substrate, able to sense temperature, adapted from [18]. F - Passive radio frequency antenna, using parylene C as a substrate and encapsulating layer, adapted from [25]. G - ultra-thin flexible parylene based PCB with multiple layers, adapted from [93]. H - temperature sensing membrane using parylene C as substrate and encapsulating layers to accommodate silicon ICs and SMDs, adapted from [8].

The last presented studies confirmed solder pastes as a connecting element to integrate silicon ICs and SMDs into flexible electronics. These pastes consist of a mixture of tiny solder spheres within a solder flux [8]. The high reflow temperature of Sn-Pb solders hinders, in most cases, its usage in flexible substrates, as well as other alternative solders that, despite reflow temperatures being < 175 °C, are still high for most of the flexible substrates [6], [8].

Generally, the cure temperatures of conductive adhesives are lower then the solder paste temperatures. However, IDTechEx forecasts that low-temperature solder pastes will eventually replace conductive adhesives since solder pastes allow the self-alignment of silicon ICs and SMDs, as exhibited in Figure 3.4 [8], [9].

Figure 3.4: Self-alignment of rigid silicon components after the reflow process, from [8].

In conclusion Table 3.1 summarizes all aforementioned mentioned research works related to FHEs, in order to facilitate their reading and interpretation.

Table 3.1: Summary of the presented FHE research work, including their references.

Year	Substrate Material	Conductive Material	Solder Paste	Communication Type	Layers	Ref.
2011	Parylene-C	Au/Pt	Ag epoxy	RFID	1	[89]
2011	Parylene-C	Pt	-	-	5	[91]
2013	Parylene-C	Ti/Au	Ag epoxy	RFID	1	[92]
2015	Parylene-C	Au	Ag epoxy	RFID	1	[19]
2016	PI	Nylon conductive fabric	-	RFID	2	[84]
2016	Kapton/PI	Au/NiO/Cu	Sn-Pb	Bluetooth	-	[72]
2017	PEN	Ag	Conductive resin	RFID	2	[86]
2017	Parylene-C	Al	-	-	1	[18]
2018	Eco30 and PI	Cu	-	Bluetooth	3	[85]
2018	PDMS/PI	Cu/Ti/SiO2	Ag epoxy	RFID	6	[87]
2019	Parylene-C	Cu	-	RFID	1	[25]
2021	PET	Ag	-	bluetooth low energy (BLE)	2	[88]
2021	PDMS	Ag micro-flakes/Cu	Silicone	Bluetooth	-	[5]
2021	PDMS	Cu	Indium 8.9E	-	2	[10]
2021	Parylene-C	Ti/Au	Sn42Bi58	-	3	[93]
2021	Parylene-C	Cu	Sn42/Bi57.6/Ag0.4	RFID	1	[8]

4

Materials and Methods

This chapter presents the overall pipeline and materials deployed throughout the fabrication and characterization of the FHE membranes developed.

An overview of the photomask design, the FHE assembling steps performed, as well as, the characterization techniques used and additional methods followed during this work, will be presented throughout this chapter.

4.1 Electrical Circuit Design (Photomasks)

Negative and positive photomasks were designed with the intent of transferring the developed electrical circuit patterns (i.e. MAXIM, PT100 or LED) onto either the metal or the parylene layers used.

After designing the electrical circuits using Eagle®, an Autodesk® software, the resultant board (.brb) files had to be imported into the Adobe Illustrator CC 2020 software as scalable vector graphic (.svg) files so the photomasks could be finalized and sent to the printing office, Guide - Artes Gráficas, in a pdf format to be printed on photolith film. As a means to convert the .brb into .svg files a user language program (ULP) was employed.

Upon arrival of the printed photolith film, the operation of cutting it into manageable masks began, either using scissors or a commercial CO2 laser with 30% power and 100% speed settings. A more in-depth explanation on the laser usage can be later found in Section 4.3.

Moreover the stages from the design to the printing of these photomasks and their cutting are outlined in Figure 4.1.

Figure 4.1: Steps involved in the production of photomasks, adapted from [8].

4.2 Assembling Flexible Hybrid Electronics

Only after the photomasks are designed and produced can the prototype's microfabrication process begin.

In this section a thorough look into the production process leading to the final functioning membrane will be given, including the parameters and conditions used in each stage of this microfabrication procedure.

4.2.1 Microfabrication Steps

Carrier Cleaning and Drying

Throughout this project the carriers used where $10 \times 10 \times 0.1$ cm common glass panes.

The cleaning and drying of such carriers is of paramount importance, especially prior to thin film depositions, since it eliminates any residual particles present on the carrier's surface, ensuring a greater uniformity and quality of the produced film, lowering its odds of presenting defects not related to the deposition, while also preventing the contamination of the samples. Therefore this step precedes all other microfabrication steps bellow-mentioned.

In order to equalise the initial conditions of the carriers they where all submitted to the same cleaning procedure. Which was comprised of:

1st- 10 minute acetone bath under ultrasounds;

2nd- 10 minute isopropyl alcohol (IPA) bath under ultrasounds;

3rd- Deionized water rinse;

4th- Carrier drying with a N_2 stream.

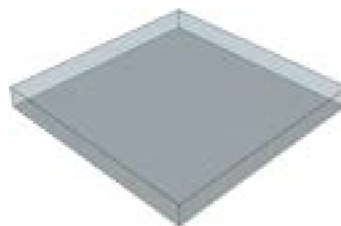

Figure 4.2: Example of a glass carrier.

Figure 4.2 represents a glass carrier, on which the sensing membrane will be produced.

Sacrificial Layer

In FHE production, one of its crucial steps is the thin film deposition, in order to obtain the desired substrates and layers.

Prior to the deposition of the parylene substrate layer a polyvinyl alcohol (PVA) sacrificial layer is added to the cleaned glass carrier. PVA is commonly used as a sacrificial layer because it is a water-soluble polymer, which in turn eases the separation of the flexible thin-film parylene membrane from the glass carrier once submerged in warmed water.

With the purpose of preparing a 500 mL, 5 wt. % PVA solution, a magnetic stirrer in a hot plate set to 90 °C and 700 rpm was employed. The dissolution process of the PVA in deionized water took a considerable amount of time since the polymer had to be added in small portions.

The resultant PVA solution was then utilised in the creation of the sacrificial layer. To do so the subsequent steps were followed in Departamento de Ciência dos Materias (DCM)'s clean room:

1st- Carrier placement on the spin coater, Figure 4.3;

Figure 4.3: DCM's spin coater equipment.

2nd- Distribution of the PVA solution over the carrier, just enough to cover its surface without bubbles;

3rd- Spin coating at 1000 rpm for 10 seconds followed by 20 seconds at 2000 rpm;

4th- Soft baking at 110 °C for 2 minutes (thin film annealing);

5th- Carrier cool down.

Figure 4.4 represents the spin-coated glass carrier with PVA. As has previously been mentioned, because the PVA layer is placed between the glass carrier and the subsequently deposited parylene substrate, once in contact with water it dissolves, freeing the parylene membrane.

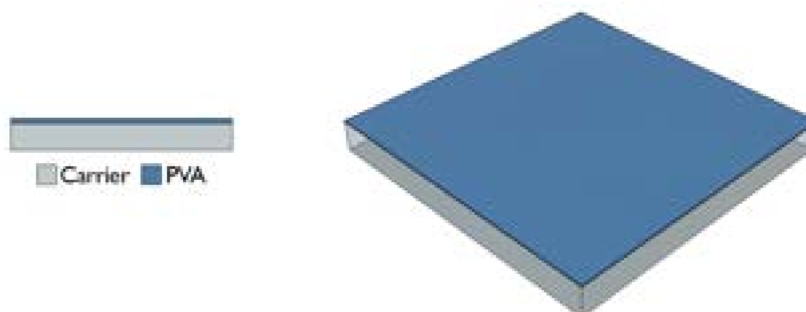

Figure 4.4: Glass carrier with the spin coated PVA layer.

Parylene Deposition - Substrate

In a series of successive depositions, the first step consists in the production of the parylene substrate through a CVD system, namely the Specialty Coating System Model PDS 2010 Labcoter 2, shown in Figure 4.5. This system not only enables the user to control the temperature in both the furnace and the vaporizer but also the pressure, by altering the process low alarm.

Figure 4.5: CVD system responsible for the deposition of parylene.

With the intention of creating a durable membrane able to withstand handling and the soldering of components, 7 g of parylene C dimer was placed in the vaporizer.

When not available, parylene C was substituted for a parylene N dimer, as a substrate, dielectric or even as an encapsulation layer. In these situations 8 g of parylene N were used to obtain the same thickness substrate film.

This deposition establishes some of the final membrane's mechanical robustness and flexibility. The several temperatures and pressures at which this process occurred are displayed in Table 4.1.

Table 4.1: Temperature and Process Low Alarm values used for parylene deposition.

Parylene	**Vaporizer** (°C)	**Pyrolyse Chamber** (°C)	**Deposition Chamber** (°C)	**Process Alarm** (Vaccum Units)
Type C	175	650	25.0	10.0
Type N	160	690	45.0	16.0

To accommodate the double layer electrical circuit and to act as a substrate, this deposition is the first out of four parylene depositions. Figure 4.6 is the depiction of the membrane status up to this stage.

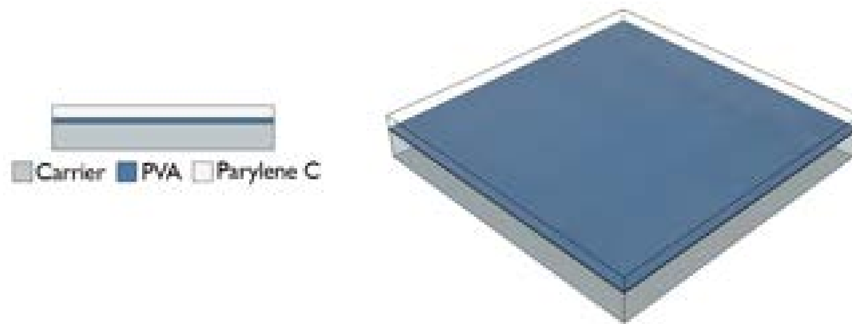

Figure 4.6: Deposition of a parylene layer to act as a substrate.

Copper Deposition

All electrical circuits presented in the different prototypes were patterned using copper and the wet etching technique.

The metal chosen to be applied throughout this project was copper. As a means to deposit this material onto the parylene substrate, the e-beam evaporation method was employed. This equipment, seen in Figure 4.7, is located at Center of Excellence in Microelectronics Optoelectronics and Processes (CEMOP)'s clean room.

Figure 4.7: CEMOP's e-beam evaporation system. A - General view of the equipment. B - Detailed view of the equipment's interior.

The deposition parameters applied can be observed in Table 4.2.

Table 4.2: Parameters used during the e-beam evaporation method.

	Copper
Density (g/cm^3)	8.96
Acoustic impedance ($\times 10^5$ g/cm^2.s)	20.2
Chamber pressure (mbar)	7.00×10^{-6}
Applied current (mA)	90.0
Deposition rate (nm/s)	6.00×10^{-1}
Expected thickness (nm)	300

After the deposition, the copper film is expected to be approximately 300 nm thick. In a later stage this will be the film in which the electrical circuit pattern will be defined via wet etching.

Figure 4.8 illustrates the deposited metal layer directly after the parylene deposition. Note that no previous treatment or preparation of the parylene film's surface was needed prior to any depositions in the microfabrication of the FHE.

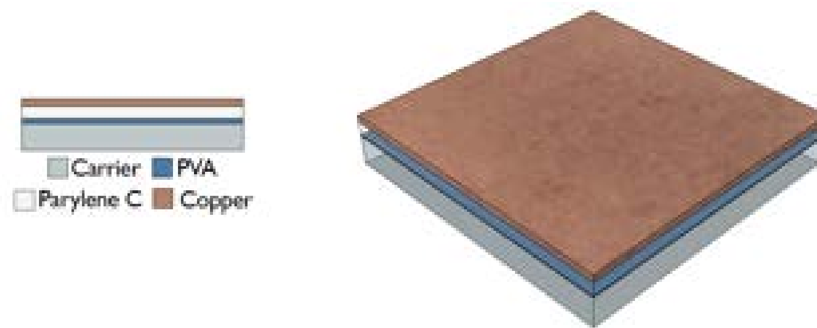

Figure 4.8: Deposition of the copper layer onto the untreated a parylene layer.

Photolithography

Subsequent to the copper deposition, photolithography is the next stage in the FHE membrane's microfabrication.

This process was performed in CEMOP's clean room using the spin-coater and the Karl Suss MA-6 mask aligner. Figure 4.9 shows these resources.

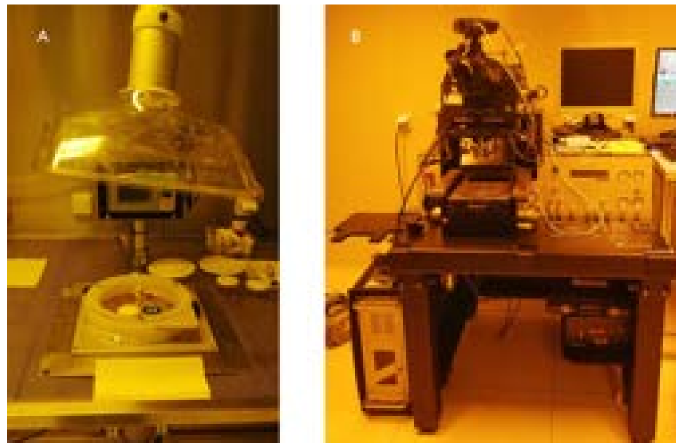

Figure 4.9: Equipment used during the photolithography process. A - CEMOP's spin coater. B - CEMOP's Karl Suss MA-6 mask aligner.

Here the positive photoresist (AZ6632) was utilised to create a photoresist layer of approximately 1.2 μm. To do so the subsequent steps were followed:

1st- Carrier placement on the spin coater;

2nd- Distribution of the photoresist solution over the carrier, just enough to cover its surface without bubbles;

3rd- Spin coating at 3000 rpm for 10 seconds followed by 20 seconds at 4000 rpm;

4th- Soft baking at 100 °C for 1 minute, to promote adhesion and remove solvents;

5th- Carrier cool down.

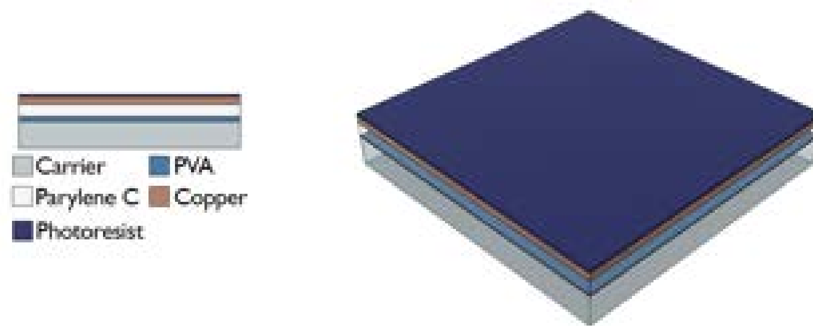

Figure 4.10: Photoresist layer spin-coated onto the metal layer.

Figure 4.10 illustrates the membrane status following the previously mentioned steps.

The next step in the photolithography process was the alignment procedure where the desired photomask is placed in between the UV light and the substrate, previously inserted into the Karl Suss MA-6 mask aligner. The mask and substrate are then aligned and exposed to 8 seconds of UV light.

Following this, the exposed photoresist becomes soluble once in contact with the developer (AZ 726 MIF), removing from the substrate the unnecessary photoresist and creating the desired pattern in the photoresist. To conclude, the substrate was submerged and rinsed in deionized water with the aim of stopping the development process and clean the substrate. The substrate was also dried under a N_2 stream. Figure 4.11 illustrates the final result of the photolithography process, in which a photoresist pattern of the sought after electrical circuit is visible.

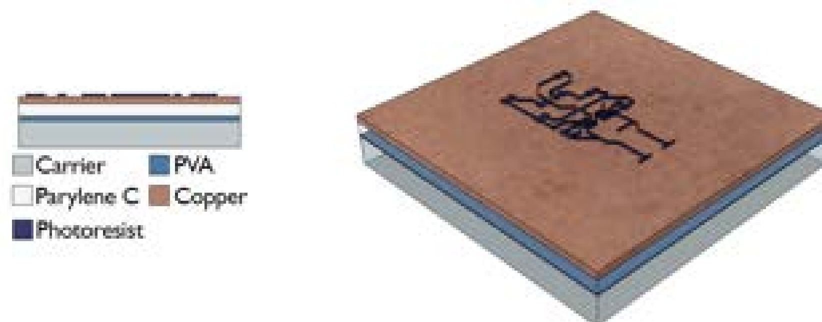

Figure 4.11: Patterned photoresist succeeding the development step. The pattern corresponds to one of the electrical circuits from the light emitting diode (LED) prototype.

Copper Wet Etching

As a result of the photolithography process, a photoresist layer remained in the areas where the copper has to stand, upon the wet etching procedure. Due to the photoresist's protection when the iron perchloride ($FeCl_3$) solution is applied, only the unprotected copper is dissolved, creating the wanted copper pattern.

For the 300 nm of copper deposited, a 1 : 1 $FeCl_3$ solution was used, taking between 1

to 2 seconds to complete this procedure. Note that as soon as the copper pattern is visible, the substrate should be immediately rinsed with deionized water to terminate the etching reaction by removing all traces of the solution.

To achieve a clean and photoresist free substrate, the substrate was immersed in acetone then placed in a laboratory shaker for 5 minutes, followed by a rinse with deionized water and another immersion but this time in IPA for 5 more minutes in the laboratory shaker, the cleaning was considered concluded once the substrate was submitted to a final rinse of deionized water and dried under a N_2 stream.

Figure 4.12 represents the copper pattern without the photoresist layer, detailing the electrical circuit and its components.

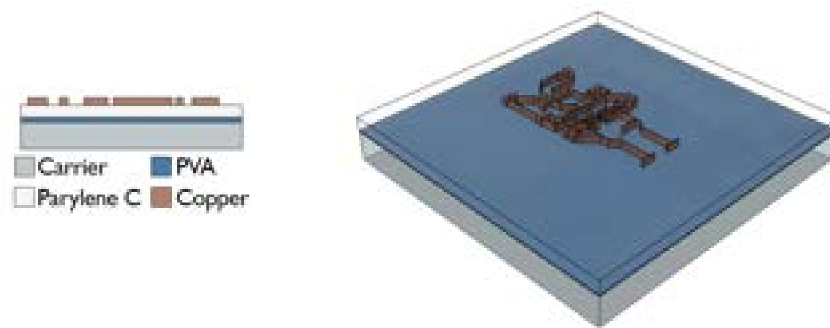

Figure 4.12: Patterned copper layer succeeding the wet etching step.

Parylene Deposition - Dielectric/Encapsulation

In order to encapsulate and protect the first layer of copper in the prototype from corrosion and wear, a second layer of parylene was deposited, Figure 4.13. This layer also enables double layered circuits, acting as a substrate for the next copper deposition and as a dielectric barrier between imminently overlapping circuit threads preventing the passing of current.

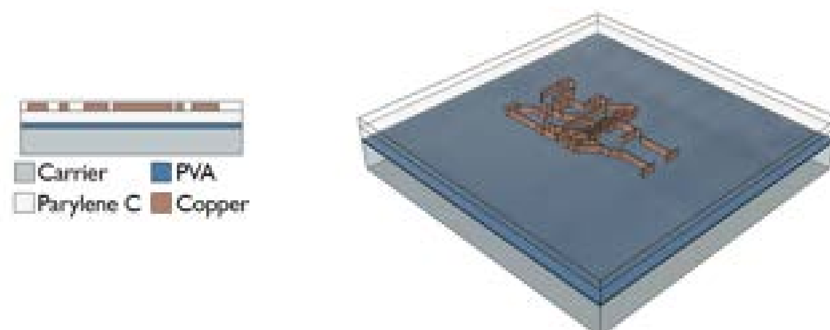

Figure 4.13: Deposition of the second parylene layer for dielectric purposes.

One singular difference sets this deposition apart from the aforementioned and it resides in the mass of parylene's dimer inserted into the CVD system, which for parylene C is 2 g and for parylene N is 3 g.

Dry Etching

All dry etching procedures were perform in CEMOP's clean room with the aid of a Minilock – Phantom RIE from Trion Technology, as shown in Figure 4.14, using O_2 plasma.

Figure 4.14: CEMOP's dry etching equipment.

Before executing the RIE, the parylene dielectric and encapsulation layer must possess the appropriate etching pattern to protect areas that should not be etched throughout the RIE process. To attain such pattern the above-mentioned photolithography process was used, given that it is the fastest and most efficient way to create patterns with the desired resolution.

Subsequent to the photolithography technique, the RIE process can begin. The parameters used in the device can be seen in Table 4.3:

Table 4.3: RIE parameters used during the dry etching process of the parylene films.

	Temperature	**O_2 flow** (ccm)	**RIE RF power** (W)	**Pressure** (Pa)	**Process time** (s)
Parylene	25.0	10.0	50.0	6,67	700 (**Type C**) 120×10^2 (**Type N**)

Figure 4.15 represents the final objective of the dry etching procedure on the parylene films which consists of opening areas (pads) where the SMDs will be soldered, opening viae, to connect the already deposited copper layer to eventually another and etching way the parylene from circuit extensions that will connect to a zero insertion force (ZIF) port.

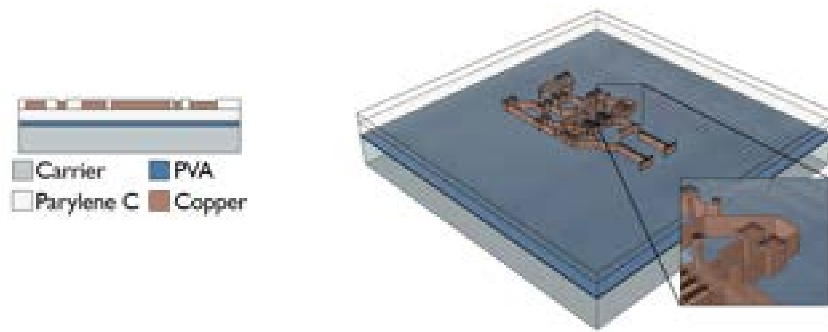

Figure 4.15: Etching of the parylene layer in specific areas.

Subsequent Steps

Since one of the goals of this project was the production of a double layered FHE membrane, the repetition of all preceding steps is required.

After the dry etching another copper layer was deposited, afterwards this layer was subjected to the photolithography process and wet etching. A parylene encapsulation layer was then deposited and exposed to the RIE technique. All the stages were performed exactly with the same conditions as the previously mentioned steps.

Figure 4.16 illustrates the double layered membrane ready for the solder of the SMDs and ICs. Note that after this step the glass carrier was cut, individualizing the several electrical circuit in the substrate, and facilitating the peel off step.

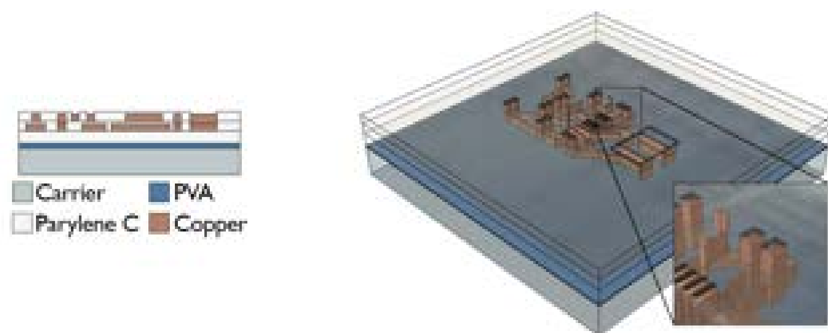

Figure 4.16: Membrane status after all microfabrication processes and prior to the soldering phase.

Once the components are solder to the membrane one final parylene encapsulation layer is deposited, in order to further protect and waterproof all SMDs and ICs. In the case of the prototype where a ZIF connector is soldered to the membrane, Kapton tape was applied in certain areas of it to prevent parylene deposition.

4.2.2 IC Integration

Solder Paste Placement

Succeeding the conclusion of all microfabrication steps, is time to place the solder paste on the pads and threads opened via the dry etching method, where the parylene was etched and the copper was exposed. The solder paste is used to fix SMDs and ICs onto the copper layer establishing an electrical contact between them.

During this project the lead-free low-temperature T3 mesh composed of Sn42 / Bi57.6 / Ag0.4 (ChipQuick) solder paste was used and together with the aid of an optical microscope situated at DCM, due to the small dimension of the pads, the deposition of solder paste was manually performed. Note that when applying the solder paste a very small amount was used on the center of the pad to prevent short-circuiting among pads and threads. Figure 4.17 illustrates the membrane status following the solder paste placement.

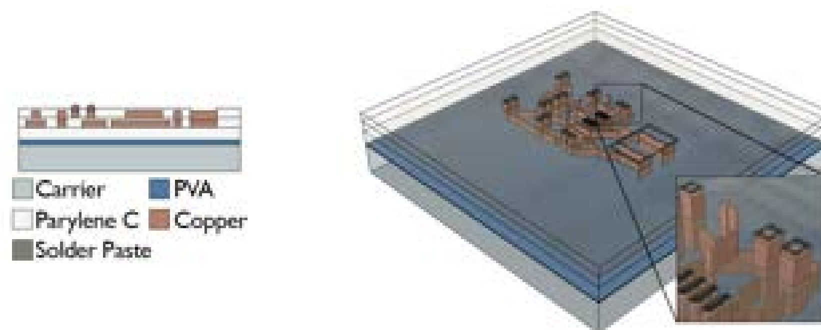

Figure 4.17: Solder paste deposition on the parylene areas opened by dry etching.

IC/SMD Placement

In order to position the SMDs and ICs on their correspondent pads in the electrical circuit, a tabletop pick and place equipment, the MPP1- Pick & Place Manipulator from Fortex, located at DCM was used. This equipment is intended for the manual assembling of PCB prototypes, where an assembling head fluidly and precisely moves on the X, Y and Z axis allowing to pick and place components, using an integrated vacuum switch. The rotation of components can as well be adjusted using a button on the manipulator's head, [94]. Figure 4.18 depicts the usage of such device.

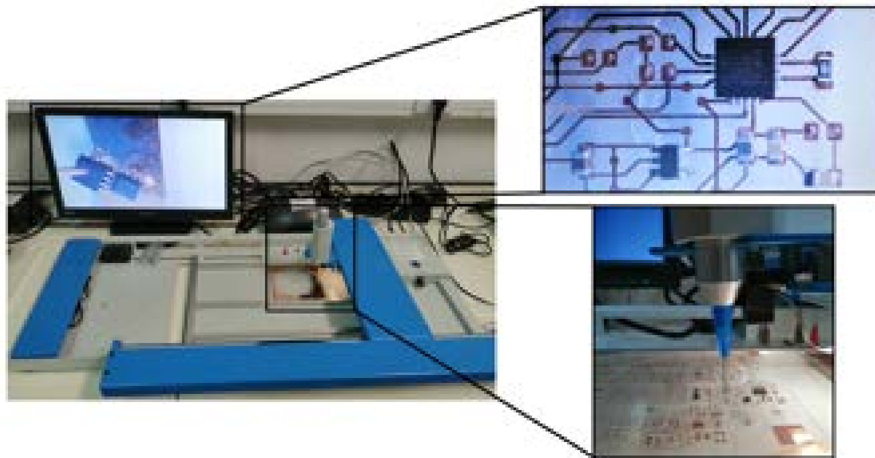

Figure 4.18: DCM's pick and place system in use.

Because of the equipment's effective lighting and vision systems (CCD camera displayed on an LCD monitor, [94]), components can be placed regardless of their size.

The ICs and SMDs of this project were placed on top of the solder paste as a means to integrate them into the electrical circuit. Following the placement of all the components the substrate is represented in Figure 4.19.

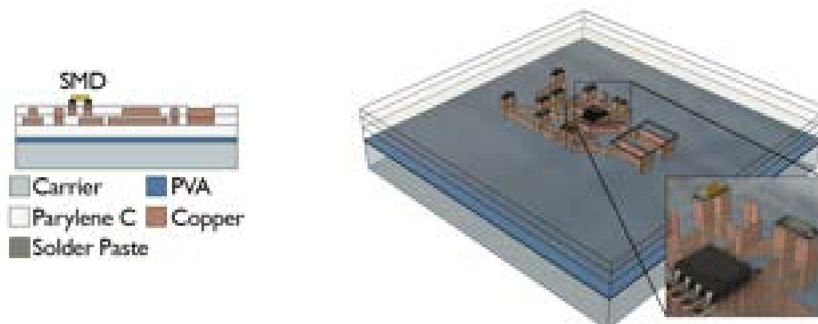

Figure 4.19: Placement of rigid ICs and SMDs over the solder paste.

Reflow Process

After the successful placement of the components on the membrane, it's necessary to fix them to the substrate enabling their integration to the electrical circuit. To do so, the solder reflow technique was deployed in which the reflow profile, suggested by the solder paste manufacturer, is uploaded to and replicated by an oven, more specifically the Infrared IC heater T-962 situated at DCM. Both the oven and the reflow profile used can be seen in Figure 4.20.

Figure 4.20: DCM's reflow oven with the time-temperature reflow profile used on screen.

Only after the substrate with the ICs was placed inside the oven and all parameters were dialed in, the reflow process was able to commence, subjecting the membrane to a rigorously controlled time-temperature profile, while also attaching and self-aligning the ICs and SMDs to its pads. Once concluded the substrate was left to cool down before its inspection under the optical microscope to check if the reflow process was successful by exhibiting shinny solder joints, no contact among solders and no short-circuiting within the prototype. If all these parameters are checked, the integration of rigid components in a flexible substrate is achieved.

4.2.3 Peel Off

Succeeding the successful integration of rigid ICs in the flexible membrane all left to do is to free the flexible membrane from its glass carrier. In order to do so, the peel off method was utilised, in which the PVA sacrificial layer is dissolved, decoupling the membrane from its carrier.

In the peel off method, deionized water was heated via a hotplate set at 70 °C. While waiting for water to warm up the sides of the glass carrier were scrapped to facilitate the contact between the water and the PVA layer. After one hour the substrate was submerged. Once the PVA layer is fully dissolved the conformable and FHE membrane is obtained, as seen in Figure 4.21. The FHE membrane was then left to air-dry for 8 hours, before being tested.

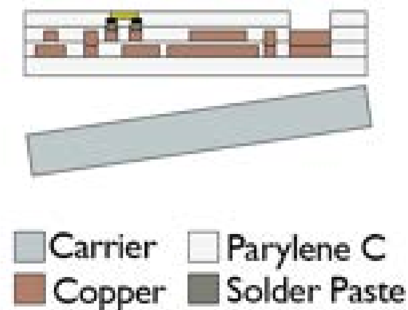

Figure 4.21: Final produced membrane without the glass carrier.

4.3 Other Production Techniques

Laser Cutting

Throughout the duration of this thesis the VLS 3.50 desktop laser by Universal Laser Systems, located at Centro de Investigação de Materiais (CENIMAT) in NOVA University Lisbon (Figure 4.22) was used.

Figure 4.22: CENIMAT's commercial laser.

This system is a pulsed cutting laser which produces a radiation beam with a wavelength of 10.6 μm and a maximum power of 50 W. To utilise this equipment, a vectorial RGB design must be imported into the laser-computer interface, responsible for controlling all settings in the laser, including encoding parameters such as speed (which determines the linear velocity of the laser gun motion, allowing the selection of a percentage of the system's travel rate), power (which enables the selection of a laser power percentage to be applied) and repetition rate on the color map of the design. The percentage speed and power parameter conversion to m/s and W can be seen in Annex I [95].

During this project, all designs were mocked up using the Adobe Illustrator CC 2020 software and then transferred to the laser software for cutting. Figure 4.23 represents one of these designs.

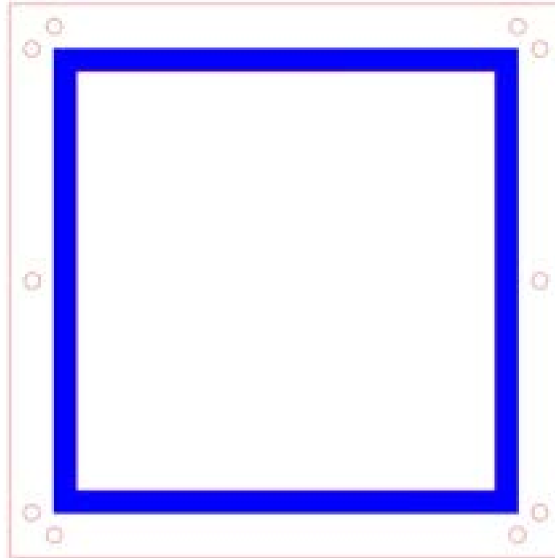

Figure 4.23: Example of a laser design used in this project.

This equipment uses two main modes, Rast where the laser beam is applied to the substrate in a series of pulses along one fixed axis sequentially, completing the design layer by layer, used for engraving and Vect mode, in which the system deploys laser pulses in a continuous movement following the vectorial lines of the design, used for cutting [95].

To fulfill the requirements of this project both of the previously mentioned modes had to be put to use. To do so the red lines, seen in Figure 4.23, encoded a Vect mode using a 100% power rate and a 0.5% speed rate, meanwhile, the blue square encoded a Rast mode using a 80% power rate and a 15% speed rate.

3D Printer

Another technology explored during this project was 3D printing. The experimentation of this technique was made possible by the use of PLA filament in a Creality Ender 3 printer with a 0.4 mm nozzel diameter (Figure 4.24) located at DCM.

Figure 4.24: DCM's 3D printer.

Similarly to the laser, all designs were created using the Adobe Illustrator CC 2020 software, however in this case the file is required to be saved in .svg format so it can be uploaded into Fusion 360®, also an Autodesk® software. In this software all the alterations necessary to transform a 2D drawing into a 3D object occur. Following these changes, the .svg file is saved in a standard triangle language (.stl) format, ready for transfer to the Ultimaker® Cura software responsible for the model's slicing. This final file is saved in .gcode form which is then used by the 3D printer to execute the print. These steps can be seen in Figure 4.25.

Figure 4.25: Steps involved in the production the 3D carrier support.

4.4 Characterization Techniques

4.4.1 Superficial Characterization

With a focus on evaluating the dimensional particularities during the different stages of membrane's microfabrication process, some techniques were used. Such as the measurement of the film's thickness and the image amplification of the electrical circuits.

Profilometer

For the purpose of measuring the thickness of the produced films a Dektak IIA surface profile measurement system from Sitek Process Solutions, found in DCM's clean room, was the primarily used device. The AMBIOS XP-200 Stylus, located at CENIMAT, which operates similarly to the previously mentioned device, was also used. Figure 4.26 shows both of these devices.

Figure 4.26: Profilometers used throughout the superficial characterizations. A - DCM's Dektak IIA surface profile measurement system. B - CENIMAT's AMBIOS XP-200 Stylus profilometer.

This measurements are made electromechanically by moving the sample beneath a diamond-tipped stylus. The stylus moves in the Z axis until it comes in contact with the sample. Once in contact, the sample is moved (Y axis) beneath the stylus according to a user-programmed scan length and speed. Surface variations cause the stylus vertical translation, an electrical analog signal proportional to its position change is created and then converted to a digital format, providing the film's profile. Such signal can be displayed or manipulated easing its analysis [96]. In this way the thickness of each of the deposited films, both metallic and parylene (despite being a polymer) can be measured.

These measurements were performed with the parameters shown on the following Table 4.4:

Table 4.4: Profilometer parameters.

	Length (mm)	**Speed** (mm/s)	**Range** (μm)	**Stylus Force** (mg)
Dektak IIA	1.00	MEDIUM	AUTO	-
AMBIOS	2.00	1.00×10^{-1}	10.0	1.00

Optical Microscopy

In order to closely inspect the produced electrical circuits, a optical microscope was employed, namely the Olympus BX51, Figure 4.27, located at CENIMAT.

Figure 4.27: CENIMAT's Olympus BX51 optical microscope.

This device permitted the examination of the conducting lines, pads, through holes, overlapping treads and soldered components in the electrical circuits ensuring that all parts were correctly placed and there were no undesirable short-circuiting. The microscope was also used to take measurements of the copper tracks and pads, as well as to photograph the circuits for later analysis.

4.4.2 Electrical Characterization

As a means to analyse the electrical properties of the developed thin film circuits, some techniques were deployed. For instance the measurement of the resistivity value present in the deposited metal and continuity tests were preformed using a digital multimeter to ensure an accurate resistance assessment.

Four Point Probe Method

A material's resistance (R) can be obtained by measuring the current that flows upon applying a voltage drop on its terminals. This resistance depends both on the resistivity (ρ) of the material, an intrinsic property, and on the physical geometry of the research subject [97]–[99]. The following equation 4.1 demonstrates this:

$$R = \frac{V}{I} = \rho \times \frac{L}{A} = \frac{\rho}{t} \times \frac{L}{W} = R_S \times \frac{L}{W} \tag{4.1}$$

where L symbolises the length of the material, A the material's area, W the width of the subject, t its thickness and R_S represents the sheet resistance of the material in $\Omega/\square$.

The four-point-probe technique is commonly used to obtain semiconductor's resistivity. It is an absolute measurement, without recourse to calibrated standards, nondestructive and useful for either bulk or thin film specimens [97]–[99]. To apply this method, the

Jandel 4-Point Probe System, located at CEMOP, was employed. Figure 4.28 presents this device and a illustrative representation of its operation principles.

Figure 4.28: Representation of the four-point-probe method. A - CENIMAT's Jandel 4-Point Probe System. B - 4-Point Probe operation principles.

Like its name suggests, this device uses four equally spaced and aligned probes, by a distance of s = 1 mm. When these come in contact with the sample's surface a constant electrical current (I) is streamed along the sample through the two outermost probes. If the material has resistance, the flowing current will be subjected to a voltage drop, this voltage change (V) is then measured between the inner probes and presented on the equipment [97]–[99]. When this value is obtained, the resistivity of the material can then be calculated.

4.4.3 Structural Characterization

With the aim of analysing the structural properties of the produced FHE membranes, X-ray diffraction (XRD) technique was performed using the X'Pert PRO MRD system from PANalytical availabe at CENIMAT, seen in Figure 4.29.

Figure 4.29: CENIMAT's X'Pert PRO MRD system responsible for the XRD method.

X-ray Diffraction

XRD analysis is an effectively used method to study a material's crystallinity, based on the interaction between a monochromatic X-ray beam and the atoms/molecules of the sample under investigation through Rayleigh scattering [33], [100].

These scattered waves either interfere constructively or destructively creating a wave-field dependent on the type and relative positions of the atoms present in the lattice. Constructive interference only occurs when X-ray waves interact with the crystal planes from the sample in specific Bragg's Law obeying angles resulting in diffraction phenomena. Bragg's Law follows equation 4.2:

$$2d\sin(\theta) = n\lambda \tag{4.2}$$

where d is the spacing between crystal planes, θ is the angle between the diffracted wave and the atomic planes, n is the order of reflection (an integer number) and λ is the wavelength of the incident X-ray beam [33], [100].

Different θs will result in distinct diffracted beam intensities, in other words, by changing the incident angle, Bragg's Law is fulfilled for different spacings. Making it possible to obtain an X-ray diffraction pattern, commonly known as a diffractogram, exclusive to each substance, acting as a material's fingerprint. This pattern is obtained when the diffracted intensities is plotted versus the detector's angle (2θ) [33], [100].

Through referenced patterns accessible in data bases, such as the International Centre for Diffraction Data it is possible to identify the composition of samples by comparing the position and intensity of diffractogram peaks present in these [33], [100].

5 Results and Discussion

Initially this chapter offers an in-depth analysis of the procedures and techniques applied in the fabrication of the developed prototypes, including a simpler LED prototype, along with a perspective on the faced hardships and created solutions throughout this thesis. Lastly the performance of these prototypes will also be presented and discussed.

5.1 Circuit and Photomask Design

Considering that this thesis has the main objective of developing flexible and conformable double layered hybrid sensing membranes for temperature monitoring, several circuits were designed to achieve this purpose.

As a means to analyse all microfabrication techniques, to corroborate the flexible double layered hybrid sensing membrane theory and to accomplish temperature sensing, three different electrical circuit prototypes were created. From this point onward each prototype will respectively be referenced as LED, MAXIM and PT100. All of these prototype's schematics and circuits can be found in Appendix A.

As observed in Appendix A.1, prototype LED is composed of three distinct circuits entitled PiscaPisca, 2Via and 6Via. Each of these electrical circuits was designed to have the same simple function of lighting LEDs on and off. In the case of PiscaPisca, its LEDs frequency is regulated according to the resistors utilized (39 and 68 kΩ) and a NE555D timer in monostable mode, whereas the power supply is established by an Arduino Uno. On the other hand, the Arduino Uno is responsible for providing 2Via and 6Via's power and LED frequency, based on the uploaded code (also developed specially for this occasion), the only difference among these two circuits is the amount of viae and tracks present on the second metal layer. As the name suggests the 2Via circuit only possesses two through holes whilst the 6Via circuit has six viae. All of these circuits required the design of extended tracks which would establish the connection between the flexible membrane and the Arduino Uno microcontroller.

Figure 5.1 represents the MAXIM prototype whose circuit is an adaptation from the MAX30205 Human Body Temperature Sensor Evaluation Kit's temperature sensor PCB.

Since the main goal was the transition from a rigid PCB to a flexible and conformable format, all components remained unchanged including their 0402 size code, exclusively their orientation and positioning varied, with the purpose of accommodating new elongated tracks for the membrane's coupling to a ZIF connector, vital for its interfacing with the rest of Maxim's rigid hardware.

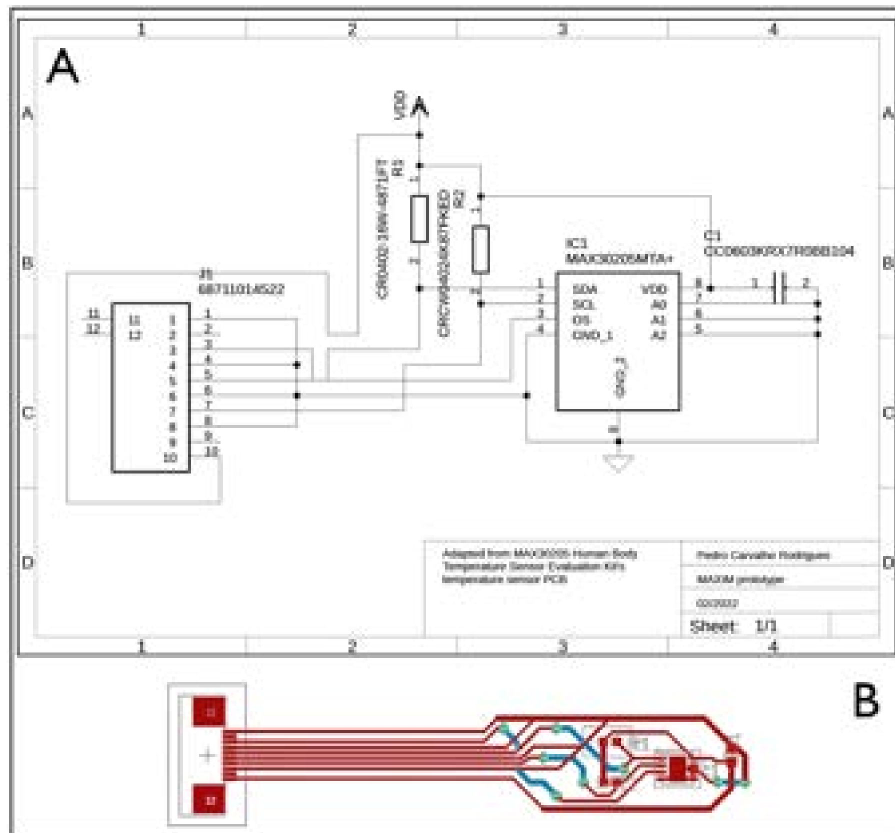

Figure 5.1: MAXIM prototype's circuit design. A - Schematic adapted from the Maxim's rigid temperature sensor PCB. B - Electrical circuit created for this prototype.

The PT100 prototype is exhibited in Appendix A.3, which similarly to the MAXIM prototype is the conversion of the Adafruit MAX31865 RTD PT100 Amplifier from its rigid format to a flexible PCB. As before, all ICs and SMDs were unaltered and an effort was made to reduce the number of viae, accompanied by the decrease in tracks on the second metal layer. However, because the PT100's sensor is required to communicate to the membrane, personalised pads were also created to be inserted in a ZIF, subsequently attached to this sensor. Extended tracks were also constructed to make the interface between the prototype and the Arduino Uno possible, this microcontroller is accountable for the temperature reading. These changes were performed in order to simplify the circuits and ease their transfer to the correspondent physical metal layers.

Concerning the creation of photolith photomasks for their later use in the photolithography process, due to the fact that throughout this work the photoresist used was either the positive photoresist AZ6632 or the AZ3012, a negative mask (transparent background with

black pattern) had to be deployed to pattern the metal layer, creating the desired electrical circuit. Meanwhile, with the aim of opening areas in the parylene film, positive masks (transparent pattern with black background) had to be applied prior to the RIE process, creating future contact points between metal layers of the circuit (viae) after the dielectric layer. In addition, these masks were also used to create openings where the solder of ICs and SMDs on the electrical circuit was possible, subsequent to the encapsulation layer. These photomasks were also created to fit a 10 × 10 cm glass carrier, since all prototypes used such carriers as the foundation for the flexible membrane. Figure 5.2 displays the negative and positive photomasks created for prototype LED, all other photomasks can be found in Appendix B. One other important detail in the design of these photomasks was to mirror them before printing, because during the photolithography phase these are flipped so their paint is as close to the substrate as possible ensuring a better resolution.

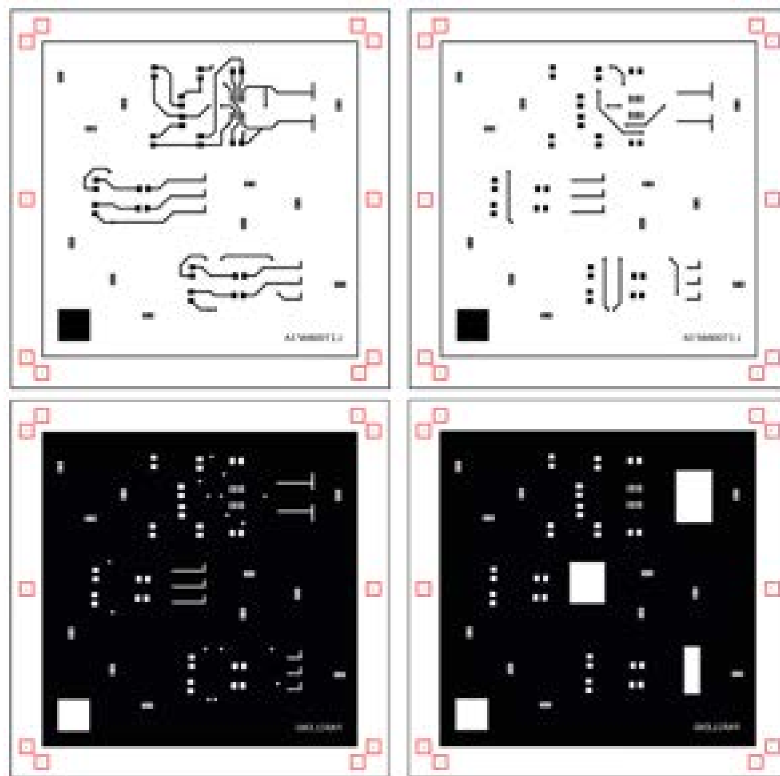

Figure 5.2: Photomasks used for the LED prototype. The top two were used to pattern the first (left) and second (right) metal layers and the bottom two were used to pattern the openings in the parylene during the dry etching of the dielectric (left) and the encapsulation layer (right).

Throughout this thesis several iterations of the photomasks were produced in order to refine aspects of the original design. Some changes include the thickening of tracks, the enlargement of pads and viae as well as the realignment of circuits. Despite these the most significant modification was the introduction of the black outlined circles, marked in red (Figure 5.2), which aided in the manual alignment of the photomasks, later explored in Section 5.4.

5.2 Manual Mask Alignment System Development

Owing to malfunctions, in CEMOP's mask aligner, all photolithography had to be adapted to the DCM's clean room, where no alignment equipment existed. To surpass this hurdle, the alignment of the photomasks and the substrates during the photolithography had to be done manually, thus a manual mask alignment system was developed.

The aforementioned manual alignment system relies on two main elements, the first one being the prototype's photomasks, which undertook some redesigning and were scaled down to an A3 size, in order for them to fully fit in the desktop laser, mentioned in Chapter 4.3. Black outlined circles and squares, seen in Figure 5.2, were also added to the photomasks as a means to help in the positioning of the laser over the photolith film. These adjustments not only guaranteed the correct cutting of holes on the photomasks where the circles were designed, but also stipulated that if any misalignment was to happen all photomasks from the same prototype remained aligned with each other, disregarding the overall misalignment. The cut holes served the purpose of attaching the photomasks, to the second element of the manual alignment system.

Additionally to the modified photomasks, a carrier support was designed and manufactured with the intention of holding a 12×12 cm photomask and a 10×10 cm glass carrier as aligned and close together as possible allowing for a better resolution in the photolithography phase, and a higher quality alignment between layers. To fabricate this support two types technologies were researched: laser cutting and 3D printing, these are thoroughly analysed in Chapter 4.3.

When it came to laser cutting, to achieve the desired support, a 7.7 mm acrylic pane was cut using a commercial CO2 laser. The final iteration of this support consisted of a picture frame design, comprised of two distinct parts, a carrier holder which would support the carrier in a 1 mm ledge, and a frame that would magnetically attached to the base, holding the photomask and the carrier in place.

Once all cuts and engraving on the acrylic were concluded each part had to be cleaned and magnets were then glued with super glue to the orifices created. The final result can be seen in Figure 5.3.

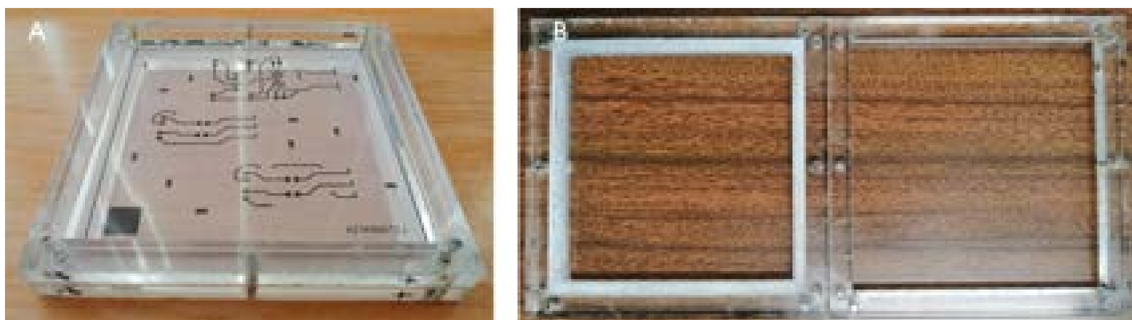

Figure 5.3: Final result of the carrier support manufactured via laser technology. A - Exhibits an assemble carrier support. B - Shows the disassembled state of the support.

Another technology researched in the fabrication of the aforementioned supports was 3D printing. In this case, several test prints had to be performed in order to obtain an acceptable support with the desired measurements. Similarly to the laser, this 3D printed support had a picture frame design composed of two parts which fit together tightly.

Following the print, a thorough cleaning of the parts was performed before its terminal use as a carrier support. The final result can be seen in Figure 5.4.

Figure 5.4: Final result of the carrier support manufactured via laser technology. A - Exhibits an assemble carrier support. B - Shows the disassembled state of the support.

Ultimately the laser technology was chosen over 3D printing due to time restrictions. Although thorough cleaning and testing was performed to the 3D printer, this equipment required further tuning and testing in order to achieve the level of precision looked for in this build, associated with this the readily availability and precision of the laser cutting technology made for good argument when deciding on which method to use.

5.3 Parylene Deposition

The microfabrication process of the physical prototypes succeeded the creation of the circuits and photomasks.

The parylene substrate, serves as the foundation on which all other layers and components will rest. On this basis, 7 g of parylene C dimer were deposited over the PVA layer using a CVD system.

In order to assess the thickness of the parylene substrate, the profilometry method referenced in Chapter 4.4.1 was used. Figure 5.5 depicts one of the thickness measurements taken in each prototype. Circled in red is the value of this measurement, the x-axis represents the scanning range of the measurement and y-axis represents the parylene's height. The surface variation of interest is bounded by the red M and R lines, all irregularities outside this area represent undesired particles and impurities on the substrate's surface. The measured thickness of the parylene substrate throughout the prototypes varied between 3.73 μm and 4.62 μm.

Additionally to serving as a substrate, parylene C was also used as a dielectric, in an

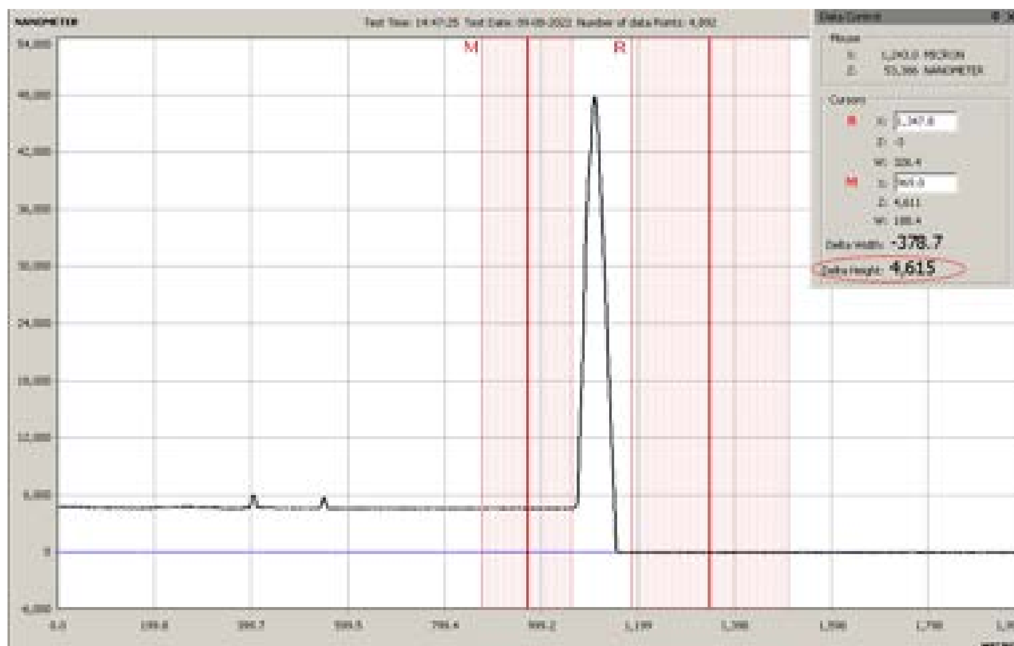

Figure 5.5: Thickness measurement of the parylene substrate layer, using the profilometry method.

effort to act as a current barrier between overlapping circuit threads, preventing short-circuiting among metal layers. As well as encapsulation of the prototypes, with the purpose of protecting the metal layers from abrasion and corrosion, it also aided in the preservation of the soldered components to the membrane providing water-proofing and better adhesion. The thickness measured amidst dielectric and encapsulation parylene C layers ranged from 1.36 μm to 1.65 μm.

A shortage in the parylene C supply led to the use of parylene N dimer in some of the prototypes, both as a substrate, dielectric and encapsulation layer. This conversion also meant several attempts at parylene N deposition, since it required plenty of tinkering with the pressure and temperature settings of the CVD system until an acceptable deposition was achieved.

Table 5.1 summarizes the types of parylene used, their roles and the average thickness's measured in the profilometers.

Table 5.1: Thickness measurements of the several parylene deposited layers.

Parylene Type	**Role**	**Dimer Mass** (g)	**Range Thickness** (μm)
C	Substrate	7.00	3.73 to 4.62
	Dielectric	2.00	1.36 to 1.57
	Encapsulation	2.00	1.40 to 1.65
N	Substrate	8.00	3.42 to 4.50
	Dielectric	3.00	1.12 to 1.59
	Encapsulation	3.00	1.22 to 1.64

5.4 Copper Deposition and Patterning

Copper was deposited using the e-beam evaporation method onto the untreated surface of the parylene thin film. This metal layer will retain the circuit pattern including pads, threads and viae. Figure 5.6 represents the deposition of a copper layer on a substrate. This was the chosen metal because of its relatively low cost, availability and reliability since there was no need for a metal with specific characteristics and previous studies favoured copper as the base for their electrical circuits.

Figure 5.6: PT100's electrical circuit etched onto the copper layer.

In order to evaluate the copper's presence and to estimate its crystallinity the XRD technique was performed with a range of 2θ between 10° and 150°, resulting in the diffractogram presented in Figure 5.7. By analysing the diffractogram of the deposited copper it is possible to distinguish peaks at angles of $2\theta \approx 14°, 43°, 50°, 74°, 89°, 95°, 136°$.

The first peak, according to literature [101] is consistent with parylene C's crystalline plane (0 2 0) of its monoclinic structure, which is understandable since the copper film was deposited over a parylene substrate. However when comparing the remaining peaks in Figure 5.7 with copper's reference diffractogram, provided by the ICDD card file number

00-004-0836, it is possible to associate them to the diffraction planes characteristic of copper's cubic structure, identified in Figure 5.7. Hence confirming the successful copper deposition on the parylene substrate.

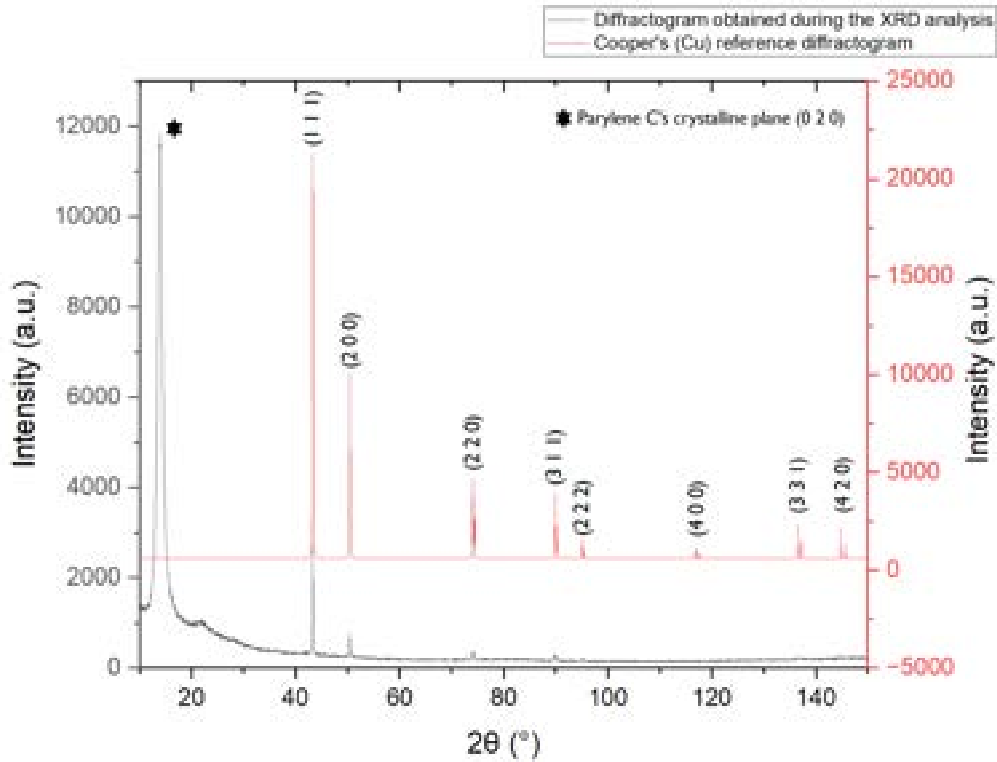

Figure 5.7: Comparison between the diffractogram from XRD analysis of the prototype's substrate (in black) and the reference diffractogram for copper (in red).

In order to verify the copper layer's thickness, the profilometry technique, referenced in Chapter 4.4.1, was used. Several measurements in different prototypes proved that the copper layer's thickness ranged from 253 nm and 358 nm.

Considering that copper circuitry is one of the focal points of this thesis, in addition to measuring the deposited copper layer's thickness, studying its resistivity (ρ) was an appealing idea. To do so the four point probe method, referenced in Chapter 4.4.2, was employed in one prototype whose copper layer possessed a thickness of 358 ± 10 nm. Once the device was in contact with the copper film a constant current of 9.00 mA was forced through the two outermost probes, the equipment's two inner probes then measured a voltage drop of $1.00 \times 10^{-1} \pm 0.01$ mV.

Because the deposited copper film is considered a thin film, since its thickness (t), is inferior to the spacing between probes (s, which in this equipment equals to 1 mm) divided by 2, in other words $t \leq \frac{s}{2}$, it is necessary to add a $\frac{\pi}{\ln(2)}$ correction factor to equation 4.1, which with these alterations the following equation is achieved:

$$R_S = R \times \frac{\pi}{\ln(2)} \tag{5.1}$$

By replacing all variables in equation 5.1 with the acquired data,

$$R_S = \frac{1.00 \times 10^{-4}}{9.00 \times 10^{-3}} \times \frac{\pi}{\ln(2)} <=> R_S = 5.00 \times 10^{-2} \pm 0.01\Omega/\square \quad (5.2)$$

the deposited copper's sheet resistance, R_S, is obtained.

In order to achieve the resistivity value of the deposited copper, equation 4.1 is adapted and fitted with all gathered data, attaining a resistivity of $1.80 \times 10^{-8} \pm 0.2 \times 10^{-8}$ Ωm.

When comparing the deposited copper's resistivity ($\rho = 1.80 \times 10^{-8} \pm 0.2 \times 10^{-8}$ Ωm) with copper's theoretical resistivity ($\rho_T = 1.68 \times 10^{-8}$ Ωm), it is possible to say that the resistivity of the deposited copper although slightly higher, matches with the copper's reference resistivity. This difference maybe due to some oxidation of the metal layer from its exposure to air in between microfabrication processes or from some impurities on the deposited metal.

Owing to the fact that the copper layers are deposited as thin films occupying the entirety of the substrate's surface, these then need to be patterned into the desired electrical circuits, specific to each prototype. The first step in this patterning involves the photolithography method, reviewed in depth on Chapter 4.2.1.

Initially this procedure took place at CEMOP's clean room where the spin-coater and the mask aligner are located. This last equipment ensured the alignment between layers, preventing predicaments associated with the misalignment of photomasks.

Owing to malfunctions, in the mask aligner, all photolithography was adapted to the DCM's clean room. Considering no alignment equipment existed at DCM's clean room, this procedure had to be performed manually. To surpass this hurdle the manual alignment system mentioned in Section 5.2, was developed. Aiding in the alignment between substrates and photomasks.

Considering the photoresist's UV exposure, this exposure time also had to be adapted to a DCM's set of UV lights. Whose activation for approximately 30 seconds, successfully resulted in the patterning of the photoresist once in contact with the AZ726 MIF developer.

5.5 Wet and Dry Etching

As a result of the photolithography process, a patterned photoresist layer is left on the surface of the previously deposited copper. The photoresist will act as a protective layer for the copper underneath, protecting it throughout the wet etching procedure. Where an copper etching solution, iron perchloride ($FeCl_3$), is applied over the substrate, dissolving the copper which was unprotected by the photoresist layer and creating the desired metal electrical circuit. Figure 5.8 exhibits some outcomes of the wet etching technique.

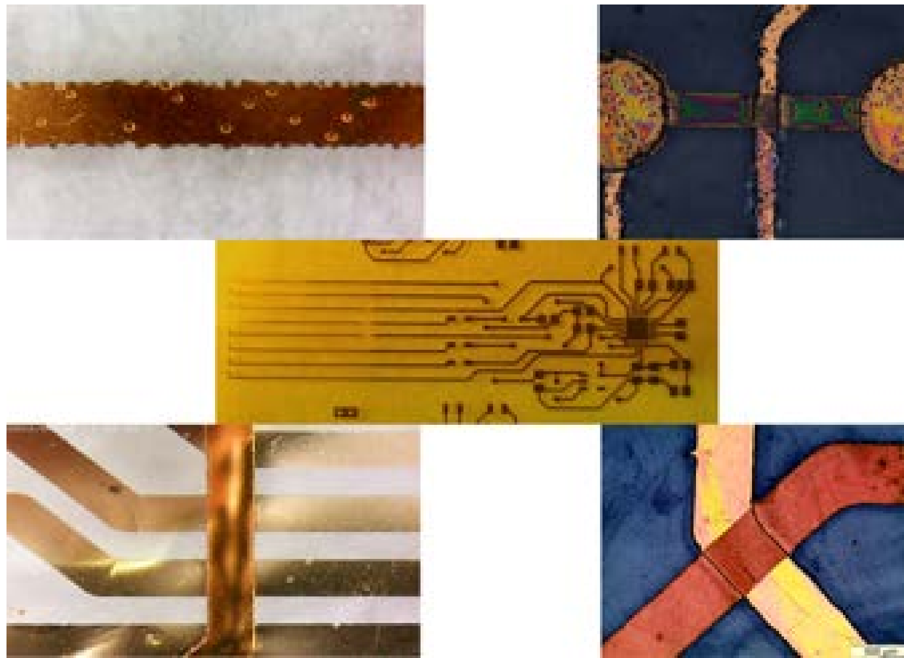

Figure 5.8: Examples of the by-products of the wet etching method.

Initially the wet etching procedures, used a 1 : 1 $FeCl_3$ solution and took 1 to 2 seconds to complete, however this method proved to be relatively difficult to control, resulting in the unwanted removal of certain copper areas regardless of being covered by the photoresist layer. Figure 5.9 demonstrates this occurrence.

Figure 5.9: Unwanted metal removal due to the over-etching of the copper layer.

To better control the wet etching process a 5 : 1 dilution of the $FeCl_3$ solution was crafted, which when used, extended the overall duration of the method to approximately 9 to 10 seconds.

In spite of being a reasonably simple step, some noticeable problems appeared after its completion. Whilst analysing the LED prototype, it was possible to observe several pads and viae detached from the main circuit, belonging to the first copper layer. Figure 5.10 shows some of these events.

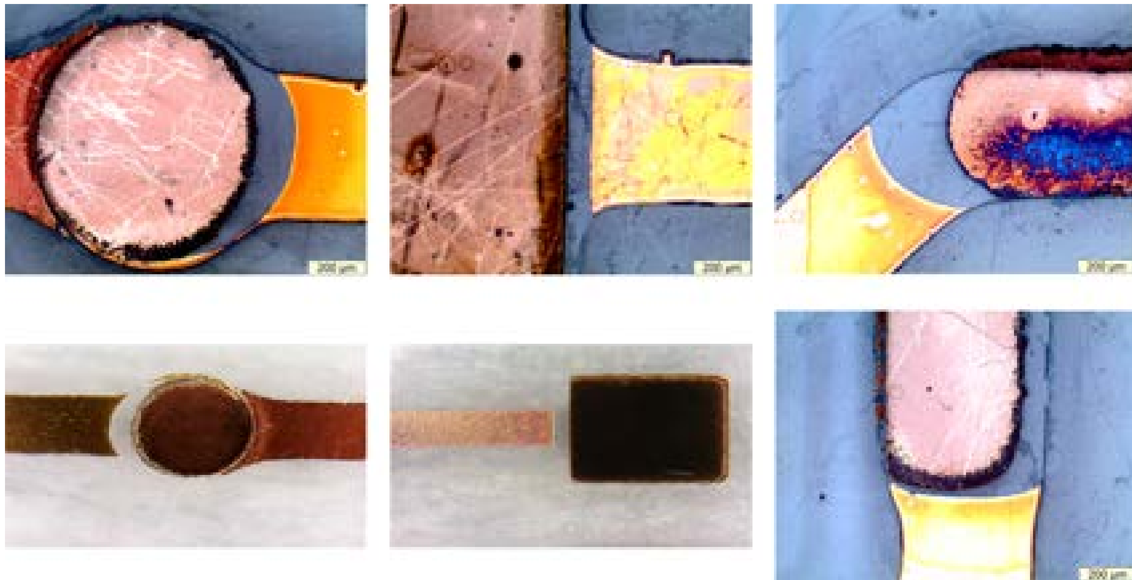

Figure 5.10: Noticed pads and viae detached from the main circuit.

A possible explanation for these events lays on a problematic alignment between the photomasks and the substrate. This situation could have happen in two occasions, either upon the parylene's photolithography phase of the first dry etching procedure or during the second copper layer's photolithography phase since both were performed using the manual alignment system created, prior to the second wet etching process. A misalignment in these stages would cause a deviation of the photoresist protective pattern once exposed to the UV light. The first case, would result in the dry etching of a deviated pattern in the parylene layer, the effects of this wrongful etching, if all other microfabrication steps went accordingly, would extend to the wet etching of the second copper layer unprotected by the parylene creating gaps among the first and second copper layers, Figure 5.11 A. On the other hand, if the misalignment occurred during the second copper layer's photolithography phase, the exposed unprotected copper from the first layer would be etched away during the wet etching process, leaving a gap between the second copper layer and the copper layer beneath, making the passing of current impossible, Figure 5.11 B. A schematic of these events can be seen in Figure 5.11 to better understand the issue at hand.

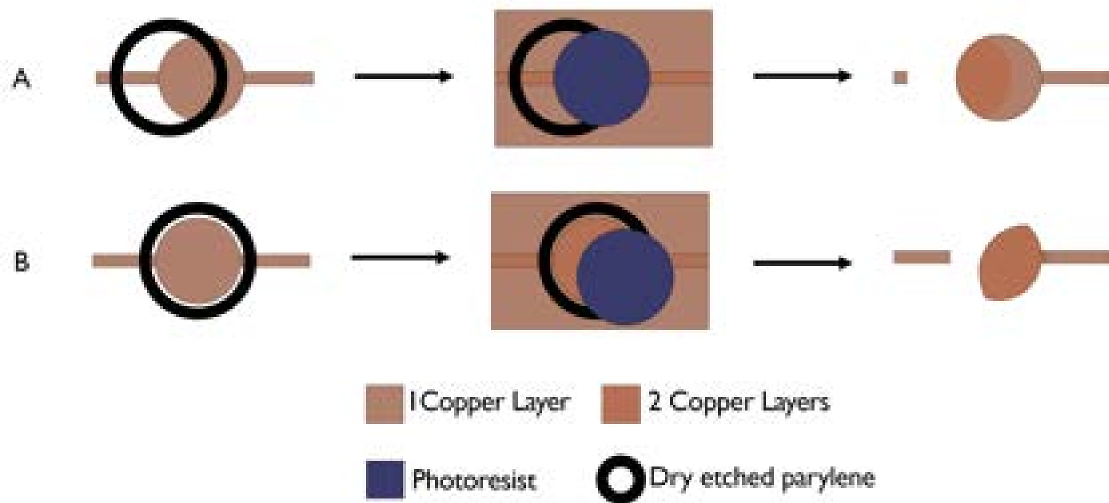

Figure 5.11: Schematic of the possible explanations for the detached pads and viae. A - Represents the situation if the issue occurred during the photolithography phase of the first dry etching procedure. B - Represents the situation if the problematic event occurred during the second copper layer's photolithography phase.

In an attempt to surpass this challenge, silver paint was used to connect the two copper layers. To do so, firstly, an enlarged pattern of the pads and viae was cut into PEN film with the aid of the laser addressed on Section 5.2. Once cut, the PEN film was aligned to the existing pads on the substrate and attached to the carrier with Kapton tape as close as it was possible to the substrate's surface.

The next step in this attempt involved the dry etching process, where all prior preparation made possible the etching of larger parylene areas around the pads which were not covered with PEN film, revealing the copper tracks belonging to the first layer near the desired pads and viae as shown in Figure 5.12 B.

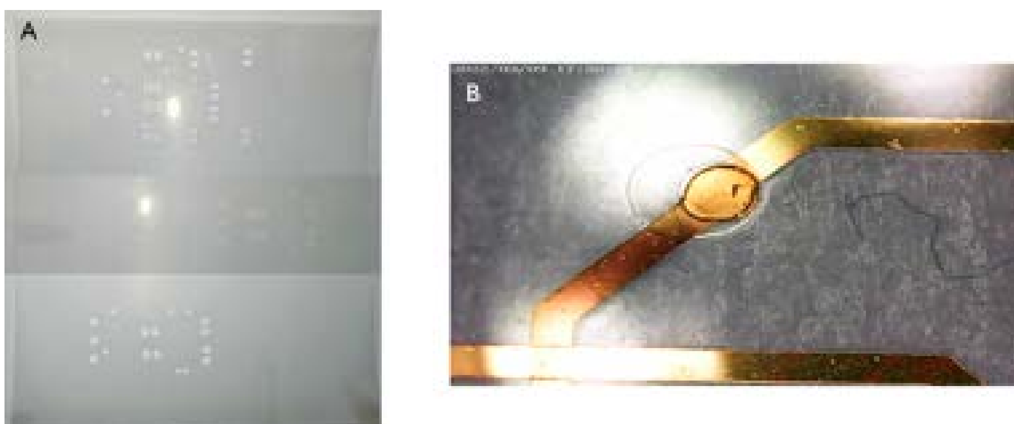

Figure 5.12: First step in the solution for the detached pads and viae. A - Patterned PEN film used for the LED prototype. B - Result of the dry etching process using PEN film as a physical mask.

To make the connection between the exposed first layer and the recently deposited copper layer a Leitsilber 200 Silver Paint from TED PELLA, INC was applied in the areas which revealed the previously mentioned problem. The membrane's final appearance after this effort can be seen in Figure 5.13. A multimeter was used to confirm the passing of current through the reformed circuits.

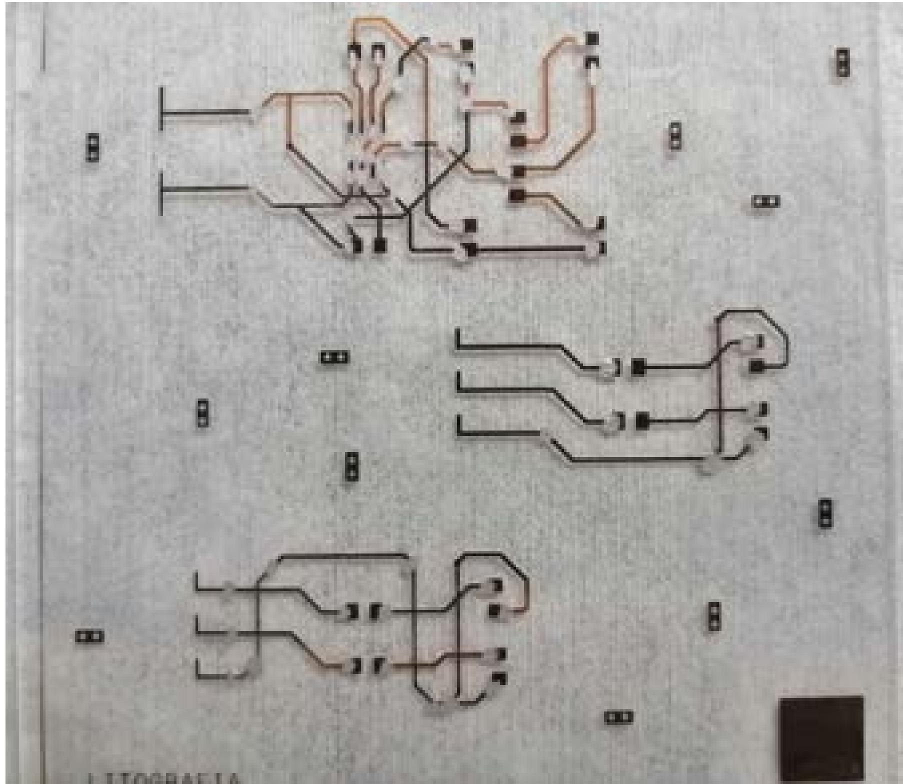

Figure 5.13: LED prototype's circuits after the deposition of the silver paint on the required areas.

The dry etching procedure was again implemented, to overcome the wrongful encapsulation of the sensor connecting pads, in PT100's prototype, only noticed once all components were soldered and encapsulated. In order to do so, the same strategy used in the LED prototype was enforced. At first the pattern of these pads was cut into PEN film as well as a square where all soldered ICs and SMDs could fit. After that, as aforementioned, the PEN film was aligned to the desired pads and components on the substrate and attached to the carrier, the previously cut square was covered with aluminium foil, enabling a closer interaction between the PEN film and the substrate's surface. The following step implicated the dry process, which only exposed the desired pads.

5.6 Soldering Process

The soldering process follows the flexible hybrid membrane microfabrication. Seeing that one of the main goals of this thesis is the creation of a thin conformable double layered FHE sensing membranes based on rigid silicon components, over parylene flexible substrates, and knowing that the primary determinant for the membrane's thickness is the size of these components. Various tests were performed in order to determine which size codes were viable for soldering using the available equipment at DCM.

Table 5.2: Component's viability for the soldering process.

Size Code	**Length** (mm)	**Width** (mm)	**Height** (mm)	**Status**
0402	1.00	5.00×10^{-1}	3.50×10^{-1}	✓
0603	1.55	8.50×10^{-1}	4.50×10^{-1}	✓
0805	2.00	1.20	4.50×10^{-1}	✓
1206	3.20	1.60	5.50×10^{-1}	✓

Table 5.2 reveals the achieved results during the previously mentioned testing. Accordingly the mainly used components throughout the developed prototypes had the size codes of 0402, 0805 and 1206, Figure 5.14 illustrates a size comparison between these size codes. Although most used components belonged to one of these size codes, MAXIM's prototype employed two components which are considerably bigger, the ZIF connector and the MAX30205MTA+ temperature sensor, whilst PT100's prototype included the MAX31865 sensor which is larger then its fellow ICs and SMDs.

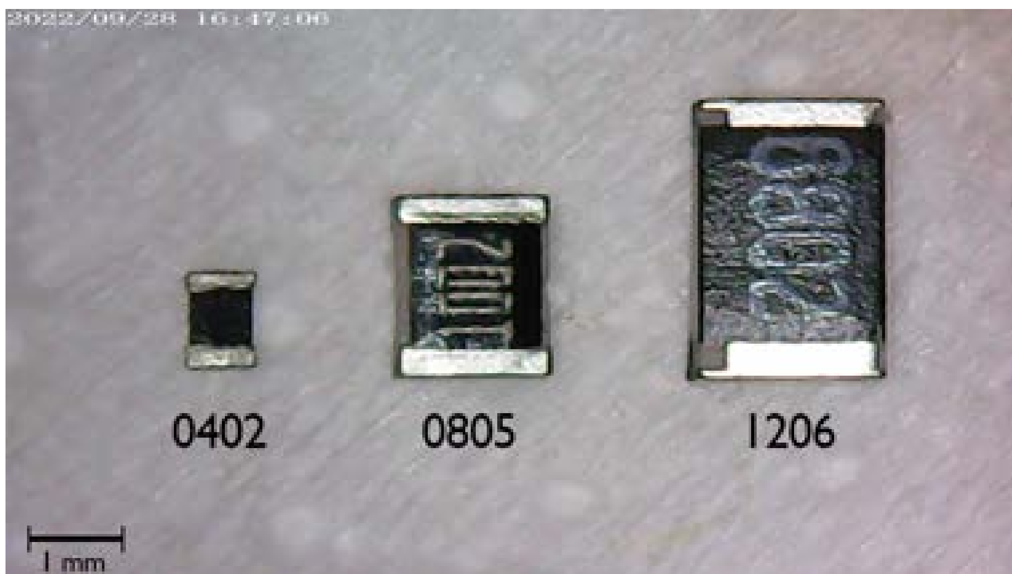

Figure 5.14: Size comparison between components of different size codes.

Firstly in the soldering process, is the solder paste placement over the pads, on which the components will be soldered to. To do so a small gauge needle was put to use to make sure only the necessary amount of paste was deposited on the pad. In order to promote the best possible integration of the ICs and SMDs onto the flexible membrane. The solder paste appearance before being submitted to a temperature reflow profile is demonstrated in Figure 5.15 A.

Succeeding the solder paste and the IC placement, the temperature reflow profile suggested by the solder paste manufacture was applied not only contributing to the coalescence of solder paste's metal spheres but also integrating these ICs and SMDs onto the membrane creating an electrical connection to the rest of the circuit. The result of this can be seen in Figure 5.15 B.

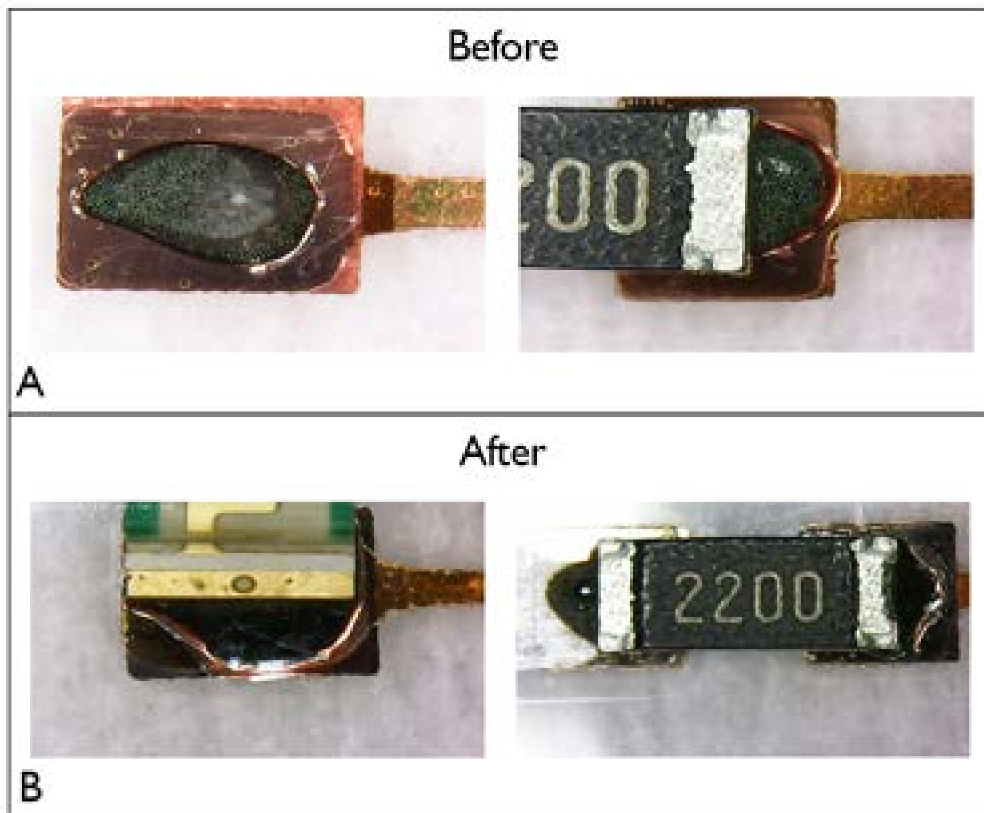

Figure 5.15: Solder paste appearance before (A) and after (B) being submitted to a temperature reflow profile.

Despite the initially successful solder process of prototype MAXIM's, first iteration, one predicament emerged when any type of force (to open or close the ZIF) or movement was applied to the integrated ZIF connector, these actions resulted in its decoupling. A total of five attempts were made to resolder this component, of substantial size, to the thin membrane substrate, until on the fifth try an acceptable connection was established. The source of this problem was attributed to the component's size, with 11.5 mm in length, and its weight whose comparison with its neighbouring 0402 components or even the

MAX30205MTA+ temperature sensor, reveal great discrepancy, supported by Figure 5.16. It was then concluded that a component of such dimensions should not be integrated into the flexible membrane.

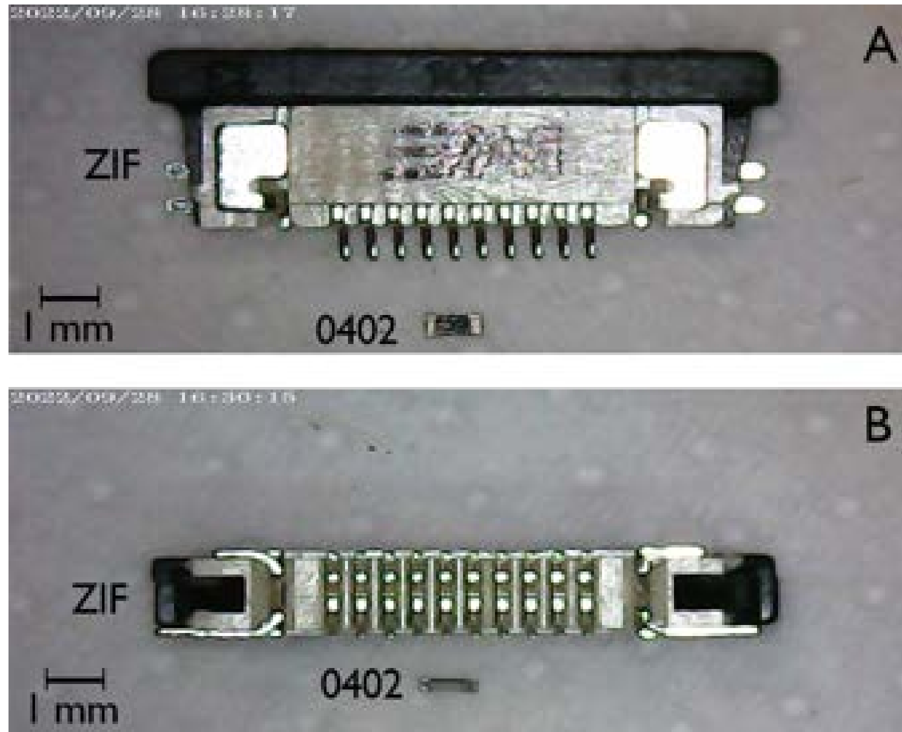

Figure 5.16: Size comparison between the ZIF connector and 0402 size code components. A - Top view comparison between these components. B - Side profile comparison among these components.

Note that all throughout this thesis project there was a worldwide shortage of electronic components and thus some of the unattainable components such as the MAX31865 sensor, the MIC5225-3.3 voltage regulator and the 1N4148 diodes, essential to the PT100's prototype, were desoldered from the rigid Adafruit MAX31865 RTD PT100 Amplifier.

5.7 Peel Off

After the integration of the rigid ICs in the flexible membrane and the prototype's encapsulation, the next step was to dissolve the PVA sacrificial layer, in order to decouple the flexible membrane from its glass carrier. Overall once in contact with the water every prototype was eventually released from it's carrier, however due to the size difference amongst components some prototypes took longer then others.

In addition, it was observed that not all final membranes possessed the same look and texture. This is most prevalent when comparing the final membranes of the first and second iteration of prototype MAXIM. Figure 5.17 A shows the first iteration MAXIM prototype, with its wrinkly look and rough texture, on the other hand, Figure 5.17 B reveals the much flatter and smoother characteristics of this prototype's second iteration.

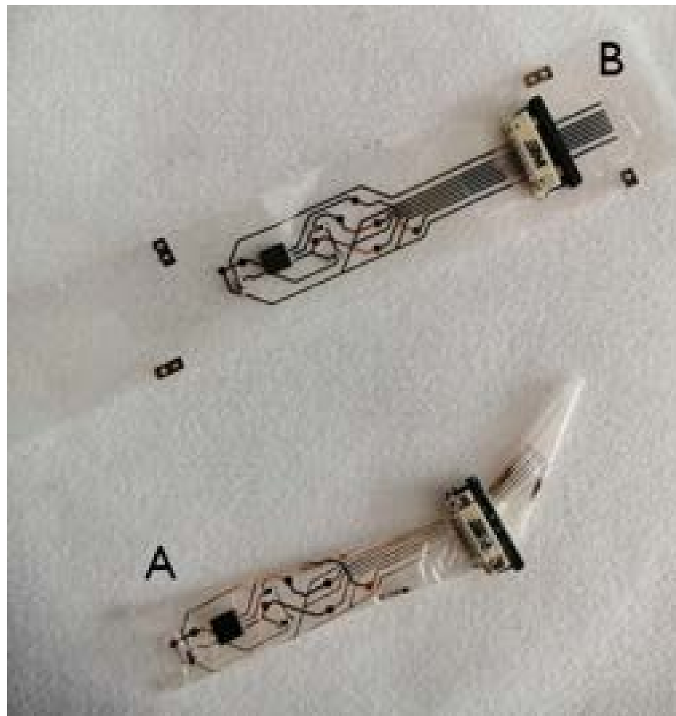

Figure 5.17: Comparison between the first (A) and second (B) iteration MAXIM prototype.

A possible reason behind this dissimilarity may reside in the fact that, as mentioned in Section 5.6, the first iteration of this prototype was subdued to five temperature reflow processes, in an attempt to resolder its ZIF connector, during which the whole substrate was subjected to five time-temperature profiles, each reaching a maximum temperature of 200 °C. Whereas the second iteration only was subjugated to this temperature reflow once. In both cases the membrane was then encapsulated with a new parylene layer, which was not submitted to any temperature treatment.

According to a study, on the influence of temperature on the crystallinity of parylene C corroborated by XRD analysis, conducted by Martins in her master thesis work. It was reported an increase in intensity accompanied by a decrease in the 2θ angle of the initial peak, correspondent to the parylene's crystalline plane (0 2 0), upon the increase in temperature. This decrease of the 2θ angle represents an increase of the inter-planar spacing, indicating an expansion/dilation of the crystal lattice. On the other hand when the sample was cooled, Martins revealed a shift in the peak to higher 2θ values, indicating a lattice contraction.

Analysing the diffractograms, of Figure 5.18, provided by Martins in her thesis [21], it can be observed that as the temperature subsides, despite a slight decrease in intensity, this value tends to stabilize and not reach its initial amount. This suggests that succeeding the parylene's heating its crystallinity increased. Furthermore the 2θ angle increased relatively more during the cooling than it decreased across the heating phase, leading to the conclusion that the crystal lattice displayed a more compressed end state than its original one.

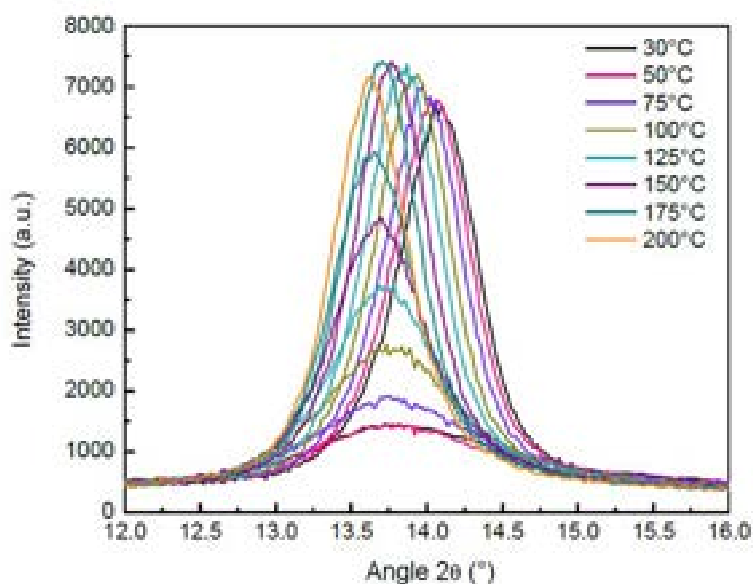

Figure 5.18: Diffractograms from a XRD analysis of parylene C at different temperatures. Adapted From [21].

Taking into consideration that MAXIM's first iteration parylene suffered five rounds of heating and cooling, is evident that its parylene crystal lattice was more compressed than MAXIM's second iteration parylene who only endured one heating and cooling phase. Additionally, both iterations were encapsulated with a parylene layer which did not sustain the temperature reflow and since the discrepancy of crystal lattices between the parylene substrate and the newly deposited encapsulation parylene is higher on the first iteration of the MAXIM's prototype. It is then expected for this prototype to possess the wrinkly look and rough texture noticed in Figure 5.17 A. Because the second iteration's parylene withholds a crystal lattice closer to the encapsulation's parylene, their disparity is not as noticeable, hence a smoother look is perceived (Figure 5.17 B).

The handling of this fragile membrane allied with the presence of an integrated ZIF connector caused a tear along the prototype's tracks responsible for its interface with the rest of MAX30205 Human Body Temperature Sensor Evaluation Kit. Due to MAXIM's dependency on ZIF connectors to establish this connection and because the ZIF connectors used in this prototype had bottom connections, a rigid board containing two re-circuited ZIFs, was developed and named Inversion Board. In a first attempt these rigid boards were manufactured *in situ*, however this attempt proved to be ineffective. Figure 5.19 A shows the outcome of this endeavour.

In order to accomplish these rigid boards, JLCPCB, a professional PCB manufacturer, was resorted to, since it was a faster and relatively cheaper solution to the problem. Figure 5.19 B exhibits the Inversion Boards produced by the PCB manufacturer.

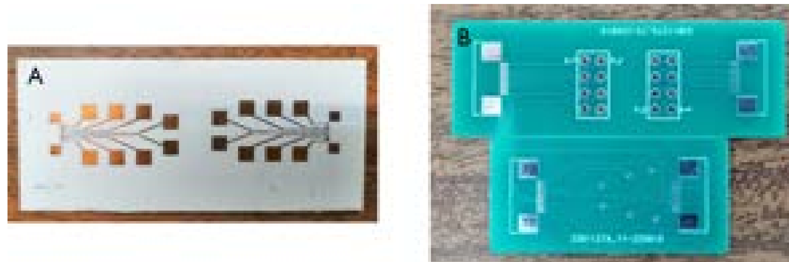

Figure 5.19: Inversion boards created. A - First attempt at DCM's clean room. B - Manufactured by JLCPCB.

In addition to prototype MAXIM, all other prototypes suffered, to some extent, the consequences of the thin and flexible nature of these parylene based membranes. One of these consequences being the membrane's susceptibility to ruptures. Figure 5.20 showcases some of these occurrences throughout the prototypes. In some cases, these tears rendered the prototypes useless, since the connection between the circuits and their respective microcontrollers were severed.

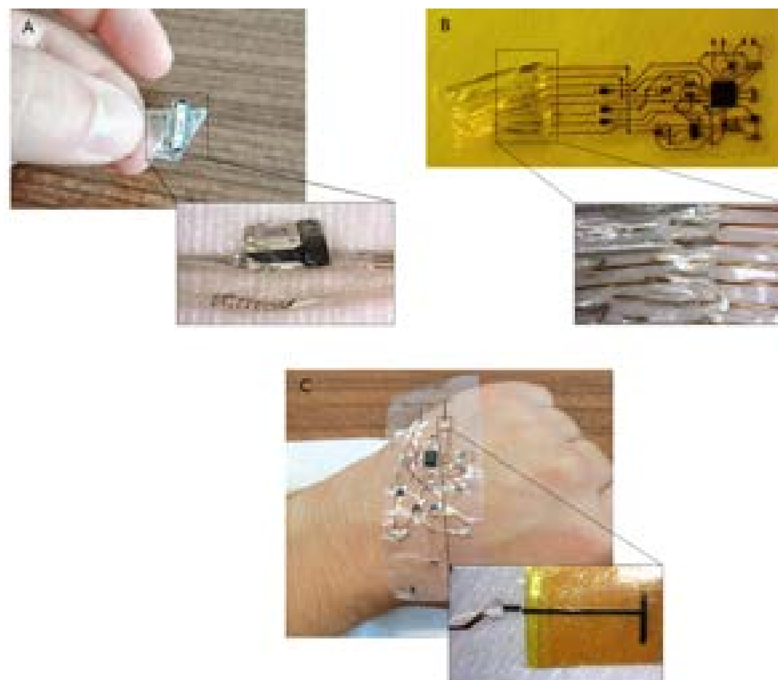

Figure 5.20: Mechanical fragilities among prototypes. A - First iteration MAXIM membrane's rupture in the region where the ZIF was integrated into the membrane. B - PT100's tear along the copper tracks responsible for its interfacing with the Arduino microcontroller. C - PiscaPisca circuit from the LED prototype, whose rupture also occurred on the interface responsible tracks.

5.8 Final Prototypes and Testing

In preparation for the testing phase, devices based on jumper wires and ZIF connectors were created, according to each prototype's requirements. Enabling the interface between the FHE membranes and the Arduino Uno microcontroller. Figure 5.21 highlights these devices and their end goal. Additionally a 100 Ω platinum RTD was soldered to a ZIF connector allowing for its interface with to the PT100's flexible prototype.

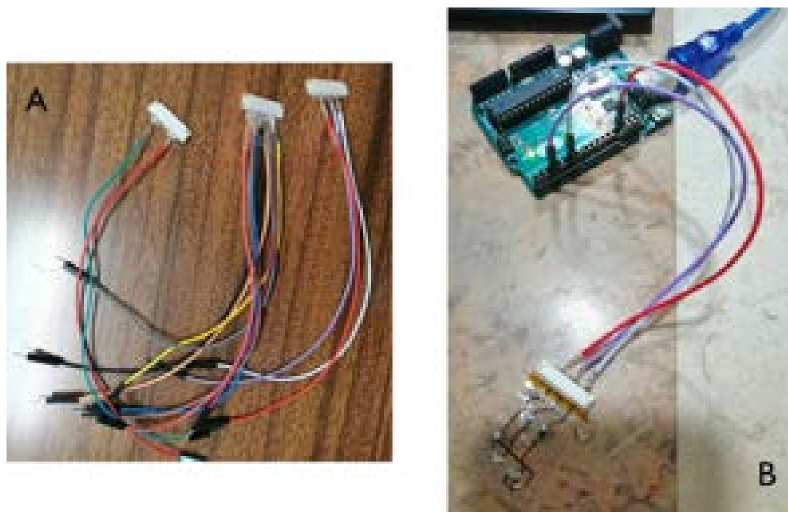

Figure 5.21: Communication enabling devices, based on ZIF connector (A) and their final purpose (B).

The Arduino code presented on Appendix C was also created/repurposed in anticipation of the testing phase. This Arduino code can also be accessed at `https://github.com/PedroCRodrigues/Fabrication_of_Flexible_Hybrid_Circuits_in_Parylene`. These simple codes were constructed as a means to establish communication between the flexible membranes and the microcontroller, allowing for temperature sensing and reading in MAXIM's and PT100's prototype, Appendix C.2 and C.3, and to coordinate the power transfer and LED lighting frequency in the LED prototype, Appendix C.1.

Subsequent to all preparations the testing phase was ready to initiate, using the final prototypes seen in Figure 5.22.

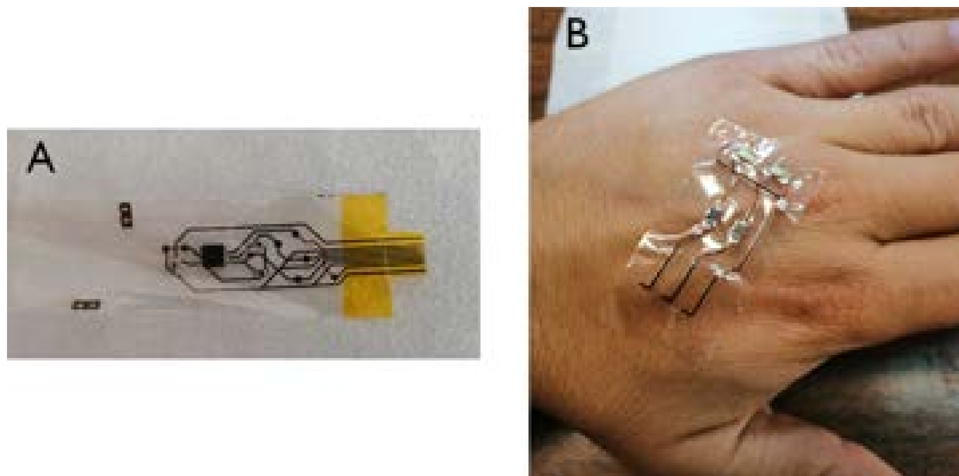

Figure 5.22: Prototypes which were submitted to the testing phase. A - MAXIM prototype. B - 2Via circuit from the LED prototype.

In an attempt to examine MAXIM's prototype, multiple types of physical connections, between the prototype's flexible membrane and the rigid MAX30205 Human Body Temperature Sensor Evaluation Kit were established (Figure 5.23 A) with and without the previously created Inversion Board. However, in all tested scenarios Maxim's GUI program always displayed the same warning message, seen in Figure 5.23 B, stating that the program did not recognize the membrane's sensor.

Figure 5.23: Tests performed to the MAXIM prototype (A) and the warning message displayed in Maxim Evaluation kit's program succeeding each test (B).

Another attempt at testing the MAXIM's prototype was performed using an Arduino Nano microcontroller and the code presented in Appendix C.2, which allowed the extraction of information directly from the membrane, including the sensor's signal. Despite these efforts, the microcontroller did not receive any signal from the MAX30205MTA+ sensor. Figure 5.24 shows this debugging process. This set up proved to be capable of replacing the rest of the rigid elements in Maxim's evaluation kit enabling direct communication with the membrane's sensor and neighbouring components.

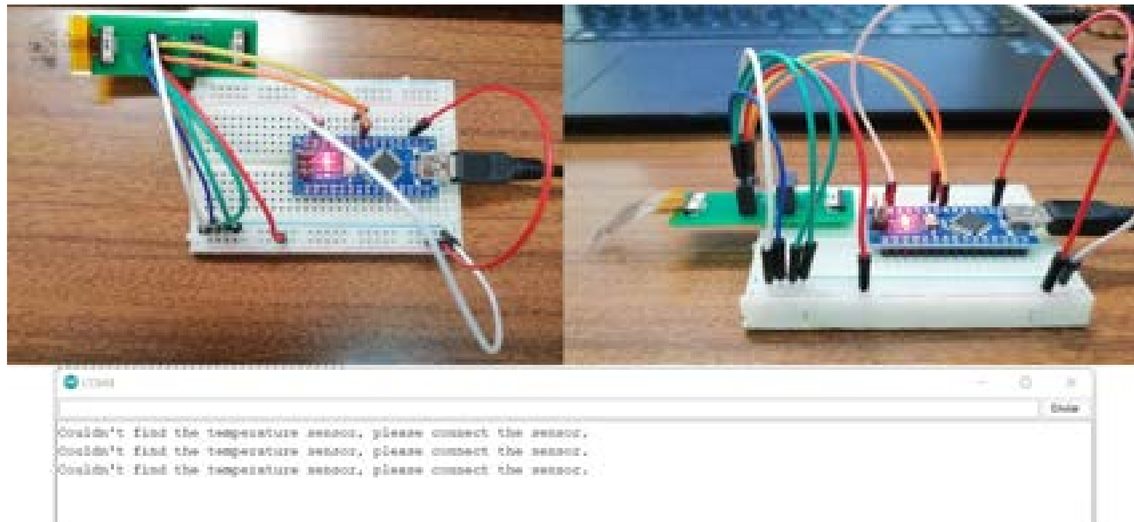

Figure 5.24: Debugging of the MAXIM prototype, including its interface with the Arduino and the confirmation that no sensor was detected.

The testing of the LED prototype went similarly to the previously mentioned. In spite of being properly interfaced with the Arduino Uno, no lights turned on. So continuity tests were performed, to corroborate if current passed through the designated areas.

These tests revealed that presumably unconnected pads and tracks were in fact allowing current to pass, short-circuiting the electrical circuits in the LED prototype. After detecting this anomaly, all other prototypes were subjected to continuity tests, concluding that the final prototypes presented short-circuiting.

The explanation for this event is an ineffective dielectric parylene layer, which does not prevent the passing of current among copper layers. By not performing as anticipated all overlapping circuit (Figure 5.25) become inter-layer passage points (pinholes) for current, instead of the designed viae, leading to the short-circuiting of tracks and pads. This occurrence was later attributed to a contamination on the parylene CVD system, detected only after the completion and testing of these last circuits.

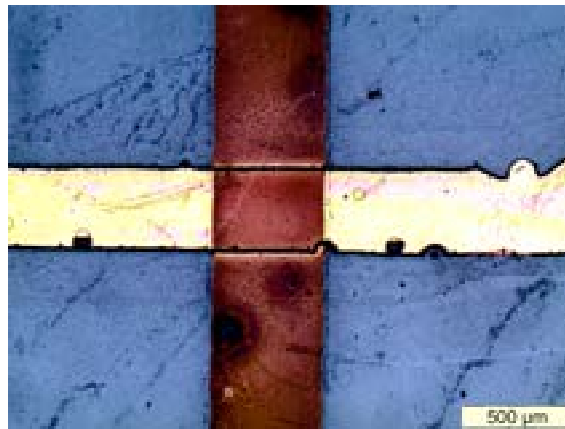

Figure 5.25: Example of overlapping circuit threads.

Despite this, it was still possible to see the activation of one LED in the 2Via circuit from LED prototype, Figure 5.26, once current was forced into this circuit by a multimeter.

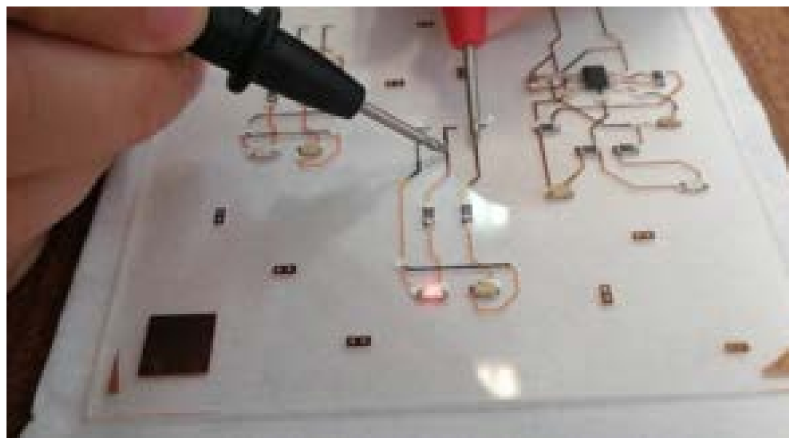

Figure 5.26: LED activation.

In addition to continuity tests performed on previous prototype versions, the aforementioned occurrence confirms the success of the double layer theory, for hybrid temperature sensing membranes. These results allied with the optimization of the soldering process on parylene substrates showcase an adequate approach to the fabrication of conformable FHE sensing membranes.

At the moment, new iterations of the developed prototypes are being manufactured and with each upcoming step these demonstrate a promising in-sight on the future of FHE membranes and their endless possibilities.

6

Conclusion

The main goal of this thesis was to develop flexible and conformable double layered hybrid temperature sensing membranes based on flexible parylene substrates and traditional rigid silicon ICs and SMDs, in order to achieve body temperature monitoring.

The final produced membranes were comprised of a parylene substrate, two patterned copper layers, various soldered ICs and SMDs, a dielectric parylene layer and two parylene encapsulation layers. Despite having multiple layers all prototypes revealed great flexibility and conformability, adapting to the curvilinear body surface.

To bring together the main attained conclusions, the main project goals mentioned in the introduction will be reviewed, and a summary of what was achieved in each one will be reported.

- **Study the individual response of two commercial rigid temperature measuring circuits**.

  Since two of the developed FHE membranes were based on the MAX30205 Human Body Temperature Sensor Evaluation Kit and the Adafruit MAX31865 RTD PT100 Amplifier, the study of the inner workings of these circuits proved to be helpful in the design phase of the electrical circuits which would later be patterned on the copper layers of the flexible membranes. The analysis of these PCB's also provided the information of which components to acquire and in some cases which to desolder from the rigid PCBs.

  In addition, this study also provided insight on how the interface of these rigid PCBs to their respective microcontrollers functioned, therefore aiding in the creation of the photomasks used.

- **Produce the flexible element of the FHE membrane, comprised of parylene films and metallic thin films**.

  Throughout the creation of the flexible prototypes and in spite of the challenges brought by the design, fabrication and use of a manual alignment system, it was

demonstrated that the parylene layers are compatible with the thin-film microfabrication techniques employed, among them, the e-beam metal deposition method, photolithography as well as the wet etching process and the RIE procedure.

It should be noted that no chemical treatments were applied to parylene film's surface during the microfabrication to increase the adherence of the following copper films.

- **Assemble rigid and silicon-encapsulated electronics (ICs and SMDs) onto the flexible substrate**.

  The soldering processes performed across the prototype's fabrication revealed that the deposited parylene and copper thin-layers were able to withstand this procedure, establishing electrical connections between the silicon rigid ICs and the patterned copper layers.

  Despite this success, it was concluded that larger and heavier components, such as ZIF connectors, which require frequent handling, should remain in rigid format PCBs. If soldered to flexible substrates, their weight and size would promote the membrane's rupture. On the other hand, the smallest size code of components, whose solder was possible with the available equipment at DCM, was 0402.

  It was also found that the FHE membrane's appearance after the peel off process is related to the amount of times its parylene layers are submitted to the reflow process's high temperatures. According to Martins's master thesis work [21], thermal treatments affect the structural properties of parylene, increasing its crystallinity and compressing its crystalline lattice. From this it can be extracted that with every temperature reflow process the changes in parylene's crystalline structure accumulate.

  Considering that, prior to peel off a final parylene encapsulation layer, with no previous temperature treatment, is deposited on top of the structurally different parylene substrate, it is possible to infer that the greater the discrepancy between crystalline lattices the wrinklier and rough the final membrane will be.

- **Interface the sensing membrane with a microcontroller.**

  Interface devices, based on ZIF connectors, were successfully constructed and linked to the flexible membranes. Additionally the prototype's respective microcontrollers were set up and prepared for this interaction.

  However, despite all physical connections being in place, no data was obtained due to the dielectric problem, explored in Chapter 5.8. It was still possible to witness the activation of one LED in the 2Via circuit from LED prototype, demonstrating the deposited copper's capability of conducting current and proving the success of the double layer theory for hybrid sensing membranes. Which combined with the optimization of the soldering process on parylene substrates indicates a promising approach on the fabrication of FHE membranes and their capabilities.

6.1 Future Perspectives

The developed work shows promising results, however, some steps in the fabrication of the conformable double layered FHE sensing membrane require more testing. In order to improve and conclude this project, suggestions of future work are presented.

The first suggestion consists in the redesigning of the electrical circuits, enlarging tracks which perform the interface between the circuit and the microcontroller as well as adding extra pads for electrical characterization and continuity tests.

Another point of improvement, in an attempt to surpass the dielectric challenge and prevent current from flowing between copper layers, would be to use silane, an adhesion promoter, in the dielectric and encapsulation parylene depositions, so as to improve the adhesion of parylene to the materials where it will be deposited.

In future works the use of ZIF connectors should be reconsidered, since other forms of interfacing flexible membranes with rigid hardware are readily available. Therefore, the application of technologies such as Pogo pin connectors, Wi-Fi data transfer or even Bluetooth communication should be researched.

Finally, in order to prevent undesirable tears during handling, the thickening of the parylene substrate is suggested, by doing this the usage of Kapton tape to thicken the membrane would become obsolete and would make the overall prototype stronger, less flimsy and less prompt to tears, although it would sacrifice some of its flexibility and ability to conform with the human body. It would be interesting to determine the exact parylene dimer mass which provides the flexible membranes the most mechanical robustness without sacrificing its flexibility.

The successful production of a fully functional flexible and conformable double layered hybrid sensing membrane could propel the adaptation of other rigid health monitoring electronics to FHE membranes, further engraving this technology into people's daily lives.

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A

Schematics and Circuits

In this first appendix, the schematic diagrams and their corresponding circuits of each of the developed prototypes, LED, MAXIM and PT100, can be respectively seen in the following images. These were created in order to corroborate the flexible double layered hybrid sensing membrane theory and to accomplish temperature sensing.

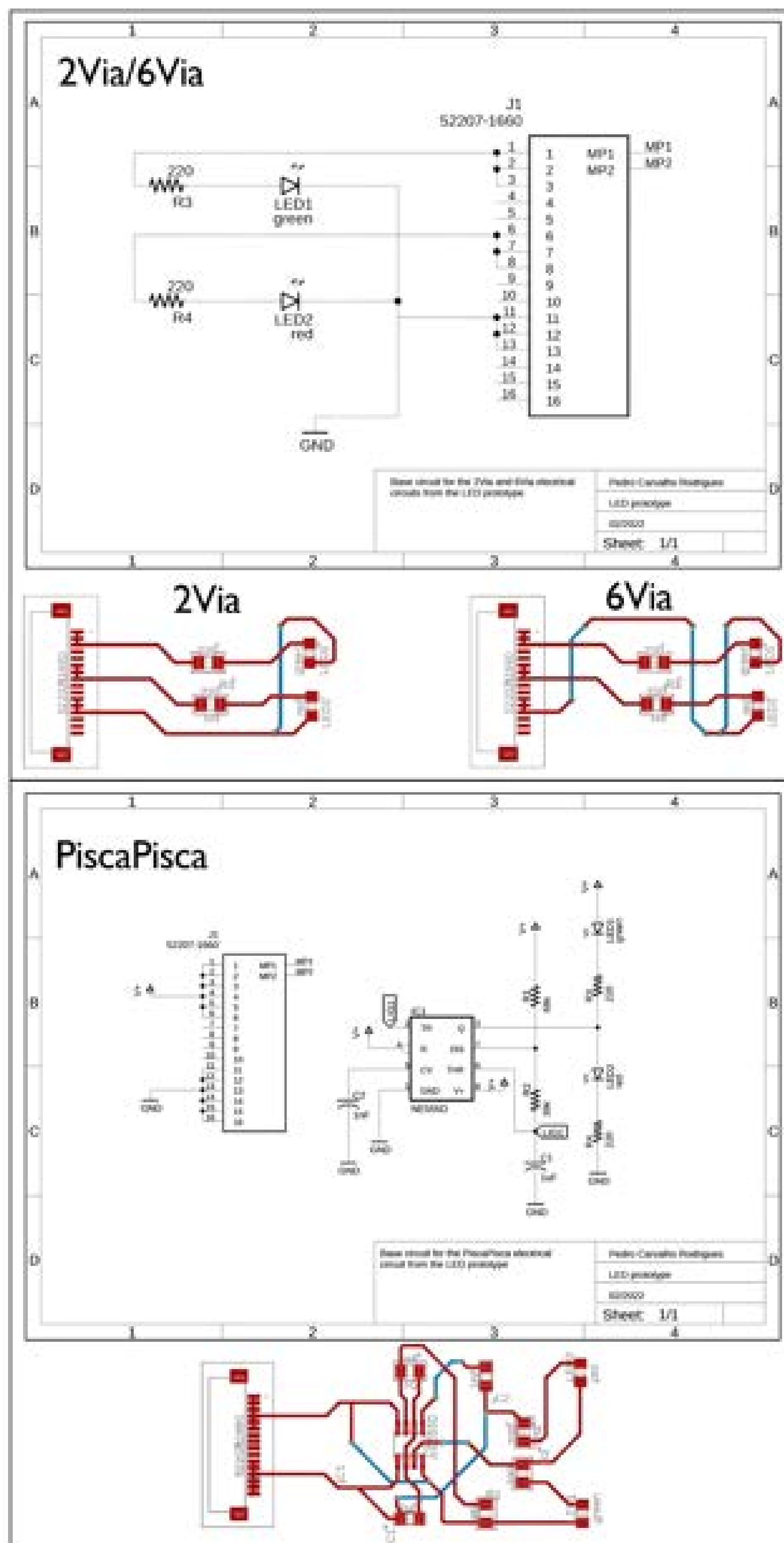

Figure A.1: Schematic diagram and circuit design for the LED prototype.

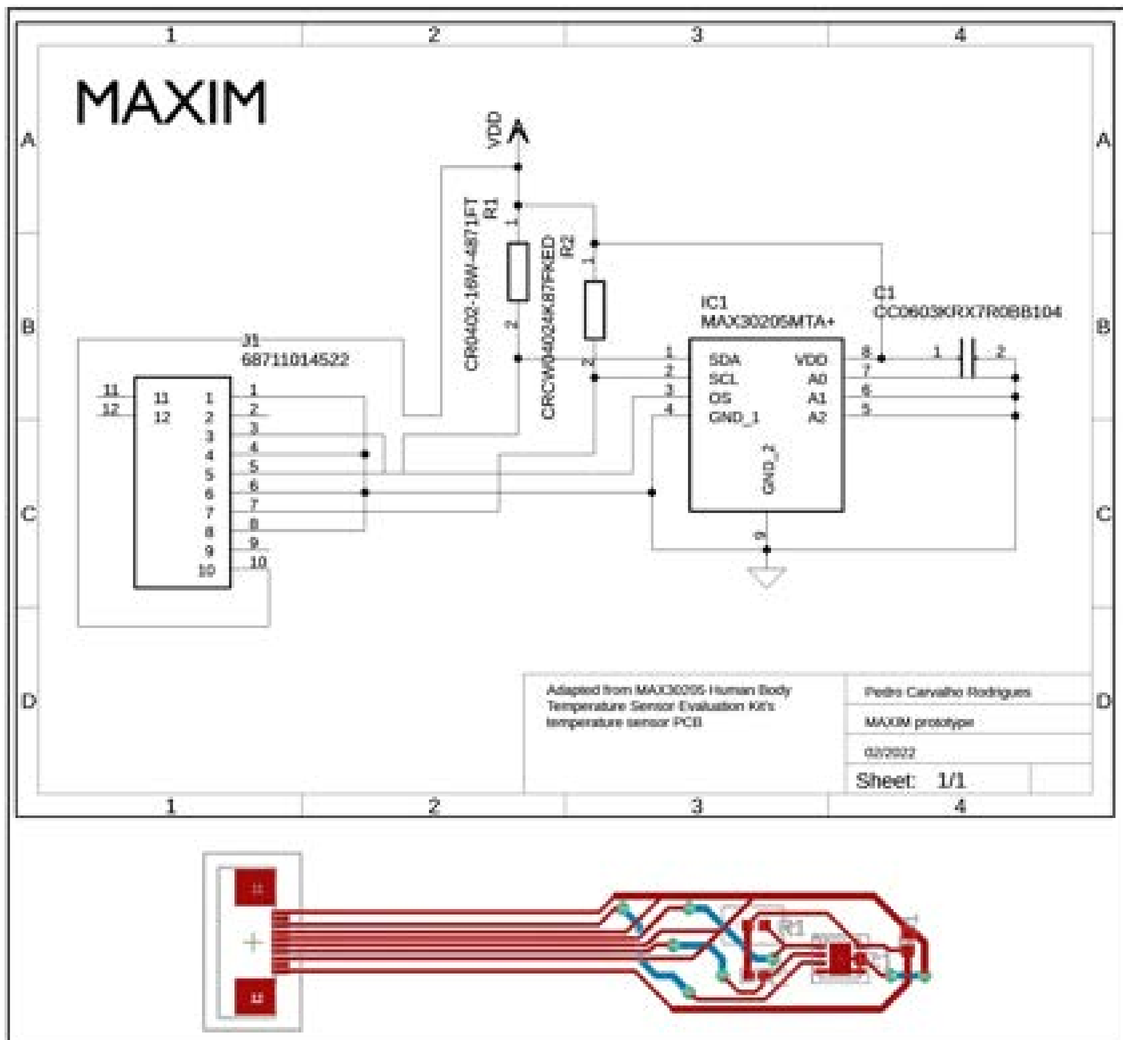

Figure A.2: Schematic diagram and circuit design for the MAXIM prototype.

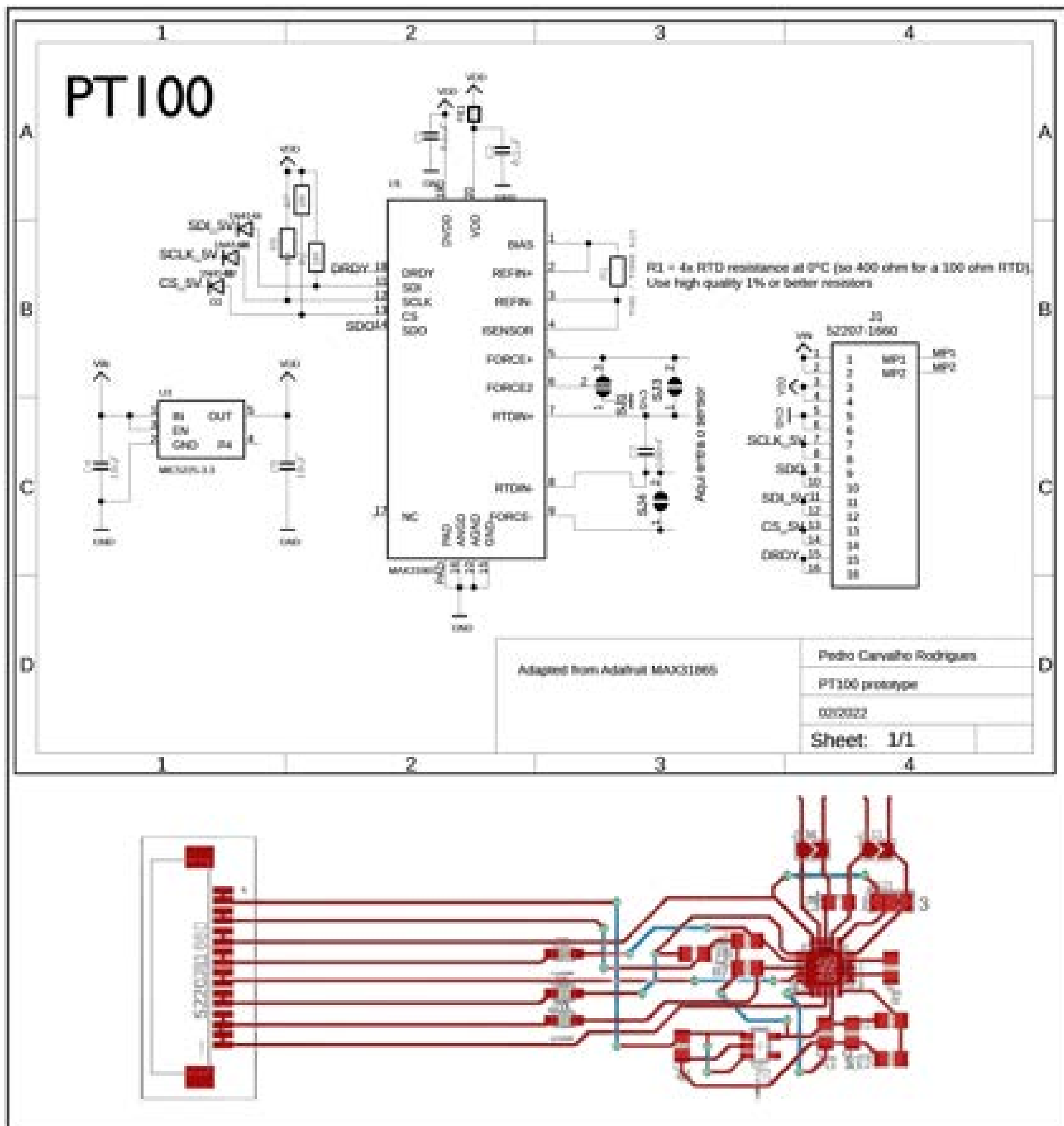

Figure A.3: Schematic diagram and circuit design for the PT100 prototype.

B

Photomasks

This appendix showcases the final iterations of the negative and positive photomasks created for all developed prototypes. In each figure the top two images represent the negative masks which were used to pattern the first (on the left) and second (on the right) metal layers. The two images below represent the positive photomasks that were used to pattern the openings in the parylene during the dry etching of the dielectric layer (on the left) and of the encapsulation layer (on the right). These photomasks were designed to be fitted on top of 10×10 cm glass carriers.

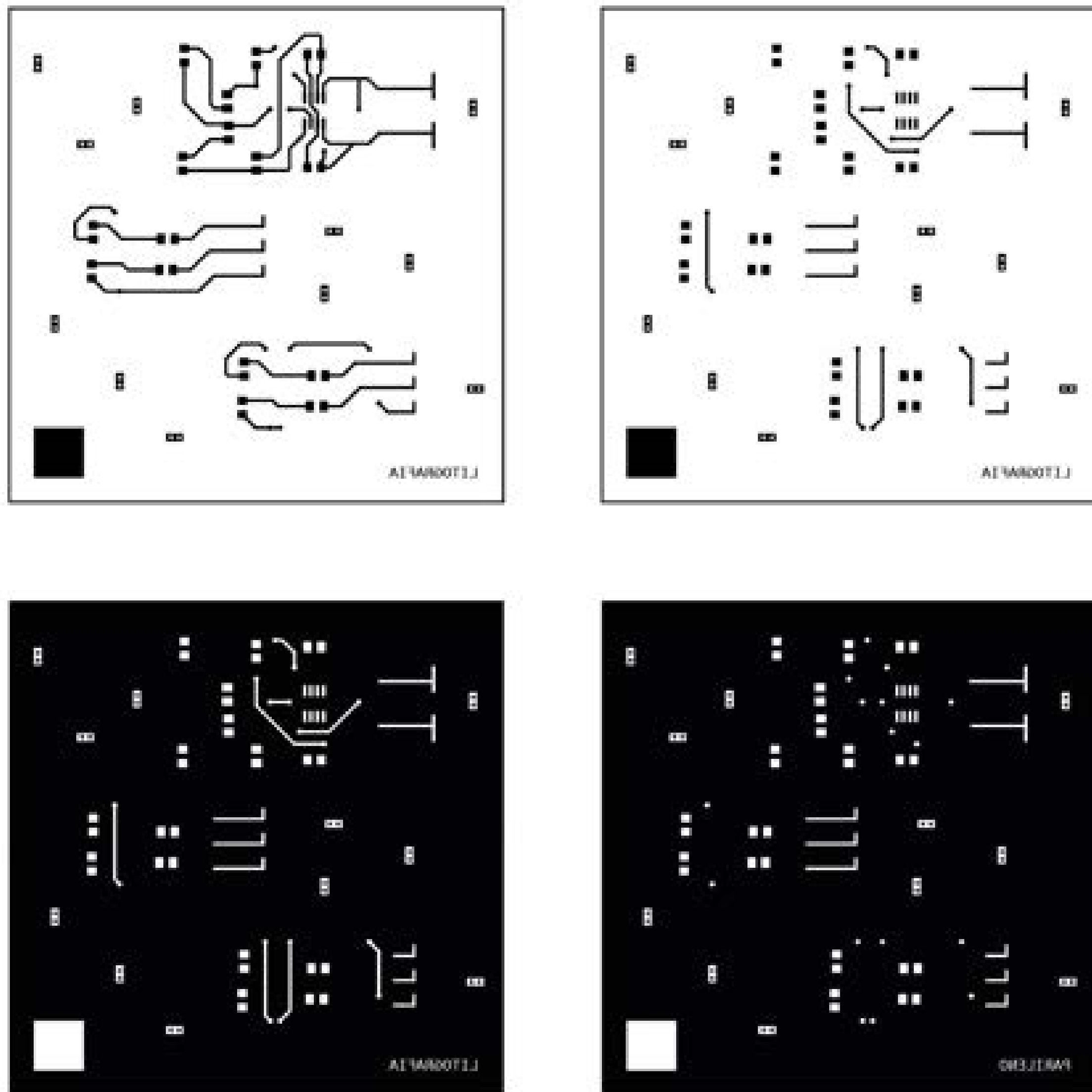

Figure B.1: Photomasks used for the LED prototype.

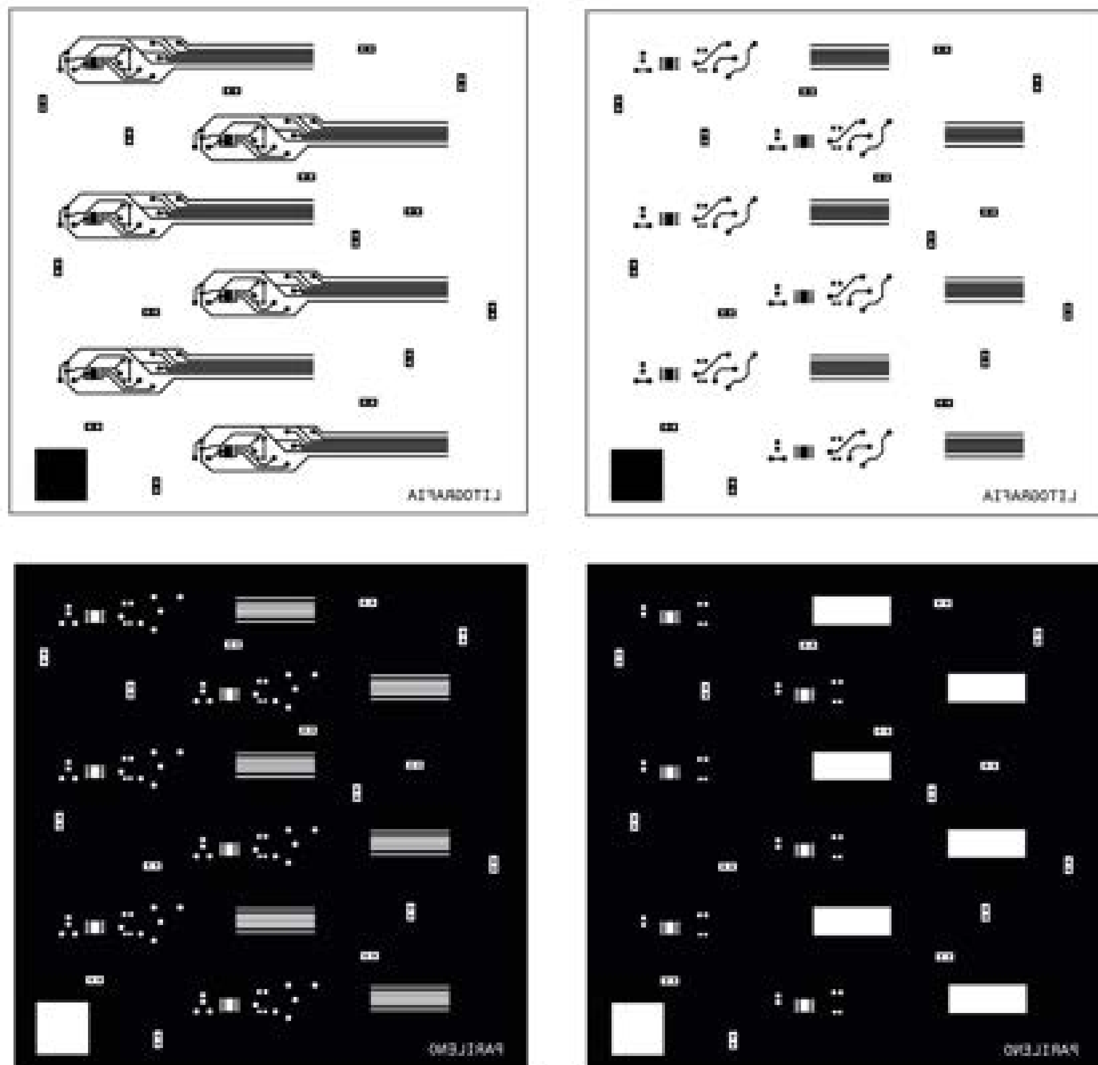

Figure B.2: Photomasks used for the MAXIM prototype.

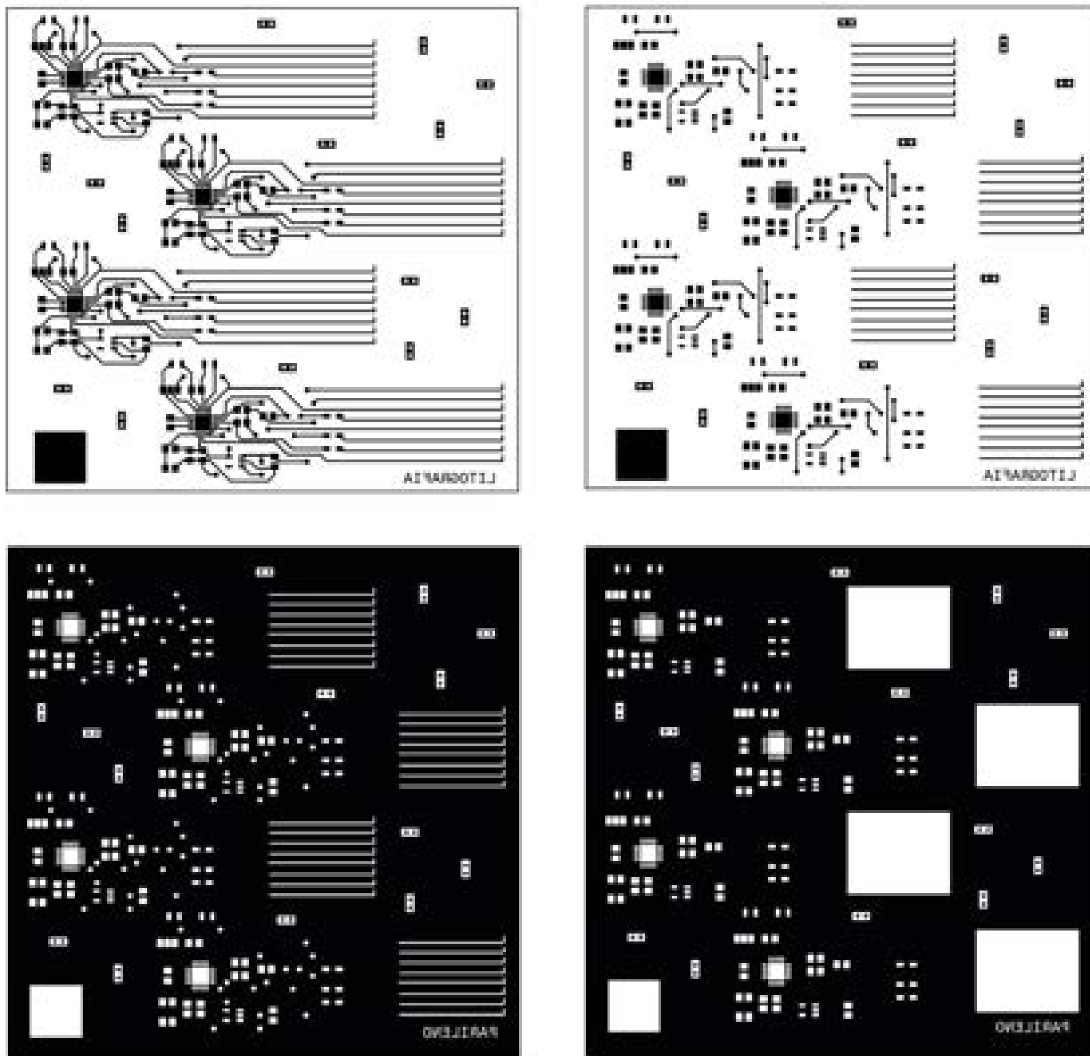

Figure B.3: Photomasks used for the PT100 prototype.

C

Arduino Codes

In this appendix the Arduino codes created and repurposed throughout this thesis are displayed. These simple codes were constructed as a means to establish communication between the flexible membranes and the microcontrollers, allowing for temperature sensing and reading in MAXIM's and PT100's prototype. As well as to coordinate the power transfer and LED lighting frequency in the LED prototype. This Arduino code can also be accessed at `https://github.com/PedroCRodrigues/Fabrication_of_Flexible_Hybrid_Circuits_in_Parylene`.

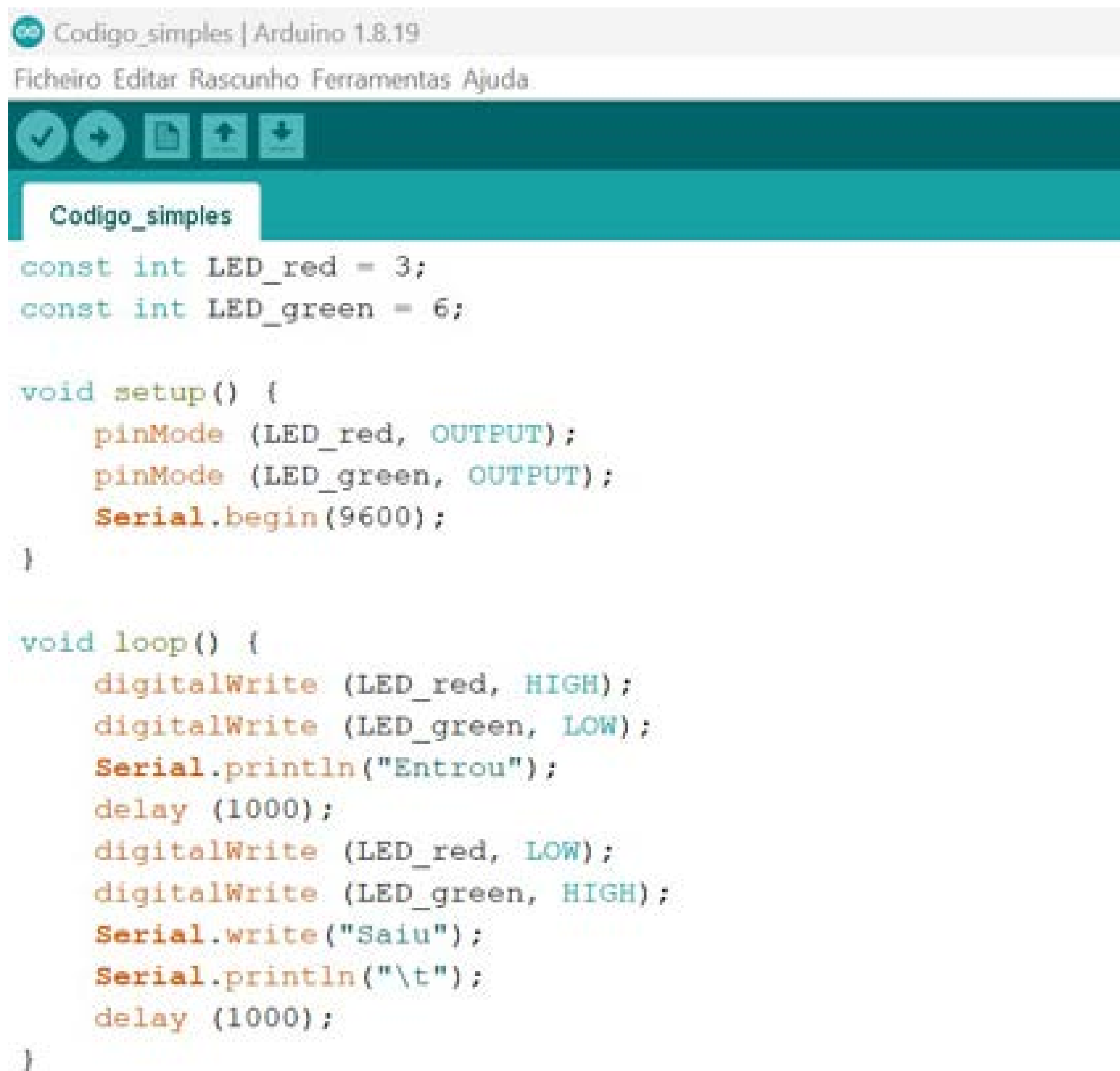

Figure C.1: Arduino code created for the LED prototype.

```
MAXIM_Arduino_code | Arduino 1.8.19
Ficheiro Editar Rascunho Ferramentas Ajuda
MAXIM_Arduino_code

/*
This program Print temperature on terminal

Hardware Connections (Breakoutboard to Arduino):
Vin  - 5V
GND - GND
SDA - A4 (or SDA)
SCL - A5 (or SCL)
*/

#include <Wire.h>
#include "Protocentral_MAX30205.h"
MAX30205 tempSensor;

void setup() {

  Serial.begin(9600);
  Wire.begin();

  //scan for temperature in every 10 sec untill a sensor is found. Scan for both addresses 0x48 and 0x49
  while(!tempSensor.scanAvailableSensors()){
    Serial.println("Couldn't find the temperature sensor, please connect the sensor." );
    delay(10000);
  }

  tempSensor.begin();   // set continuos mode, active mode
}

void loop() {

  float temp = tempSensor.getTemperature(); // read temperature for every 100ms
  Serial.print(temp ,2);
  Serial.println("'c" );
  delay(100);
}
```

Figure C.2: Arduino code, adapted from [102], for the MAXIM prototype.

max31865_comp | Arduino 1.8.19

Ficheiro Editar Rascunho Ferramentas Ajuda

max31865_comp §

```
/***************************************************
  This is a library for the Adafruit PT100/P1000 RTD Sensor w/MAX31865

  Designed specifically to work with the Adafruit RTD Sensor
  ----> https://www.adafruit.com/products/3328
  This sensor uses SPI to communicate, 4 pins are required to
  interface
  Adafruit invests time and resources providing this open source code,
  please support Adafruit and open-source hardware by purchasing
  products from Adafruit!
  Written by Limor Fried/Ladyada for Adafruit Industries.
  BSD license, all text above must be included in any redistribution
 ****************************************************/
#include <Adafruit_MAX31865.h>
// Use software SPI: CS, DI, DO, CLK
Adafruit_MAX31865 thermo = Adafruit_MAX31865(10, 11, 12, 13);
// use hardware SPI, just pass in the CS pin
//Adafruit_MAX31865 thermo = Adafruit_MAX31865(10);
#define RREF      430.0 //Rref resistor = 430.0 for PT100
// The 'nominal' 0-degrees-C resistance of the sensor 100.0 for PT100
#define RNOMINAL  100.0

void setup() {
  Serial.begin(9600); // Comunication with "serial monitor" at a 9600 bits/s rate
  Serial.println("Adafruit MAX31865 PT100 Sensor Test!");
  thermo.begin(MAX31865_2WIRE);  // Because the measurment is performed with 2 wires in the Pt100
}
void loop() {
  uint16_t rtd = thermo.readRTD();     //reads from the previous function

  Serial.print("RTD value: "); Serial.println(rtd);
  float ratio = rtd;
  ratio /= 32768;          // 2^15, 15 bits resolution
  Serial.print("Ratio = "); Serial.println(ratio,8);
  Serial.print("Resistance = "); Serial.println(RREF*ratio,8);  // analogic resistance value
  Serial.print("Temperature = "); Serial.println(thermo.temperature(RNOMINAL, RREF)); // resistance value

 Serial.println();
 delay(1000);
}
```

Figure C.3: Arduino code, adapted from [43], for the PT100 prototype.

I

Laser Power and Speed Conversion Charts

In this annex, the conversion charts, for the VLS 3.50 desktop laser by Universal Laser Systems, are included. These charts serve as a conversion reference for the laser speed and power parameter percentages to standard units (m/s and W). This is useful in the translation of the PXSY syntax for laser settings combinations, where P and S refer to the power and speed, and X, and Y are its respective percentages.

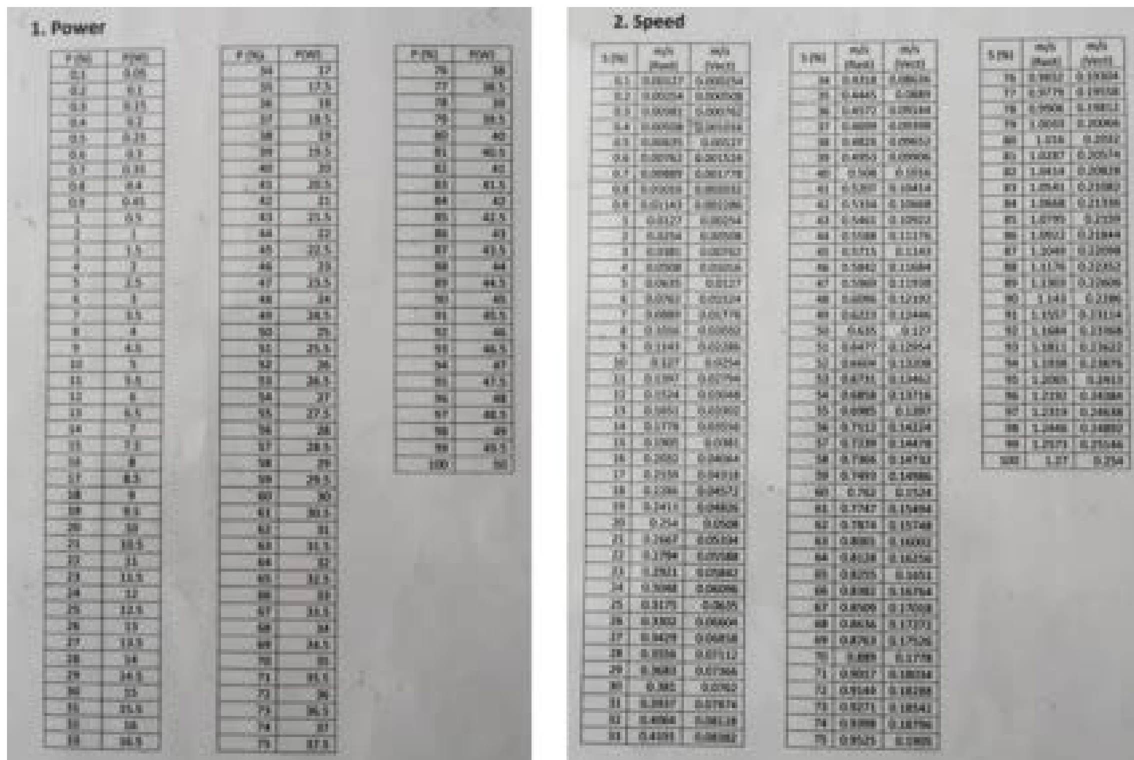

Figure I.1: Laser speed and power percentage conversion to standard units for the VLS 3.50 desktop laser by Universal Laser Systems.