NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF MATERIALS SCIENCE

INÊS RODRIGUES DIOGO

BSc in Micro and Nanotechnology Engineering

RAPID THERMAL PROCESSING AND ITS EFFECTS ON HIGH ASPECT RATIO SILICON FEATURES

MASTER IN MICRO AND NANOTECHNOLOGY ENGINEERING

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Adviser: Prof. Dr. Rafael Taboryski
Full Professor, Technical University of Denmark

Co-advisers: Prof. Dr. Henri Jansen
Full Professor, Technical University of Denmark

Prof. Dr. Joana Pinto
Invited Assistant Professor, NOVA University Lisbon

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Rapid Thermal Processing and its Effects on High Aspect Ratio Silicon Features

Para a minha avó,

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‘I am not afraid of storms, for I am learning how to sail my ship.’
(Louisa May Alcott, Little Women)

ABSTRACT

Silicon (Si) is the most widely used material in semiconductor devices fabrication, and silicon wafers undergo many steps before achieving the final product, including heat treatments. A rapid thermal processor, with a base pressure of 10^{-6} mbar, is the case study of this work, and it's proposed as an alternative to more conventional furnace methods. Moreover, the main goal was to investigate the impact rapid thermal processing (RTP) has on different high aspect ratio (HAR) structures etched into Si substrates. The 'clear – oxidize – remove – etch' (CORE) process was used as the primary etching process, resorting to a deep reactive ion etching (DRIE) tool. The structural characterization was mainly carried out by scanning electron microscopy, although ellipsometry has also been used. RTP refers to any process that implies elevating the temperature of a given material, mainly semiconductors, to high values during short periods (minutes or even less). As such, it can be used as a multi-functional and versatile microfabrication tool, capable of performing rapid thermal oxidation, hydrogenation, annealing and nitridation, among others. The project focused on the first three, which led to several experimental studies. According to the results, the atom migration phenomenon was witnessed in both 5% hydrogen/argon-ambient and argon-ambient rapid thermal annealing (RTA). Thus, it resulted in either three-dimensional (3D) profile transformation or silicon-on-nothing (SON) structures due to empty-space-in-silicon (ESS) formation. However, silicon volume loss was reported, possibly caused by sublimation and etching by reaction with oxygen (O_2). Furthermore, the tool was able to grow uniform silicon oxide (SiO_2) thin films – below 17 nm and 20 nm for Si (100) and Si (110) surfaces, respectively. The removal of previously grown black silicon (BSi) was also accomplished by RTA, with some margin for improvement. In general, a better understanding of these techniques will allow for their insertion, for instance, into the metal-oxide-semiconductor (MOS) and micro-electromechanical systems (MEMS) devices manufacturing process and the large-scale integrated circuits world.

Keywords: Rapid thermal processing; argon anneal; hydrogen anneal; surface atom migration; SON structures; 3D profile transformation; oxidation; BSi removal; CORE sequence.

RESUMO

Mundialmente, o silício (Si) é dos materiais mais utilizados na indústria de dispositivos semicondutores, sendo que um substrato pode ser submetido a vários processos até ser atingido um produto final, incluindo tratamentos térmicos. Neste trabalho, um processador térmico de rápido aquecimento - pressão base de 10^{-6} mbar - é estudado e proposto como alternativa à utilização de fornos convencionais. Assim, o principal objetivo é investigar o impacte que processamentos térmicos de curta duração (RTP) podem ter em estruturas com elevada razão de forma, fabricadas em substratos de silício. Com esse propósito, a sequência "*clear – oxidize – remove – etch"* (CORE) foi utilizada como principal processo de erosão, utilizando um equipamento dedicado a erosão reativa iónica em profundidade. Para a caracterização recorreu-se maioritariamente a microscopia eletrónica de varrimento, embora também se tenha recorrido a elipsometria. RTP refere-se a processos que impliquem aumentar a temperatura de um dado material, normalmente semicondutores, até valores elevados, num curto espaço de tempo (minutos ou mesmo segundos). Deste modo, pode ser utilizado como uma ferramenta multifuncional e bastante versátil, capaz de efetuar oxidação térmica, hidrogenação, recozimento, nitrogenação, entre outros. Neste projeto, focaram-se os primeiros três, conduzindo a vários estudos experimentais. De acordo com os resultados, o fenómeno de difusão atómica do silício, pela sua superfície, em estado sólido, foi presenciado, quer utilizando 5% hidrogénio/árgon ou apenas árgon como ambiente para recozimento térmico de curta duração (RTA). Assim, foi presenciada a transformação tridimensional (3D) das estruturas em silício ou a formação de espaços vazios no interior do Si (ESS). Contudo, foi reportada perda de volume de silício, possivelmente causado por sublimação e erosão por reação com oxigénio. Adicionalmente, foi possível obter filmes finos uniformes de óxido de silício – abaixo de 17 nm e 20 nm em superfícies Si (100) e Si (110), respetivamente. A remoção de *black silicon* (BSi) foi também conseguida através de RTA. De uma forma geral, aprofundar o conhecimento sobre estas técnicas permitirá a sua inserção, por exemplo, no processo de fabricação de dispositivos MOS e MEMS e no mundo de circuitos integrados à grande escala.

Palavras-chave: processamentos térmicos de curta duração; recozimento com árgon; recozimento com hidrogénio; difusão atómica superficial; estruturas SON; transformação estrutural 3D; oxidação; remoção BSi; sequência CORE.

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ACRONYMS

3D	three-dimensional
AR	aspect ratio
a-Si	amorphous silicon
BARC	bottom anti-reflective coating
BSi	black silicon
CORE	clear – oxidize – remove – etch
CPR	center point run
Dedam	de-damage
DRIE	deep reactive ion etching
DTU	Technical University of Denmark
DUV	deep ultra-violet
EHT	electron high tension
ESS	empty-space-in-silicon
Fin-FET	fin field-effect transistor
HAR	high aspect ratio
IC	integrated circuit
ICP	inductively coupled plasma
IR	infrared
RIE	reactive ion etching
RTA	rapid thermal annealing
RTN	rapid thermal nitridation
RTO	rapid thermal oxidation
RTP	rapid thermal processing
SEM	scanning electron microscope
SOI	silicon-on-insulator
SON	silicon-on-nothing
SOS	silicon-on-sapphire
MEMS	micro-electromechanical systems
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field effect transistor

MSE mean squared error

MSTS microstructure transformation of silicon

VASE variable angle spectroscopic ellipsometry

MOTIVATION AND OBJECTIVES

Alternatively to conventional furnaces, a rapid thermal processor can reach elevated temperatures in a short period, under several different process environments. It can perform rapid thermal annealing (RTA), rapid thermal oxidation (RTO), and rapid thermal nitridation (RTN), among others. The unique characteristics associated with rapid thermal processing (RTP) allow for a reinvention of conventional techniques and approaches, which can be translated into optimized microfabrication process flows.

As such, RTP has been revealed as key in metal-oxide-semiconductor (MOS) devices fabrication. For instance, RTO and RTN are of great interest in producing high-quality thin-film oxides [1] and nitrides [2] - these are mainly used as gate dielectric materials [3]. During the thermal processing, the diffusion of any dopants present in silicon (Si) substrates is minimized and the thermal budget on the wafer is reduced [1]. Besides, RTP tools have been of great value in studying the kinetics involved in silicon dioxide (SiO_2) growth in the thin-film regime, as the processing time is short and suitable for research work [1]–[5]. On the other hand, rapid thermal annealing in hydrogen (H_2) ambient has been proven helpful in transforming and precisely controlling Si features' shape to fabricate three-dimensional (3D) devices. This process is particularly relevant for trench gates metal-oxide-semiconductor field effect transistors (MOSFETs) and fin field-effect transistors (Fin-FETs), which can translate into overall improvement of the device's performance – to enhance gate oxide reliability, trench corner rounding and trench sidewall surface smoothing are crucial procedures [6], [7]. To reduce the concentration of electric field and stress at the trench corner, the trench corner curvature must be low [8]. Furthermore, the same H_2-RTA process can be used for sidewall roughness reduction in micro-optical devices, such as optical waveguides and micromirrors, to avoid loss by scattering [9].

Additionally, RTA has also been presented as a method to achieve an ideal silicon-on-insulator structure (SOI), as it beholds the lowest dielectric constant when compared to other available structures [10]–[12]; used in not only integrated circuit (IC) technology but also in micro-electromechanical systems (MEMS) [13, 14]. SOI structures have been the preferable approach in MOS devices for high-speed and low-power applications [10]–[12]. Nevertheless, the fabrication methods represent a high cost when producing large-scale ICs due to the prior required preparation of specific substrates. Furthermore, creating Si layers free from crystal defects - either caused by ion implantation or induced during the epitaxial growth process – is difficult [10], [11]. Hence, instead of introducing a buried oxide layer, the formation of an empty cavity was proposed. The silicon-on-nothing (SON) structure minimizes the parasitic capacitance and leak current through the p-n junction between the transistor and substrate in IC technologies, such as MOSFETs, preventing the deterioration of the operation speed and power efficiency [14]. The reduction is insufficient when using silicon-on-sapphire (SOS) or SOI structures [14]. With SON, the transistor is placed on a vacant region that can be fabricated 1) by resorting to complex etching sequences after the device is manufactured, which is unsuitable for large-scale ICs. Besides, achieving and controlling the desired shape is challenging [10], [11]; 2) due to empty-space-in-silicon (ESS) formation caused by atom migration through the Si's surface [10], [11], which is promoted by H_2-RTA.

This work aimed to explore a research RTP tool's capabilities and how it can be used as a multi-functional and versatile microfabrication tool. Besides, little to no previous knowledge was associated with the equipment. Hence, contributing with results would considerably ramp up the tool's learning process and expand its use for possible applications mentioned above, composing yet another main objective.

1 INTRODUCTION

1.1 Heat treatments in Microfabrication

Heat treatments are a fundamental step in micro and nanoscale silicon devices fabrication. They are mainly used in the patterning step (soft bake, hard bake and development), doping step (post ion implant anneal) and layering step (post metal deposition and patterning annealing) [15]. Besides, they are essential to induce oxidation, solid-state diffusion and many other physical changes in the silicon and its overlayers [16]. During heat treatments, there is no addition or removal of materials from the wafer; apart from the evaporation of some contaminates or solvents from its surface, the wafer is simply heated or cooled [15].

In contrast to the radical changes that have occurred in areas like lithography, etching and epitaxy, heat treatment technology didn't proportionally evolve. Between 1968 and 1978, the first international conference on Laser Processing of Semiconductors took place – the under-development heating technique involved exposing a silicon surface to a pulsed laser for 20 to 50 nanoseconds. Between 1978 and 1982, a wide range of other radiant heating sources was explored, including continuous lasers and electron beams (scanned or unscanned), lamps (both filament and arc) and even ion beams [16].

Nowadays, all these systems continue under investigation and development, but conventional furnace systems are still the industry's standard process. The batch furnace method allows for resistive thermal exposure of multiple wafers simultaneously. Also, it guarantees better thermal stability and process stability time. However, its two main disadvantages lie in long exposure periods as well as overall process time - it can take several hours to complete one cycle [17]. Therefore, the need for thermal cycle time reduction and improvement in temperature-control accuracy arises and RTP becomes relevant and indispensable in the present day. This method has replaced conventional furnace systems to satisfy device and production requirements for reduced thermal budget, process uniformity, high throughput, ease of process development and low manufacturing cost. These systems also present compatibility with single-wafer processing [18], high performance, high reliability, and low cost of ownership and operation [19].

1.2 Rapid Thermal Processing

Rapid thermal processing, RTP, is the given name to any process that implies elevating the temperature of a given material, mainly semiconductors, to high values during short periods (minutes or even less) [17], [20]. This technology has a fundamental role in fabricating silicon-based micro and nanoscale devices. It can be used, for instance, to form metal nitrides (RTN), for silanization, post-ion implantation annealing, dopant activation, thin-film oxide layer growth (RTO) and annealing (RTA) [18], [20]. More specifically, RTA refers to short-duration heat treatments in the solid phase, thus, without melting the wafers [20]. Usually, it is used as a complementary step after ion implantation to eliminate crystal defects by annealing and to activate impurity dopant species previously introduced in the wafer [19].

RTA is characterized as a single-wafer process[17], [20], which means each wafer is heated individually in the chamber. The main challenge of abandoning conventional furnaces and opting for thermal cycles that have fast, controllable rates led to the creation of an infrared (IR) spiking process. The process is based on fast-rate heating and cooling of the wafer by exposing it to a transient flux of IR radiation from an array of incandescent lamps. The term 'spiking' refers to the sharply peaked function obtained: temperature as a function of time.

For this method, graphite heaters, microwave, plasma arc, and tungsten halogen lamps can be used as heat sources, whereby tungsten halogen lamps are the most often used [15]. The lamps are comprised of tungsten filaments, kept inside quartz envelopes, and protected by an halogen-atmosphere ambient. This source is considered to have a long working lifetime and emits radiation from the visible region to the near-IR of the electromagnetic spectrum [20].

Two possible methods to measure the substrate's temperature are thermocouple junctions and IR radiation pyrometry. Thermocouples are contact temperature probes, usually used to measure process temperatures and play an essential role in sensor calibration as temperature references. Nonetheless, the probes are not the most convenient method in single-wafer rapid systems because they require back contact with the wafers, which also implies thermal contact resistance that leads to unreliable measurements and may have a longer response time than some RTP cycles [15], [20]. Therefore, the preferred one of the two available methods is IR radiation pyrometry, corresponding to the one available on the tool used for the present work (Figure 1). Optical pyrometers determine the temperature of the wafer by analyzing part of the radiation that is thermally emitted by the wafer, that is, determine the emissivity. Thus, a non-contact measurement with high precision is achieved. However, this method tends to be more complex, as the heater and quartz components contribute with parasitic reflections that need to be considered in the wafer emissivity measurement. Additionally, especially on wafers with distinct layers, it is difficult to relate the emitted radiation by the wafer to its actual surface temperature because emissivity variations result from differing heat transfer rates [15], [20].

Temperature control is a fundamental and critical key in this kind of processing, yet some difficulties must be addressed to achieve reliable measurements. When a wafer is subjected to a rapid thermal process, it never achieves thermal stability. To worsen the situation, the edges of the wafer tend to receive less radiation than its centre and have a more significant radiative emission [20]. Additionally, if the wafer has already undergone some other fabrication steps, there is another problem that results from the number of layers of the wafer and the difference between them. Different layers absorb light differently, meaning these differences result in a nonuniform temperature across the wafer. Wafer emissivity is the term for this phenomenon, characteristic of both the material and the heating radiation wavelength. This nonuniform temperature does not allow a uniform heat treatment inside the wafer nor at its surface. Strategic lamp placement, individual lamp control and usage of top and bottom lamps are critical to solving these issues [15].

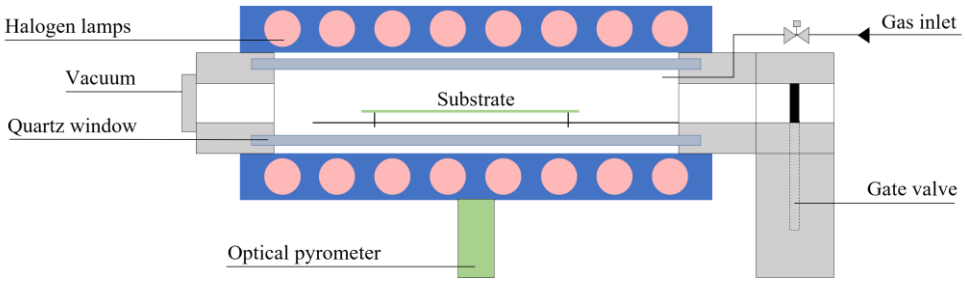

Figure 1 - Schematic representation of the RTP chamber's profile view (Rapid Thermal Processor AS-Premium from ANNEALSYS). The substrate (in green) rests on top of three quartz pins, supported by a quartz holder (in black). The drawing is not to scale.

For instance, this work was based on an RTP tool with a top and bottom halogen lamp-configuration, as shown in Figure 1, maximizing the thermal equilibrium inside the chamber. Hence, temperature nonuniformity issues are minimized. Moreover, since optical pyrometry does not require contact with the wafer and the chamber is enclosed by two quartz-windows, temperature measurements do not disturb the required thermal equilibrium. Besides, the chamber is only connected to two external vacuum pumps, to a gas line and the loadlock – in front

of the chamber, separated by the gate valve. While processing, the valve is closed, preventing any disturbance; it is only opened to exchange the substrates when both chamber and loadlock are under vacuum.

1.3 Si Atom Migration Phenomenon

The performance of short-period and high-temperature processes, on Si substrates, under an H_2-ambient atmosphere has been extensively studied [6], [9]–[11], [21]–[24] throughout the years. Seemingly, the microstructure of the silicon surface can be altered into different shapes by using H_2 annealing on Si substrates that have been etched using the reactive ion etching (RIE) technique – microstructure transformation of silicon (MSTS) mechanism firstly proposed by Sato *et al.* [21]. The atom diffusion along the Si's surface takes place, so its total surface energy is minimized, causing the rounding of the corners of any existing surface feature [6], [10], [11], [21], [23], without volume loss [9]. In other words, the Si is reshaped into an ideal, more stable curvature that lowers its surface Gibb's free energy [25], [26]. Figure 2 shows an illustration of this occurrence.

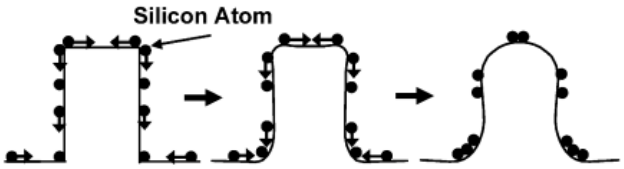

Figure 2 – Schematic representation of the atom migration mechanism through a silicon surface, during hydrogen annealing, at high temperature and low pressure. Source: Lee and Wu [9]. Copyright © 2006 IEEE Journal of Microelectromechanical Systems.

The Si atom migration mechanism, also known as Si surface migration or surface self-diffusion, occurs at elevated temperatures, below the Si melting point (1414 ºC). Using H_2 as process gas, it takes place at temperatures between 900 ºC and 1100 ºC and pressure conditions from 10 to 760 Torr (≈13 mbar to ≈1000 mbar) [25]; however, it is enhanced when using low pressures and high temperatures, for 1 s to 10 min [21], [23]. As mentioned by Kant *et al.* [25], there's a shortage of tools capable of providing these kinds of environments when processing a whole wafer, enhancing the necessity to look for alternative process gases, under which surface migration is also induced. As a result, the rapid thermal processors would be less complex, less expensive, and allow to abandon the use of unsafe environments. Other experimental works have discussed the use of noble process gases [25]–[28] as an alternative to explosive hydrogen gas. Although in earlier stages of investigation, the same self-organized diffusion phenomenon has been reported.

Depending on the silicon features, the atom migration can lead to 3D profile transformation, sidewall roughness reduction and the formation of SON structures. 3D profile transformation can be achieved when the silicon structure dimensions are smaller when compared to the surface self-diffusion length, which leads to the reshaping of the silicon into a spherical geometry. On the other hand, if the structure dimensions are comparable or much greater than the surface self-diffusion length, the rounding only happens at the edges, allowing for overall shape maintenance [9]. That is the case when hydrogen-annealing is applied for sidewall roughness reduction on high aspect ratio (HAR) features, etched using deep reactive ion etching (DRIE) sequences, such as the Bosch process[29], [30] or the newly developed 'clear – oxidize – remove – etch' (CORE) process [31].

The CORE process is a fluorocarbon-free directional silicon dry etching process, requiring a switching sequence of sulfur hexafluoride (SF_6) and O_2. This process is similar to the well-established Bosch process [29], [30] - both in function and results - but replaces the usual octafluorocyclobutane (C_4F_8) passivation (polymerization) by O_2 passivation (silicon self-limiting oxidation). Compared to other room temperature and cryogenic

mixed RIE processes, its advantages are higher etch selectivity, pattern independency of etching profiles and success operating at room temperature. Additionally, it eliminates the deposition of fluorocarbon residues at the topside of deep-etched or nano-scale features and on the reactor wall, keeping it clean and minimizing any process drift. Replacing the non-green C_4F_8 for O_2 is also essential to finding environmental sustainability in the dry-etch world [31]. The scallops caused by either of these etching sequences can be removed based on the sidewall roughness reduction principle by H_2-annealing [9], [26].

The SON structures can be fabricated, for instance, based on the MSTS technique. The most crucial element in their fabrication is the original inlet form that was patterned on the Si substrate. When the inlet or set of inlets' structure is annealed in a deoxidizing environment, such as H_2, a transformation takes place to reduce the surface energy – Si surface migration. The ESS phenomenon is the outcome of the inlet's transformation; the most-common products are spherical, pipe-shaped and plate-shaped ESS [10], [11], visible in Figure 3.

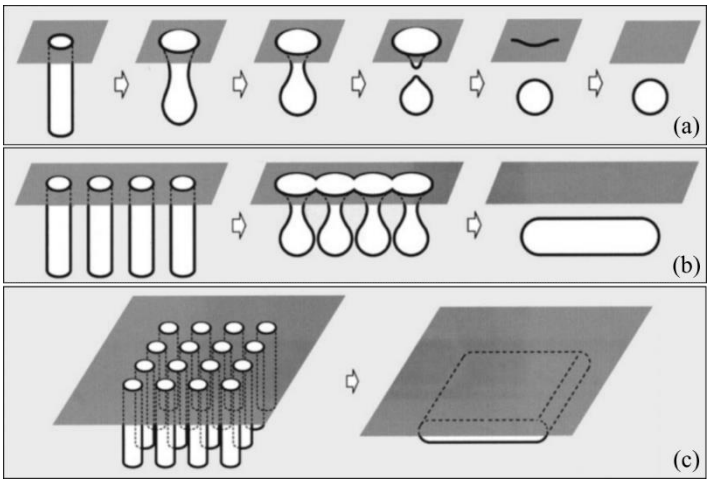

Figure 3 – Schematic representation of the three most common ESS fabrication mechanisms: (a) spherical, (b) pipe-shaped and (c) plate-shaped ESS. Modified from Mizushima *et al.* [10]. Copyright © 2000 American Institute of Physics.

A spherical ESS is created from a singular, deep inlet, as shown in Figure 3(a). The smallest radius of curvature is situated at the top and bottom corners of the first-stage feature; hence it is where the spherical ESS initiates its formation. One can also conclude the final ESS depth is shorter than the initial well depth and that the originated spherical ESS's diameter surpasses the initial trench's diameter. As a result, when there is a combination of aligned side-by-side deep inlets (Figure 3(b)), each pit will evolve as described before and originate a spherical ESS at the bottom. However, as they are closely spaced, they will combine and coalesce between each other, forming a buried channel shaped like a pipe. For the last situation represented in Figure 3(c), instead of individual pits or pits arranged in a line, there's an array of deep-etched inlets [10], [11]. Similarly, all the generated spherical ESSs at the bottom combine and a large, buried cavity, shaped like a thin plate, is formed.

The ESS structure shape can then be influenced by the initial layout of the etched features, in other words, by the distance and positioning between inlets [10], [11], [22]. Producing these kinds of buried features is only possible using HAR etched features and a masking layer that can sustain the annealing process and suppress the surface migration on the sample's surface [21]. In fact, the spherical ESS formation is reported by Sato *et al.* [11] only to occur when the initial inlet aspect ratio (AR) is located between ≈ 3 and ≈ 9.5. Above 9.5, many sphere-shaped ESS can be formed vertically aligned, depending on the AR. These considerations were essential for this study. The next sections follow the description of the carried experimental work, whereby most of the processes mentioned in this section and literature were attempted and explored.

2 MATERIALS AND METHODS

2.1 Rapid thermal processor: Additional remarks

A Rapid Thermal Processor (RTP AS-Premium, serial number AS0415C4 - 7484, from ANNEALSYS), with a base pressure of 10^{-6} mbar, was used (Figure S1). The optical pyrometer measurements range from 400 ºC to 1300 ºC, either using silicon wafers or silicon wafers coated with silicon nitride (Si_3N_4). The usage of the latter was adopted to prevent the harm of the tool, further discussed in more detail. It is also important to mention the temperature inside the chamber can be controlled either by fixing the power irradiated by the lamps or the measured temperature by the pyrometer – power control mode and temperature control mode, respectively. In other words, using power control mode, the tool is programmed to fix the lamp's power at a specific value (in percentage) and consequently, the temperature inside the chamber varies with time; using the temperature control mode, the tool is programmed to vary the lamps' power to maintain the temperature stable and constant inside the chamber at a previously established value in the recipe. As available gases, there is argon (Ar), 5% H_2/Ar, oxygen (O_2) and ammonia (NH_3) and 2000 SCCM is the maximum flow permitted for each gas line. Pressure-wise, it can be controlled by the valve's position or by establishing a maximum pressure that should be maintained constant during the process. Lastly, in cases where small chips are processed, bonding to the carrier it's not required; the chips are placed on the wafer.

2.2 Fabrication Methods

Si <100> wafers (phosphorous-doped n-type, 1-20 Ωcm, single side polished, 150 mm diameter, 675 µm thick) were used as the substrate throughout this work. The fabrication process flow can be found in Figure S2.

2.2.1 High aspect ratio features: Trenches, Nanoholes and Black Si Nanoholes

Two different multi-layered stacks were used as starting points to fabricate HAR trenches, nanoholes and black silicon (BSi) nanoholes. Both types were previously manufactured by other users in Technical University of Denmark (DTU) Nanolab and are shown in Figure 4.

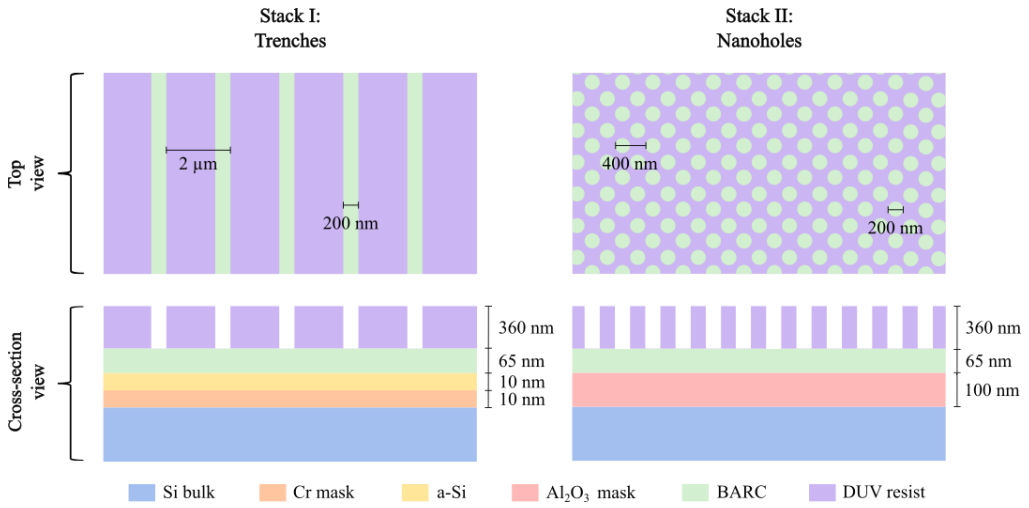

Figure 4 - Schematic representation of the two different multi-layered stacks used as starting points to fabricate HAR features. The drawing is not to scale.

Stack I comprised the Si <100> wafer as substrate, a sputter-coated 10 nm chromium (Cr) hard mask layer, a sputter-coated 10 nm intermediate amorphous silicon (a-Si) layer, a spin-coated 65 nm bottom anti-reflective coating (BARC) layer and a spin-coated 360 nm deep ultra-violet (DUV) resist layer. The resist was already exposed and patterned with 200nm-width and 2µm-pitch trenches. Stack II was very similar. However, it comprised a 100 nm aluminum oxide (Al_2O_3) layer (deposited by atomic layer deposition) as a hard mask, a spin-coated 65 nm BARC layer and a spin-coated 360 nm DUV resist layer, patterned with 200nm-diameter and 400nm-pitch holes. The Cr hard mask was abandoned due to some limitations found in both etching and rapid thermal processing.

Using a diamond pen, the Stack I (Trenches) wafer was manually broken into 1 cm x 1 cm samples so each chip could be processed and tested individually. None of the layers was removed before this step. The chips were etched using a DRIE tool (Nemotek Advanced DRIE Pegasus 2, serial number MP0641, from SPTS) in a single-run multi-step program. All parameters were optimized for each step and are displayed in Table S1, whereas the tool is shown in Figure S3. A 'BARC strike' step and a gentle de-damage (Dedam) etch step were added to strike and stabilize the plasma and remove any residues, dust or particles lying on top of the sample. Once 5µm-deep and 300nm-wide trenches were etched into the silicon, the Cr hard mask was removed, by RIE, using the same tool and identical parameters from the Cr etch recipe already shown. However, it is important to mention that the a-Si and Si etch steps were achieved using the CORE process.

The etched samples were annealed, under a 40 SCCM argon atmosphere, using the rapid thermal processor at ≈ 1300 ºC (80 % of lamp power), pressures of 0.18 mbar and 12 mbar, for 8 s up until 3 min. Some samples were covered with a same-material chip, others were placed facing the carrier wafer, and others were dipped in a 5% hydrogen fluoride (HF) bath before annealing.

In the Nanoholes case, the Stack II wafer was processed as a whole. Only the BARC layer is initially etched using the DRIE tool and the same parameters mentioned before (Table S1). After this step, the hard mask layer is etched using a different dry etch inductively coupled plasma (ICP) tool, primarily dedicated to etching III-V materials (III-V PRO ICP, serial number MP0647, from SPTS). The equipment is presented in Figure S4. The samples were etched using a switching sequence of Ar and boron trichloride (BCl_3), then etched under constant chlorine (Cl_2) atmosphere and finally underwent an O_2 clean on the DRIE tool. The process parameters are shown in Table S2. These three consecutive processes would allow not only to transfer the pattern into the hard mask but also to etch the DUV resist and the BARC layer without leaving any residues. However, the two last steps were discarded as the DUV/BARC etch could be achieved during the subsequent Si etch step on the DRIE tool. An additional 10 minutes, under identical conditions (Table S2), were required on one of the Stack II wafers (not from the same batch as the other wafers and used to produce BSi nanoholes); 260 minutes revealed insufficient to etch the hard mask and reach the silicon. Once all these steps were completed, the Stack II wafers (Nanoholes and BSi Nanoholes) were equally broken into 1 cm x 1 cm samples. The exposed Si was then etched using the DRIE tool. The HAR nanoholes were achieved using the ORE process - identical to the CORE process already described, except the 'Clear' step is removed and an 'Etch delay' step (E_1) is added – according to the recipe shown in Table S3. On the other hand, a different CORE process was used to produce BSi at the bottom of the nanoholes (Table S4).

The nanoholes samples were then submitted to different rapid (4 s to 40 min) and high temperature (1000 ºC to 1300 ºC) processing using the rapid thermal processor. The pressure conditions varied between 0.18 mbar and 74 mbar. The process gases (Ar, 5% H_2/Ar, O_2) and correspondent flows (between 40 and 2000 SCCM)

were changed according to the carried study. The BSi nanoholes samples were also finalized using the rapid thermal processor for periods from 1 to 60 seconds. These experiments required high temperatures - 1000 ºC, 1100 ºC, 1200 ºC and 1300 ºC – and both high and low pressures - 43 mbar and 0.18 mbar when using, respectively, 2000 SCCM Ar and 40 SCCM Ar and 1.50 mbar when using 40 SCCM 5% H_2/Ar.

2.2.2 BSi wafer

A Si <100> wafer was placed inside the Pegasus 2 plasma etching tool, with its unpolished side facing the chamber ambient. A small area of the wafer was covered using a square-shaped chip, placed on top without bonding. Next, the wafer was submitted to etching using a CORE sequence whose parameters are presented in Table S5. The recipe was optimized in a way that intentionally creates Si grass, that is, black silicon. In this case, the ICP power (DRIE mode) was used to achieve a faster directional etch rate [31]. Then, the BSi wafer went through a 'clean BSi' process, on the rapid thermal processor tool, at ≈ 1300 ºC (80 % of lamp power), 0.18 mbar and 40 SCCM Ar, during 8 s.

2.3 Oxidation wafers

These samples were used as starting point for the oxidation study. Foremost, the native SiO_2 present on the surface of the Si <100> wafers was removed by wet etching for 20 s using an oxide etch bath. The bath contained buffered HF (BHF) with surfactant (12% HF with ammonium fluoride etching mixture) and had an oxide etch rate of 75-80 nm/min. The etch was followed by a 5 min-rinse sequence with deionized water in another dedicated bath. Once they were dry, using a spin dryer, the wafers were ready to be processed on the RTP tool. It's worth noting the interval between preparing and processing the wafers should be as short as possible so there's no native oxide growth in between. To study the SiO_2 thickness growth by RTO on silicon wafers as a function of oxidation time, it was necessary to perform three rounds of RTO experiments – each round comprising both short and long oxidation processes (from 0 s to 40 min) - in which every completed RTO process had the temperature fixed at 1200 ºC, pressure at 12 mbar and an oxygen flow at 1500 SCCM. However, during the final round, one of the equipment's quartz plates broke, and the experiments could not be completed.

2.4 Characterization Methods

The small chips (Nanoholes, BSi nanoholes and Trenches samples), as well as the BSi wafer, were manually cleaved (parallel to the plane direction <110>) using a diamond pen. Thereby, it was possible to observe the cross-section of each sample using a scanning electron microscope (SEM) (Zeiss Supra 40VP SEM, serial number 4825). The tool is shown in Figure S5. All SEM images were taken using a secondary electrons detector (InLens detector), which was adequate for short working distances, obtaining good contrast and a better resolution. Before RTP and cleaving, the BSi wafer was also photographed.

Regarding the oxidation wafers, since the goal was to establish the correlation mentioned before, ellipsometry was the most suitable technique to resort to. Using a variable angle spectroscopic ellipsometry (VASE) ellipsometer (M2000XI-210 ellipsometer from J.A. Woollam Co., Inc.), it was possible to study the uniformity of the thermally grown SiO_2 thin film but also get its average thickness (acquired from a 9-point measurement). The ellipsometer is presented in Figure S6.

3 RESULTS AND DISCUSSION

The studied RTP tool is a research tool from which there was little knowledge of its capabilities as microfabrication equipment and its effects on HAR Si features or even on plain Si (100) wafers. Thus, the experimental work was considered a learning period about the tool. Consequently, many approaches were taken to investigate it. Five main topics were studied: RTA using Ar as the only process gas, a comparison between using Ar and an Ar/H_2 mixture, the physical mechanisms associated with RTA, the smoothing process of BSi by RTA and the capabilities of RTO processing. The corresponding results are presented and explained in this section.

3.1 RTA: Argon Study

This study aimed to understand if one could achieve the same atom migration phenomenon described in the literature by RTA but using only Ar as process gas instead of H_2. Consequently, the first RTA recipes were created using 40 SCCM of Ar flow, 0.18 mbar and 80 % of lamp power (≈ 1300 ºC), resorting to the power control feature.

As a result of the unfamiliarity with the allowed materials inside the RTP chamber, the Cr hard mask layer was removed before processing the samples, as described in the previous section. Hence, the starting point for this study is a batch of mask-stripped samples, identical to the ones represented in Figure S7(B) and Figure 5 - Si trenches 5-µm deep and 300-nm wide, resulting in an AR of approximately 17. Nonetheless, the effect of RTA recipes on Cr was investigated using trenches samples that did not have the Cr mask stripped before undergoing RTA processing (Figure S7(A)). As a result, as visible in Figure S8, the Cr layer crumbles and leaves the underneath silicon exposed to the chamber ambient. This occurrence confirmed that Cr is not suitable as a masking material for this type of high-temperature process and that its removal was necessary before any following RTP process.

As revealed by Figure 5, using the already mentioned recipe, for only 3 minutes, allowed for an entirely 3D profile transformation, from deep trenches to smooth semi-round droplet structures. As explained, this occurrence might be due to the Si surface self-diffusion, also present in H_2-ambient annealing above 1000 ºC.

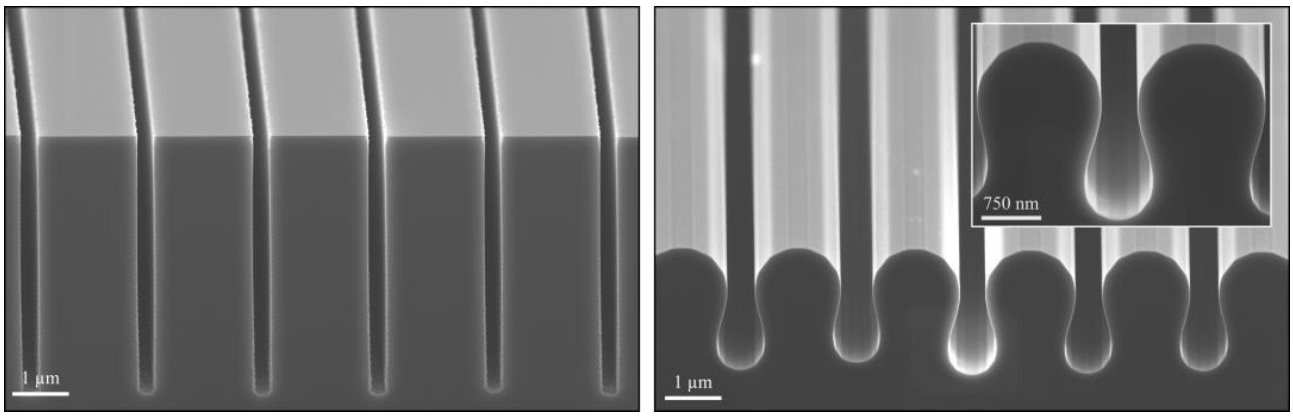

Figure 5 - 3D profile transformation achieved by 3-minute RTA using 80 % of lamp power (≈ 1300 ºC), 0.18 mbar and 40 SCCM of Ar flow. The sample was covered with an identical (in size) Si chip during the process. Left: initial state, without Cr mask. Right: post-annealing state. Cross-section SEM images, 20º tilt and EHT 5 kV.

Exploring the same sample, it was also possible to find a series of almost-spherical buried holes parallel to the (100) plane (Figure 6), with the direction of the previously etched trenches. However, the area where these buried features were found was surrounded by faceted droplets, which were not closed at the top. The lithography and etch steps might have influenced this different result. If the hard mask was not correctly patterned during the lithography in this area, it might have resulted in semi-closed or narrow trenches. However, the trench opening had to be enough for the Si etch step to occur. These factors combined allowed for the formation of trenches etched into the Si, similar to the surrounding ones, but with margins closely spaced at the top. Hence, the top-part reshaping and closure, induced by the atom migration during the RTA process, were facilitated.

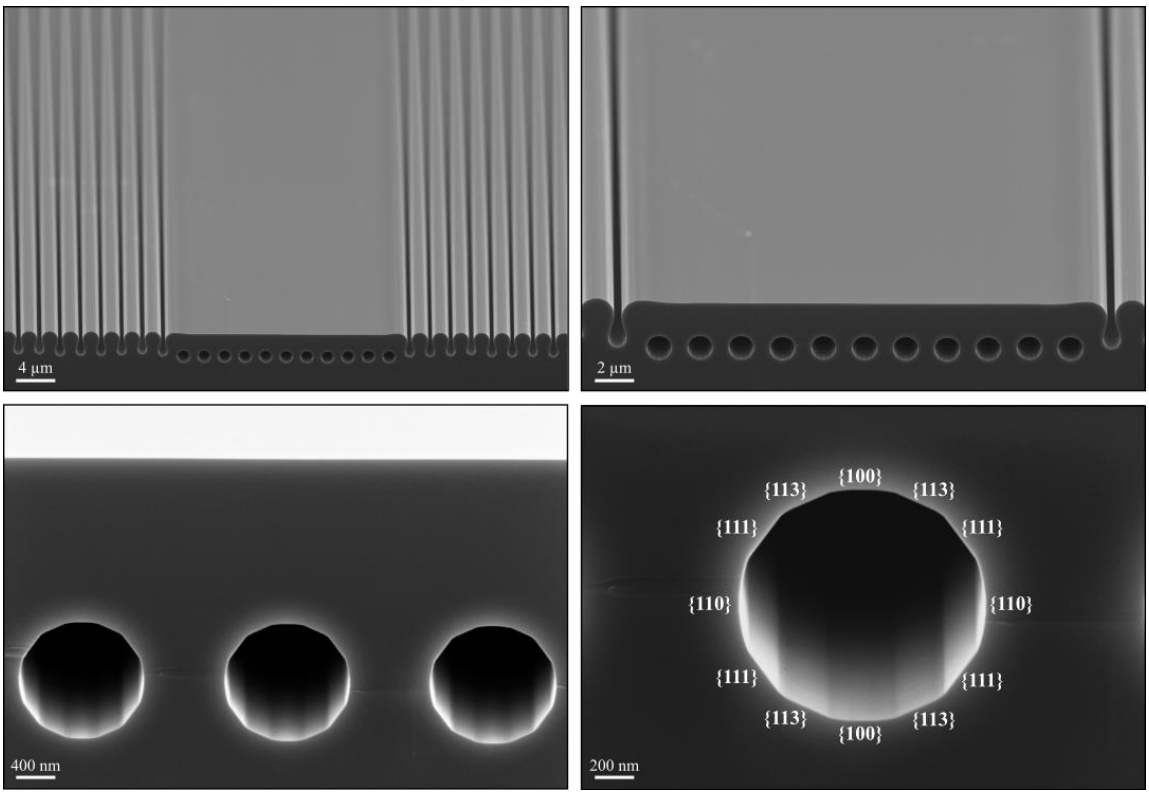

Figure 6 - Area of the post-annealing sample (3-minute RTA, 80 % of lamp power (≈ 1300 ºC), 0.18 mbar, 40 SCCM Ar) where faceted buried holes were found. The sample was covered with an identical (in size) Si chip during the process. Indication of the corresponding crystallographic directions is on the bottom-left image. Cross-section SEM images, 20º tilt and EHT 5 kV.

In both types of structures, droplets and holes, the silicon crystal planes are visible, indicating that the atom migration phenomenon is affected when the planes are reached. As a result, neither the droplets nor the holes are completely round and smooth. Ott *et al*. [32] also found these faceted features, in which pores with a faceted geometry would appear after annealing porous Si layers at 1070 ºC in an H_2 atmosphere. In this case, as visible in Figure 6, all facets are approximately the same length (in the order of 300 nm) and belong to the {100}, {113}, {111} and {110} plane families, reaching silicon's most stable form [22], [33], referred as the '*equilibrium shape of silicon'* by Eaglesham *et al.* [34].

In most processed samples, at the edge of the sample, where the patterned area meets the non-patterned area, it is common to find a third type of feature – faceted voids (Figure 7). These are identical to the ones reported by Sudoh *et al*. [22]. The voids differentiate from the faceted holes because the atom migration mechanism is interrupted before the coalescence of two voids by lateral expansion. The appearance of faceted voids may be

related to another type of hard mask defect, causing the opening of the trenches to be interrupted, that is, connected at the top part in only some places. Instead, the etching would produce a series of individual aligned holes that, after RTA, would close by distension of the area around it [22] and evolve into the shape of a faceted void before reaching the surrounding ones.

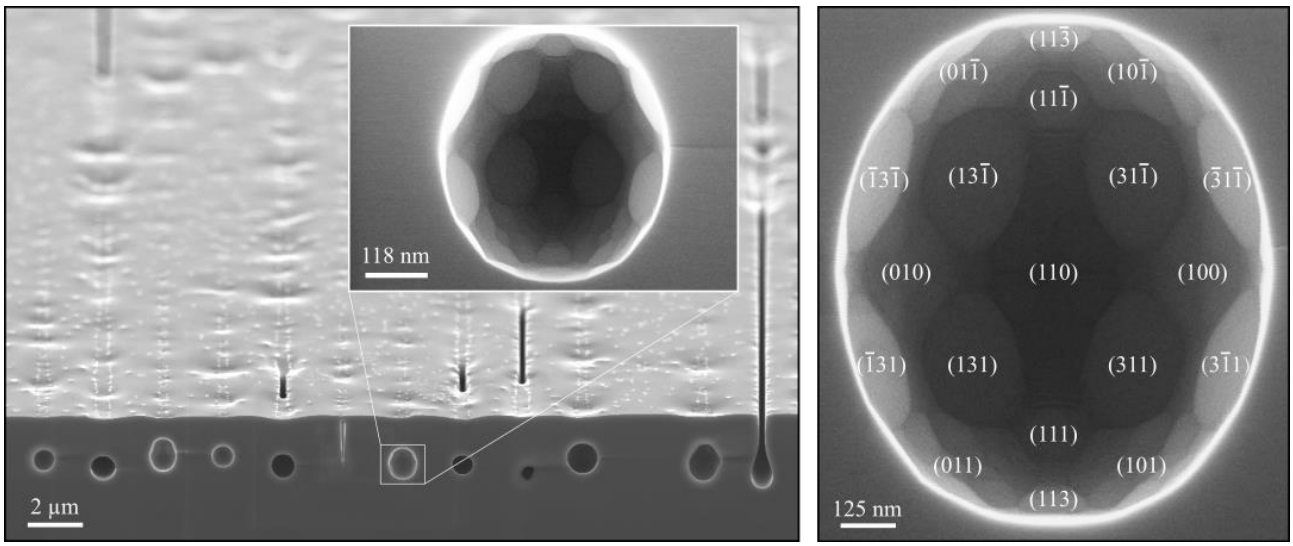

Figure 7 – Faceted void found at the edge of a sample rapid thermal annealed for 60 s (80 % of lamp power (≈ 1300 ºC), 0.18 mbar, 40 SCCM Ar), with the indication of Si crystallographic planes. Cross-section SEM images, 20º tilt on both the pictures on the left and 0º tilt on the right, EHT 20 kV.

Furthermore, the trenches samples were put through a series of subsequential experiments – following the order presented in Figure 8 – in which the Ar gas flow, pressure and lamp power were the fixed parameters and the processing time the differing parameter. The effect of dipping the samples for 30 s in HF, immediately before RTA processing, has also been tested. Additionally, the influence of keeping the samples facing the chamber ambient *vs* flipping them (i.e., facing the Si carrier wafer) was studied. By observation of Figure 8 (a), (b) and (c), it is possible to say the longer the time, the wider the droplet and the shorter the distance to the surface. It is also visible an increase in the sample's surface roughness as the processing time is increased.

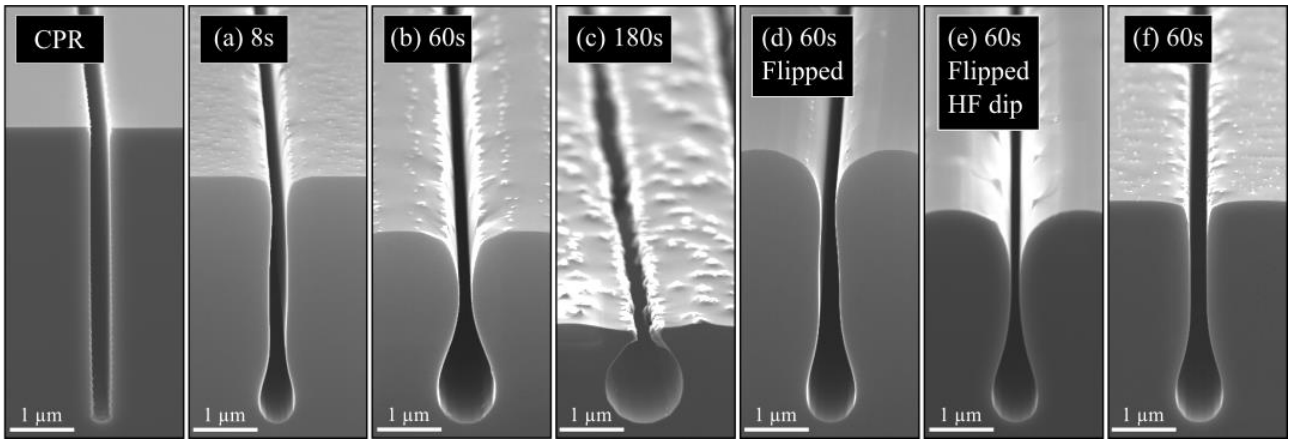

Figure 8 – Influence of process time, prior HF dip and flipping the samples during an RTA process (80 % of lamp power (≈ 1300 ºC), 0.18 mbar, 40 SCCM Ar). All features were aligned at the bottom as a way of comparison, between each other and with the centre point run (CPR). Cross-section SEM images, 20º tilt, EHT 1 kV in (c), EHT 5 kV in (CPR), (e), (f) and EHT 20 kV in (a), (b), (d).

In contrast, comparing two samples, one facing the chamber ambient and the other facing the Si carrier wafer, respectively, in Figure 8(b) and (d), it is possible to conclude the roughness is decreased for the latter. In fact, this approach was used in other samples to get a smoother surface, for instance, in the sample shown in Figure 5 and Figure 6, but instead of flipping the sample, it was covered with an identical (in size) Si chip. Regarding the effect of the HF dip, observing Figure 8(d) and (e), both flipped during the process, there seems to be no substantial difference between the two, in terms of surface roughness and feature shape, only in depth. The purpose was to induce H_2-termination of the Si surface and mimic the effects of an H_2-ambient RTA. As the surface mobility of Si atoms can be enhanced by the presence of heated (<< 1414 ºC) hydrogen [9], it could lead to the formation of a different feature; it was not verified.

Additionally, another sample was submitted to the same 60-second RTA sequence to investigate the process's reproducibility. Analyzing Figure 8(b) and (f), it's possible to conclude that something is preventing the RTA process from producing the same result – the droplet shape is wider in Figure 8(b), and the distance to the surface (depth) is shorter. In addition, the surface roughness seems to be enhanced in Figure 8(f). Hence, these experiments revealed an issue, raising the question of what is causing this non-reproducibility.

There are some indications that the non-reproducibility may be caused by one or the combination of two possible phenomena – Si sublimation and 'burning'. Sublimation refers to the transition between the silicon solid state and its gas state. In contrast, 'burning' refers to the reaction between unwanted oxygen inside the chamber and silicon atoms from the sample's surface, promoting the formation of volatile silicon monoxide (SiO). Consequently, this causes the silicon surface to be etched and as a result, a pure Si surface is left behind. The latter is common in high-temperature processing and low O_2 partial pressures [27], [28], [35], [36], which are the conditions used in this experimental study. For these experiments, the O_2 flow is set to 0 SCCM; nonetheless, it cannot be guaranteed the chamber is oxygen-free during the process.

Foremost, the structure depth differs from sample to sample and, more specifically, is getting shortened as the processing time increases. As seen in Chapter 1.3 and as we will see in Chapter 3.3, a decrease in depth is expected when this type of buried features is formed; however, it's not usually this significant, which indicates some Si volume loss. Besides, the AR of the initial trenches is higher than 9.5, which suggests that more than one spherical ESS would be expected to form if no volume is lost during the process. In addition, after these experiments, the top quartz plate had to be thoroughly cleaned due to some deposited material causing the loss of transparency. The deposited material was considered silicon, most likely sublimated from the 150 mm Si carrier wafers and then condensed on the top plate. The same applies to the exposed silicon on the small chips, however, with only a fraction of the contribution.

Furthermore, keeping in mind the recipes used were in power control mode, it would be expected that the same applied lamp power would lead to identical chamber temperatures for each consecutive experiment. However, a percentage of the energy irradiated from the lamps was being absorbed by the deposited Si instead of being transmitted through the window and absorbed by the sample/carrier wafer. Such was verified - the maximum temperature achieved by the samples dropped 55 ºC between the first and last experiment in Figure 8, all of them receiving, in theory, 80 % of lamp power. In sum, it's plausible to assume that sublimation, 'burning', or both are occurring and that these two phenomena can justify the lack of reproducibility. These assumptions lead to the subsequent study.

3.2 RTA: Sublimation & Burning Study

This experimental work aimed to study the effect of sublimation and burning phenomena more extensively. For that purpose, another set of samples was chosen – nanoholes samples, prepared as described but without the final Si etch step. A picture of the samples - 'Nanoholes Virgin'- is presented in Figure 9. As mentioned, due to some limitations of using Cr as a hard mask during the CORE process, Al_2O_3 was the chosen material to replace it. Keeping the hard mask during RTP would allow observing if this alternative material would also be better suitable to withstand processing than Cr. If so, this batch of samples would have the advantage of having only a few spots where the silicon is exposed to the chamber ambient, allowing for a better analysis of the potential Si volume loss; If no alteration were visible in any of the openings on the mask revealing the silicon underneath, then that would indicate that neither of the phenomena was happening. Furthermore, the Si carrier wafers were replaced by single-side polished Si_3N_4 coated wafers. The state of the already-cleaned top quartz window was also monitored.

The initial approach compared the use of lower (40 SCCM + 0.18 mbar/1.5 mbar) and higher pressure (1500 SCCM + 12 mbar) in Ar ambient and Ar with 5% H_2 ambient, at 1100 ºC, for 60 s. It is worth mentioning that, from this study, the RTP recipes are programmed using the temperature control mode, preventing any temperature variation during the process. Additionally, using identical flow and valve position, the minimum value for ambient pressure differs if using Ar or Ar with 5% H_2. Hence there cannot be a direct comparison as the conditions are not precisely similar. Nonetheless, as shown in Figure 9, some nuances are visible in the SEM analysis.

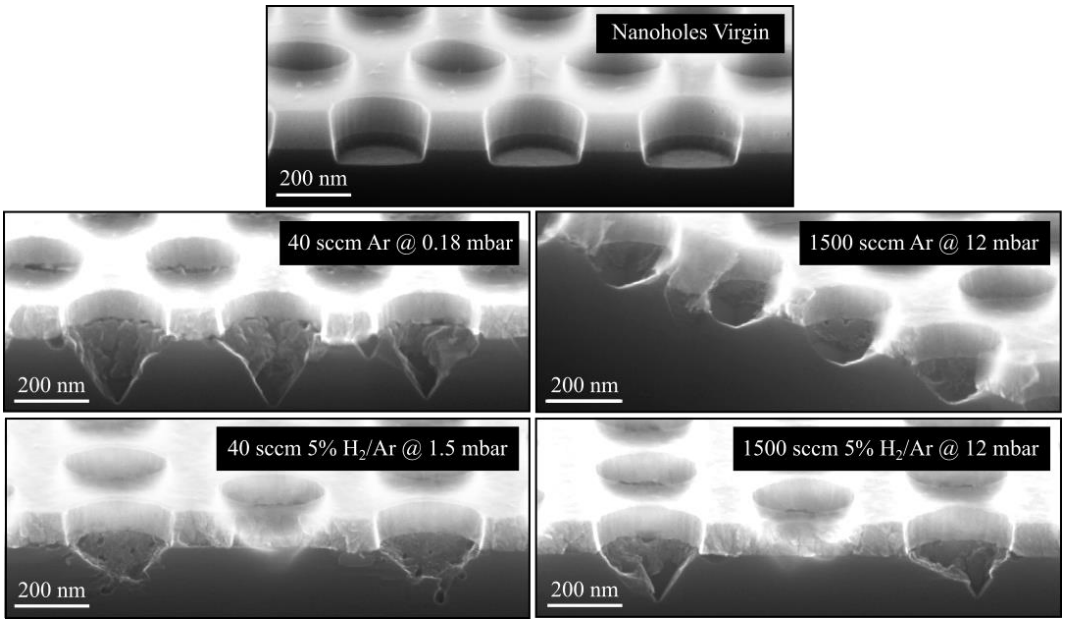

Figure 9 – Comparison of the effect of different pressure and ambient conditions on exposed Si, during RTA processing, for 60 s at 1100 ºC. Cross-section SEM images, 20º tilt, EHT 20 kV.

It is clear the Al_2O_3 mask suffers an alteration in its appearance - it is no longer amorphous but polycrystalline – however, it does not lose function as a masking material. It is also observable that a percentage of the existing silicon in the virgin samples is lost, using only Ar as process gas, both for high and low pressure/flow. Although less severe, the same applies to the experiments using the mixture of hydrogen and argon. Overall, the exposed Si surface is under attack and appears to be etched, which confirms the 'burning' phenomenon. Similar

thermal-induced defects with an inverted-pyramid shape were also found in other studies [27], [28], [35], promoted by the reaction between silicon and oxygen. However, when using the mixture of both gases, the etching seems less profound, indicating that the Si atoms may be protected as the surface is hydrogen-terminated, preventing its reaction with the existing oxygen inside the chamber.

In another set of experiments, as shown in Figure 10, a higher temperature was used for a shorter period. After 20 s at 1200 ºC, the surface also suffers alterations for both Ar and 5% H_2/Ar mixture ambients. Using only Ar, it seems the attack is more severe and that, besides the 'burning', the atom migration also occurs, as the surface appears rounded and smoothen, similarly to what was seen before. On the contrary, when using the gas mixture, the result is very similar to that obtained with the same conditions but using more time and lower temperature (60 s at 1100 ºC) in Figure 9. In these two cases, there is no indication that atom migration is taking place, as the surface is not smooth, on the contrary. However, the etching appears more intense for a higher temperature, even for a shorter period.

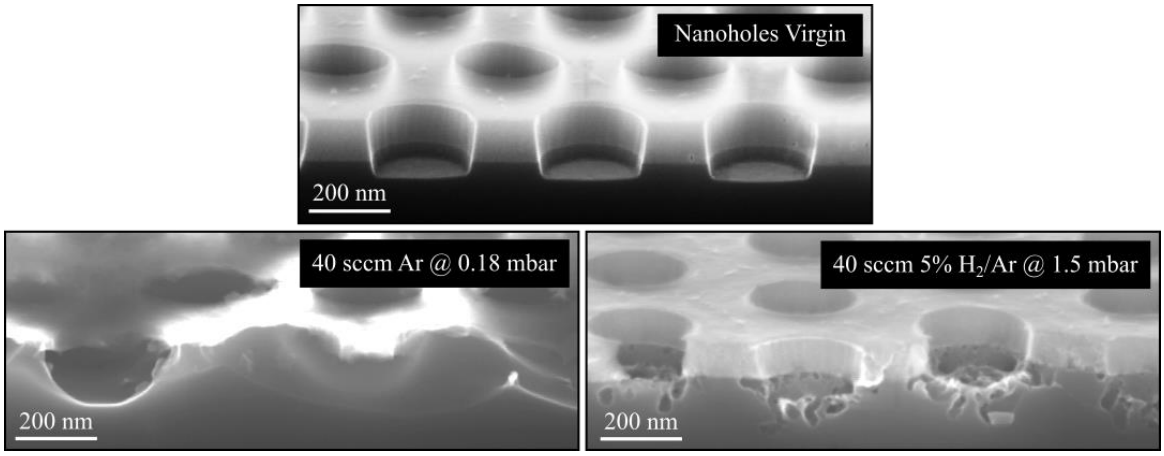

Figure 10 - Comparison of the effect of different ambient conditions on exposed Si, during RTA processing, for 20 s at 1200 ºC. Cross-section SEM images, 20º tilt, EHT 20 kV on the bottom-left image and EHT 5 kV on the bottom-right image.

A less severe attack is also achieved by performing a 30s-HF dip prior to the RTA process, as shown in Figure 11; due to the hydrogen-termination on the sample's surface, that area is protected and the reaction with oxygen is prevented. However, the Al_2O_3 is etched during the HF dip, even when performed for only a few seconds, which might have facilitated the Si etch underneath the mask, raising another issue. Lastly, using only 1000 ºC appears to have minimized the severity of the etching, even for a 3-minute RTA process, in combination with the prior HF dip.

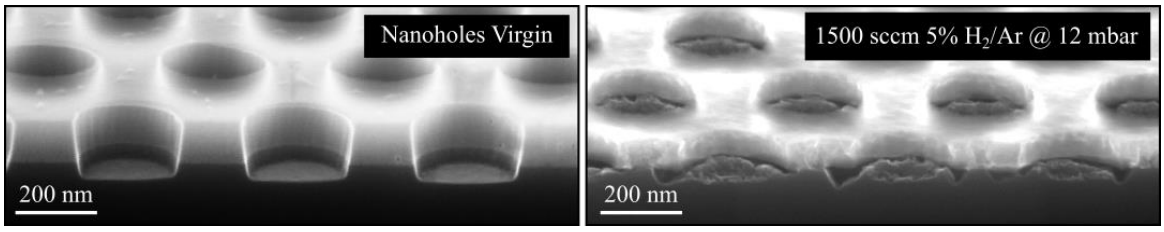

Figure 11 - Effect of HF dip on exposed Si before RTA processing (3 min at 1000 ºC). Cross-section SEM images, 20º tilt, EHT 20 kV.

Although many other experiments were carried out simultaneously with this study, in which Si_3N_4 wafers were used as carriers for the small chips, the quartz window remained clean and transparent. This indicates that

silicon sublimation and consequent deposition were present when using Si wafers - the primary source of deposited silicon. Hence, it is safe to conclude that Si sublimation is also occurring from the samples, but in a smaller proportion, having a less meaningful impact on the quartz window. Since sublimation is confirmed, it is possible to explain why using high pressures (Figure 9) prevents Si volume loss – at high temperature and high pressure, the silicon vapour pressure is decreased; there is a more significant amount of molecules inside the chamber, preventing silicon in the gas state to escape and travel across the chamber, reaching the quartz window.

Assuming that both phenomena are co-occurring in the same sample, the surface roughness and Si volume loss found on the samples in Figure 8 (a, b, c and f) can be explained by two mechanisms: 1) a percentage of the Si vapours that escape from the sample are forced to redeposit by the gas molecules inside the chamber and return to the solid state, attaching to the surface until they are sublimated again. This would lead to both volume loss and the appearance of small particles attached to the surface, as visible in, for instance, Figure 8(c); 2) the Si etching with consequent formation of SiO - 'burning' – leads to volume loss. Additionally, it leads to a second reaction referred to as reoxidation; in other words, gaseous phase SiO, released by chemical desorption, reacts with the remaining O_2 inside the chamber and forms SiO_2 in the solid state [27], [28], [36]. Hence, the small white particles visible in Figure 8(c) could also be SiO_2 deposited and attached to the Si. Furthermore, as the oxygen keeps reacting with the Si surface during the processing, the oxygen partial pressure decreases with time while the temperature remains high. As already mentioned, these are the ideal conditions for which 'burning' is enhanced. Thus, the reaction between SiO and O_2 is promoted even more, perpetuating the cycle, similar to what Mohadjeri *et al*. [37] explain when using pure N_2 as process gas during RTP at 1100 ºC. If so, this can justify why the sample in Figure 8(c) shows more roughness (more attached white particles) when compared to shorter-time samples, like those in Figure 8(a) or (b).

Overall, it can be concluded the interaction between oxygen and silicon causes surface roughness and thermal-induced defects. In that sense, Kim *et al.* [9] proposed a cover method that prevents those defects – covering the sample with an identical-composition material. If the mean free path of oxygen is larger in magnitude than the gap between the sample and covering material, then the oxygen cannot reach the covered-area surface. The approach used on the samples shown in Figure 5, Figure 6 and Figure 8(d) is identical, causing the samples to have a smooth surface with minimal defects and deposited particles. A gas purifier would also possibly guarantee the absence of unwanted oxygen inside the chamber during the process, preventing these issues.

In general, it is safe to assume that both phenomena are occurring. However, a mixture of both gases as ambient in combination with higher pressures and gas flows were revealed as the preferable conditions to prevent the surface attack, without damaging the hard mask. That assumption was taken into consideration when advancing to the following study.

3.3 RTA: Argon and Hydrogen Study

Since unwanted Si surface modification is prevented using high pressure and gas flow, it was necessary to resort to another available process gas in the RTP tool – hydrogen. Therefore, this study aimed to reflect the effects of simultaneously using two process gases – H_2 and Ar - under high pressure and gas flow conditions.

Considering the results from the previous studies presented in this work, a new set of samples was required. The chosen batch consisted of samples patterned with 200-nm diameter and 400-nm pitch nanoholes, 3.5 µm

deep (AR of 17.5). Similarly, the samples had a 100 nm Al_2O_3 hard mask, capable of undergoing RTA processing and consequently protecting the Si from sublimation and interaction with oxygen (that may be present inside the chamber). In addition, the mask could suppress the surface migration on the sample's surface. The starting point for the experiments is presented in Figure 12.

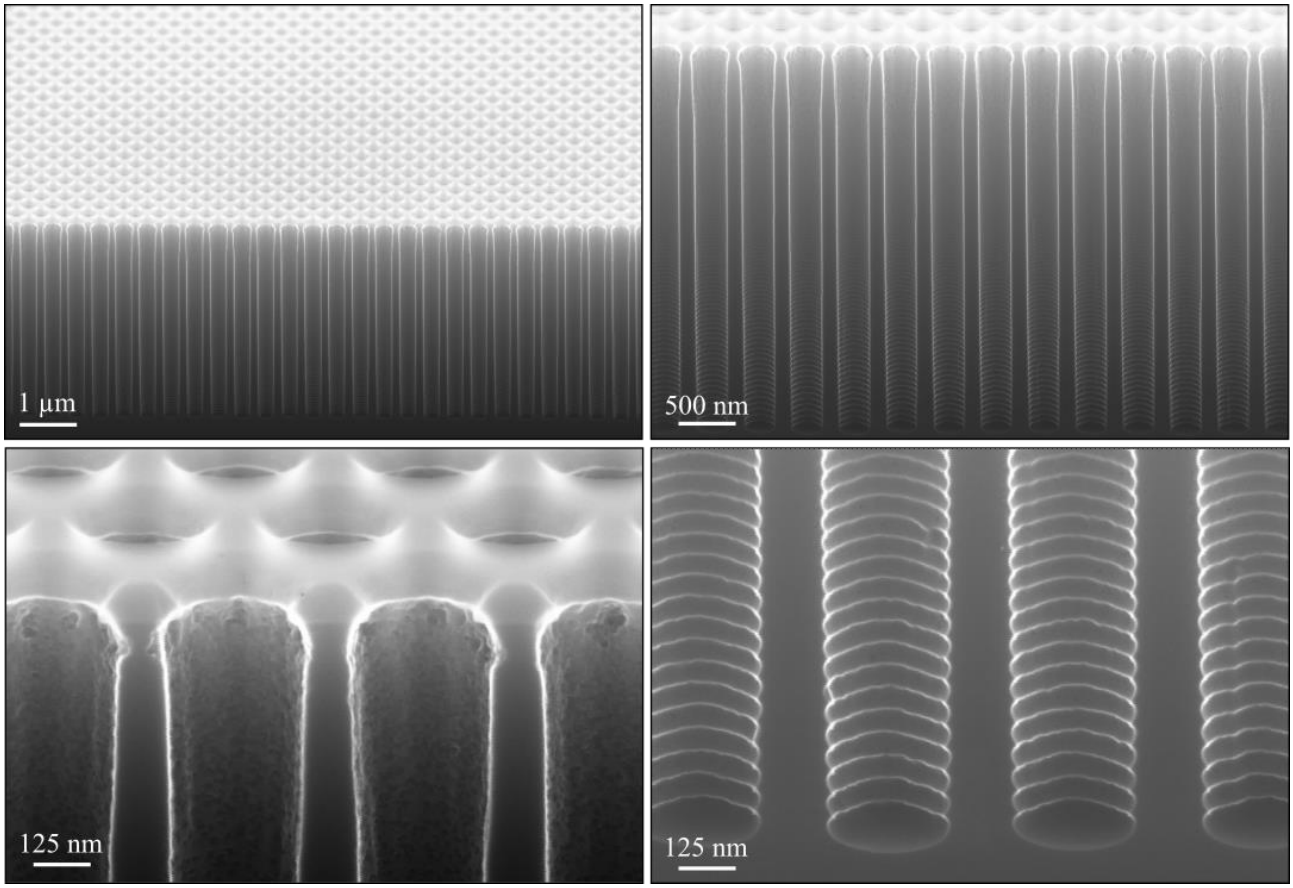

Figure 12 – Sample used as starting point in the 'Argon and Hydrogen study' from the nanoholes batch. The holes are 3.5 µm deep and have a 200 nm diameter and 400 nm pitch. Cross-section SEM images, 20º tilt, EHT 20 kV.

A previously used RTA recipe was tested for a better understanding of where to initiate the study and of the effect of RTA on this new type of sample. Although, a higher temperature and two different process durations were used. The results were compared and are shown in Figure 13.

As visible in Figure 13 (a)i and (a)ii, using only 20 s, two buried channels and a superficial layer of nanopores are formed. In theory, the latter corresponds to the nanoholes' top part. In addition, the hard mask is preserved. Looking under a different tilt (Figure 13 (a)iii) shows that the ESS channels in front are combined with other ESS behind them, forming an almost perfect plate-shaped ESS. However, a few rounded silicon columns are also visible, showing that the atom migration process was not completed and that the ESS is not continuous in any direction of the sample. On the other hand, increasing the time to 40 s resulted in two smooth horizontal buried plates. In this case, the third layer of nanopores is not present and the silicon surface is completely exposed to the chamber ambient.

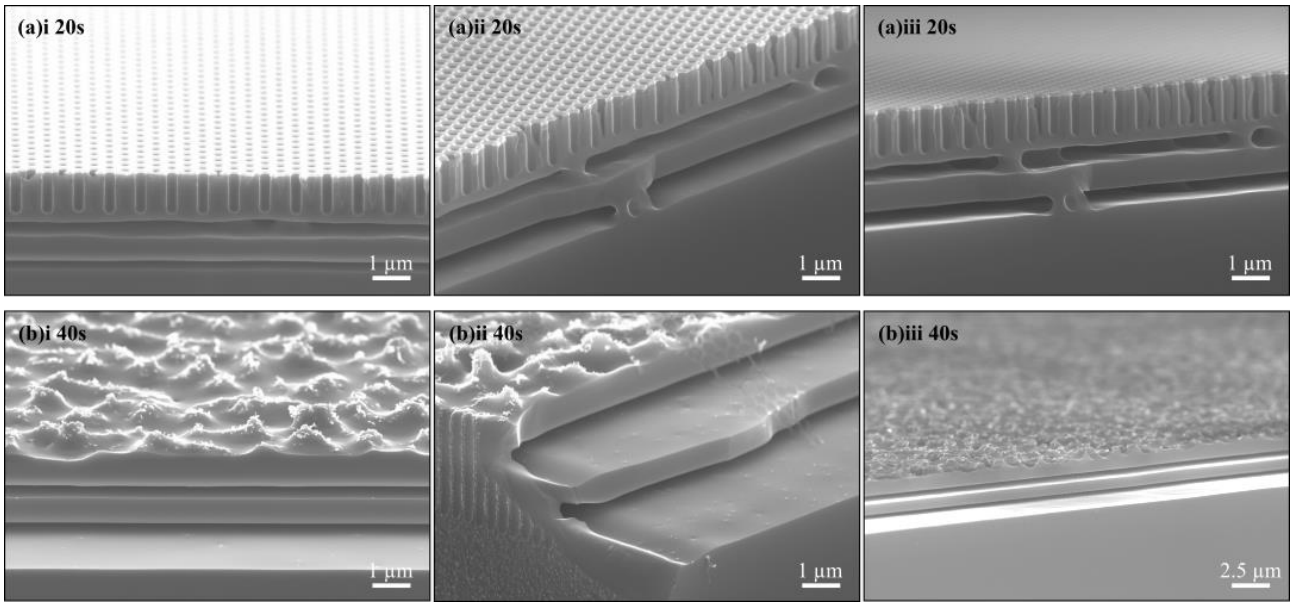

Figure 13 – Comparison of two consecutive experiments using different RTA times. Both were processed at 1250 ºC, 1500 SCCM Ar, and 12 mbar. (a)i, (a)ii and (a)iii correspond to the same sample, processed for 20 s, viewed from different angles. (b)i, (b)ii and (b)iii correspond to the same sample, processed for 40 s, viewed from different angles. Cross-section SEM images, 5º tilt on (a)iii and (b)iii and 20º tilt on the rest, EHT 5 kV on (a)i and (b)i and EHT 20 kV on the rest.

The absence of the mask can be explained by assuming that sublimation and burning are occurring – as the process follows, there is silicon volume loss, either by sublimating or being consumed due to the interaction with oxygen. If so, the interface between Si and mask is decomposed, the mask is detached and the silicon is left exposed. Closely observing Figure 13(b)ii makes it possible to identify a small residue from the hard mask lying on top of the sample. In addition, the sample's superficial roughness is similar to that found in the 'Argon Study' samples, which indicates the mask was lifted during the process, leaving the silicon exposed to react with the chamber ambient. Nonetheless, it can be concluded that a longer time is required to achieve continuous smooth pipe and plate-shaped ESS along the sample. Assuming the process is reproducible, the 40 s sample went through the same 3-layer phase as the 20 s one. Hence, in both experiments, the formation of buried features appears to have initiated at the bottom of the nanohole, as was reported by Sato *et al.* [11], [21] and Mizushima *et al.* [10] and explained in Chapter 1.3.

The gas flow and pressure were increased to preserve the hard mask and prevent the silicon's surface exposure, maintaining the temperature at 1250 ºC and the process duration at 20 s. The result is shown in Figure 14. Increased gas flow and pressure led to the evolution of the previously observed pipe-shaped ESS into smoother features that travel across the sample, almost without discontinuances. A third buried channel has also started to appear, as seen more closely in Figure 14(a) and (b). This one was formed entirely as approaching the right edge of the sample (end of the patterning), as seen in Figure 14(d). As the bottom channels are completely formed and the top one is still on the verge of formation, it is confirmed that the appearance of spherical ESSs starts at the bottom of the nanohole. These end up merging and forming the pipe-shaped ESS.

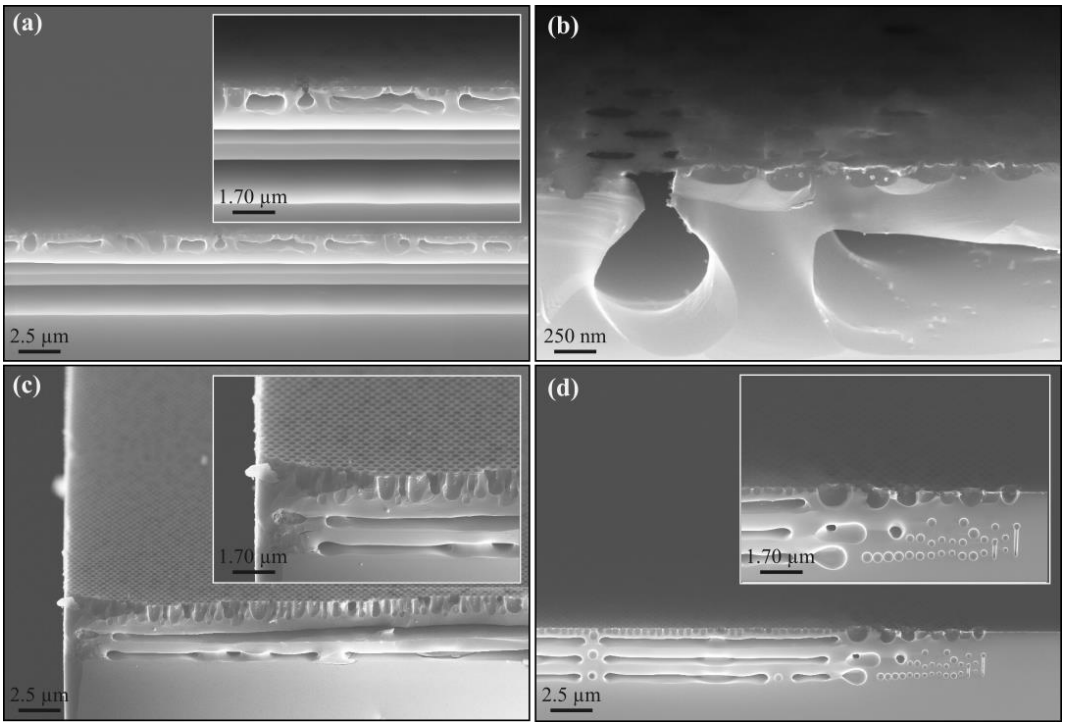

Figure 14 – Result no.1 from using a maximum pressure and gas flow RTA process for 20 s - 1250 ºC, 74 mbar, 2000 SCCM Ar, 2000 SCCM 5% H_2/Ar. (a) and (b) are pictures from the centre of the sample. (c) and (d) are images taken at the end of the pattern on both sides of the sample. Cross-section SEM images, 20º tilt, EHT 20 kV.

Furthermore, the experiment was repeated in a different sample to assess the process reproducibility, maintaining the same RTA conditions and duration. The results are shown in Figure 15.

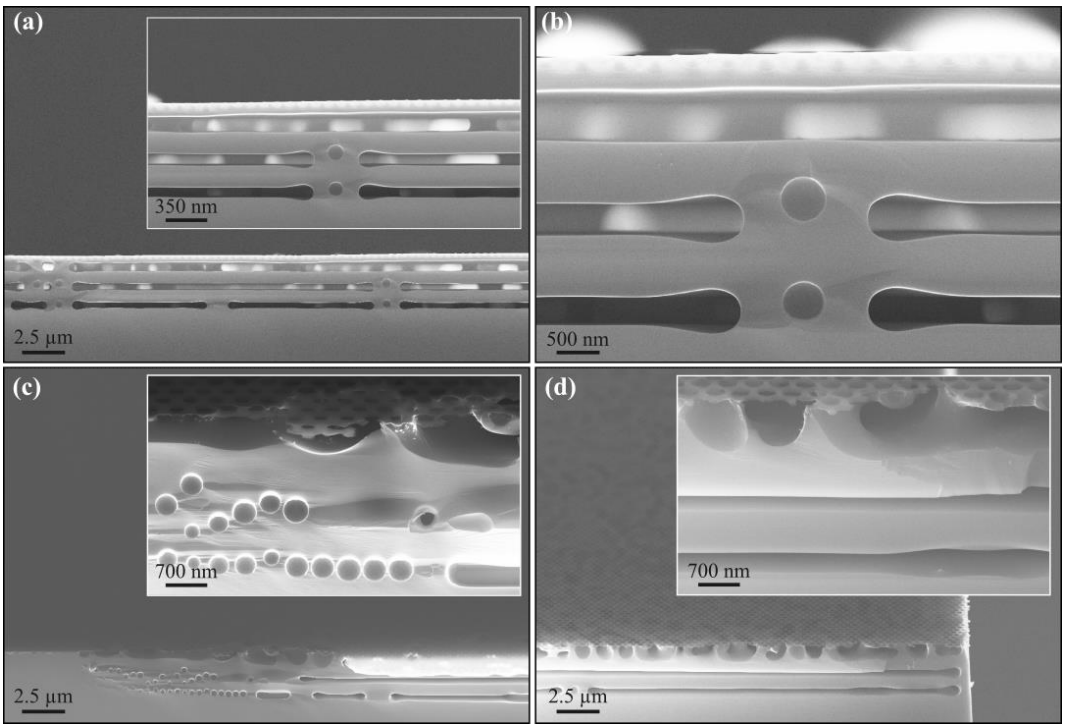

Figure 15 – Result no.2 from using a maximum pressure and gas flow RTA process for 20 s: 1250 ºC, 74 mbar, 2000 SCCM Ar, 2000 SCCM 5% H_2/Ar. (a) and (b) are pictures from the centre of the sample. (c) and (d) are pictures taken at the end of the pattern on both sides of the sample. Cross-section SEM images, EHT 20 kV, 0º tilt on (a) and (b), 20º tilt on (c) and (e).

As visible in Figure 15(a) and (b), there are already three completely formed buried channels, while on the edges, (c) and (d), there are only two formed and a third one is starting to appear. Thus, the results are not coherent with the ones from Figure 14. Nonetheless, both samples share some similarities: 1) the mask was preserved; 2) the buried channels are not continuous across the sample, in any direction, as visible under the 0º tilt (Figure 15 (b)). It seems that each row of the array of nanoholes has its own buried channels that are not aligned with the ones in front or on the back; 3) the silicon seems to gain a circular shape at the edge of a buried channel since it is a product of the merging of round, faceted holes or voids; 4) faceted voids were found, mainly at the edge of the sample, – as shown in Figure 14(d) and Figure 15(c) – indicating there wasn't enough time for them to merge into forming a channel before reaching their most stable shape. Some voids were also found in the middle of the samples, as Figure 15(b) shows; 5) Identical nanoholes originate different features depending on their positioning on the sample, indicating the heating is not uniform across the samples.

Consequently, two different experiments were necessary to clarify if the position of the sample in the carrier wafer would influence the results and, ultimately, the inter and intra-process capability of achieving similar results in consecutive processes. With that purpose, two identical nanoholes-array chips were manually cleaved and broken in half, parallel to the <110> plane direction, and were annealed under similar RTA conditions. Both halves of the first chip were processed together, and then the remaining two halves. The results are shown and compared in Figure 16.

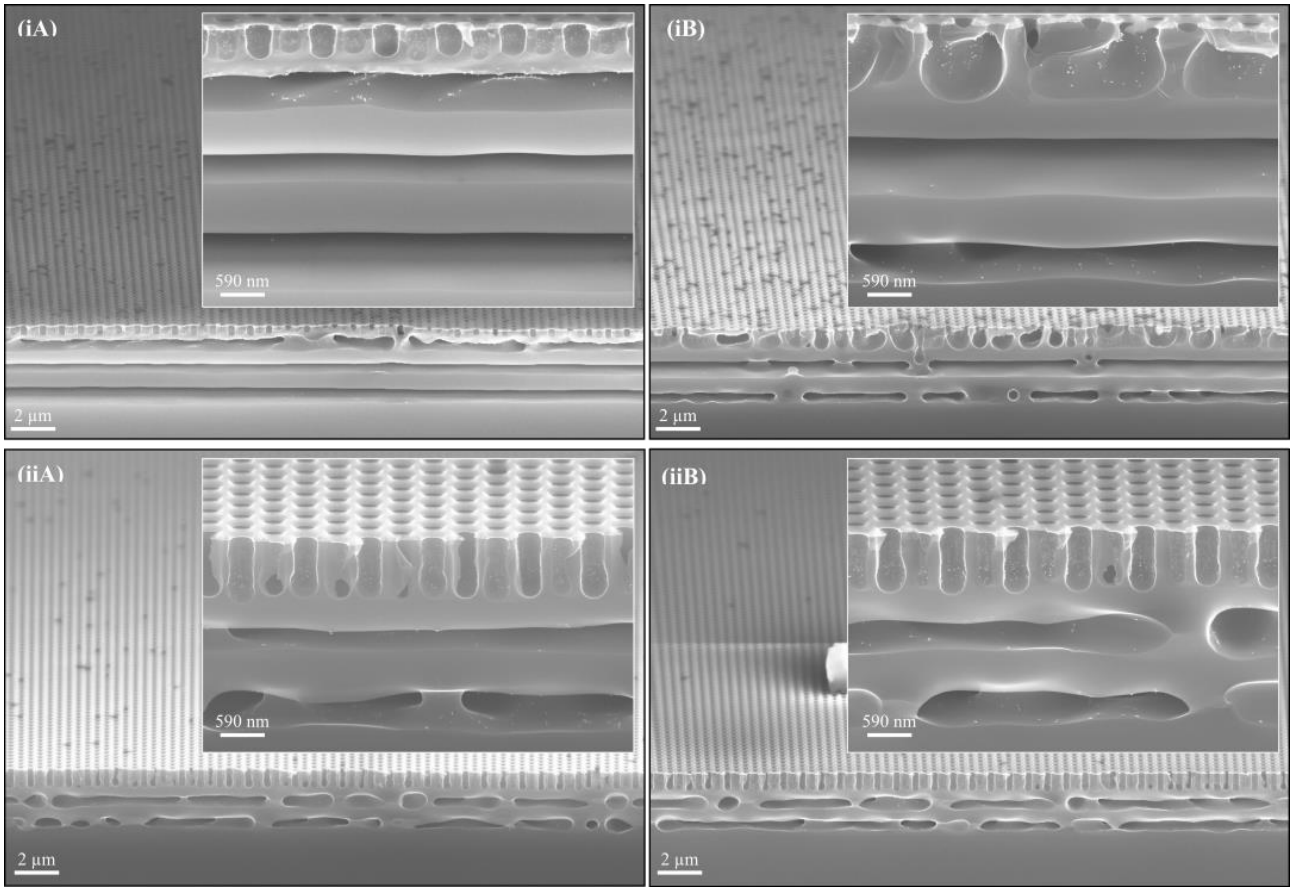

Figure 16 – Results of RTA processing using 2 pairs of half-samples, each pair processed together, placed next to each other on top of the Si_3N_4 coated carrier wafer. (iA) and (iB) are halves of the same chip, as well as (iiA) and (iiB). The process parameters were 30 s, 1200 ºC, 74 mbar, 2000 SCCM Ar and 2000 SCCM 5% H_2/Ar. Cross-section SEM images, 20º tilt, EHT 20 kV.

By observation, it is possible to affirm the positioning of the sample on the carrier wafer influences the final result – while the (iA)-half presents almost three completely formed buried channels, the (iB)-half does not even have one entirely formed. However, comparing the other two halves, (iiA) and (iiB), they show similar behaviours between each other. The evidence allows us to conclude the tool cannot reproduce results between processes nor during the same process for different positionings on the carrier.

Besides sublimation and burning - phenomena that have been established are occurring during the annealing sequences - another issue was raised when using high flows of the 5% H_2/Ar mixture. The tool is obliged to perform a post-cleaning process by flushing N_2 into the chamber, whereas the atmospheric pressure is reached in just a few seconds. Thus, there is a possibility that this rapid change in pressure and gas flow is causing one of the quartz pins supporting the carrier wafer to be expelled from its place, as it is just docked in another quartz piece. Hence, the unbalanced carrier wafer leads the samples resting on top to slide and sometimes even fall off into the chamber. During this study, it was noticed that several samples, after being out of the chamber (in the loadlock), either were rotated, rotated in a different position or were not there. In case of falling, the samples were later found and retrieved from inside the chamber, along with the expelled pin. As a result, opening the chamber several times caused its pre-conditioning to be changed over time, which might have led to a deterioration of process reproducibility. Similar process disturbance may also be the case when the samples would just slide or rotate, even without falling. In an attempt to fix this recurring issue, a soft-start valve was installed to prevent the pressure-rising from being so abrupt and minimize the number of samples lost inside the chamber. Ultimately, the number of times the chamber had to be disturbed would also decrease.

On the other hand, the DRIE tool had to be serviced and suffered extensive chamber sidewall cleaning, resulting in different process conditioning. In other words, according to the new chamber status, the etch recipes had to be re-optimized, enabling the production of similar but not identical nanoholes samples. Therefore, a new batch of nanoholes samples was produced and is shown in Figure S9. Compared with the other set of samples used in this study, they only differ in depth and etching profile – these are 4 µm deep and present a slightly positive profile. Nonetheless, a less straight profile is interesting to test the already working RTA recipes. Accordingly, this new set of samples was annealed using the 1250 ºC RTA process, with maximum gas flow and high pressure, for different periods.

As revealed by Figure 17, a visual temporal evolution of the buried features formation process was attempted. In each experiment, three layers of buried structures were achieved. After only 4 seconds, one buried channel is created, one interrupted channel is under formation in the middle and a combination of faceted voids and holes composes the bottom layer. With additional 4 seconds, the top and middle layers appear identical. Nevertheless, the third layer no longer contains faceted voids, only faceted holes that seem closer together. After 4 more seconds, the top channel remains identical, the central channel is completely formed and the bottom layer is now almost a channel due to the coalescence of the previously developed faceted holes. However, looking into the bottom one, it is possible to identify the silicon planes, which means the channel has no connection with possible adjacent channels. Finally, after a 16s-process, three buried channels are formed, while the bottom one is still discontinuous. Nonetheless, the top part is preserved as well as the mask, for all process times. An interesting remark, though, is that the buried features formation mechanism appears to have started from top to bottom, alternatively to what happened until this set of experiments and presented in the literature. This may be justified by the positive profile that characterizes this alternative batch of nanoholes. Even if the bottom holes are the first ones to form, they are farther apart than those created at the top. Given a short process time, only the closest ones coalesce, that is, the top ones.

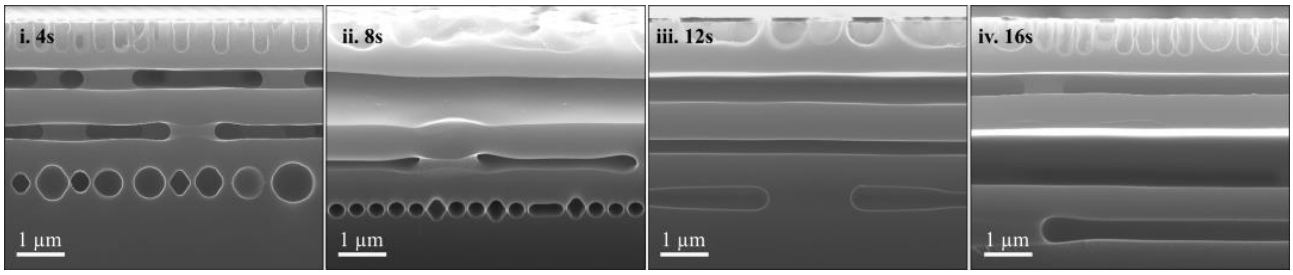

Figure 17 – Comparison between different consecutive experiments using different RTA processing times. Samples were processed at 1250 ºC, 74 mbar, 2000 SCCM Ar and 2000 SCCM 5% H_2/Ar. Cross-section SEM images, 0º tilt on (i), (iii) and (iv), 20º tilt on (ii), EHT 20 kV.

Since the machine suffered some alterations, the reproducibility of the tool was investigated by comparing three consecutive experiments using the same RTA sequence. The process took 20 s for all three and the results are shown in Figure 18. Even though they share some similarities, the samples behaved differently when facing identical process conditions. The soft-start valve installation helped minimize the number of times the quartz pins were expelled from their position, leaving the samples to slide and eventually fall inside the chamber mid-process. Nonetheless, this issue was not entirely eliminated, as the tool had to be opened a few more times to retrieve samples, which can be the primary cause of non-reproducibility. In addition, and as a result, the amount of oxygen inside the chamber constantly fluctuates, which is problematic from the process point of view: there is less control over the mixture of gases inside the chamber during the process. In general, even if programmed, it cannot be guaranteed that inside there are only 2000 SCCM of Ar, 2000 SCCM of 5% H_2/Ar and no oxidizing vapours. These aspects contribute to varying Si sublimation/burning rates from experiment to experiment.

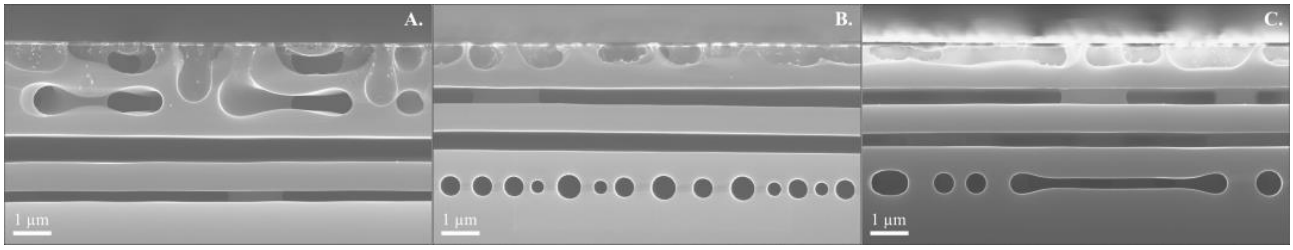

Figure 18 – Comparison between three consecutive experiments undergoing an identical 20s-RTA process. Samples were processed at 1250 ºC, 74 mbar, 2000 SCCM Ar and 2000 SCCM 5% H_2/Ar. Cross-section SEM images, 0º tilt, EHT 20 kV.

For the last set of experiments, a different perspective was studied – the effect of using different temperatures during the RTA process. As shown in Figure 19i), when the process temperature drops to 1100 ºC, the result after RTA is very similar to the samples' initial state. However, by closer observation, it is possible to see the bottom part is being re-shaped, starting to appear what in the future would be a faceted void; in this case, it is not yet separate from the main inlet. Furthermore, different stadiums of the rounding and reshaping mechanism are also visible, which means it is neither a uniform nor simultaneous phenomenon across the sample. Equally important, within the same etched nanohole, some areas still exhibit scallops - typical for the CORE process - and other regions don't. As such, the scallop removal does not seem to be a uniform process, which may indicate it is not achieved by smoothing through the atom migration mechanism. On the contrary, it looks like some parts of the surface are being sublimated and etched – Si etch with SiO formation, leaving a pure Si surface behind, hence the different colouration. On the inlet's bottom, though, the atom migration mechanism can be responsible for the scallop removal by smoothing it, combined with the other two phenomena. On the other hand, it is also interesting to see that using 1200 ºC as the temperature process (Figure 19ii) produces

such a different result when compared to the ones gotten with 1250 ºC – a 50 ºC drop, keeping every other parameter at the same value, was enough to get three discontinued layers of several different buried features instead.

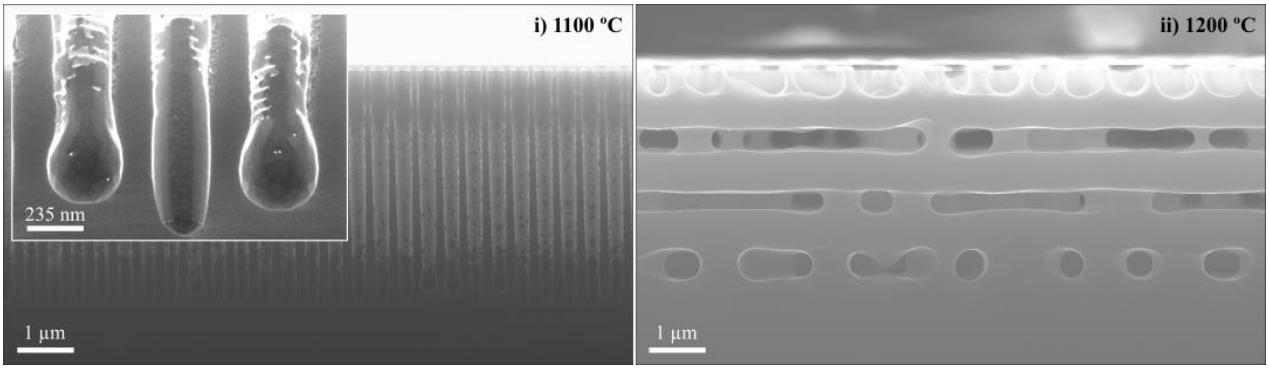

Figure 19 – Comparison between two consecutive experiments using different RTA temperatures. Both were processed for 20 s, at 74 mbar, 2000 SCCM Ar and 2000 SCCM 5% H_2/Ar. Cross-section SEM images, 0º tilt, EHT 20 kV. In the magnified picture, in the top-left, there's a 20º tilt.

In sum, the results have confirmed the non-reproducibility of the RTA process, even though they were carried out under sublimation and etching minimizing conditions and the soft-start valve was installed. Nonetheless, this study has proved that the formation of ESS is not exclusively correlated with H_2-ambient RTA processing. On the contrary, different shaped ESS were obtained using a mixture of both Ar and H_2, with only 5% H_2, using distinct process conditions. Therefore, the following chapter further explored other process windows to expand the tool's capabilities to other applications.

3.4 Clean BSi Study

The present study was pursued as the tool was considered an available approach to eliminate BSi from carrier wafers, already used in the DRIE tool a substantial number of times. Furthermore, the goal was to recycle them as an alternative to using new ones. Figure 20 shows the visual effect of this 'cleaning' process. As a result, more experiments were carried out to understand how to induce BSi smoothing and the factors affecting it.

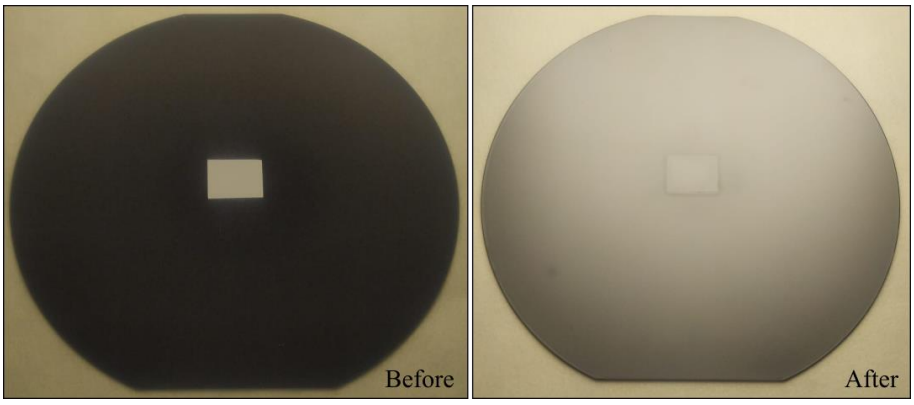

Figure 20 - BSi wafer before and after undergoing an 8s-RTA process showing the effect RTA has on BSi removal. Process parameters: 80 % of lamp power (≈ 1300 ºC), 0.18 mbar and 40 SCCM Ar. Digital camera images, 150 mm Si wafer, unpolished side up.

As visible in Figure 21, the surface of the Si wafer reveals that no BSi is present after the processing. However, compared to a non-processed surface, there was an increase in surface roughness, similar to what was observed

in the 'Argon study' and accordingly hypothesized. In addition, buried features were formed, such as faceted voids, typically induced by RTA processes, as seen. The vertical elements originated from the appearance of BSi during the CORE process, as it is achieved by etching: the etching process produces small inlets that, after the RTA process, have their top part closed and the bottom reshaped. The presence of scallops and an almost non-reshaped state may indicate the annealing time was too short for them to evolve into more stable forms. Regardless, it can be considered a friendly approach to removing BSi to reuse carrier wafers. However, it cannot be regarded as a good method to produce new Si wafers as an initial substrate, for instance, for micro-fabrication. As a result, more tests were required in an attempt to perfect the process.

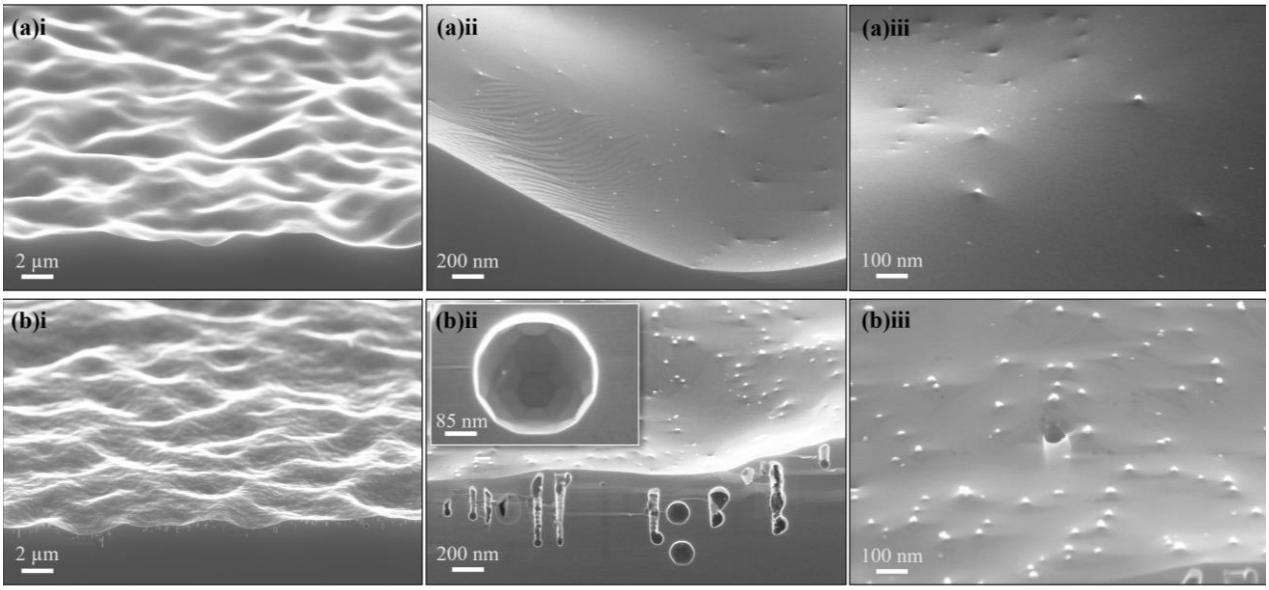

Figure 21 – Si wafer surface (a) without any processing (unpolished side) and (b) after BSi formation on the DRIE tool and subsequent removal through RTA processing - 80 % of lamp power (≈ 1300 ºC), 0.18 mbar and 40 SCCM Ar, 8 s. Cross-section SEM images, 20º tilt and EHT 20 kV.

The influence of the process temperature was investigated, using the BSi nanoholes as the starting point - referred to as 'Virgin' in the following SEM pictures (Figure 22). Varying only the temperature, even for a 1s-period, the effects are significant. Increasing the temperature, and keeping the pressure low, induces re-shaping and smoothing by the already proposed mechanisms in this work. However, the goal is to remove only the BSi and not reshape the nano inlets. The only sample without any reshaping is shown in Figure 22a), which indicates that there is a margin to study the effect time has on eliminating BSi, using 1000 ºC.

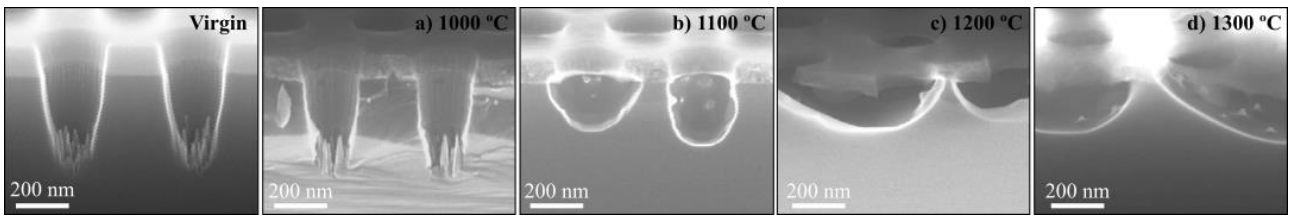

Figure 22 – Effect of temperature on the BSi removal process achieved by RTA. The process parameters were 0.18 mbar, 40 SCCM Ar, for 1 s. Cross-section SEM images, 20º tilt and EHT 20 kV.

Observing Figure 23, after only 8 s at 1000 ºC, there is no significant inlet re-shaping; however, some residual roughness is still visible. Hence, more process time was used. It's not until the 20s-process that the residual particles and roughness are minimized. On the other hand, the inlet is growing shorter and gaining a more

rounded shape, defeating the purpose of the study. In the same way, reshaping and roughening are enhanced as the time is increased even further, as shown in f) and g). Therefore, other approaches were followed, such as studying the influence of different pressure/flow combinations and process gases.

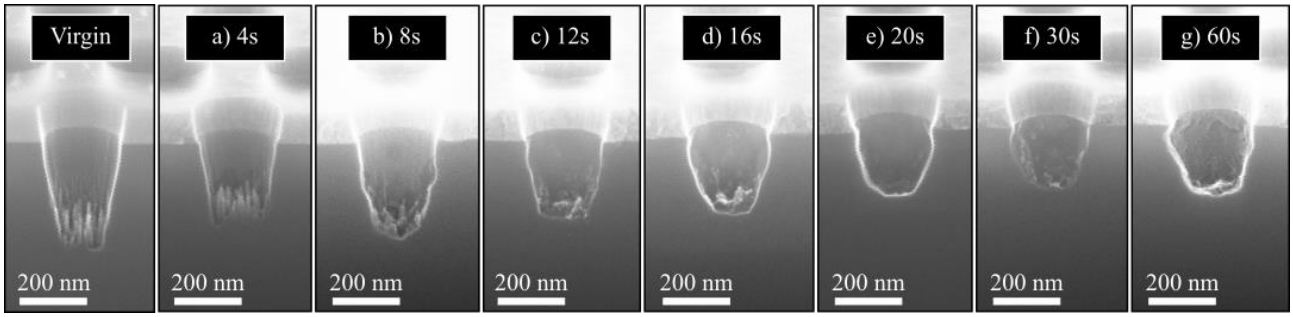

Figure 23 – Effect time has on the BSi removal process. The process parameters were 1000 ºC, 0.18 mbar and 40 SCCM Ar. Cross-section SEM images, 20º tilt and EHT 20 kV.

Comparing the low-temperature processed samples, a) and b) from Figure 24, one can assume that a high flow and pressure combination allows the annealing effect to slow its rate. Consequently, the reshaping of the inlets is retarded. The same applies to the high-temperature processed samples, Figure 24c) and d). As visible, the sample in Figure 24b) is very similar to the virgin sample, so almost no change was induced by the process in those conditions.

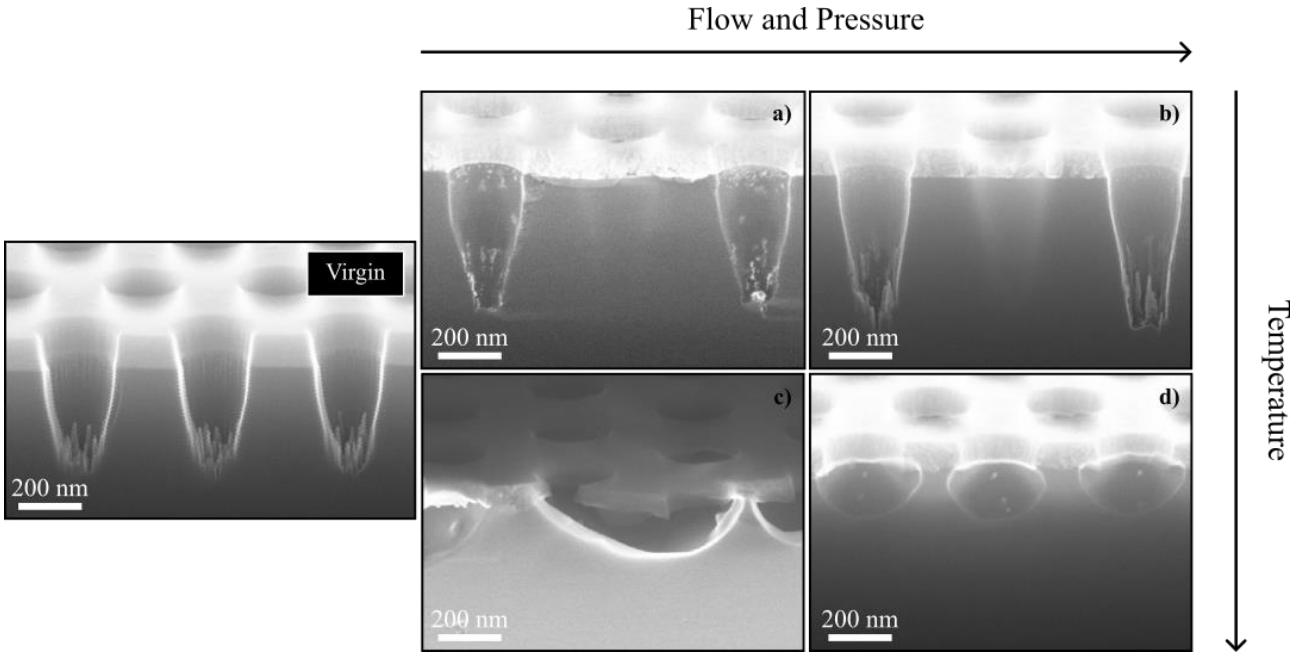

Figure 24 – Flow and Pressure vs Temperature Effect on the BSi removal process. a) 10 s, 0.18 mbar, 40 SCCM Ar, 1000 ºC; b) 10 s, 43 mbar, 2000 SCCM Ar, 1000 ºC; c) 1 s, 0.18 mbar, 40 SCCM Ar, 1200 ºC; d) 1 s, 43 mbar, 2000 SCCM Ar, 1200 ºC. Cross-section SEM images, 20º tilt and EHT 20 kV.

Regarding the process gas, Figure 25 shows that using the 5% H_2/Ar mixture prevents smoothing, identical to high-pressure/flow combinations. These two considerations are consistent with the previous studies and the proposed mechanisms that could explain smoothing and reshaping.

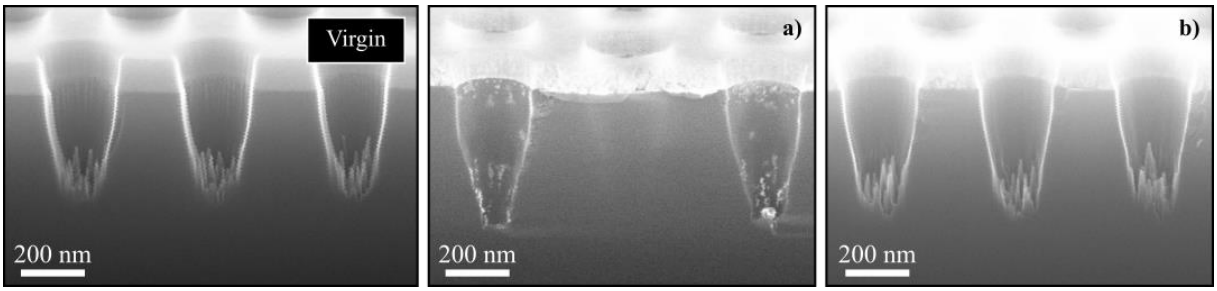

Figure 25 - Effect the process gas has on the BSi removal process. a) 10 s, 0.18 mbar, 40 SCCM Ar, 1000 ºC; b) 10 s, 1.5 mbar, 40 SCCM 5% H_2/Ar, 1000 ºC. Cross-section SEM images, 20º tilt and EHT 20 kV.

As a final remark, in the majority of the results from this study, white particles are present, identical to those attached to exposed silicon in the 'Argon study'. For instance, as shown in Figure 25 a). Two mechanisms that would possibly cause this occurrence were proposed and explained in Chapter 3.2. Nonetheless, this experimental work allowed for the formulation of a third one, considering the passivation step present in the CORE process, which was not taken into account before. BSi comprises a series of nanoneedles, and a thin SiO_2 layer passivates their surface. In some cases, the nanoneedles are so thin that they can be fully transformed into SiO_2. These needles change shape during the atom migration process, causing this superficial layer to burst, leaving SiO_2 residues inside the inlets. The same goes for the inlet's sidewalls, which were also passivated. This mechanism does not exclude the possibility of the other two occurring, on the contrary. Assuming Si sublimation/redeposition combination is one of the occurring phenomena, it might occur after the oxide layer's disruption. The reaction between Si and existing O_2 inside the chamber, leading to the formation of SiO vapours, might have a lower rate before the oxide layer disruption - the O_2 must diffuse through the oxide and reach the interface with the silicon - but it's not considered inexistent. In sum, all three mechanisms might coexist.

3.5 RTO: Oxidation Study

This chapter is dedicated to analyzing and discussing the results achieved using one of the other features of the rapid thermal processor tool – RTO. This study aimed to reflect the effects of rapid thermal oxidation on HAR Si features. Thereupon, it was necessary to establish a process window and ensure the process was reproducible within those parameters. Hence, the study was initiated by testing the reproducibility and stability of a programmed RTO recipe using Si wafers (prepared as described in Chapter 2.3). The recipe is translated as an oxidation process at 1200 ºC, 12 mbar and 1500 SCCM of O_2 flow.

The dataset for each RTO round was plotted together and can be found in Figure 26. For each round, each point represents an ellipsometry measurement, with corresponding error bars (based on the mean squared error (MSE) for each). It is essential to mention that the RTO sequence is programmed to include an initial 10s-interval to stabilize the temperature inside the chamber as well as pressure and gas flow. However, this interval is not included in the designated RTO process time; the RTO process is only considered to have begun after this period. There might be SiO_2 growth during the stabilization period as the temperature is already being increased. Hence, the initial thickness cannot be considered zero. To determine the initial oxide thickness before RTO processing, i.e., after the 10s-period, the RTO process time was fixed to 0 s.

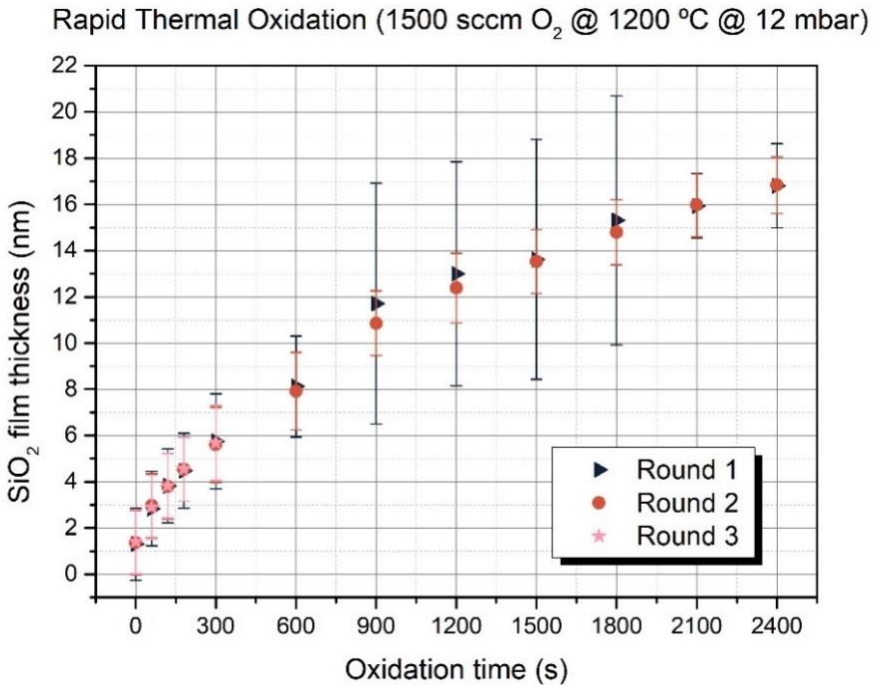

Figure 26 - Graphic representation of the correlation between SiO_2 thin film growth and oxidation time. The third-round dataset (pink stars) it's not completed as one of the quartz-window broke mid-process.

By plotting the data together and analyzing the results, it's safe to assume the RTO process, under these conditions, is relatively reproducible, as most of the points are coincidental. However, some discrepancies may be caused by different initial chamber conditioning – the quartz plate was not completely transparent during the first round, presenting some deposited silicon from previous processes using the same tool. Over time, the oxidation sequences caused an improvement in plate transparency and cleanliness. Additionally, due to some technical issues encountered during the studies described in this section, the tool had to be opened several times, disrupting the tool's reproducibility and stability. As a result, the different RTO experiments were carried out under different chamber conditioning, which may have impacted the results. Regarding the ellipsometry measurements, there could also be an error margin due to fluctuations in the temperature and humidity of the cleanroom air. These variations may significantly influence the measurements, whereas thin films are characterized.

Moreover, the characterization performed by ellipsometry allowed an analysis from a film uniformity perspective. This analysis was as necessary as the previous one since it can provide information about heat distribution across the whole wafer used during the RTO process. Figure 27 shows different colour maps for each RTO process time. The maps were achieved by using the average film thickness on nine distinct points of the wafers, considering the three rounds of experiments. The dark-lined circle represents the wafer area.

Interpreting the graphic representations, it's worthwhile noting that the thin film is thicker in the centre of the wafer and thinner as it approaches its edge, considering the area analyzed with the ellipsometer. The thickness increase towards the centre could be explained by the non-uniformity of the heat transfer from the lamps towards the wafer and slow heat distribution by conduction within the wafer. This is aggravated by the fact that the pyrometer sensor is aligned with the centre of the wafer. When the desired temperature is achieved, the pyrometer tells the system that, in that position, the wafer is already at the desired temperature. This causes an automatic decrease in lamp power to maintain the temperature at that constant value. However, the edges of

the sample might not have heated properly or not have the required time to heat thoroughly (for short oxidation times); if so, the system does not recognize it. For longer oxidation times, there is yet another concern – a higher oxidation rate at the centre (when compared to the edge) leads to a higher difference between the thicker and thinner positions of the sample than when short oxidation times are used. For instance, that difference is 0.960 nm for a 40-minute RTO process and only 0.230 nm for a 60-second RTO process.

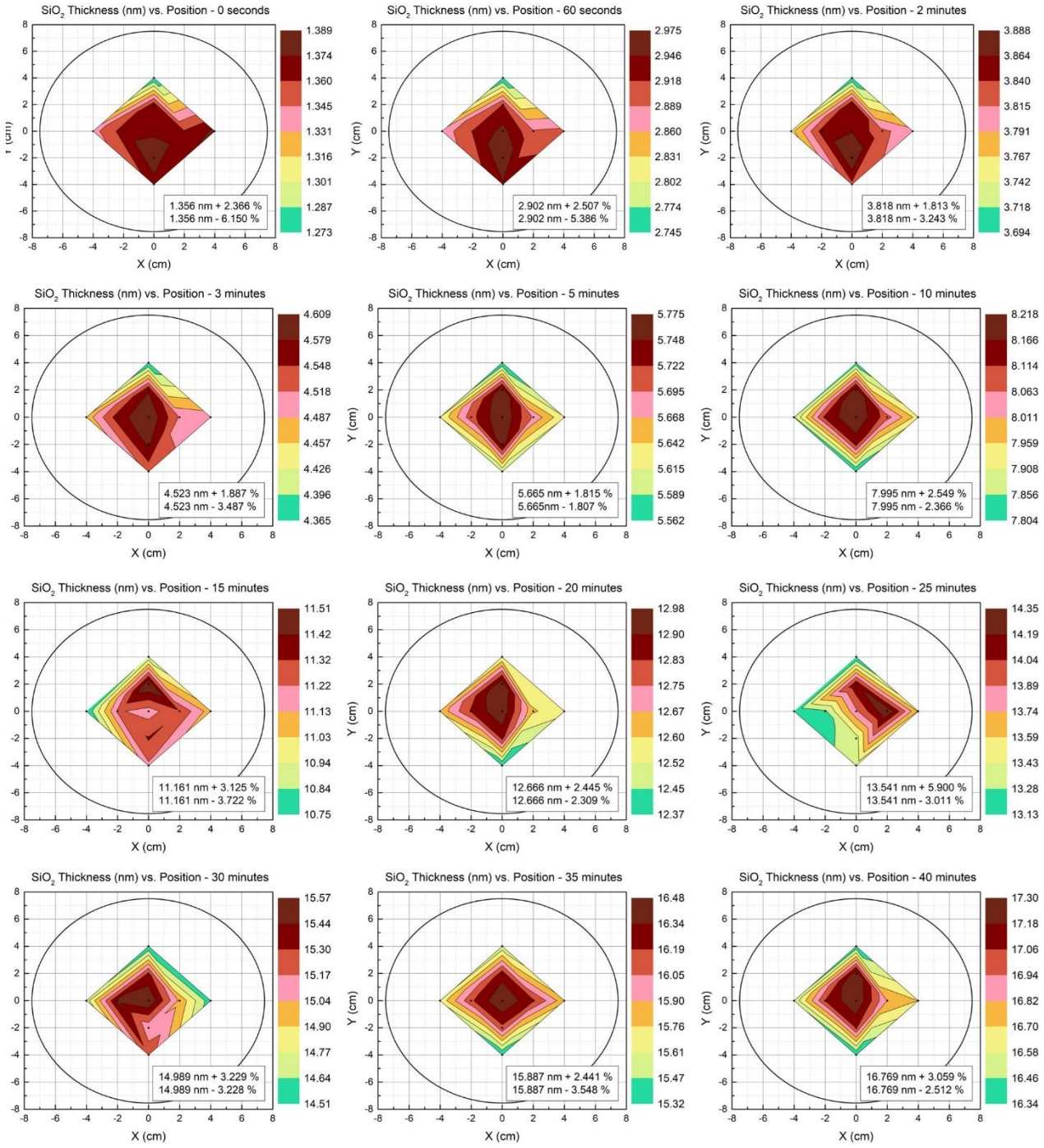

Figure 27 - Graphic representations of the grown SiO_2 thin film thickness vs position in the wafer for different RTO process times. It is also indicated the thickness variation (in percentage) when compared with the average oxide thickness across the wafer.

Lamp compensation might improve these issues, which means the different-positioned lamps could be programmed to provide more or less power, depending on their position concerning the wafer. In this case, a good

approach would be to progressively decrease the power from the edge-positioned lamps to the centre-positioned ones. Nevertheless, overall, it's possible to affirm that good thin film uniformity is achieved using the RTO process, considering the low thickness variations compared to the average thickness – translated into less than 0.8 nm.

Therefore, all the conditions were gathered to study the effects of the RTO process on the HAR Si features prepared in advance (as explained in Chapter 2.2.1) - the nanoholes samples. A 40min-RTO process was performed as it corresponds to a higher oxide thickness growth, being the easiest one to capture using the SEM tool. Observing Figure 28 and comparing both before and after RTO process pictures, it is safe to assume that a continuous SiO_2 thin film has grown along the sidewalls and bottom of the etched features into the silicon. The grown oxide corresponds to the brighter-toned layer, which is not visible in the pictures on the left.

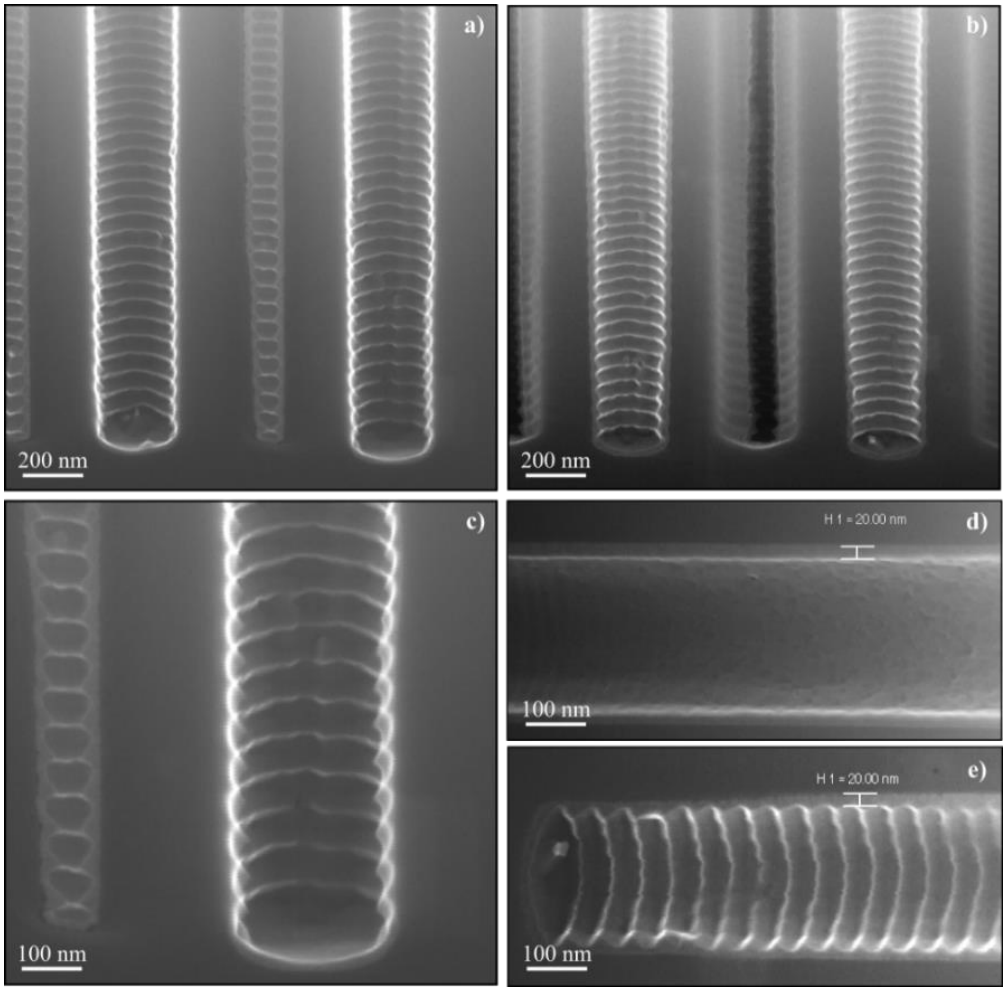

Figure 28 – Nanoholes sample a), c) before and b), d), e) after a 40min-RTO process (1200 ºC, 12 mbar and 1500 SCCM O_2). Pictures d) and e) were rotated during the characterization due to some existing vibrations preventing a good resolution in the vertical position. The thermal oxide thickness was measured in two places (d)top and e)bottom) of the inlet using the SEM tool. Cross-section SEM images, 20º tilt and EHT 20 kV.

Using the potentialities of the SEM tool, it was possible to measure 20 nm as the layer's thickness; this value is not so far from the 16.769 nm achieved before on a wafer after undergoing the same 40-minute RTO sequence. Afterwards, the thermal oxide thickness at the bottom of the feature was also measured, and the result was 15.730 nm. The difference between the sidewall oxide thickness and the bottom/wafer oxide thickness may be related to the dependency between oxidation rate and the silicon surface orientation. In other words, it

depends on the amount of Si atoms available on the surface being oxidated to react with the oxygen. According to the literature [17], [37]–[42], Si (110) has more available atoms per unit area on its surface when compared to Si (100). Hence, a faster oxidation rate is achieved on Si (110) in the linear rate regime of the well-established Deal-Grove model [43], valid for conventional thermal oxidation. The model is not suitable for predicting the rapid initial oxide growth behaviour (thin-oxide growth) [37], [39], [41], [43] present in short-RTO processes. Nevertheless, based on the results, it is still possible to assume that different silicon crystallographic orientations influence the oxidation rate in this case. Consequently, the Si (110) sidewalls are oxidated faster than the Si (100) at the bottom of the features and the wafer surface. As such, thicker layers are obtained for the first situation, as visible in the SEM images and previous discussion.

In sum, it was established that the RTO process is reproducible within the parameters chosen as the ideal process window (1200 ºC, 12 mbar and 1500 SCCM O_2). It was also determined that the obtained SiO_2 thin films are sufficiently uniform in both cases: as passivation for the HAR feature sidewalls and for the Si (100) wafer surface.

4 CONCLUSIONS AND FUTURE PERSPECTIVES

This work aimed to investigate the capabilities of a research RTP tool and how it can be used as a versatile and multifunctional microfabrication tool. In addition, there was little to no prior knowledge of the instrument. Therefore, providing results has significantly sped up the tool's learning process. In contrast to conventional furnaces, a rapid thermal processor can quickly reach high temperatures in a variety of processing environments. In order to create optimized microfabrication process flows, conventional techniques and approaches can be reinvented thanks to the unique properties of RTP. As a result, research has been done into how HAR Si features are affected by RTP.

Exploring the capabilities of the RTP tool was the first step that ultimately led to five different studies, already extensively described - the 'Argon study', the 'Sublimation & Burning study', the 'Argon and Hydrogen study', the 'Clean BSi study' and the 'Oxidation study'. In short, these focused on five main topics: RTA processing using only Ar as process gas, a comparison between using Ar and an Ar/H_2 mixture, the physical mechanisms associated with RTA, the smoothing process of BSi by RTA and the capabilities of RTO processing.

The 'Argon study' allowed to conclude the atom migration phenomenon can be induced using only Ar as the process gas for RTA. Moreover, three types of structures were obtained due to the Si self-diffusion mechanism through the surface of trench-patterned samples: faceted droplets, buried faceted holes and enclosed faceted voids. The faceted droplets carved into the Si are a product of the deep and narrow trenches' complete 3D profile transformation. The other two types were achieved by reshaping the Si into its equilibrium and most stable form, inducing ESS formation. Same-length facets were found in the droplets, holes and voids and belong to the {100}, {113}, {111} and {110} families of Si crystal planes. Furthermore, it was also possible to conclude that Cr is unsuitable as a masking material for this type of high-temperature processing, as it crumbles and detaches from the silicon surface. The Al_2O_3 hard mask emerges as an alternative masking material, proven to be capable of sustaining RTP and suppressing the surface migration at the sample's surface.

Equally important, the result's lack of reproducibility combined with the discovery of deposited Si on the tool's top quartz-window was evidence enough to suspect other physical mechanisms were associated with RTA processing. The 'Sublimation & Burning study' confirmed, as the name implies, that both phenomena occur for high and low temperatures as well as for high and low pressures/gas flows. Nonetheless, using the 5% H_2/Ar mixture as a process environment and higher pressures combined with higher gas flows appear to prevent surface attack without damaging the Al_2O_3 hard mask.

Regarding the 'Argon and Hydrogen study', this study explored various RTA process conditions, using the 5% H_2/Ar mixture as the process gas environment and nanohole-patterned samples. As a result, it was proved that the formation of ESS is not exclusively correlated with H_2-ambient RTA processing. On the contrary, different shaped ESS were obtained using a mixture of both Ar and H_2, with only 5% H_2, using distinct process conditions. Additionally, the study allowed a better comprehension of the early stages of the buried channel/cavity formation, indicating that the appearance of spherical ESSs starts at the bottom of the inlets. These coalesce and form pipe or plate-shaped ESSs. The same follows, subsequently, from the bottom to the top of the inlet. The spherical ESS formation mechanism is similar when the inlet's etch profile is slightly positive tapered. However, the merging process is initiated at the inlet's top and middle parts, as the bottom ESS are not as closely-spaced.

Taking advantage of the smoothing caused by atom migration during RTA processes, the 'Clean BSi study' aimed to prove that BSi removal could be achieved using the same tool. Accordingly, the elimination of BSi, previously grown using the CORE process in Si wafers and at the bottom of nanoinlets, was successfully achieved. The effect of temperature, time, pressure/flow combination and process gas were investigated as improving factors for the RTA process involved. However, neither of the used combinations of parameters was ideal for removing the BSi while preserving the nanoinlet shape and enhancing the surface smoothness. As such, further work is required to establish the ideal process window. Nevertheless, the results from this study were consistent with those from the other studies and sustained every former conclusion.

Overall, it was concluded that identical RTA processing does not always produce comparable results. One of the possible causes lies in the sublimation and burning phenomena combination. The second cause might be related to the constant retrieval of fallen samples inside the chamber, leading to multiple re-conditioning as the chamber is opened. For future work, it would be of interest to guarantee the process gases' purity and minimize the quantity of oxygen inside the chamber by adding a gas purifier. As such, the silicon surface attack by reaction with oxygen could be avoided. Equally important, finding the cause behind the falling-pins issue is necessary, as a soft-start valve installation proved insufficient in solving the problem.

As additional future perspectives, it would also be interesting to use these various RTA conditions and test them on smaller patterned arrays. As a result, during the sample breaking for cross-section observation, the probability of damaging the SON structures is minimized. Moreover, capturing the entire buried feature under SEM visualization would be helpful and could provide more information about the buried features as a whole. Furthermore, varying the pattern pitch value would be relevant to investigate the correlation between initial inter-inlet distance and the coalescing mechanism. Consequently, it would provide valuable information on how to control the ESS's final size, shape and depth. This pitch-related study could first be attempted using the nanoholes and trench-patterned Si samples, with Al_2O_3 as a hard mask. In addition, according to what was mentioned in Chapter 1.3, creating larger-dimensioned Si structures could be helpful to witness surface roughness removal and not profile transformation. For instance, this concept could be applied to study not only BSi but also etch-induced scallops removal without compromising the inlet's shape.

The main benefit of RTO over traditional thermal Si oxidation is the ability to produce thin films of excellent quality while keeping the processing time short. As such, its capabilities were investigated. As a result, RTO processing was regarded as a relatively stable and repeatable process in the 'Oxidation study'. For Si (100) surfaces and Si (110) surfaces, SiO_2 thin films could be grown with only minor uniformity issues, below 17 nm and 20 nm, respectively. Nonetheless, more experiments carried out under different conditions – such as temperature, pressure, oxygen flow and even shorter oxidation periods - would be helpful to study further the RTO process and consequently model the experimental data, using, for instance, the thin-oxide growth model proposed by Massoud *et al.* [3], [5]. Besides, this future approach could allow a better understanding of the rapid thin-oxide kinetics; its physical mechanism is still controversial, as the Deal-Grove model does not predict this behaviour during dry O_2 oxidation [38], [39]. The uniformity issues could be addressed using lamp compensation.

In brief, different approaches were taken to study the behaviour of HAR structures when exposed to varying conditions inside a rapid thermal processor. Consequently, the knowledge about the available tool was deepened, as well as the understanding of RTP processing. With further investigation, future work can evolve towards process optimization and fabrication of application-oriented structures, such as SON structures for MOS and MEMS devices.

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A SUPPLEMENTARY TABLES

Table S1 - Parameters for the single-run multi-step trenches stack etching.

		Time (s)	Pressure (mTorr)	O_2 (SCCM)	SF_6 (SCCM)	Platen Power (W)
BARC strike RIE		10	10	50	0	0→20*
BARC etch RIE		600	100%**	50	0	10
Dedam etch RIE		60	100%**	0	15	10
a-Si etch CORE process (4 cycles)	C	4	100%**	50	0	0
	O	2	50	50	0	10
	R	20	100%**	0	10	10
	E	20	30	0	15	10
Cr etch (15 cycles)	Deposition	9	37	50	0	40
	Etch	1	37	50	3	40
Resist strip		900	200	200	0	40
Si etch CORE process (122 cycles)	C	10	3%**	200	0	40
	O	10	100%**	0	5	40
	R	2	4%**	0	350	40
	E	0→15*	4%**	0	350	300

*This representation means the value for the correspondent parameter is ramped up, throughout the cycles.
** Percentage corresponds to valve position, whereas 100% corresponds to approximately 0 mTorr.

Table S2 – Process parameters of the consecutive steps used to etch the Al_2O_3 hard mask, DUV resist and BARC layer.

			Time (s)	Pressure (mTorr)	Ar (SCCM)	BCl_3 (SCCM)	Cl_2 (SCCM)	O_2 (SCCM)	Power (W)
III-V ICP etch tool	**Al_2O_3 etch** (255/260* min)	Dep.	1	≈ 0	1	100	-	-	0
		Etch	1	≈ 0	10	0	-	-	30
	DUV/BARC etch	Etch	30	5	-	-	30	-	30
DRIE tool	**O_2 clean**	Etch	2700	0.01	-	-	-	50	30

*The last two steps (DUV/BARC etch and O_2 Clean) were discarded when using 260 min for the Al_2O_3 etch.

Table S3 - ORE process parameters used to fabricate high aspect ratio nanoholes.

		Time (s)	Pressure (mTorr)	O_2 (SCCM)	SF_6 (SCCM)	Platen Power (W)
Si etch ORE process (122 cycles)	O	10	220	200	0	40
	R	10	≈ 0	0	40	40
	E_1	2	220	0	350	0
	E_2	0→15	220	0	350	100→300

Table S4 - CORE process parameters used to produce black silicon at the bottom of high aspect ratio nanoholes.

		Time (s)	Pressure (mTorr)	O_2 (SCCM)	SF_6 (SCCM)	Platen Power (W)
Si etch CORE process (100/200 cycles)	C	5	50	200	0	40
	O	7	≈ 0	0.1	40	20
	R	1	50	0	1200	0
	E	0→1	50	0	350	100→300

Table S5 - CORE process parameters used to produce black silicon on a Si <100> wafer.

		Time (s)	Pressure (mTorr)	O_2 (SCCM)	SF_6 (SCCM)	Platen Power (W)
Si etch CORE process (100 cycles)	C	5	50	200	0	40
	O	7	100%	0.1	40	20
	R	1	50	0	350*	0
	E	0→1	50	0	350	500→750**

* 1200 SCCM during 0.5 s.

** Coil/ICP power.

B SUPPLEMENTARY FIGURES

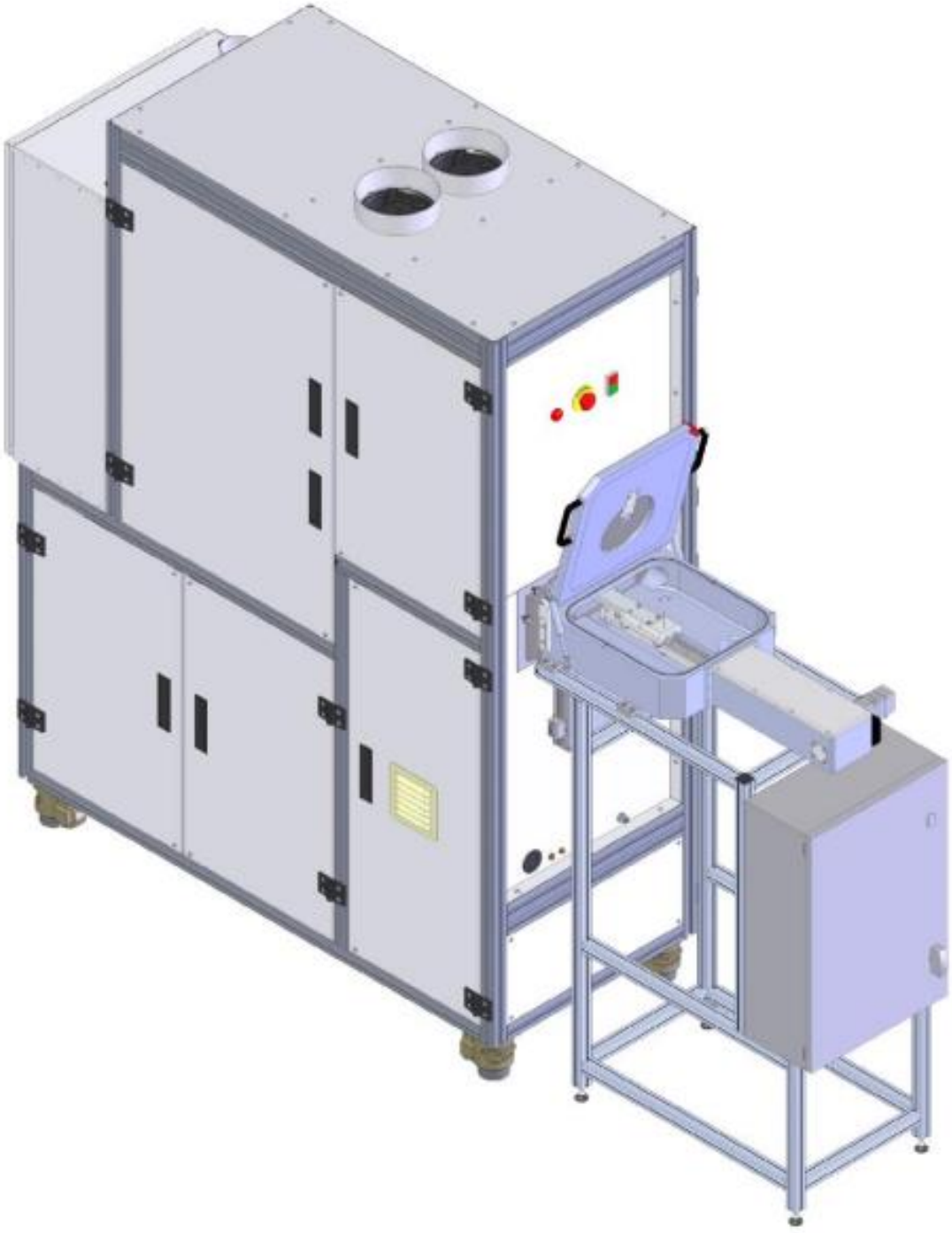

Figure S1 – A 3D digital model of the rapid thermal processor used in this work. RTP AS-Premium, serial number AS0415C4 - 7484, from ANNEALSYS. The image was adapted from the tool's user manual, available in a closed-access DTU database.

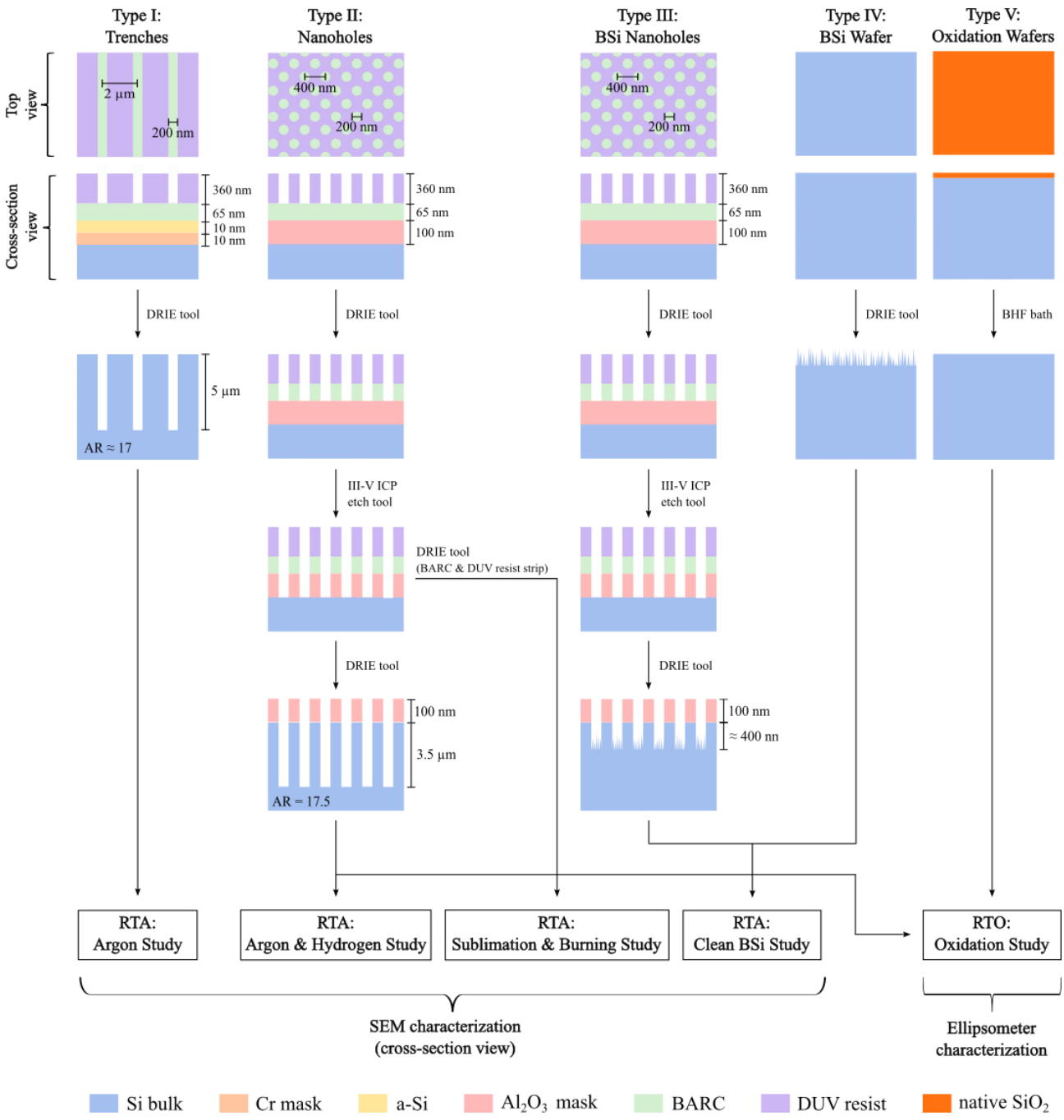

Figure S2 – Schematic representation of the fabrication process flow for each type of samples used during the experimental work. The drawings are not to scale.

Figure S3 – Image of the DRIE tool used in this work. Nemotek Advanced DRIE Pegasus 2, serial number MP0641, from SPTS. The picture was obtained from a closed-access DTU database.

Figure S4 – Image of the ICP etch tool, primarily dedicated to etching III-V materials, used in this study. III-V PRO ICP, serial number MP0647, from SPTS. The picture was obtained from a closed-access DTU database.

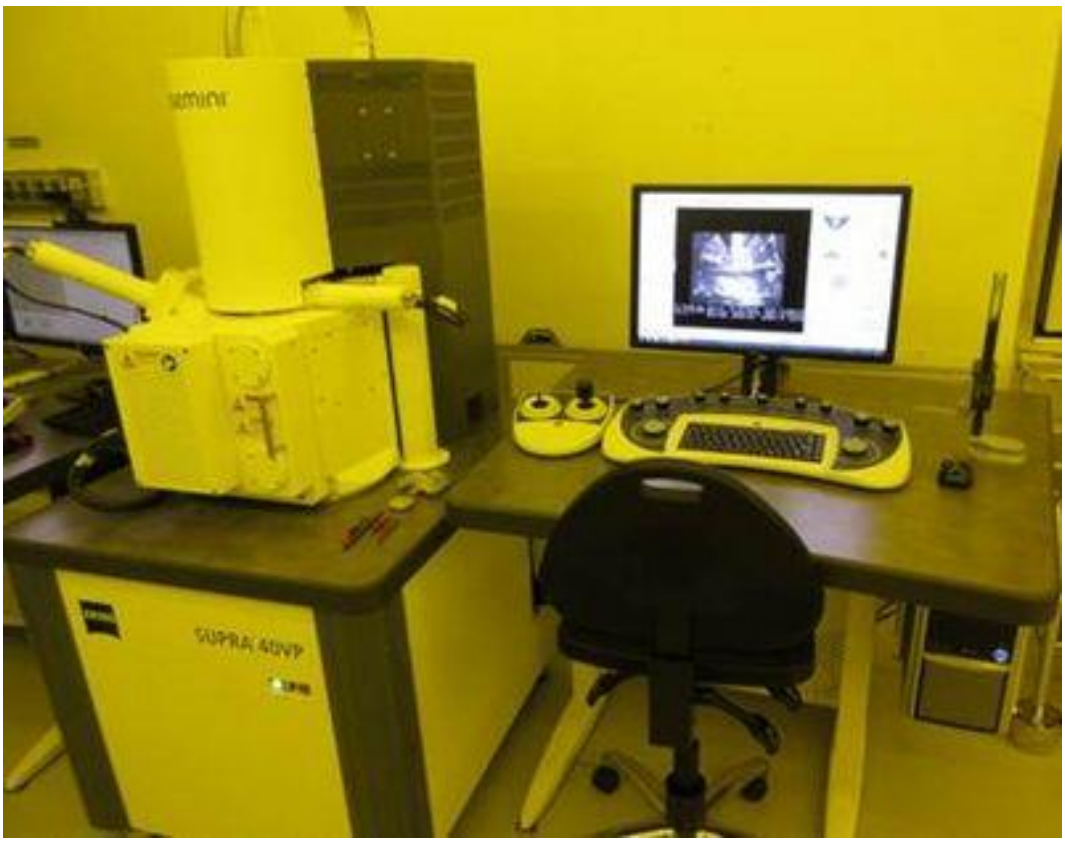

Figure S5 – Image of the SEM tool used to characterize the samples throughout the experimental work. Zeiss Supra 40VP SEM, serial number 4825. The picture was obtained from a closed-access DTU database.

Figure S6 - Image of the VASE ellipsometer tool used to characterize the samples in the 'Oxidation Study'. M2000XI-210 ellipsometer from J.A. Woollam Co., Inc.. The picture was obtained from a closed-access DTU database.

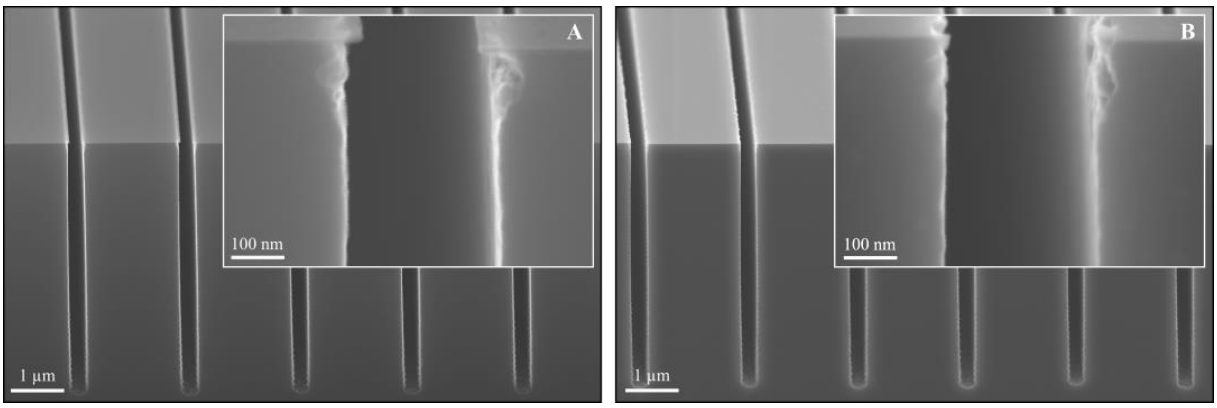

Figure S7 - Trenches samples (A)before and (B)after Cr hard-mask layer removal. The samples represented by (B) were used in the Ar study. Cross-section SEM images, 20º tilt and electron high tension (EHT) (A)20 kV and (B)5 kV.

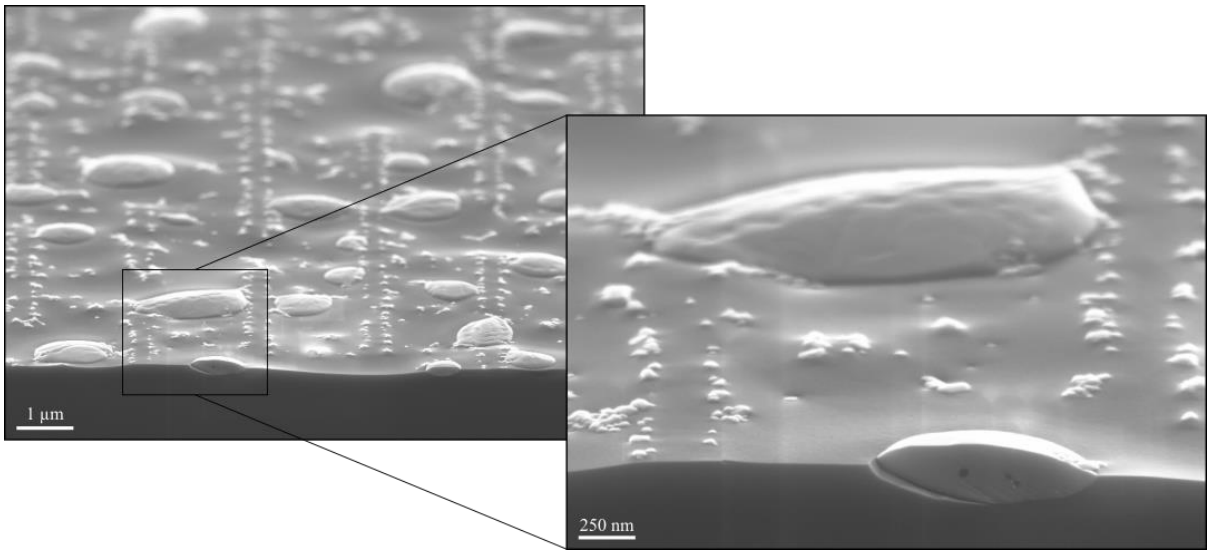

Figure S8 - Effect of rapid thermal annealing for 3 min - 80 % of lamp power (≈ 1300 ºC), 40 SCCM Ar, 12 mbar - on the Cr hard mask at the edge of the sample (non-patterned area). Cross-section SEM images, 20º tilt and EHT 5 kV.

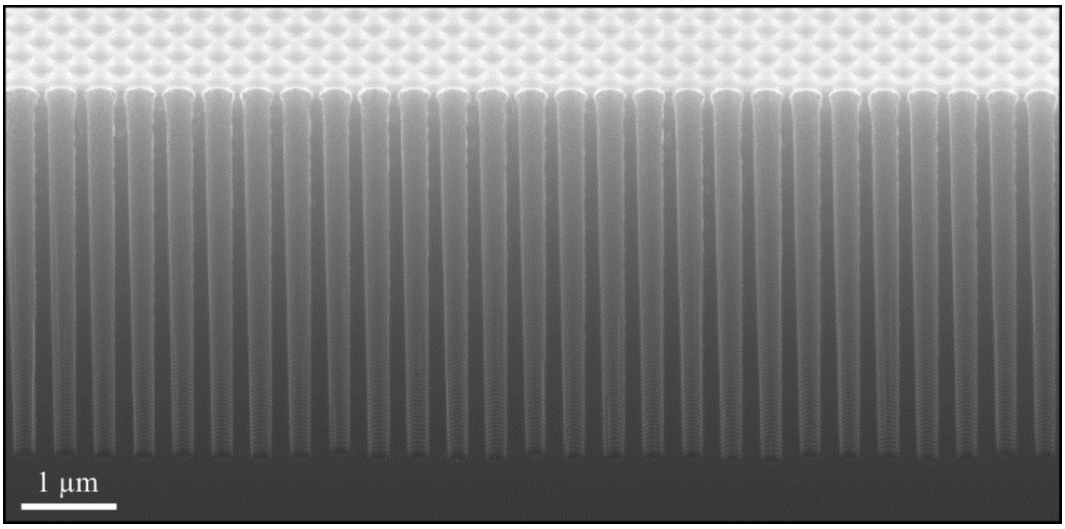

Figure S9 – Nanoholes sample from a new batch after re-conditioning the DRIE tool. The holes are 4 µm deep and have a 200nm-diameter and 400nm-pitch. Cross-section SEM images, 20º tilt, EHT 20 kV