NOVA SCHOOL OF SCIENCE & TECHNOLOGY

DEPARTMENT OF MATERIALS SCIENCE

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Bachelor in Micro and Nanotechnology Engineering

SF_6/O_2 PLASMA ETCHING: OPTIMIZING THE CORE PROCESS AND GOING INTO 3D ENGINEERING

MASTER OF SCIENCE IN MICRO AND NANOTECHNOLOGY ENGINEERING

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Para a minha avó Gena.

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"Ter um destino é não caber no berço onde o corpo nasceu, é transpor as fronteiras uma a uma e morrer sem nenhuma."

Miguel Torga

ABSTRACT

Silicon plasma etching is a well-known method, extensively studied, that has been revealing some drawbacks recently since the technology is constantly evolving, and the techniques have to improve to keep up with it. As plasma etching techniques advanced, the microfabrication industry expanded, but so did the environmental costs of these operations. Therefore, finding ways to lessen the ecological imprint is urgent. One way to do it is to substitute pollutant chemicals daily used in the industry by others with lower environmental impact. Directly in plasma etching, the Bosch process uses both SF_6 and C_4F_8 that has a Global Warming Potential with time horizon of 100 years (GWP_{100}) of 23500 and 9500 times more potent than the known CO_2, respectively, having both a lifetime of more than 3000 years; making C_4F_8 one of the most potent greenhouse gases detected in the atmosphere to date.

A new method of silicon plasma etching, called CORE (Clear, Oxidize, Remove, Etch), has been developed to solve it. This fluorocarbon (FC) free directional silicon etching process switches between SF_6 and O_2 cycles. The O_2 Oxidation replaces the common C_4F_8 of Bosch's approach, being more beneficial for the industry as it prevents FC pile-up at the topside of nano-sized structures and minimizes drift due to the clean reactor walls. In this study, high aspect ratio (HAR) features were fabricated, starting with a Cr mask that later was changed to Al_2O_3, to obtain different patterns, i.e., trenches, pillars, 1 µm and 200 nm holes, to understand the different behaviors. Even though some tool setbacks occurred, reliable recipes were achieved for each type of pattern, and by using Rapid Thermal Processing (RTP) to anneal the etched samples, buried cavities were also accomplished. With greater selectivity, independent etching profiles, room-temperature operation, and the possibility of producing black silicon (BSi) on demand, this technology meets the current requirements.

Keywords: CORE process, high aspect ratio (HAR) features, deep reactive ion etching (DRIE), SF_6/O_2 plasma, annealing, buried cavities.

RESUMO

A erosão seca de silício é um método amplamente estudado, que tem vindo a revelar alguns inconvenientes recentemente, visto que a tecnologia está em constante evolução e os métodos têm de melhorar para se manterem atuais. Com o desenvolvimento destas técnicas, a indústria da microfabricação evoluiu e as consequências ambientais associadas aumentaram. É urgente procurar soluções para reduzir a pegada ecológica, e uma forma de o fazer é substituir as substâncias químicas poluentes utilizadas por outras de menor impacto ambiental. Nomeadamente o processo Bosch utiliza SF_6 e C_4F_8 que têm um potencial de aquecimento global (PAG) de 23500 e 9500 vezes mais forte que o CO_2, respetivamente, tendo ambos uma vida útil de mais de 3000 anos; fazendo do C_4F_8 um dos gases com efeito de estufa mais potentes detetados na atmosfera até à data.

Para o resolver foi desenvolvido um novo método de erosão seca de silício, chamado CORE (Clear, Oxidize, Remove, Etch). Este processo de erosão de silício direcional sem fluorocarbono (FC) comuta entre ciclos de SF_6 e O_2. A oxidação de O_2 substitui o C_4F_8 comumente usado no processo de Bosch, sendo mais benéfico para a indústria uma vez que evita a acumulação de FC na parte superior das estruturas e as paredes do reator permanecem limpas. Neste estudo foram obtidas perfis com elevado razão de aspeto, começando com uma máscara Cr que mais tarde foi alterada para Al_2O_3, utilizando diferentes padrões, valas, pilares e furos de 1 µm e 200 nm, para compreender os diferentes comportamentos. Embora tenham ocorrido contratempos com a máquina, foram conseguidas receitas fiáveis para cada tipo de padrão e, utilizando o RTP para recozer as amostras, foram também conseguidas cavidades enterradas. O CORE dá resposta às necessidades atuais com alta seletividade, independência dos perfis, pode ser operado à temperatura ambiente e torna possível produzir *black silicon* (BSi) a pedido.

Palavras chave: Processo CORE, perfil com elevada razão de aspeto (HAR), erosão reativa iónica em profundidade (DRIE), plasma de SF_6/O_2, recozimento, cavidades soterradas.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACRONYMS

ALD	Atomic Layer Deposition
APC	Automatic Performance Control
AR	Aspect Ratio
ARDE	Aspect Ratio Dependent Etching
aSi	Amorphous Silicon
BARC	Bottom Anti-Reflective Coating
BSi	Black Silicon
CCP	Capacitively Coupled Plasma
CORE	Clear, Oxidize, Remove, Etch
CPR	Center Point Run
DC	Direct Current
DEM	Deposit, Etch, Many times
DREAM	Deposit, Remove, Etch, Ash, Many times
DREM	Deposit, Remove, Etch, Many times
DRIE	Deep Reactive Ion Etching
DUV	Deep Ultraviolet
ER	Etch Rate
EU	European Union
FC	Fluorocarbon
GWP	Global Warming Potential
HAR	High Aspect Ratio
HF	High Flow
HP	High Pressure
IAD	Ion Angular Distribution
ICP	Inductively Coupled Plasma
MEMS	Micro Electromechanical Systems
MFC	Mass Flow Controler
PAG	Potencial de Aquecimento Global

RF	Radio Frequency
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
RTP	Rapid Thermal Processing
SEM	Scanning Electron Microscope

MOTIVATION AND OBJECTIVES

From the beginning of the transistor development, the pattern sizes have been lowered to create more functionality and computing power in smaller chips. Modern nanodevices are being downscaled continuously, which calls for ever-improving performance from the underlying fabrication processes. These techniques include lithography, film deposition, and etching, which are carried out in cleanroom facilities. In order to miniaturize electronic devices, lithography has long been the bottleneck and the main focus. In addition, the vertical dimension is getting increasing attention in order to further improve the device density as the lateral dimensions have possibly reached the limit of what appears to be feasible [1]–[3].

Hence, dry plasma etching is vital in today's semiconductor industry, allowing to attain anisotropic patterns, sculpture precise and deep features and even clean or roughen surfaces, among others. Each of these factors makes it possible to exploit high aspect ratio (HAR) characteristics for multiple applications, i.e., microelectromechanical systems (MEMS), microactuators and sensors, optics, and microfluidics [4]–[9]. However, in the following years, the lateral dimensions will hit a limit as they will attain what is now possible due to More Moore's law becoming progressively inaccurate [10]. Consequently, the new focus is on the miniaturization of vertical dimensions with plasma etching to upgrade the device density since this technique has a low impact on the environment compared to others in the industry [11]. The main challenge is the Reactive Ion Etching (RIE) lag since when the aspect ratio (AR) increases, the etch rate (ER) of the mask remains the same while the silicon ER decreases, putting the mask at risk of being completely eroded. Different hard mask materials with high selectivity to etching on Si have been studied to tackle this issue, such as Cr, SiO_2 and Al_2O_3 [12]–[15].

Addressing the current etch state-of-the-art, one of the most chosen silicon etch mixtures of gases is SF_6, sulfur hexaflouride, and C_4F_8, octafluorocyclobutane, combined, using the Bosch process. However, SF_6 is one of the gases with higher greenhouse effect, with a Global Warming Potential (GWP) of 23500, meaning thst 1 mol of SF_6 is 23500 times stronger than 1 mol of CO_2 to global warming [16]. Moreover, SF_6 has a 3000 years lifetime, making future atmospheric repair difficult, if not impossible. Regarding C_4F_8, the GWP_{100} is 9500 times stronger than CO_2 and has approximately the same lifetime as SF_6, making C_4F_8 one of the most potent greenhouse gases detected in the atmosphere to date, behind SF_6.

In addition, there is a recent acceleration in the EU to go for a total ban on fluorocarbons (FCs) [17], [18]. The change to green gases for the etch process is late, but it is crucial to start focusing on the matter. Although the contribution of these potent greenhouse gases is less than 1% when compared to CO_2 contribution, it is vital to remember that these gases have a long lifetime, making the future consequences devastating. Moreover, some of these gases will be banned, as C_4F_8, obligating the industry to search for greener resources to replace FCs. Thereby, the Clear, Oxidize, Remove and Etch (CORE) process was invented, a four-step process that uses less SF_6 feed and removes C_4F_8 from the equation, being just the start in the direction of a zero GWP plasma etch process.

With this thesis work, HAR features and different patterns will be studied in order to know more about this promising high accuracy etch process, having more fixed recipes, some faster ones and others more accurate for each pattern type.

1. INTRODUCTION

Within the last years, plasma etching evolved and can be categorized according to the introduction of the etch gases into the etch tool, being divided into two methods. One technique is the mixed mode, in which the etch gases are added to the chamber simultaneously. The other is the switched mode in which the etch gases are sequentially fed into the chamber during the etching process. Depending on the type of gas used to protect the sidewall, silicon etching can be divided into oxygen-inhibitor or FC-inhibitor. By now, the mixed mode has both $SF_6 + C_4F_8$ and $SF_6 + O_2$, and the switched mode has SF_6/C_4F_8, the known Bosch process and the new addition SF_6/O_2, being the CORE process.

In the mixed mode, the etch selectivity between silicon and the mask material is mainly affected by the continuous bias applied [19]. The DC-self bias is formed when the RF voltage (platen power) is applied. As the bias increases, the ion bombardment will increase, creating the requested directionality. However, this increased directionality can cause the mask to be totally eroded with time, not protecting the sample anymore. Besides, if it is an $SF_6 + C_4F_8$ mixed mode, the chamber is contaminated due to the FC inhibitor, making the etching results difficult to predict. Alternatively, for the same mode with an O_2 inhibitor, the selectivity is improved as the bias applied is lower. Although the selectivity improved, it was insufficient to withstand some processes. Moreover, the mixed mode presents another disadvantage of being pattern-dependent, making optimization a difficult task, not being embraced by the semiconductor industry. Nevertheless, when solely using O_2 as an inhibitor, the mixed mode is clean with low process drift and is tool-friendly.

When going for the switched mode with the inlet of SF_6 and C_4F_8 sequentially, the process allows for good sidewall protection and directionality, creating visible scallops. Furthermore, the pattern dependency is almost nonexistent, allowing for good tuning and enabling 3D engineering by optimizing the parameters of each step. Moreover, it has more selectivity than the mixed mode due to bias only being applied during the etch step instead of during the entire process, as in the mixed mode.

1.1 Reactive Ion Etching Evolution

Etching methods have advanced remarkably in the past few decades. Different techniques have been created, using a chemical process, a physical one, or combining both. Pure chemical methods involve a chemical reaction between a reactive species (typically in the form of a solution or gas) and the substrate material. While this approach can achieve high values of mask selectivity, the etch is mainly isotropic, as the etch rate is roughly identical in all directions. Purely physical etching, such as ion milling, involves the removal of substrate material by momentum transfer of energetic chemically inert particles. The combination of both chemical and physical methods integrates chemically reactive species with momentum transfer, resulting in selectivity and anisotropy. The reactive ion etching falls into the latter group, achieving the required characteristics for advanced microfabrication etching.

The RIE method is part of the dry etch spectrum of techniques that depend on the pressure used during the etching. For instance, RIE occurs when the process pressure is between 10^{-1} and 10^{-3} torr. For ion milling

lower pressure is used, and for plasma etching is higher pressure until 10^2 torr. With the development of RIE, techniques such as the inductively coupled plasma (ICP) etch started to appear. This technique is better suited for deeper and HAR etching, as in bulk micromachining. While ICP etching allows for deeper etching, it is insufficient for HAR anisotropic etching of single-crystal silicon, resulting in the creation of the Deep Reactive Ion Etching technique (DRIE) [20], [21].

Several novel DRIE methods were developed in the 1990s, allowing the etching of hundreds of microns into single-crystal silicon. The Bosch Process was one of them, introduced by Robert Bosch in 1993 [22]. The Bosch is divided into two different processes, the cryogenic one, which is very difficult to adequate to complex patterns since it has pattern dependency due to being a mixed mode, and the DEM (Deposit, Etch, Many times), which has low pattern dependency being a switched mode procedure, but still having the bias coupled [22]. To overcome it, DREM (Deposit, Remove, Etch, Many times) was developed in 2018, having the bias decoupled from the etch step, being possible to set and adjust the time to remove just the bottom of the desired feature, enabling a theoretically endless mask selectivity. However, at HAR features, the RIE lag is very pronounced in DREM, decreasing the silicon etch rate with the increasing etch depth, while the mask etches rate remains the same. Although DREM can counterattack the problem by increasing the ramping time (etch time of one cycle), achieving features with HAR over 50 still has another problem. The pile-up of FC can clog trenches or holes, closing their entrance and limiting its use in nanoscale features [2], [23], [24]. The FC pile-up can be overpassed by fine-tuning the recipes. However, it is a long-lasting process and, therefore, impractical.

Adding an extra ash step after the etch and a new method arises, DREAM, with less drift and pile-ups, since the ash step removes de FC to prevent clogs and cleans the chamber walls. The process has a C_4F_8 deposition, bottom removal with Ar, etching with SF_6, and ashing with O_2, repeating many times. However, the infinite selectivity is lost, considering that the photoresist will erode quickly due to the constant removal of FC, making DREAM mainly used with hard mask materials [23].

The goal is to reach and combine the advantages of the mixed mode with the switched mode. The last one is user-friendly and gives design freedom and 3D options due to the pattern independence. Additionally, the mixed mode barely drifts, is easy to maintain, and is a clean process since it uses oxygen as an inhibitor instead of the FC commonly used in the switched mode. Unfortunately, FC gases are not environmentally friendly and are more expensive than oxygen. Besides, the FC also contaminates the chamber causing notorious drift. Knowing the advantages and challenges of each mode, the CORE process is developed, mixing the benefits of both modes. It started with replacing the C_4F_8 inhibitor from DREAM for O_2, which meets the need for a greener process.

1.1.1 CORE process

The CORE is a four-step process, Clear, Oxidize, Remove and Etch, in which all the parameters are interconnected. The SPTS/Pegasus Advanced DRIE tool is dedicated to SF_6/O_2 based plasma etching and has no prior FC history. This FC-free chamber is needed to prevent contamination or influence on the fragile oxygen plasma oxidation required for the CORE sequence. In **Figure 1.1**, a schematic of the CORE process is presented, and to further understand it, the next sub-chapters will succinctly describe each step.

1.1.1.1 Clear Step

The clear step is crucial for the performance of the CORE process. Some SiF_x products from the last SF_6 plasma etching step stay in the chamber walls and must be cleared so the oxidation step can occur correctly. So, a sweeping O_2 flow with no power applied is performed to clear the chamber and the sample's surface of the remaining products of the last etch. If the step is not carried out properly, either the incoming O_2 will be obliterated by the fluorine radicals or the oxygen radicals will react with SiF_x to form silicon-oxide species, compromising the passivation.

It was observed by Nguyen *et al.* [11] that is was needed 4 s of clear for a successful clear step of a 1 µm diameter pillar. Therefore, only after 4 s that F products and O_2 radicals are correctly separated. However, before the 4 s, the profile is highly undercut as new incoming oxygen radicals are lost due to annihilation with the F radicals from the previous E-step [11]. Besides, if not correctly separated, SiF_4 is one of the possible etch products that, if in contact with O radicals might form SiO_2 particles, forming black silicon (BSi).

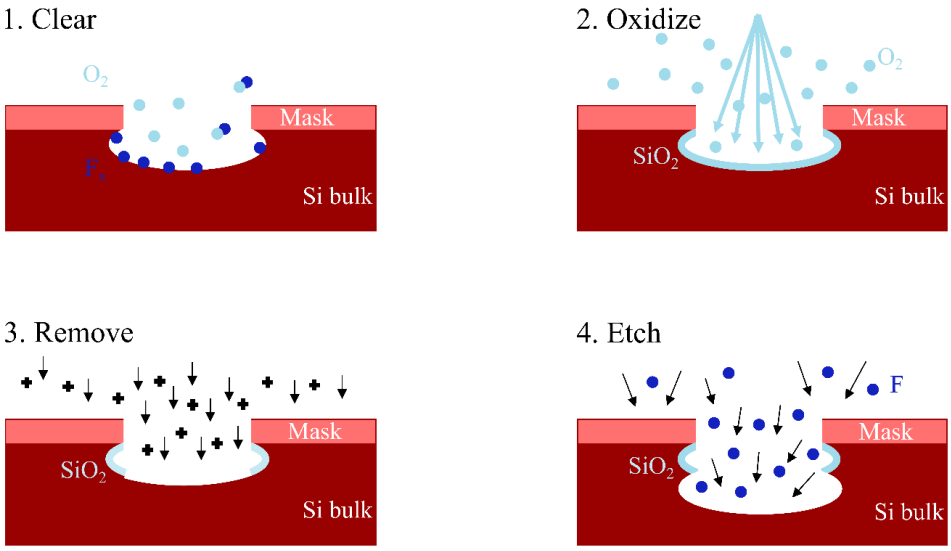

Figure 1.1- CORE process steps: clear, oxidation, removal and etch. In the clear step, a sweeping flow of O_2 without power is added to clear the remaining F-products from the last etch step. For the oxidation, an O_2 flow is added to O-terminate the sample surface. For the removal, the incoming ions remove only the bottom of the sample, giving directionality to the process and the etch step with a powerful SF_6 flow etches the feature, providing depth to the structure.

1.1.1.2 Oxidize Step

Even though the surface was cleared in the previous step, some fluorine products remain in the Si substrate. Therefore, to create a thin layer of SiO_2, the F-products are replaced by oxygen-terminated products on the Si surface once the oxidation stage has begun. It was documented by Nguyen *et al.* [11] that it was possible to understand the time relation between steps. Hence, the duration of the oxidation step follows the first rule of CORE design [11]:

I. Every extra second of oxidation time needs 2 extra minutes of etch time until a maximum of extra 8 s O-time.

Moreover, it was still documented that it is only after at least 5 s of oxidation that the scallops created by the process start to become smooth. From 8 s of O-time on, the rule cannot be used anymore since the

relation between the etch and oxidation times becomes nonlinear caused by the oxidation process's self-terminating feature, which stops after nearly 2 nm. This is due to the silicon oxide acting as a diffusion barrier, similar to heat oxidation [11].

1.1.1.3 Remove Step

This next step gives the so-needed directionality to the process, while using low SF_6 flow. In the removal step it is essential to remember that the higher the plasma potential, the lower the pressure since plasma potential is a function of the pressure [25], [26]. Low pressure creates a high plasma potential in combination with the DC self-bias. This will further straighten the ion trajectory. With that in mind, the plasma potential is tuned by fully opening the throttle valve through the removal step by adjusting the reactor pressure. This enables the process to operate at very low pressure ensuring the directional path of the incoming ions and making sure that ions remove the thin oxide layer on the horizontal surfaces.

For an accurate removal rate, the second rule of CORE design [11]:

II. Every second of Oxidation time needs at least 3 s of Remove time (for a fixed 8 minutes of etch time).

It was seen by Nguyen *et al.* [11] that at the beginning, with only 5 s, the surface is still rough with the so-called black silicon, and only when it reaches 25 s that the bottom becomes clear. However, after 25 s, the bottom becomes rougher due to silicon damage below the passivation, lowering the mask etch selectivity, which is undesirable.

1.1.1.4 Etch Step

For the last step, it is essential to remember that the lateral and vertical dimensions do not have the same etch rate, being responsible for the amount of undercutting, controlling the profile [2], [11]. Unlike the removal step, during the etch, both pressure and SF_6 flow are generally high. This etching step is done between the ideal viscous transport and the ideal free molecular transport, having a vertical etch two or three times faster than the lateral rate. If the maximum value of etching is surpassed, the scallops' protection starts to be eroded by the etch plasma. This is important to set the third rule of CORE design [11]:

III. The undercut is roughly half of the gained etch depth per CORE cycle.

As reported by Nguyen *et al.* [11], the sidewall pitting starts to appear after 4 minutes of etching. After that, the scallop's oxide protection starts to be degraded by the continuous etching, depending directly on the previous oxidation time. It is also notorious that open-field structures suffer more damage for extended etching when compared to closed-field structures.

1.1.2 Additional remarks

When the CORE sequence is performed at an extended E-time, more than 2 minutes, surface particles below a certain threshold of lateral size will be totally undercut, making the surface relatively smooth. The shorter the E-time, the smaller this threshold will be, resulting in more particles that can survive the lateral undercutting. Subsequently, surface roughening is more pronounced with lower E-time. To withstand that, a

longer R-time is needed to prevent this issue. Using this fine-tuned CORE cycle, the scallop-size decreases and suitable profiles emerge with smooth, straight sidewalls and minimal resist mask undercutting [2], [11].

Regarding the formation of plasma during the process, it is imperative to respect the balance between the parameters of each process step, constantly tuning them. Furthermore, as the plasma is formed by the electromagnetic field that is maintained by the inductivity and capacity of the chamber, it is also essential to maintain the chamber with the same conditioning throughout all processes, just changing the needed parameters for each step as mentioned. This emphasizes the importance of having a conditioning window to guarantee that no excesses that could disrupt chamber conditioning are performed.

As with DREAM, the CORE process also allows to do 3D patterns. Combining a CORE cycle interspersed with a short isotropic etch can create a 3D pattern, and tuning both cycles will create different results. However, it is essential to notice that the passivation of the sidewall has to be enough to withstand the following isotropic etch, not compromising the top part of the structure. This process enables the production of HAR features with good performance designs in several areas [11], [27].

Despite the CORE focus on the nanoscale, it is also being explored to increase MEMS performance to find a higher etch rate limit. With the CORE process design rules limiting E-step time, the approach is to add an ICP source to promote stronger oxidation, enabling higher F-pressure during the etch step. In addition, when using the ICP source, the platen source can be removed, taking out the DC bias and improving selectivity [28]. Adopting a faster etch rate implies sacrificing nanoscale accuracy. The increased F-pressure and bigger undercut at the sidewalls are responsible for this accuracy loss. Furthermore, sidewall sputtering is more common in faster etch rates, compromising the etch process.

Even though these limitations can make the process less appealing, making it faster would be a significant advantage, enabling the process to compete with Bosch. Moreover, a Faraday cage would address the sidewall sputtering caused by the ICP source.

2. MATERIALS AND METHODS

This chapter will describe the study methodology, from the fabrication procedure to the characterization techniques used. Sample fabrication is shown in **Figure 1.1**, starting with a chromium (Cr) mask and later changing to aluminum oxide (Al_2O_3). The sample design includes microscale and nanoscale features to be able to study both cases simultaneously. The CORE process is tested with a screening approach followed by some rapid thermal annealing tests. The last subchapter describes the characterization techniques used in the process.

2.1 Sample fabrication

All steps taken to produce the desired wafers are shown in **Figure 2.1**. Silicon 150 mm wafers were used to fabricate the samples to etch with the CORE process. The wafers were cut into approximately 1 cm x 1 cm, meaning that one wafer would give between 30 to 40 chips to process in Pegasus 2 tool (Nemotek Advanced Deep Reactive Ion Etching (DRIE) Pegasus 2, serial number MP0641), presented in **Figure S. 1**.

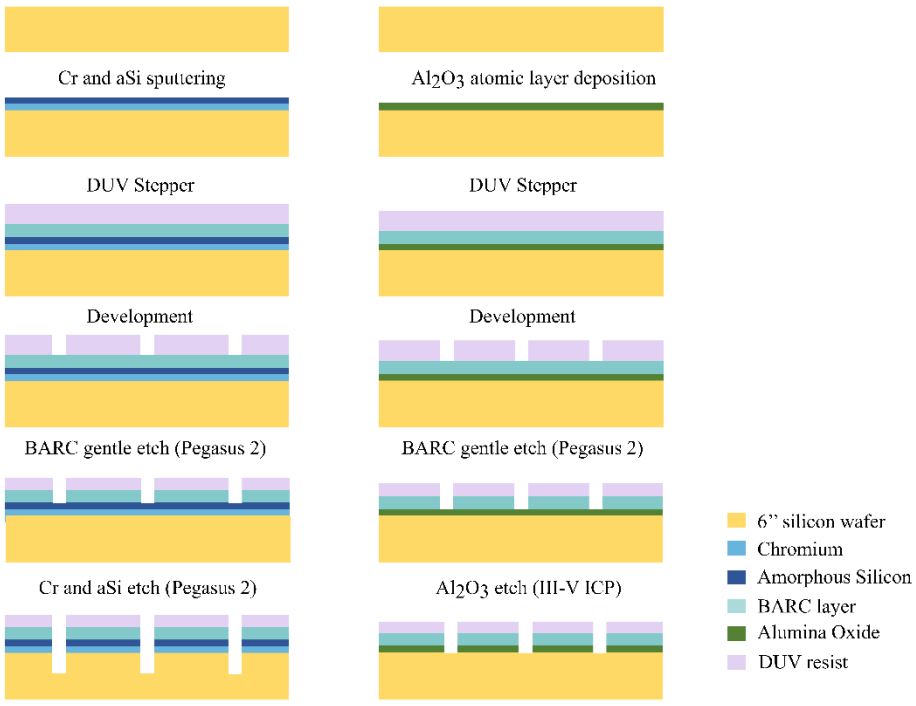

Figure 2.1- Scheme of the sample fabrication using different mask materials. On the left are the chromium samples where 10nm of Cr and aSi are deposited, then 65 nm of BARC and 360 nm of DUV resist. On the right are alumina oxide samples where different layers of 50 and 100 nm Al_2O_3 were deposited, followed by 65 nm of BARC and 750 nm of DUV resist. No at scale.

2.1.1 Chromium hard mask samples

The 150mm Si wafers were coated with 10 nm of Cr and 10 nm of aSi in a single run without breaking vacuum in a high vacuum sputtering deposition system (Sputter-system for DC/RF sputtering, Model 2017

PRO Line PVD75, Lesker) presented in **Figure S. 2**. Important to mention that aSi was deposited after the Cr to assure the pattern transfer during the Cr etch, as photoresist offers low selectivity towards Subsequently, lithography was done using the DUV stepper (Canon FPA-3000 EX4) presented in **Figure S. 3** to deposit 65 nm of BARC, bottom anti-reflective coating layer (DUV42S-6) to better control the critical dimentions uniformity, and 360 nm of DUV resist (KRF 230Y). As mentioned previously, each wafer had multiple patterns of 1 cm x 1 cm trenches, with 200 nm diameter and 2 µm pitch. The BARC layer was etched on Pegasus 2 for 12 minutes using the recipe "BARC gentle etch". The Cr and aSi layers were etched in a single run along the CORE process in Pegasus 2, as described in **Figure 2.1**. Afterwards, the wafer was cleaved into samples approximately 1 cm x 1 cm to test the CORE process in Pegasus 2.

2.1.2 Alumina hard mask samples

In these samples, the hard mask, Al_2O_3, was coated in the 150 mm Si wafers using the atomic layer deposition tool (ALD Picosun R200), presented in **Figure S. 4**. These sets of samples also had the lithography process done in the DUV stepper (Canon FPA-3000 EX4) to deposit 65 nm of BARC and 750 nm of DUV resist. Three different patterns were created after the development:

I. Pillars of 1 µm with 1 µm pitch (50 nm Al_2O_3 + 65 nm BARC + 750 nm DUV).
II. Holes of 1 µm with 1µm pitch (50 nm Al_2O_3 + 65 nm BARC + 750 nm DUV).
III. Nanoholes of 200 nm with 400 nm pitch (100 nm Al_2O_3 + 65 nm BARC + 750 nm DUV).

The Si/Al_2O_3/BARC/DUV stack was first processed in Pegasus 2 to etch the BARC layer, and the alumina was etched in the III-V ICP tool (III-V Inductively Coupled Plasma, SPTS serial number MP0647), presented in **Figure S. 5**, using a BCl_3/Ar recipe. With pillars and holes, the BARC was etched for 12 min on Pegasus 2, followed by 90 minutes on the III-V ICP. The nanoholes had two different approaches, starting with 260 minutes on the III-V ICP. However, it was seen that after the III-V ICP process, the leftover resist on the sample was removed during the CORE process on Pegasus 2.

2.2 Etching experiments

A deep reactive ion etching (DRIE) tool was used to test the CORE process. Pegasus 2 is an STPS DRIE etch tool designed for Bosch processes, but it was modified to withstand CORE. On Pegasus 2, 1 cm x 1 cm chips are processed on top of a 150 mm Si carrier wafer without electrostatic clamping, helium backside cooling, galden oil, or any other bonding technique. Also, all four chamber heaters are off, the temperature process is ca. 20 °C, and the outer electromagnet is set at 10 A.

Regarding the CORE process, the microscale was first tested with 200 nm trenches with a Cr mask and then with the 1 µm pillars and holes with an Al_2O_3 mask. The nanoscale was also tested with the 200 nm nanoholes. In both cases, the process has these two steps, the "plasma strike" and the "Dedam etch". The first one is to initiate and stabilize the plasma for the subsequent processes. The second is a gentle etch to remove any wafer process history, such as native oxide or resist scum.

The process has multiple steps for the Cr samples in a single run, as shown in **Figure 2.1**. The first steps were already reasonable, and only the CORE process recipe was optimized and studied, tuning the needed parameters. Important to notice that Pegasus 2 has two modes of pressure, valve control, represented by a

percentage of how open the valve is, and pressure control, as in the BARC strike step (**Table 2.1**), having a fixed value in mTorr. The Al_2O_3 hard mask samples only had two previous steps to the CORE, the Dedam strike and the Dedam etch, as shown in **Table 2.2**.

Table 2.1- Process parameters for a single run with CORE in Pegasus 2. BARC strike needed to initiate the plasma to then etch it. Next, Dedam etch is performed to clean the remaining particles on the surface and the amorphous silicon etch. The chromium etch is a two-step process, and then the resist strip concludes it before the real CORE process starts. Trench sample used.

		Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
BARC strike		10	10 mTorr	50	0	0 → 20
BARC etch		720	100%	50	0	10
aSi etch		180	100%	5	5	20
Resist strip		900	2.5%	200	0	40
Cr etch	**D**	9	2.5%	50	0	40
	E	1	2.5%	50	3	40
Dedam etch		60	100%	0	15	10
CORE process						

Table 2.2- Parameters of previous CORE process steps for the aluminum oxide hard mask samples. Dedam strike is done to initiate the plasma and the Dedam etch is performed to clean the remaining particles on the surface before the CORE process starts.

	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
Dedam strike	10	10 mTorr	0	15	0 → 20
Dedam etch	60	100%	0	30	10
CORE process					

2.3 Annealing experiments

Rapid Thermal Annealing (RTA) was performed on different etch profiles with the Rapid Thermal Processor (RTP, AS-Premium serial number AS0415C4-7484, ANNEALSYS), presented in **Figure S. 6**. The recipe used for the RTA was "RTA 1250 HP HF MAX", using 1250 °C for 8 s while using 74 mbar, 2000 SCCM of Argon and 2000 SCCM of 5 % H_2/Argon. This recipe was chosen since it was believed to be the most successful in forming buried cavities.

2.4 Characterization Techniques

The leading equipment to characterize this project's samples was the SEM (serial number 4825, acceleration voltage 20 V - 30 kV), presented in **Figure S. 7**. This essential analytical tool offers a remarkable depth of field and resolution. The secondary electrons were used, as it gives information about the topography of each sample. In addition, SEM pictures of the sample's cross-section were taken at a 20° tilt to analyse the features and without inclination to measure the features.

3. RESULTS AND DISCUSSION

3.1 Microscale CORE etching

Studying CORE at the microscale puts this process one step closer to competing with the old Bosch process, and the ultimate goal is to have a greener process included in the microfabrication technology. For this purpose, different patterns were fabricated, the 200 nm trenches, the 1 µm pillars and the 1 µm holes. These different patterns show the CORE possibilities and what to consider with each type of recipe. The standard recipe to start all tests is presented in **Table 3.1**.

Table 3.1- Standard recipe for CORE process.

	Time (s)	**Pressure**	**O_2 flow (SCCM)**	**SF_6 flow (SCCM)**	**Platen power (W)**
C-step	4	100%	50	0	0
O-step	3	0.5%	50	0	15
R-step	20	100%	0	5	15
E-step	53	1%	0	15	15

3.1.1 Trenches

CORE tests with the 200 nm trenches pattern were performed to study the influence of each process step. To fully understand the impact of each step, experiments eliminating one step at a time were carried out. In **Figure 3.1**, COR structure accumulates the self-terminated oxygen layer on the sideways until the layer reach ~ 3 nm, so it starts to get a positive etch profile as the etch step is not present. If the R-step were eliminated, the bottom of the feature would not be removed, causing the next E-step to not etch properly due to the passivation layer created in the bottom. It would probably etch initially, but the passivation would start to be too big to be completely etched, stopping the process. Even though the bottom part would not be etched anymore, the top part would continue to be under attack, almost resembling an isotropic etch or presenting a positive profile [2], [11]. For the ORE, the feature gets deeper than CORE, 933 nm and 745 nm, respectively. Regarding the width variation, both are practically insignificant, of 9 nm and 6 nm, respectively, but for the ORE, the trench width is closer to 200 nm than in the CORE feature. For this particular recipe, the ORE recipe seems to be advantageous, evidencing deeper and with less width variation features. However, to decide either to go for CORE or ORE, the final application will impact this decision. If a accurate profile is needed, without visible scallops, the Clear step will be needed, as the cycles will be processed with less power and take longer. Though, if going for a scallops profile, the C-step may not be needed, as the recipe will have faster cycles with higher powers.

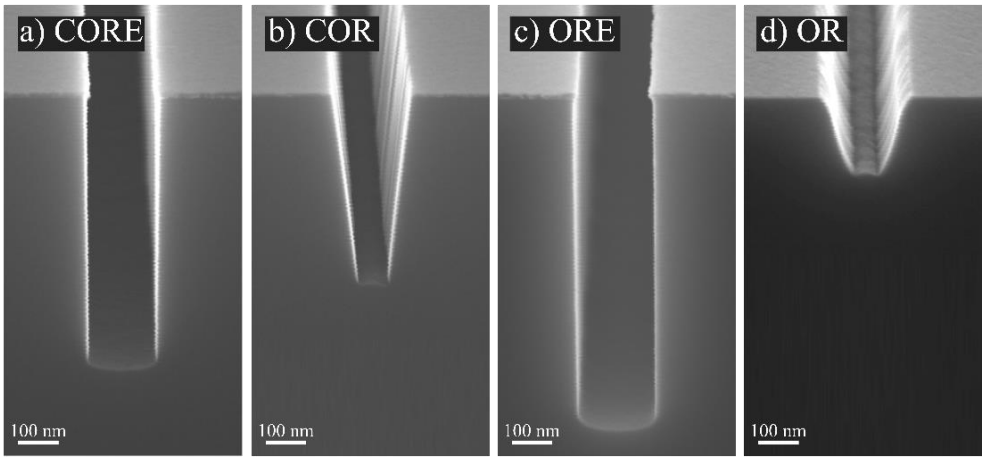

Figure 3.1- Effect on 200 nm trenches of each step by experimenting with elimination of one step at a time, reaching: a)745 nm, b) 517 nm, c) 933 nm and d) 224 nm. SEM images are tilted 20°.

Moreover, the oxidation time, the removal power and time were analyzed. Starting with time tests, the time of the C-step and O-step were varied, making 7 s in total. Regarding **Figure 3.2**, the Oxidation time, O_t, is increased to search for an optimal value and relation between clear and oxidation steps. It is clear that having more C-time than O-time is not ideal (O_t= 3 s) since the top part gets undercut due to insufficient oxidation to protect the trench sidewalls. When increasing the O_t to 4 s, the feature gets less undercut beneath the mask, and the width alongside the trench decreases to 14 nm.

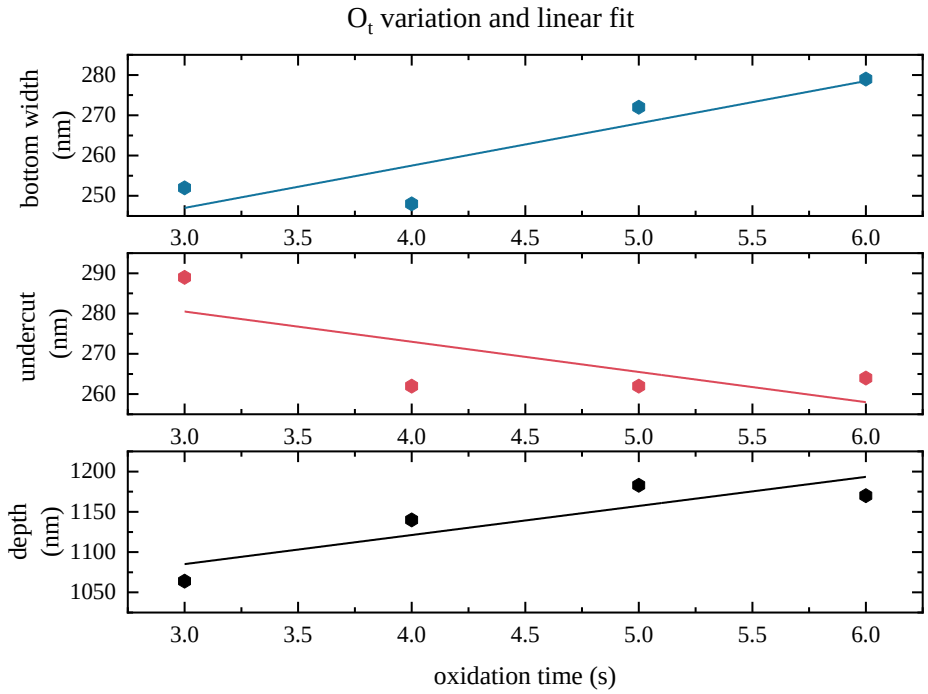

Figure 3.2- Variation of oxidation time from 3 to 6 s, of a 200 nm trench, versus the depth, undercut and width achieved.

Additionally, with 5 s, the width variation is even lower, of 10 nm. However, the bottom side of the trench increased, having a slight negative profile. At O_t = 6 s, the undercut is almost the same, but the bottom continues to get more etched, causing the profile to get more negative. Even though the bottom was getting wider with 5 s of oxidation time, it was the deeper feature from this experiment, with 1183 nm.

For additional comprehension of the O-step, three power values (0 W, 10 W and 40 W) were tested for different process times, as seen in **Figure 3.3**. In the case of 0 W, oxidation platen power was turned off, just sweeping an O_2 flow of 200 SCCM at high pressure, around 220 mTorr, for a given time interval.

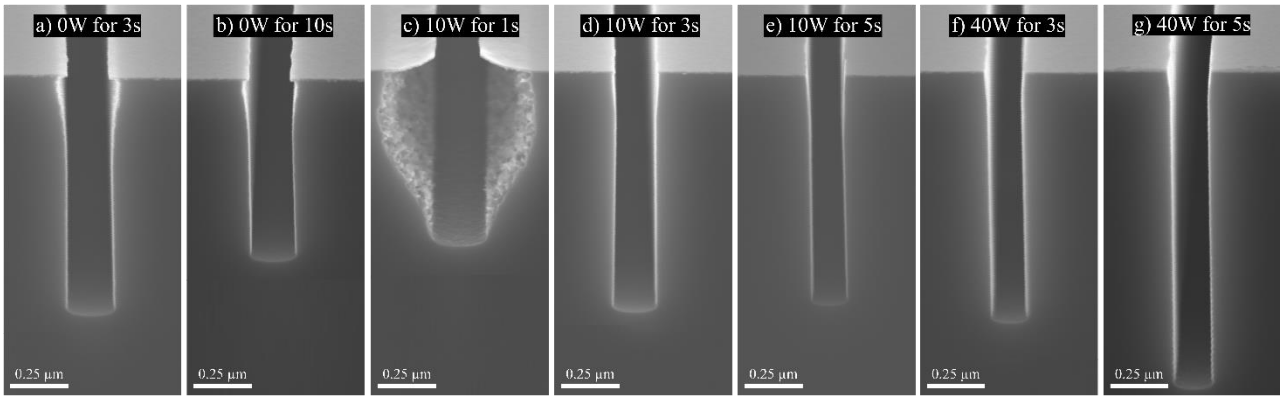

Figure 3.3- Effect on 200 nm trenches of different power values and duration of the O-step. From left to right, lengths are 1171 nm, 878 nm, 857 nm, 1167 nm, 1113 nm, 1222 nm and 1540 nm. SEM images are tilted 20°.

For the different oxidation power values, 40 W was the most promising one, giving more depth and a lesser width variation between the trench profiles, as seen in **Table 3.2**. It is important to mention that ion deflection is seen in these tests, being more aggressive where the power applied is lower. There is a big undercut beneath the mask without power applied, at 0 W, and with 10 W for 1 s. In the case of no power applied, the top part gets attacked since the oxidation is insufficient to protect the sidewall since the top part of the feature is always the one to be most exposed to the attack of incoming species. With 10 W applied, the top part has less width, not even reaching the 200 nm of the pattern, which could mean the pattern on the mask could previously be lower than 200 nm for this to happen. Furthermore, when the oxidation is performed for 3 s with 10 W and 40 W, it seems that the O-step is enough to oxygen-terminate the silicon surface entirely and withstand the following E-step since they have less width variation, being the straighter profiles [11].

Table 3.2- Different values achieved of the 200 nm trenches when varying oxidation time and power. The values of undercut and width were achieved with ImageJ.

Parameters	Depth (nm)	Etch rate (nm/s)	Undercut (nm)	Width bottom (nm)	Width variation (nm)
0W for 3s	1171	0.65	280	219	61
0W for 10s	878	0.49	243	205	38
10W for 1s	857	0.48	652	239	413
10W for 3s	1167	0.65	202	194	8
10W for 5s	1113	0.62	171	157	14
40W for 3s	1222	0.68	169	157	12
40W for 5s	1540	0.86	192	174	18

Tests regarding the R-step were performed, changing time and power. It was observed that both time and power would not influence the structure until a specific minimum value. These values were when the bottom of the feature was starting to be effectively removed, giving the requested directionality of deep microscale structures [11]. In conclusion, having the R-step with 40 W for 10 s was the best combination found, even though more powers were tested, but the profile was getting visibly positive, having a width variation of 78 nm with 234 nm at the top and 156 nm at the bottom of the profile.

Trying to get deeper trenches, the top part of the feature started to get more attacked due to the strong process parameters, even though the only power used was platen power. After unsuccessful trials of tuning the process recipe, it was understood that only with platen power was impossible to eliminate the sidewall undercut. So, instead of only using Capacitively Coupled Plasma (CCP, platen power), Inductively Coupled Plasma (ICP, coil power) was tested in the CORE process. Although coil power is not meant to help with high-density plasma, it was notorious that selectivity was improved due to the disappearance of DC bias [11].

With the development of the trench's recipe, shorter cycles were aimed, ending up with C-steps of only 1 or 2 s. As stated by Nguyen *et al.* [11], the SF_6 and O_2 fluxes are only separated after 4 s during the C-step, so shorter times than that do not execute the clearing step correctly. After testing the same recipe with only 1 s or without the C-step, it was understood it could be eliminated, showing more deepth as well as less undercut. From then on, not CORE but ORE recipes were applied (D/E = O/RE).

For ORE recipes, some parameters were optimized, but the balance between steps needed fine-tuning due to some visible unwanted DC-self bias. The bias was in the E-step (**Figure 3.4**), and it was caused by a delay of approximately 2 to 3 s between the pressure and the power in the E-step, which was the time that the Mass Flow Controller (MFC) took to measure and stabilize these values. Hence, the E-step was divided into E_1 and E_2. The E_1 step was created, with only 2 s to allow the pressure to increase along with the power increase, solving the problem. With these two etch sub-steps, the rise of bias in the E-step decreased, as shown in **Figure 3.4** (see **Table S. 1** and **Table S. 2** for more details about the two recipes).

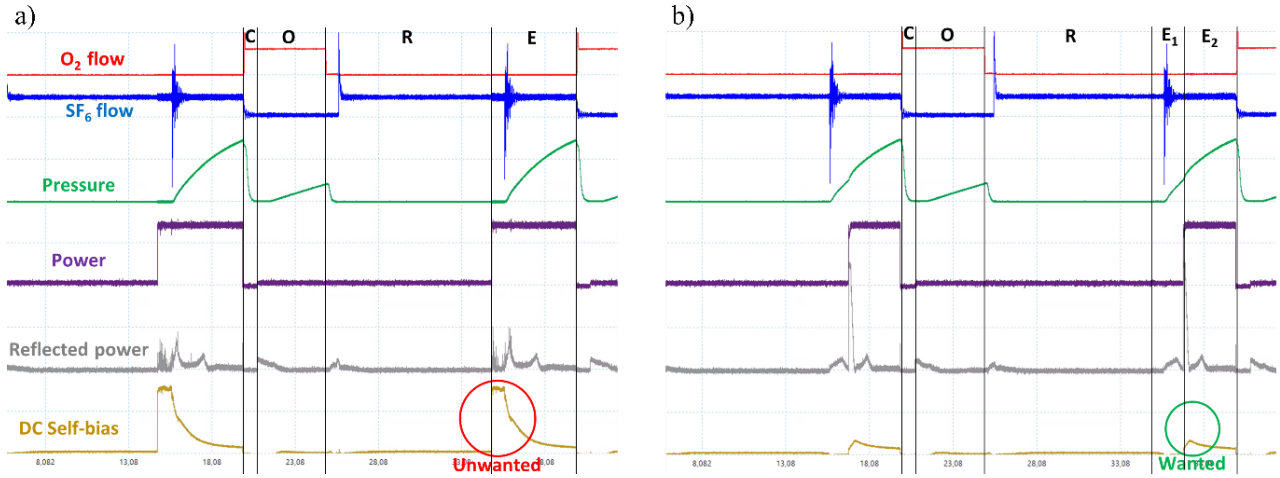

Figure 3.4- Graphics with arbitrary units of real-time signal acquisition of CORE process and its parameters taken by Pico-Scope software: a) presents an unwanted DC bias during the E-step while in b) the etch is separated into two steps and E_1 is already eliminating the unwanted DC self-bias.

Additionally, the DC self-bias is wrongly measured in Pegasus 2 since the samples are not electrostatically clamped. More importantly, the chuck is not grounded as it is, by default, an insulator to ensure the

existence of electrostatic force. With this, the wafer potential is undefined. Therefore, to correctly measure the DC bias, the substrate pins of the chuck have to be adjusted, lifting the chuck up. This way, the DC bias is measured correctly, but the CORE process runs with the chuck down, not having the correct DC bias measurement. However, the DC bias measurements from Pegasus 2 can be used to predict the ion impact quantitively. Accordingly to previous studies, the bias has an off-set of 52 V when using 10 W, decreasing linearly with the increased power, and even though the incorrect bias measured is only considered as a rough value, it is enough to know when increases and decreases, in order to minimize it whenever necessary, as shown. Other options to decrease it would be to use the coil power instead of platen power since the coil will not create a detrimental DC bias and, ideally, do it in combination with high pressure [28].

After all the experiments with trenches, the optimized etching recipes were compiled and the result is shown in **Figure 3.5** (recipes in **Table S. 3**, **Table S. 4** and **Table S. 5**, respectively). These recipes were chosen for presenting a very straight profile while going deeper. They have different depths, the first of 0.75 µm, the second of 3.26 ± 0.13 µm and the last 4.75 ± 0.08 µm. These recipes can still be adapted, either by changing the number of cycles according to the wanted depth or by changing and tuning the same parameters to achieve the profile characteristics for the wanted application.

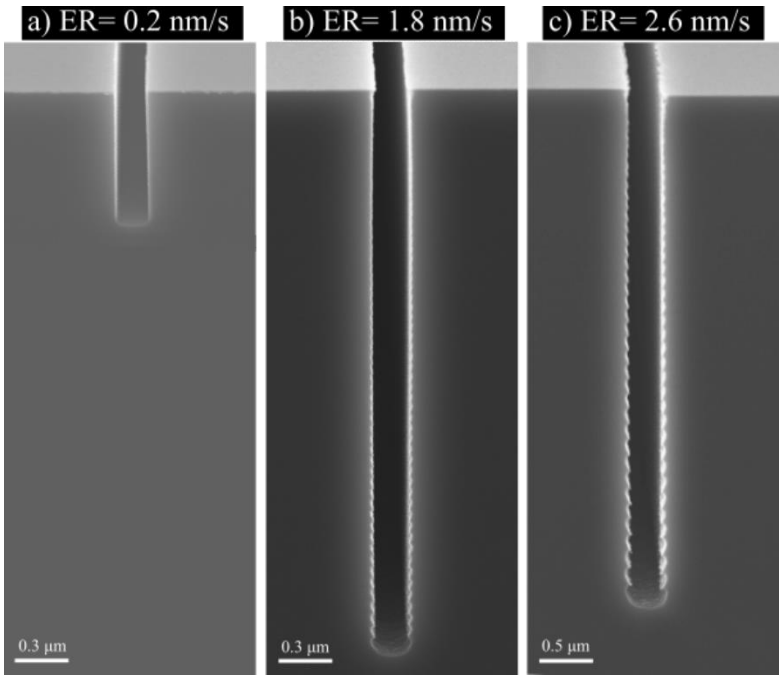

Figure 3.5- The optimazed trench recipes, differing in etch rate, from lower to higher (left to right) being 0.76 µm, 3.26 µm and 4.75 µm deep, respectively. Recipes in **Table S. 3**, **Table S. 4** and **Table S. 5**, respectively. SEM images are tilted 20°.

In a) the recipe etches for 59 minutes, equivalent to 54 cycles having an ER of 0.21 nm/s. This trench is 0.75 µm deep and the profile is straight, with a width deviation of only 10 nm (**Table 3.3**). The recipe in **Table S. 3** has valve control, which can cause some pressure oscillation, but it is not noticed here due to the slow ER, which does not present visible scallops. Also, the power used was not very high, helping with the straight profile since the steps were not aggressive toward the sidewalls.

Nonetheless, **Figure 3.5**b) and **Figure 3.5**c) already present scallops along their profiles due to more aggressive steps, having faster ER and cycles. In the fastest ER (recipe in **Table S. 5**), two parameters were ramped and the coil power was used since the profile was not behaving as wanted when trying to achieve deeper structures. As mentioned, the coil power allows for a higher selectivity, and since the platen has a

maximum of 300 W in this tool and coil power can reach 5000 W, it is beneficial to use coil, or mix it with platen power. As the trench gets deeper, the scallops get bigger, as seen between b) and c). The result was expected since the process total time is the same, but c) has fewer cycles, meaning that the E-step occurs fewer times, and if it is deeper, it means that each etch step etches more than in the b). Additionally, in **Figure 3.5**c), it is noticeable that the mask starts to have some problems in the pattern corner.

Table 3.3- Different values achieved with the 200 nm trenches presented in **Figure 3.5**. The values of undercut width and tilt were achieved with ImageJ.

Parameters	Depth (nm)	Etch rate (nm/s)	Undercut (nm)	Width bottom (nm)	Width variation (nm)
#54	750	0.21	175	185	10
#61	3260	1.80	200	195	5
#48	4750	2.64	309	305	4

With further attempts to have a deeper and straighter profile, the Cr mask started to present some abnormal behaviors. First, the mask started to curl up, possibly due to the stress and the gap between Si and Cr etch rates. The curling resulted in an attack on the top part of the trench, and it got worst with the increase in SF_6 flow and the use of coil power (**Figure 3.6**). To fight it, either the mask or the intermediate layer would have to be replaced, and the plan was to test a stack of Si + SiO_2 + Cr, though the Lesker tool was down for a few weeks, so the samples could not be produced. Alternatively, a 50 nm Al_2O_3 hard mask Si wafer was produced previously. Since Al_2O_3 is also known to be a good hard mask, samples were used for tests to check if there is an upgrade in the mask behavior. The samples used to test it were the pillars mentioned in section 2.1.2.

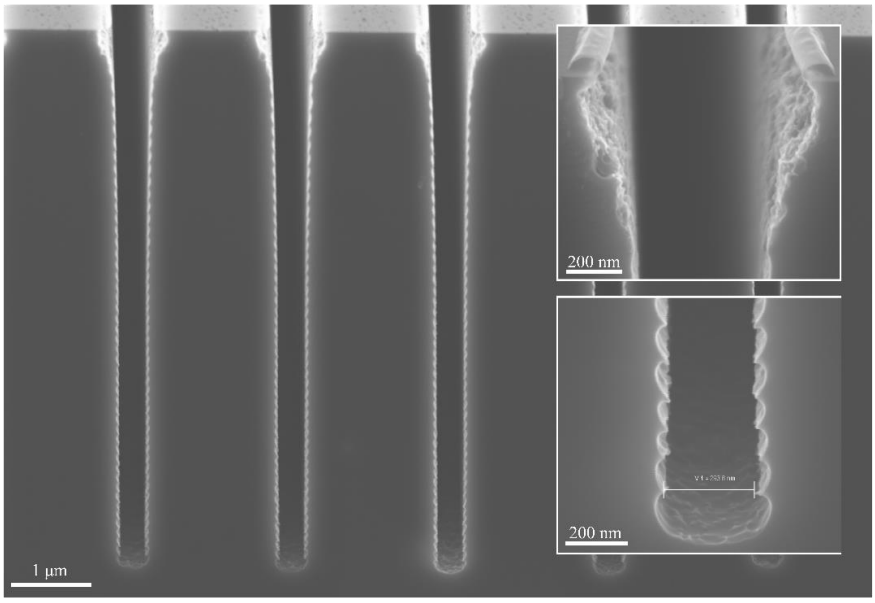

Figure 3.6- SEM image of 200 nm trenches where the Cr hard mask is visibly curled and under attack at the top. Aggressive recipe performed with 2000 W of coil power during 8 s of etching, plus 220 mTorr during oxidation and etch steps and 1200 SCCM of SF_6 during the etching. SEM images are tilted 20°.

3.1.2 Pillars

Starting with a new mask, the plan was to stress it as much as the Cr mask to see if there were advantages with this Al_2O_3 mask. For that purpose, pillars were submitted to the same recipe as one of the trenches when the mask curled up. As can be seen in **Figure 3.7**, the mask was intact and did not detach or curled as with the Cr. Besides the need for a new mask material, the pillar pattern was chosen to study an open-field feature in order to see the differences between these different patterned samples.

Moreover, a thin resist layer is visible on top of the 50 nm hard mask. To eliminate the thin resist layer, the resist strip time was increased, starting with 15 min until 45 min, and even though the layer got thinner, it was impossible to remove it altogether. However, the cause of this thin layer appearance may be due to the wafer's lifetime since it was not used right after its production.

When working with 1 µm pillars instead of 200 nm trenches, it is important to remember that there is no need to compensate for RIE lag since it is an open-field structure, as mentioned, and the AR is not very high, so ramping is switched off.

The major parameter tested was the E-time, from 6 to 10 s, to understand how that directly impacts the feature (**Figure 3.8**). Starting with 6 s, the feature was particularly good, presenting a negative etch profile with 3.82 µm deep and a width variation of 205 nm, presented in **Table 3.4**. With 7 s of etching, the same happened, and as expected, being more negative, reaching 7.90 µm. However, after 8 s, the top part starts to get under attack and the etch profile becomes positive, presenting a width variation of 290 nm. More tests were done with 10 and 15 s, but the profile became increasingly attacked until the top part fell. This presents a direct result of the higher fluorine pressure, which thins the pillars and erodes the passivation layer, as seen in **Figure 3.8**d). Consequently, during SEM, the thin pillars (AR ≈ 45 in d)) tend to collapse and stick together. This collapse can be avoided by scanning the electron beam parallel to the pillar profile rather than perpendicular. Therefore, increasing E_t is only beneficial until 6 or 7 s for this recipe in particular [2].

Knowing that 8 s was too much for the top part but was suitable for the bottom, a new recipe was designed, presented in **Table S. 6**. This recipe enables straight pillars, with approximately 8 µm depth, with reasonable undercutting at the top.

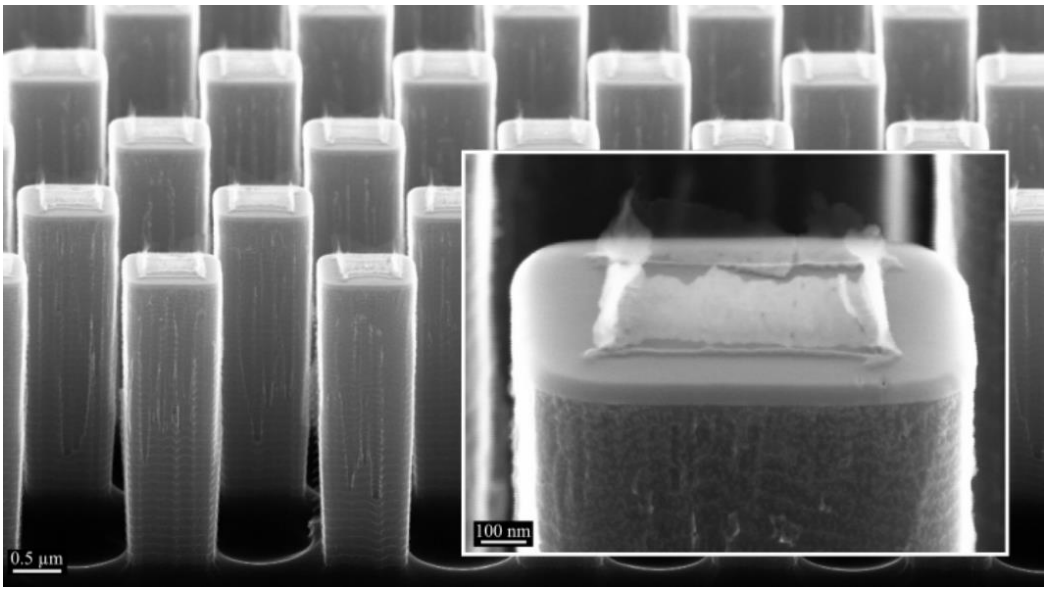

Figure 3.7- SEM image of 1 µm pillars showing good response from Al_2O_3 mask, with a depth of 3.35 µm. SEM images are tilted 20°.

Table 3.4- Different values achieved with the 1 µm pillars presented in **Figure 3.8**. The values of top and bottom width were achieved with ImageJ.

Etch time (s)	Depth (µm)	Width top (nm)	Width bottom (nm)	Width variation (nm)
6	3.82	981	776	205
7	7.90	908	677	231
8	15.03	894	1184	290
10	18.00	836*	1051	215

*counting with the aggressive undercut at the top part, the width is 434 nm

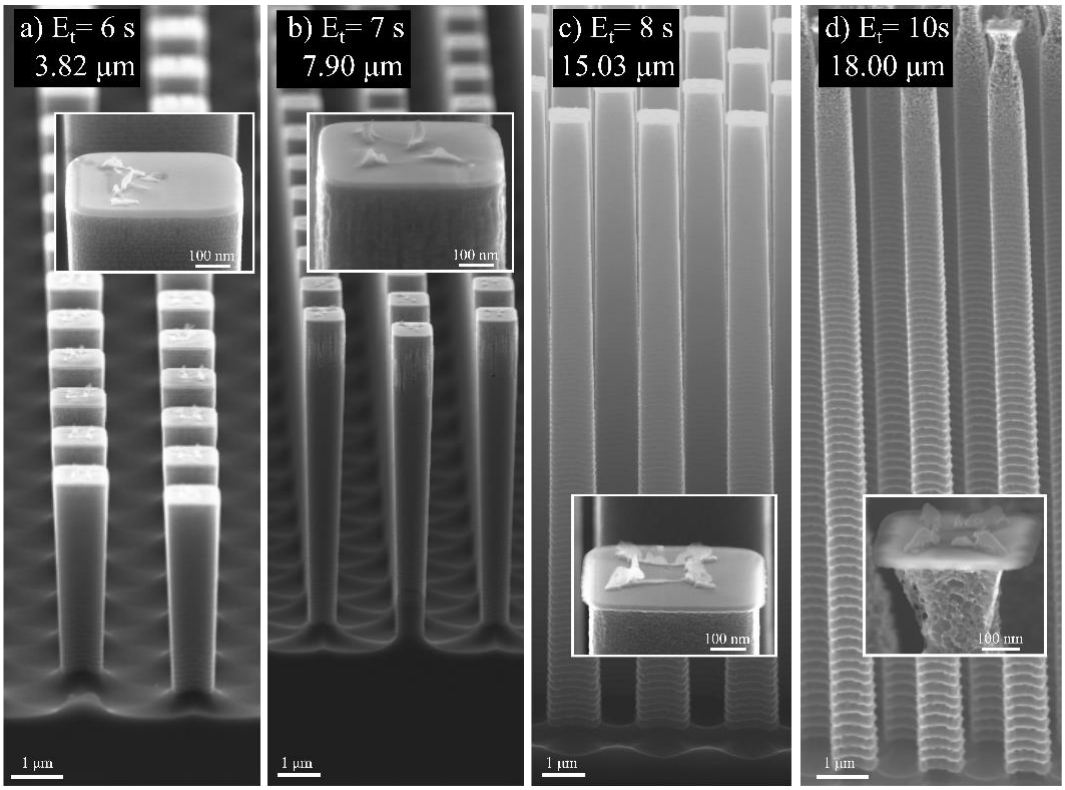

Figure 3.8- SEM image of 1 µm pillars, with different etch times: a) 6 s, b) 7 s, c) 8 s and d) 10 s. The profile gets straighter from 6 to 7 s, but more than 7 s starts to cause damage to the pillar top part, undercutting below the Al_2O_3 hard mask. SEM images are tilted 20°.

3.1.3 Holes

Considering that open-field structures were studied, 1 µm holes were another set of experiments to research closed-field structures and the recipe's main differences. As shown above, the Al_2O_3 hard mask was also capable of withstanding aggressive recipes, revealing a reliable performance in both cases. Regarding the 1 µm holes, more ramping will be needed compared with the pillars, but to start with, some pillar recipes were adapted in that sense. Starting with ramping the etch time, the starting time value was studied. The alternative was to start either without any time or with 1 or 2 s. Looking at **Figure 3.9**a) and **Figure 3.9**b) and comparing them with the values in **Table 3.5**, it is visible that starting with 1 s of etching when ramping makes the structures deeper, which is expected since it has more time to etch into the silicon.

Moreover, the top part suffers more undercut with 1 to 8 s of E-time, of almost 500 nm, and with 0-8 s, the undercut is less than half compared to the latter (229 nm). This result demonstrates that the recipe does not handle starting the ramping in 1 s. Starting with 1 s implies etch right in the beginning, so it gets deeper faster, and due to that, the passivation layer in the top part is compromised sooner. To handle 1-8 s of E-time, the remove and oxidation steps would have to be optimized in this direction. That can be proven since **Figure 3.9**c) has the same recipe and number of cycles performed as the others (recipe in **Table S. 7**), but the etch time is ramping from 1-5 s. With less total etch time, it enables the oxidation step to keep up with the etch step, not damaging the sidewalls, eliminating the undesired undercut.

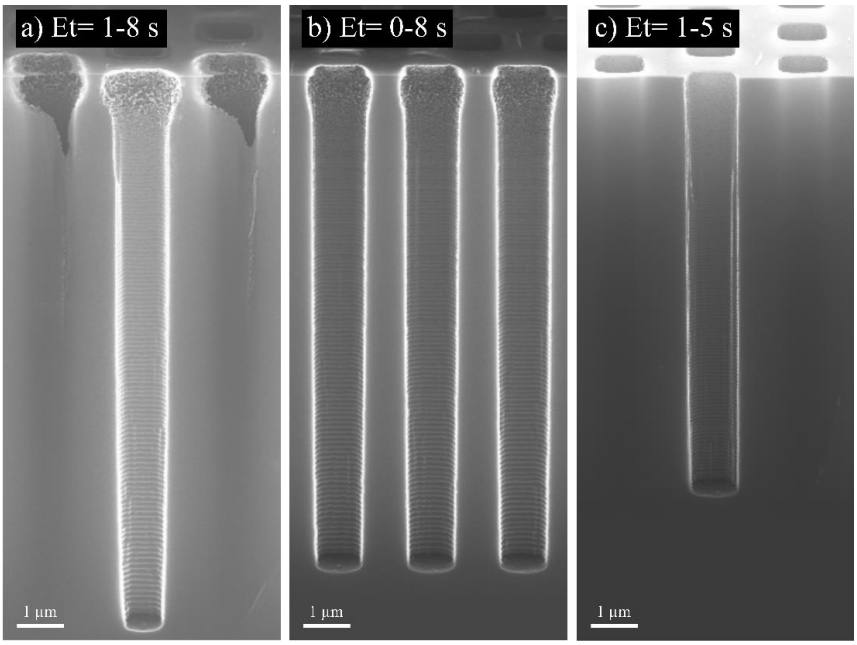

Figure 3.9- Effect of different ramping intervals on the etch time. In a) with 1-8s ramping, 136 cycles lasting 60 min and reached 12.96 µm, b) with 0-8s ramping, 139 cycles lasting 60 min and reached 11,99 µm and c) with 1-5s ramping, 144 cycles lasting for 60 min and reached 10.18 µm. The recipe is presented in **Table S. 7**. SEM images are tilted 20°.

Table 3.5- Different values achieved with the 1 µm holes presented in **Figure 3.9**. The values of top and bottom width were achieved with ImageJ. The recipe is presented in **Table S. 7**.

Etch time (s)	Depth (µm)	Undercut (nm)	Width top (nm)	Width bottom (nm)	Width variation (nm)
1-8	12.96	495	1243	914	329
0-8	11.99	229	1223	1038	185
1-5	10.18	-	1168	1072	96

In order to maximize the etch rate, regarding the E-step SF_6 flow, the following relation between platen power, pressure and SF_6 flow is followed: the flow is set at 0.2 SCCM/W and the pressure is set at 0.15 mTorr/SCCM [2], [29]. Applying it to 400 SCCM, it would be necessary 2000 W platen power and 60 mTorr. Since in Pegasus 2, the maximum value for platen is 300 W, as already mentioned above, the coil power had to be turned on to reach the maximum etch rate and not go under a power-limited regime. If not, the maximum flow for the 300 W platen would have to be 60 SCCM. In **Figure 3.10**, 400 and 1200 SCCM flows are tested (full recipe in **Table S. 8**), wherein a) the structure presents a very straight profile, measuring 1055 nm at the top and 1020 nm at the bottom, presenting a width variation of 35 nm while reaching a 6.54 µm depth. This

feature shows that SF_6 flow could be increased if well-tuned, optimizing other parameters to better protect the sidewall. The same recipe was maintained just by changing the SF_6 flow to 1200 SCCM, and even though the top part starts to get undercut, the rest of the feature still presents a slight straight profile due to the depth achieved. The top width reached 1202 nm and the bottom 1038 nm, showing a width variation of 164 nm while reaching an 11.50 µm depth. As mentioned, by fine-tuning the recipe for 1200 SCCM, the feature would become straighter by better protecting the passivation layer through optimisation of the O-step and, consequently, the R-step.

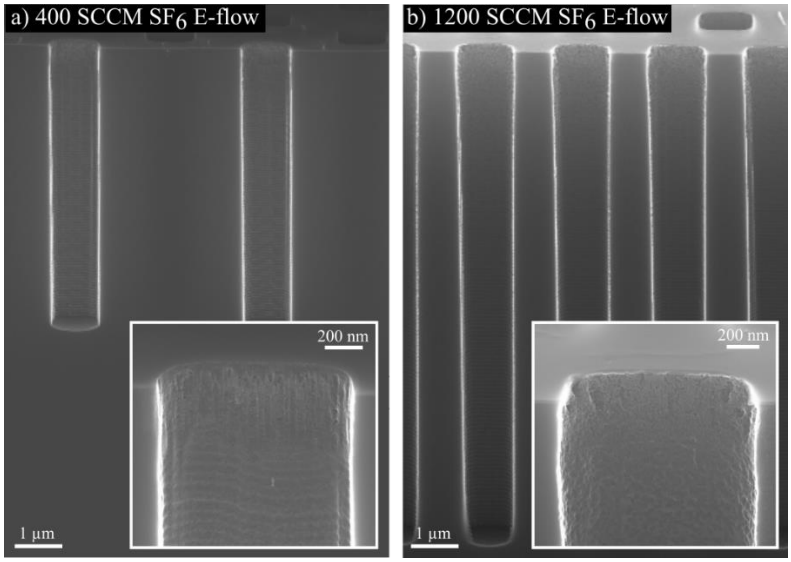

Figure 3.10- Effect of different SF_6 flow during etch step. In a) with 400 SCCM, 144 cycles and 60 min reached 6.54 µm and b) with 1200 SCCM, 144 cycles and 60 min reached 11.50 µm. Notice that in b), the bottom part is not well cleaved, thus, the impression of a positive profile while in reality is much straighter than positive. The recipe is presented in **Table S. 8**. SEM images are tilted 20°.

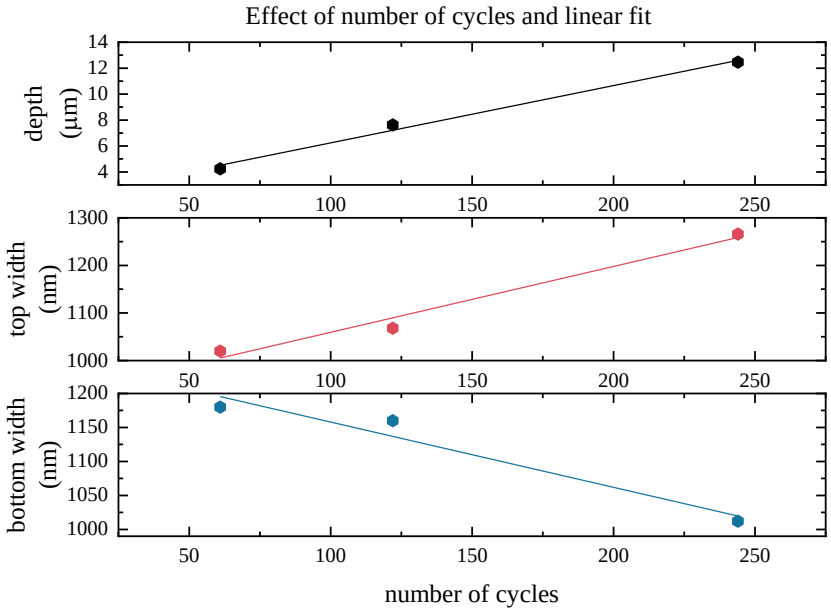

Figure 3.11- Effect of increasing the total number of cycles, from 61 to 244 on a 1 µm hole, versus the depth, and top and bottom width achieved. Images are presented in **Figure 3.12** and recipe in **Table 3.6.**

Additionally, the total number of cycles was increased using the same recipe to understand how the profile evolves. In **Figure 3.12**, the recipe (**Table 3.8**) was tested with 61, 122 and 244 cycles. The etch rates obtained were 2.36 nm/s, 2.12 nm/s and 1.73 nm/s, respectively. It is visible in **Figure 3.12** that the top part gets under attack with the continuous exposition of the fluorine radicals that etch the oxide layer away. With the increase in total time, the effect of RIE lag/ARDE is also visible, which is worst with 244 cycles as expected because the AR increased [30], [31].

Comparing the profiles in **Figure 3.12**, for 61 cycles, the profile gets negative as it has a width variation of 160 nm, even though it seems more negative than reality due to the cleavage of the sample. For 122 cycles, it continues to present a negative etch profile, with a width variation of 92 nm. However, with 244 cycles, the sidewalls start to be destroyed due to the ion deflection, and eventhough it appear to have a positive etch profile, it still is negative, however the top part was destroyed. This profile type change is due to the RIE lag mentioned above since the AR increased to 12:1.

Important to notice that the recipes used with the 1 µm hole are already out of the CORE design rules since the design rules, mainly the first one, do not apply as it only covers oxidation times until 8 s, and these recipes are built for 10 s in order to work [11]. Even though these are new recipes where the oxidation time does not behave linearly with the etch step, they present an outstanding result.

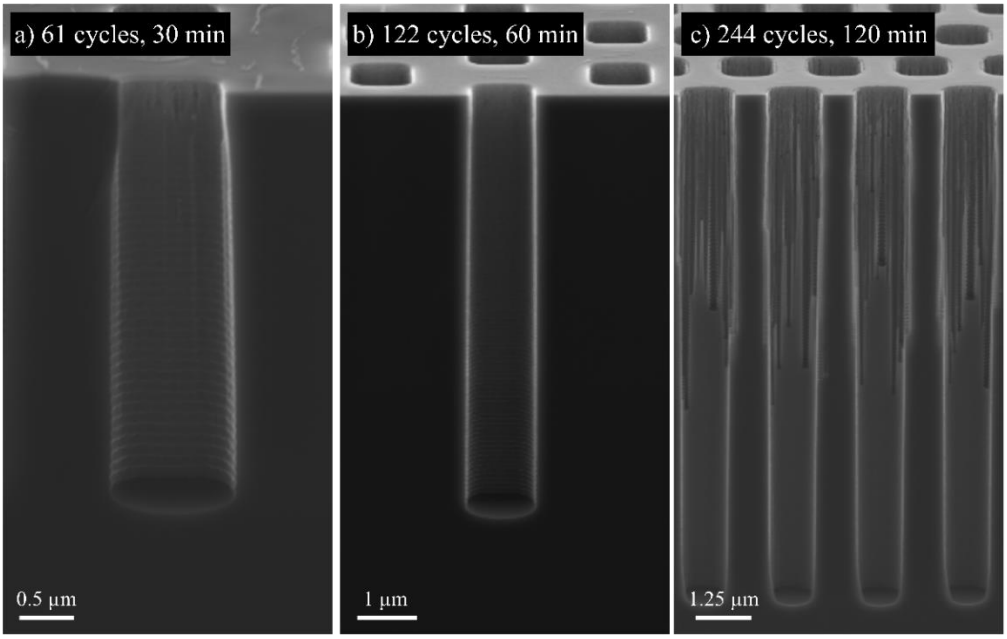

Figure 3.12- Effect of increasing the number of cycles in the process. In a) with 61 cycles (30 min) the features reached 4.24 µm. In b) with 122 cycles (60 min), it reached 7.63 µm, and in c) with 244 cycles (120 min), it reached 12.46 µm. The recipe is presented in **Table 3.7.** SEM images are tilted 20°.

Table 3.8- ORE recipe used in **Figure 3.12**, where the number of cycles was increased from 61 to 122 and then to 244.

	Time (s)	**Pressure**	**O_2 flow (SCCM)**	**SF_6 flow (SCCM)**	**Platen power (W)**
O-step	10	3%	200	0	40
R-step	10	100%	0	5	40
E_1-step	2	4%	0	350	40
E_2-step	0-15	4%	0	350	300

3.2 Nanoscale ORE etching

To continue to study the CORE process, new samples were tested using only ORE cycles. The 200 nm nanoholes with 400 nm pitch were produced to study the behavior of the process at the nanoscale. Since this process aims at nanoscale accuracy, it is beneficial for innumerous applications in the semiconductor industry.

3.2.1 Nanoholes

When searching for accuracy and precision, nanoholes were vastly tested to check, among other things, the reproducibility, the loading effect, the continuous isotropic etch and the RIE lag of HAR features. To start with, the power of the removal step was analyzed (**Figure 3.13**, recipe in **Table S. 9**), going from 20 to 60 W. For the initial value, it was clear that more power was needed since the removal step is responsible for the directionality of the process, as mentioned. So, if there is very low power, the bias is not high enough to sharpen the ion angular distribution (IAD) as it should, not having enough ions reaching the bottom and etching the passivation layer [2].

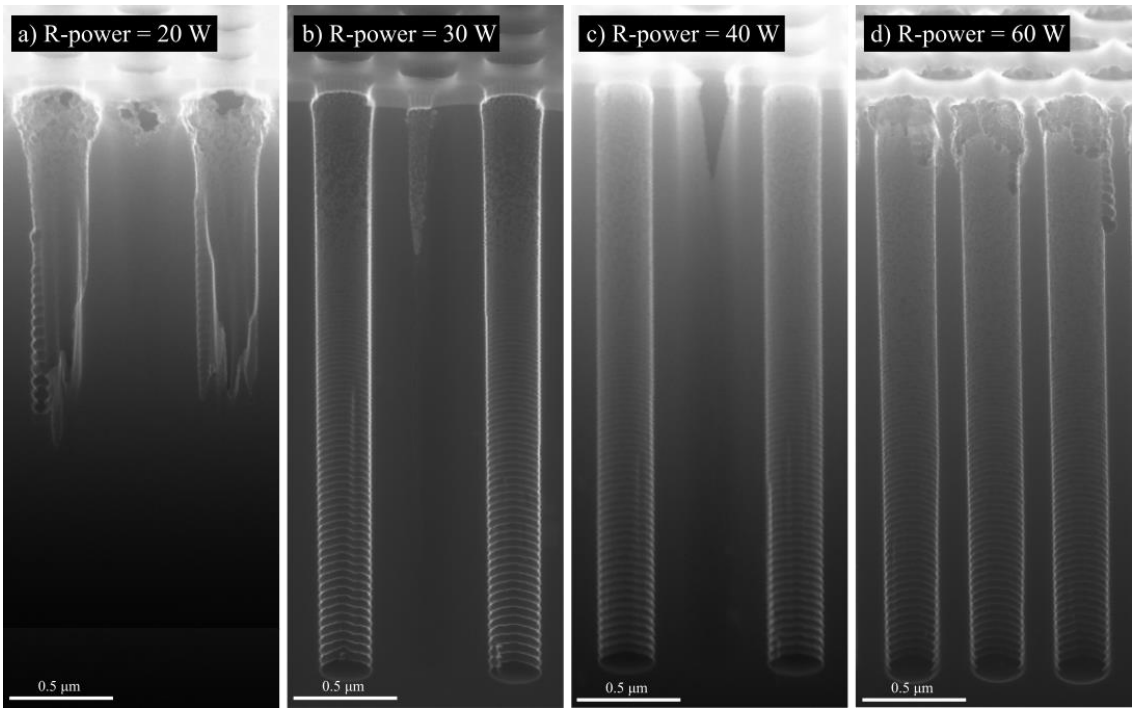

Figure 3.13- Effect of R-power on 200 nm nanoholes, ranging from 20W to 60W. In a) with 20W of R-power, the features reached 2.12 µm. In b) with 30W of R-power, it reached 2.84 µm. In c) with 40W of R-power, it reached 2.91 µm and in d) with 60W of R-power reached 2.79 µm. The recipe used is presented in **Table S. 9**. SEM images are tilted 20°.

For 30 W, the profile starts to get closer to straight, but it still is slightly positive, visible at the top part of the nanoholes, but it changes when it reaches 40 W. As with the 1 µm holes, the more suitable power for the 200 nm nanoholes is also 40 W for 10 s, achieving an effective removal of the bottom oxide layer. However, when it goes for 60 W, it is notorious that is already too much power, removing the passivation layer where it should not, harming the top part of the structure.

3.2.1 Bottles shape features

In order to evaluate 3D features, a few tests were completed. To begin with, an inverted bottle shape feature was the first step to go for a straight bottle shape feature. Even though going for not inverted was known to be very hard to say impossible with a nanoholes pattern, some attempts were performed, but unfortunately, they were not achieved. However, for the inverted shape, some tests were successful. In **Figure 3.14**, the first two SEM images show the attempts, and the recipes are presented in **Table S. 10** and **Table S. 11**. The recipes were divided into three steps: the larger tube, the positive cone, and the smaller tube. For c), the steps in the recipe were inverted (**Table S. 12**) to see how the profile would turn out.

The only difference between a) and b) is the oxidation time in the first tube, which in b) is higher, originating a decrease of 100 nm in depth when compared to a). The result is expected since just by increasing the oxidation time, the sidewalls as well as the bottom of the feature, are better protected with this passivation layer [2]. Having a more significant passivation layer will be harder or at least slower for the removal step to act as effectively as it would with probably less 0.5 nm passivation. One possibility is that the layer did not increased conformingly to the doubling in oxidation time since this step is self-terminated, as mentioned above [2], [32], [33].

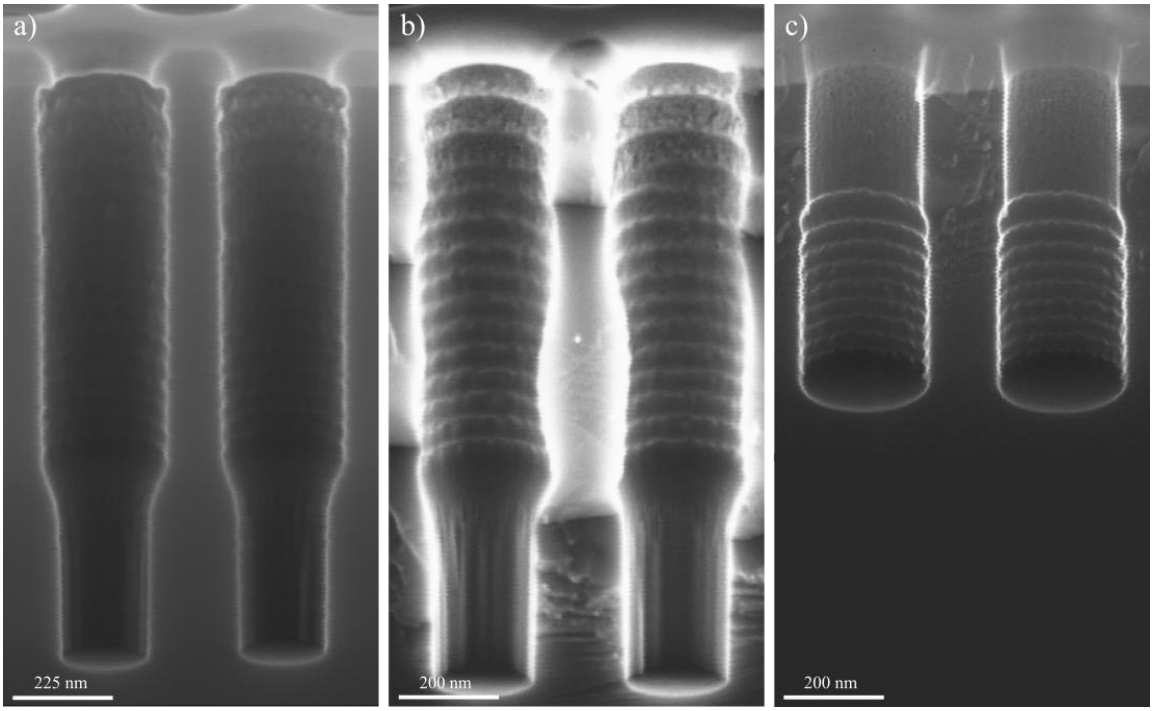

Figure 3.14- SEM images showing features with the shape of bottles with three steps inside the designed CORE recipe. In a) the features reached 1372 µm. In b) it reached 1266 µm and in c) 639 µm. The recipes used are presented in **Table S. 10**, **Table S. 11** and **Table S. 12**, respectively. SEM images are tilted 20°.

3.2.2 Center Point Run + isotropic etch

A few recipes were optimized with the 200 nm nanoholes to act as main and versatile recipes in the tool, calling them Center Point Runs (CPR). After a few tries, the E-time was adapted for a ramping from 0 to 15 s having the CPR I, but to better understand the effect of ramping, it was tested with 1 to 15 s, with 5 to 15 s and with only 15 s, without ramping (recipe presented in **Table 3.9**). In **Figure 3.15**, the profile of the four experiments mentioned is presented, and it is clear that all profiles are almost totally straight, considering that the

top part is slightly eroded in all. The depth achieved in each case is the main difference. The profiles reached 3.17 µm, 3.21 µm, 2.87 µm and 3.67 µm from a) to d), respectively. Comparing the results to what was expected, it is visible in **Figure 3.15**c) that there is an inconsistency since it should be deeper than the previous one (E_t=1-15s) since it has more total etch time. This inconsistency can be related to two different possibilities:

First, changing from valve control to pressure control was necessary as Pegasus 2 valve started to give some software alerts. In order to be a smooth transition, some tests were done to understand if changing to pressure control would help. In fact, it helped since the pressure was more accurate, enabling the process to be more efficient. Furthermore, some limits were drawn regarding the tool pressure. The maximum value in pressure control mode should be 220 mTorr, and valve control should only be used when it is totally open, meaning 100 %. However, this particular recipe has a 100% valve position during the R-step, and the valve, as mentioned, was having some troubleshooting. Initially, it was thought that it was only influencing the steps with high pressure where the throttle valve was almost closed (valve position below 4%). Nevertheless, it has been seen that low pressures, meaning 100% valve position, also raised problems. The plasma becomes very unstable, most probably caused by a massive chamber clean-up.

Secondly, the major clean-up of the chamber may have contributed to the problems raised. This service was done to Pegasus 2 because the tool was down with some high reflected power problems, with some parameters peaking, causing the processes to be stopped. For instance, the SF_6 flow set at 40 SCCM would reach 320 SCCM. The same happened with the power and pressure parameters a few times. Regarding why the clean-up affected the plasma, it is known that the reactor wall is a substantial part of the plasma discharge and, as such, will affect the plasma parameters. A clean surface implies that a new conducting surface is facing the discharge, indicating that electrons and ions will easily leak away, destabilizing the discharge. At low pressure (100% APC valve position, around 0.1 mTorr), most avalanche electrons are created at the discharge boundary, so this behavior is lethal. It is less problematic at higher pressures (below 4% valve position, around 220 mTorr) because the avalanche electrons are created in the plasma bulk, far away from the conducting surfaces. If instead, the wall was insulating, the charge arriving from the plasma glow would not leak away as it is with the dielectric. The latter insulating property, which forms with processing time, is perceived as contaminated, but it can be advantageous under certain circumstances.

Given that Pegasus 2 never performed Bosch processes, not having any FC history, and being free of FC pile-up, the formation of layers in the sidewalls is different. The oxide layer formation is self-limited due to the oxidation step stopping at a few nm, not being able to form a thick insulating layer at the sidewalls. Even though it can appear to be contaminated, it improves the discharge ability of the process. To put the chamber close to the previous conditions, the tool must go under a determinated process with a carrier wafer inside.

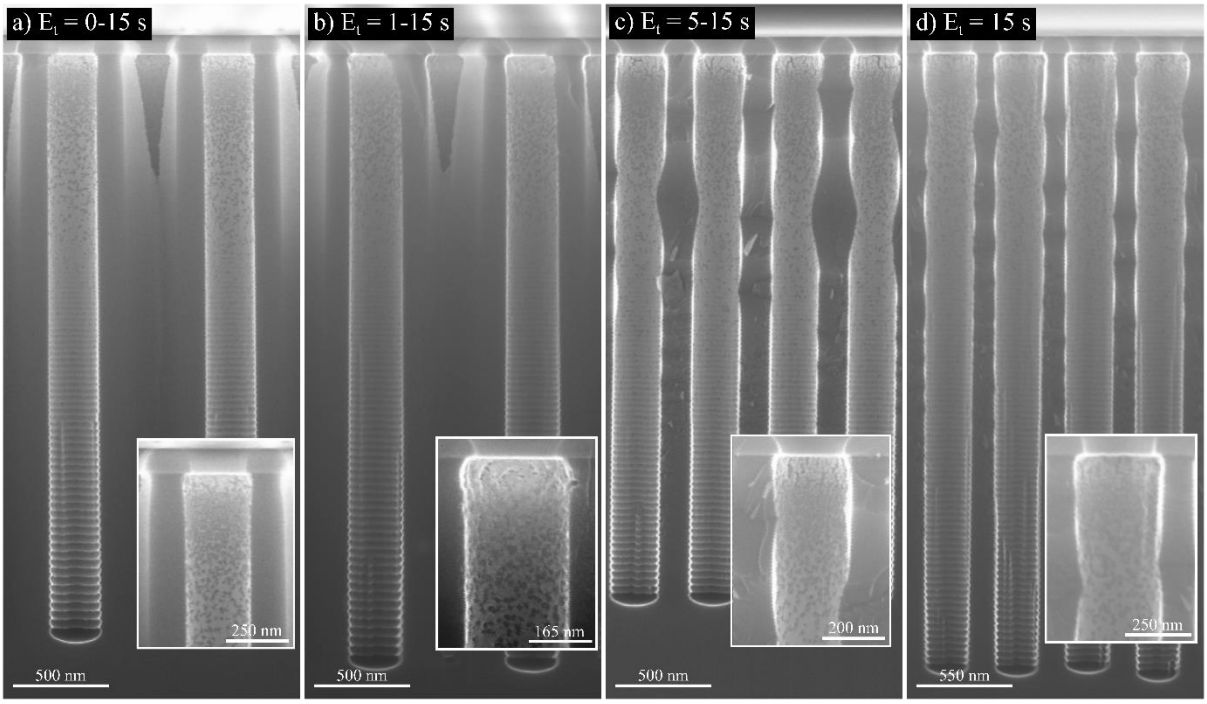

Figure 3.15- SEM images showing the effect of ramping and not ramping the etch time with 200 nm nanoholes, where a) reached 3.17 µm with 0-15 s of ramping, b) reached 3.21 µm with 1-15 s of ramping, c) reached 2.87 µm whit 5-15s of ramping and d) reached 3.63 µm with 15 s without ramping. The generic recipe is presented in **Table 3.9**. SEM images are not tilted.

Table 3.9- ORE recipe of images presented in **Figure 3.15**, where the E-time is the only parameter changed, explaining why not presented here. The number of cycles was 122 for the four samples, and the total time changed between them due to the change in E-time.

#122	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
O-step	10	220 mTorr	200	0	40
R-step	10	100%	0	40	40
E_1-step	2	220 mTorr	0	350	40
E_2-step	-	220 mTorr	0	350	300

Continuing with the tests, in order to achieve deeper features, the number of cycles was increased from 122, presented in **Figure 3.15**, to 182, and the result was closer to what was expected. For a etch time of 1-15 s, it reached 3,61 µm. For 5-15 s, it reached 4.45 µm, and for a total of 15 s of etch time, it reached 5.62 µm. All the etch profiles were positive, with undercut at the top, differing from top to bottom of 55 nm, 95 nm and 140 nm, respectively. Despite the fact that 15 s of E-time may seem appealing, going for deeper structures without ramping the etch time would kill the top part of the profile. Even if the other parameters were adjusted to it, it would continue to undercut the top part, becoming positive. To save it, the whole recipe would have to be rebuilt to allow deeper structures without the help of ramping in E-time. After knowing this, tests were continued with just two ramping times, with 1-15 s and 5-15 s.

In **Figure 3.16**i), with E-time ramping from 5-15 s, the straighter profile is achieved with 82 cycles (#80), with a width variation of only 8 nm. For 123 cycles, the profile achieved a low variation of 16 nm. The change from negative to positive profile happens in the middle of these two profiles, between 2.46 µm and 3.32 µm. Before that, the profile is negative, and with more total time, it starts to get positive due to RIE lag.

To overcome it, different approaches can be taken. If for the 163 cycles, the oxidation time or power is slightly increased, it can benefit the top part. Nevertheless, it is a complicated equilibrium that must be tested until the profile becomes straight. For the 204 cycles, even if the parameters of the oxidation power were adjusted, it would become challenging not to erode the top part as the cycles are relatively fast. If the etch rate was slower it would help, having a more accurate profile, and process in general. In addition, as mentioned, the samples can be oxidized in the RTP to get better passivation, so it can be a possibility to etch until the profile gets straight, do the thermal oxidation in RTP and then continue the etching, but this will undoubtedly raise different problems.

The same is observed when ramping E-time from 1 to 15s (**Figure 3.16**.ii). The straighter profiles are also the 80 and 120 cycles, with a width variation of 15 nm and 18 nm, respectively. The transition from negative profile to positive also occurs between them, 2.34 µm to 2.89 µm. Moreover, for 205 cycles, the profile suffers a bigger undercut, as well as in e.i), but comparing the width variation in e.i) and e.ii), the latter is bigger, of 136 nm, even though the feature in e.i) is deeper than this one (width variation of 104 nm).

Observing **Figure 3.17**, the evolution of the etch rate is notorious, starting with the 1-15 s having a higher ER, but the 5-15 s surpassed and has an average ER of 0.88 nm/s while the other is 0.02 nm/s slower in average.

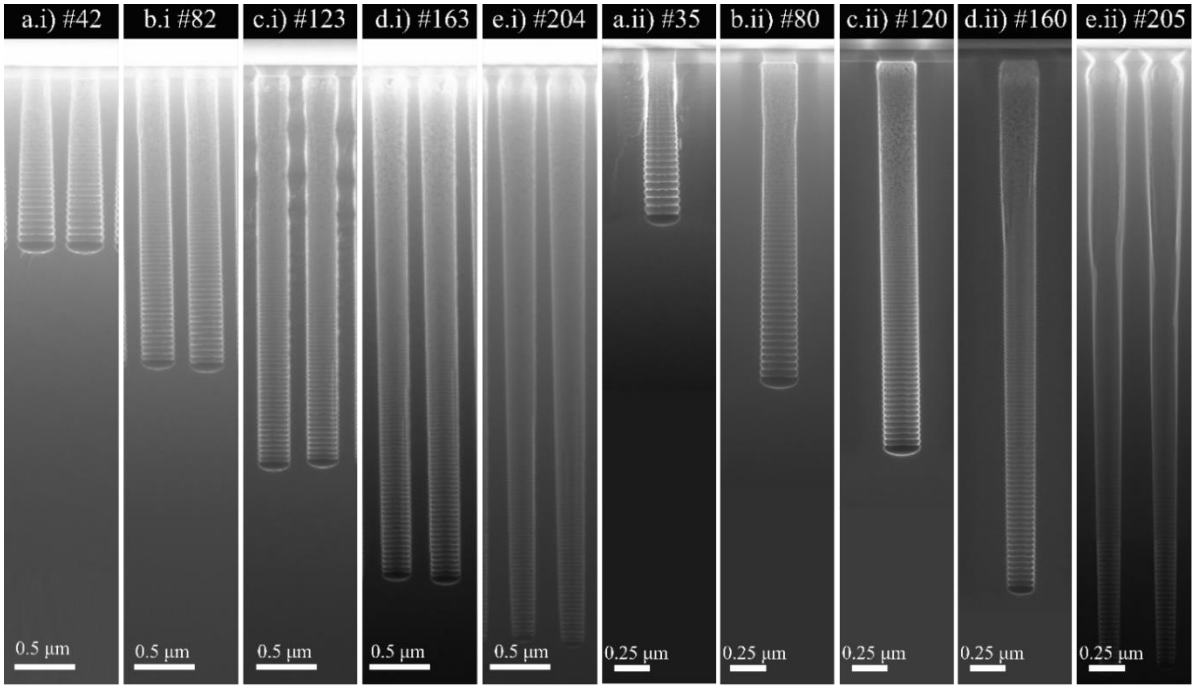

Figure 3.16- Effect of increasing the number of cycles on 200 nm nanoholes. The recipe used is presented in **Table 3.9**, having E-time ramping from 5 to 15s in i) and 1 to 15s in ii). For a.i) with 22 min reached 1.45 µm, b.i) 43 min reached 2.46 µm, c.i) 65 min reached 3.32 µm, d.i) with 87 min reached 4.27 µm and e.i) with 109 min reached 4.85 µm. For a.ii) 17 min reached 1.17 µm, b.ii) 40 min and reached 2.34 µm, c.ii) 60 min reached 2.89 µm, d.ii) 80 min reached 3.70 µm and e.ii) with 102 min reached 4.39 µm. SEM images are not tilted.

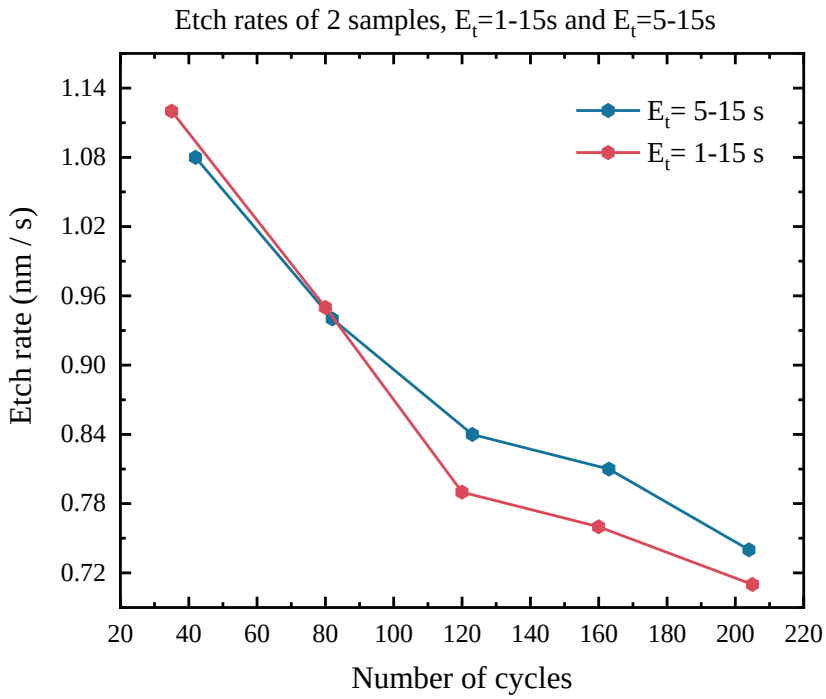

Figure 3.17- Plot from the features presented in **Figure 3.16**, with the number of cycles vs depth for both ramping etch times of 1 to 15 s and 5 to 15 s. The full recipe is presented in **Table 3.9**.

Important to notice another abnormality during the experiments with nanoholes and not just these last tests. As can be seen in d.i), b.ii) and d.ii), the features are tilted with respect to the normal of the wafer surface, roughly 3°. First, it was thought that it would be due to the carrier wafer being re-used for some processes having a residual history between the wafer and the sample. Still, even with new carrier wafers, the profile sometimes would get tilted. Moreover, this can happen due to the plasma sheath not being formed completely parallel to the sample's surface or even if the mask profile is not vertical to the wafer. Therefore, to decrease the tilting, it is crucial to make sure that the plasma sheath has a uniform thickness, and this can be modulated through the plasma density, as they are inversely proportional [31], [34], [35].

Another issue was the loading effect which seemed to get more emphasized over time, probably with the influence of the problems that appeared in the tool. When processing samples in Pegasus 2, it was generally just 1 sample at a time, so the loading effect was not very visible, as the samples were 1 cm x 1 cm. Nevertheless, there were times when some samples would be processed in one run, and when that happened, all the samples would have to be checked. For example, if three lines of three samples were processed in one go, the samples there were more outside would be more influenced by the loading effect, as the etch rate varies accordingly to different pattern densities [15], [30]. Besides, within a sample, the loading effect could be visible very close to the corners, where the pattern density was different as the pattern would end there, and it would just be bulk silicon on the side. Moreover, since the primary source of the loading effect is the reactant depletion and with the decrease of pressure, the consumption of reactants has less effect. By having a lower pressure of the process, it is reported that the loading effect will decrease as a consequence [36].

Furthermore, oxidation and isotropic etch were also tested in Pegasus 2 with the recipe in **Table S. 9** and 40 W of power. The experiments will determine if it is beneficial to create the passivation layer in the RTP to withstand an isotropic etch at the end of the nanoholes structures or if it is enough to oxidate the samples in Pegasus 2. To compare both oxidation processes, the oxidation was processed in both tools after both samples were isotropically etched in Pegasus 2 (**Figure S. 8**). In Pegasus 2, the plasma oxidation was done for 1800 s,

200 SCCM of O_2 and 2000 W of coil power. In RTP, the oxidation was for 2400 s, using 12 mbar, 1500 SCCM O_2 and 1200 SCCM of Ar. The oxide thickness of both was checked on the ellipsometer VASE, and for Pegasus 2, the oxide growth was 3.2 nm, while for the RTP was 19.2 nm. The difference between both oxide growth techniques is major; in Pegasus 2, the oxide growth rate was 1.07 nm/min, and the RTP was 4.8 nm/min, so an interrupted process flow may be promising. Instead of doing a single-run in Pegasus 2, after the directional etch, the samples can go for oxidation in RTP if the structure needs more sidewall protection and then go again into Pegasus 2 to do the desired isotropic etch. As for the latter, after different recipes, the one presented in **Table 3.10** was the best found so far for the purpose. Important to note that the recipe was better for this structure in particular. For different structures, the time or power has to be adapted to help with the desired profile.

Table 3.10- Recipe for the isotropic etch used with 200 nm nanoholes with 400 nm pitch in Pegasus 2. The power used is only coil, having 2000 W during the oxidation and the etch. In the removal step, only platen power is used.

	Time (s)	**Pressure**	**O_2 flow (SCCM)**	**SF_6 flow (SCCM)**	**Platen power (W)**	**Coil power (W)**
O-step	30	200 mTorr	200	0	0	2000
R-step	30	100%	0	40	40	0
E-step	20	200 mTorr	0	1200	0	2000

3.2.3 Rapid Thermal Annealing

To study the effect of the etch profile in the formation of buried cavities, the features were tested in Pegasus 2 and then annealed in the RTP. The two features used were very similar, composed of an anisotropic etch followed by an isotropic etch, presented in **Figure 3.18** a.i) and b.i).

In the annealing, the recipe "RTA 1250 HP HF MAX" was used (mentioned in section 2.3 and presented in **Table S. 13**), as it was the most effective one, with already some interesting results. However, there was a problem with the sample setup in the tool. Due to a malfunction or wrong setup of the tool, when the sample would be in the chamber, it would fall as the support pins for the carrier wafer sometimes would jump off, leaving the wafer unbalanced, causing the sample to fall in the chamber. Moreover, when this problem was minimized by inserting a soft-start valve, which would help by making the pressure changes less abrupt, another problem happened, the upper quartz window broke, thus no more experiments were done.

Further, SEM was not optimal for the buried cavities characterization. To prepare the sample for characterization, the sample is cleaved in half to see the sample's cross-section. By breaking it in half, the tension during cleaving increases as the sample is only supported by the corners, as below a buried cavity is formed. Therefore, other characterization techniques were studied to try to investigate the buried cavity without breaking it. However, since the RTP tool was down, it was not possible to execute new techniques to analyze them.

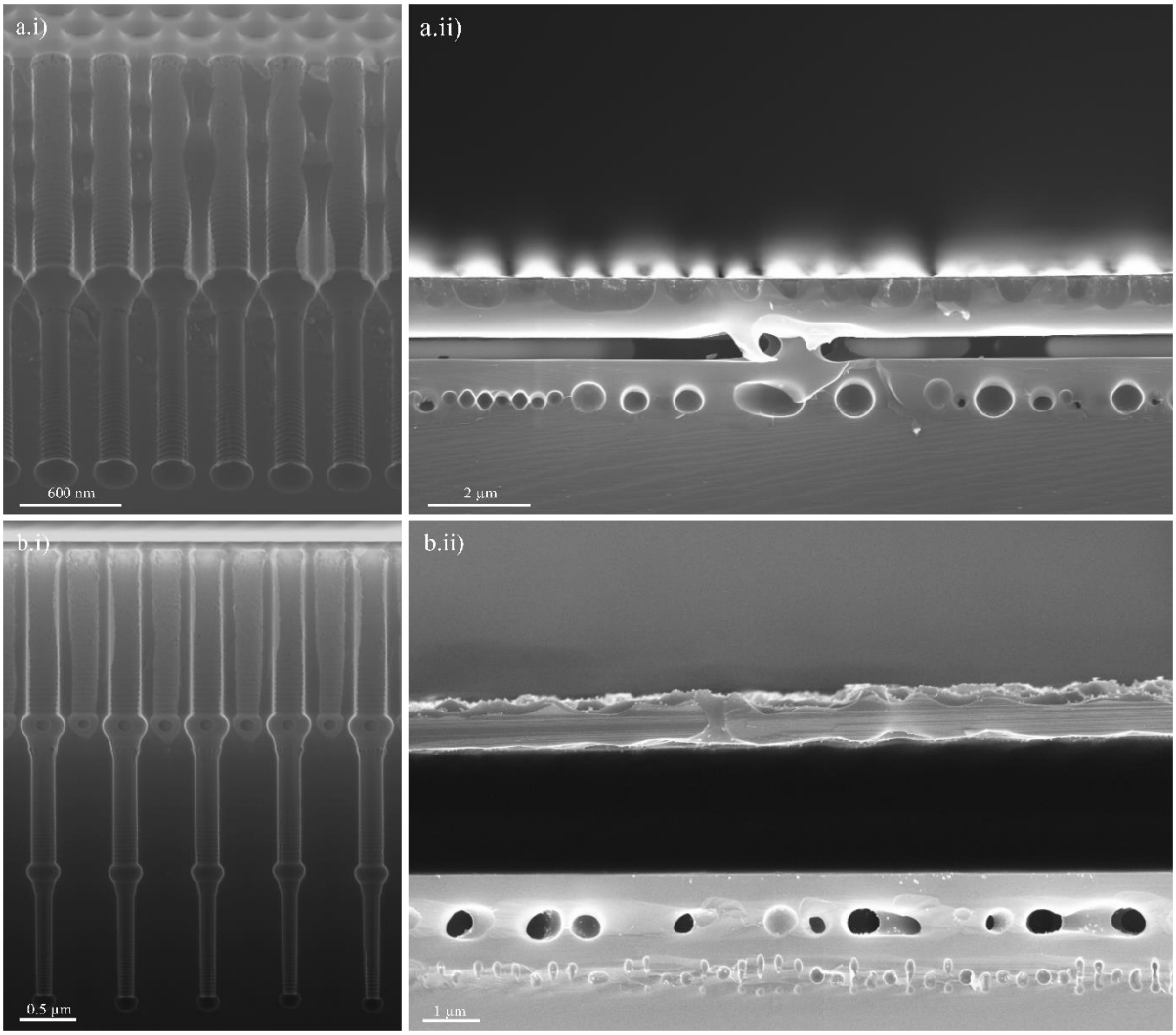

Figure 3.18- Effect of the etch profile after the annealing in RTP. In a.i) and b.i) is after the etch on Pegasus 2 and in a.ii) and b.ii) is after the annealing, respectively. The depth of a.i) is 3.03 µm and of b.1) is 4.64 µm. The RTP recipe is presented in **Table S. 13**. Just a.i) is tilted 20º.

As seen in **Figure 3.18**, with a deeper profile, it is easier to achieve a fully buried cavity, but there are still holes below the one formed that will form another cavity if more process time is given. The evolution of the cavity formation would help to understand how the cavity is formed, and experiments were started; however, it ended in the middle since the tool was down, and the results achieved were not thrust wordy as the tool behaved differently before. When these last tests were performed, the cavities were almost fully formed in only 12 s, while before, it would take 20 s at least, depending on the etch profile. Due to technical problems with the tool, tests were only made with 8 and 12 s, with the same etch profile as in **Figure 3.18**a.i). Indeed, 8 s had almost a fully buried cavity created, and with 12 s, there was one fully formed, and the second one was in the process of formation, being almost formed, just with some connections in some places of the sample. Even though the positive results, it is impossible to recreate the exact result since the process is still not reproducible.

4. CONCLUSIONS AND FUTURE PERSPECTIVES

The work performed with this thesis provided an update on the opportunities of using the CORE/ORE process and the possible challenges to face. Furthermore, it provides up-to-date recipes for the specific tool for open and closed field structures, such as trenches, pillars, holes and nanoholes. The work aimed to study the CORE/ORE process and the dependency between steps, the conditioning of the Pegasus 2 chamber and having a processing window for each type of structure.

Some recipes were developed and optimized for the 200 nm trenches where the optimal oxidation power was found to be 40 W, but more importantly, boundaries were set in the process. An etch pre-step was created to repair the high bias at the beginning of the etch step, stabilizing the process for the etch to occur without reflected power. Further, the pressure was changed from valve control to pressure control to handle the tool's APC throttle valve problems. After that, straight trenches with 3 µm were achieved, but to go further in depth, the Cr mask started to present stress-related issues by curling up, exposing the top part of the feature and being totally under attack.

Straight features were created with a new mask, Al_2O_3, using a 1 µm pillar pattern. The main recipes had to be adjusted as ramping is not needed when etching open field structures, achieving 8 µm straight pillars with the recipe in **Table S. 6**. In the 1 µm holes studies, it was found that the etch time with less undercutting was 1-5 s, regarding the process recipe in **Table S. 7**. For the SF_6 flow during the etch, it was found that using 1200 SCCM could work if the oxidation was optimized to protect the sidewalls, by lowering the 164 nm width variation.

Regarding the nanoscale, problems such as RIE lag, loading and tilting became more evident. Even reproducibility that in previous studies was accounted for, whether due to the valve instability or related to the conditioning of the chamber, has been unreliable. For instance, when repeating the same recipe, the result will vary in depth, as the plasma is unstable due to the cleaning procedure done to the chamber. After the reconditioning of the chamber, some processes were back to normal, but a few presented alterations. Despite that, 200 nm nanoholes were achieved with a depth between 3 µm and 4,5 µm. The studies found that 40 W for 10s during the removal step was enough to remove the bottom while not undercutting the top part.

Working with the nanoholes and the isotropic etch recipes enabled appealing features, which were further annealed in the RTP. The thermal annealing created buried cavities along the sample and in some cases, even one stacked on top of the other. Just with the isotropic etch, a cavity was also achieved with holes connecting to the sample's surface. Though the cavity was very rough to be used for any application, such as microfluidic sensors or in MEMs fabrication, it needed a following anneal to smooth every surface.

Future tests should be done regarding the buried cavities since the study presented here was just the very beginning of it, so more studies should be done to really take advantage of both techniques to create a buried cavity and to study the effect of the ORE etch profile on the formation of the cavities. Furthermore, a new characterization technique should be selected to investigate this type of sample, to gather more information about the transformation during the RTA process, and to improve the previous ORE etch of the structures.

In Pegasus 2, some actions should be taken to guarantee the well-function of the tool and, most importantly, the CORE process. For that, the APC valve throttle should be investigated to check if it needs to be

replaced entirely or if it is just a smaller component that can fix the problem by replacing it. This would solve the reproducibility issue and help with the process stability since the pressure value would be much more precise and closer to the set value. Another thing would be to have an effective way of conditioning the chamber that would not affect, or at least would not change, the plasma formation. This would make Pegasus 2 a more reliable tool.

Moreover, further tests with the CORE/ORE process should be done to go more into the 3D features and try different patterns to see the possibilities of the process. The process still must be intensely studied to be able to compete with less green methods that are more efficient on a larger scale. Also, as this process came as a greener solution for the Bosch process that uses a very bad inhibitor, C_4F_8, the next step would be to try new greener gas mixtures, for instance, F_2-O_2, and maybe later, dream about a fully green H_2-O_2 etch chemistry. Even though CORE/ORE still must be submitted to innumerous tests and still has its flaws, it continues to be a very promising technique of DRIE, capable of achieving HAR features and being a greener option to the Bosch process.

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A.

APPENDIX- MATERIALS AND METHODS

1. Wafers characteristics

- Diameter (mm): 150 ± 0.3
- Material: Silicon
- Growth: CZ
- Type/Dopant: N/Ph
- Orientation: <100> ± 0.5 °
- Resistivity (Ω.cm): 1-20
- Thickness: 675 ± 20 µm
- Surface Finish: Single Side Polished
- Flat: 1 Primary Flat
- Particles (µm): < 20 @ 0.3

2. Equipment Identification

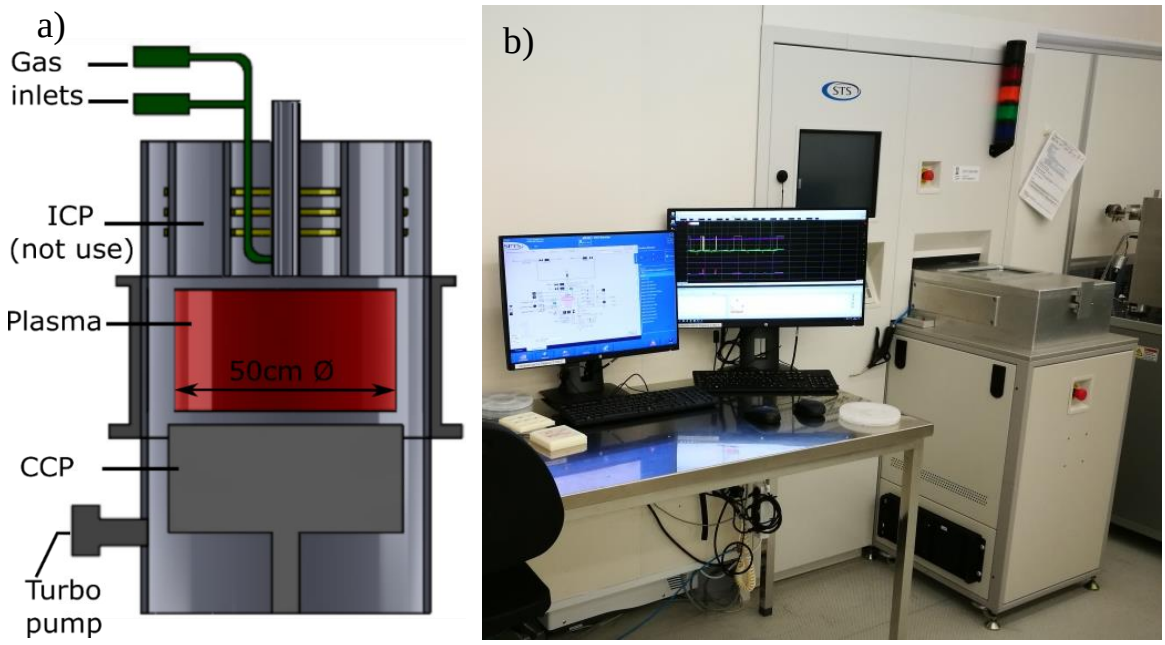

Figure S. 1- STPS Advanced Deep Reactive Ion Etching (DRIE) Pegasus 2, serial number MP0641, Nemotek. In a) is a schematic of the etch system, adapted from [2]. In b) STPS Pegasus 2 operator station, adapted from a closed-acess DTU database.

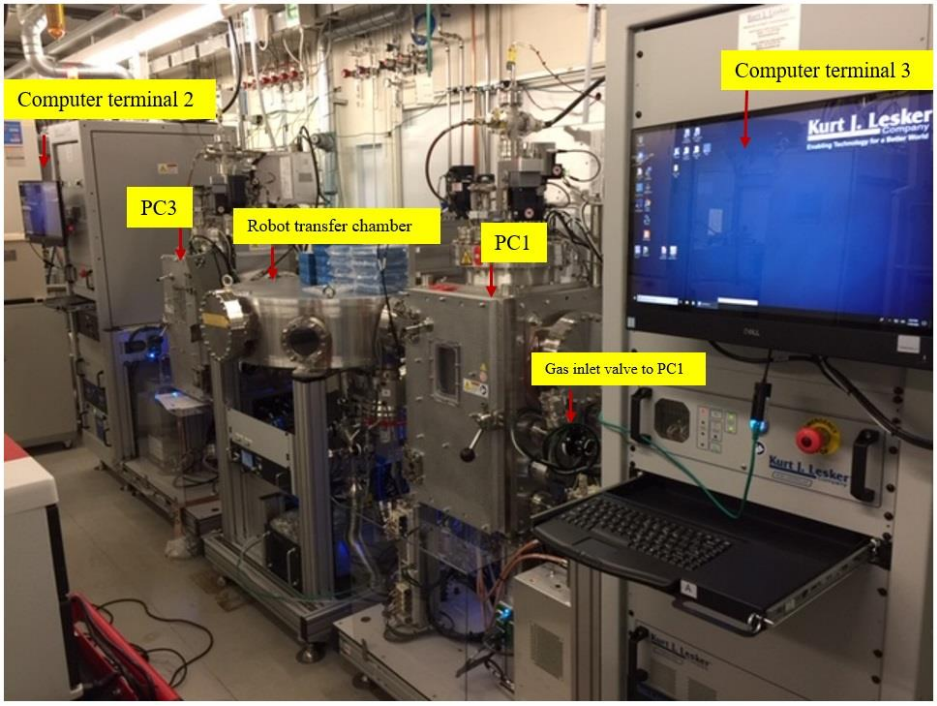

Figure S. 2- Placement and identification of sputter-system for DC/RF sputtering, Lesker. Model 2017 PRO Line PVD75 thin film deposition cluster system. In PC1 (process chamber 1) it is possible to deposit any material with N2 or O2 reactive gases. In PC 3 (process chamber 3) is dedicated to oxygen free materials - nitrides and metals. It is supplied with N2 process gas for reactive deposition. Picture adapted from a closed-acess DTU database.

Figure S. 3- DUV Stepper from Canon (FPA-3000EX4 Stepper system), with excimer laser unit 248 nm wavelength. Picture adapted from a closed-acess DTU database.

Figure S. 4- Picosun thermal atomic layer deposition model R200 equipment. The tool is able to deposit a very thin layer of Al_2O_3, TiO_2 (amorphous or anatase), HfO_2, ZnO and AZO (Al-doped ZnO) on different samples. Picture adapted from a closed-acess DTU database.

Figure S. 5- III-V ICP tool, Inductively Coupled Plasma, SPTS serial number MP0647. Picture adapted from a closed-acess DTU database.

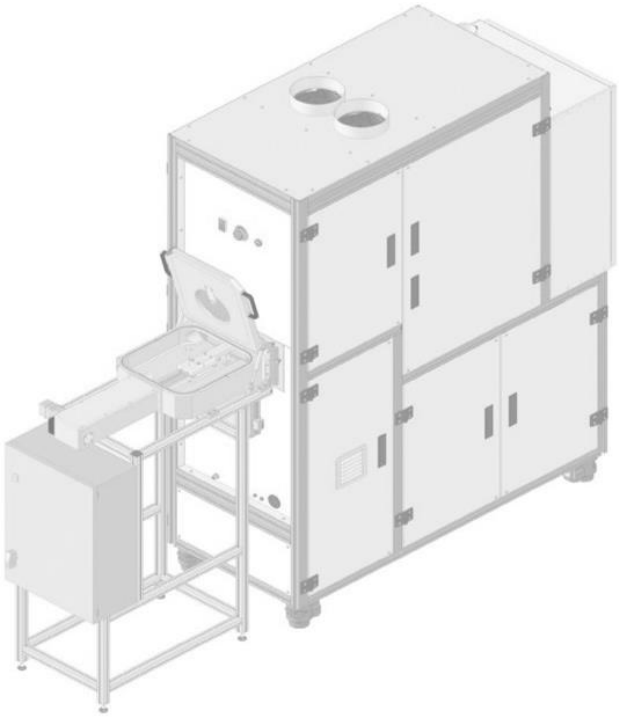

Figure S. 6- Illustration of the Rapid Thermal Processor (RTP) operating system, serial number AS0415C4-7484, ANNEALSYS. Between the process options that this tool offers, only annealing was performed, with the recipe "RTA 1250 HP HF MAX". Picture adapted from a closed-acess DTU database.

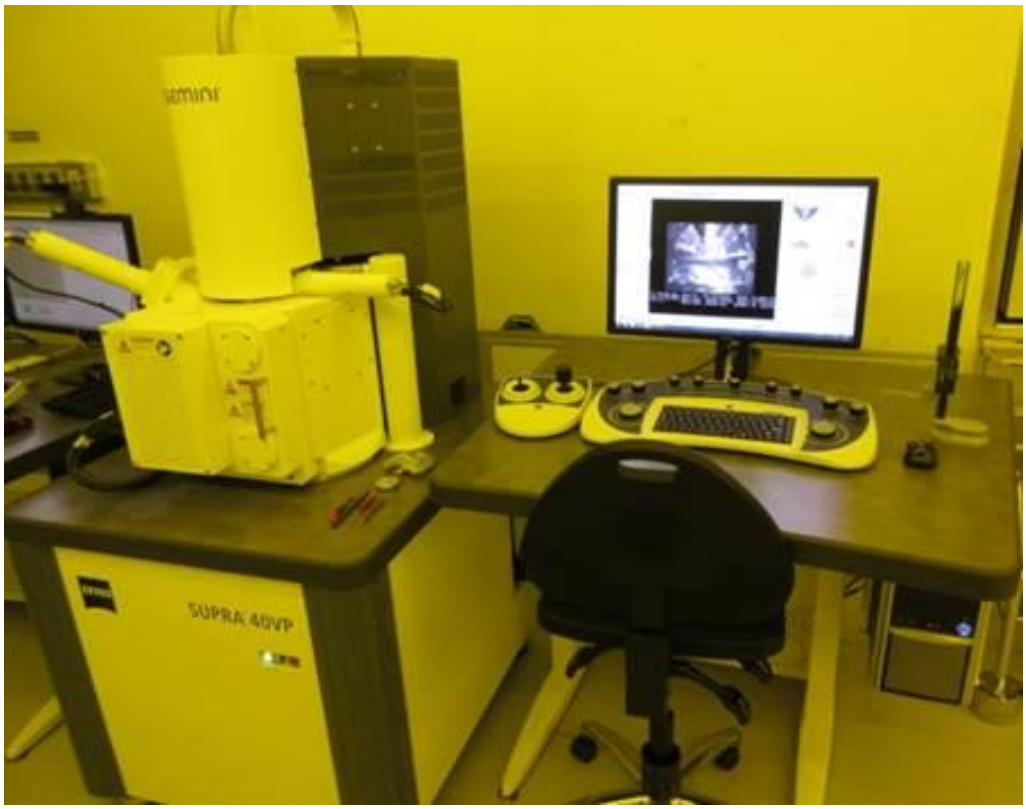

Figure S. 7- Scanning electron microscope (SEM 3) operator stage. The SEM is a ZEISS Supra 40VP, acceleration voltage 20 V - 30 kV, with HDasB detector, serial number 4825. Picture adapted from a closed-acess DTU database.

B.

APPENDIX- RESULTS AND DISCUSSION

Table S. 1- CORE recipe from when the DC bias on the E-step was high, presented in **Figure 3.4**a).

	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
C-step	1	100%	50	0	0
O-step	4	0.5%	50	0	10
R-step	3	100%	0	5	10
E-step	7	3%	0	175	175

Table S. 2- CORE recipe when the E-step was divided into two steps (E1 and E2), presented in **Figure 3.4**b).

	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
C-step	1	100%	50	0	0
O-step	4	0.5%	50	0	10
R-step	10	100%	0	5	10
E_1-step	2	3%	0	175	10
E_2-step	3	3%	0	175	175

Table S. 3- The CORE recipe for 200 nm trenches, reaching 0.75 µm having 54 cycles. The power used was always platen power. **Figure 3.5**a) shows the feature result, with an etch rate of 0.2 nm/s.

#54 = 59 min	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
C-step	4	100 %	50	0	0
O-step	3	0.5 %	50	0	15
R-step	20	100 %	0	5	15
E-step	20-100	1 %	0	15	15

Table S. 4- The ORE recipe for 200 nm trenches reaching 3.26 µm, having 61 cycles. The power used was always platen power. **Figure 3.5**b) shows the feature result, with an etch rate of 1.8 nm/s.

#61 = 30 min	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
O-step	10	3%	200	0	40
R-step	10	100%	0	5	40
E_1-step	2	4%	0	350	40
E_2-step	0-15	4%	0	350	300

Table S. 5- The ORE recipe for 200 nm trenches reaching 4.75 µm, having 48 cycles. The other steps only used platen power. **Figure 3.5**c) shows the feature result, with an etch rate of 2.6 nm/s.

#48 = 30 min	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)	Coil power (W)
O-step	10	220 mTorr	200	0	40	0
R-step	10	100%	0	5	60-100	0
E_1-step	2	220 mTorr	0	1200	0	0
E_2-step	0-10	220 mTorr	0	1200	1	2000

Table S. 6- Pillars recipe with depth of 8 µm, with a low top undercut. 244 cycles were performed, totaling 122 min of the process.

#244 = 122 min	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
O-step	10	3%	200	0	40
R-step	10	100%	0	5	40
E_1-step	2	4%	0	350	40
E_2-step	7	4%	0	350	300

Table S. 7- CORE recipe of structures in **Figure 3.9**. The only parameter changing is the time during the etch step.

60 min	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)	Coil power (W)
O-step	10	220 mTorr	200	0	40	0
R-step	10	100%	0	20	40	0
E_1-step	2	220 mTorr	0	1200	0	0
E_2-step	Ramping	220 mTorr	0	1200	1	2000

Table S. 8- The recipe of **Figure 3.10** where * where SF_6 flow is changing. In a) is 400 SCCM and in b) is 1200 SCCM. The recipe has a total of 144 cycles for 60 min.

	Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)	Coil power (W)
O-step	10	220 mTorr	200	0	40	0
R-step	10	100%	0	20	40	0
E_1-step	2	75%	0	*	0	0
E_2-step	1-5	75%	0	*	1	2000

Table S. 9- The recipe for the 200 nm nanoholes is presented in **Figure 3.13**. The power of the removal step is changed from 20 to 60 W.

	Time (s)	**Pressure**	**O_2 flow (SCCM)**	**SF_6 flow (SCCM)**	**Platen power (W)**
O-step	10	220 mTorr	200	0	40
R-step	10	100%	0	40	*
E_1-step	2	220 mTorr	0	350	0
E_2-step	0-15	220 mTorr	0	350	100-300

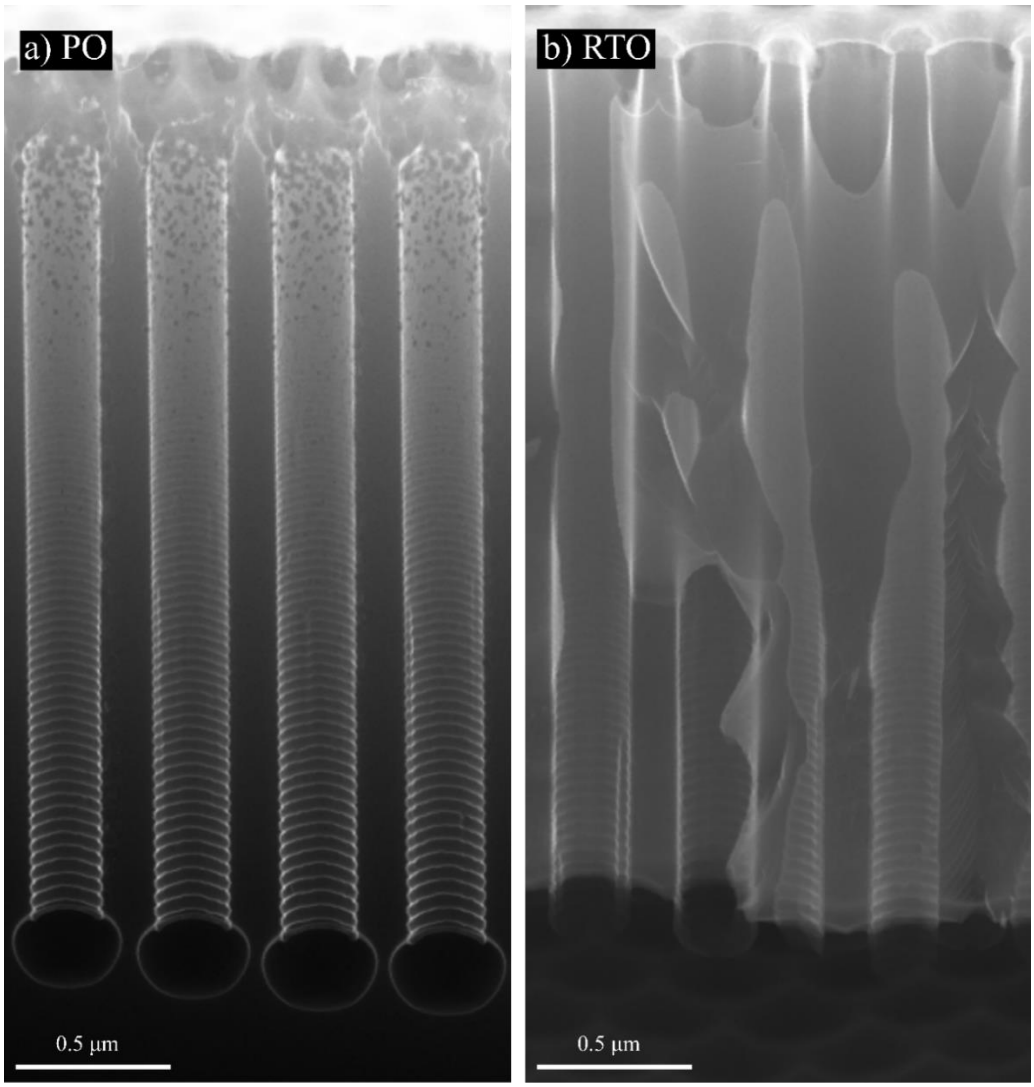

Figure S. 8- Effect of different approaches to oxide growth, wherein a) is used plasma oxidation in Pegasus 2, achieving 3.2 nm of oxide and b) is used rapid thermal oxidation in RTP, achieving 19.2 nm. Both samples were then submitted to an isotropic etch in Pegasus 2 to test the passivation layer. In a) the isotropic etch measures 373 nm wide and is 291 nm deep. In b) due to the excellent sidewall protection, the isotropic etch duration was increased (+250 s) and the bottom of the nanoholes was completely etched, making a buried cavity.

Table S. 10- The recipe for a bottle shape feature, presented in **Figure 3.15**a), reaching 1372 nm.

		Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
Si tube #16 29min 52s	C-step	4	100%	50	0	0
	O-step	8	50 mTorr	50	0	40
	R-step	16	100%	0	5	35
	E-step	84	4%	0	10	30
Si cone #32 14min 56s	C-step	4	100%	50	0	0
	O-step	8	50 mTorr	50	0	15
	R-step	10	100%	0	5	25
	E-step	6	100%*	0	5**	25***
Si tube #42 29min 24s	C-step	4	100%	50	0	0
	O-step	8	50 mTorr	50	0	15
	R-step	16	100%	0	5	35
	E-step	14	1.5%	0	10	15

* In the first 5 s is a 100% valve open, but in the last second has a 1.5% valve open.

**In the first 5 s, the SF_6 flow is 5 SCCM, but in the last second is 10 SCCM.

***In the first 5 s, the power is 25 W, but in the last second is 15 W.

Table S. 11- The recipe for a bottle shape feature, presented in **Figure 3.15**b), reaching 1266 nm.

		Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
Si tube #15 30min	C-step	4	100%	50	0	0
	O-step	16	50 mTorr	50	0	40
	R-step	16	100%	0	5	35
	E-step	84	4%	0	10	30
Si cone #32 14min 56s	C-step	4	100%	50	0	0
	O-step	8	50 mTorr	50	0	15
	R-step	10	100%	0	5	25
	E-step	6	100%*	0	5**	25***
Si tube #42 29min 24s	C-step	4	100%	50	0	0
	O-step	8	50 mTorr	50	0	15
	R-step	16	100%	0	5	35
	E-step	14	1.5%	0	10	15

* In the first 5 s is a 100% valve open, but in the last second has a 1.5% valve open.

**In the first 5 s, the SF6 flow is 5 SCCM, but in the last second is 10 SCCM.

***In the first 5 s, the power is 25 W, but in the last second is 15 W.

Table S. 12- The recipe for an inverted bottle shape feature, presented in **Figure 3.15**c), reaching 639 nm.

		Time (s)	Pressure	O_2 flow (SCCM)	SF_6 flow (SCCM)	Platen power (W)
Si tube #24 16min 48s	C-step	4	100%	50	0	0
	O-step	8	50 mTorr	50	0	15
	R-step	16	100%	0	5	35
	E-step	14	1.5%	0	10	15
Si cone #17 7min 56s	C-step	4	100%	50	0	0
	O-step	8	50 mTorr	50	0	15
	R-step	10	100%	0	5	25
	E-step	6	100%*	0	5**	25***
Si tube #9 16min 48s	C-step	4	100%	50	0	0
	O-step	8	50 mTorr	50	0	40
	R-step	16	100%	0	5	35
	E-step	84	1.5%	0	10	30

* In the first 5 s is a 100% valve open, but in the last second has a 1.5% valve open.

**In the first 5 s, the SF6 flow is 5 SCCM, but in the last second is 10 SCCM.

***In the first 5 s, the power is 25 W, but in the last second is 15 W.

Table S. 13- Recipe from the Rapid Thermal Processor, with a mix of gases and not pure Ar due to tool limits. A total of 4000 SCCM was applied with 74 mbar and 1250 °C. The control type during the annealing was both power and temperature control.

Recipe	Time (s)	Gas	Flow (SCCM)	Pressure (mbar)	Temperature (°C)
RTA HP HF MAX 1250	8	Ar + 5% H_2/Ar	2000 + 2000	74	1250