Universitá degli Studi di Padova

Department of Industrial Engineering
Master Thesis in Electrical Engineering

Comparative analysis of design and control strategies for Three-Phase Four-Legs Power Converters

Student:
Federica Chiereghin

Supervisor:
Prof. Nicola Bianchi (UNIPD)
Co-Supervisor:
Prof. Fernando Briz (UNIOVI)

Academic year: 2016/2017

Abstract

The topic of this thesis is the design and the comparison of different configurations of three-phase four legs power converter, including the study of all possible controllers. Working in grid-forming, with the issue to create a low-voltage grid, a neutral line is usually needed to provide a current path for possible unbalanced three-phase loads or single-phase loads. If the neutral point, which is the point between the neutral path and the fourth leg, is not well controlled, the neutral current usually makes the neutral point shift. This may result in unbalanced grid voltage, DC component or larger neutral current.

The situation studied in this thesis is the following. Connecting a DC energy source, in this case two batteries in series to DC side and balanced and unbalanced loads to AC side, the voltages and currents behaviors in the system are analyzed to understand when is more convenient to use one configuration instead of another. The possibilities to study different topologies of three-phase power converter with different loads, like balanced and unbalanced three-phase loads or single-phase loads, allows to face the problem about the control of positive, negative and zero sequences of grid voltage and the complexity of fourth leg control.

A resume of all possibly configurations are considered only in the beginning of the thesis to have an idea of the differences.

Starting to control of positive and negative sequences of grid voltage of the power converters, the equivalent circuit is design and studied in *dqo* rotating frame, after applying the Park's transformation theory. In this way, it will be easier to work with DC signals. Positive and negative sequences control loops are designed in *dq0* coordinates.

Subsequently, zero sequence voltage and fourth leg controls are faced. Different control fourth leg control strategies are considered in order to know which could be an effective solution to provide the neutral point for a three-phase four wire system and to handle the neutral current due to unbalanced load.

At the end, the results are compared.

All the performances are simulated with balanced and unbalanced loads. The models' evaluation has been analyzed using Matlab and Simulink Power System ToolBox simulation environment.

Sommario

Il tema di questa tesi è l'analisi comparativa di diverse configurazioni e strategie di controllo di un convertitore di potenza trifase a quattro rami. Lavorando con l'obiettivo di creare una rete a bassa tensione, una linea del neutro è generalmente utilizzata per fornire alla corrente un percorso nel caso di carichi trifase squilibrati o carichi monofase. Se il punto neutro, il quale è il punto di connessione tra il percorso del neutro è la quarta rama, non è controllato, la corrente che scorre attraverso il neutro causa un'oscillazione del punto neutro. Tutto questo può portare ad uno squilibrio della tensione di rete, la presenza di componenti in continua o grandi valori della corrente che fluisce nel neutro.

Lo scenario studiato in questa tesi è il seguente. Connettendo una fonte di energia in continua, nel caso studiato due batterie in serie nel lato di continua e un carico equilibrato e uno squilibrato nella parte alternata, tensioni e correnti dell'intero sistema sono analizzate con l'obiettivo di capire quando sia la migliore utilizzare una certa configurazione invece di un'altra. La possibilità di studiare diffenrenti topologie di un convertitore di potenza trifase connesso a diversi tipi di carichi, ad esempio un carichi trifase equilibrati e disequilibrati o un carico monofase, permette di affrontare problemi legati al controllo della sequenza positiva, negativa e omopolare della tensione e inoltre la complessità del controllo della quarta gamba.

All'inizio ciascuna configurazione è presentata per permettere ai lettori una miglior comprensione delle differenze.

Iniziando dal controllo della sequence positiva e negativa della tensione di rete del convertitore di potenza, si è ottenuto il circuito equivalente che sarà studiando nel sistema di riferimento rotante *dq0*, dopo aver applicato la teoria Trasformata di Park. In questa maniera sarà più facile lavorare con grandezze continue. Gli anelli di controllo della sequenza positiva e negativa sono progettati nelle coordinate *dq0*.

Successivamente, il problema relativo ai controlli della sequenza zero e della quarta rama sono affrontati. Diverse strategie di controllo della quarta rama sono proposte per capire quale sia la soluzione migliore per controllare il punto neutro del convertitore di potenza trifase con quattro rami e gestire la corrente che scorre nel neutro causata dalla presenza di carichi squilibrati.

Alla fine tutti i risultati sono confrontati.

Tutte le simulazioni sono studiate supponendo la presenza di carichi equilibrati e squilibrati. Il software utilizzato per implementare tutti i modelli analizzati è Matlab e Simulink Power System ToolBox.

To my parents,
without whom none of my success would be possible.

Contents

Chapter 1

Introduction

1.1 Context and Motivations

Power converters are electronic circuits associated to the conversion, control and conditioning of electric power. The power range can be from milliwatts, for example mobile phone, to Megawatts, in electric power transmission systems. Nowadays power electronics play a key role in energy conversion and consumption and it is expected that power electronics will be more active in energy generation and distributions as well. The task of power converter is to process and control the flow of electrical energy between two systems, by changing the character of electrical energy, for example:

- from AD to DC;
- in different voltage levels;
- frequency;
- phase angle;
- number or phases in AC/AC converters.

An example of a power electronic system in a block diagram form is shown in fig. 1.1.1, where the power input to this power processor is

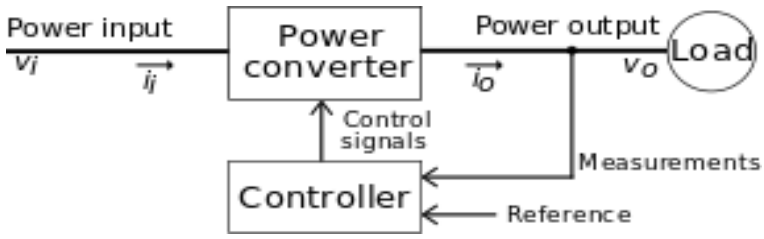


Figure 1.1.1: Block diagram of a power electronics system [9]

usually from the electric utility at a line frequency of 60 or 50 Hz, single-phase or three-phase. Assumed that the power converter has a limited energy store capability, input and output powers must be balanced. Usually, the input voltage is fixed by the grid and output current or output voltage are determined by the control. For example, if the power converter is fixing the output current, the output voltage will be determined by the load, and, in the other way, if the power converter fixes the output voltage, the load will decide the current. Consequently, the input current will be whatever is needed to balance input and output powers.

Usually a feedback controller compares the output of the power system with a reference value and the error between the two is minimized by the controller. If the issue is to obtain stable load voltages, the quantities compare will be the output voltage, effectively measured in the system, and the target value. Generally, the controller in the block diagram consists of linear integrated circuits and/or digital signal processors. A controller could be for example a proportional-integral-derivative controller, called PID, which is a control loop feedback mechanism and continuously calculates an error value as the difference between a desired setpoint and a measured variable and applies a correction based on proportional, integral and derivative terms.

Nonlinearity is a prevailing phenomenon in a system using power converters. The nonlinearity comes from power converters, due to their on/off switching actions, and the load or source of the power converters. A high quality control is achieved when the power converter can see clean, stable grid voltages and the grid voltage doesn't feel the real consume harmonics current or reactive power of the load.

The most common classification of power converters is based on the waveform of the input and output signals, thus:

- DC to DC;
- DC to AC, inverter mode, where is possible to adjust magnitude and frequency;
- AC to DC, rectifier mode;
- AC to AC.

This is one of the possible classification.

A vast body of all the loads consuming electric energy manifests some degree of nonlinearity. All those nonlinear loads draw harmonic currents. Those harmonics cause a lot of problems, such a distorted voltage, voltage flicking, overheating transformer, severe EMI noise to communication systems and computer systems, which could become more and more severe as more and more nonlinear loads put in use in the grid. Unbalanced three-phase source could also cause an overheated neutral conductor due to excessive neutral current.

The purpose of this thesis is to study different topologies for the power converter DC-AC, for example with split capacitors or half bridge, or both in the same power converter, with different connections (mid-point of the capacitors connected to the neutral or not), fed by DC energy sources and connected to the filter, that could be *LCL* or *LC*, and three-phase balanced and unbalanced loads using different control strategies for three-phase power converter with fourth leg systems.

1.2 Overview and Methodology

A lot of research has recently been focused on power converters due to increasing deal of interest in power electronics. This is mainly caused by their broad applicability domain that includes telecommunications systems, transmission and distribution systems, applications in renewable energy, distributed generation and smart grids. This current research is interested also in studying, for various reasons, small power generating units which are connected to the power grid at the low-voltage end, which nowadays are increasing. Some of these units use synchronous generators, but most use DC or variable frequency generators coupled with electronic power converters.

In these low-voltage grid connected systems, a neutral line is usually needed to provide a current path for possible unbalanced loads or for single phase loads. If the neutral point is not well controlled, the neutral current usually makes the neutral point shift. The shift of the neutral point may result in unbalanced/variable output voltage, DC component in the output, larger neutral current. For these reasons, there is often a need to have a neutral line to work with inverters. The neutral line is usually needed on the AC side of the converter to provide a current path for the zero-sequence current components.

If the neutral line is not well controlled and the neutral current has strong low-frequency components, then the neutral current causes the neutral point to deviate severely from the mid-point of the DC source. This deviation of the neutral point may result in an unbalanced or modulated output voltage, the presence of zero- sequence voltage components, and hence an even larger neutral current. Thus, the generation of a balanced neutral point efficiently and simply has now become an important problem.

Tackling the control problems in detail for each power converter's configuration is the scope of the thesis.

1.3 Main objectives

Four different possibilities are studied.
The principle objective is to study the four configurations for the converter, which and are:

- conventional neutral leg, which is a three-phase power converter with fourth leg;
- split DC-link capacitors;
- independently-controlled neutral leg;
- independently-controlled neutral leg, without the connection between the filter and the neutral wire.

In the Chapter 2 each configuration will be explain with additional details in order to understand the differences and the equivalences of each.
Subsequently, the topologies will be studied with two types of passive filters, *LC* or *LCL* filter and with different control strategies to control the output voltage.
The objectives of the control can be grouped into two families:

- the first group consists of the control of positive and negative sequence. Working with balanced and unbalanced loads, it's necessary to control the positive and negative sequence of the output voltage of the power converter simultaneously. The positive sequence is controlled to achieve the imposed target of the output voltage. The unbalance compensation is achieved by cancelling the negative sequence component of the line-to-line voltages of the inverter output, reducing the load voltage to a balanced system with amplitude given by the positive sequence. Each of two controls can be realized using PI because the analysis is done working with DC components, after the Park's transformation of the three-phase signals from *abc* to *dq0* reference's systems.

- the second one consists of the control of zero voltage sequence and neutral leg. The idea is to attenuate the 50 Hz component of the zero-voltage sequence of the output voltage and to control the neutral point in order not to have neutral current which usually makes the neutral point shift. This allows the system to also perform load voltage regulation. Since the target is to attenuate oscillations of 50Hz, the controllers will be Proportional-Resonant, called PR.

The use of pulse-width modulation (PWM) results in a system with fast dynamic response, and the possibility to use a high switching frequency allows a considerable reduction in the power rating of the required filter.

1.4 Thesis structure

This thesis is divided in 5 chapters.

Chapter 1 is a general introduction and presentation of power electronics and problems related to power electronics. The issues of the thesis are presented.

Chapter 2 presents four-legs three-phase power converter topologies. Considering the possibility to connect to the power converter different passive filters, the advantages and disadvantages are discussed. At the end of chapter, the characteristics of the power converters, filters and loads are presented.

Chapter 3 discusses the control objectives. At the begining a small presentation of all possible control design is proposed to have a global idea of them. After the chapter is focus on positive sequence and negative sequence control, with a brief overview about what symmetrical component and Park's transformation are. At the end zero voltage sequence and fourth leg control are analyzed for each topology.

Chapter 4 addresses the comparative analysis and simulation results. In order to see the principle difference, the harmonic spectrum of each voltage and current of the topologies are shown. After the THD is calculated to respect the limits imposed by the law. Being the harmonic contents of voltages and currents enough sensible to the control stategies, type of filter and controllers, all these aspects are analyzed and compared for each topology.

Chapter 5 is the conclusive chapter, when a brief summary of my work is presented and the conclusion are briefly illustrated.

Chapter 2

Configurations of Three-Phase Power Converters

2.1 Introduction

This chapter discusses the power converter topologies, principle operation of power devices.

A power converter is an electric circuit that changes the electric energy coming from a source one to the desired form, optimized for example for a specific load. The power converter is the link between the power source and the power supply output.

Control technology is integrated to obtain proper performance of power converters. Improvement in system performance involves not only the use of advanced control techniques, but often also the integration of several converters into a larger system. Individual power converters are often part of a larger system which can include for example a motor drives, active power filter, DC power supplies, etc. In addition to the control of the converter, integration and communications are also important functions since they are at the heart of factory automation.

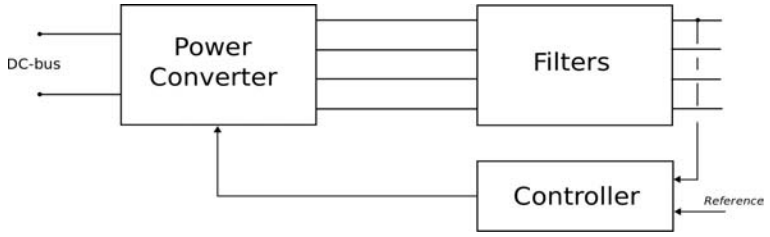


Figure 2.1.1: Generic system

A generic power system is shown in fig. 2.1.1. It is seen to consist of three major block: electronic power converter, filter and control. A DC-link feeds the power converter, which will be a three-phase power converter with three legs or four legs. The chosen filters are or *LC* or

LCL. For the three-phase three-leg case, loads can be balanced and unbalanced. For three-phase four leg case, single phase load can also exist.

Since the issue is to control the voltage grid, the measured voltage is compared with the reference value and the error enters a controller. Controllers can be of different types, as PID or a PR regulators. The output of the controller is a voltage command which is later modulated to have the gate signals for the switches of the power converter. In the following chapter, there will be a section in order to analyze the details of the controllers.

A power converter uses non-linear component such as the semiconductor switches, and linear reactive components such as the inductors or capacitors for intermediate energy storage. The size, weight and cost of the converter are largely determined by these components. In this grid-connected inverter, IGBT are normally used, gate signals being normally modulated by the high frequency PWM. On-off behaviour of the power switches produces large $\frac{du}{dt}$ which care result in relatively large values of $\frac{di}{dt}$. Passive filters, placed between the power converter and the grid, are used to reduce the amount of switching harmonics being injected into the grid.

This chapter deals with the four topologies of three-phase power converter with four legs, to illustrate the structure and their most important characteristics. The basic structure is the same, which includes the three legs of the three-phase power converter and neutral wire which is connected to the neutral point of three-phase unbalanced loads or single-phase. Depend on the topologies, the fourth leg, the neutral inductor L_n and the split DC capacitors could be present. The principle idea is to list all the topologies and underline the importance of the components which belong to. A briefly presentation of the configuration control is mentioned, emphasizing the control objectives. As just said, the switches are modulated by PWM, for this reason a summery is reported to have a clear idea of how it works. Due to the use of PWM, a high harmonic content is present. A simple way to reduce the harmonic content of the current and grid voltage is the use of passive filter. These filters can be *L*, *LC* or *LCL* types, and are usually placed between the power converter and the loads/grid. For this reason, at the end of the chapter, the possible passive filters are listed, which are *L*, *LC* and *LCL*, with respectively proprieties.

2.2 Description of the configurations

In this section, a description of each controllers and studied configurations is presented, control configuration being also briefly discussed. Block diagrams using *LC* and *LCL* filters are shown for each configura-

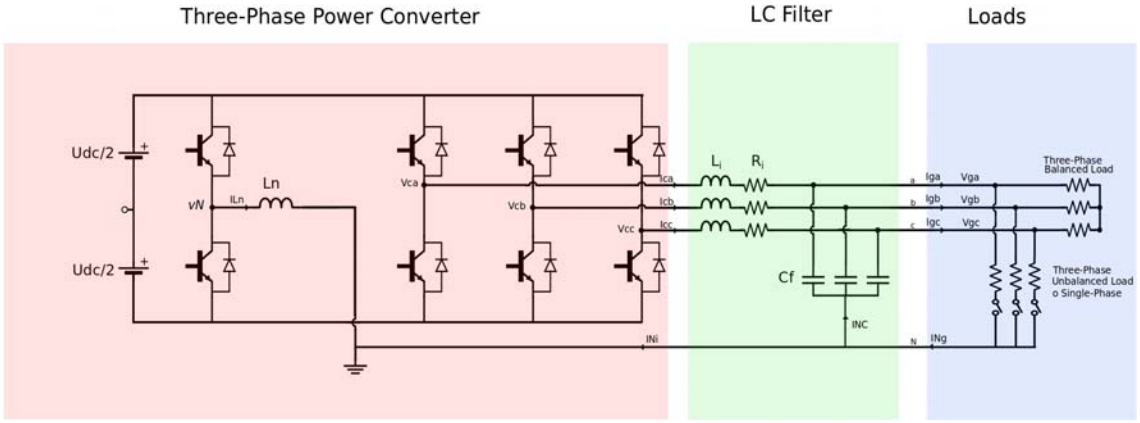


Figure 2.2.1: Three-Phase power converter with fourth leg, *LC* filter, balanced and unbalanced load without the capacitors in the DC-bus

tion. The load includes three-phase elements, which can be symmetric or asymmetric as well as single phase elements.

The circuit topologies available to generate a neutral point are:

1. conventional neutral leg, which is a three-phase power converter with fourth leg, as shown in figures 2.2.1 and 2.2.2;

2. split DC-link capacitors, which is a three-phase power converter with split capacitors in the DC-bus and the neutral wire, tying the neutral point to the mid-point of the DC-link capacitors, as depicted in figures 2.2.3 and 2.2.4;

3. independently-controlled neutral leg, which is the combination of the first two, as represented in figures 2.2.5 and 2.2.6;

4. independently-controlled neutral leg, without the connection between the filter and the neutral wire, shown in fig.2.2.7 and 2.2.8.

2.2.1 Conventional Neutral Leg

A main provide a neutral line is to add an additional fourth leg, called neutral leg, to the conventional three-legs power converter. Neutral inductor is connected to the ground. An advantage of this approach is that there is no requirement for a split DC-link and the neutral point is more stable.

Connecting to the power converter the filters and the balanced and unbalanced loads, the global systems are shown in 2.2.1 and 2.2.2, with *LC* and *LCL* filters, respectively. The neutral inductor L_n is connected between the middle point of the fourth leg and the neutral path, which includes the neutral wire between the middle point of the fourth leg, the filter and the neutral point of the unbalanced load. The idea is to

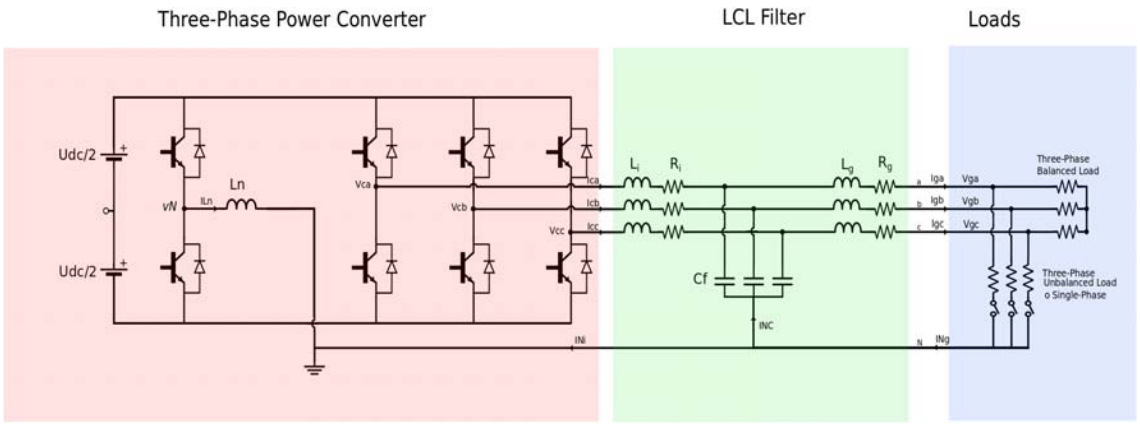


Figure 2.2.2: Three-Phase power converter with fourth leg, *LCL*-filter, balanced and unbalanced load without the capacitors in the DC-bus

achieve the target value and balance the output voltage V_{ga}, V_{gb} and V_{gc} controlling positive and negative sequences and after, to control the voltage in the neutral point N to attenuate the 50 Hz component will consequently prevent the oscillation of this point respect the DC-bus due to the current which is flowing through the inductor L_n and containing 50 Hz component due to the unbalanced load. The inductor L_n in connected directly to the ground.

2.2.2 Split DC-link Capacitors

The simplest mechanism to obtain the neutral voltage is to use split DC-link capacitors. The ground point is clamped at mid point of the DC-link. Since the neutral current flows through the DC-link capacitors, unrealistically high capacitances are needed to avoid oscillations of the neutral voltage if the load unbalance is severe. The neutral point usually shifts and becomes non-neutral. By tying the load neutral point to the mid-point of the fourth leg, this configuration can handle the neutral current caused by an unbalanced load or balanced single-phase nonlinear loads. Large and expensive DC-link capacitors are needed to maintain an acceptable voltage ripple level across the DC-link capacitors in case of a large neutral current due to unbalanced and/or nonlinear load[15].

Connecting to the power converter the filters and the loads, the global systems are shown in 2.2.3 and 2.2.4, with *LC* and *LCL* filters, respectively. The middle point of the capacitors is connected to the ground to the neutral path, which connects the filter and the neutral point of the unbalanced loads. The system is similar to a normal three-phase power converter with three legs, for this reason it's only necessary to control the positive, negative and zero sequences of the output voltage V_{ag}, V_{bg} and V_{cg} in order to balance the voltage and achieve the target.

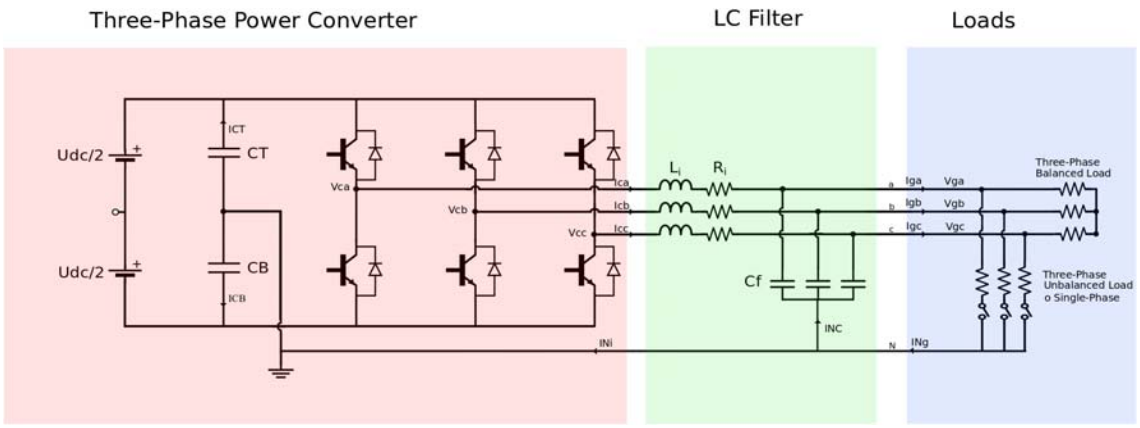


Figure 2.2.3: Three-Phase power converter with the capacitors in the DC-bus and neutral wire, *LC*-filter, balanced and unbalanced load

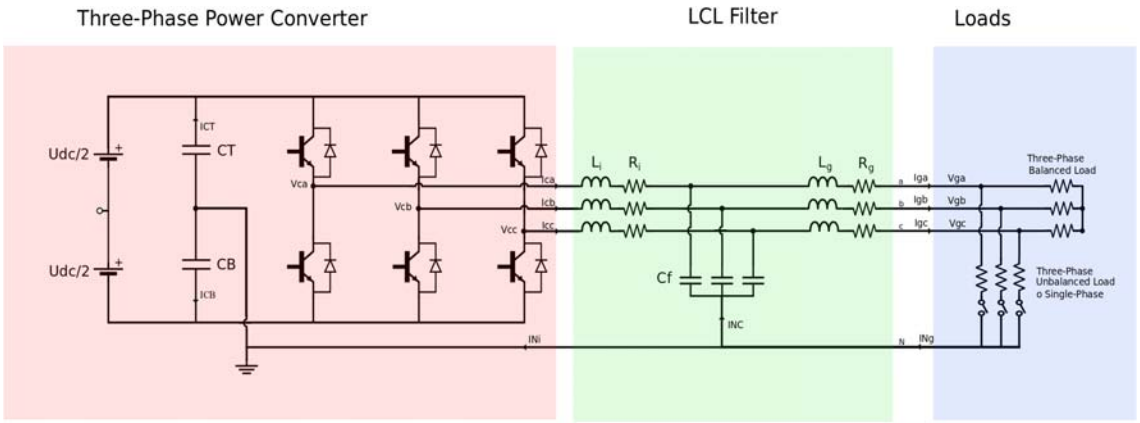


Figure 2.2.4: Three-Phase power converter with the capacitors in the DC-bus and neutral wire, *LCL*-filter, balanced and unbalanced load

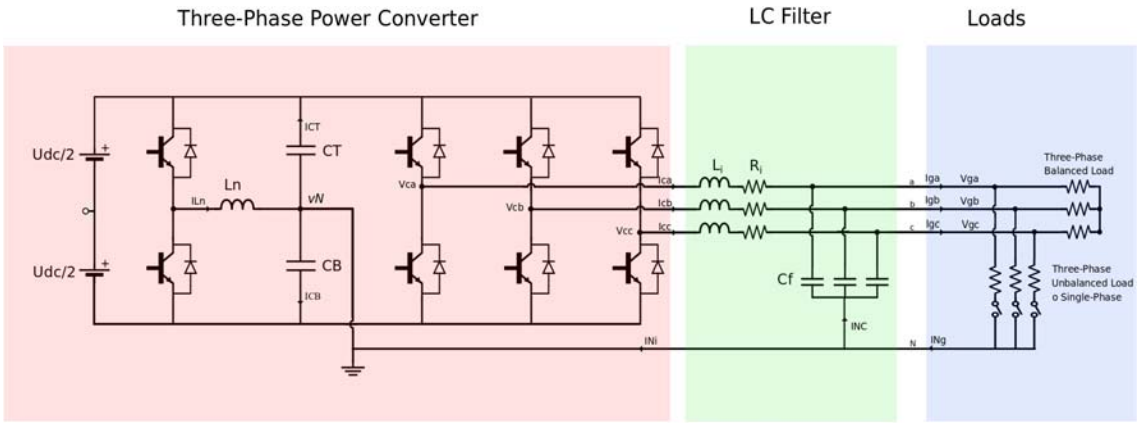


Figure 2.2.5: Three-Phase power converter with four legs and split capacitors in the DC-bus, *LC*-filter, balanced and unbalanced load

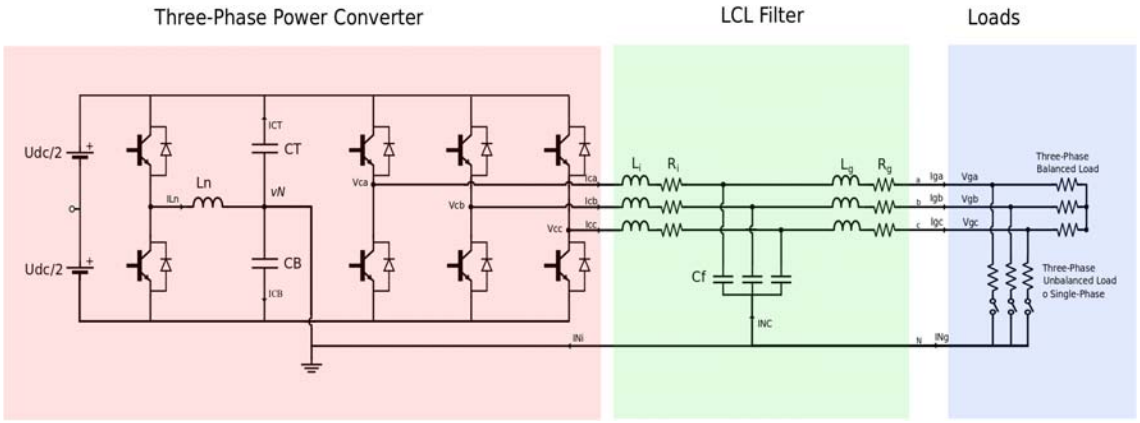


Figure 2.2.6: Three-Phase power converter with four legs and split capacitors in the DC-bus, *LCL*-filter, balanced and unbalanced load

2.2.3 Independently Controlled Neutral Leg

Another topology is the combination of the first two circuits shown. The control of the neutral point is decoupled from the control of the three-phase converter. The neutral current can be controlled to flow through the inductor so that the neutral point is maintained at the mid-point of the DC-link. This allows the phase legs and the neutral leg to be controlled independently, which means the three phases can be controlled independently as well. Since the 50 Hz component of the neutral current no longer flows through the DC-link capacitors, large capacitors are not needed anymore, saving weight, volume and cost. It allows the neutral leg to be controlled independently from the inverter phase legs.

Connecting to the power converter the filters and the loads, the global systems are shown in 2.2.5 and 2.2.6, with *LC* and *LCL* filters, respectively. In this configuration, the neutral inductor L_n is placed in the middle of the split capacitors and the fourth leg. Also in this case, the middle

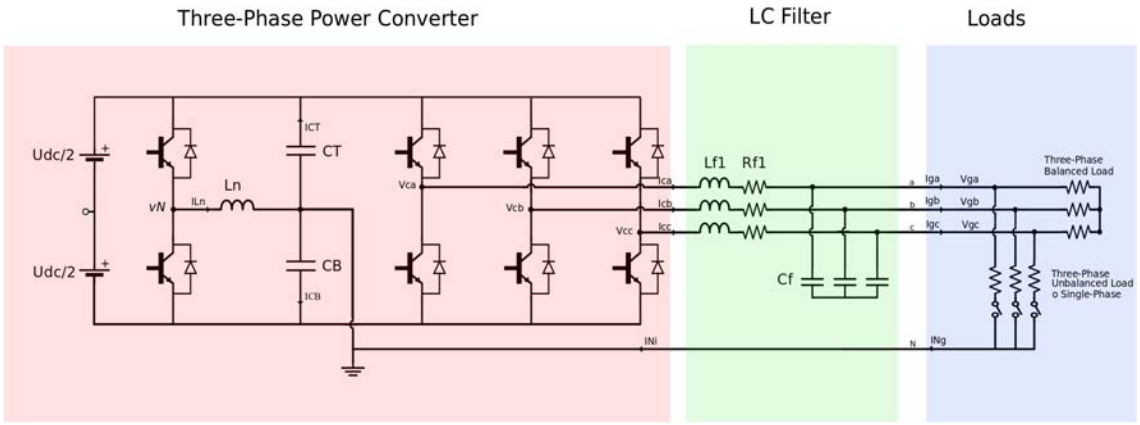


Figure 2.2.7: Three-Phase power converter with four legs and with the capacitors in the DC-bus, *LC*-filter, balanced and unbalanced load, without the connection between neutral path and *LC*-filter

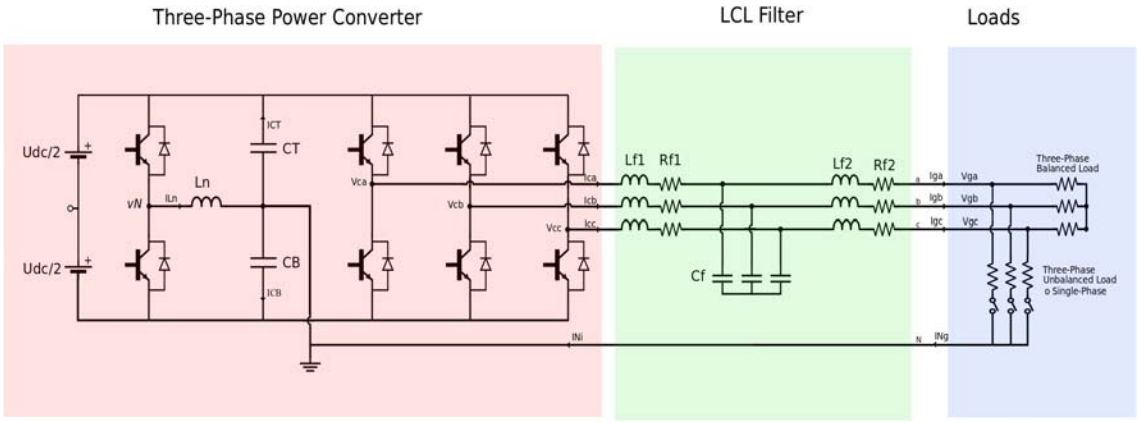


Figure 2.2.8: Three-Phase power converter with four legs and with the capacitors in the DC-bus, *LCL*-filter, balanced and unbalanced load, without the connection between neutral path and *LCL*-filter

point of the fourth leg and L_n are connected directly to the ground. The issue in this case is again to balance and achieve the target of the output voltage V_{ag}, V_{bg} and V_{cg} controlling not only the positive, negative and zero sequences but also the neutral voltage vN, with a voltage control loop, in order to reduce the 50 Hz component using a PR.

2.2.4 Independently Controlled Neutral Leg, without the connection between the filter and the neutral wire

The configuration is similar to the previously case, but without the connection the mid point of the *LCL* or *LC* filter and the neutral.

Connecting to the power converter the filters and the loads, the global systems are shown in 2.2.7 and 2.2.8, with *LC* and *LCL* filters, respec-

tively. This configuration is similar to the previously one, with the only difference that the filter is not connected to the neutral path and consequently not to the ground. It's interesting to study this configurations because of the variation of the harmonic content in the current and in the voltages of the system. The details of the effects of connecting or not the neutral of the capacitors to the neutral of the inverter will list in the following chapters.

2.3 Pulse Width Modulation

The power devices of the DC-AC inverters are usually controlled using Pulse Width Modulation. The PWM concept is borrowed from communication systems, where a signal is modulated before its transmission, and then demodulated at the receiving terminal to recover the original signal. The same concept can be applied to a power converter and motors.

PWM control requires the generation of both reference and carrier signals that feed into a comparator which creates output signals based on the difference between the signals, as shown in figure 2.3.1. Normally the reference signal is a sinusoidal voltage or current and at frequency of the desired output signal, while the carrier signal is often either a saw tooth or triangular wave at a frequency significantly greater than the reference, and which is equal to the switching frequency of the power devices. When the reference is greater than the carrier signal, the comparator output signal is 1; the top power switch is closed in this case, the bottom power switch being open. On the contrary, when the reference is lower than the carrier signal, the comparator output is 0; the top power switch is open and the bottom power switch is closed.

In the fig. 2.3.2, it's shown what happens in the comparator which creates the gates commands. Knowing that switches in a branch should never be turned on simultaneously, 8 feasible states of switching are possible, which are classified in active and zero states. Zero states are two and signifies that the switches at the top or at the bottom of each legs are opened simultaneously. In the fig. 2.3.2 zero states are the first and the last configuration. The active states are four and are the other possible switching configurations.

At the top of fig. 2.3.3, a period of triangle wave T is shown. Since the switching frequency is higher the sine frequency, the sine wave will appear constant in a triangle wave period. The sine waves are the references of each phase, which compared with the triangle wave generate the gate commands. To get the sinusoidal output, the reference is set to be sinusoidal. In this way, a pulse train is obtained. Comparing the reference voltage with the carrier a modulated phase voltages is obtained, which is the voltage what the grid really sees.

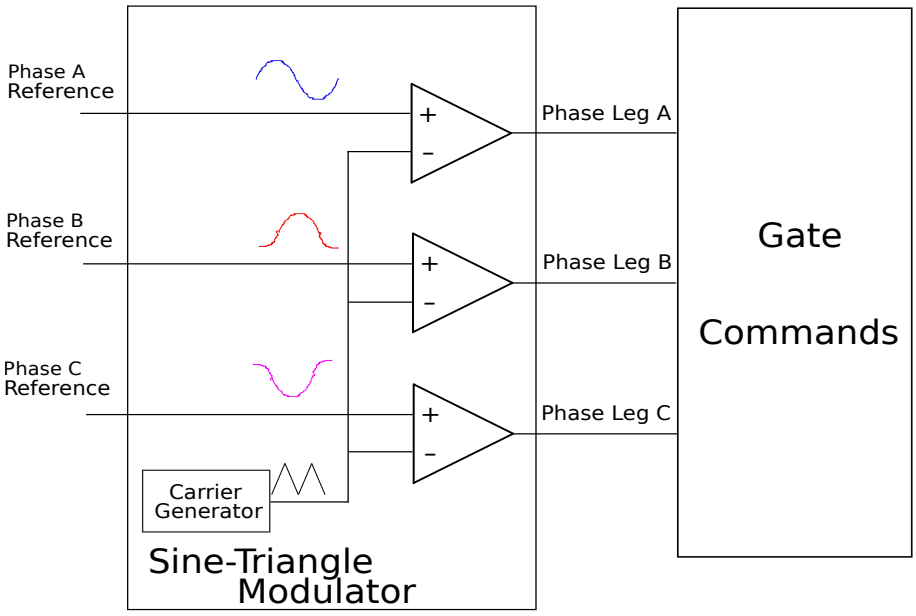


Figure 2.3.1: PWM: Block diagram

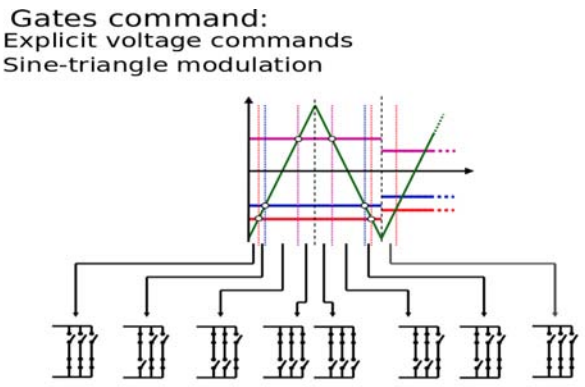


Figure 2.3.2: PWM: Gates commands

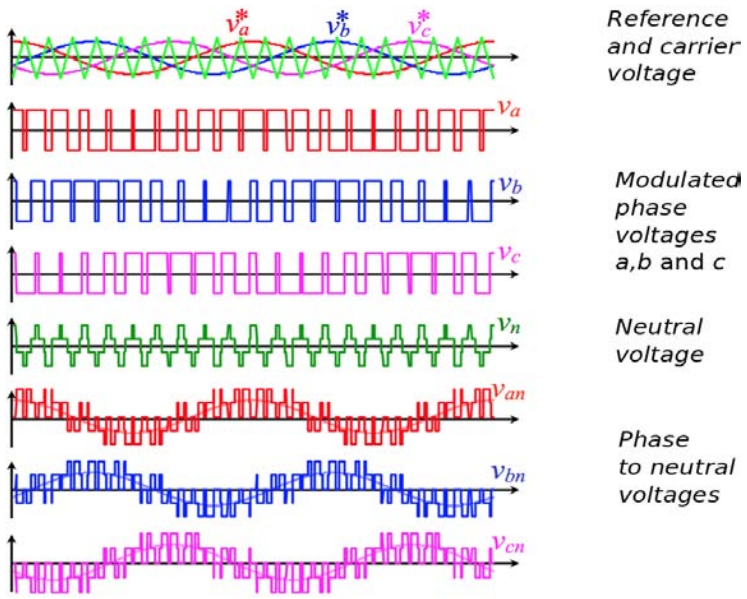


Figure 2.3.4: PWM analysis: relation between gate commands and phase to neutral voltage in the time

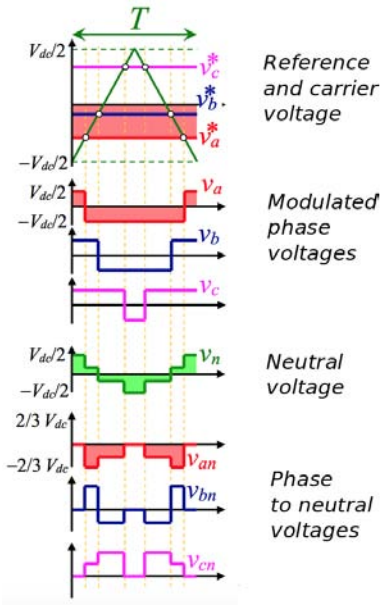


Figure 2.3.3: PWM analysis: relation between gate commands and phase to neutral voltage in a triangle wave period

Knowing that the phase to neutral voltage is, considering just the phase *a*, $v_{an}=v_a-v_n$, it will be easy to calculate it. The procedure is analogous for the other two phases, just moving the sine of $-\frac{2\pi}{3}$ for phase *b* and $-\frac{4\pi}{3}$ for the phase *c* and knowing that $v_{bn}=v_b-v_n$ and $v_{cn}=v_c-v_n$. Repeating the same process for more time, the results is shown in fig. 2.3.4. Generally, the amplitude of the sine wave is smaller than the amplitude of the triangle wave. There is the possibility in which the amplitude of the sine wave becomes bigger than the amplitude of the triangle wave, and it's called overmodulation. The problem of the overmodulation is that it generates an output voltage with much more harmonics respect the previous case.

In this case, the PWM is used not only to command the switches of the three conventional legs of power converter but also the switches of the fourth leg.

Since the modulator has a great impact on voltage/current distortions, switching losses and EMI, it is of a great interest to the power electronics researchers. It is always desirable to minimize the distortion of the output voltage or current. The power losses are related to the total number of switching actions in one switching cycle, and the current level at switching. Harmonic spectrum of the output voltage or current is related to the EMI issue and acoustic noise [14].

2.4 Filters

In this thesis, each power converter configuration is studied with two passive filters in the load side, which are:

- *LC* filter
- *LCL* filter

In order to understand the reason why *LC* and *LCL* filters are used, it's convenient to introduce also the *L*-filter.

Passive filters are considered as one of the cheapest way to reducing harmonics. Other way to reduce the harmonic content is, for example the use of active filters[8]. This type of filter attenuates the harmonic content injecting equivalent current exactly in the moment where there are harmonics.

2.4.1 *L*-filter

The first filter used was the first-order *L*-filter with attenuation 20 dB/decade over the whole frequency range, as shown in the fig 2.4.1. However, they suffer from poor harmonic attenuation. Due to this, large values for the inductor are required, what affects to the dynamic response, increase the voltage drop across the filter as well as its size and weight. For these reasons, higher order filters were introduced to overcome the limitations of *L*-filter.

2.4.2 *LC*-filter

LC-filter is a second-order type of passive filter. It contains an inductor connected in parallel with capacitor, as shown in Figure 2.4.2. For easy of study, equivalent single-phase circuit of *LC*-filter is analyzed instead of three-phase circuit. The filter transfer function is given by 2.1

$$G(s) = \frac{V_{\text{out}}}{V_{\text{in}}} \tag{2.1}$$

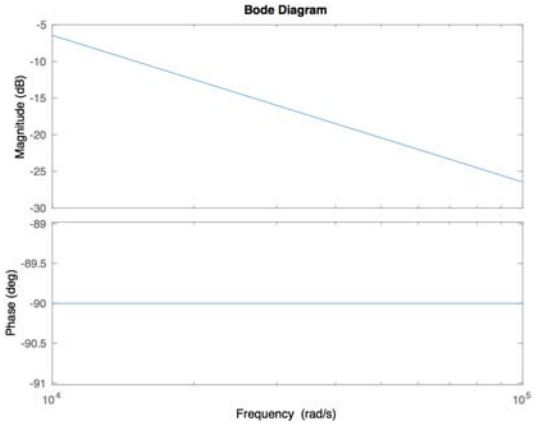


Figure 2.4.1: *L*-filter: Bode Diagram

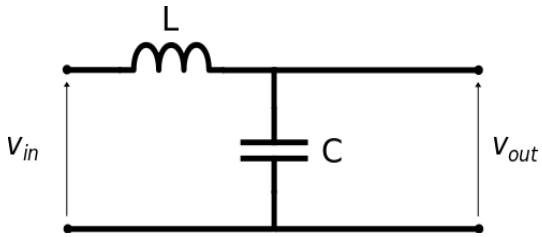


Figure 2.4.2: *LC* filter: Example

where, considering the specific case of an *LC*-filter, V_{in} is the input voltage of the *LC*-filter circuit, which could be the output voltage of the inverter, and V_{out} is the output voltage across the load. Using voltage division rule, the expression of V_{out} and V_{in} are given [7]

$$V_{\text{out}} = \frac{Z_{\text{load}}}{1 + j\omega C Z_{\text{load}}} \tag{2.2}$$

$$V_{\text{in}} = j\omega L + \frac{Z_{\text{load}}}{1 + j\omega C Z_{\text{load}}}. \tag{2.3}$$

Using 2.2 and 2.3, 2.1 can be rewritten as

$$G(j\omega) = \frac{1}{1 + LC(j\omega)^2 + j\omega \frac{L}{Z_{\text{load}}}} \tag{2.4}$$

where Z_{load} is the impedance of the load connected to the power converter.

As shown in fig. 2.4.3, it has a better damping behaviours than *L*-filter. It provides 12 dB per octave of attenuation after the cut-off frequency f_0, it has no gain before f_0, but it presents a peaking at the resonant frequency f_0. The inductance L should be limited to a minimum possible

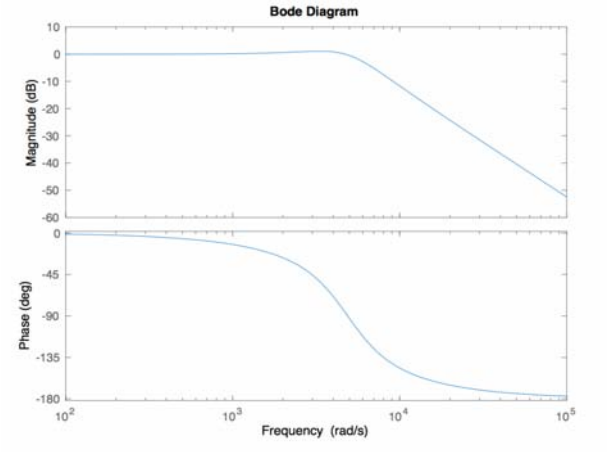


Figure 2.4.3: *LC*-filter: Bode Diagram

value to reduce its large volume. The capacitor C attenuates the harmonics by providing a low resistance path to the ground. The value of C should be such that it provides a good power factor at fundamental frequency as well as to avoid large currents that may damage the power device. The own design of the filter is a compromise between the value of the capacity and inductance.

The resonant frequency of the *LC*-filter is given by 2.5

$$f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{LC}}. \tag{2.5}$$

The resonant frequency of the *LC*-filter must be lower than the switching frequency of the inverter switches for the proper attenuation of the switching harmonics.

2.4.3 *LCL*-filter

LCL-filters are becoming popular in the renewable energy industry today [6]. They provide an efficient and economical way to improve the quality of power fed. *LCL* filters are of third order and require more complex current control strategies to maintain system stability and are more susceptible to interference caused by grid voltage distortion.

The *LCL* filter has good current ripple attenuation even with small inductances values. It also provides better decoupling between the filter and the grid impedance and lower current ripple across the grid inductor. Depicted the fig. 2.4.4, the attenuation of the *LCL*-filter is 60dB/decade for frequencies above resonant frequency, therefore lower switching frequency for the converter can be used.

Despite the advantages, it can bring also resonances and unstable states into the system. To suppress the resonance effect of the fil-

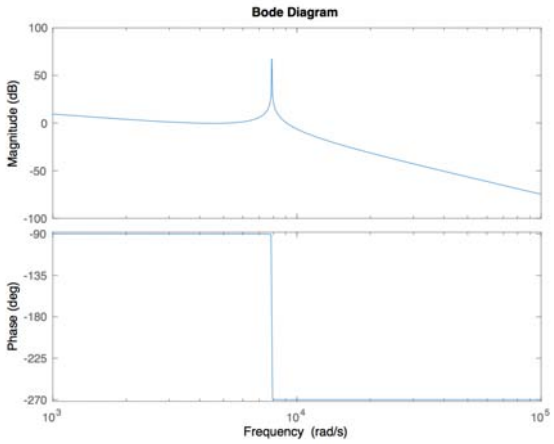


Figure 2.4.4: : Bode Diagram*LCL*-filter

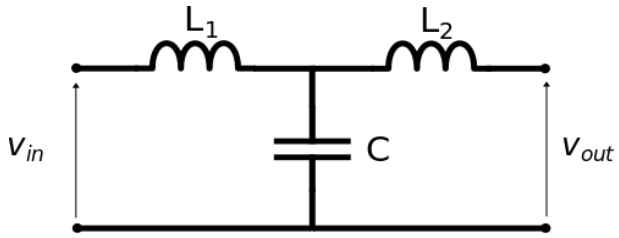


Figure 2.4.5: *LCL*-filter: Example

ter components, active and passive damping techniques are employed. Therefore the filter must be designed precisely according to the parameters of the specific converter.

As shown in Fig. 2.4.5 and considering just the equivalent single-phase circuit instead of the three-phase, the *LCL*-filter circuit consists of inductance L_1 on the power converter side, inductance L_2 on the load side and a capacitor C. The *LCL* filter transfer function is given using 2.6 and neglecting the internal resistances of inductance and capacitance,

$$G(j\omega) = \frac{1 + Z_{\text{load}} j\omega C}{L_1 L_2 C(j\omega)^3 + (L_1 + L_2) Z_{\text{load}} C(j\omega)^2 + (L_1 + L_2) j\omega} \tag{2.6}$$

where Z_{load} is the impedance of the load connected to the power converter. Choosing large values of C provides higher order harmonic suppression. But it results in higher reactive power and increased demand of current from L_1 thereby decreasing the efficiency of the overall filter system. Decreasing the capacitor size requires large inductance to meet the harmonic mitigation requirement. Thus, selection of C value for the *LCL* filter is a tradeoff between the reactive power and the selection of inductors. The design parameters for a passive *LCL*-filter include the power rating of the inverter, the line frequency, and the switching frequency of the inverter switches. The inductors in the *LCL*-filter are designed by de-

termining the current ripple. However, the size of the inductor increases. Thus, the selection of the current ripple is a trade-off between the inductor size and switching losses. The resonant frequency of the *LCL*-filter should be chosen such that it is in the range $10\omega_0 \leq \omega_{res} \leq (\omega_{switch}/2)$ to avoid resonance problems, where ω_0 is the utility frequency (rad/s), ω_{res} is the switching frequency (rad/s) and ω_{switch} is the switching frequency (rad/s) [10].

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{2.7}$$

The resonant frequency of *LCL* filter is given using 2.7. Usually L_1 and L_2 have the same values, but the inductor in the grid side should be lower than L_1 because it's necessary to consider the grid inductor.

2.4.4 Design of filters

In order to design the values of *LC* and *LCL*-filter, it's useful to use an interactive approach due to the considerations of resonance damping, reactive power compensations, harmonic attenuation limits, etc [6]. As literature suggests, a properly designed filter should have the following characteristics:

1. minimum voltage drop across the filter;
2. minimum stored energy in the filter;
3. minimum reactive power produced by *LCL*-filter capacitor;
4. high-power-factor operation;
5. robust to external parameter variations such as grid impedance;
6. improved damping performances;
7. minimum damping losses in the damping scheme;
8. low electromagnetic interference;
9. robust to parameter variations due to aging.

In this thesis, the used values are chosen implementing a Matlab code to follow the previously characteristics.

2.5 Characteristics of the power converters and filters

In this section the parameters for the power converter, filters and loads are presented. Matlab-Simulink is the software used to implement all the models.

The system is made by three parts: power converter, filter and load. For this reason the datas are listed in three different tables. The design targets of the three-phase four-leg inverter are presented in the following table 2.1:

Table 2.1: Nominal Values of Power converter

Variable		value
PWM carrier frequency	f_{sw}	10 kHz
Grid frequency	f_g	50 Hz
DC-link Voltage	V_{DC}	800 V
DC-link Capacitors	C_T and C_B	500 μF
Neutral Inductor	L_n	90 μH

The table 2.2 shows the values of *LC* and *LCL* filters:

Table 2.2: Values of Filters

Variable	LC		LCL	
Inverter side inductor	L	210 μH	L_i	210 μH
Inverter side resistor	R	0,01 Ω	R_i	0,01 Ω
Grid side inductor	-	-	L_g	130 μH
Grid side resistor	-	-	R_g	0,01 Ω
Capacitor filter	C_f	200 μH	C_f	200 μH
Damping resistor	R_f	0,0001 Ω	R_f	0,0001 Ω

L_i and L_g usually have same values. In this case the values are different because of the consideration of the grid inductor.

The power converters models are simulated connecting two possible three-phase loads: balanced and unbalanced load. Using balanced load, the output voltage will not unbalance because of the absence of unbalanced current, which includes -50 Hz component. With unbalanced load, the output voltage will be unbalanced. In this way it's possible to compare the difference and verify the exact operating of the controllers.

The values of the three-phase loads are 2.3:

Table 2.3: Balanced and Unbalanced Three-phase loads

	balanced load	unbalanced load
R_a	10	50
R_b	10	10
R_c	10	5

Chapter 3

Control objectives

3.1 Introduction

In this chapter, the control problem as well as potential configurations for the controllers are discussed.

The main goal of the control is to provide a perfectly balanced three-phase output voltage, with low distortion under all the possible load conditions. This refers both to line (phase-to-phase) voltages as well as phase (phase-to-neutral) voltages. Unbalanced three-phase loads will produce unbalanced phase currents, eventually resulting in a negative sequence component in the voltage vector. On the other hand, single phase loads will produce currents in the neutral wire, which results in oscillations in the neutral voltage, and produces errors in the phase-to-neutral voltages therefore. Consequently, proper control of the three-phase four wires power converter implies, at least, control of the positive, negative and zero sequence voltages.

Since the voltage value is forced by the control, the current will change to achieve the voltage targets. Consequently, the voltage loop will include an inner current loop, using the grid current.

For the analysis following, all the voltages are measured with respect the ground connected with the inductor L_n, the middle point of filter and the middle point of the unbalanced load, and the used current is the current out of the inverter, depicted from fig. 2.2.1 to 2.2.8 in the Chapter 2.

All voltages are measured with respect the ground connected with the inductor L_n, the middle point of filter and the middle point of the unbalanced loads.

Figure 3.2.1: Open-loop control system: without feedback

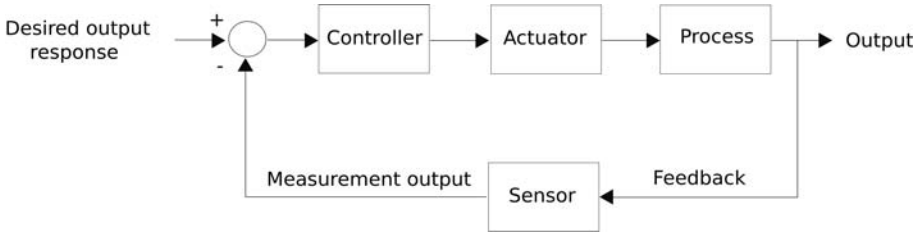


Figure 3.2.2: Closed-loop control system: with feedback

3.2 Control configuration

A control system is an interconnection of components forming a configuration that will provide a desired response. There are essentially two categories of control systems: open-loop and closed-loop.

An open-loop control system is designed to meet the desired goals by using a reference signal and an inverse model to drive the actuators feeding the system. As there is no feedback, and therefore no error term, they are fully driven by the reference 3.2.1.

A closed-loop control system measures of the actual output which is compared with the desired response. The resulting error signal is processed by the regulator to produce the error signal feeding the actuator [4]. This is shown in fig. 3.2.2.

A feedback control system is a control system that tends to maintain a prescribed relationship of one system variable to another by comparing functions of these variables and using the difference as a means of control. With an accurate sensor, the measured output is a good approximation of the actual output of the system [1].

3.3 Controller design

A key element in closed-loop control system is the controller. The controller receives the error signal, and decides the control action being commanded to the system by means of the actuator.

PID (Proportional- Integral-Derivative) and PR (Proportional-Resonant) are widely used in electronic power converters. A PID controller applies a correction based on proportional, integral and derivative terms (denoted P, I and D respectively). A PR controller applies a correction based on proportional and resonant terms (denoted P and R).

These actions are briefly discussed following.

3.3.1 P

The proportional (P) action connects the input and the output algebraically with a constant value K_P, called proportional gain. In this case, the attenuation is proportional to the error between the reference value and the measured value. P produces an instantaneous response to error, but in general, using only a P controller the system will have steady state error.

3.3.2 I

The integral (I) action integrates the error. The principle characteristic is to eliminate the error in the steady state. The reason for this is the infinite gain at DC. The integral part has a slow response to the error, but if the system is stable, it will guarantee zero steady state error. Contrary to most of the systems, in AC systems variables in steady state are sinusoidal. This means that integral action will fail to achieve zero steady-state error if it is implemented in a stationary frame.

3.3.3 D

The derivate (D) action produces an output which is proportional to the derivative of the error with respect to time. D acts only during the transient, as in steady-state the derivatives are normally zero. It improves the dynamic response and the stability of the system. A concern for this action is that if the signals are contaminated with high frequency noise, the D action will amplify this noise.

3.3.4 R

The resonant (R) part is similar to the integral I component, but instead of having an infinite gain at DC (and therefor guaranteeing zero steady-state error at DC), they do it at the resonance frequency.

3.3.5 Type of used controllers

Combining each of the terms, the result is to get different controllers with different characteristics.

PD

A PD is the combination of the proportional part P and the derivative D. The transfer function of a PD is 3.1:

$$G_{\mathrm{PD}}(s) = K_{\mathrm{P}} + K_{\mathrm{D}} s \tag{3.1}$$

PD controllers are advisable in general for the case of systems suffering from excessively oscillatory or even unstable behaviours.

PI

The Proportional-Integral algorithm PI controller is the combination of the proportional part and the integral part. The transfer function of PI is 3.2:

$$G_{\mathrm{PI}}(s) = K_{\mathrm{P}} + \frac{K_{\mathrm{I}}}{s} \tag{3.2}$$

PI controllers guarantee zero steady state error, this is the reason why they are used very often in industry. Unfortunately, PI controllers often worse the stability of a system. Consequently, their implementation and tuning must be carefully addressed.

As just said, the integral action will fail to achieve zero steady-state error with AC variables if it is implemented in a stationary reference frame. Generally, there are two implementations to overcame this problem:

- use a PI in the synchronous reference frame (using for example the Park's transformation);
- use a resonant controller in the stationary reference frame.

In this way, a synchronous PI controller is equivalent to a resonant controller in the stationary reference frame.

PID

Generally speaking, in a PID controller P gain usually influences how fast the systems can response, D is used to reduce the magnitude of the overshoot, and I-controller used to eliminate the steady- state error. The transfer function of the controller is shown in 3.3:

The transfer function of a PID is 3.3:

$$G_{\mathrm{PID}}(s) = K_{\mathrm{P}} + \frac{K_{\mathrm{I}}}{s} + K_{\mathrm{D}} s \tag{3.3}$$

The parameters are K_P, K_I, K_D and they are called three degrees of liberty of the controller.

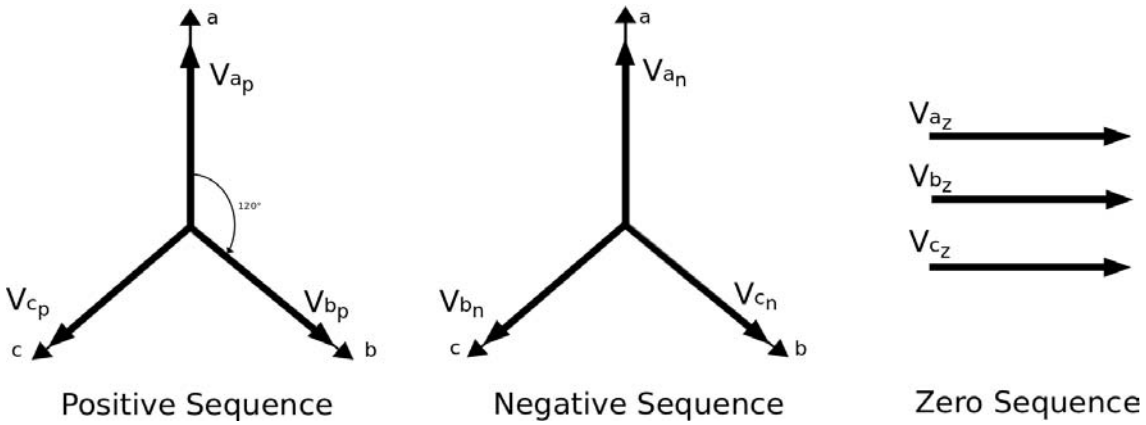


Figure 3.4.1: Sequence component phasors of three unbalanced phasors

PR

The Proportional-Resonant controller PR aims to get a good reference tracking and to reduce the output voltage harmonic distortion when the inverter feeds linear and nonlinear loads. The resonant controller is a generalized PI controller that is able to control not only DC but also AC variables. The transfer function is given by 3.4:

$$G_{\mathrm{PR}}(s) = K_{\mathrm{P}} + K_{\mathrm{I}} \frac{s}{s^2 + \omega^2{}_{\mathrm{o}}} \tag{3.4}$$

where ω_{o} is the resonant frequency to attenuate in [rad/s], K_{P} and K_{I} are the two degrees of liberty of the controller.

3.4 Positive, Negative sequences

Control strategies, used in three-phase AC power converters, strongly depend on whether the system is balanced or unbalanced. Symmetrical components are a power tool in this case, they are briefly discussed following.

3.4.1 Symmetrical component analysis

An unbalanced set of three-phase phasors, according to symmetrical component analysis proposed by C. L. Fortescue in 1918, can be decomposed into three sets of balanced three-phase variables, namely, positive sequence component, negative sequence component and zero sequence component, respectively, as shown in 3.4.1 [13].

Using three-phase quantities *abc* in a stationary reference frame, where phase *a* leads phase *b* by 120° and phase *b* leads phase *c* by

120°, it's possible to define:

- positive sequence component which consists of three voltage phasors, designated by Va_p, Vb_p, and Vc_p, of equal magnitude, displaced from each other by 120° in phase angle, namely Va_p leads Vb_p by 120°, Vb_p leads Vc_p by 120°;
- negative sequence component consisting of three voltage phasors, designated by Va_n, Vb_n, and Vc_n, which are equal in magnitude, displaced from each other by 120° in phase angle and namely Va_n lags Vb_n by 120°, Vb_n lags Vc_n by 120°;
- zero sequence component consisting of three voltage phasors, designated by Va_z, Vb_z, Vc_z, which are equal in magnitude and without phase displacement from each other.

The voltage phasor of each phase is the sum of its positive, negative and zero sequence components,

$$Va = Va_p + Va_n + Va_z \tag{3.5a}$$
$$Vb = Vb_p + Vb_n + Vb_z \tag{3.5b}$$
$$Vc = Vc_p + Vc_n + Vc_z \tag{3.5c}$$

From the definition of positive and negative sequence components and defining the operator $\alpha = \angle 120$ ($\alpha^2 = \angle 240$), the following relations are obtained:

$$Vb_p = \alpha^2 Va_p \tag{3.6a}$$
$$Vc_p = \alpha Va_p \tag{3.6b}$$

$$Vb_n = \alpha Va_n \tag{3.7a}$$
$$Vc_n = \alpha^2 Va_n \tag{3.7b}$$

From the definition of zero sequence, it's known that:

$$Va_z = Vb_z = Vc_z \tag{3.8}$$

Now, substituting equations 3.8, 3.6 and 3.7, a system of equations 3.5 can be rewritten as 3.9,

$$Va = Va_z + Va_p + Va_n \tag{3.9a}$$
$$Vb = Vb_z + \alpha^2 Vb_p + \alpha Vb_n \tag{3.9b}$$
$$Vc = Vc_z + \alpha Vc_p + \alpha^2 Vc_n \tag{3.9c}$$

Solving this system of linear equations, positive, negative and zero sequences of phase ground voltage are obtained:

$$Va_{\mathrm{z}} = \frac{1}{3}(Va + Vb + Vc) \tag{3.10a}$$

$$Va_{\mathrm{p}} = \frac{1}{3}(Va + \alpha Vb + \alpha^2 Vc) \tag{3.10b}$$

$$Va_{\mathrm{n}} = \frac{1}{3}(Va + \alpha^2 Vb + \alpha Vc) \tag{3.10c}$$

Looking at the equation 3.10, it's clear that the zero sequence components are one third of the sum of three phase vectors.

3.4.2 Park's transformation

Generally, the references of the control are selected based on the control objective. In this case, just looking at positive and negative sequences, the objectives are:

- to make the positive sequence voltage equal to the reference vector $\mathbf{V}_{\mathrm{dq0}}{}^{\mathrm{p}}$, where p means positive sequence, that in this case will be equal to

$$\mathbf{V}_{\mathrm{dq0}}{}^{\mathrm{p}} = \begin{bmatrix} V_{\mathrm{d}} \\ V_{\mathrm{q}} \\ V_0 \end{bmatrix} = \begin{bmatrix} V^* \\ 0 \\ 0 \end{bmatrix} \tag{3.11}$$

- to make the negative sequence voltage as closer as possible to zero, to minimize (or totally eliminate) the voltage imbalance. This means that the reference vector $\mathbf{V}_{\mathrm{dq0}}{}^{\mathrm{n}}$, where n means negative sequence, is equal to

$$\mathbf{V}_{\mathrm{dq0}}{}^{\mathrm{n}} = \begin{bmatrix} V_{\mathrm{d}} \\ V_{\mathrm{q}} \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.12}$$

In order to realize the controller design, the stationary frame functions are transformed into a synchronously rotating *dq0* reference frame using Park's transformation. The *dq0* transform is made of the Park and Clarke transformation matrices. The Clarke transform converts vectors in the *abc* reference frame to $\alpha\beta\gamma$ reference frame. The Park transform converts vectors in the $\alpha\beta\gamma$ reference frame to the *dq0* reference frame [2].

Considering the matrix Park's transformation $\boldsymbol{T}_{\mathrm{P}}$ presented in 3.13

$$\boldsymbol{T}_{\mathrm{P}} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.13}$$

where:
- ω is the angular frequency of the electrical variables;
- t is the time;
- θ=ωt is the angle between the axis of phase *a* and the direct axis component *d*-axis.

To convert an *abc* referenced vector $\mathbf{u}_{\mathrm{abc}}$ to the *dq0* reference frame, the column vector signal must be pre-multiplied by the *dq0* transformation matrix:

$$\mathbf{u}_{\mathrm{dq0}} = \boldsymbol{T}_{\mathrm{P}}\mathbf{u}_{\mathrm{abc}}. \tag{3.14}$$

And, to convert back from *dq0* referenced vector $\mathbf{u}_{\mathrm{dq0}}$ to the *abc* reference frame, the column vector signal must be pre-multiplied by the inverse *dq0* transformation matrix:

$$\mathbf{u}_{\mathrm{abc}} = \boldsymbol{T}_{\mathrm{P}}{}^{-1}\mathbf{u}_{\mathrm{dq0}}, \tag{3.15}$$

where $\boldsymbol{T}_{\mathrm{P}}{}^{-1}$ is the inverse of $\boldsymbol{T}_{\mathrm{P}}$, and it's equal a 3.16:

$$\boldsymbol{T}_{\mathrm{P}}{}^{-1} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & sin(\omega t) & 1 \\ \cos(\omega t - \frac{2\pi}{3}) & \sin(\omega t - \frac{2\pi}{3}) & 1 \\ \cos(\omega t + \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} \tag{3.16}$$

Using Park's transformation is possible the voltage and current transformation from the $\mathbf{V}_{\mathrm{abc}}$ phase variables to the $\mathbf{V}_{\mathrm{dq0}}$ variables and from the $\mathbf{I}_{\mathrm{abc}}$ phase variables to the $\mathbf{I}_{\mathrm{dq0}}$, as shown in fig. 3.4.2 and 3.4.3, where:

- $\mathbf{V}_{\mathrm{dq0}}$= $[V_{\mathrm{d}}\ V_{\mathrm{q}}\ V_0]^T$ is the vector of signals $\mathrm{V}_{\mathrm{dq0}}$;
- $\mathbf{I}_{\mathrm{dq0}}$= $[I_{\mathrm{d}}\ I_{\mathrm{q}}\ I_0]^T$ is the vector of signals $\mathrm{I}_{\mathrm{dq0}}$;
- V_{d}, V_{q} and V_0 are the direct, quadrature and zero sequence components of the transformed voltage;
- I_{d}, I_{q} and I_0 are the direct, quadrature and zero sequence components of the transformed current;
- $\mathbf{V}_{\mathrm{abc}}$= $[V_{\mathrm{a}}\ V_{\mathrm{b}}\ V_{\mathrm{c}}]^T$ is the vector of signals $\mathrm{V}_{\mathrm{abc}}$;
- $\mathbf{I}_{\mathrm{abc}}$= $[I_{\mathrm{a}}\ I_{\mathrm{b}}\ I_{\mathrm{c}}]^T$ is the vector of signals $\mathrm{I}_{\mathrm{abc}}$;

In this specific case, θ is the angle between the axis of phase V_{a} and the direct axis component *d*-axis, and in this case in the angle of the grid voltage.

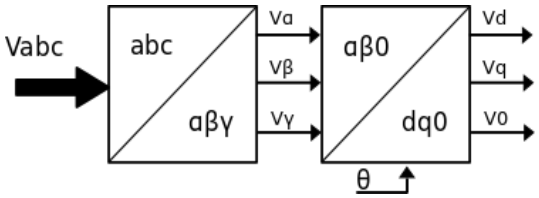


Figure 3.4.2: Voltage V_{abc}: Park's transformation

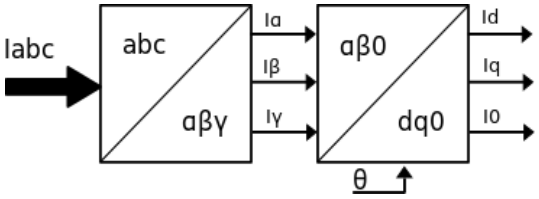


Figure 3.4.3: Current I_{abc}: Park's transformation

The transformation from the $\mathbf{V}_{abc}$ and $\mathbf{I}_{abc}$phase variables to the $\mathbf{V}_{dq0}$ and $\mathbf{I}_{dq0}$ variables can be written in the following matrix forms, as 3.18 for the voltages and 3.17 for the currents:

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.17}$$

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.18}$$

The following relations are obtained 3.19:

$$\mathbf{V}_{dq} = v_d + jv_q = \frac{2}{3}(v_a + v_b e^{-j\frac{2}{3}} + v_c e^{j\frac{2}{3}})e^{-j\omega t} \tag{3.19}$$

$$V_0 = \frac{1}{3}(v_a + v_b + v_c) \tag{3.20}$$

$$\mathbf{I}_{dq} = i_d + ji_q = \frac{2}{3}(i_a + i_b e^{-j\frac{2}{3}} + i_c e^{j\frac{2}{3}})e^{-j\omega t} \tag{3.21}$$

$$I_0 = \frac{1}{3}(i_a + i_b + i_c). \tag{3.22}$$

where v_d and i_d are the voltage and the current components in *d*-axis, v_q and i_q are in the *q*-axis, $\mathbf{V}_{dq}$ and $\mathbf{I}_{dq}$ are the complex vectors, as depicted in fig. 3.4.4.

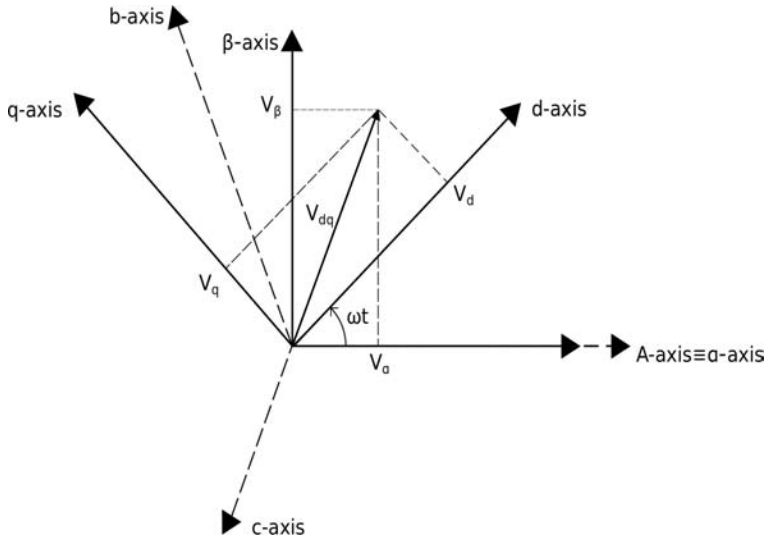


Figure 3.4.4: Park's transformation

3.4.3 Control of positive and negative sequence

In a first approach, to study the positive and negative controllers, the neutral path in the system will not be considered, i.e. it is assumed that $(V_a+V_b+V_c)=0$.

With unbalanced loads, the output voltage of three-phase converter will be unbalanced. However, it's possible to balance the voltage load and the amplitude controlling the amplitude of the positive sequence and eliminating the negative one.

The idea is to use the three-phase power converter as grid-forming power converter, which is controlled in closed-loop to work as ideal AC voltage source with a given voltage amplitude and frequency. A practical example of a grid-forming power converter can be a UPS. This system remains disconnected from the main grid when the operating conditions are within certain limits. In the case of a grid failure, the power converter of the UPS forms the grid voltage.

An example of a controller for a grid-forming power converter is shown in 3.4.5, which includes:

- DC-source. Usually, in industrial applications, DC voltage sources could be batteries, fuel cells, or another primary source;
- three-phase power converter, which could be one of the topologies studied in this thesis;
- filter, which could be *LC* or *LCL*;
- load, which could be three-phase balanced or unbalance, or one-single phase load.

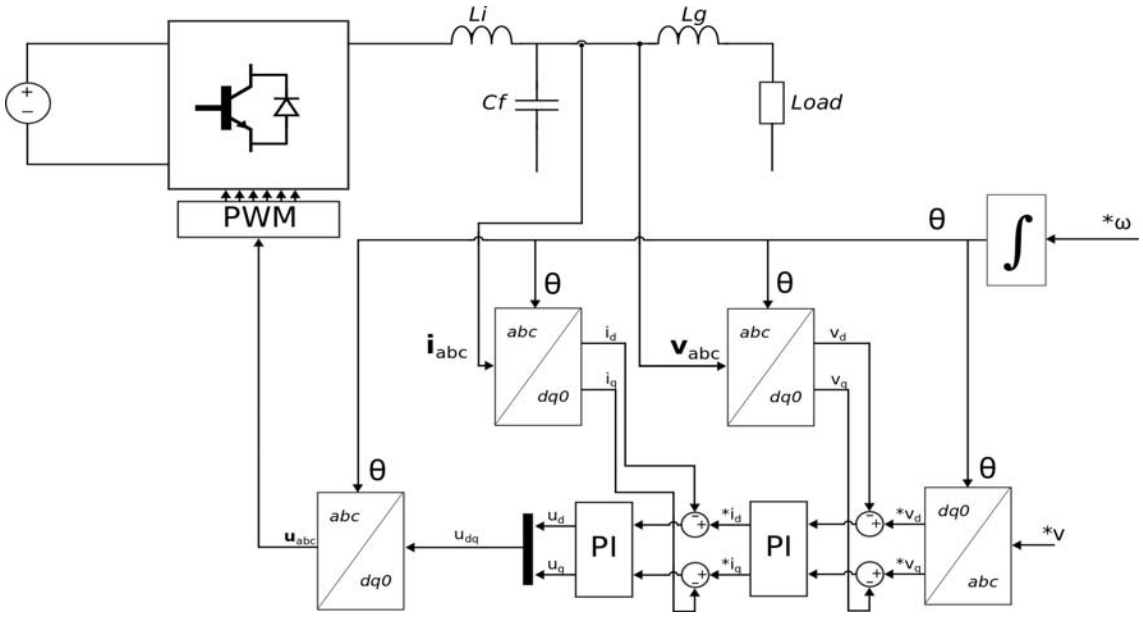


Figure 3.4.5: Basic control structure in a three-phase grid-forming voltage source inverter generating a sinusoidal voltage determined by a nominal voltage amplitude v^* and reference frequency ω^*, connected to a load

Synchronous reference frames are used: a positive-sequence voltage is regulated by a proportional integral controller in a positive synchronous reference frame (SRF) and a negative-sequence voltage is regulated by a PI controller in a negative synchronous reference frame. In the positive SRF, which rotates counter clockwise, the positive sequence appears as DC, while the negative sequence appears as 100 Hz, which is the double of the fundamental frequency. In contrast, the negative SRF, which rotates clockwise, the negative sequence appears as DC, while the positive sequence appears like 100 Hz. By deleting the 100 Hz components using a band-stop filter in each SRF, one can measure positive and negative sequence voltages separately, and use them for constructing two feedback controllers. Since the voltage control includes an inner current loop, the same is done for the current [12].

Control of the positive sequence voltage

Considering the positive sequence, the control is implemented by using two cascaded synchronous controllers working on the *dq0* reference frame, which rotates counter clockwise.

The inputs to the control system are the amplitude and the frequency of the voltage to be formed by the power converter. There is an external loop controls the grid voltage to match its reference value and an internal control loop which regulates the current supplied by the converter [11]. PI controllers are used because, thanks Park's transformation, it's

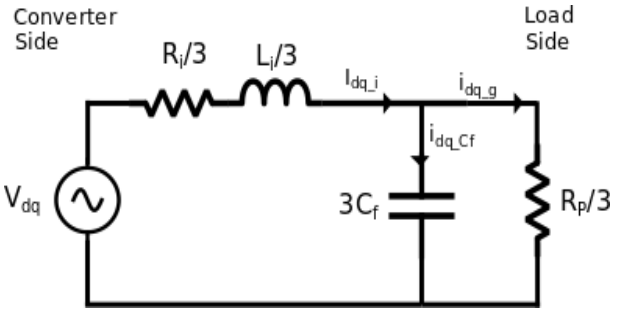


Figure 3.4.6: Three-Phase Power Converter and *LC*-filter: Equivalent circuit for positive sequence

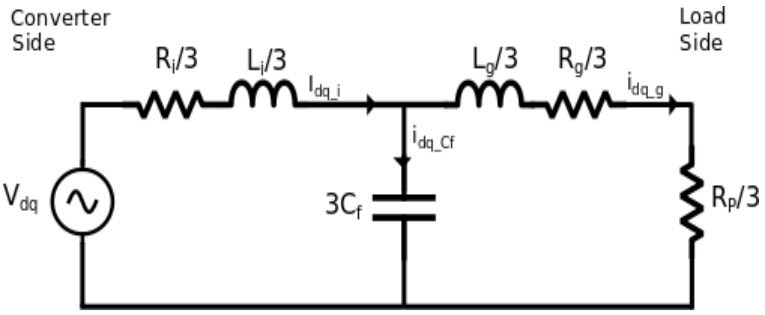


Figure 3.4.7: Three-Phase Power Converter and *LCL*-filter: Equivalent circuit for positive sequence

possible to work with DC variables and to eliminate the steady-state error.

The simplified model of power converter of each configuration is the same, 3.4.6 with *LC* filter and 3.4.7 with *LCL* filter. After applying the Park's transformation, instead of $\mathbf{V}_{abc}$ and $\mathbf{I}_{abc}$, $\mathbf{V}_{dq0}$ and $\mathbf{I}_{dq0}$ vectors will be used. The single-phase circuit is easy to obtain, just remember that L_g, L_i, C_f and the load are in parallel in the real physical system. For this reason, in the equivalent circuit the values of the inductors will be divided into the phases number and the capacitor will be multiplied by the same number. R_p is the load value in each phase, if it's a three-phase load.

In order to simplify the analysis, the main idea is to place the voltage vector $\mathbf{V}_{dq0}{}^{p}$ on the *d*-axis, as shown in 3.4.8, where $\theta=\omega t$ is the angle rotating counter clockwise and $\mathbf{V}_{dq0}{}^{p}$ is the reference vector for the positive sequence. Numerically it means:

$$\mathbf{V}_{dq0}{}^{p} = \begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \begin{bmatrix} V^* \\ 0 \\ 0 \end{bmatrix} \tag{3.23}$$

where V^* is the rated output voltage, fixed respect the *d*-axis.

The positive sequence control for *d* and *q* components is the same shown in fig. 3.4.5 using Proportional Integral controllers. In order to

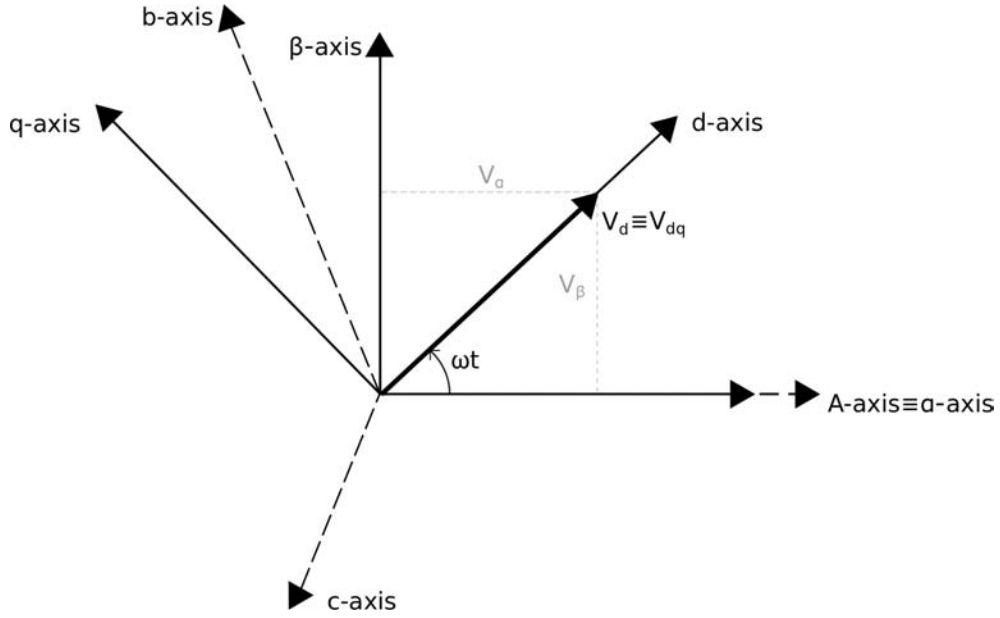


Figure 3.4.8: Positive sequence control in *dq0* reference frame

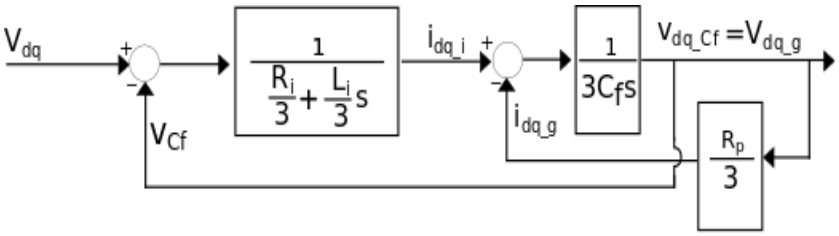


Figure 3.4.9: Block diagram with *LC*-filter in a *dq0* synchronous reference frame

tune the value K_P and K_I of the controllers, the block diagrams are considered, fig. 3.4.9 and 3.4.10.

Cancellation of the negative sequence voltage

In order to eliminate the negative sequence voltage, a feedback control is engaged.

As just said, in the positive SRF, which rotates counter clockwise, the negative sequence appears as 100 Hz, which is the double of the fundamental frequency. To have just DC variables and to use the same the same control loop used in the positive sequence, it could be convenient

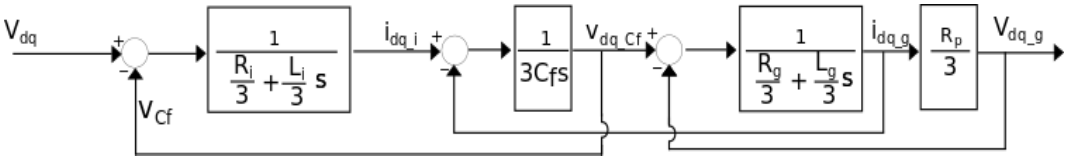


Figure 3.4.10: Block diagram with *LCL*-filter in a *dq0* synchronous reference frame

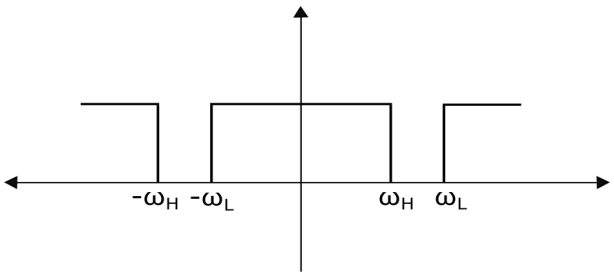


Figure 3.4.11: A generic ideal band-stop filter, showing both positive and negative angular frequencies

supress the 2ω ripple.

An easy way, as shown in fig. 3.4.12, is to apply, after the Park's transformation, a band-stop filter with natural frequency in 100 Hz. A band-stop filter is a filter that passes most frequencies unaltered, but attenuates those in a specific range to very low levels. The ideal characteristic of the band-pass filter is shown in fig. 3.4.11, where ω_L indicates the cut off frequency of the low pass filter and ω_H is the cut off frequency of the high pass filter. The centre frequencies are the frequencies blocked. In this way, the negative voltage control is similar to the positive voltage control, as depicted in fig. 3.4.12, just adding the band-stop filter after the Park's transformation.

Since the issue is to limit the effect of the unbalanced loads, the reference vector $\mathbf{V}_{dq0}{}^{n}$ will be:

$$\mathbf{V}_{dq0}{}^{n} = \begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{3.24}$$

The equivalent circuits are equal to the equivalent circuits for positive sequence, in fig. 3.4.6 and 3.4.7, consequently the block diagrams are the same, 3.4.9 and 3.4.10.

The study the zero voltage sequence will be presented in the follow section.

3.5 Zero Voltage Sequence and Four-Leg control

In this subsection, the tasks of each configurations will be presented.

The configurations with four legs has to generate firing pulses for the switches in the neutral leg. This is possible to realize in different ways. This is not necessary in the configuration with just the split DC capacitors.

In all the configuration is possible to control the zero sequence volt-

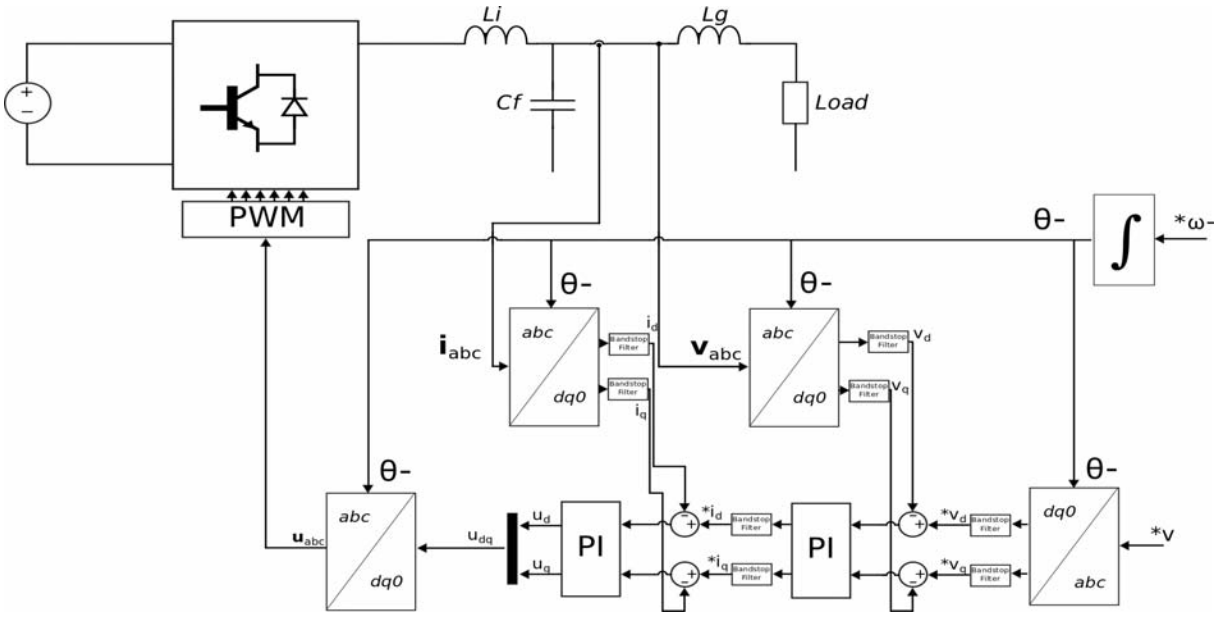


Figure 3.4.12: Basic control structure of negative sequence in a three-phase grid-forming voltage source inverter, connected to a load

age, which depends on the unbalances.

Generally speaking, in the control of neutral leg and zero voltage sequence, for the voltage loop, a proportional resonant controller will be used, which introduces an infinite gain at a selected resonant frequency ω_o, to eliminate the voltage harmonic at that frequency.

As already said, the transfer function of a PR controller is 3.25:

$$G(s) = K_p + \frac{K_i s}{s^2 + \omega^2{}_o} = \frac{K_p s^2 + K_i s + K_p \omega^2{}_0}{s^2 + \omega^2{}_o} = K_p \frac{s^2 + Ks + \omega^2{}_0}{s^2 + \omega^2{}_o} \quad (3.25)$$

where $K = \frac{K_i}{K_p}$, $\omega_o = 2\pi f_o$ and f_o is the frequency in [Hz] to attenuate.

An equivalent circuit can be obtained from the three-phase circuit when the voltage is symmetric and the current is balanced. This is possible when the load is balanced. Sometimes it's convenient to use the equivalent single-phase circuit because it's easier to study and voltage and current have same behaviours of the three-phase.

In order to verify if the system with the control is stable or not, it's useful to check the root locus of the system. Being the systems complex, it's not immediate to calculate the transfer function. Changing the controllers, the root locus changes and it could become instable. A system is stable if the poles of the transfer function have real part negative. This means that all the poles have to be in the right part of the root locus.

In a general case, the transfer function of a system is the ratio be-

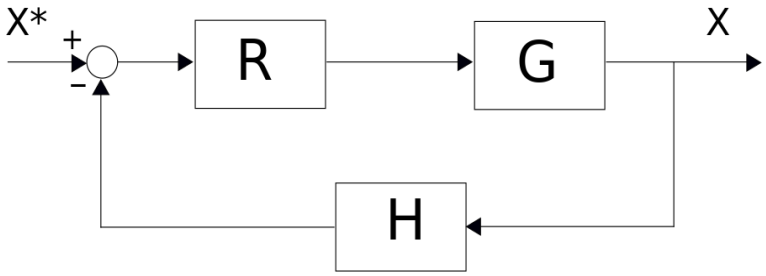


Figure 3.5.1: Generic block diagram with feedback

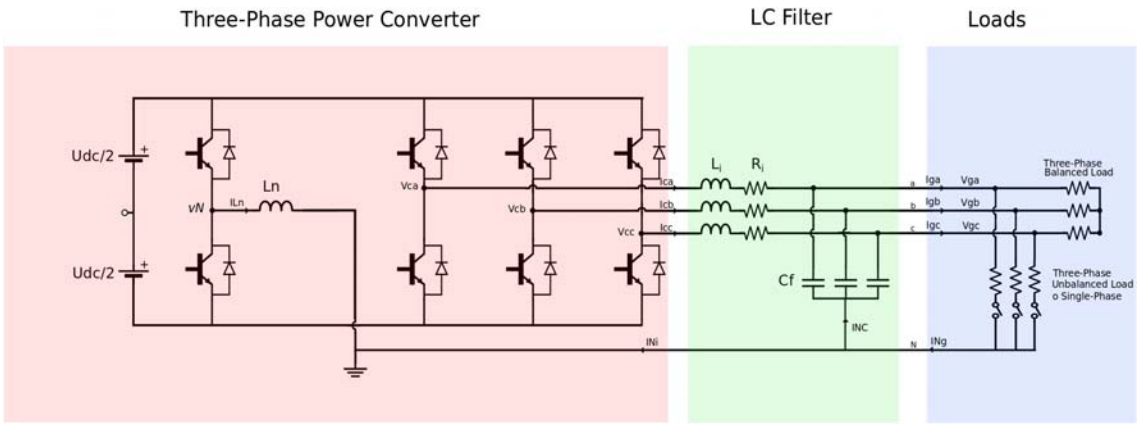


Figure 3.5.2: Three-Phase power converter with fourth leg, *LC* filter, balanced and unbalanced load without the capacitors in the DC-bus

tween the output X and the input X*, fig. 3.5.1, where:

- R is the transfer function of the regulator used;
- G is transfer function of the system which is needed to control;
- H is the transfer function of the feedback, that could be for example the transfer function of the transducer.

The transfer function of a generic case it will be 3.26:

$$\frac{X}{X*} = \frac{RG}{1 + RGH}. \tag{3.26}$$

To know if the system is stable, it's possible to look at the root locus of RGH, because if it is stable, all the system will be stable.

In order to study the zero sequence control and four-leg control is necessary to analyzs each single configuration alone because the equivalent circuits are different.

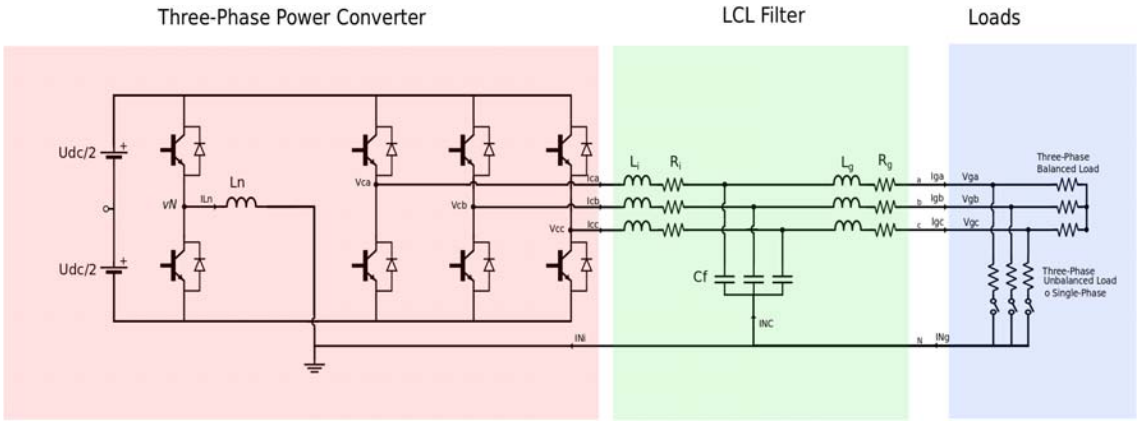


Figure 3.5.3: Three-Phase power converter with fourth leg, *LCL*-filter, balanced and unbalanced load without the capacitors in the DC-bus

Conventional Neutral Leg

As already said in the previous chapter, this configuration doesn't present the capacitors in the DC-bus, fig. 3.5.2 with *LC*-filter and 3.5.3 with *LCL*-filter.

Without the zero voltage sequence control Just controlling the positive and negative sequence, the situation is the following.

With a balanced load, the zero voltage sequence and fourth leg controls are not necessary because the positive and negative sequence are able to control and balance the output voltage. This is possible to see through the FFT of the grid voltage 3.5.4, in which there isn't -50 Hz component because the load is balanced and the 50 Hz component is equal to the target value imposed by the positive sequence.

The grid voltage waveform is shown in fig. 3.5.5 and it's perfectly balanced.

The FFT of zero sequence voltage is depicted in fig. 3.5.6. It doesn't present 50 Hz component because the load is balanced, but it has a big DC component, which is also presented in the neutral voltage, fig. 3.5.7

The situation is more complicated when unbalanced loads are connected to the inverter and however it's necessary to control the grid voltage. In this case, positive and negative sequence controls are not able to balance the grid voltage, 3.5.8. Like with balanced load, grid voltage hasn't -50 Hz thanks to the control of negative sequence, but there is an oscillation, as it's possible to see in fig. 3.5.9 due the presence of unbalanced loads connected to the grid.

In this case, not only a DC component is present, but also the oscillation of 50 Hz is possible to see in the FFT of zero voltage sequence and of neutral voltage, 3.5.10 and 3.5.11.

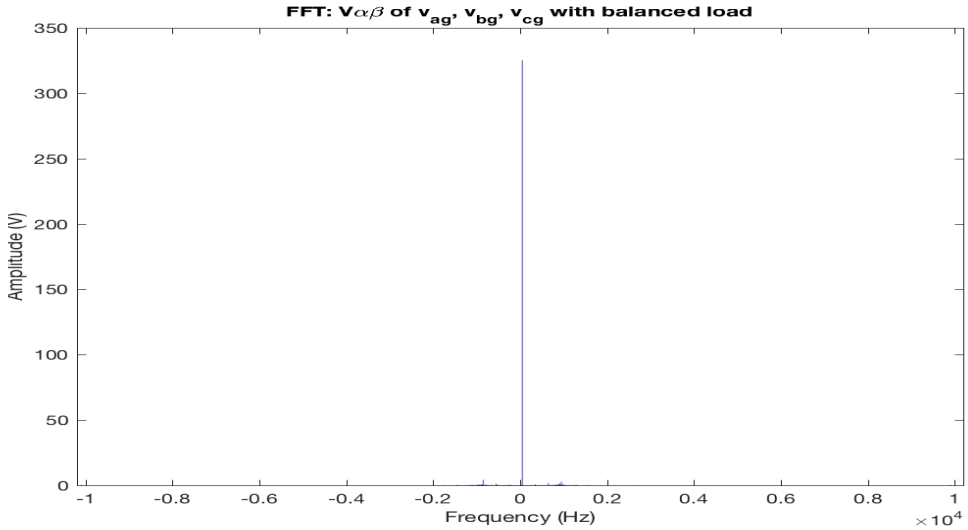


Figure 3.5.4: Conventional Neutral leg with balanced load: no zero voltage sequence and no neutral leg controls. Harmonic spectrum of inverter voltage with balanced load

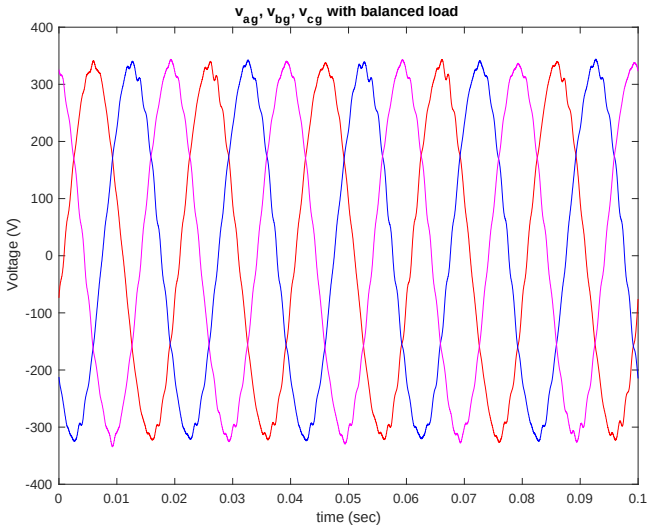


Figure 3.5.5: Conventional Neutral leg with balanced load: no zero voltage sequence and no neutral leg controls. Waveform of grid voltage with balanced load

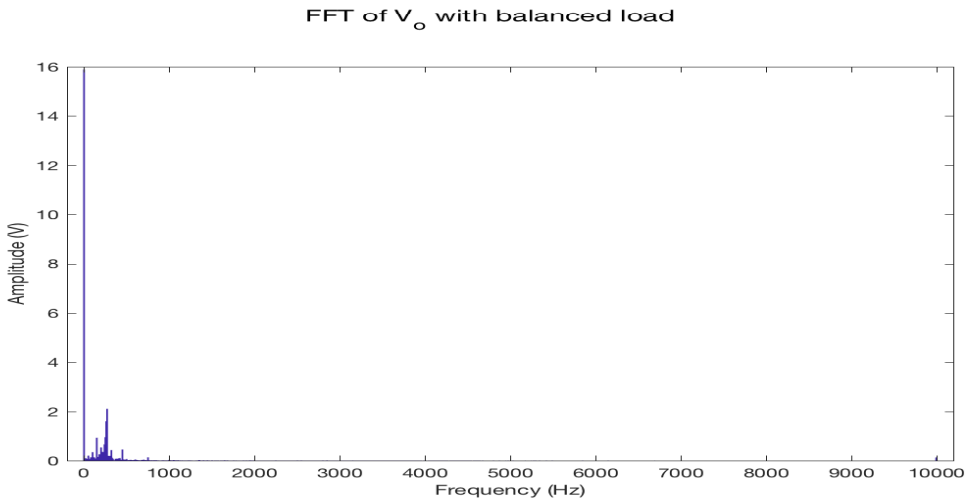


Figure 3.5.6: Conventional Neutral leg with balanced load: no zero voltage sequence and no neutral leg controls. FFT of zero voltage sequence with balanced load

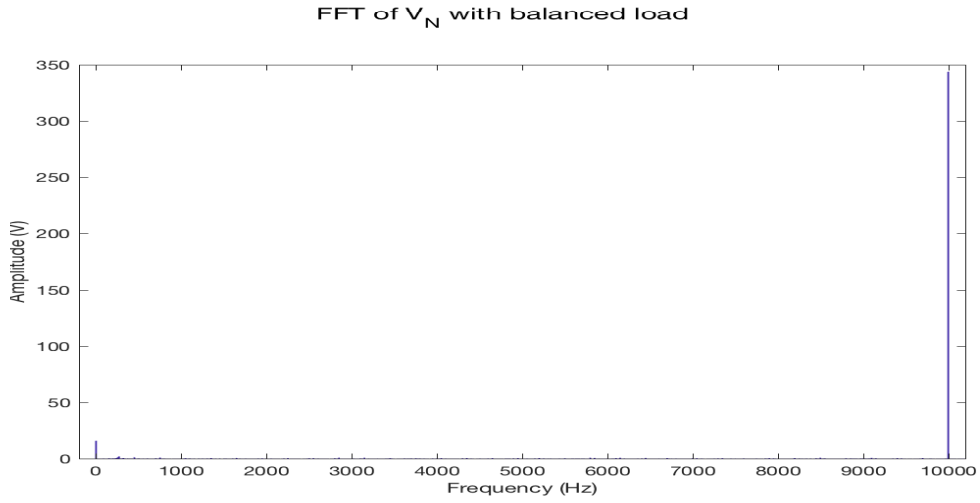


Figure 3.5.7: Conventional Neutral leg with balanced load: no zero voltage sequence and no neutral leg controls. FFT of neutral voltage with balanced load

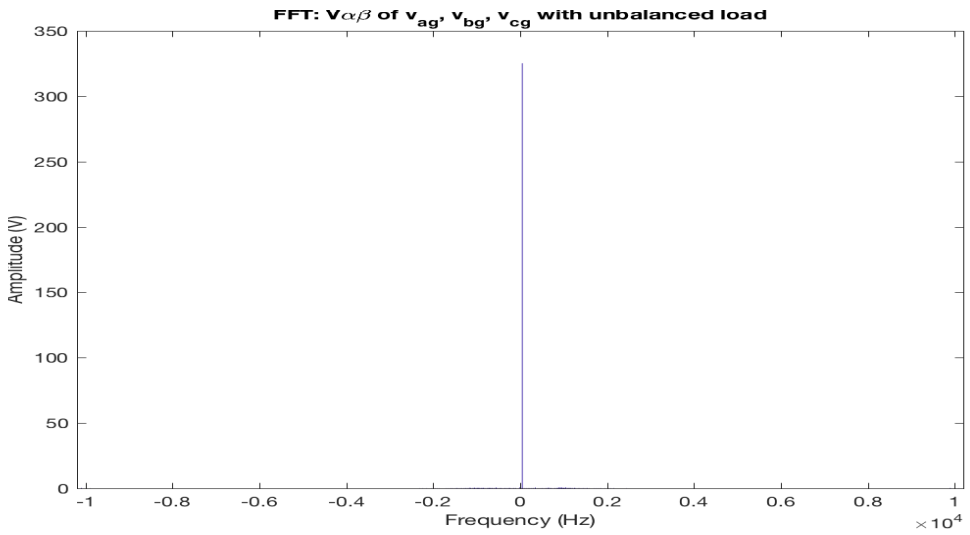


Figure 3.5.8: Conventional Neutral leg with unbalanced load: no zero voltage sequence and no neutral leg controls. Harmonic spectrum of inverter voltage with unbalanced load

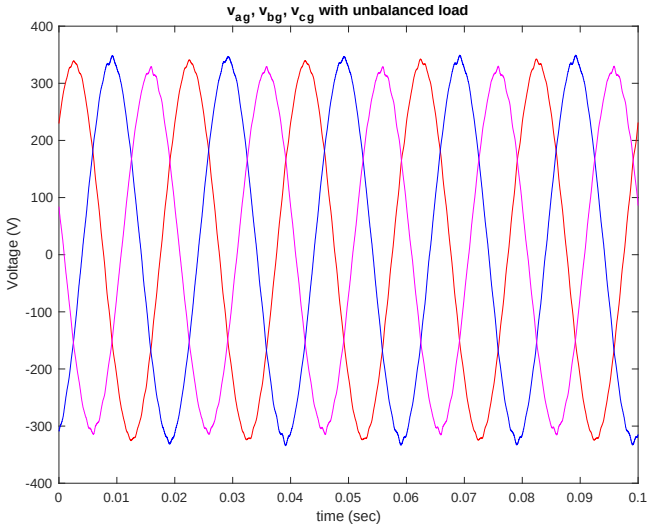


Figure 3.5.9: Conventional Neutral leg with unbalanced load: no zero voltage sequence and no neutral leg controls. Waveform of grid voltage with unbalanced load

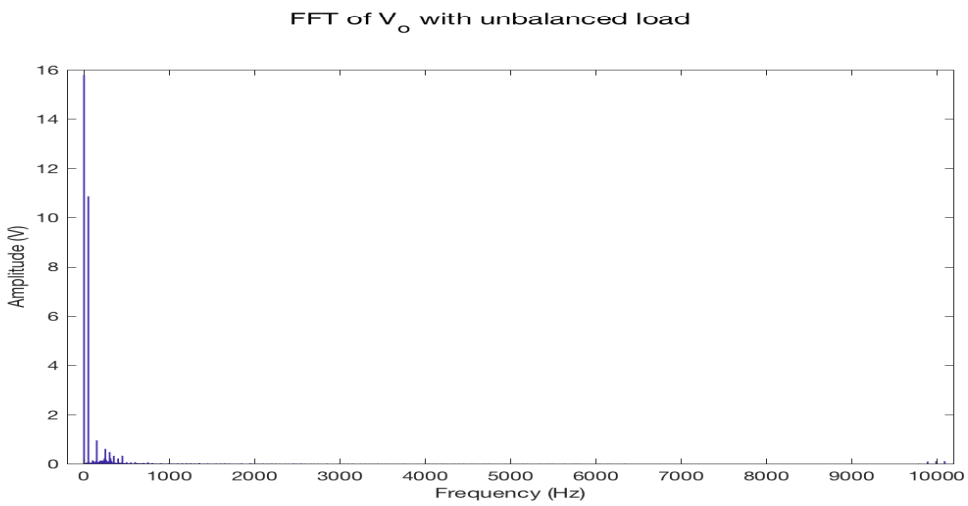


Figure 3.5.10: Conventional Neutral leg with unbalanced load: no zero voltage sequence and no neutral leg controls. FFT of zero voltage sequence with unbalanced load

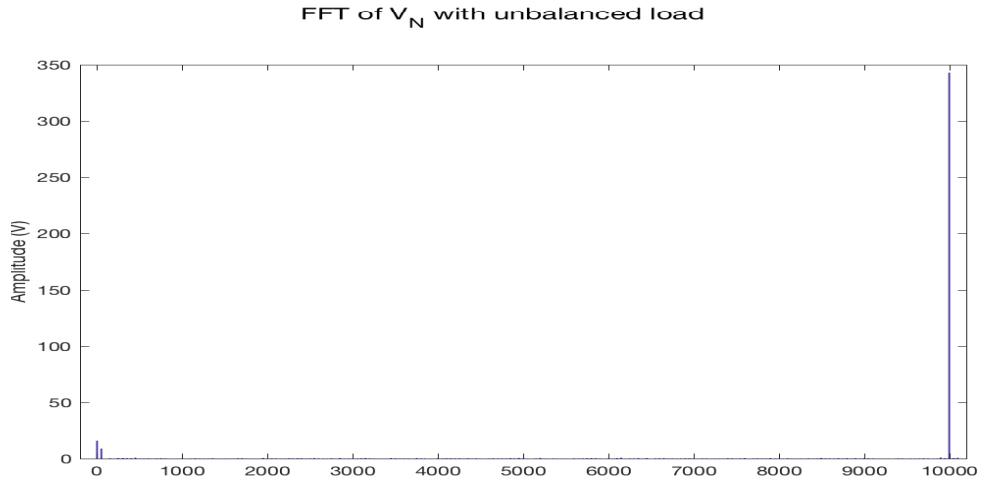


Figure 3.5.11: Conventional Neutral leg with unbalanced load: no zero voltage sequence and no neutral leg controls. FFT of neutral voltage with unbalanced load

Control Strategy The equivalent circuits are shown in 3.5.12, with *LC*-filter, and 3.5.13, with *LCL*-filter, remembering that L_i, C_f, L_g and the load are in parallel in the real physical model. U_{oi} is the zero voltage command of the zero voltage sequence of the output voltage, U_{Ni} is voltage command for the neutral voltage, L_n is the inductor presents in the neutral wire.

According to the Kirchhoff's laws and neglecting the resistors R_i and R_g, the following equations are obtained, firstly with *LC*-filter, 3.27 and secondly with *LCL*-filter, 3.28.

$$LC\text{-filter}\begin{cases} U_{oi} = \left(\frac{L_i}{3} + L_n\right)\frac{di_i}{dt} + V_{Cf} + U_{Ni} \\ V_{Cf} = \frac{R_l}{3} i_g \\ i_i = i_g + i_{Cf} \\ V_{Cf} = \frac{1}{3C_f}\int i_{Cf}\, dt \end{cases} \tag{3.27}$$

$$LCL\text{-filter}\begin{cases} U_{oi} = \left(\frac{L_i}{3} + L_n\right)\frac{di_i}{dt} + V_{Cf} + U_{Ni} \\ V_{Cf} = \frac{L_g}{3}\frac{di_g}{dt} + \frac{R_l}{3} i_g \\ i_i = i_g + i_{Cf} \\ V_{Cf} = \frac{1}{3C_f}\int i_{Cf}\, dt \end{cases} \tag{3.28}$$

The control objectives of this configuration are two:

- control of zero voltage sequence U_o of the output voltage of the power converter to reduce the effects of unbalances, using a PR in the voltage and current loops with the resonant frequency ω_o in 50 Hz;
- control of the neutral voltage, just controlling the voltage U_N, which is the voltage of the inductor L_n. The control is made just with a voltage loop, knowing that it's impossible the control of the current i_{LN} flowing through the inductor L_n because it's imposed by the system. The controller is a PR with the resonant frequency ω_o in 50 Hz.

Applying Laplace transform to the previous equations 3.27 and 3.28 and adding the control loops, it's easy to obtain the block diagrams 3.5.12 and 3.5.13.

In the voltage loop of zero sequence voltage control, the reference value U_o^* is compared with the zero voltage sequence U_o, that, as just

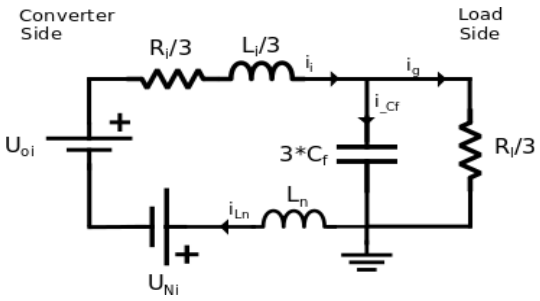


Figure 3.5.12: Three-Phase Power converter with fourth leg and *LC*-filter: equivalent circuit for zero voltage sequence and neutral voltage

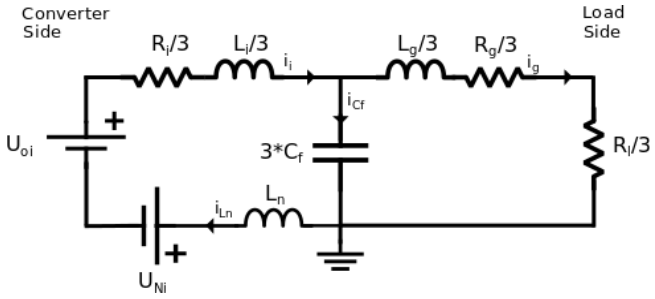


Figure 3.5.13: Three-Phase Power converter with fourth leg and *LCL*-filter: equivalent circuit for zero voltage sequence and neutral voltage

said, is one third of the sum of the output voltages *abc*. In the inner current loop, the current used is the current in the neutral path i_g, which could be the current in the grid (i_{Ng}) or in the inverter side (i_{Ni}), looking the physical system in fig. 3.5.2 and 3.5.3. U_N^* is the reference value of the voltage in the inductor L_n and U_N is the measured voltage.

Concerning the zero voltage sequence U_o, the transfer function of the system, including the controllers, is the ratio between the output, U_o, and the input, U_o^*, which is the reference value. The transfer function presents nine zeros and twelve poles.

The root locus is shown in fig. 3.5.16. How is possible to note in the figure 3.5.16b, all the poles are in the right side. This proves the stability

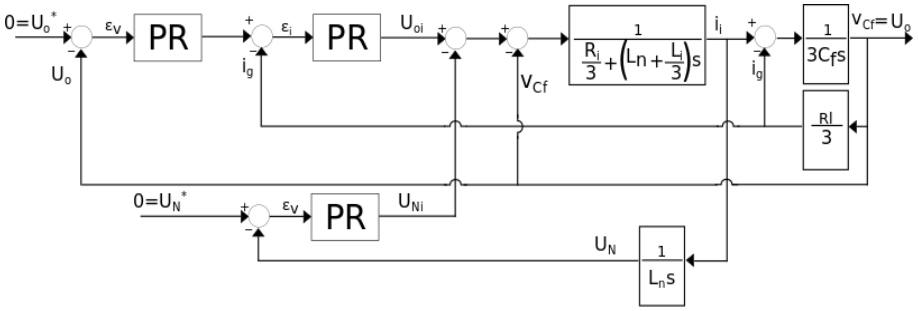


Figure 3.5.14: Three-Phase Power converter with fourth leg and *LC*-filter: Block diagram for zero voltage sequence and neutral voltage controls

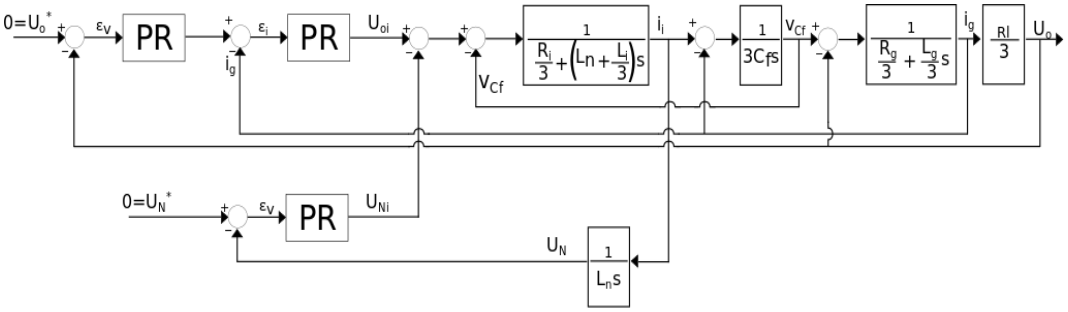
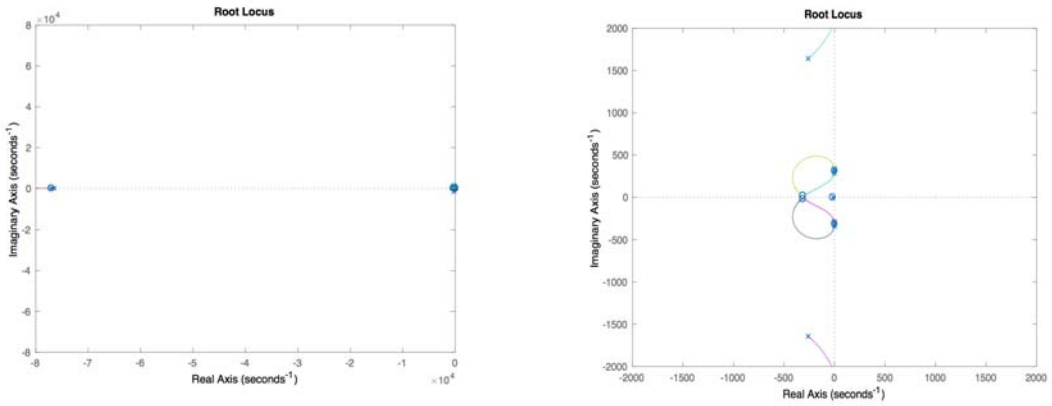


Figure 3.5.15: Three-Phase Power converter with fourth leg and *LCL*-filter: Block diagram for zero voltage sequence and neutral voltage controls



(a) **(b)**

Figure 3.5.16: Conventional Neutral Leg topology with *LCL*-filter: Root locus of transfer function $\frac{U_O}{U_O{}^*}$ in fig. (a) In fig. (b) a zoom in the critical part

of the system with the controllers chosen.

It possible to do the same just looking at the fourth leg control, calculating the transfer function which is the ration between U_N, which is the voltage of the inductor L_n, and U_N*, which is the target value.

Split DC-link Capacitors

The fourth leg doesn't belong to this configuration, as just seen in the previous chapter, 3.5.17 and 3.5.18. Consequently, the four-leg control is not necessary.

Without the zero voltage sequence control Just controlling the positive and negative sequence, the situation is the following.

With a balanced load, the zero voltage sequence control is not necessary because the positive and negative sequence are able to control the output voltage, without any unbalances. This is possible to see through the FFT of the grid voltage 3.5.19, in which there isn't -50 Hz component

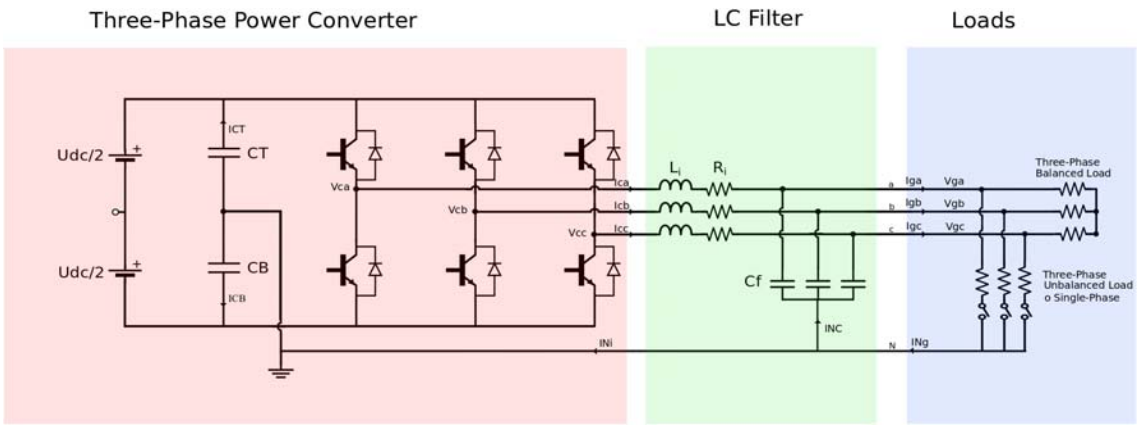


Figure 3.5.17: Three-Phase power converter with the capacitors in the DC-bus and neutral wire, *LC*-filter, balanced and unbalanced load

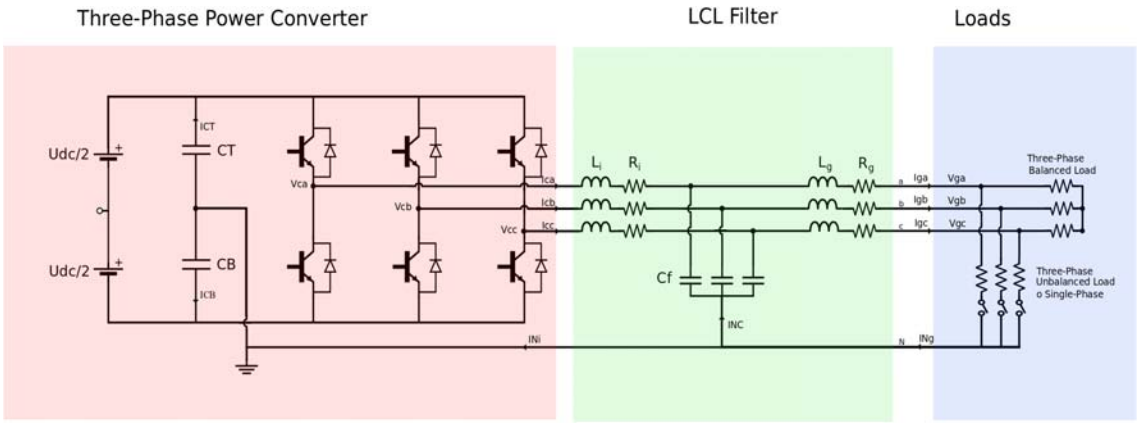


Figure 3.5.18: Three-Phase power converter with the capacitors in the DC-bus and neutral wire, *LCL*-filter, balanced and unbalanced load

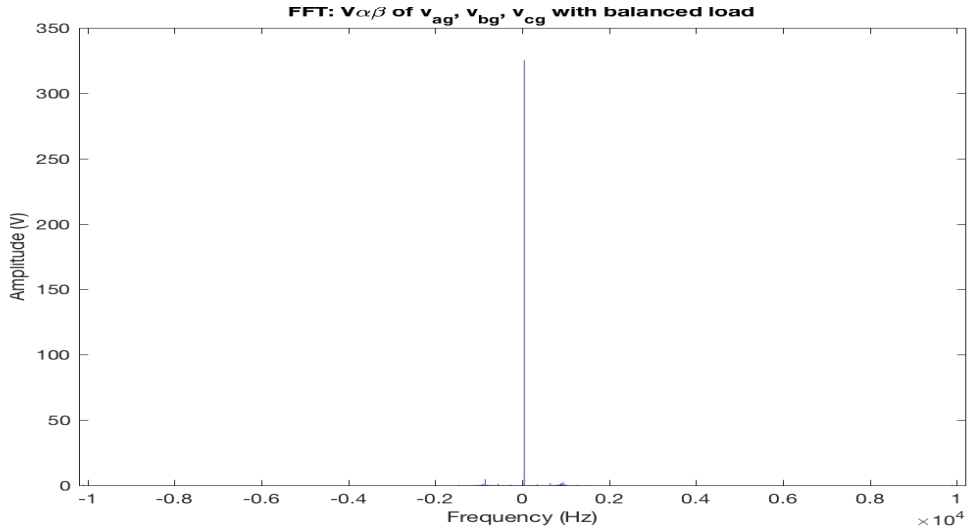


Figure 3.5.19: Split DC-capacitors with balanced load: no zero sequence voltage. Harmonic spectrum of grid voltage with balanced load

and the 50 Hz component is equal to the target value imposed by the positive sequence control.

The grid voltage waveform is shown in fig. 3.5.20.

The FFT of zero sequence voltage is depicted in fig. 3.5.21. It doesn't present 50 Hz component because the load is balanced.

When unbalanced loads are connected to this topology, positive and negative sequence controls are not able to balance the grid voltage, as shown in fig. 3.5.22. Anyway, it hasn't -50 Hz thanks to the control of negative sequence as it's possible to see in fig. 3.5.23.

The zero voltage sequence, with unbalanced load, has a oscillation at 50 Hz depicted in the FFT of zero voltage sequence in fig. 3.5.24

Control Strategy In this case, the issue is just the control of the zero voltage sequence U_o, using the equivalent circuits, fig. 3.5.25 with *LC*-filter and 3.5.26 with *LCL*-filter, remembering that L_i, C_f, L_g and the load are in parallel in the real physical model. U_o is the zero sequence voltage controlled and, as denied, is equal to $U_o = \frac{U_a+U_b+U_c}{3}$. Being in the physical system the capacitors in the DC-bus in parallel, in the equivalent circuit the equivalent capacitor has the double of the value, the load is one third of R_l, which is the real value of the load. Using Kirchhoff's laws and neglecting R_i and R_g, the systems 3.29 with *LC*-filter and 3.30 with *LCL*-filter are obtained.

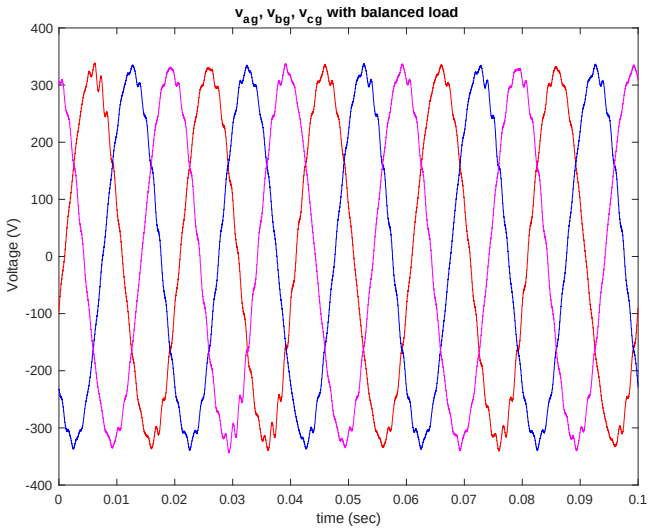


Figure 3.5.20: Split DC-capacitors with balanced load: no zero sequence voltage. Waveform of grid voltage with balanced load

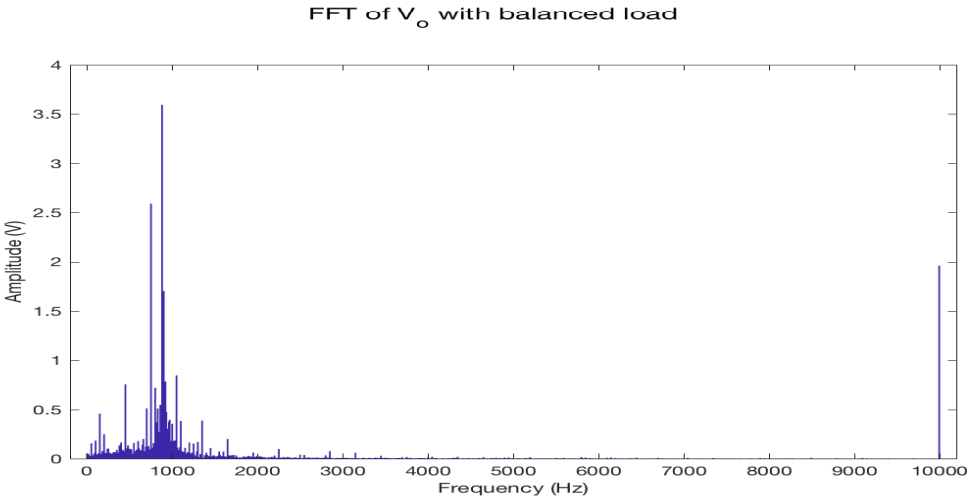


Figure 3.5.21: Split DC-capacitors with balanced load: no zero sequence voltage. FFt of zero voltage sequence with balanced load

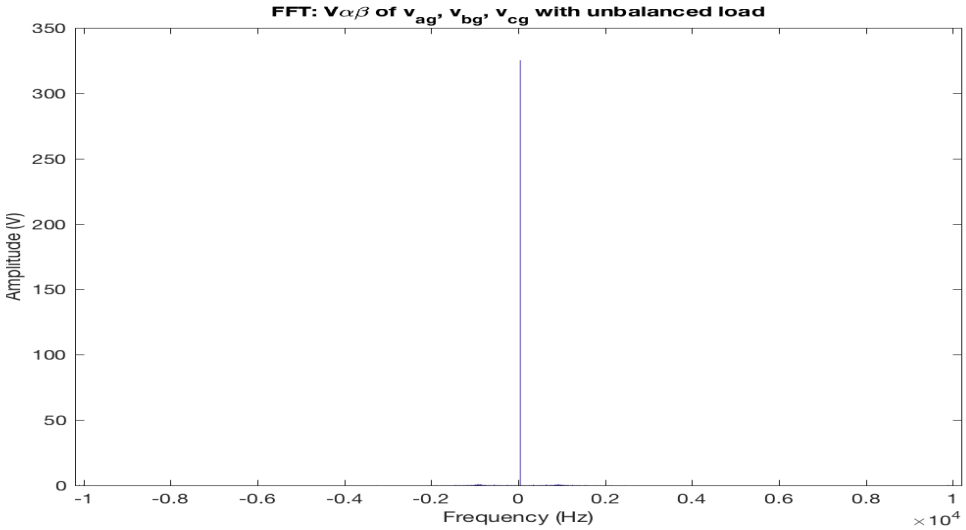


Figure 3.5.22: Split DC-capacitors with unbalanced load: no zero sequence voltage control. Harmonic spectrum of grid voltage with unbalanced load

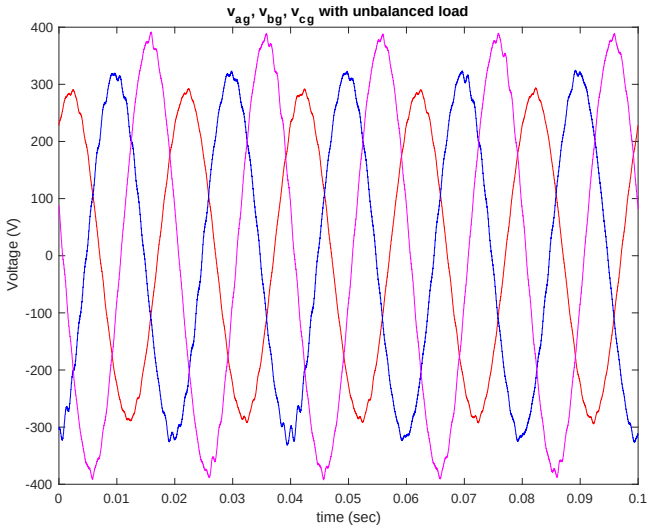


Figure 3.5.23: Split DC-capacitors with unbalanced load: no zero sequence voltage. Waveform of grid voltage with unbalanced load

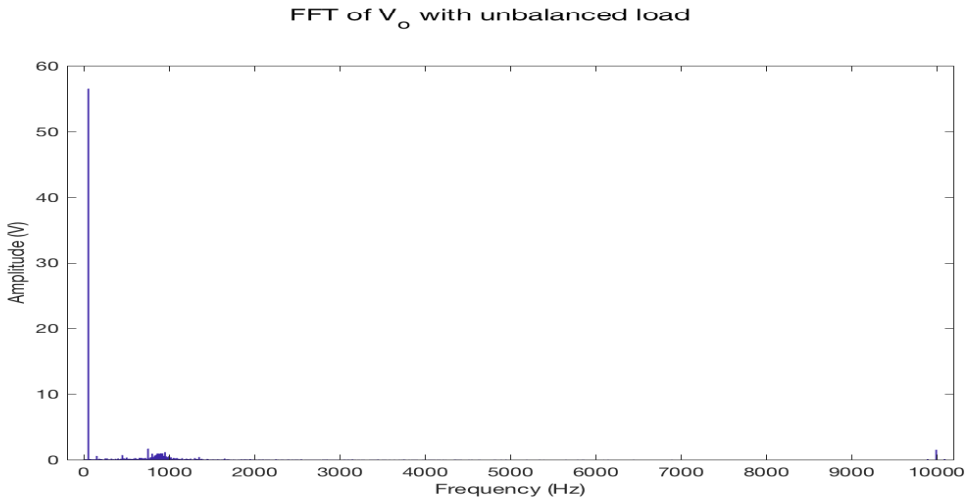


Figure 3.5.24: Split DC-capacitors with unbalanced load: no zero sequence voltage. FFT of zero voltage sequence with unbalanced load

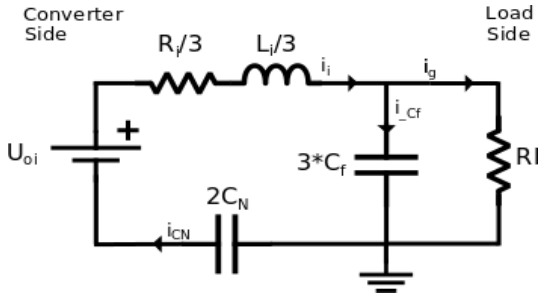


Figure 3.5.25: Three-Phase Power converter with slit DC-bus capacitors and *LC*-filter: equivalent circuit for zero voltage sequence

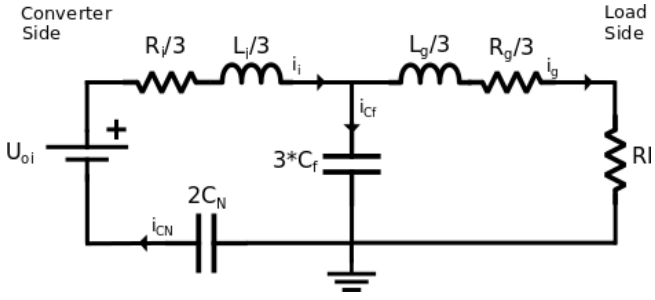


Figure 3.5.26: Three-Phase Power converter with slit DC-bus capacitors and *LCL*-filter: equivalent circuit for zero voltage sequence

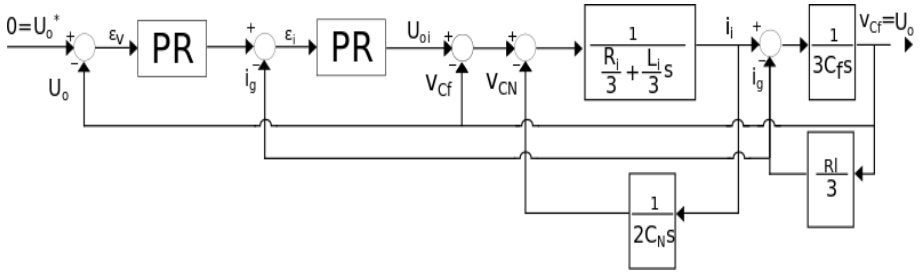


Figure 3.5.27: Three-Phase Power converter with split DC-link capacitors and *LC*-filter: Block diagram for zero voltage sequence control

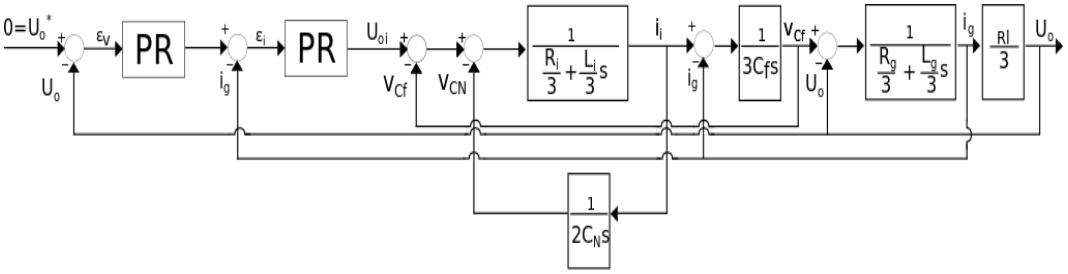


Figure 3.5.28: Three-Phase Power converter with split DC-link capacitors and *LCL*-filter: Block diagram for zero voltage sequence control

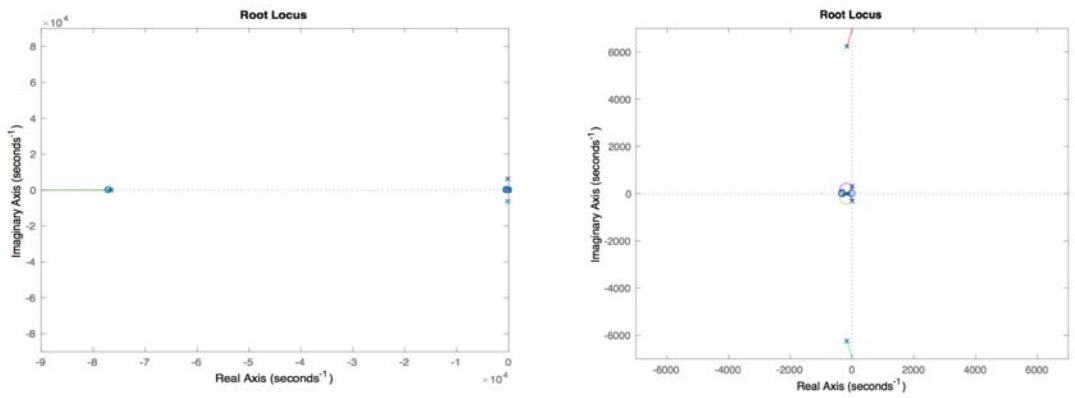
$$LC\text{-filter}\begin{cases} U_{oi} = \dfrac{L_i}{3}\dfrac{di_i}{dt} + V_{Cf} + V_{CN} \\ V_{Cf} = \dfrac{R_l}{3} i_g \\ i_i = i_g + i_{Cf} \\ V_{Cf} = \dfrac{1}{3C_f}\displaystyle\int i_{Cf}\, dt \end{cases} \tag{3.29}$$

$$LCL\text{-filter}\begin{cases} U_{oi} = \dfrac{L_i}{3}\dfrac{di_i}{dt} + V_{Cf} + V_{CN} \\ V_{Cf} = \dfrac{L_g}{3}\dfrac{di_g}{dt} + \dfrac{R_l}{3} i_g \\ i_i = i_g + i_{Cf} \\ V_{Cf} = \dfrac{1}{3C_f}\displaystyle\int i_{Cf}\, dt \end{cases} \tag{3.30}$$

where V_{Cf} is the voltage in the capacitor of the filter and V_{CN} is the voltage in the equivalent capacitors of the DC-link.

Following, with Laplace transformation, it's easy to develop the blocks diagrams, fig. 3.5.27 and fig. 3.5.28, including the control.

In order to attenuate the component at 50 Hz of zero voltage sequence of the output voltage of power converter, two PR are used, both



(a) **(b)**

Figure 3.5.29: Split DC-capacitors with unbalanced load: Root locus of transfer function $\frac{U_o}{U_o{}^*}$ in fig. (a). In fig. (b) a zoom of critical part

with resonant frequency ω_o equal to 50 Hz. One is used in the voltage loop and the other in the inner current loop. $U_0{}^*$ is the voltage reference and it's imposed to be equal to 0 in order to eliminate the 50 Hz oscillation, U_o is the voltage measured in the system and U_{oi} is the voltage command. In the current loop, the neutral current i_g is used, which could be in the inverter (i_{Ni}) or load (i_{Ng}) side in the physical system.

The transfer function of the system, including the controllers used in the zero voltage sequence and *LCL*-filter, is the ratio between the output, which is U_o, and the input $U_o{}^*$, which is the target value, and has six zeros and nine poles.

The root locus is shown in fig. 3.5.29. It's clear that, how shown in fig. 3.5.29b, that the system is stable because all the poles are in the left part of the root locus.

It's possible to say that the chosen values of the controllers don't destabilize the system.

Independently Controlled Neutral Leg

In this configuration, shown in fig. 3.5.30 and 3.5.31, zero voltage sequence and the fourth leg will be controlled.

Without the zero voltage sequence and neutral controls Just controlling the positive and negative sequence, the situation is the following.

The positive and negative sequence controls are able to control the output voltage with a balanced load. How it's possible to see in fig. 3.5.32, grid voltage hasn't -50 Hz component and the 50 Hz component is equal to the target value imposed by the positive sequence control.

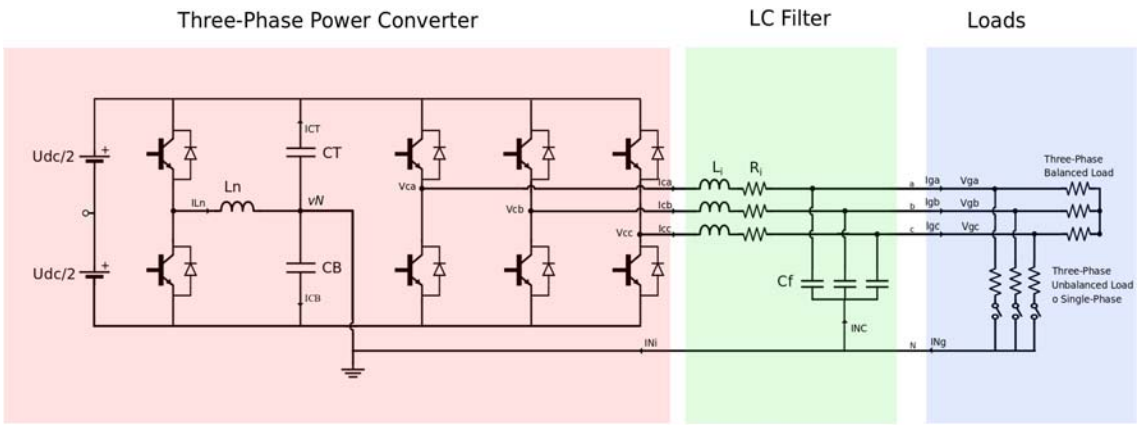


Figure 3.5.30: Three-Phase power converter with four legs and split capacitors in the DC-bus, *LC*-filter, balanced and unbalanced load

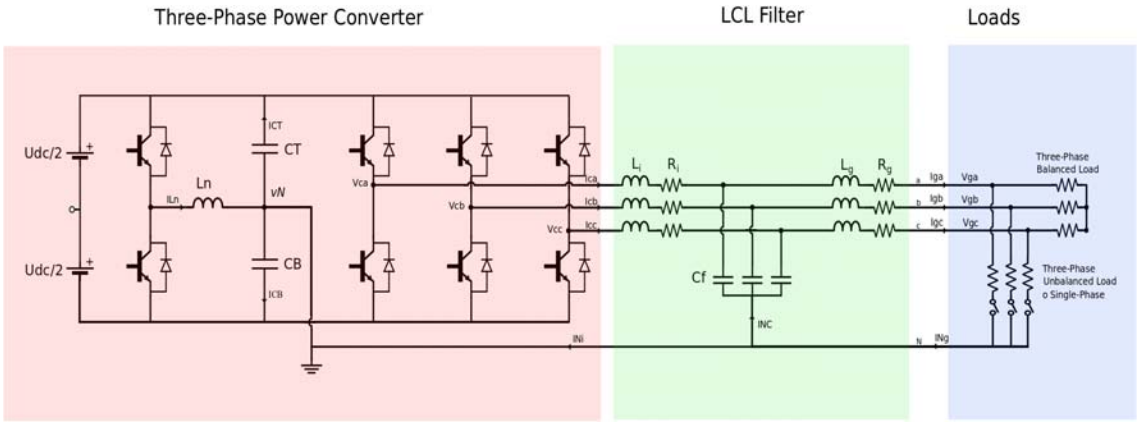


Figure 3.5.31: Three-Phase power converter with four legs and split capacitors in the DC-bus, *LCL*-filter, balanced and unbalanced load

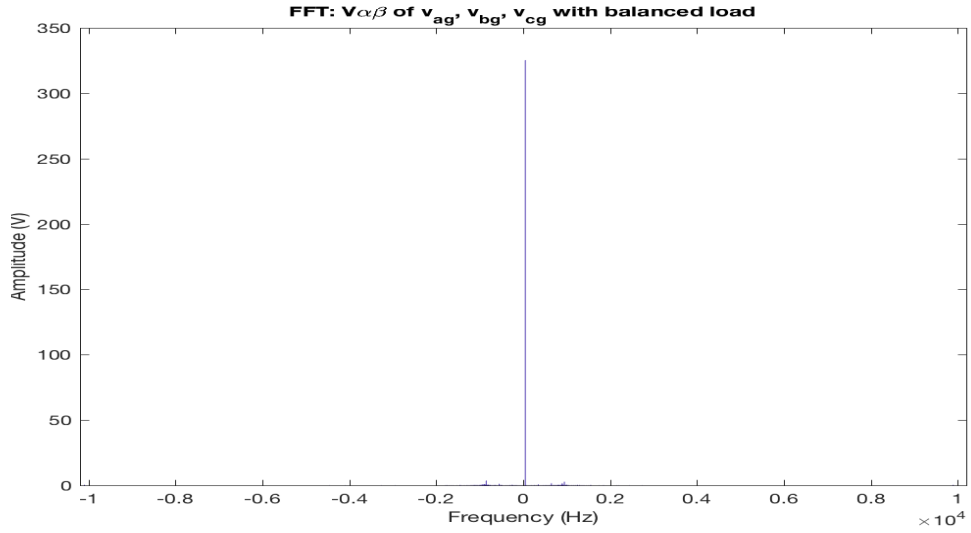


Figure 3.5.32: Independently Controlled Neutral Leg with balanced load: no zero sequence voltage and no neutral voltage control. Harmonic spectrum of grid voltage with balanced load

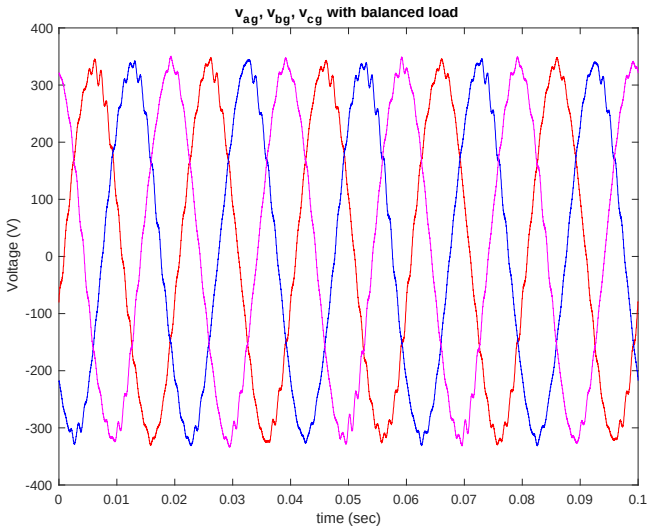


Figure 3.5.33: Independently Controlled Neutral Leg with balanced load: no zero sequence voltage and no neutral voltage control. Waveform of grid voltage with balanced load

The grid voltage waveform is perfect balances, as shown in fig. 3.5.33.

The zero sequence voltage hasn't 50 Hz component, as it is depicted in fig. 3.5.34. Contrarily, it has a big DC component, which is also equal in the neutral voltage, 3.5.35

Now, connecting an unbalanced load to the power converter, the voltage is unbalanced due to the unbalances of the loads. Once again, positive and negative sequence controls are able to achieve the target value of the voltage and eliminate the -50 Hz component, 3.5.36. Anyway, the grid voltage is not balanced, as shown in fig. 3.5.37 due the presence of unbalanced loads connected to the grid.

In this case, not only a DC component is present, but also a oscillation at 50 Hz is present, as it's possible to see in the FFT of zero voltage sequence and of neutral voltage in the fig. 3.5.38 and fig. 3.5.39.

Also, the current i_{CT}, which is the current through the DC-link capacitors, has a component at 50 Hz, depicted in fig. 3.5.40.

Control Strategy The equivalent circuits of the physical system with *LC* and *LCL* filters are shown in 3.5.41 and 3.5.42, respectively. The capacitor CT and CB have the same values and are in parallel. For this reason, in the equivalent circuit the equivalent capacitor's value is the double of the single capacitor's value. Assuming that CT=CB=C_N, the equivalent capacitor C_{eq} will be two times C_N. L_i, L_g, C_f and R_l are in parallel. U_{oi} is the voltage command of zero voltage sequence of the output voltage, U_{Ni} is the voltage command of the middle point voltage in the fourth leg that is necessary to balance in order to control the fourth leg, L_n is the inductor presents in the neutral wire.

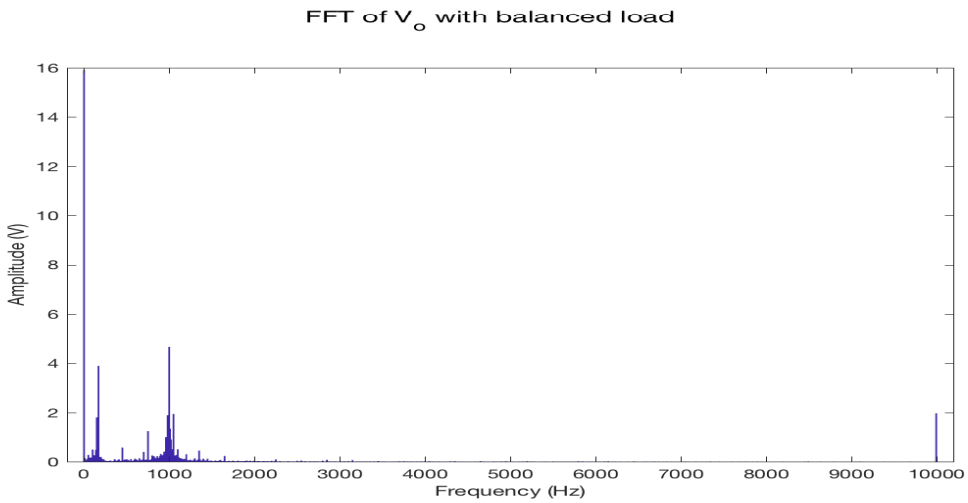


Figure 3.5.34: Independently Controlled Neutral Leg with balanced load: no zero sequence voltage and no neutral voltage control. FFT of zero voltage sequence with balanced load

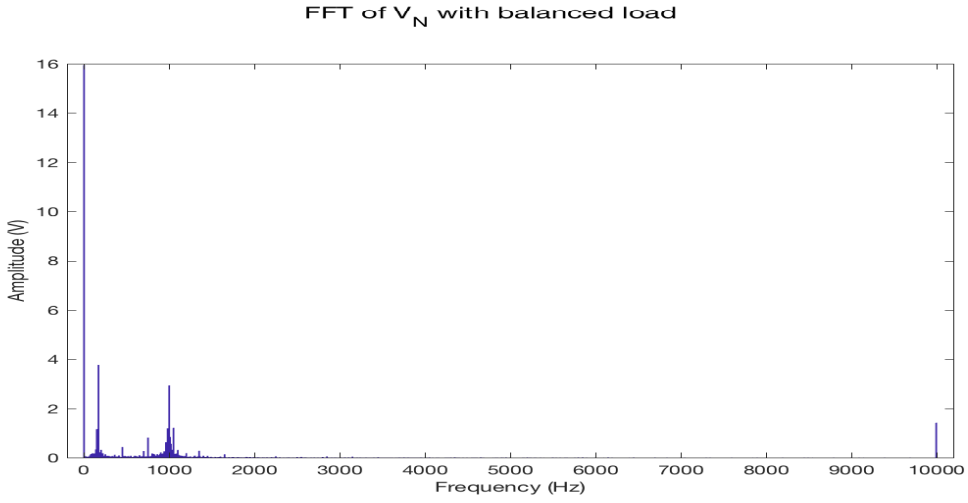


Figure 3.5.35: Independently Controlled Neutral Leg with balanced load: no zero sequence voltage and no neutral voltage control. FFT of neutral voltage with balanced load

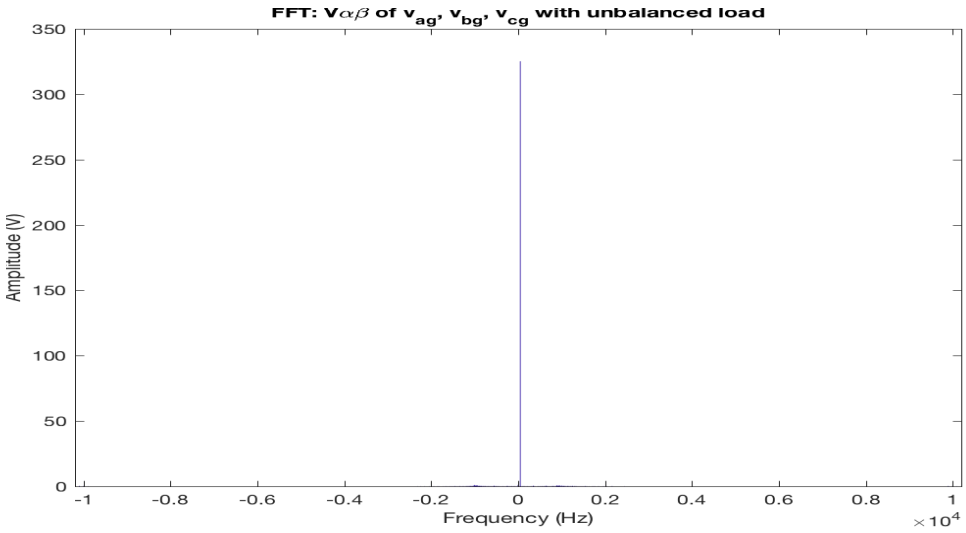


Figure 3.5.36: Independently Controlled Neutral Leg with unbalanced load: no zero sequence voltage and no neutral voltage control. Harmonic spectrum of grid voltage with unbalanced load

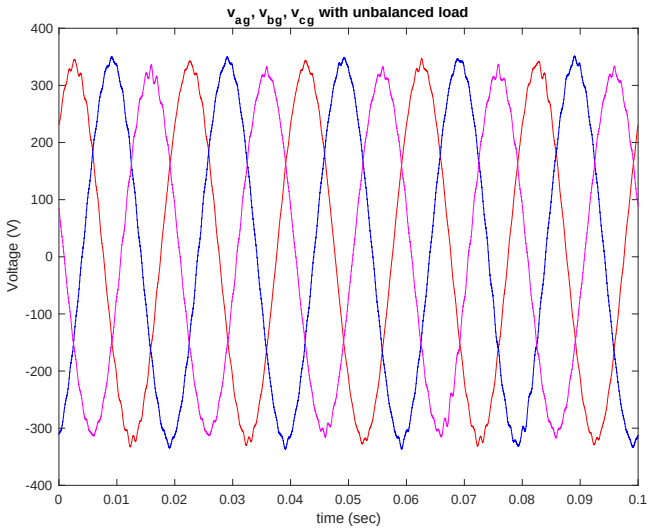


Figure 3.5.37: Independently Controlled Neutral Leg with unbalanced load: no zero sequence voltage and no neutral voltage control. Waveform of grid voltage with unbalanced load

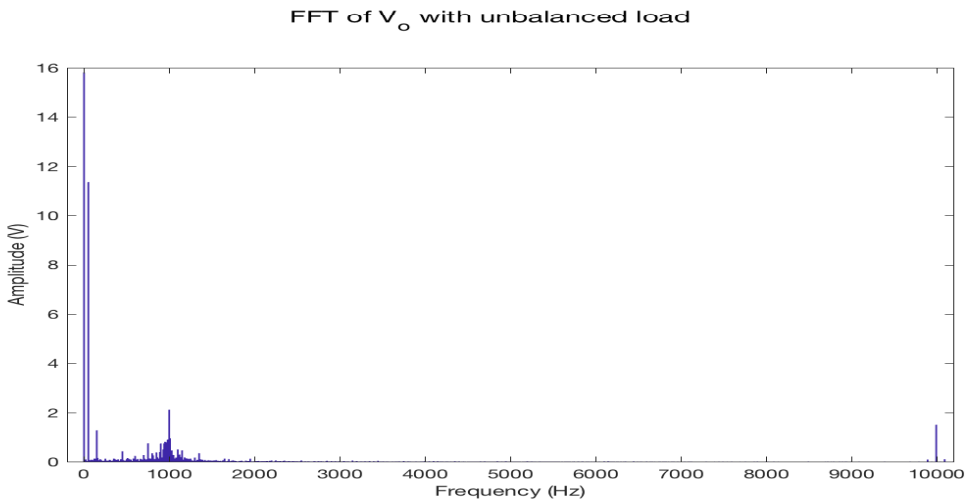


Figure 3.5.38: Independently Controlled Neutral Leg with unbalanced load: no zero sequence voltage and no neutral voltage control. FFT of zero voltage sequence with unbalanced load

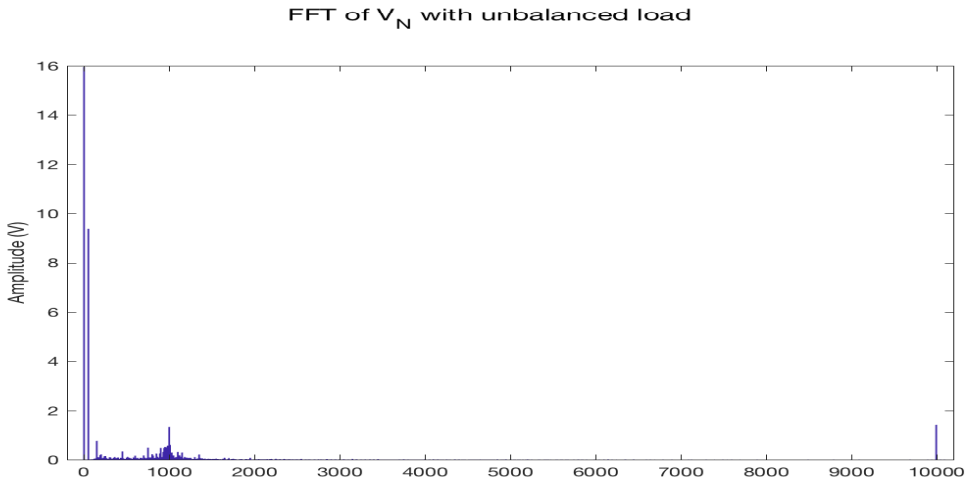


Figure 3.5.39: Independently Controlled Neutral Leg with unbalanced load: no zero sequence voltage and no neutral voltage control. FFT of neutral voltage with unbalanced load

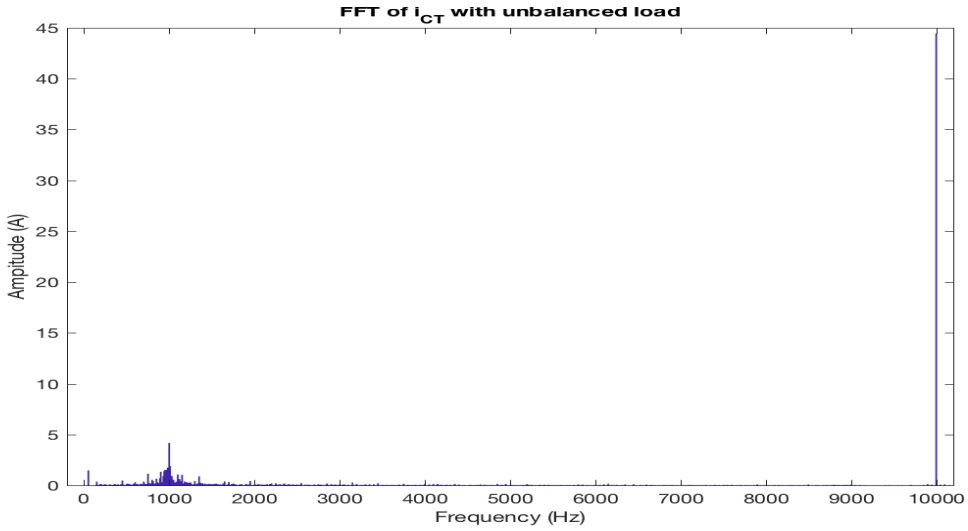


Figure 3.5.40: Independently Controlled Neutral Leg with unbalanced load: no zero sequence voltage and no neutral voltage control. FFT of the current through the DC-link capacitors with unbalanced load

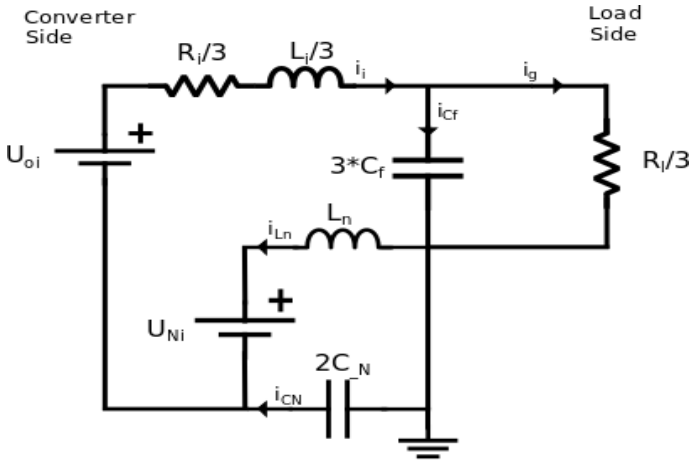


Figure 3.5.41: Three-Phase Power converter with fourth leg, slit DC-bus capacitors and *LC*-filter: equivalent circuit for zero voltage sequence and neutral voltage

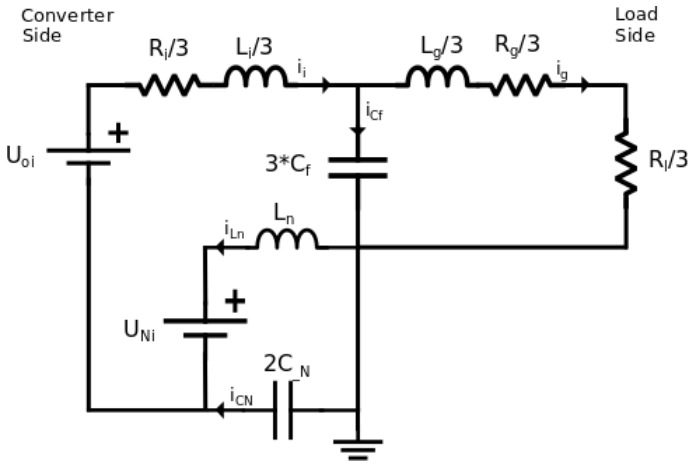


Figure 3.5.42: Three-Phase Power converter with fourth leg, slit DC-bus capacitors and *LCL*-filter: equivalent circuit for zero voltage sequence and neutral voltage

The goal of zero voltage sequence control is to attenuate the 50 Hz component. Because of this reason, for the voltage loop a PR will be used with an infinite gain in 50 Hz. For the current loop, another PR will be used, always with an infinite gain in 50 Hz. It's impossible to control using just a proportional (P) or proportional integral (PI) because at the beginning the simulation is done only with balanced load, that generally is not connected to the ground, i.e. motor connected to the grid, and consequently the integral part integrates the error between the current reference, that is the output of the voltage loop, and the real value that will be always zero because there is not the connection. After an unbalanced load is connected, which is necessary the neutral wire. The current used in the inner current loop is the current flowing through the neutral path i_g, which could be in the load side, called i_{Ng}, or in the inverter side, called i_{Ni} in the physical model. The different between the two currents is the harmonic content that will be shown in the next chapter.

The other task is to generate firing pulses for the switches N^+ and N^- in the fourth leg. The general aim of the controller is to maintain the voltage at the mid-point of capacitors in the DC-bus close to zero all the times. If the DC-link voltage is constant, the controller has to maintain the voltage capacitors balanced by forcing the inductor current i_{Ln} equal to the neutral current i_g in the equivalent circuit, or i_{Ni}/i_{Ng} in the physical model, so there isn't 50 Hz current component flows through the capacitors CT and CB in the DC-bus.

Two possibilities of fourth leg's control are taking into consideration:

- control the voltage v_N, which is the voltage in the middle point of the fourth leg [15] [16]. This means to eliminate the 50 Hz component, as depicted in fig. 3.5.43 and 3.5.44

- control the current in the split capacitors, i_{CT} and i_{CB}, that means to reduce or eliminate completely the 50 Hz component, as 3.5.50 and 3.5.51.

a. Control of U_N Assuming that the capacitors in the DC-link are the same, and the voltages across the capacitors CT and CB with respect the neutral point N are V_+ and V_-, respectively.

The issue is to balance two capacitors' voltages, and this can be expressed by making U_N very small. U_N is defined as:

$U_N = \frac{V_+ - V_-}{2}$

According to the Kirchhoff's laws, the following equations are satisfied, neglecting the resistors R_i and R_g, firstly with *LC* filter 3.31 and secondly with *LCL* filter 3.32.

$$LC\text{-filter}\begin{cases} U_{oi} = \frac{L_i}{3}\frac{di_i}{dt} + V_{Cf} + L_n\frac{di_{Ln}}{dt} + U_{Ni} \\ V_{Cf} = \frac{R_l}{3}i_g \\ V_{CN} = U_N + L_n\frac{di_{Ln}}{dt} \\ i_i = i_g + i_{Cf} \\ i_i = i_{Ln} + i_{CN} \\ V_{Cf} = \frac{1}{3C_f}\int i_{Cf}\,dt \\ V_{CN} = \frac{1}{2C_N}\int i_{CN}\,dt \end{cases} \tag{3.31}$$

$$LCL\text{-filter}\begin{cases} U_{oi} = \frac{L_i}{3}\frac{di_i}{dt} + V_{Cf} + L_n\frac{di_{Ln}}{dt} + U_{Ni} \\ V_{Cf} = \frac{L_g}{3}\frac{di_g}{dt} + \frac{R_l}{3}i_g \\ V_{CN} = U_N + L_n\frac{di_{Ln}}{dt} \\ i_i = i_g + i_{Cf} \\ i_i = i_{Ln} + i_{CN} \\ V_{Cf} = \frac{1}{3C_f}\int i_{Cf}\,dt \\ V_{CN} = \frac{1}{2C_N}\int i_{CN}\,dt \end{cases} \tag{3.32}$$

Using the Laplace transformation in the equations 3.31 and 3.32, the

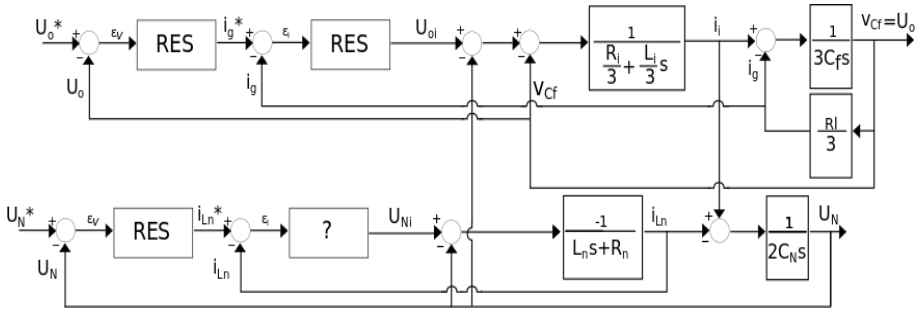


Figure 3.5.43: Three-Phase power converter with fouth leg, split DC capacitors and *LC*-filter: global block diagram for the control of zero voltage sequence U_o and neutral voltage U_N

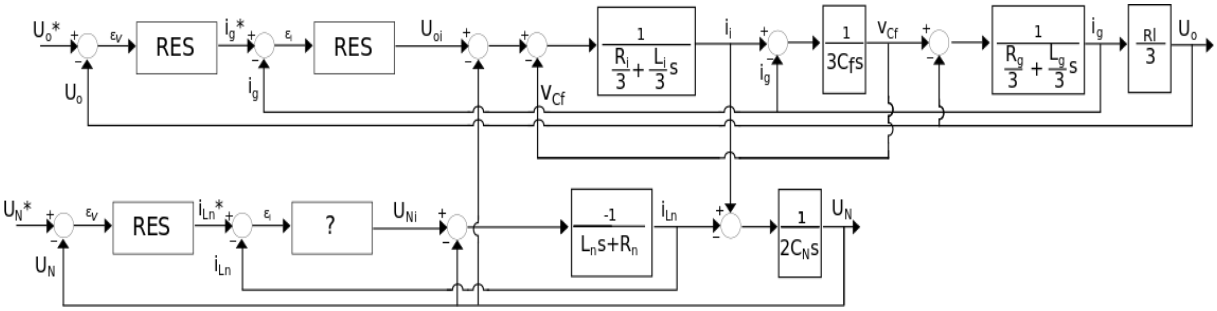


Figure 3.5.44: Three-Phase power converter with fouth leg, split DC capacitors and *LCL*-filter: global block diagram for the control of zero voltage sequence U_o and neutral voltage U_N

blocks diagrams of the four legs three-phase power converter are obtained. The block diagrams, adding the control loops, are shown in figures 3.5.43 and 3.5.44.

In order to control the neutral voltage U_N, the idea is to use a PR for the voltage loop and change the type of the control for the inner current loop, that could be just a proportional (P), a proportional integrator (PI), a proportional resonant (PR) or PI and PR in parallel, as in figure 3.5.45. In the current loop, it's used the current in the inductor L_n because the voltage depends on the current flows through the inductor i_{Ln}.

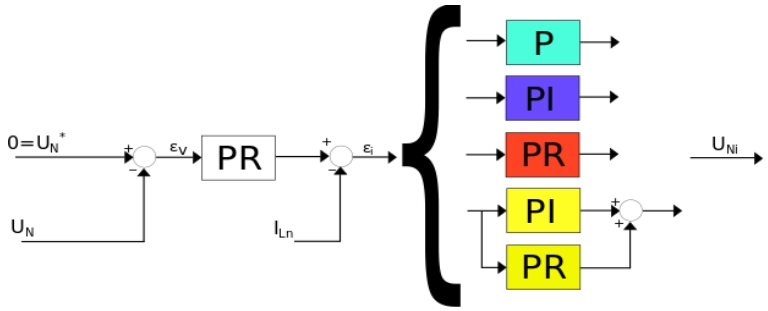
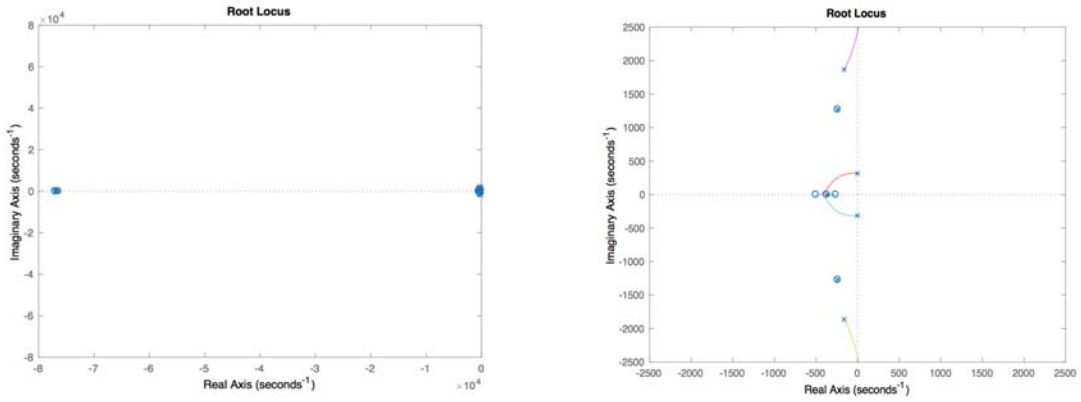


Figure 3.5.45: Neutral voltage control: different controllers for the inner current loop



(a) **(b)**

Figure 3.5.46: Split DC-capacitors with unbalanced load using a Proportional controller in the inner current loop: Root locus of transfer function $\frac{U_O}{U_O{}^*}$ in fig. (a). In fig. (b) a zoom of critical part

Being the system complex, it's not immediate to calculate the transfer function but it could be useful to understand if the system, including the controllers, is stable or not. Changing the controllers, the root locus will change.

Considering now the first case, in which in the inner current loop of the neutral voltage control is used a proportional P and *LCL*-filter, the transfer function, for the neutral control, is the ratio between the output U_N and the input $U_N{}^*$. The transfer function presents nine zeros and eleven poles. Now, just looking the root locus, shown in fig. 3.5.46, it's possible to see the position of them.

In fig. 3.5.46b there is a zoom of the critical part of the root locus because in this are it could be possible to find poles in the right part, with real part positive. Thanks to the values of the controllers chosen, the system is perfectly stable.

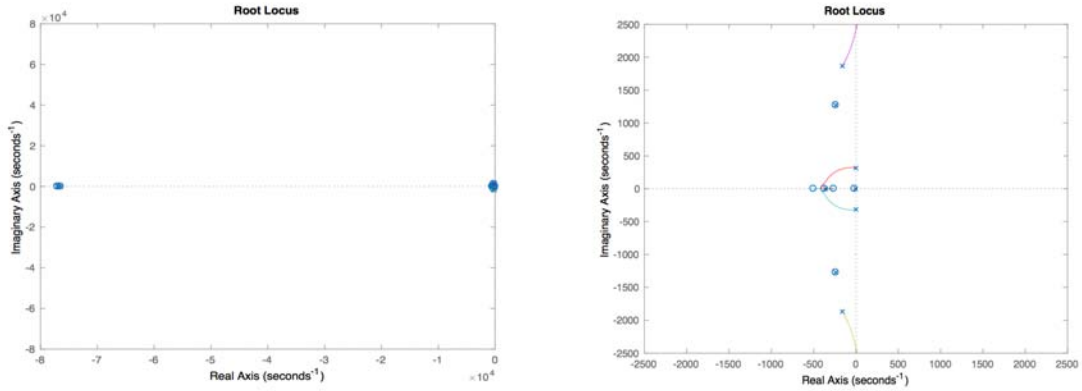
The second option is the use of a PI. The transfer function has ten zeros and twelve poles. The number of zeros will increase changing the controllers because each controller has different number of zeros and poles. These could compromise the stability of the system. The root locus is 3.5.47:

Once again, the poles are in the left part, so the system is stable.

The third option is the use of a PR. The transfer function has eleven zeros and thirteen poles. The root locus is shown in fig. 3.5.48:

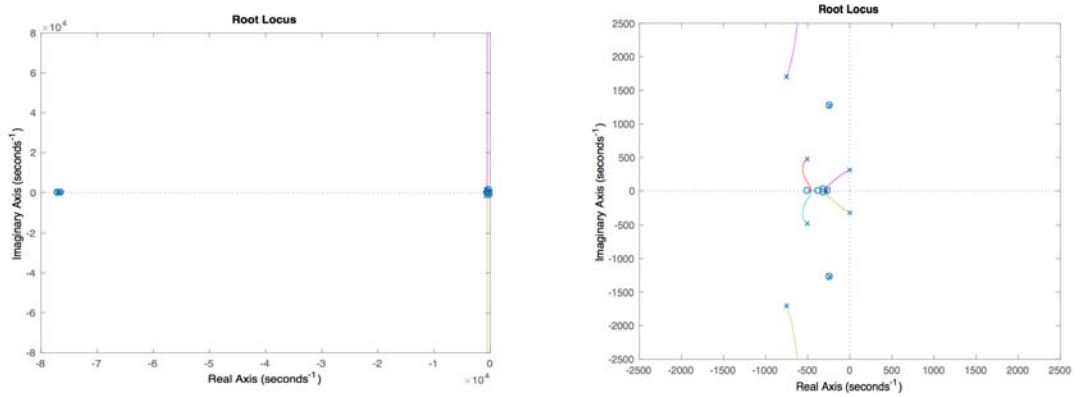
In fig. 3.5.48b is possible to see that, once again, the system is stable.

The last option is the parallel between a PI and a PR, increasing the number of poles and zeros of the system. In fact the transfer function has twelve zeros and fourteen poles.



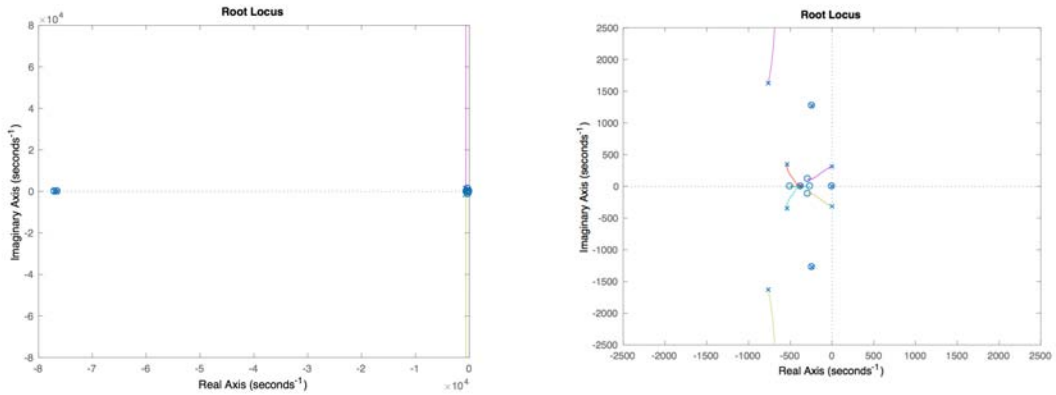
(a) **(b)**

Figure 3.5.47: Split DC-capacitors with unbalanced load using a PI controller in the inner current loop: Root locus of transfer function $\frac{U_o}{U_o{}^*}$ in fig. (a). In fig. (b) a zoom of critical part



(a) **(b)**

Figure 3.5.48: Split DC-capacitors with unbalanced load using a PR controller in the inner current loop: Root locus of transfer function $\frac{U_o}{U_o{}^*}$ in fig. (a). In fig. (b) a zoom of critical part



(a) **(b)**

Figure 3.5.49: Split DC-capacitors with unbalanced load using a PI in parallel with a PR in the inner current loop: Root locus of transfer function $\frac{U_o}{U_o^*}$ in fig. (a). In fig. (b) a zoom of critical part

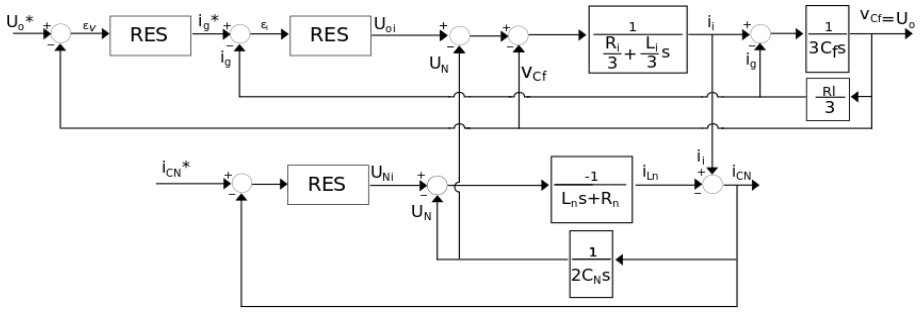


Figure 3.5.50: Three-Phase Power converter with fourth leg, split capacitors in DC-bus and *LC*-filter: block diagram for zero voltage sequence and neutral current controls

b. Control of iCT and iCB Assuming that the capacitors in the DC-link are the same, the currents i_{CT} and i_{CB} of the capacitors are equal. It is possible to consider the simplified circuits, 3.5.12 and 3.5.13, with the systems 3.31 and 3.32 used previously.

Now the target is to control the currents i_{CT} and i_{CB} flow through the capacitors CT and CB in the physical system, or the current i_{CN} flows in the equivalent capacitor $C_{eq}=2C_N$ in the equivalent circuit.

The task is attenuate or eliminate the 50 Hz component such a way to reduce the oscillation of the middle point of the capacitors, N, respect the ground.

Now just considering the equivalents circuit, it's possible to control the current i_{CN} flows through C_{eq}, using just a PR in the current loop. U_{Ni} is the voltage command to control the neutral switches N_+ and N_-. The diagram blocks of the system with the control loops are shown in fig. 3.5.50 and 3.5.51.

As just done, it is useful to calculate the transfer function of the global

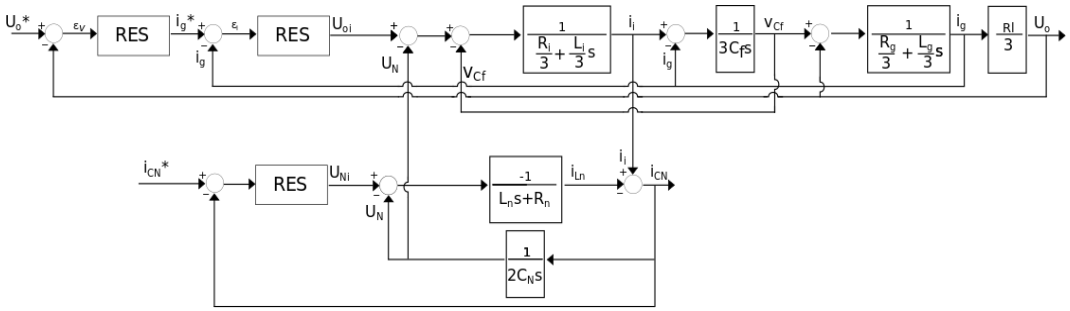


Figure 3.5.51: Three-Phase Power converter with fourth leg, split capacitors in DC-bus and *LCL*-filter: block diagram for zero voltage sequence and neutral current controls

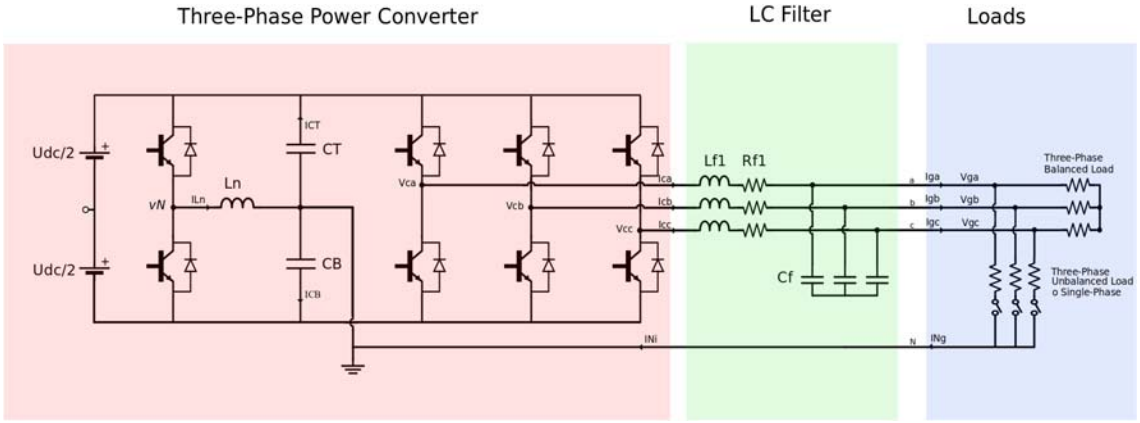


Figure 3.5.52: Three-Phase power converter with four legs and with the capacitors in the DC-bus, *LC*-filter, balanced and unbalanced load, without the connection between neutral path and *LC*-filter

system, to demonstrate that effectively the system is stable.

Independently Controlled Neutral Leg, without the connection between the filter and the neutral wire

This topology is similar to the previous one, but without the connection between the filter and the neutral path.

In this configuration, shown in fig. 3.5.52 and 3.5.53, zero voltage sequence and the fourth leg will be controlled.

Without the zero voltage sequence and neutral controls Just controlling the positive and negative sequence, the situation is the following.

With a balanced load, the positive and negative sequence are able to control the output voltage, without any unbalances as it's shown FFT of the grid voltage in fig. 3.5.54, where there isn't -50 Hz component and the 50 Hz component is equal to the target value imposed by the positive sequence.

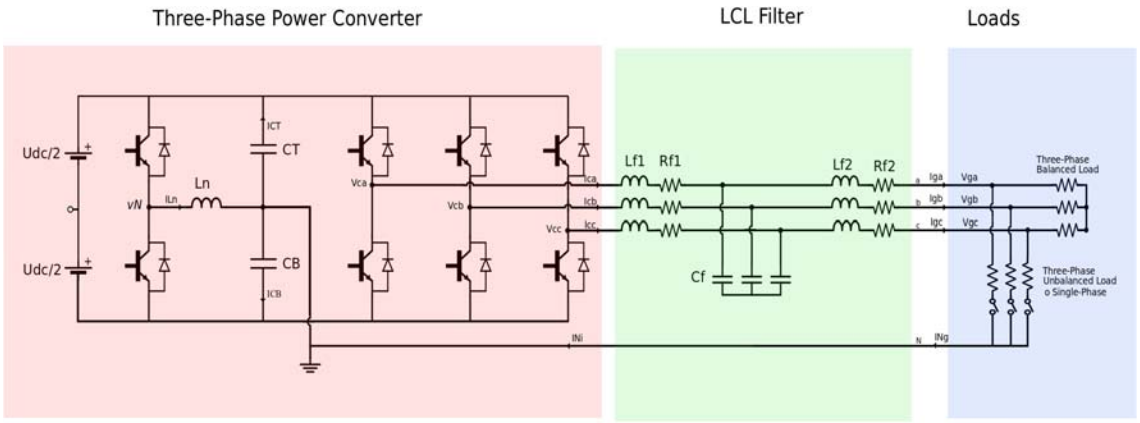


Figure 3.5.53: Three-Phase power converter with four legs and with the capacitors in the DC-bus, *LCL*-filter, balanced and unbalanced load, without the connection between neutral path and *LCL*-filter

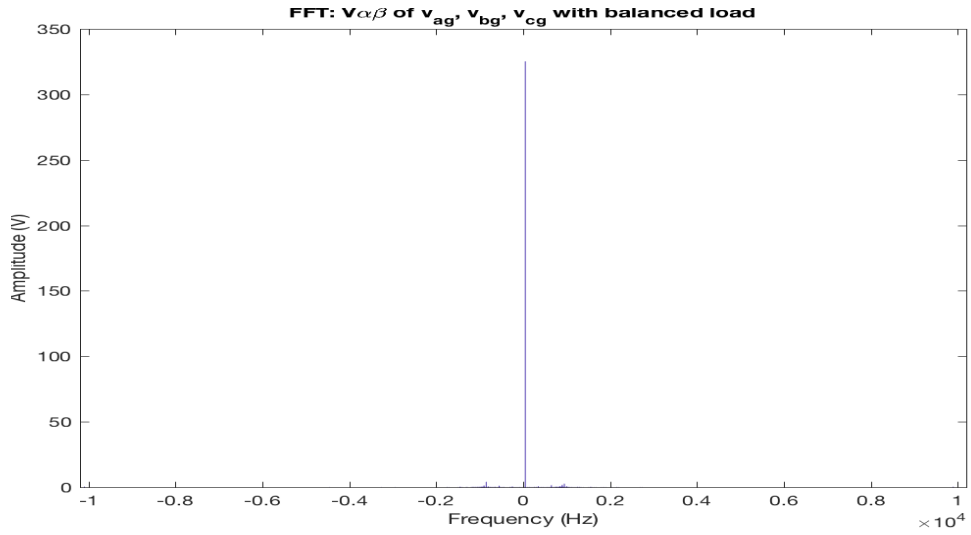


Figure 3.5.54: Independently Controlled Neutral Leg without the connection between the neutral path and the filter: no zero sequence voltage and no neutral voltage control. Harmonic spectrum of grid voltage with balanced load

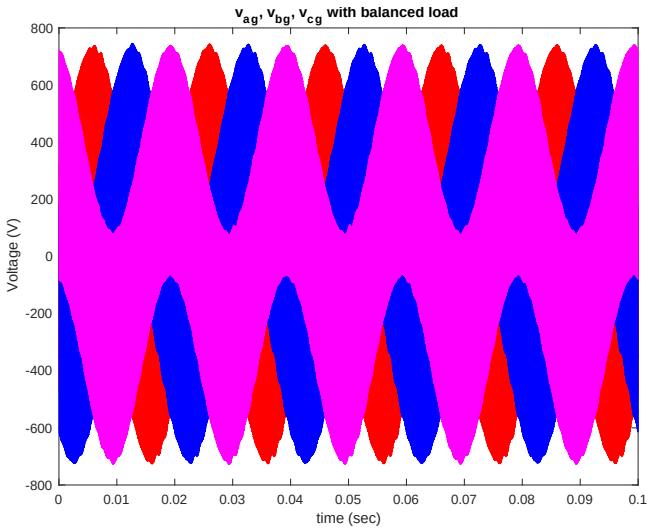


Figure 3.5.55: Independently Controlled Neutral Leg without the connection between the neutral path and the filter: no zero sequence voltage and no neutral voltage control. Waveform of grid voltage with balanced load

The grid voltage waveform is perfect balances, as shown in fig. 3.5.55.

The zero sequence voltage hasn't 50 Hz component, as it is depicted in fig. 3.5.56. Contrarily, it has a big DC component and a big component at switching frequency.

The neutral voltage has just a big DC component, 3.5.57.

Now connecting an unbalanced load to the power converter, the voltage should be unbalanced due to the unbalances of the load. It's necessary to control the grid voltage. Positive and negative sequence control are able to achieve the target value of the voltage and eliminate the -50 Hz component, 3.5.58. There is an oscillation, as it's possible to see in fig. 3.5.59 due the presence of unbalanced loads connected to the grid.

In this case, not only the DC and switching frequency components are present, but also the oscillation of 50 Hz is possible to see in the FFT of zero voltage sequence in fig. 3.5.60. Now the neutral voltage has a component at fundamental frequency, but lower than U_o, as shown in fig. 3.5.61.

Also the current i_{CT} has a small 50 Hz component, 3.5.62.

Control Strategy The equivalent circuits are depicted in fig. 3.5.63, with *LC*-filter, and 3.5.64, with *LCL*-filter, respectively. The targets are the same. The control is developed in the same way of the previous configuration, considering the two possibilities for the four leg control:

- U_N control;
- i_N control.

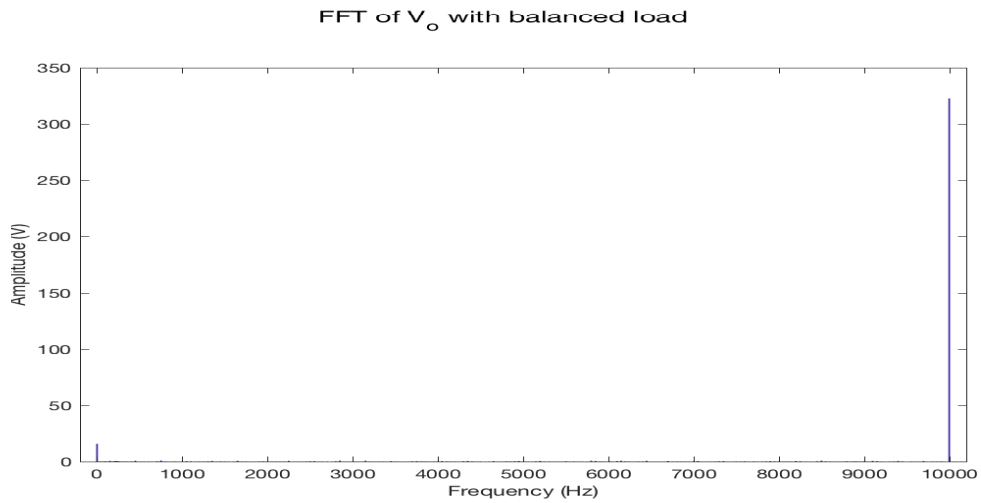


Figure 3.5.56: Independently Controlled Neutral Leg without the connection between the neutral path and the filter: no zero sequence voltage and no neutral voltage control. FFT of zero voltage sequence with balanced load

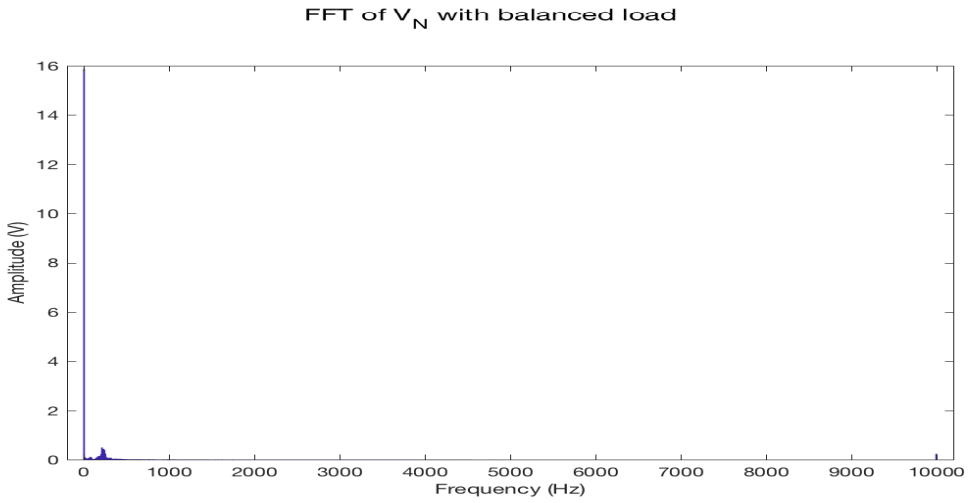


Figure 3.5.57: Independently Controlled Neutral Leg without the connection between the neutral path and the filter: no zero sequence voltage and no neutral voltage control. FFT of neutral voltage with balanced load

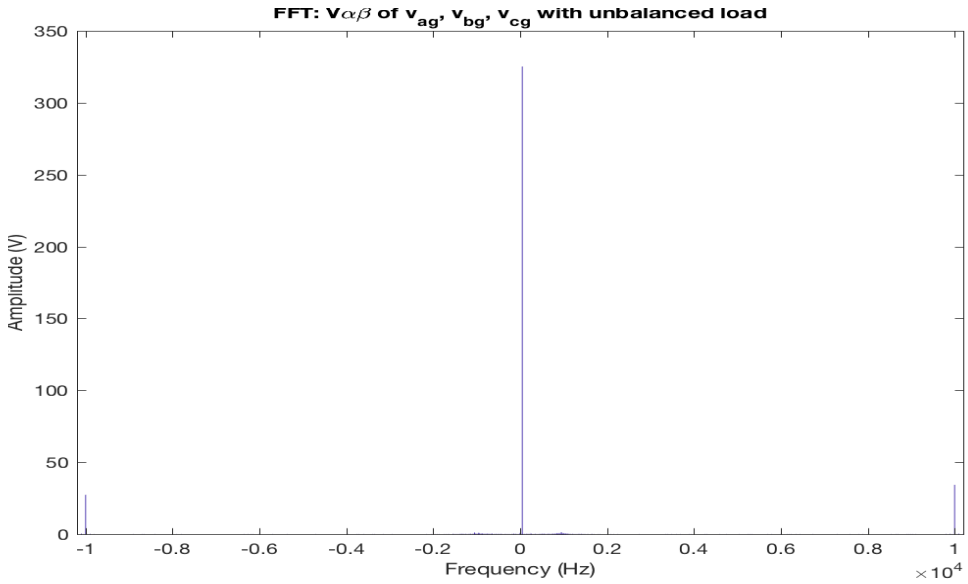


Figure 3.5.58: Independently Controlled Neutral Leg without the connection between the neutral path and the filter: no zero sequence voltage and no neutral voltage control. Harmonic spectrum of grid voltage with unbalanced load

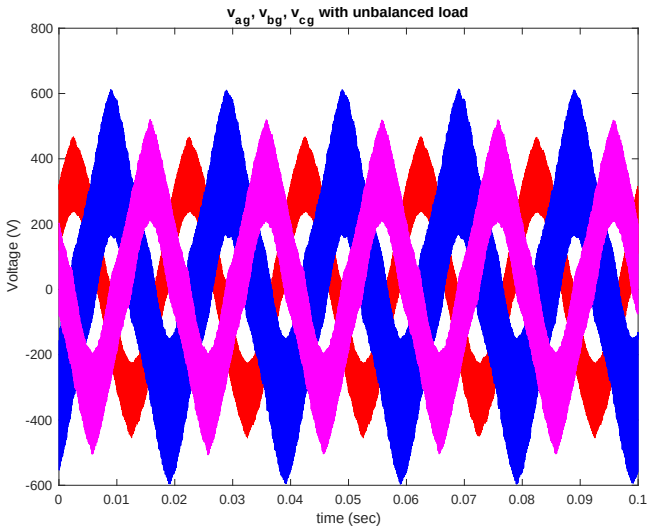


Figure 3.5.59: Independently Controlled Neutral Leg without the connection between the neutral path and the filter: no zero sequence voltage and no neutral voltage control. Waveform of grid voltage with unbalanced load

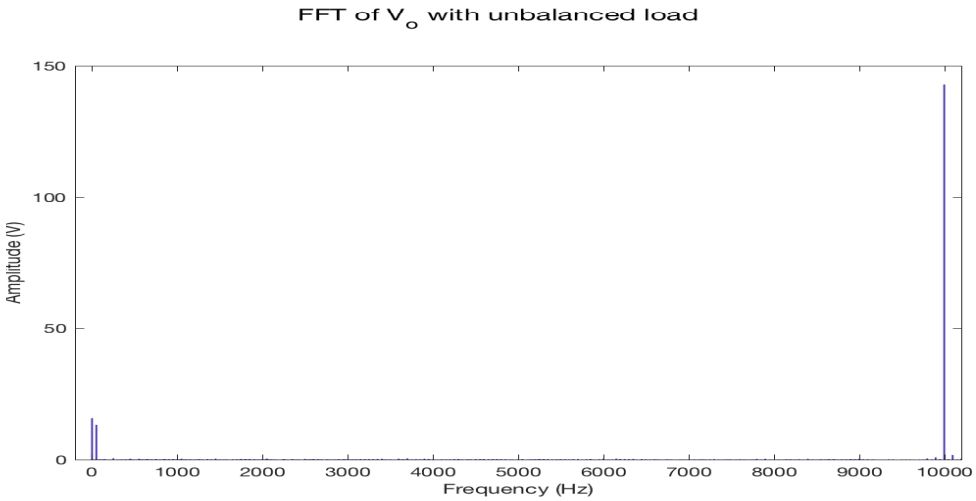


Figure 3.5.60: Independently Controlled Neutral Leg without the connection between the neutral path and the filter: no zero sequence voltage and no neutral voltage control. FFT of zero voltage sequence with unbalanced load

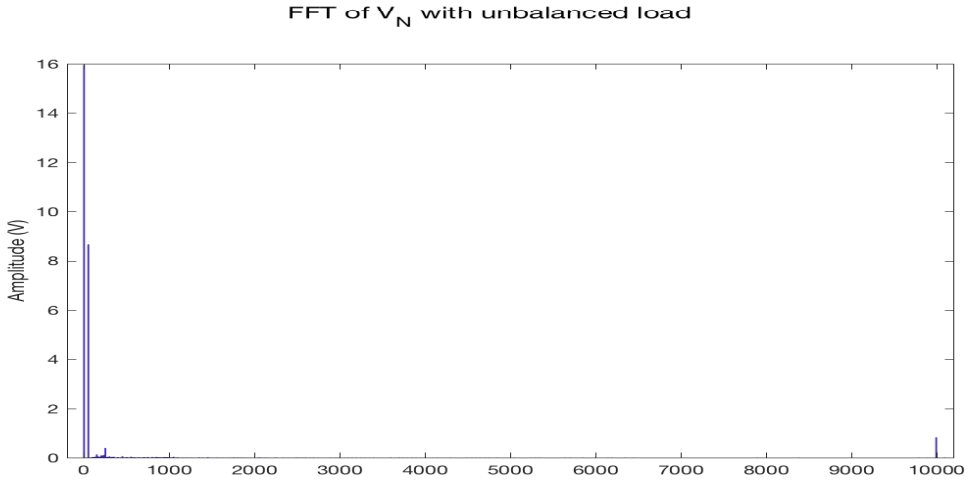


Figure 3.5.61: Independently Controlled Neutral Leg without the connection between the neutral path and the filter: no zero sequence voltage and no neutral voltage control. FFT of neutral voltage with unbalanced load

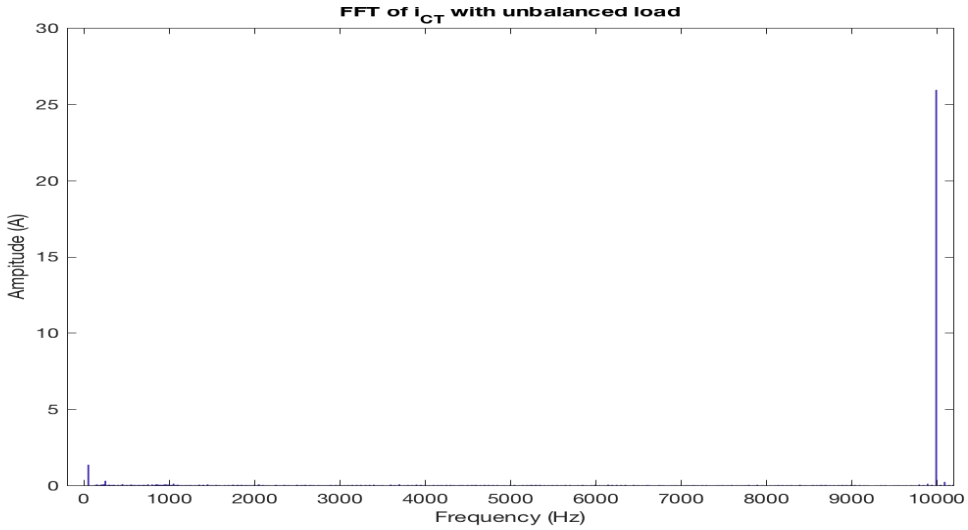


Figure 3.5.62: Independently Controlled Neutral Leg without the connection between the neutral path and the filter: no zero sequence voltage and no neutral voltage control. FFT of the current through the DC-link capacitors with unbalanced load

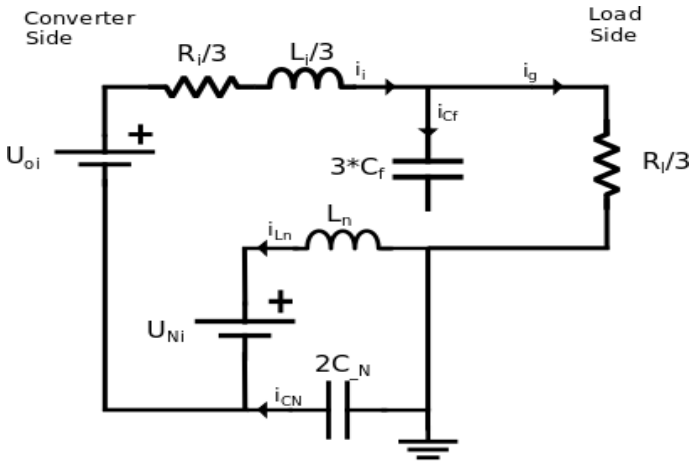


Figure 3.5.63: Three-Phase Power converter with fourth leg, split capacitors and *LC*-filter, without the connection between the filter and the neutral wire: equivalent circuit for zero voltage sequence and neutral voltage controls

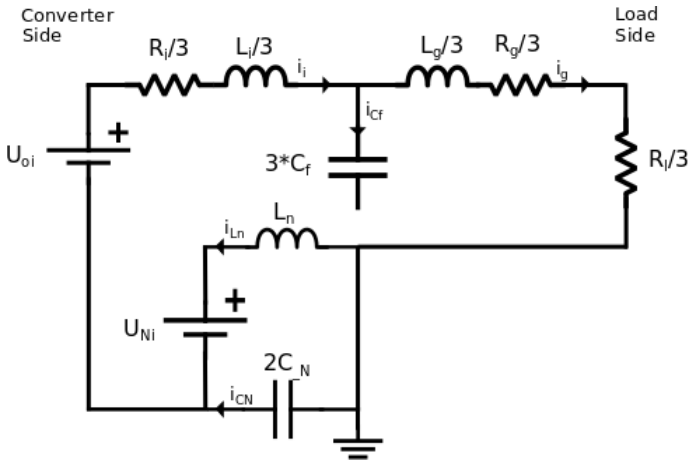


Figure 3.5.64: Three-Phase Power converter with fourth leg, split capacitors and *LCL*-filter, without the connection between the filter and the neutral wire: equivalent circuit for zero voltage sequence and neutral voltage controls

Chapter 4

Comparative analysis and simulation results

4.1 Introduction

In this chapter, some simulations are performed in order to show, for each configuration and for each type of control, the results.

Matlab-Simulink is the software used to implement the models. The data of the three-phase power converter used in the simulations are listed in the tables 2.1, 2.2 and 2.3 in the Chapter 2.

The Three-Phase four-legs inverter is supposed to provide rated load voltage in presence of unbalanced and non-linear loads. The idea is to study all configurations, controlling all the time positive and negative sequence and changing the type of controllers for zero voltage sequence and for the fourth leg controller. In order to define the best utilities and the best controllers for each configuration the harmonic spectrum (FFT), the total harmonic distortion (THD) are valuated.

Due to the high number of the configuration and types of controllers, the work will be developed in the following way.

In order to understand the following tables, it's necessary to define the nomenclature in the Table 4.1, in which all the abbreviation used are explicated:

In the Tables 4.2 and 4.3, the configuration with four legs and split DC-link capacitors is presented. In the first one there is the possibility to control the zero voltage sequence U_o and the neutral voltage U_N; in the second one the control of the zero voltage sequence U_o is the same, the neutral leg is controlled by controlling the currents flowing through the DC-capacitors.

In the Tables 4.4, the configuration with just four legs is studied, controlling the neutral voltage U_N which is the inductor L_n voltage and zero voltage sequence U_o, changing the possibly of controlling the both, the first or just the second.

Table 4.1: Nomenclature

Abbreviation	Meaning
PR_v	Proportional Resonant used in the voltage loop
PR_i	Proportional Resonant used in the inner current loop
PI_i	Proportional Integral used in the inner current loop
P_i	Proportional used in the inner current loop
$(PR;PI)_i$	Proportional Resonant and Proportional Integral in parallel used in the inner current loop

Table 4.2: Neutral configurations: Four legs with capacitors. Control strategy: Independently Controlled Neutral Leg with U_o and U_N control

Case	Filter	Zero sequence control	Fourth leg control
1.	*LCL*	PR_v+PR_i	PR_v+PI_i
2.	*LCL*	open-loop	PR_v+PI_i
3.	*LCL*	PR_v+PR_i	open-loop
4.	*LCL*	PR_v+PR_i	four leg PR_v+P_i
5.	*LCL*	open-loop	PR_v+P_i
6.	*LCL*	PR_v+PR_i	$PR_v+(PR;PI)_i$
7.	*LCL*	open-loop	$PR_v+(PR;PI)_i$
8.	*LCL*	PR_v+PR_i	PR_v+PR_i
9.	*LCL*	open loop	PR_v+PR_i
10.	*LC*	PR_v+PR_i	PR_v+PI_i
11.	*LC*	open-loop	PR_v+PI_i
12.	*LC*	PR_v+PR_i	open-loop
13.	*LC*	PR_v+PR_i	PR_v+P_i
14.	*LC*	open-loop	PR_v+P_i
15.	*LC*	PR_v+PR_i	$PR_v+(PR;PI)_i$
16.	*LC*	open-loop	$PR_v+(PRi;PI)_i$
17.	*LC*	PR_v+PR_i	PR_v+PR_i
18.	*LC*	open-loop	PR_v+PR_i

Table 4.3: Neutral configurations: Four legs with capacitors. Control strategy: Independently Controlled Neutral Leg with U_o and i_N control

Case	Filter	Zero sequence control	Fourth leg control
19.	*LCL*	PR_v+PR_i	PR_v+PR_i
20.	*LCL*	open-loop	PR_v+PR_i
21.	*LC*	PR_v+PR_i	PR_v+PR_i
22.	*LC*	open-loop	PR_v+PR_i

Table 4.4: Neutral configuration: Four legs. Control strategy: Conventional Neutral Leg with U_o and U_N control

Case	Filter	Zero sequence control	Fourth leg control
23.	*LCL*	PR_v+PR_i	PR_v
24.	*LCL*	open-loop	PR_v
25.	*LCL*	PR_v+PR_i	open-loop
26.	*LC*	PR_v+PR_i	PR_v
27.	*LC*	open-loop	PR_v
28.	*LC*	PR_v+PR_i	open-loop

Table 4.5: Neutral configuration: Split DC-link Capacitors with U_o control

Case	Filter	Zero sequence control	Fourth leg control
29.	*LCL*	PR_v+PR_i	/
30.	*LC*	PR_v+PR_i	/

As shown in the tab. 4.5 referred the topology with split DC-capacitors, it's necessary to control just the zero sequence voltage U_o.

The Tables 4.6 and 4.7 are referred to the last topology, including the possibility to control not only the zero voltage sequence U_o but also the fourth leg or controlling U_N or i_N.

The chapter will be organized in this way:

- in the section 4.2 FFT of currents and voltages with balanced/unbalanced loads and *LC*/*LCL*-filters for each configuration with the same type of control will be shown, just to have a clear idea how the four topologies work;
- in the section 4.3 different control systems are compared. This means works with open or closed loop of zero voltage sequence or neutral voltage.
- in the section 4.4 different control strategies are studied, in order to understand the main differences.

4.2 Harmonic spectrum

In order to study and analyse each single case, it could be useful to study the spectrum analysis with the Fast Fourier Transform (FFT) [3]. FFT is a computational tool which facilitates signal analysis such as power spectrum. It is a method for efficiently computing the discrete Fourier transform of a series of data samples. FFT is a method for efficiently

Table 4.6: Neutral configuration: Four legs with capacitors. Control strategy: Indipendently Controlled Neutral Leg, without the connection between the filter and the neutral wire with U_o and U_N control

Case	Filter	Zero sequence control	Fourth leg control
31.	*LCL*	PR_v+PR_i	PR_v+PI_i
32.	*LCL*	open-loop	PR_v+PI_i
33.	*LCL*	PR_v+PR_i	open-loop
34.	*LCL*	PR_v+PR_i	PR_v+P_i
35.	*LCL*	open-loop	PR_v+P_i
36.	*LCL*	PR_v+PR_i	$PR_v+(PR;PI)_i$
37.	*LCL*	open-loop	$PR_v+(PR;PI)_i$
38.	*LCL*	PR_v+PR_i	PR_v+PR_i
39.	*LCL*	open-loop	PR_v+PR_i
40.	*LC*	PR_v+PR_i	PR_v+PI_i
41.	*LC*	open-loop	PR_v+PI_i
42.	*LC*	PR_v+PR_i	open-loop
43.	*LC*	PR_v+PR_i	PR_v+P_i
44.	*LC*	open-loop	PR_v+P_i
45.	*LC*	PR_v+PR_i	$PR_v+(PR;PI)_i$
46.	*LC*	open-loop	$PR_v+(PR;PI)_i$
47.	*LC*	PR_v+PR_i	PR_v+PR_i
48.	*LC*	open-loop	PR_v+PR_i

Table 4.7: Neutral configuration: Four legs with capacitors. Control strategy: Indipendently Controlled Neutral Leg, without the connection between the filter and the neutral wire with U_o and i_N control

Case	Filter	Zero sequence control	Fourth leg control
49.	*LCL*	PR_v+PR_i	PR_v+PR_i
50.	*LCL*	open-loop	PR_v+PR_i
51.	*LC*	PR_v+PR_i	PR_v+PR_i
52.	*LC*	open-loop	PR_v+PR_i

computing the discrete Fourier transform (DFT) of a time series (discrete data samples).

The harmonic currents and voltages will be examined in the $\alpha\beta\gamma$ coordinates. It's just done using the Clark transformation from *abc* reference frame to $\alpha\beta\gamma$ reference frame.

To understand the big differences between each configuration, it could be useful to see the harmonic performance of each current and voltage of the systems. The simulations are done using the same type of control in all the topologies. This means that the cases compared are:

- Conventional Neutral Leg. The cases are 26 with *LC*-filter and 23 with *LCL*-filter;
- Split DC-link Capacitors. The cases are 30 with *LC*-filter and 29 with *LCL*-filter;
- Independently Controlled Neutral Leg. The cases are 10 with *LC*-filter and 1 with *LCL*-filter;
- Independently Controlled Neutral Leg, without the connection between the filter and the neutral wire. The cases are 40 with *LC*-filter and 31 with *LCL*-filter;

All cases will be studied with balanced (a.) and unbalanced (b.) loads. The results are presented.

4.2.1 Conventional Neutral Leg

The topology is studied in the Chapter 2.2.1.

a. balanced load with *LCL*-filter

Looking at the figures from 4.2.1 to 4.2.9, the results with balanced load and *LCL*-filter are presented.

As was already provided, in the 4.2.1, which is the spectrum of the current incoming to the filters, and 4.2.2, which is the current outgoing to the filters, there is absence of -50 Hz, being the load balanced. The respectively values of 50 Hz, at fundamental frequency, are equal because the filters let pass the fundamental frequency, cleaning the harmonic content. For this reason, the only difference between the two currents is the harmonic content, that obviously will be lower in the grid current, after the action of the filters.

Fig. 4.2.3 depicts the respective waveforms.

In fig. 4.2.4 and 4.2.5 the input and output voltages spectrums are shown. What just said for the currents is valid for the voltages. The 50 Hz value is the same of the reference value chosen in the positive sequence

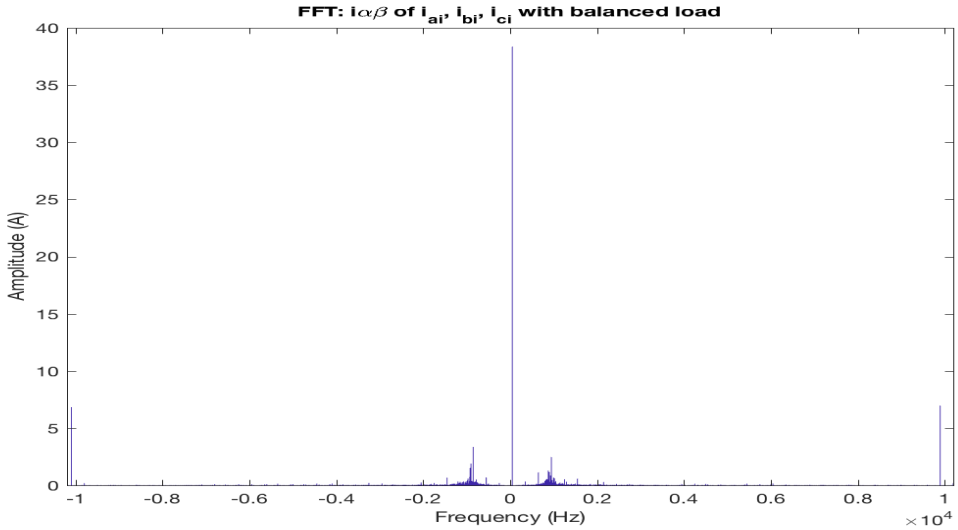


Figure 4.2.1: Case 23: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Harmonic spectrum of inverter current

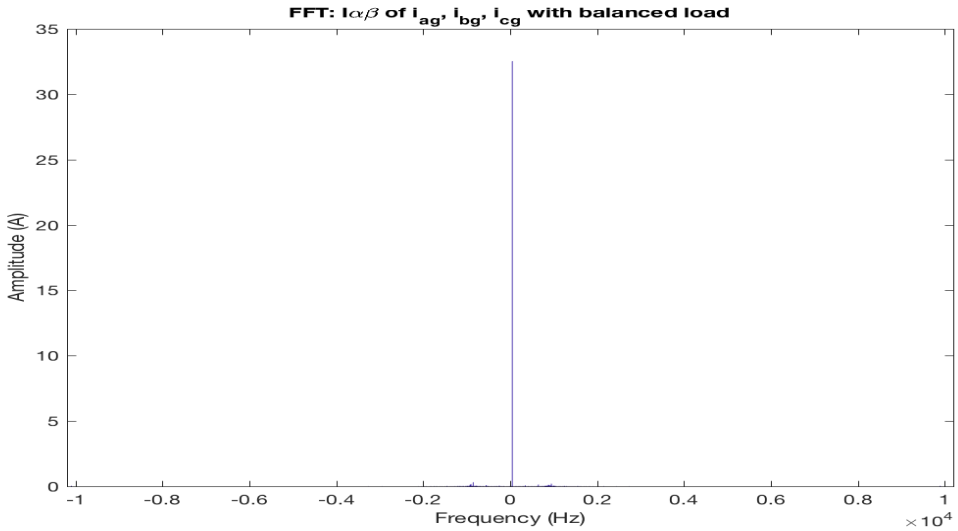
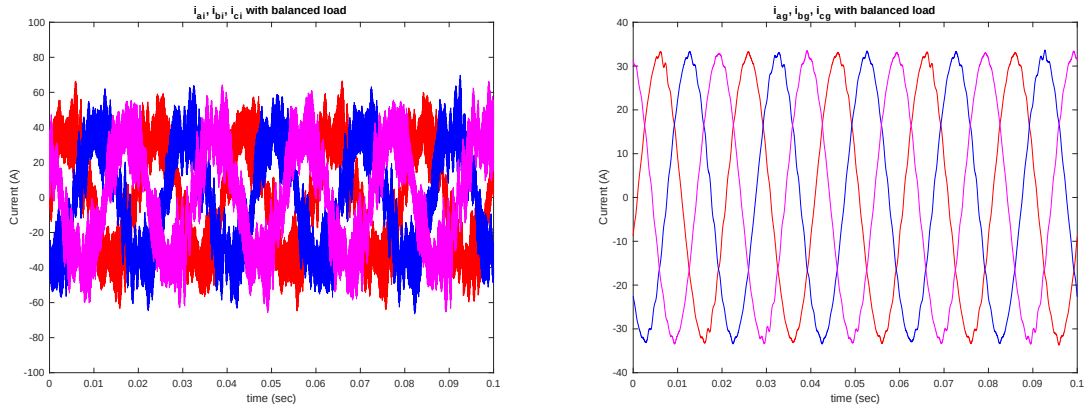


Figure 4.2.2: Case 23: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Harmonic spectrum of grid current



(a) **(b)**

Figure 4.2.3: Case 23: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) waveform of inverter current; fig. (b) waveform of grid current

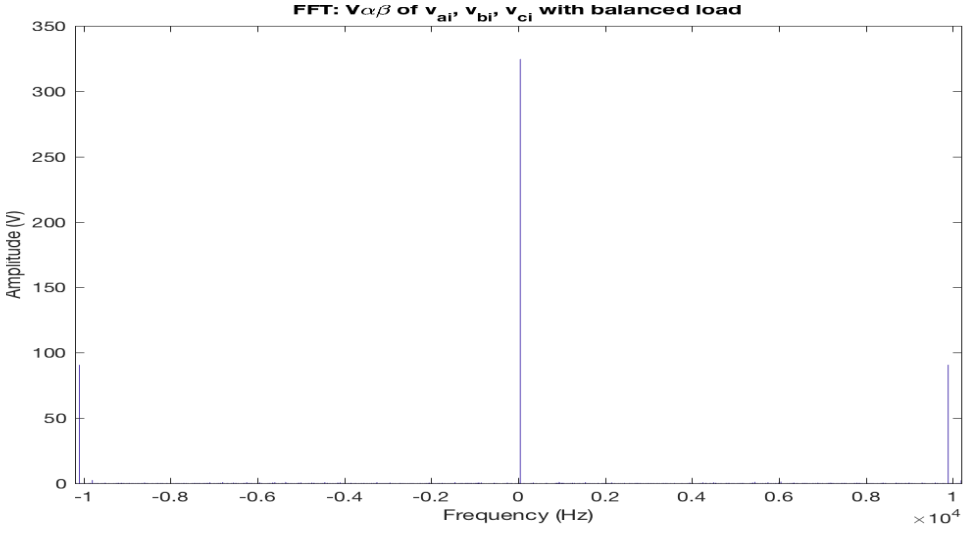


Figure 4.2.4: Case 23: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of inverter voltage

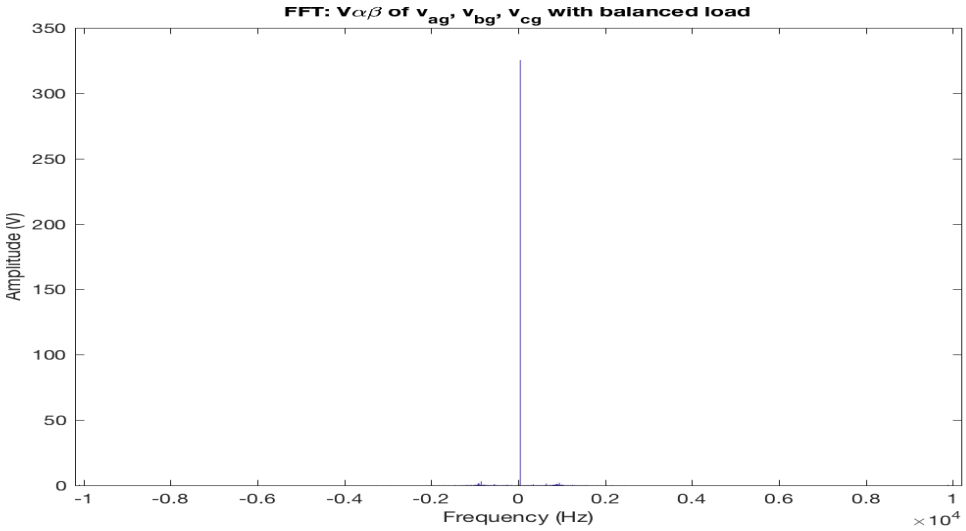
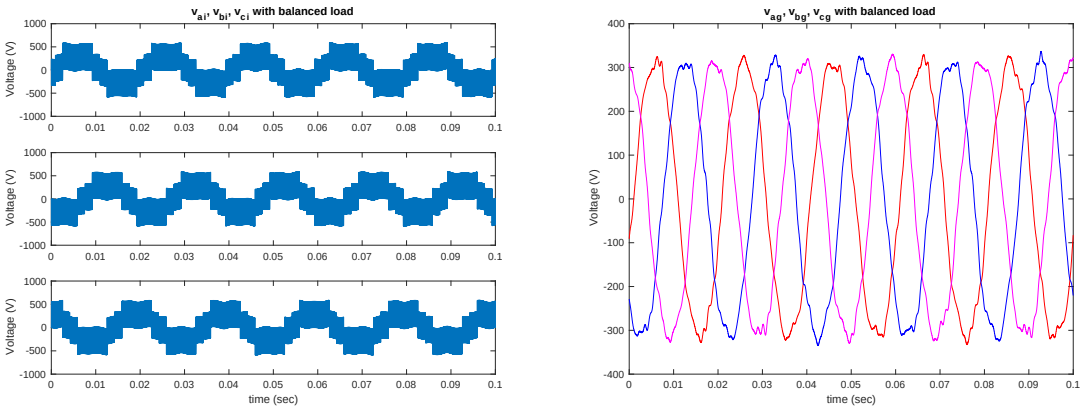


Figure 4.2.5: Case 23: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of grid voltage



(a) **(b)**

Figure 4.2.6: Case 23: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) inverter voltage; fig. (b) grid voltage

control. The inverter voltage, like inverter current, contains high values of harmonics, that using the filters, will disappear in the grid voltage and current.

In the fig. 4.2.5, the voltages waveforms are shown: 4.2.6a the input voltage of the three phases and 4.2.6b the three-phases V_{ag}, V_{bg}, V_{cg} of the output voltage. The voltages are measured respect the ground of the system, which is connect to the neutral path.

The zero sequence voltage U_o, fig. 4.2.7, doesn't have a big component at switching frequency, 10 kHz, and neither at fundamental frequency because the last one is controlled. It presents a high harmonic distortion, where third harmonic is the highest.

On the contrary, the neutral voltage U_N, fig. 4.2.8, has a high component of switching frequency due the presence of the fourth leg, without

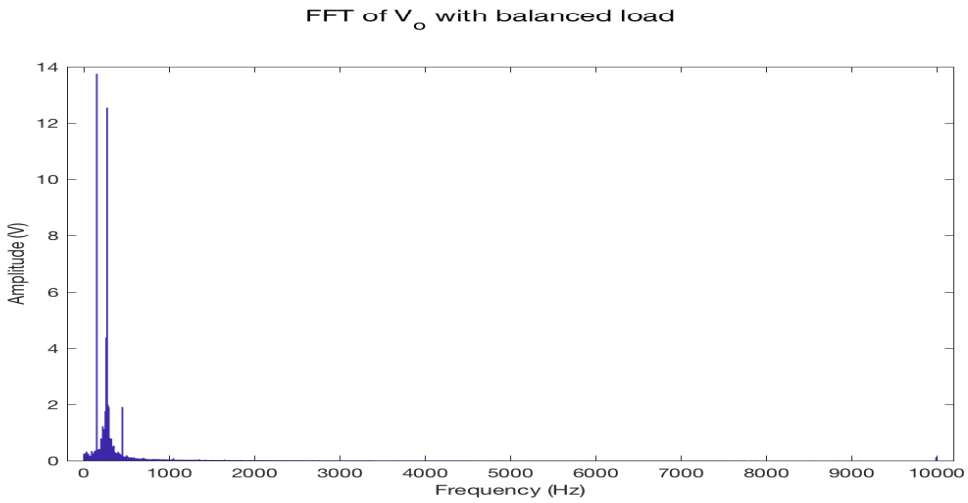


Figure 4.2.7: Case 23: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Harmonic spectrum of zero voltage sequence

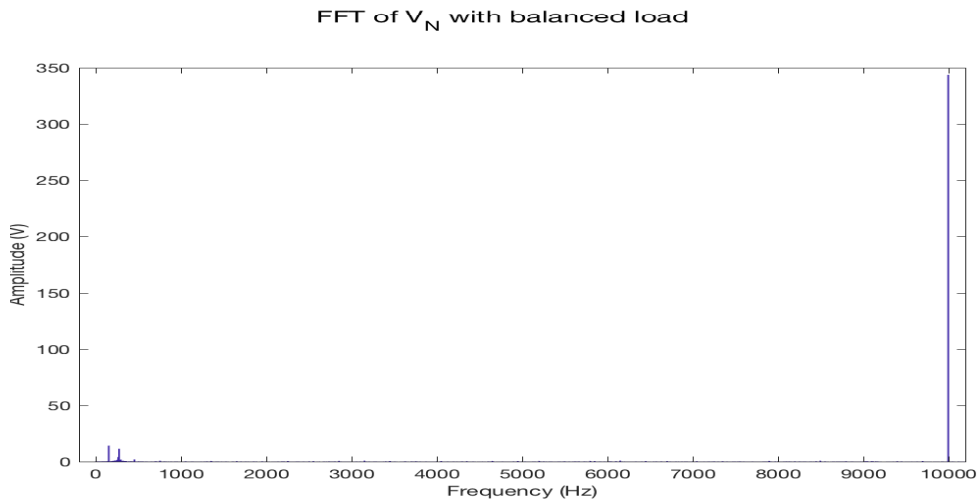
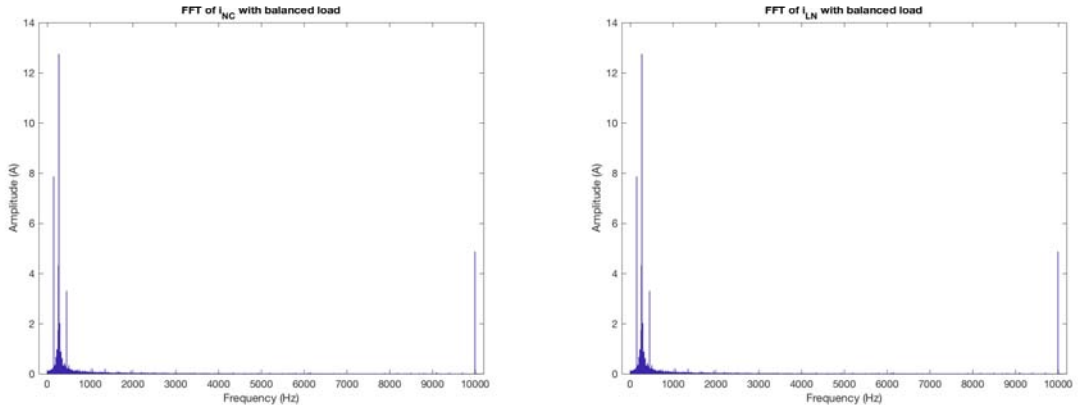


Figure 4.2.8: Case 23: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Harmonic spectrum of neutral voltage



(a) i_{NC} **(b)** i_{Ln}

Figure 4.2.9: Case 23: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) FFT of i_{NC}. Fig. (b) harmonic spectrum of i_{Ln}

50 Hz component, once again thanks to the fourth leg control. The harmonic content is similar to the zero voltage sequence U_o.

As it's possible to see in the fig. 4.2.9, the spectrums of the currents through the neutral inductor L_n and through the path which connects the filter to the neutral wire, are the same because the load is balanced and there isn't the neutral path connected to the neutral point of the load. There is not 50 Hz current flowing.

b. unbalanced load with *LCL*-filter

Using the same configuration and the same filter, an unbalanced load is connected and the results are shown in fig. 4.2.10-4.2.19.

In this case, due to the presence of unbalanced load, the currents will be unbalanced, this means that the current amplitude of each phase is different, as depicted in fig. 4.2.12. In terms of harmonic content, the -50 Hz component will be present, which is the negative sequence of the current, 4.2.10 and 4.2.11. The 50 Hz and -50 Hz values of the input and output currents are the same. The difference is the harmonic content. Like before the inverter current has high harmonic content that is filtered by the filter.

Despite the presence of an unbalance load which is producing unbalanced current, the voltage is balanced thanks to the positive and negative controllers, 4.2.13 and 4.2.14, where the positive sequence control imposes the reference value and the negative sequence control eliminates the -50 Hz due the unbalances.

As the case with balanced load, the zero sequence voltage U_o doesn't have switching and fundamental frequencies component, 4.2.16. The highest harmonic component is the fifth. Exactly like before, the neutral voltage U_N has just a high switching frequency component, 4.2.17, and

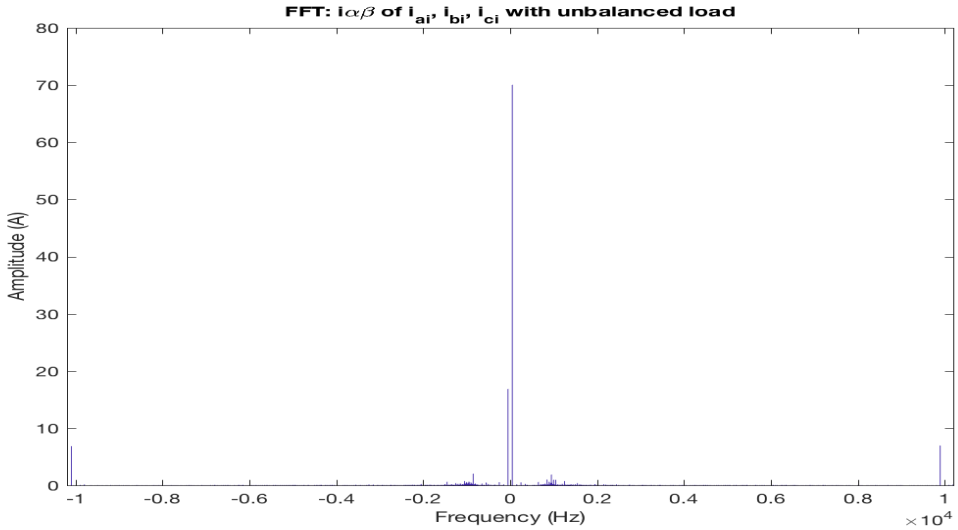


Figure 4.2.10: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of inverter current

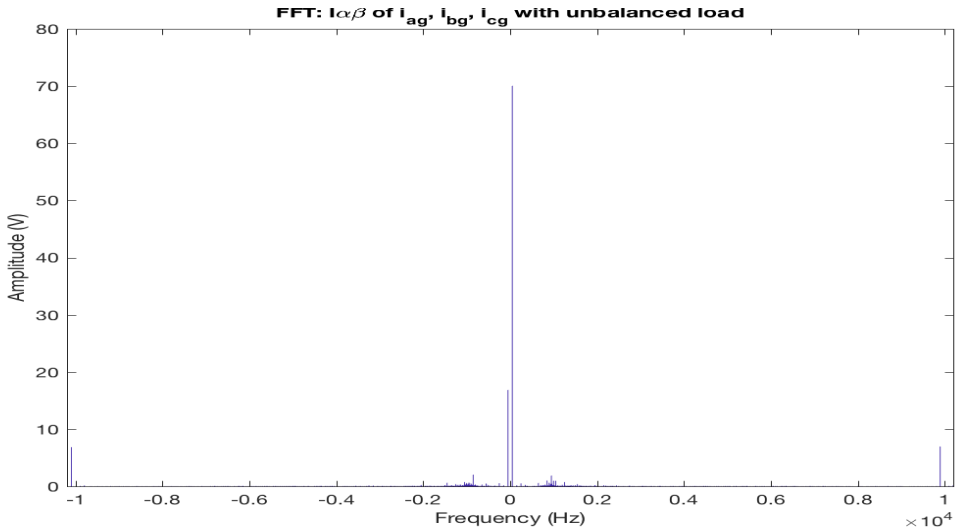
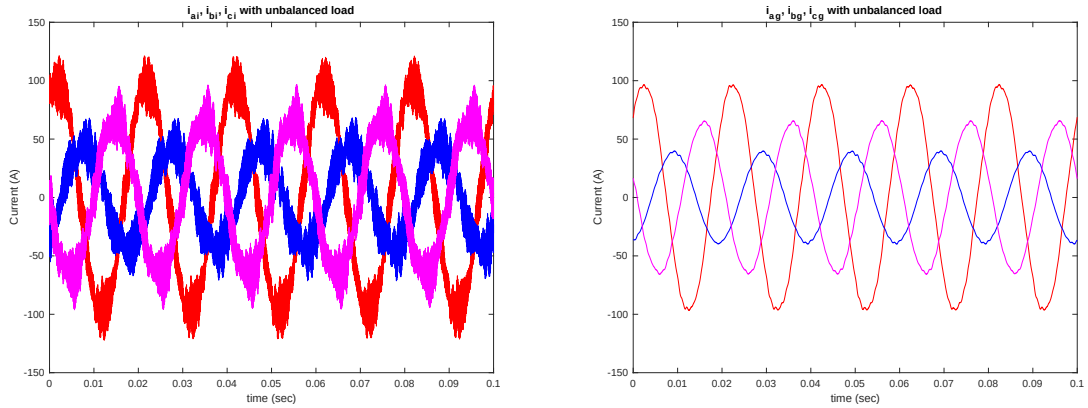


Figure 4.2.11: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of grid current



(a) **(b)**

Figure 4.2.12: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig.(a) waveform of inverter current current. Fig. (b) waveform of grid current

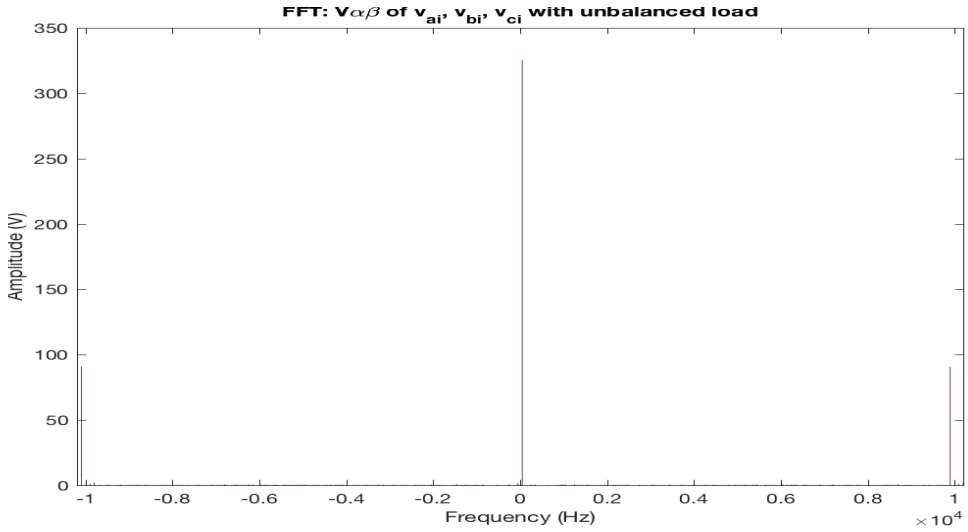


Figure 4.2.13: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of inverter voltage

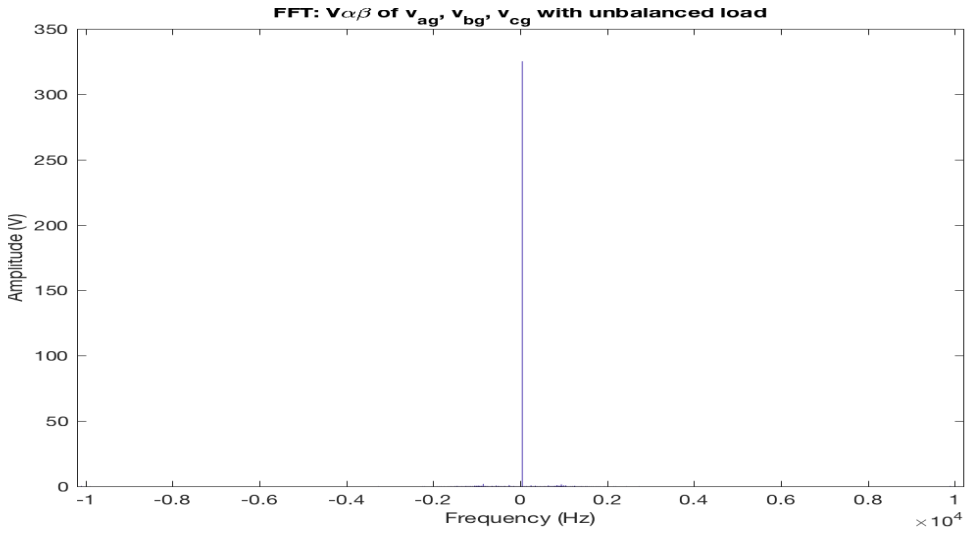
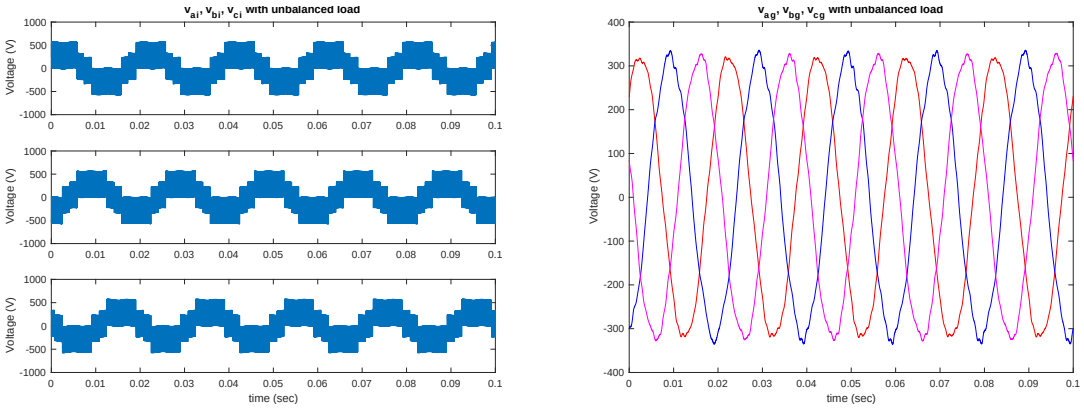


Figure 4.2.14: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of grid voltage



(a) **(b)**

Figure 4.2.15: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) waveform of inverter current. Fig. (b) waveform of grid voltage

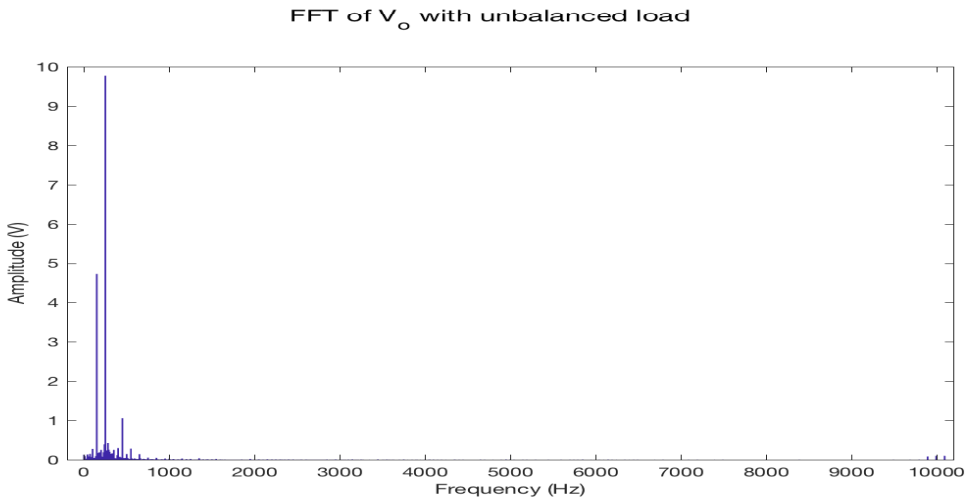


Figure 4.2.16: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of zero voltage sequence of grid voltage

the harmonic content is similar to the U_o.

Knowing now that the neutral point of unbalanced load is connected to the neutral path, i_{Ln}, in addition to the switching frequency, has 50 Hz component due to the presence of unbalances, which is flowing through the neutral path in the grid side i_{Ng}. i_{NC} is the same of the previous case because the capacitors of the filter C_f filters the switching frequency and it's not affected by the unbalances, as shown if figures 4.2.18 and 4.2.19.

Changing the filter, the behaviours of currents and voltages at fundamental, switching and -50 Hz frequencies are the same, just the harmonic content is different. The results are presented in the appendix A.1.

4.2.2 Split DC-link Capacitors

The following topology is analysed in the Chapter 2.2.2.

a. balanced load with *LCL*-filter

Starting with *LCL*-filter and balanced load, the results are depicted in fig. 4.2.20-4.2.28.

The input and output currents, 4.2.20 and 4.2.21, don't have -50 Hz component due to the balanced load effect. The inverter current has a higher harmonic content than the grid current, but in both cases the current is balanced, this means that current amplitude of each phase is equal, as shown in fig. 4.2.22.

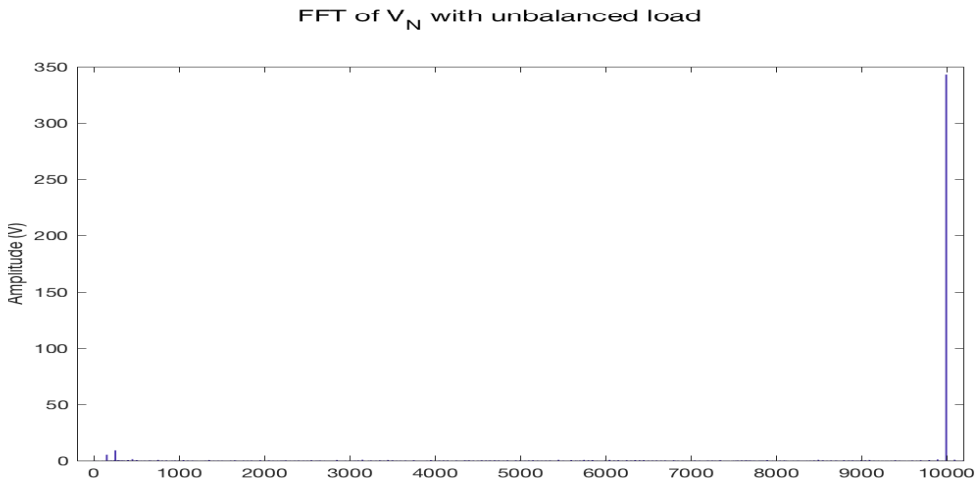
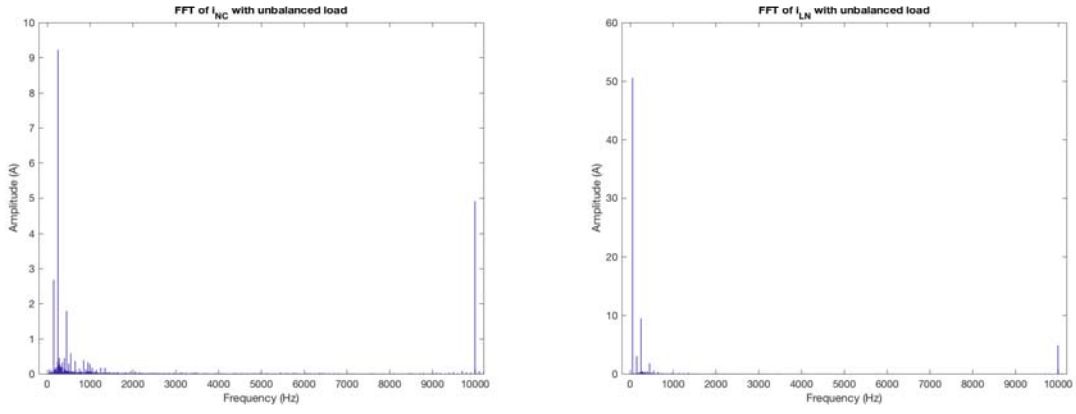


Figure 4.2.17: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of neutral voltage



(a) i_{NC} **(b)** i_{Ln}

Figure 4.2.18: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) FFT of i_{NC}. Fig. (b) FFT of i_{Ln}

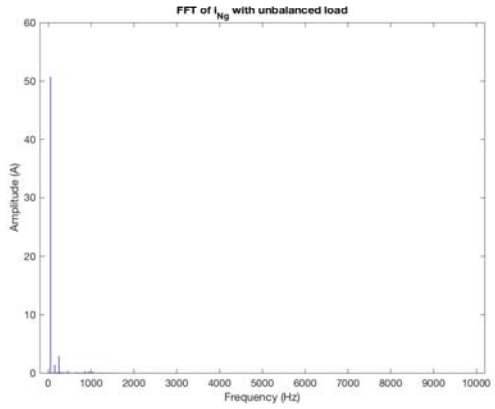


Figure 4.2.19: Case 23: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of i_{Ng}

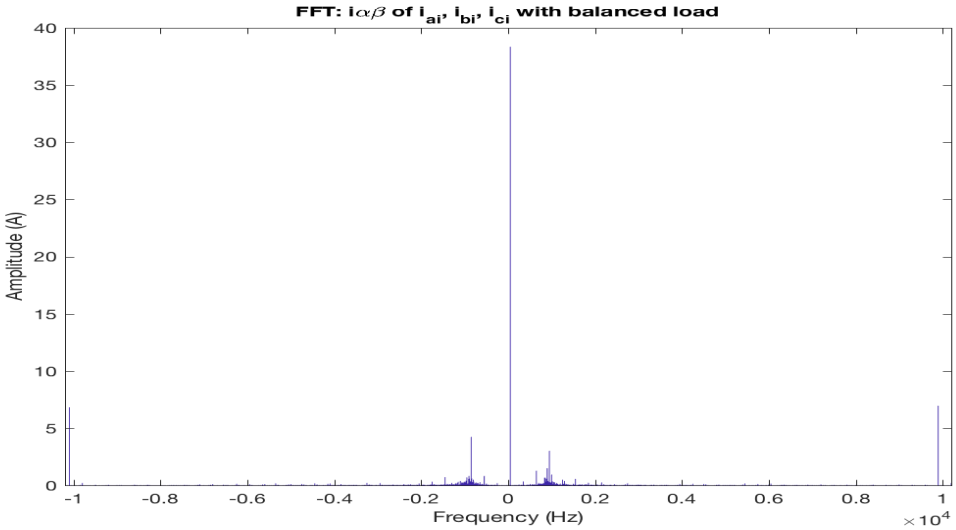


Figure 4.2.20: Case 29: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of inverter current

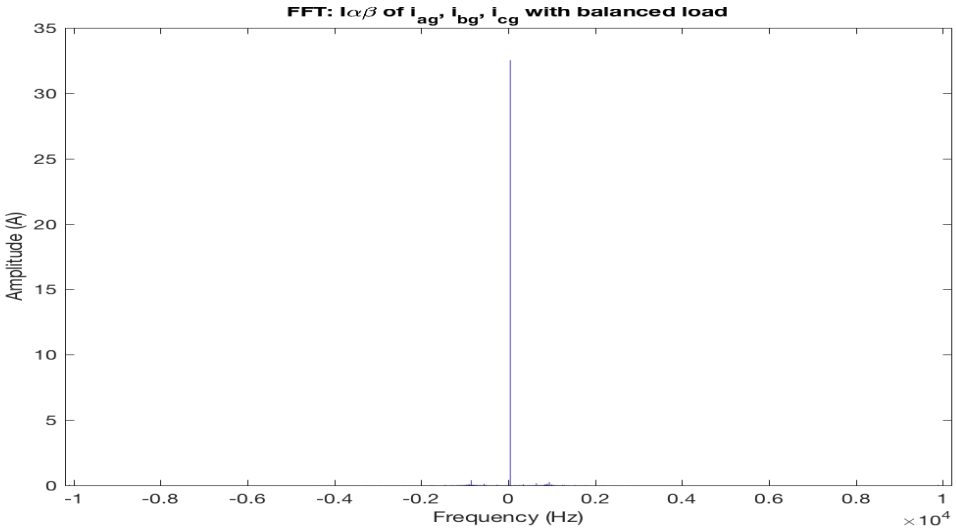
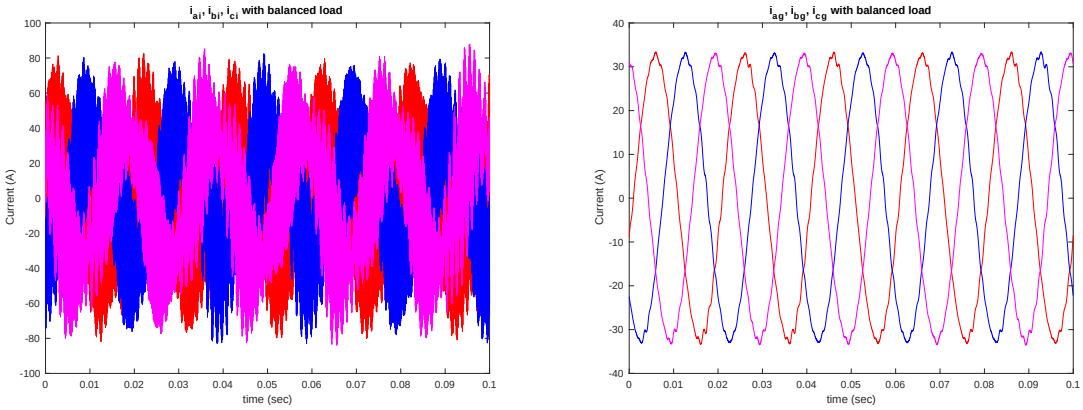


Figure 4.2.21: Case 29: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of the grid current



(a) **(b)**

Figure 4.2.22: Case 29: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) waveform of inverter current. Fig. (b) waveform of grid current

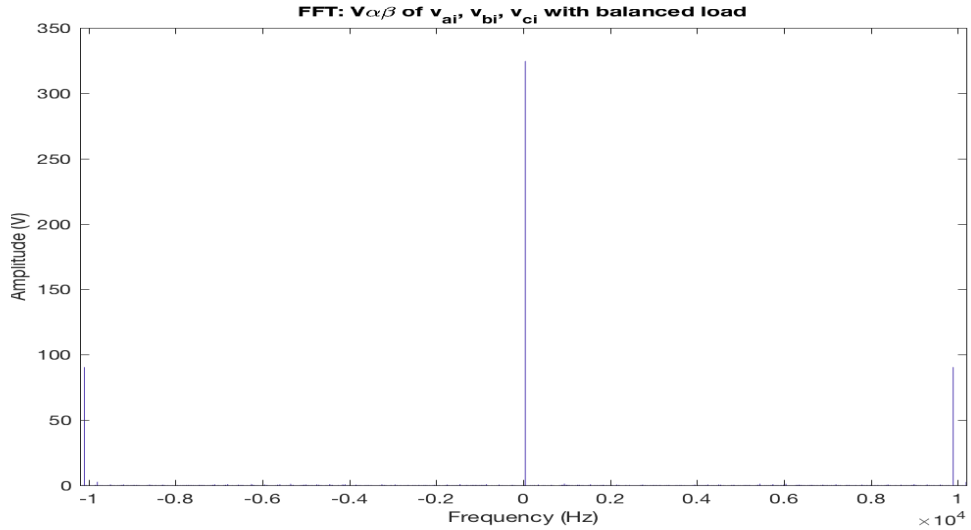


Figure 4.2.23: Case 29: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of the inverter voltage

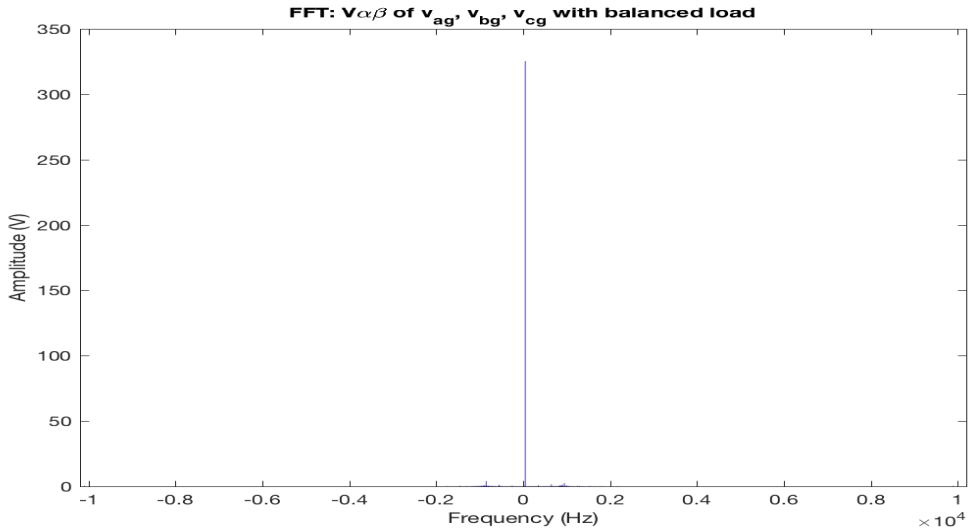
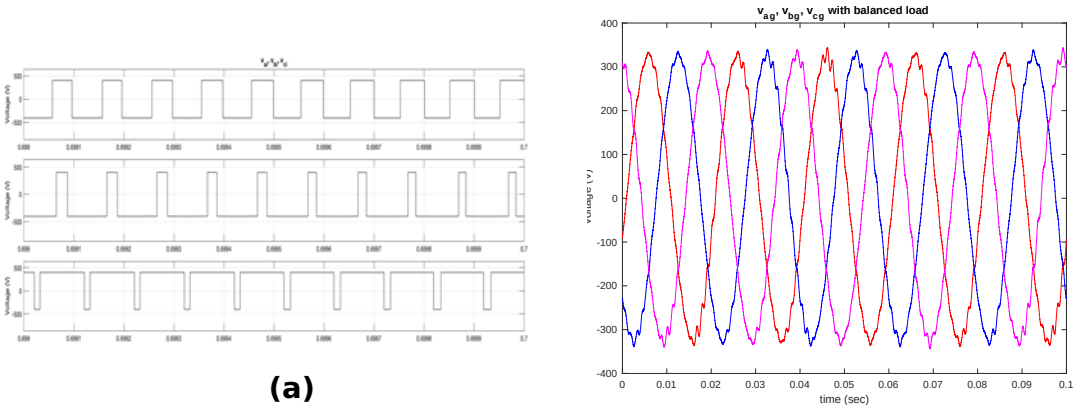


Figure 4.2.24: Case 29: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of the grid voltage



(a) **(b)**

Figure 4.2.25: Case 29: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) waveform of inverter voltage. Fig. (b) waveform of grid voltage

The voltage is depicted in fig.4.2.23 which is before the filter, and in fig. 4.2.23, which is after the filter. Once again, the grid voltage is perfectly balanced with the value of fundamental frequency equal to the target value.

In this topology, the zero voltage sequence U_o doesn't have a high switching frequency component, and the 50 Hz component is zero due the control, 4.2.26.

Being without the fourth leg, this configuration doesn't present the neutral control.

Connecting just a balanced load, the load is not connected to the neutral, for this reason the neutral current which flows through the capacitors C_f is the same of the current in the neutral path in the inverter side, connected to the middle point of the DC-link capacitors, 4.2.27. Not being unbalances, the currents i_{NC} and i_{Ni} don't present 50 Hz component. The half of i_{NC} flows in each of the two DC-link capacitors, as shown in fig. 4.2.28.

b. unbalanced load with *LCL*-filter

Using now the same configuration, just with an unbalanced load, the results are shown in fig. 4.2.29-4.2.37.

The currents, 4.2.29 and 4.2.30, is unbalanced due the use of unbalanced load. It presents -50 Hz due the unbalances.

Despite the load is unbalanced, the grid voltage is balanced thanks to the positive and negative sequence controls, 4.2.33.

The zero voltage sequence U_o is perfect controlled, without 50 Hz component. It presents a small component at switching frequency, like with a balanced load.

In this case, the current i_{NC} and i_{Ni} are not equal 4.2.36, because the

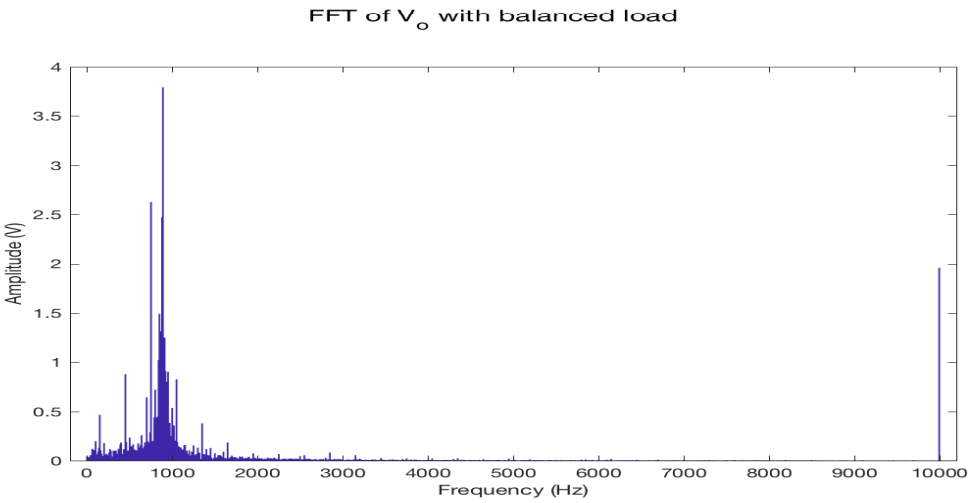
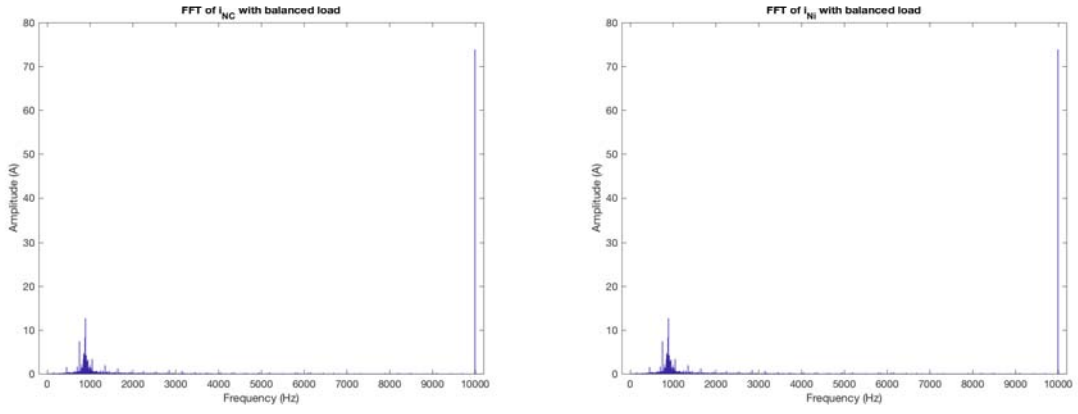


Figure 4.2.26: Case 29: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of zero voltage sequence



(a) i_{NC} **(b)** i_{Ni}

Figure 4.2.27: Case 29: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) FFT of i_{NC}; Fig. (b) FFT of i_{Ni}

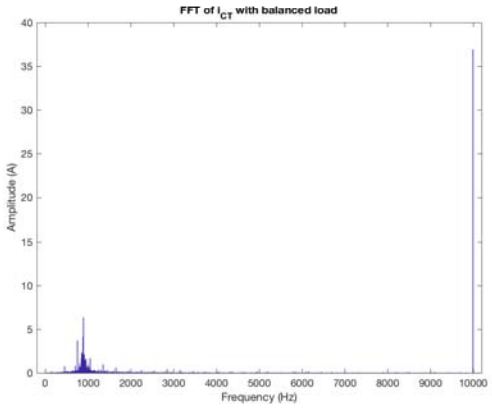


Figure 4.2.28: Case 29: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of i_{CT}

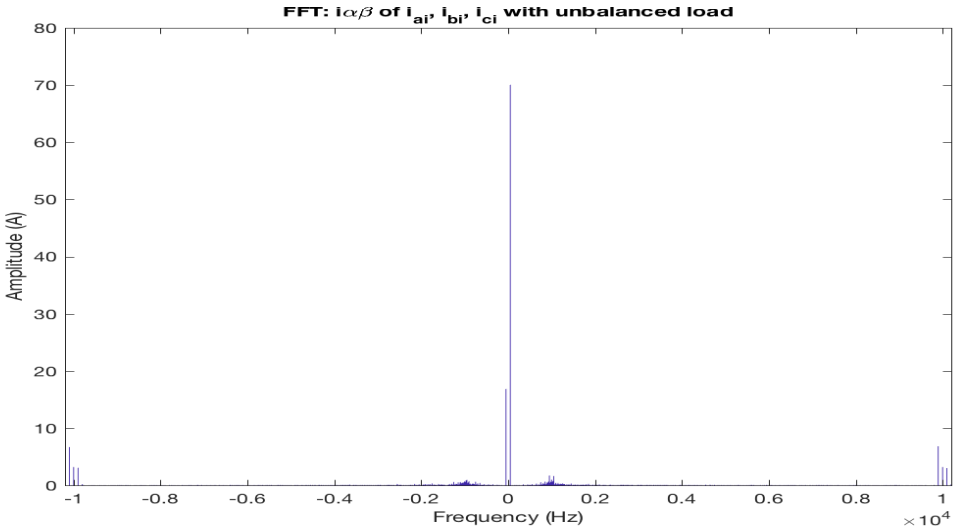


Figure 4.2.29: Case 29: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; FFT of inverter current

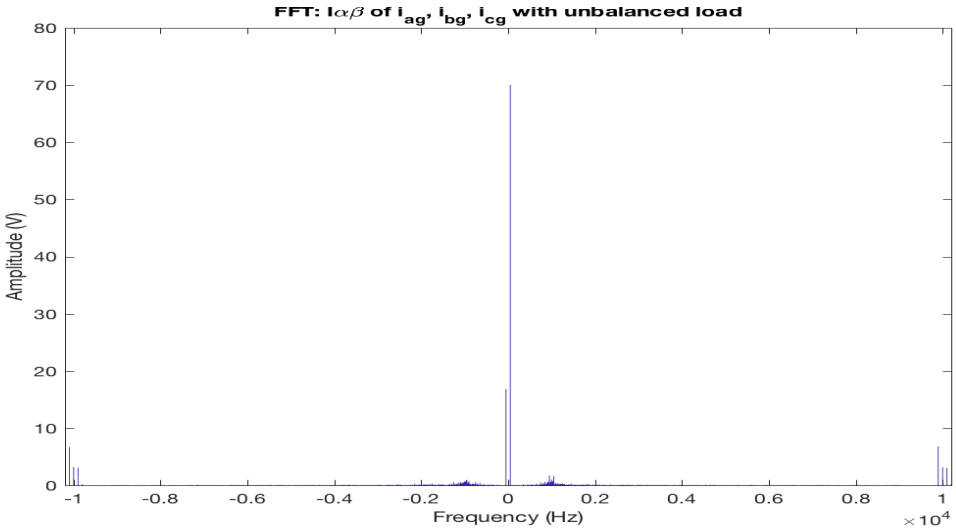
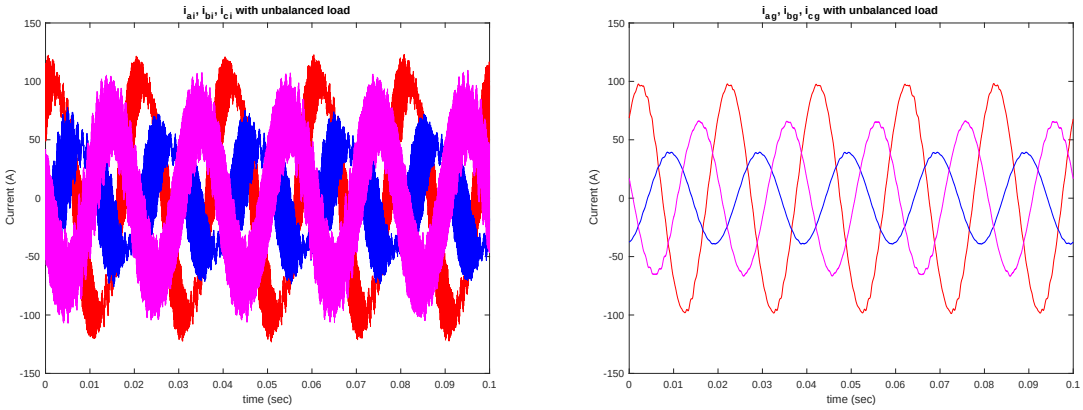


Figure 4.2.30: Case 29: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; FFT of grid current



(a) **(b)**

Figure 4.2.31: Case 29: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) waveform of inverter current; Fig. (b) waveform of grid current

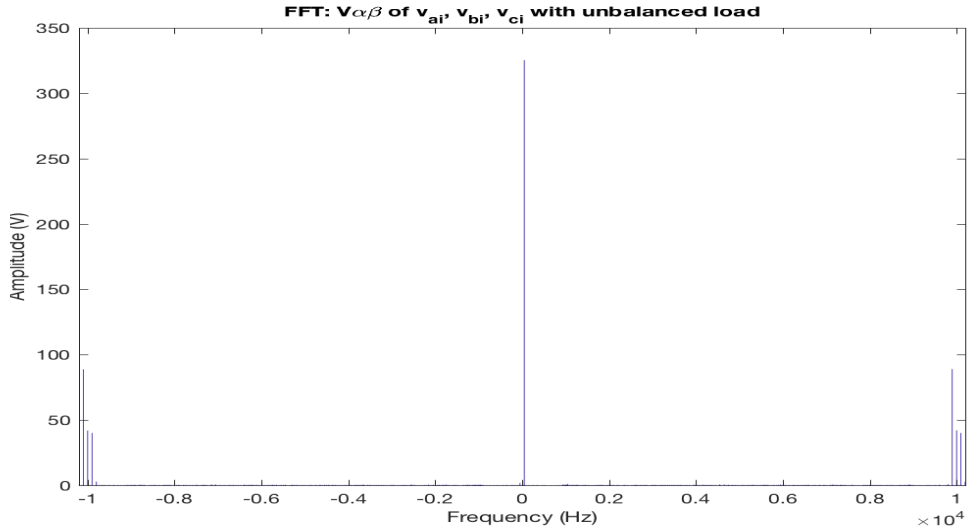


Figure 4.2.32: Case 29: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; FFT of inverter voltage

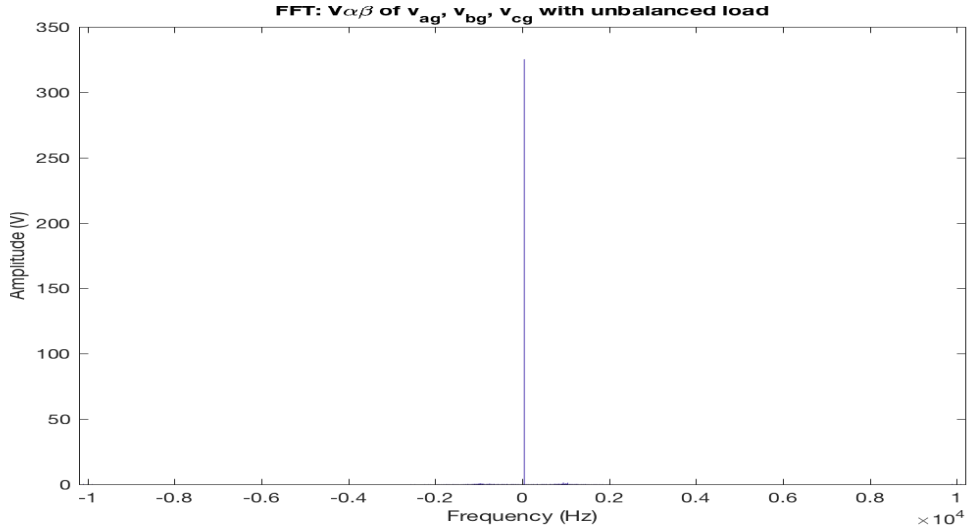


Figure 4.2.33: Case 29: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; FFT of grid voltage

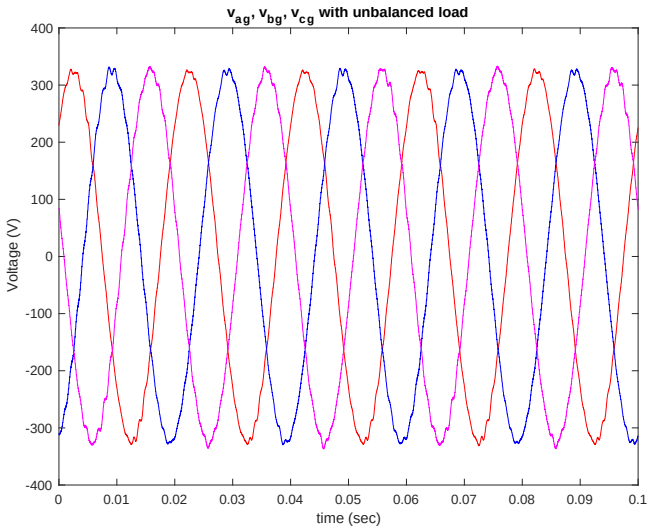


Figure 4.2.34: Case 29: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Waveform of grid voltage

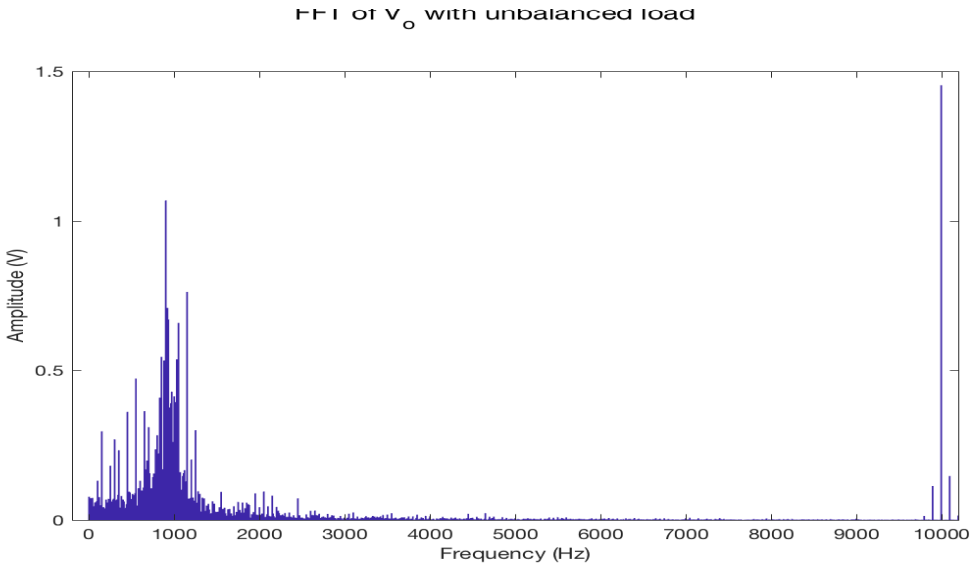
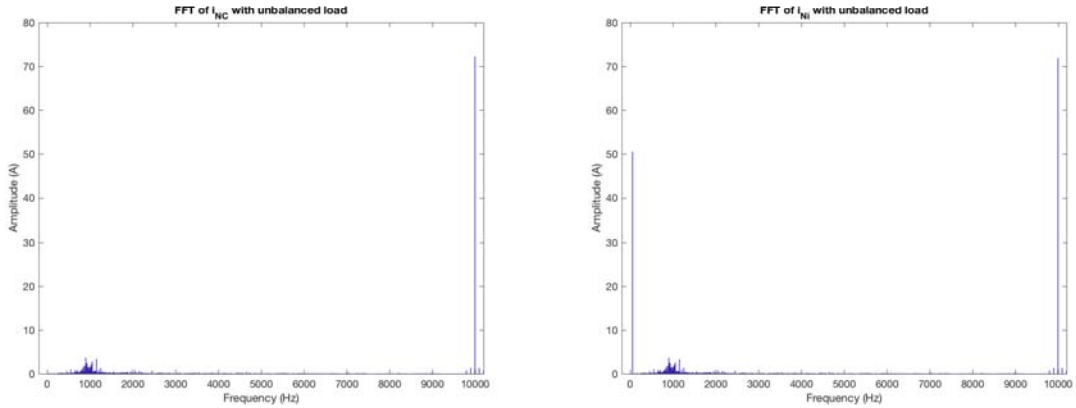
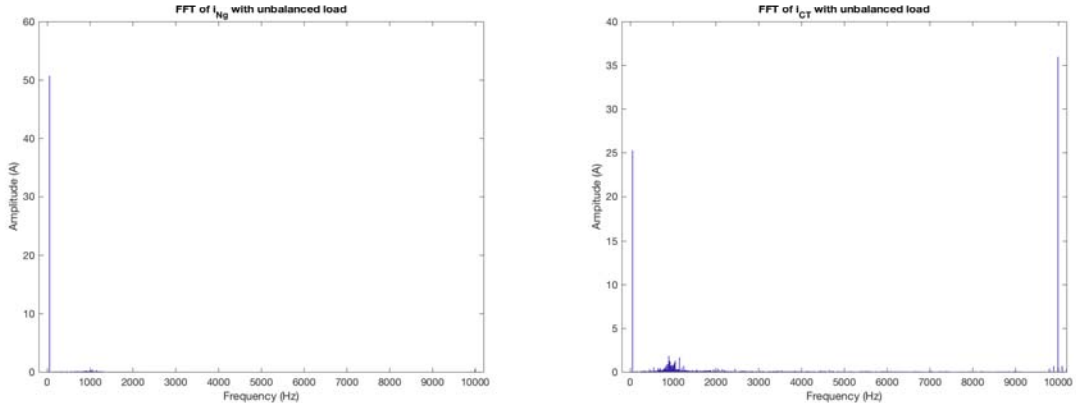


Figure 4.2.35: Case 29: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i;FFT of zero sequence voltage



(a) i_{NC} **(b)** i_{Ni}

Figure 4.2.36: Case 29: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) FFT of i_{NC}: fig. (b) FFT of $_{Ni}$



(a) i_{Ng} **(b)** i_{CT}

Figure 4.2.37: Case 29: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) FFT of i_{Ng}: fig. (b) FFT of $_{CT}$

last one has 50 Hz component once again, due to the presence of an unbalanced load which in connected to the neutral path. In fact, in the neutral path in the grid side, the current i_{Ng} presents not only 10 kHz component, but also a fundamental frequency component, 4.2.37 that flows through all the neutral path and also through the DC-link capacitors. In this way, the current through the capacitors in the DC-bus, with unbalanced load, not presents only 10 kHz but also component at 50 Hz.

Also in this case, changing the filter, the behaviours of currents and voltages at fundamental, switching and -50 Hz frequencies are the same, just the harmonic content is different. The results are presented in the appendix A.2.

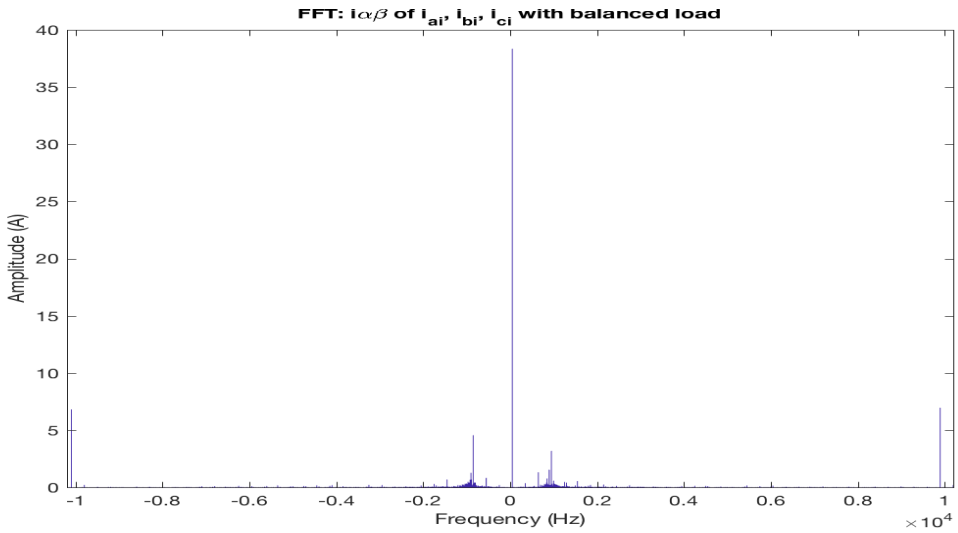


Figure 4.2.38: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter current

4.2.3 Independently Controlled Neutral Leg

This configuration is studied in Chapter 2.2.3.

a. balanced load with *LCL*-filter

The results of the controls with balanced load and *LCL*-filter are presented in the Figs. 4.2.38 - 4.2.47.

As it's possible to see in the 4.2.38 and 4.2.39 figures, both currents present only the 50 Hz component because of the load used to the simulation is balanced, therefor the negative component at -50 Hz is zero. The main difference between these currents is the harmonic distortion, that, obviously, will be higher in the inverter side and lower in the grid side due to the *LCL*-filter presence.

The same is valid for the voltages, 4.2.41 and 4.2.42, which don't present the component at - 50 Hz. The 50 Hz component value is equal to the reference chosen during the positive sequence control.

Thanks to the zero voltage control and fourth leg control with respectively resonant controllers, the output voltage doesn't present the 50 Hz homopolar component, fig. 4.2.44, and the neutral voltage, 4.2.45. Also in this configuration U_o has a small value at the switching frequency, equal to the value of U_N at the same frequency.

As it is possible to note in the figure 4.2.47, the current in the neutral path i_{Ni} and the current i_{NC} through to the filter's capacitors, are the same in this case because the simulation is just done with balanced load, and usually the balanced load is not physically connected to the neutral wire. They present a high value at high frequency, 10 kHz, which

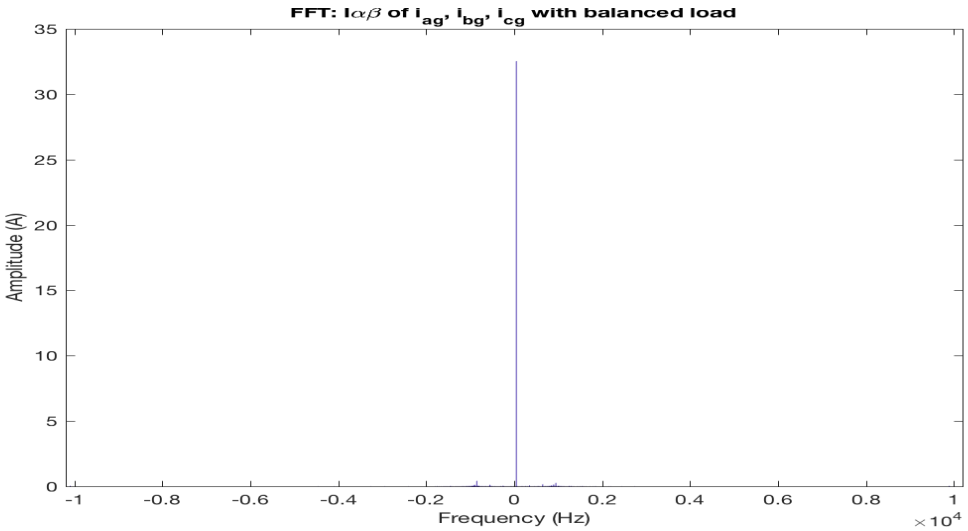
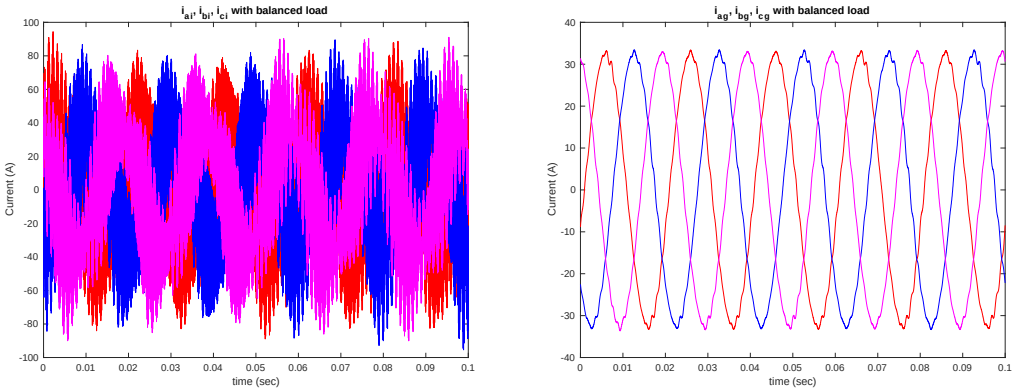


Figure 4.2.39: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. FFT of grid current



(a) i_{Ng} **(b)** i_{CT}

Figure 4.2.40: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) waveform of inverter current: Fig. (b) waveform of grid current

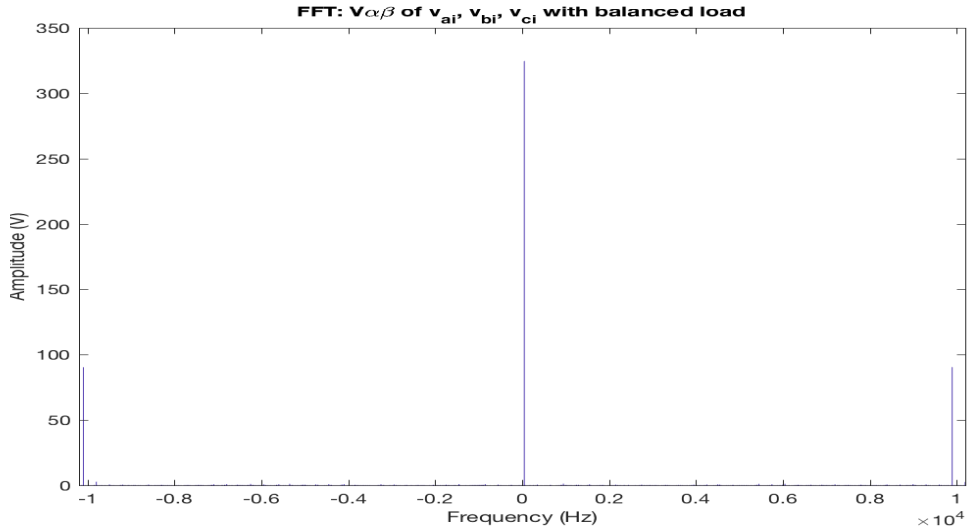


Figure 4.2.41: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter voltage

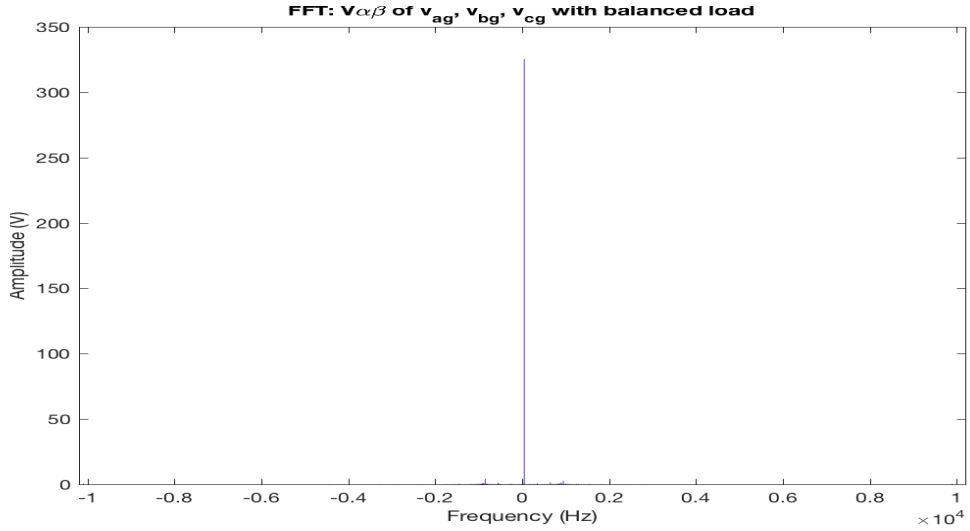


Figure 4.2.42: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid voltage

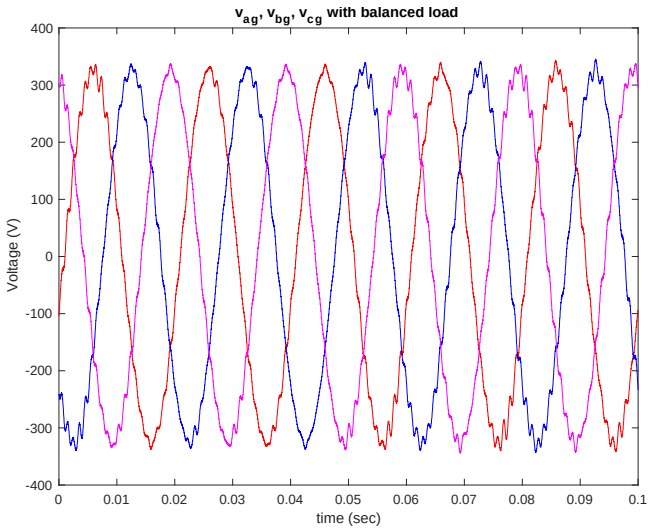


Figure 4.2.43: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Waveform of grid voltage

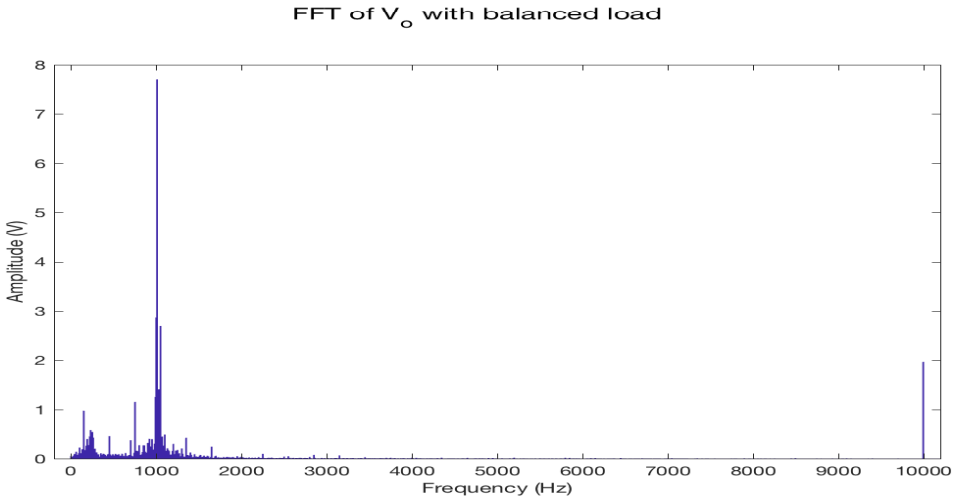


Figure 4.2.44: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of zero voltage sequence

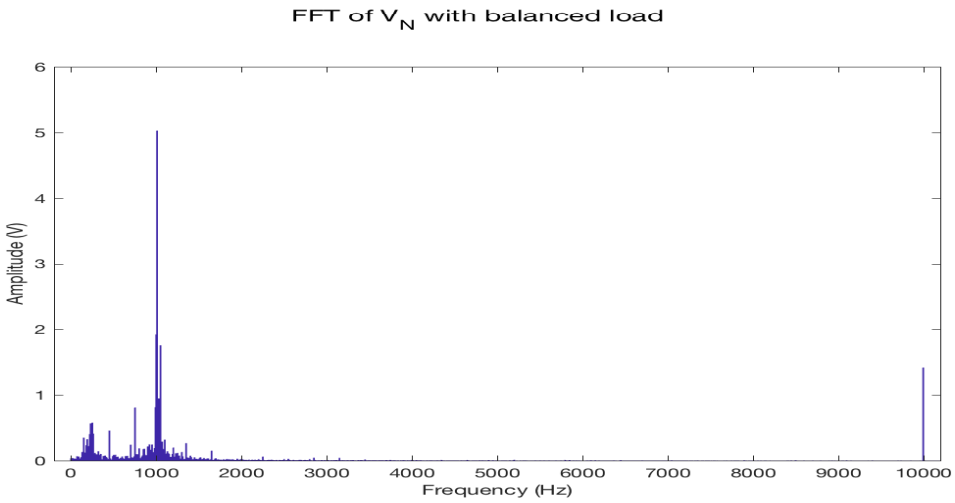
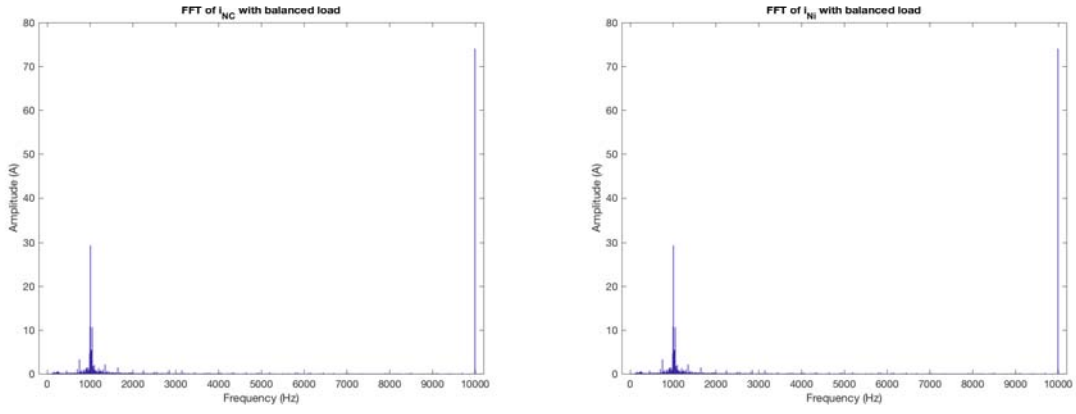
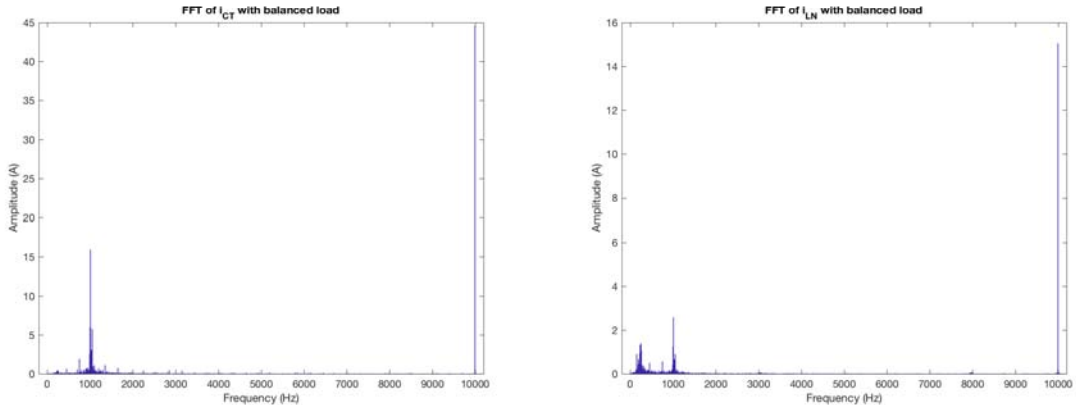


Figure 4.2.45: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of neutral voltage



(a) i_{NC} **(b)** i_{Ni}

Figure 4.2.46: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig.(a) FFT of i_{NC}; Fig (b) FFT of i_{Ni}



(a) i_{CT} **(b)** i_{Ln}

Figure 4.2.47: Case 1: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{CT}; Fig. (b) FFT of i_{Ln}

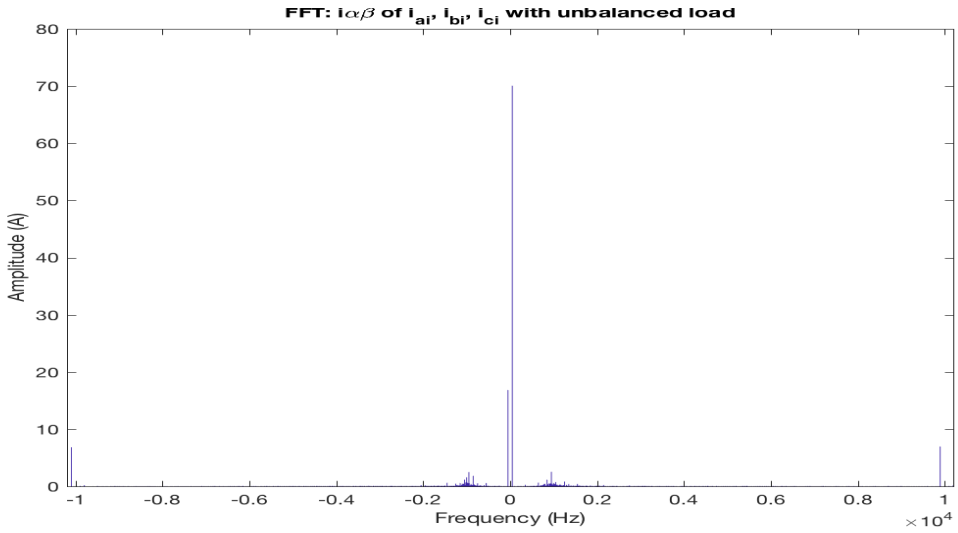


Figure 4.2.48: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter current

is the switching frequency and there isn't current to the fundamental frequency (50 Hz). The same applies to the current i_{Ln} through the inductor L_n and the current i_{CT} through the capacitors in the DC-link, where the value of 10 kHz component in the inductor and capacitors will depend on the values of each component.

b. unbalanced load with *LCL*-filter

Connecting now an unbalanced load, the results are depicted in fig. 4.2.48-4.2.58.

Conversely, with un unbalance load, the currents, 4.2.48 and 4.2.49, have not only the 50 Hz component, but also the -50 Hz due to the

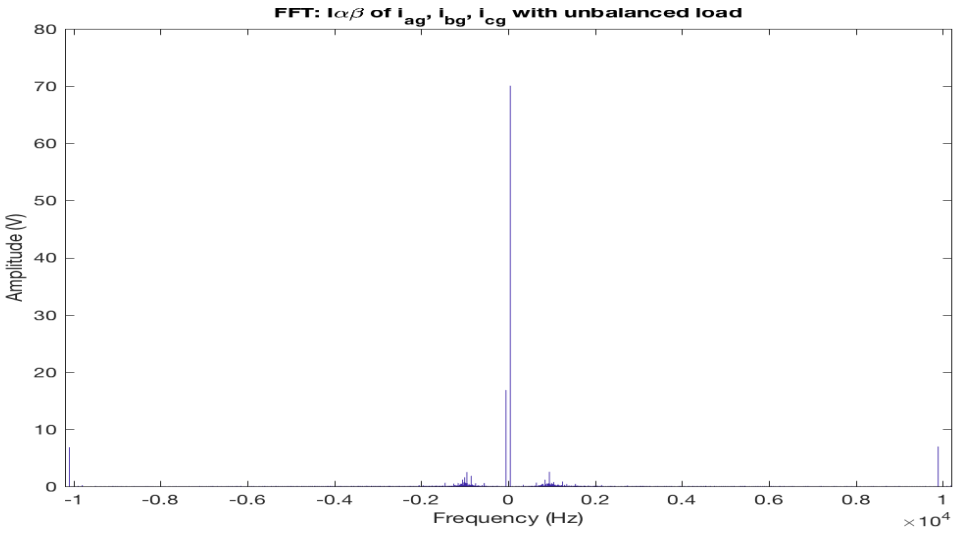
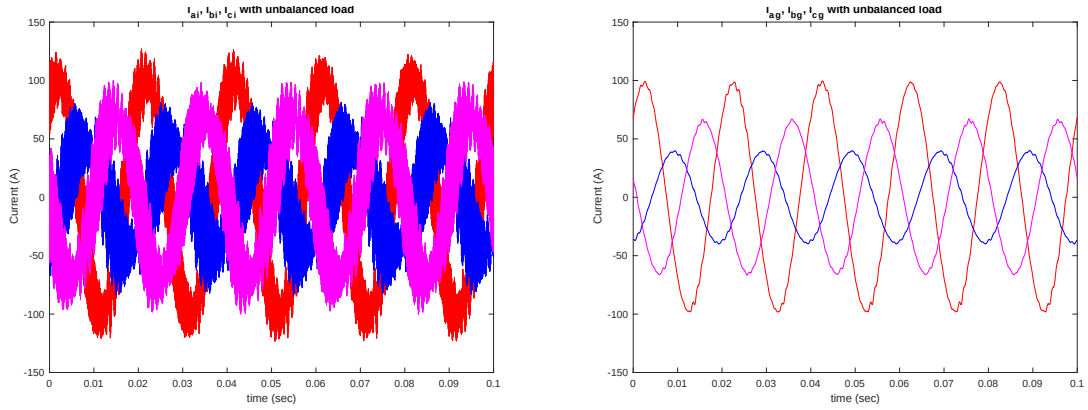


Figure 4.2.49: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid current



(a) **(b)**

Figure 4.2.50: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) waveform of inverter current; Fig. (b) waveform of grid current

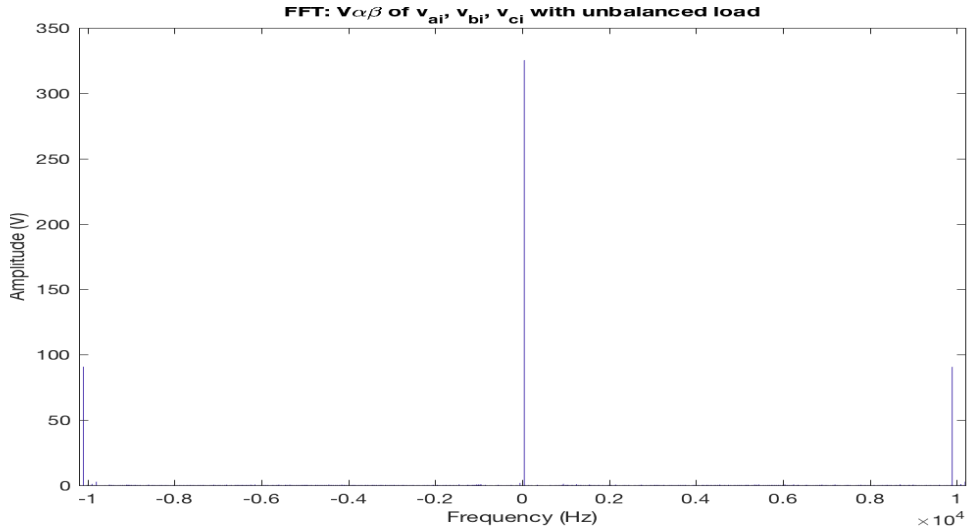


Figure 4.2.51: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter voltage

imbalances. The value of -50 Hz depends on the disequilibrium of the loads.

Despite the imbalance, the voltage is balanced, 4.2.51 and 4.2.52, thanks to the positive and negative controllers.

As the case with balanced load, the zero sequence voltage V_o, 4.2.54, and the neutral voltage v_N, 4.2.55, don't present the 50 Hz component due to the control.

The neutral wire, on the contrary, presents a current with a high value of 50 Hz component. More specifically, in the inverter side the current i_{Ni} has also a high value of 10 kHz component, 4.2.56, equal to i_{NC}, while in the load side the current i_{Ng} has just the 50 Hz component, 4.2.58.

The capacitors in the DC-link have just 10 kHz, while the 50 Hz component flows through the neutral inductor L_n and the value is the same of I_{Ni}. Despite this, i_{Ln} contains also a small component at switching frequency.

Facing now the same power converter configuration with the same type of control, the idea is to change the filter, from *LCL*-filter to *LC*-filter, and compare them.

What already said for the case with *LCL*-filter is valid with *LC*-filter, as explained in appendix A.3.

4.2.4 Independently Controlled Neutral Leg, without the connection between the filter and the neutral wire

This configuration is studied in Chapter 2.2.4.

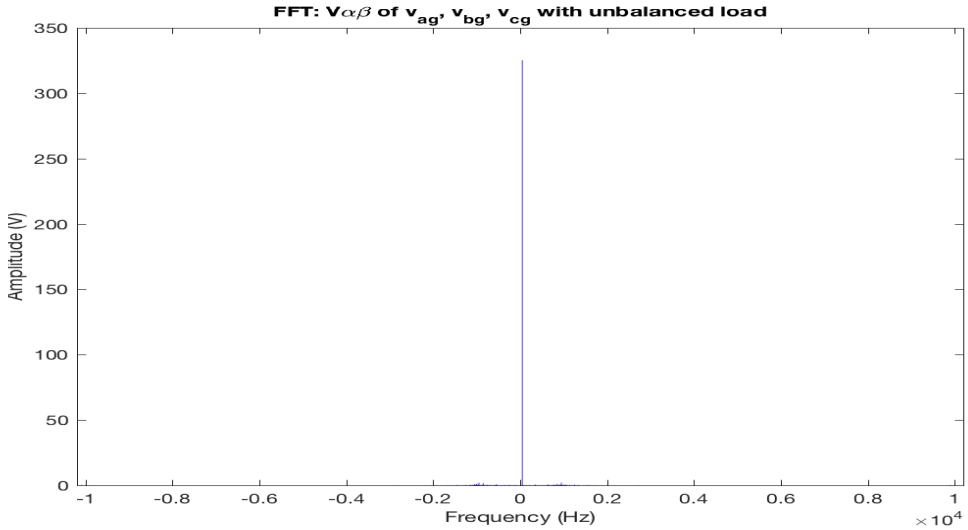


Figure 4.2.52: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid voltage

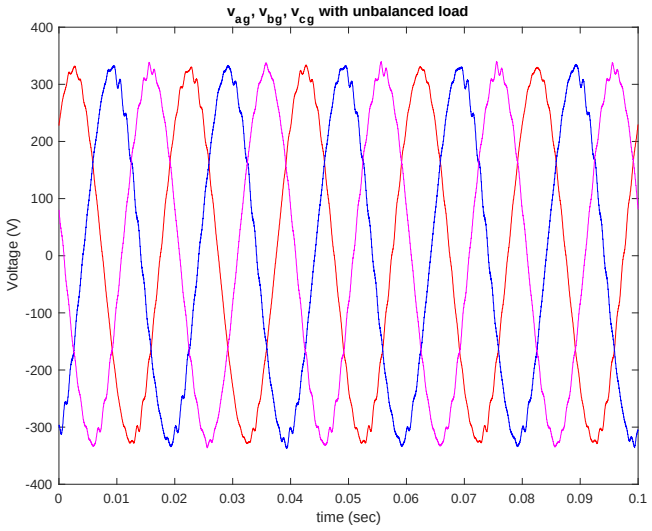


Figure 4.2.53: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Waveform of grid voltage

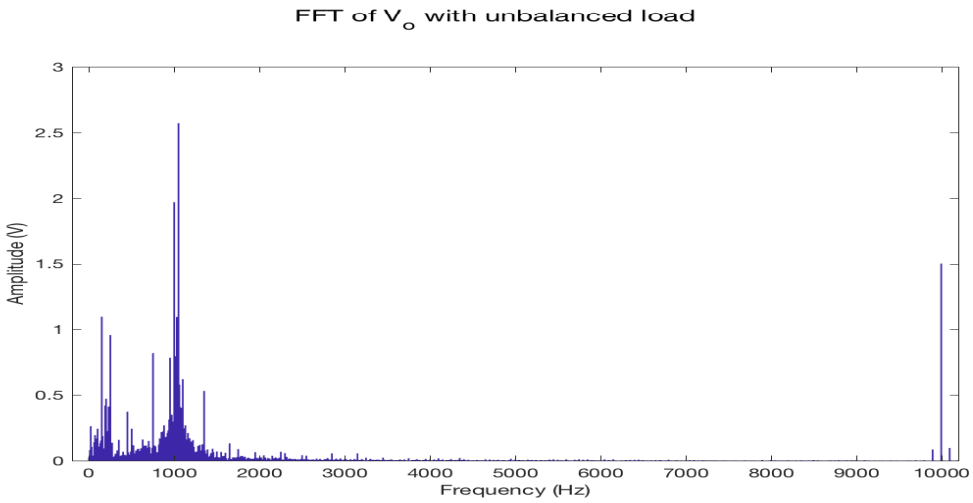


Figure 4.2.54: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Harmonic spectrum of zero sequence voltage

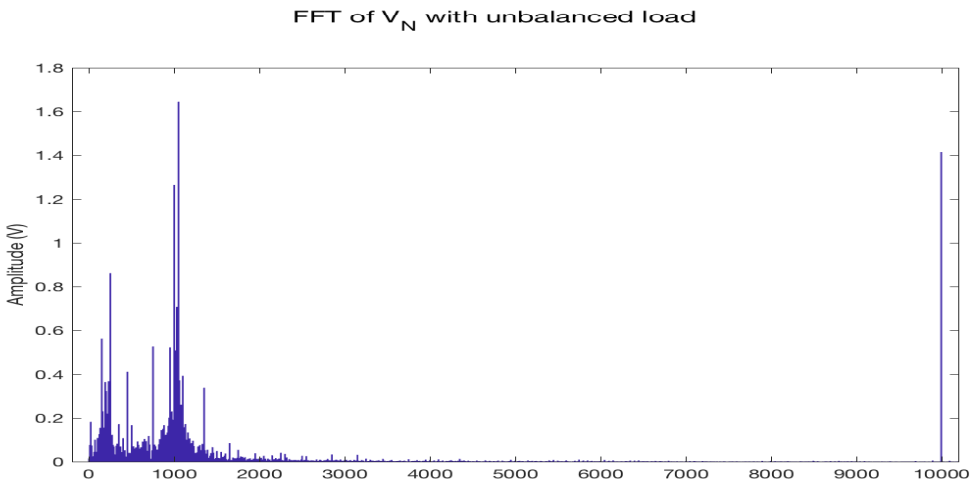
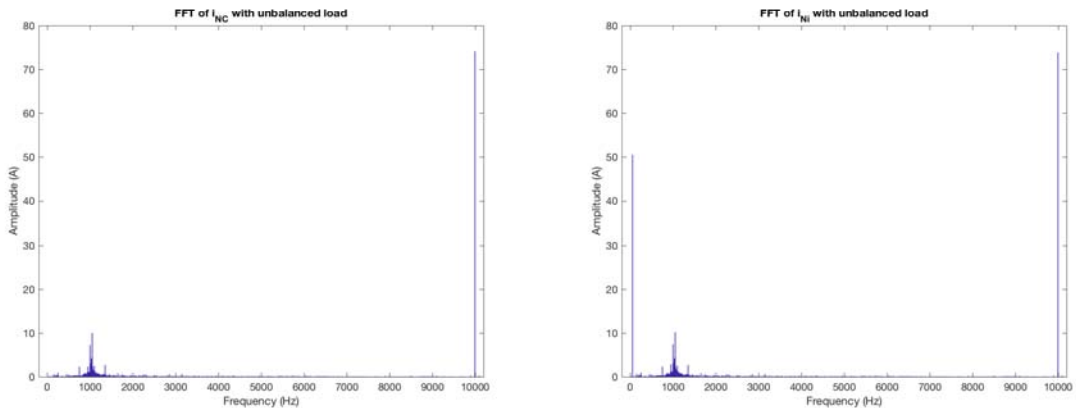
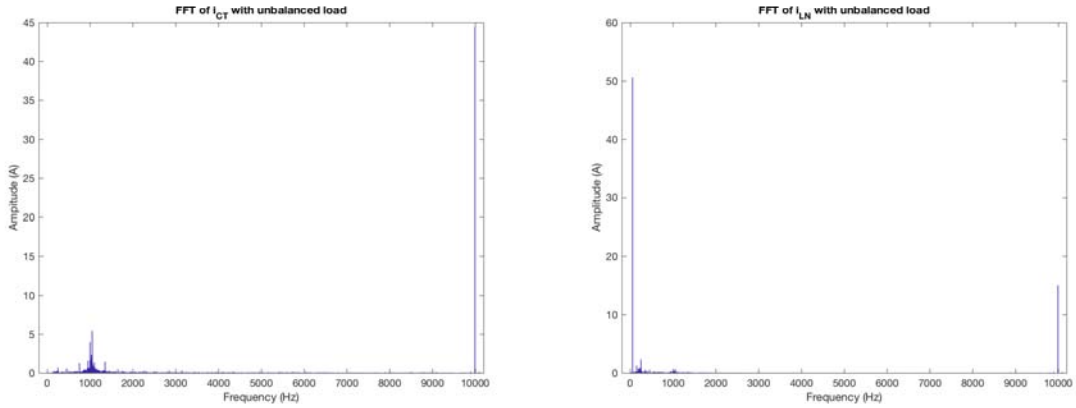


Figure 4.2.55: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Harmonic spectrum of neutral voltage



(a) i_{NC} **(b)** i_{Ni}

Figure 4.2.56: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{NC}; Fig. (b) FFT of i_{Ni}



(a) i_{CT} **(b)** i_{Ln}

Figure 4.2.57: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{CT}; Fig. (b) FFT of i_{Ln}

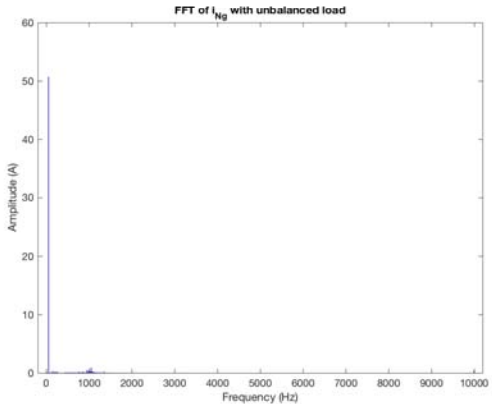


Figure 4.2.58: Case 1: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of i_{Ng}

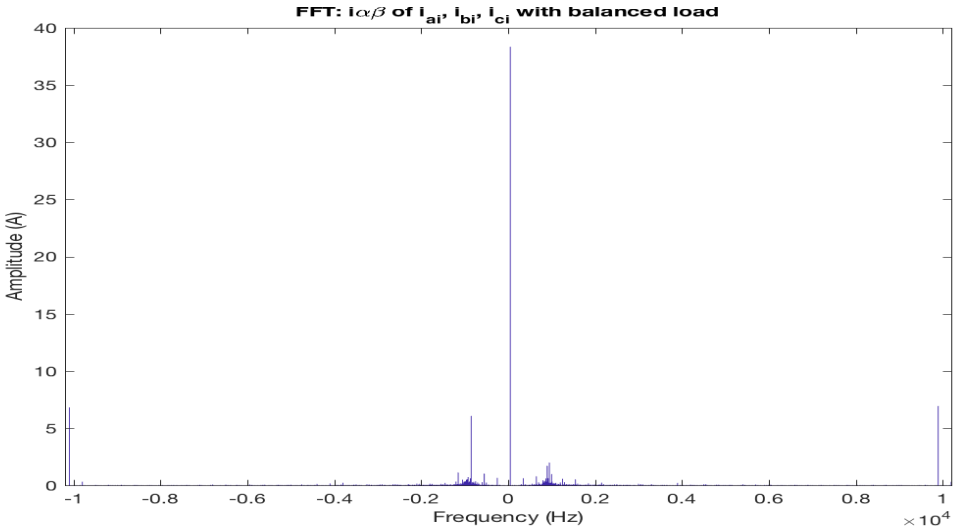


Figure 4.2.59: Case 31: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter current

a. balanced load with *LCL*-filter

Using an *LCL* filter and balanced load, the results are shown from fig. 4.2.59 to fig. 4.2.67. How it was possible to see before, the input, 4.2.59, and the output, 4.2.60, currents don't have the -50 Hz component but just the 50 Hz component due to balanced load.

The FFT of the input and output voltage is shown in fig. 4.2.62 and 4.2.63. The grid voltage is perfectly balanced, according the target imposed by the positive sequence, 4.2.64.

On the contrary of all the previously case, the zero voltage sequence U_o has a big switching frequency component due the lack of connection between the neutral path and the C_f, as depicted in fig. 4.2.65. Looking the spectrum of the neutral voltage U_N in fig. 4.2.66, it's clearly possible to say that is equal to zero.

It's interesting to note in this topology, with a balanced load, there isn't a neutral path. There is just current at switching frequency through the inductor L_n and the DC-split capacitors, as shown in fig. 4.2.67.

b. unbalanced load with *LCL*-filter

As in the previous topologies, due to an unbalanced load, the currents, 4.2.68 and 4.2.69, are unbalanced.

Despite the unbalances, the grid voltage doesn't have -50 Hz component, as depicted in fig.4.2.73, but it has a significant switching frequency component.

With an unbalanced load, the zero voltage sequence U_o has always a big component at switching frequency, but half than the case with balanced load.

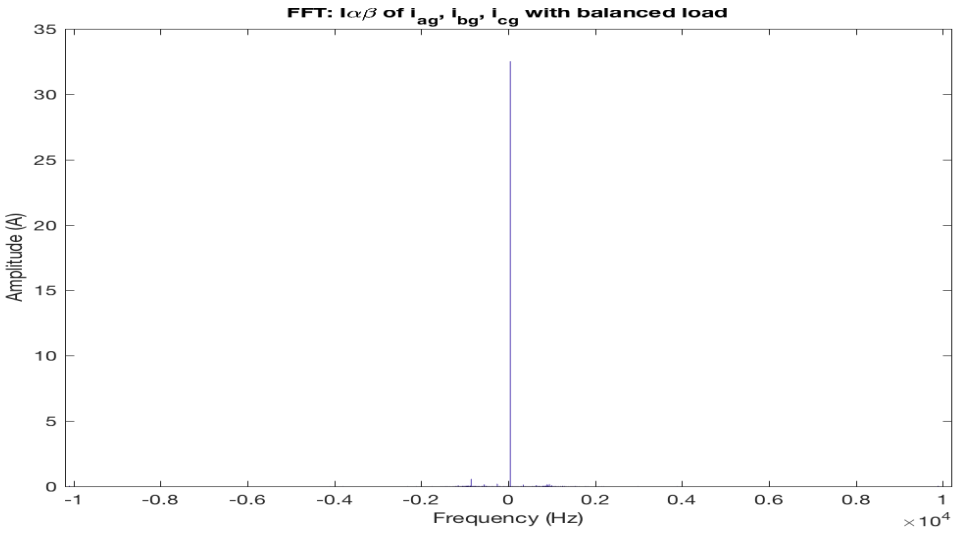
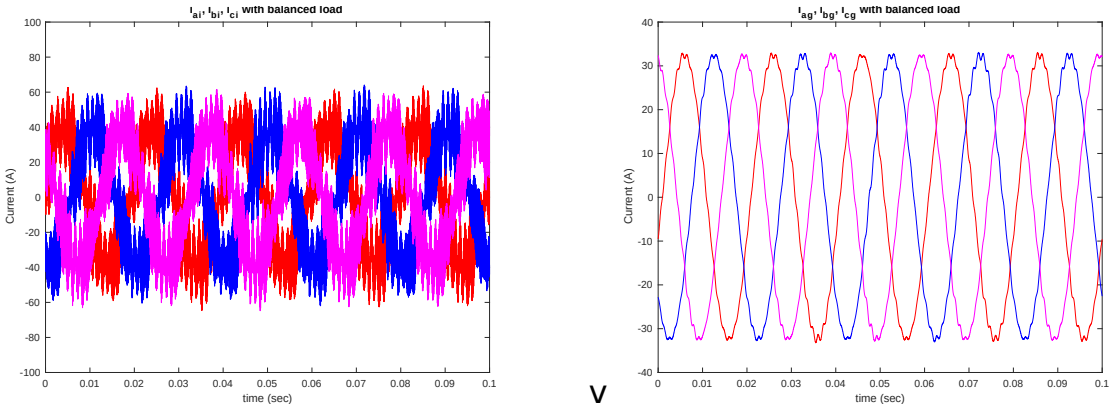


Figure 4.2.60: Case 31: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid current



(a) **(b)**

Figure 4.2.61: Case 31: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) waveform of inverter current; Fig. (b) waveform of grid current

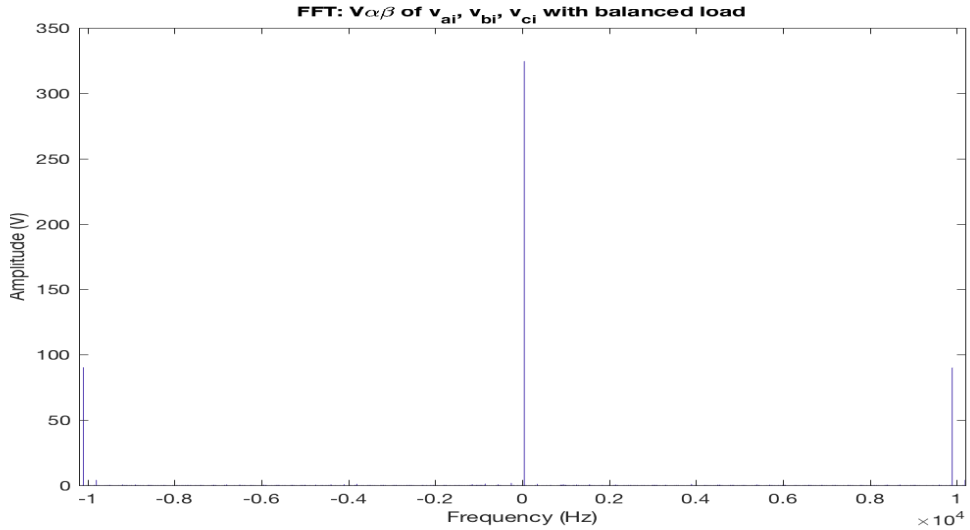


Figure 4.2.62: Case 31: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter voltage

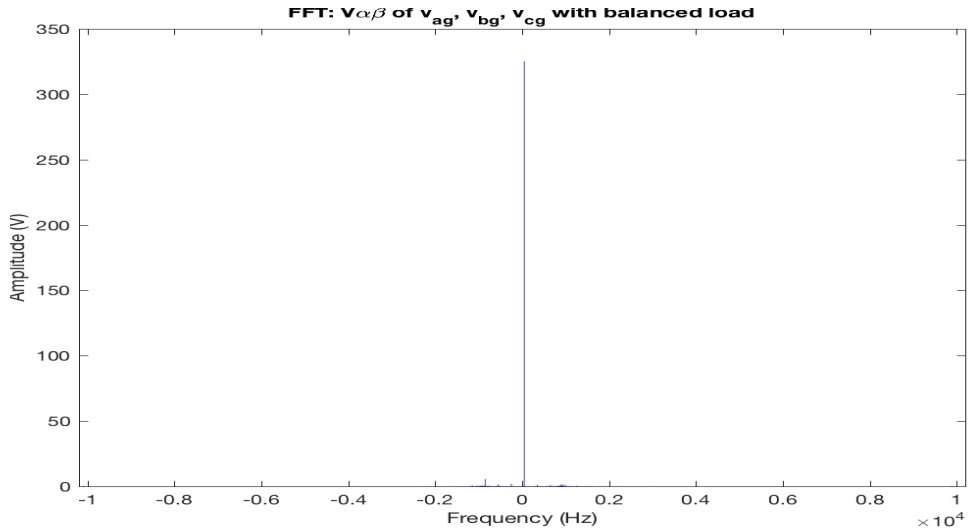


Figure 4.2.63: Case 31: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid voltage

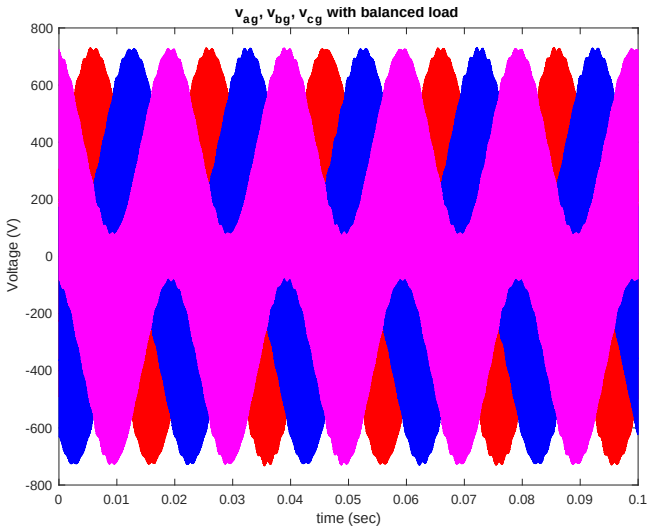


Figure 4.2.64: Case 31: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Waveform of grid voltage

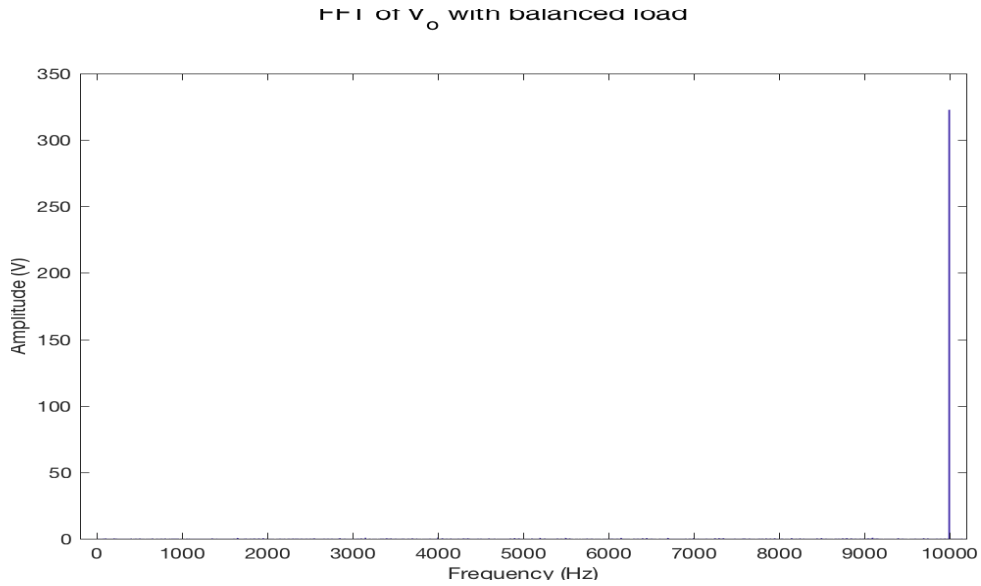


Figure 4.2.65: Case 31: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of zero voltage sequence

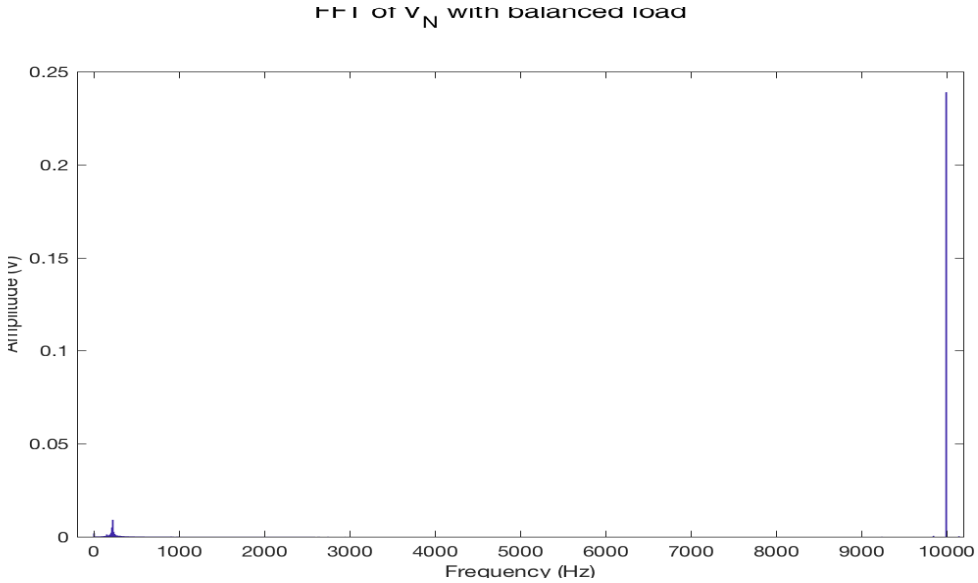
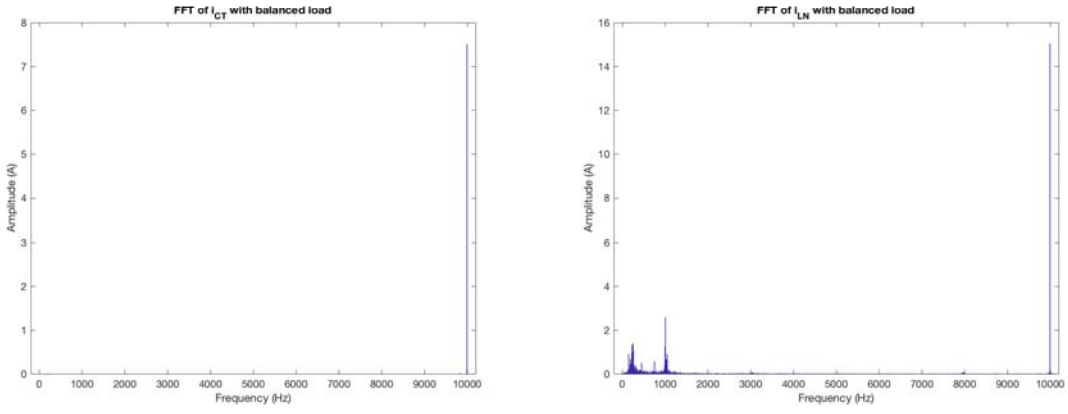


Figure 4.2.66: Case 31: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of neutral voltage



(a) i_{CT} **(b)** i_{Ln}

Figure 4.2.67: Case 31: *LCL*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{CT}; Fig. (b) FFT of i_{Ln}

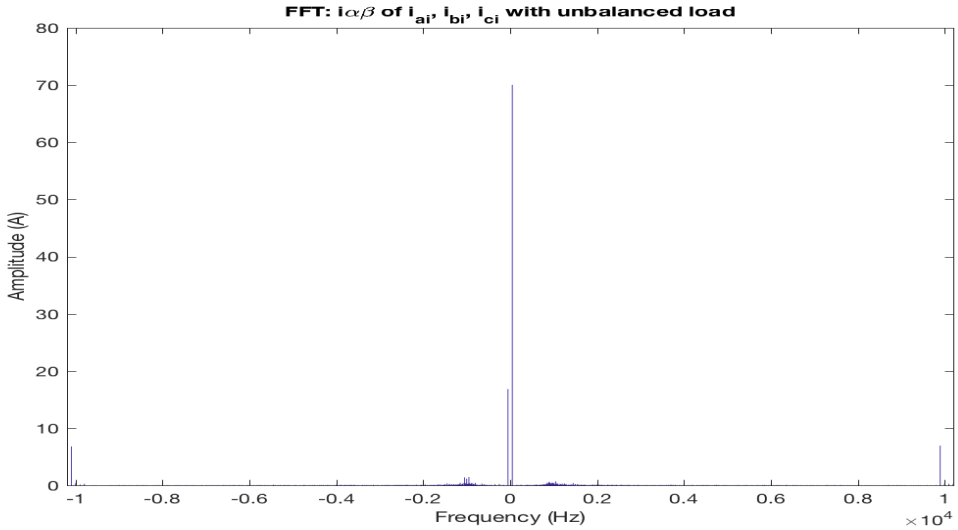


Figure 4.2.68: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter current

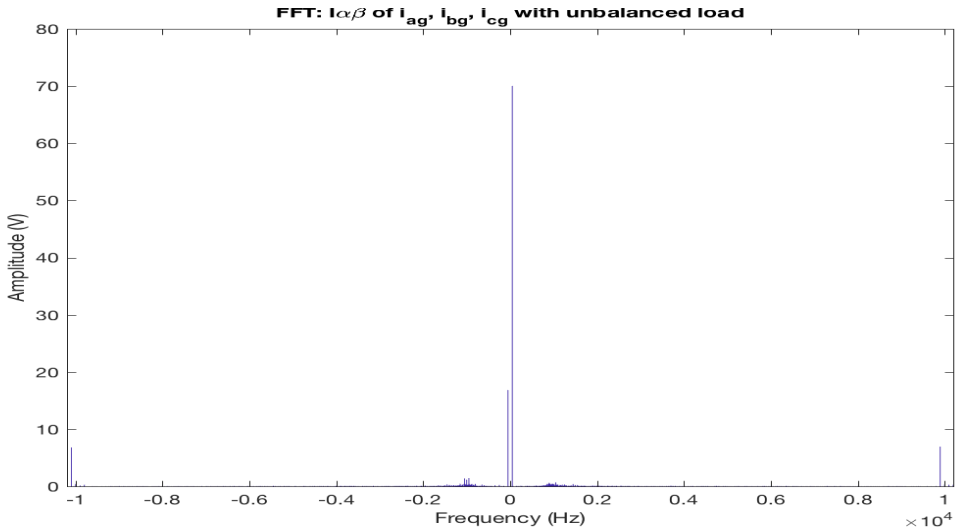
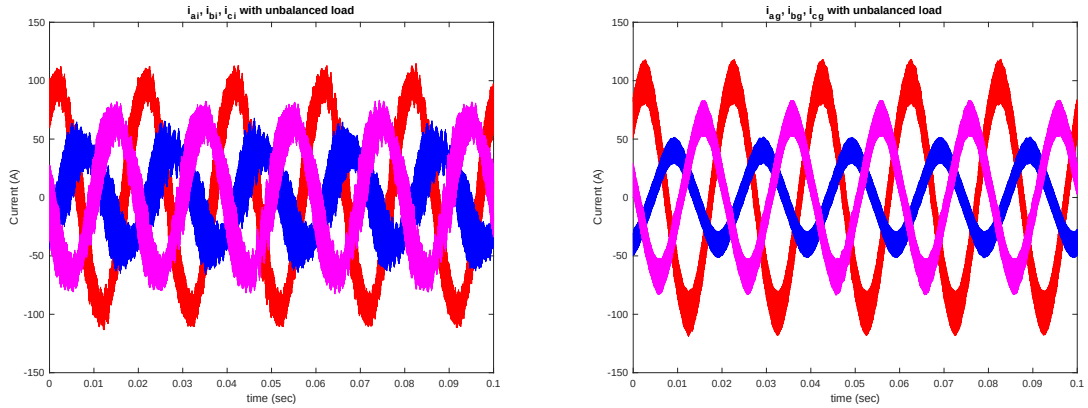


Figure 4.2.69: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid current



(a) **(b)**

Figure 4.2.70: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) waveform of inverter current; Fig. (b) waveform of grid current

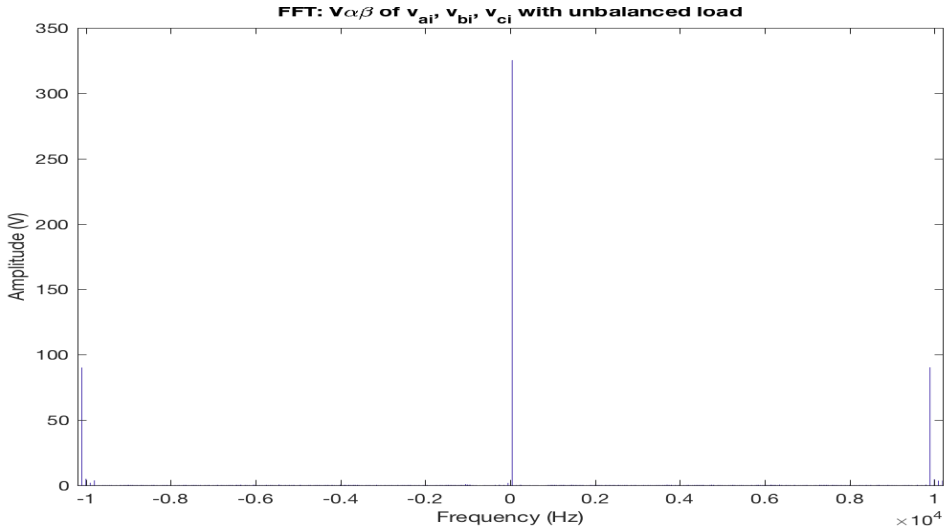


Figure 4.2.71: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter voltage

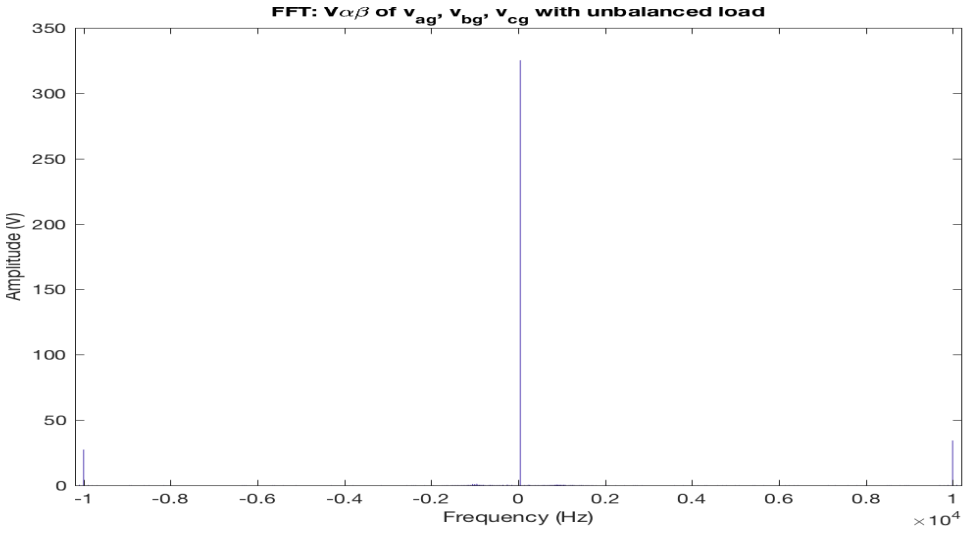


Figure 4.2.72

Figure 4.2.73: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid voltage

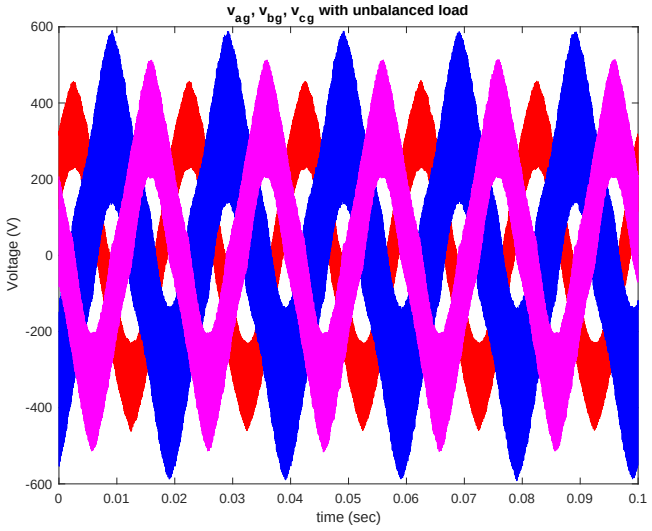


Figure 4.2.74: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Waveform of grid voltage

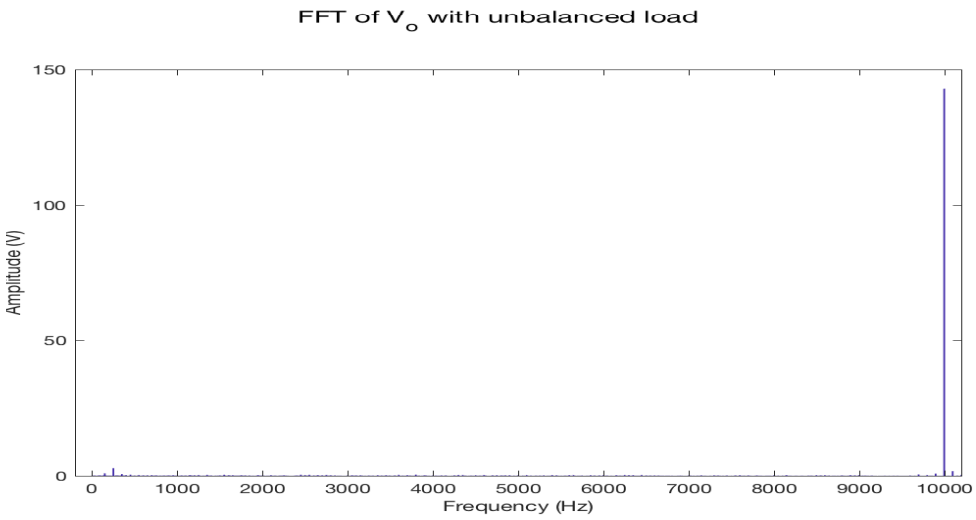


Figure 4.2.75: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of zero sequence voltage

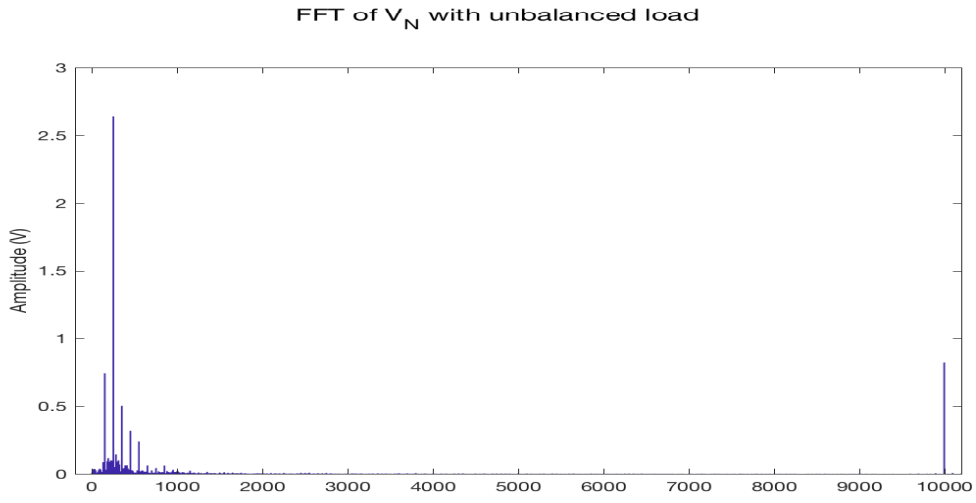


Figure 4.2.76: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of neutral voltage

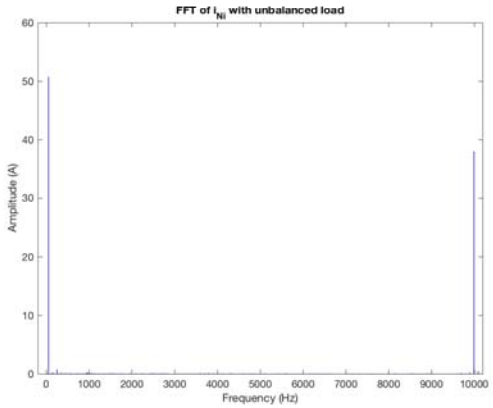
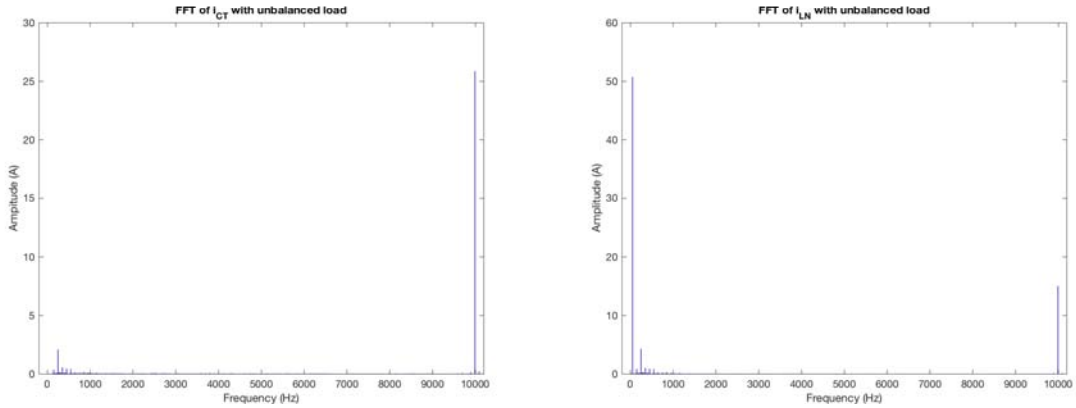


Figure 4.2.77: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of i_{Ni}



(a) i_{CT} **(b)** i_{Ln}

Figure 4.2.78: Case 31: *LCL*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{CT}; Fig.(b) FFT of i_{Ln}

As shown in fig. 4.2.76, U_N has harmonic content and 10 kHz component. it doesn't have component at fundamental frequency thanks to the control.

As just known, with unbalanced load, the neutral point of the load is connected to the neutral path. With unbalanced load in the neutral path there is a sinusoidal current i_{Ni} at 50 Hz, fig. 4.2.77, which flows through the neutral inductor L_n. i_{Ni} has also a big 10 kHz component, that will flow principally in the DC-link capacitors, and in the inductor, 4.2.78.

4.2.5 Resume

To have a general idea is useful to resume the components at 50 Hz, which is the fundamental frequency, and at 10 kHz, which is the switching frequency, of all the variables of each configurations in the table 4.8, where:

- Four legs is the conventional neutral leg topology, in section 2.2.1;
- Split capacitors is the split DC-link capacitors topology, in section 2.2.2;
- 4l+C is the independently controlled neutral leg configuration, in section 2.2.3;
- 4l+C* is the independently controlled neutral leg, without the connection between the filter and the neutral path, in section 2.2.4.

Analysing the table 4.8, it's possible to obtain the following conclusions:

- With balanced load, the inverter and the grid voltage, V_{abci} and V_{abcg}, are balanced and achieve perfectly the target value thanks to the positive sequence control. In all the configurations, they have a 50 Hz component and don't present a component at switching frequency.
- With unbalanced load, the inverter and the grid voltage, V_{abci} and V_{abcg}, are once again balanced and achieve perfectly the reference value in all the configurations. In the configuration with just split DC-link capacitors, V_{abci} has 10 kHz component is different from zero and also there is a big component at a frequency close to switching frequency. On the contrary, in the topology with split DC-link capacitors without the connection between filter and neutral path the grid voltage, V_{abcg}, has a component at 10 kHz.
- With balanced load, the inverter and the grid current, I_{abci} and I_{abcg}, are balanced, without 10 kHz.
- With unbalanced load, the inverter and the grid current, I_{abci} and I_{abcg}, are obviously unbalanced. In the topology 4l+C*, which is the independently controlled neutral leg, without the connection between the filter and the neutral path, studied in section 2.2.4, the grid current presents a 10 kHz component, while the configuration with the split DC-link capacitors, has 10 kHz in the inverter current.
- Forgetting the configuration with split DC-link capacitors topology, view in section 2.2.2, because it doesn't have the neutral inductor L_n, in the case with balanced load, in the current i_{Ln} there isn't 50 Hz. The component at 50 Hz is present with an unbalanced load, due obviously to the unbalances of the load. The harmonic content at switching frequency is independent from the nature of the load. The component at switching frequency is lower in the configuration with just the four legs.

Table 4.8: Resume: values at fondamental and switching frequencies

Topology	V_{abcg}				V_{abci}				I_{abcg}				I_{abci}			
	balanced		unbalanced		balanced		unbalanced		balanced		unbalanced		balanced		unbalanced	
	50Hz	10KHz	50Hz	10KHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz
Four legs	325	0	325	0	325	0	325	0	32	0	67	0	38	0	70	0
Split Capacitors	325	0	325	0	325	0	325	42	32	0	67	0	38	0	70	3
4l+C	325	0	325	0	325	0	325	0	32	0	67	0	38	0	70	0
4l+C*	325	0	325	34	325	0	325	5	32	0	67	4	38	0	70	0

Topology	i_{Ln}				i_{Ni}				i_{Ng}			
	balanced		unbalanced		balanced		unbalanced		balanced		unbalanced	
	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz
Four legs	0	5	50	5	0	5	50	5	0	0	50	0
Split Capacitors	/	/	/	/	0	73	50	73	0	0	50	0
4l+C	0	15	50	15	0	74	50	74	0	0	50	0
4l+C*	0	15	50	15	0	0	0	38	0	0	50	38

Topology	U_o				U_N				i_{CN}				i_{NC}			
	balanced		unbalanced		balanced		unbalanced		balanced		unbalanced		balanced		unbalanced	
	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz	50Hz	10kHz
Four legs	0	0	0	0	0	344	0	344	/	/	/	/	0	5	0	5
Split Capacitors	0	2	0	2	/	/	/	/	0	36	25	36	0	73	0	73
4l+C	0	2	0	2	0	2	0	2	0	44	0	44	0	74	0	74
4l+C*	0	323	0	143	0	0	0	0	0	7	0	26	/	/	/	/

- In the neutral path, with balanced load, there isn't current with component at fundamental frequency. On the contrary, this happens when there are unbalances in the grid. The values in each configuration is the same because it is independent from the configuration and it depends just on the unbalances degree of the grid. The difference is the amplitude of switching frequency component, which is bigger in the second and third configuration in the inverter side (i_{Ni}). In the same configurations, it disappears in the grid side (i_{Ng}). In the last configuration, the 10 kHz component doesn't change because the current is always the same ($i_{Ni} = i_{Ng}$).

- The zero voltage sequence U_o presents a big component at switching frequency only in the 4l+C* topology, which is bigger with a balanced load. It doesn't have 50 Hz component because the cases studied are with zero voltage sequence control in closed-loop.

- The neutral voltage U_N has a big value at 10 kHz in the configuration with just four legs, without the split DC-link capacitors.

- Excluding the configuration with just the four legs that doesn't have DC-link capacitors, with a balanced load, there isn't 50 Hz current flowing through the capacitors in the DC-link. With an unbalanced load, the 50 Hz component is present just in the case without the fourth leg because the middle point of the capacitors is connected to the neutral path where, with unbalanced load, a neutral current at 50 Hz flows. The component at switching frequency doesn't depend on the nature of the load, and it's higher in the second topology.

- In the path which connects the filter to the neutral wire, independently from the nature of the load, always there isn't 50 Hz component. What changes is the value of the 10 kHz component, which is really lower in the configuration without the split DC-link capacitors, and it's equal in the other two configurations.

4.3 Total Harmonic Distortion

The total harmonic distortion, or THD of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. THD is used in power systems and lower THD means reductions in peak currents, heating, emissions. The THD of a generic signal V is for definition 4.1:

$$THD = \frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + \ldots}}{V_1} \tag{4.1}$$

where V_n is the value of the signal V of the *n*-th harmonic and n=1 is the fundamental frequency. The amount of distortion in the voltage or current waveform is defined by means of THD. An example could be the THD of the voltage $v(t)_s$ [9], assuming that there is no DC component in v_s,

$$v_s(t) = v_{s1}(t) + \sum_{h \neq 1} v_{sh}(t) \tag{4.2}$$

where v_{s1}(t) is the fundamental (line-frequency f_1) component and v_{sh}(t) is the component at the *h* harmonic frequency f_h (=hf_1). These voltage components in eq. 4.2 can be expressed as 4.3

$$v_s(t) = \sqrt{2} V_{s1} \sin(\omega_1 t) + \sum_{h \neq 1} \sqrt{2} V_{sh} \sin(\omega_h t) \tag{4.3}$$

The rms value V_s of the line current can be calculated by applying the definition of rms to v_s waveform, as in the following equation (where $T_1 = \frac{1}{f_1} = \frac{2\pi}{\omega_1}$):

$$V_s = \sqrt{\frac{1}{T_1} \int_0^{T_1} v_s(t)^2 dt.} \tag{4.4}$$

Substituting from v_s 4.2 into 4.4 and nothing that the integrals of all the cross-product terms are individually zero 4.5,

$$V_s = \sqrt{V_{s1}{}^2 + \sum_{h \neq 1} V_{sh}^2.} \tag{4.5}$$

The amount of distortion in the voltage or current waveform is quantified by means of an index called total harmonic distortion (THD). The distortion component v_{dis} of the voltage is 4.6:

$$v_{dis}(t) = v_s(t) - v_{s1}(t) = \sum_{h \neq 1} v_{sh}(t) \tag{4.6}$$

and in terms of the rms values 4.7,

$$V_{dis} = \sqrt{V_s{}^2 - V_{s1}{}^2} = \sqrt{\sum_{h \neq 1} V_{sh}} \tag{4.7}$$

Table 4.9: Voltage distortion limits

Voltage value	Individual harmonic (%)	Total harmonic distortion THD (%)
V ≤ 1.0 kV	5.0	8.0
1kV < V ≤ 69 kV	3.0	5.0
69kV < V ≤ 161 kV	1.5	2.5
161kV < V	1.0	1.5

The THD in the voltage is defined as 4.8:

$$\%THD_{\mathrm{v}} = 100 \times \frac{V_{\mathrm{dis}}}{V_{\mathrm{s1}}} = 100 \times \frac{\sqrt{{V_{\mathrm{s}}}^2 - {V_{\mathrm{s1}}}^2}}{V_{\mathrm{s1}}} \tag{4.8}$$

where the subscript v indicates the THD in voltage.

Doing the same and using current components it's possible to obtain a similar index called $\mathrm{THD_i}$.

Harmonics limits are recommended for the grid voltage. The recommended values are based on the fact that some level of voltage distortion is generally acceptable and owners and users must work cooperatively to keep actual voltage distortion below the levels [5]. The table 4.9 applies to voltage harmonics whose frequencies are integer multiplies of the power frequency.

Since the situation is studied in a voltage low, the limit to respect is the first case.

Studying all the configuration with different controllers and different loads, it's possible to design two trends, one with balanced load 4.3.1, and one with unbalanced load, 4.3.2. In this way, it's easy to identify which configuration presents the lower and the higher THD in the grid voltage and which respects the limit imposed by the law. The THD calculated includes the 40th harmonic, which is equal to 2000 Hz.

All the configurations, with balanced and unbalanced loads, are inside the acceptable range. In both cases the THD is lower than 1.2%.

4.4 Comparative Analysis

In this section, the issue is to compare same or different configurations with equal or different controllers in order to understand the similitudes and diversities.

To get which the best performance is, it could be useful to use figures of merit (FOM). A figure of merit is a quantity used to characterize the performance of systems or methods, relative to its alternatives.

The idea is to split the harmonic content of currents and voltages

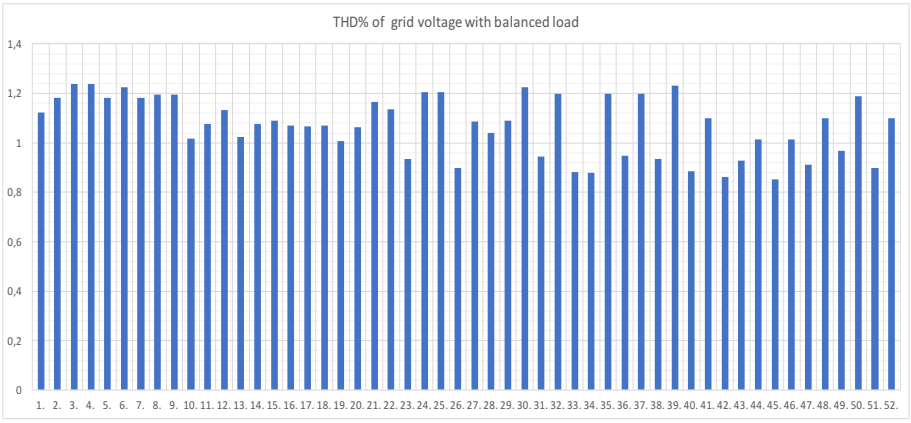


Figure 4.3.1: THD of grid voltage considering all configurations with all possible controllers with balanced load

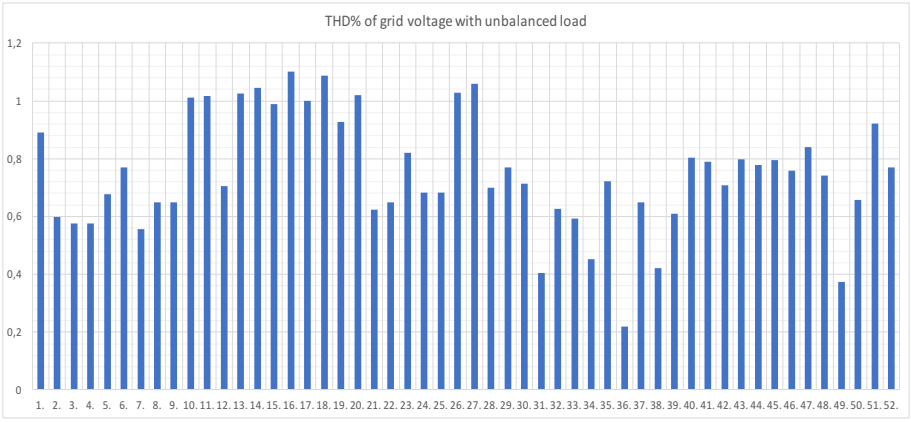


Figure 4.3.2: THD of grid voltage considering all configurations with all possible controllers with unbalanced load

of the power converter and calculate a coefficient for each harmonics group. It will possible to compare different coefficients respectively for different configuration or different control, dependently with type of comparison is done.

The harmonic content will be split in 6 groups, defining K_i as the value of *i*-harmonic and α_a the respectively coefficient of *a*-group:

- (-150, -100 Hz), with the coefficient equal to

$$\alpha_1 = \sqrt{K_{-150}{}^2 + K_{-100}{}^2};$$

- (-50 Hz), where

$$\alpha_2 = K_{-50};$$

- (0 Hz), where

$$\alpha_3 = K_0;$$

- (50 Hz), where

$$\alpha_4 = K_{50};$$

- (150, 250, 450, 500, 650, 750, 950, 1000, 1050, 1100 Hz), where

$$\alpha_5 = \sqrt{K_{150}{}^2 + K_{250}{}^2 + K_{450}{}^2 + K_{500}{}^2 + K_{650}{}^2} + \\ + \sqrt{K_{750}{}^2 + K_{950}{}^2 + K_{1000}{}^2 + K_{1050}{}^2 + K_{1100}{}^2};$$

- (9900, 10000, 10100, 10200 Hz), where

$$\alpha_6 = \sqrt{K_{9900}{}^2 + K_{10000}{}^2 + K_{10100}{}^2 + K_{10200}{}^2}.$$

The abbreviations used are 4.10:

4.4.1 Influence of filter design with balanced and unbalanced loads

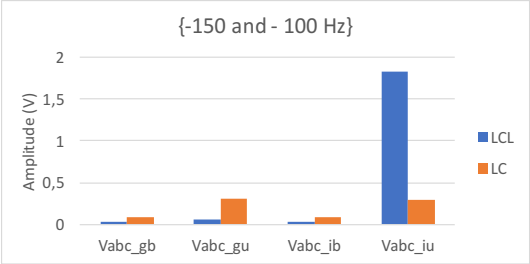
All the configurations are studied with two possible types of filters: *LC* and *LCL* filters. In order to get the differences between *LC* and *LCL* filters, it could be useful to compare same types of configuration with different filters.

Conventional Neutral Leg

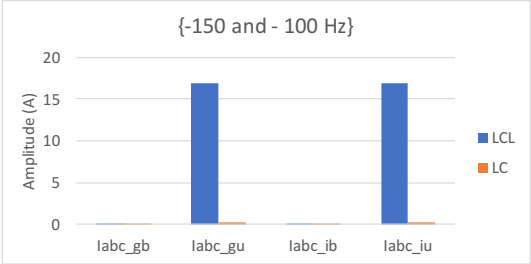
Starting from the first configuration, studied in the section 2.2.1, the cases studied are:

Table 4.10: Abbreviations

Abbreviations	Meaning
V_{abc_gb}	Grid voltage with balanced load
V_{abc_gu}	Grid voltage with unbalanced load
V_{abc_ib}	Inverter voltage with balanced load
V_{abc_iu}	Inverter voltage with unbalanced load
I_{abc_gb}	Grid current with balanced load
I_{abc_gu}	Grid current with unbalanced load
I_{abc_ib}	Inverter current with balanced load
I_{abc_iu}	Inverter current with unbalanced load
I_{Ln_b}	Current through the neutral inductor L_n with balanced load
I_{Ln_u}	Current through the neutral inductor L_n with unbalanced load
I_{Ni_b}	Current through the neutral path in the inverter side with balanced load
I_{Ni_u}	Current through the neutral path in the inverter side with unbalanced load
I_{Ng_b}	Current through the neutral path in the grid side with balanced load
I_{Ng_u}	Current through the neutral path in the grid side with unbalanced load
I_{NC_b}	Current through the neutral path connected to the filter with balanced load
I_{NC_u}	Current through the neutral path connected to the filter with unbalanced load
U_{o_b}	Zero voltage sequence with balanced load
U_{o_u}	Zero voltage sequence with unbalanced load
U_{N_b}	Neutral voltage with balanced load
U_{N_u}	Neutral voltage with unbalanced load
I_{CT_b}	Current through the capacitors in the DC-bus with balanced load
I_{CT_u}	Current through the capacitors in the DC-bus with unbalanced load

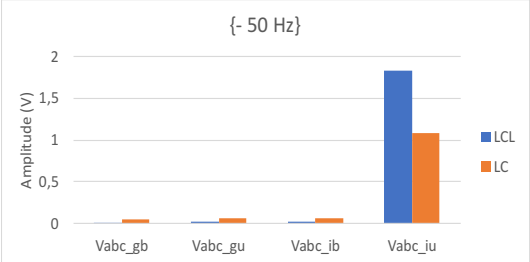


(a) Grid and inverter voltage

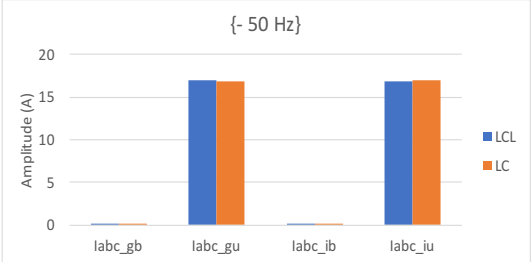


(b) Grid and inverter current

Figure 4.4.1: Comparison of α_1: topology with four legs; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i



(a) Grid and inverter voltage



(b) Grid and inverter current

Figure 4.4.2: Comparison of - 50 Hz: topology with four legs; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i

- 23 with *LCL*-filter, color blue.
- 26 with *LC*-filter, color orange;

These two cases will be compared, controlling the zero voltage sequence U_o and the neutral voltage U_N.

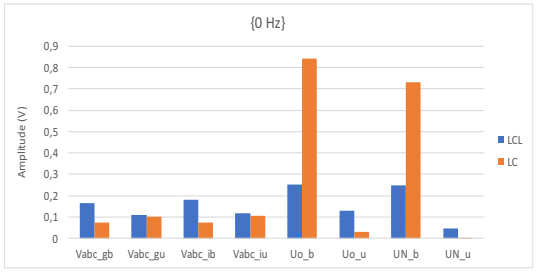
As depicted in fig. 4.4.1b, this configuration presents a high value of negative harmonic content (-150 and -100 Hz) in the inverter and grid current with unbalanced load and with *LCL* filter.

The -50 Hz component doesn't depend on the filters but just on the unbalances, fig. 4.4.2. Being the grid voltage balanced by negative control, there isn't -50 Hz component in the voltage grid, with unbalanced load, as depicted in fig. 4.4.2a. Regards the current, there is -50 Hz with unbalanced load, 4.4.2b.

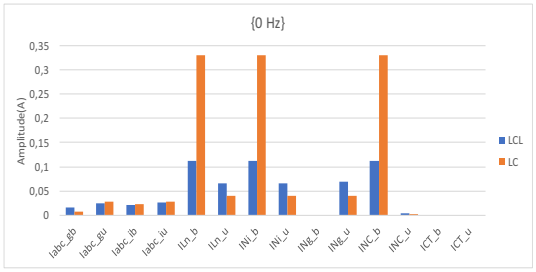
DC component is globally low in voltages and currents thanks to the zero voltage sequence and neutral voltage controllers. In this way, the DC component doesn't affect the system, fig. 4.4.3.

What said for -50 Hz component in the grid voltage, it's valid for 50 Hz component, because it doesn't depend on the types of the filters, just only on the nature of the loads,4.4.4a. U_o and U_N don't have component at fundamental frequency because they are controlled.

How it's possible to note in the fig. 4.4.5, the harmonic content, close

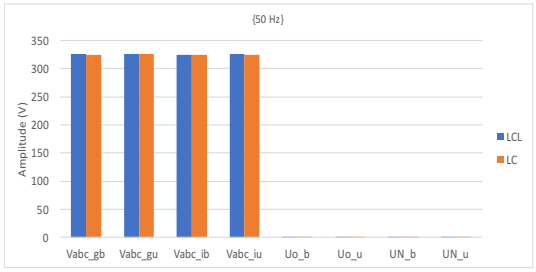


(a) Voltages

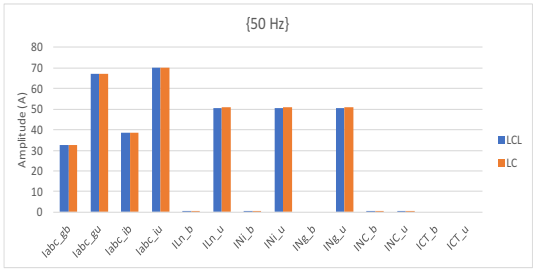


(b) Currents

Figure 4.4.3: Comparison of DC component: topology with four legs; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i

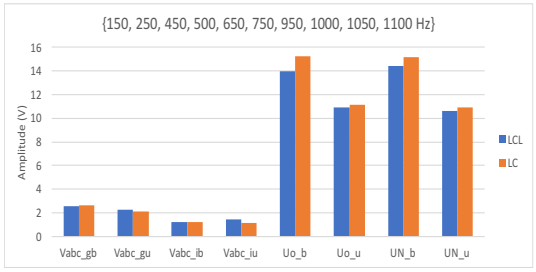


(a) Voltages

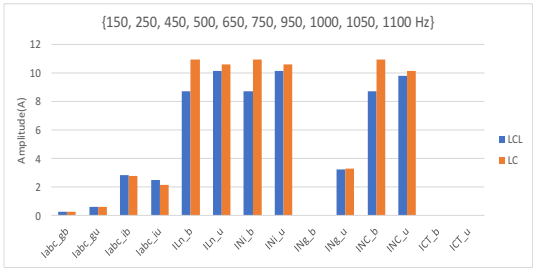


(b) Currents

Figure 4.4.4: Comparison of 50 Hz: topology with four legs; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i

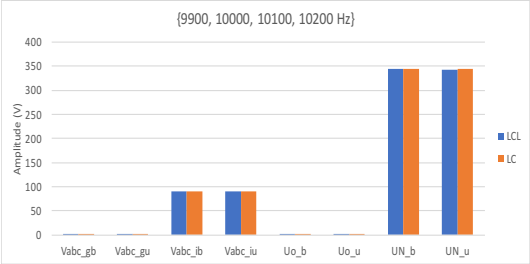


(a) Voltages

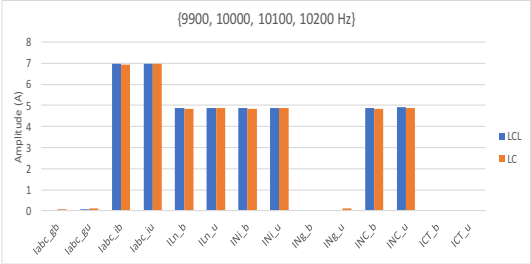


(b) Currents

Figure 4.4.5: Comparison of α_5: topology with four legs; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i

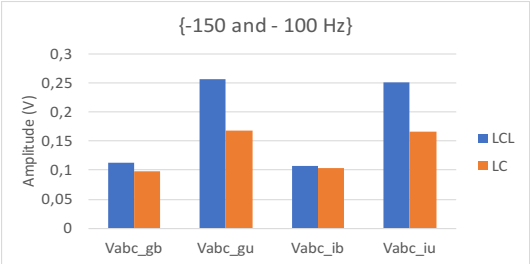


(a) Voltages

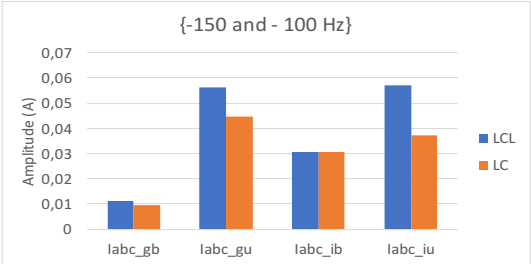


(b) Currents

Figure 4.4.6: Comparison of α_6: topology with four legs; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i



(a) Grid and inverter voltage



(b) Grid and inverter current

Figure 4.4.7: Comparison of α_1: topology with split DC-link capacitors; zero sequence voltage control: PR_v+PR_i

to fundamental frequency, is higher with *LC*-filter, as predictable. The high harmonic content, close to switching frequency, depends on the type of the configuration. In this case, fig. 4.4.6a, the neutral voltage U_N presents a high content.

Split DC-link Capacitors

The second configuration is just with the split DC-link capacitors and the cases are:

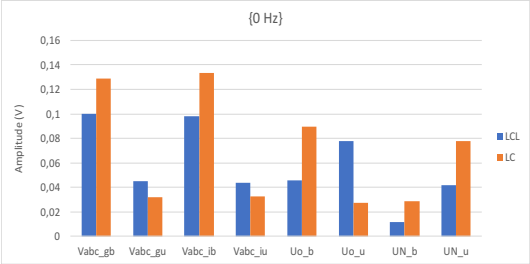
- 29 with *LCL*-filter, color blue.
- 30 with *LC*-filter, color orange;

Controlling the zero voltage sequence U_o, the results are following shown.

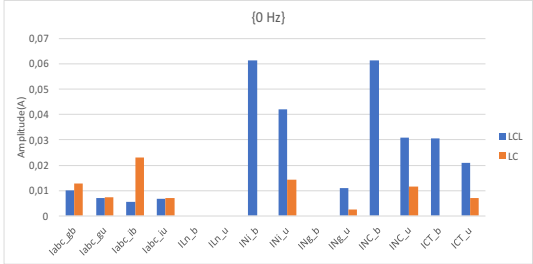
The value of negative harmonic in voltages and currents is negligible in both cases, 4.4.7.

The -50Hz component, not depending on the filters but just on the unbalances, will be equal in each configuration. The DC component, once again, is irrelevant, 4.4.8.

The harmonic content is higher, in currents and voltages, using *LC*-filter, as predictable, 4.4.9.

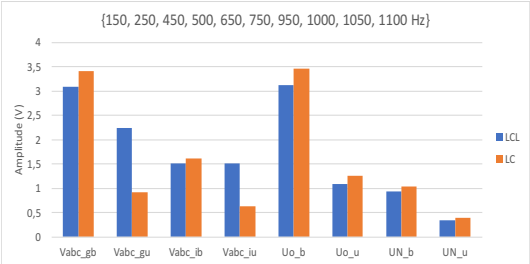


(a) Voltages

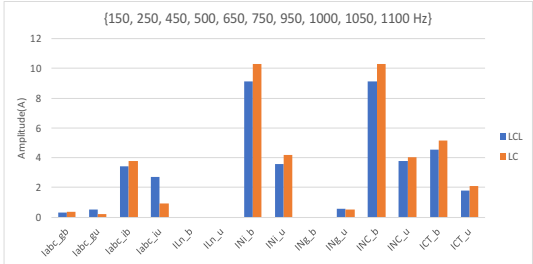


(b) Currents

Figure 4.4.8: Comparison of DC component: topology with split DC-link capacitors; zero sequence voltage control: PR_v+PR_i



(a) Grid and inverter voltage



(b) Grid and inverter voltage

Figure 4.4.9: Comparison of α_5: topology with split DC-link capacitors; zero sequence voltage control: PR_v+PR_i

Independently Controlled Neutral Leg

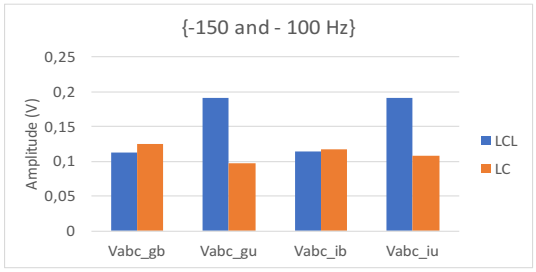
It's turn of independently controlled neutral leg configuration, seen in section 2.2.3. Knowing that the neutral point could be controlled in two ways, firstly the results with zero sequence voltage and neutral voltage control are presented, and following with zero sequence voltage and current i_{CT} control.

a. Control of U_o and U_N The cases are:

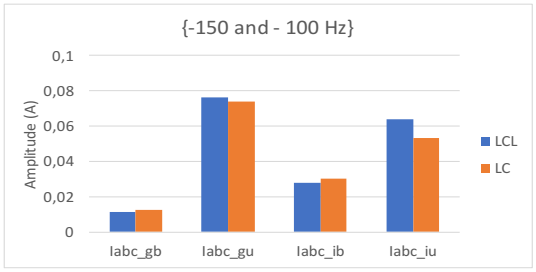
- 1 with *LCL*-filter, color blue.
- 10 with *LC*-filter, color orange;

As shown in fig. 4.4.10, voltages and currents present negative frequencies components which are very small, thus they can't affect the system using balanced or unbalanced load.

It's clear to see in fig. 4.4.11 that the currents will present -50 Hz just with unbalanced load, and the values will be the same independently if the current will be measured before or after the filters, thus independently the type of the filters. The input voltage has a small component because the voltage controlled is the voltage in the grid side.

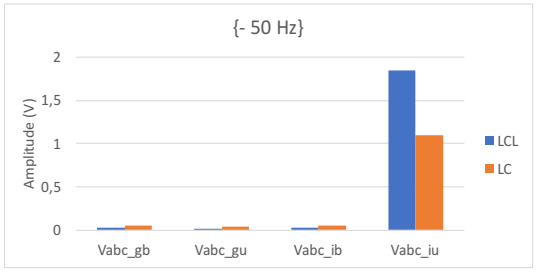


(a) Grid and inverter voltage

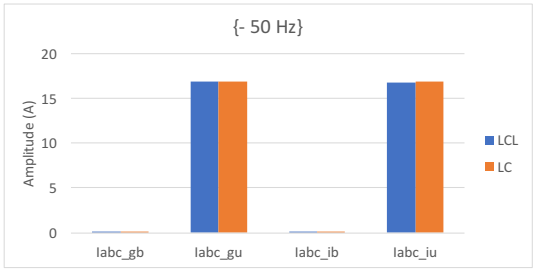


(b) Grid and inverter current

Figure 4.4.10: Comparison of α_1: topology with four legs and split DC-link capacitors; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i

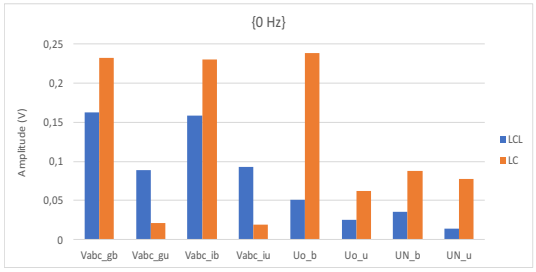


(a) Grid and inverter voltage

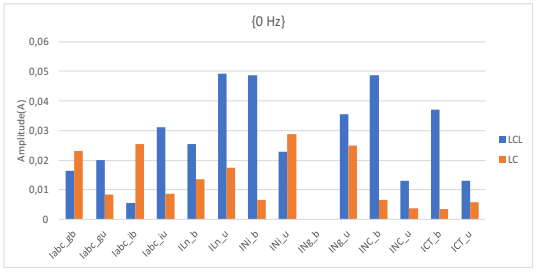


(b) Grid and inverter current

Figure 4.4.11: Comparison of -50 Hz: topology with split DC-link capacitors; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i

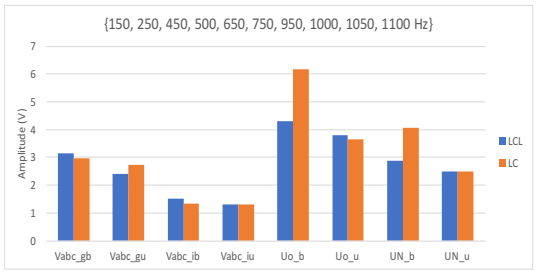


(a) Voltages

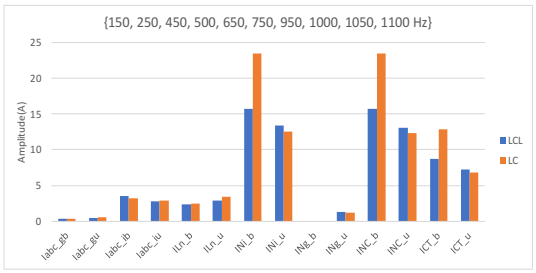


(b) Currents

Figure 4.4.12: Comparison of DC component: topology with split DC-link capacitors; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i

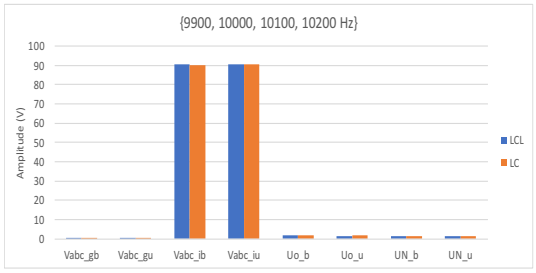


(a) Voltages

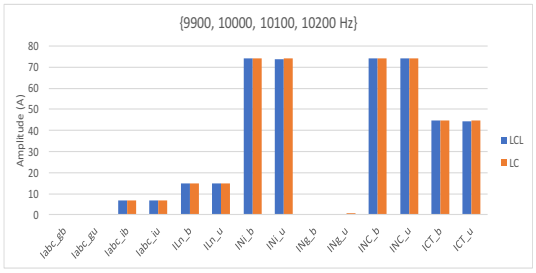


(b) Currents

Figure 4.4.13: Comparison of α_5: topology with split DC-link capacitors; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i



(a) Voltages



(b) Currents

Figure 4.4.14: Comparison of α_6: topology with split DC-link capacitors; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i

As just seen in the Chapter 3, without the control of U_o and U_N, with unbalanced loads, the grid voltage presents a big value of 0 Hz. On the contrary, this doesn't happen with the control of both, fig. 4.4.12, thus independently from the filters.

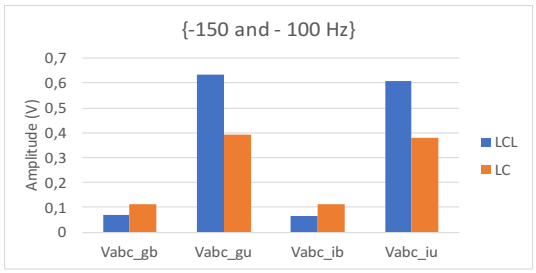
Independently the filters used, the 50 Hz components are equal to the previous cases.

The harmonic content close to the fundamental frequency depends on the filters. As shown in the fig. 4.4.13, it's higher with *LC*-filter, as provided.

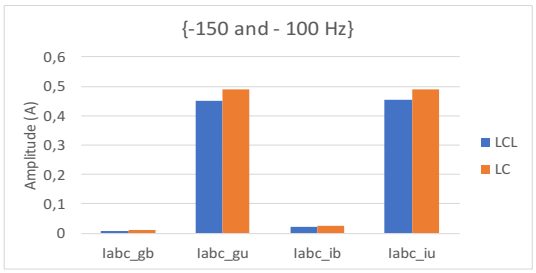
The high harmonic content, close to switching frequency, doesn't depend on the type of filters, as shown in 4.4.14. It's interesting to see that the high harmonics are presented in the input voltage and input current, which are not affected by the filters. On the contrary, output voltage and output current don't have high harmonic content, thanks to the presence of the filters.

b. Control of U_o and i_N The second option, in order to balance the neutral point, is to eliminate the 50 Hz component in the current through the DC-link capacitors. The cases are:

- 19 with *LCL*-filter, color blue.

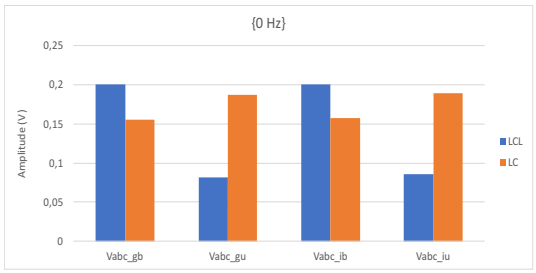


(a) Grid and inverter voltage

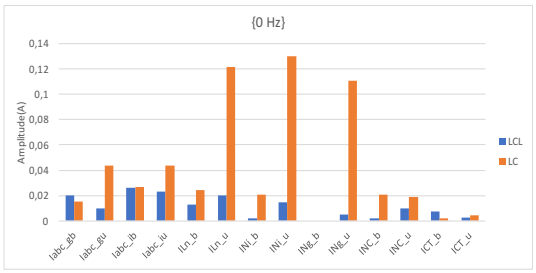


(b) Grid and inverter current

Figure 4.4.15: Comparison of α_1: topology with four legs and split DC-link capacitors; zero sequence voltage control: PR_v+PR_i; Neutral current control: PR_i



(a) Voltages



(b) Currents

Figure 4.4.16: Comparison of DC component: topology with four legs and split DC-link capacitors; zero sequence voltage control: PR_v+PR_i; Neutral current control: PR_i

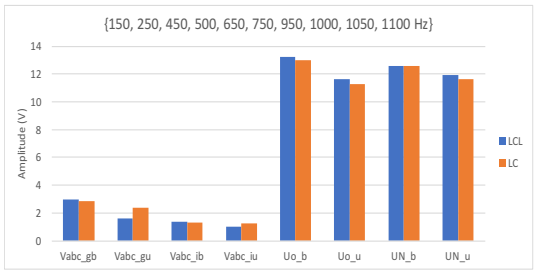
- 21 with *LC*-filter, color orange;

As shown in fig. 4.4.15, once again voltages and currents present negative frequencies components but very small, and like the previously control, it's possible to neglect it. It's not necessary to show the -50 Hz component because it's exactly equal in each configuration depending just on the loads. The same is valid for 50 Hz components.

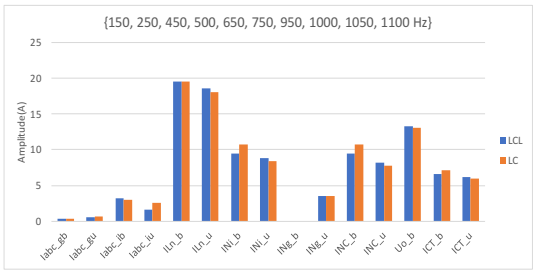
It's possible to say the same in the fig. 4.4.16, where controlling in the same time zero voltage sequence and neutral current, the DC component doesn't affect the system. In this case, the harmonic content close to the fundamental frequency, 50 Hz, is not excessively influenced by the type of filters. As shown in the fig. 4.4.17, the values are more or less the same between the use of *LC* and *LCL* filter. The values are not so bigger than the previously case.

Independently Controlled Neutral Leg, without the connection between the filter and the neutral wire

The configuration is similar to the previous one and the control strategy is equal, as seen in section 2.2.4.

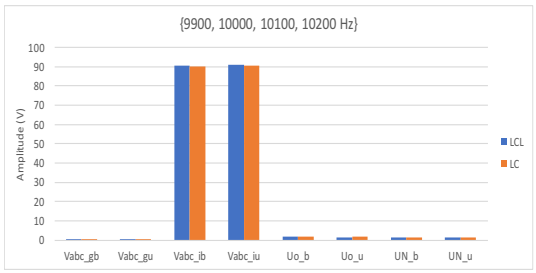


(a) Voltages

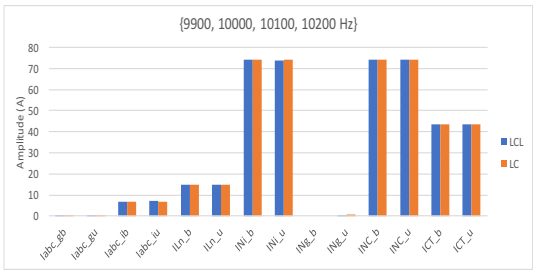


(b) Currents

Figure 4.4.17: Comparison of α_5: topology with four legs and split DC-link capacitors; zero sequence voltage control: PR_v+PR_i; Neutral current control: PR_i



(a) Voltages



(b) Currents

Figure 4.4.18: Comparison of α_6: topology with four legs and split DC-link capacitors; zero sequence voltage control: PR_v+PR_i; Neutral current control: PR_i

a. Control of U_o and U_N Another configuration is the three-phase power converter with four legs and split capacitors with the connection between neutral wire and filters. The cases are:

- 31 with *LCL*-filter, color blue.
- 40 with *LC*-filter, color orange;

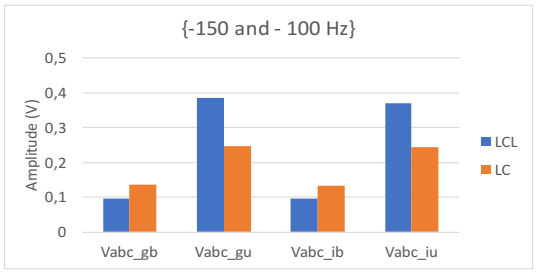
The -150, -100 Hz are irrelevant, as possible to see in fig. 4.4.19. As said previously, the -50 Hz doesn't depend on the filter, but just on the loads, 4.4.11.

Controlling zero voltage sequence and neutral voltage, the 0 Hz is not high, fig. 4.4.20.

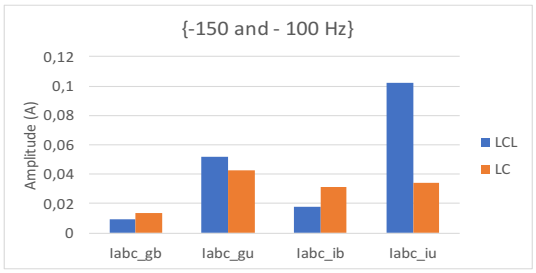
Using the controllers of the first configuration, the low harmonic content is generally lower than the first configuration, 4.4.21.

In this configuration, cutting the link between filter and neutral path, the harmonic content close to switching frequency is bigger in zero sequence voltage. Also, the grid voltage with unbalanced load, is affected by switching frequency. For this reason, this configuration can be used only in particular applications.

b. Control of U_o and i_{CT} As in the previous case, it's possible to control the four leg controlling the currents through the split capacitors.

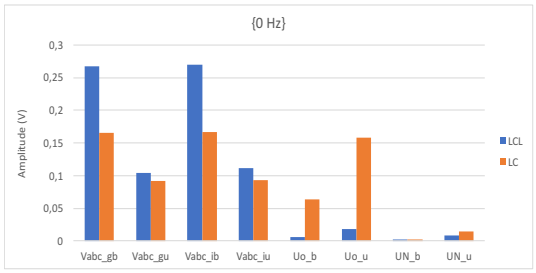


(a) Grid and inverter voltage

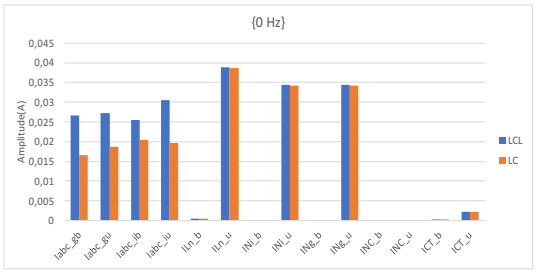


(b) Grid and inverter current

Figure 4.4.19: Comparison of α_1: topology with four legs and split DC-link capacitors withouth the connectrion between the neutral path and the filter; zero sequence voltage control: PR_v+PR_i; Fouth leg control: PR_v+PI_i

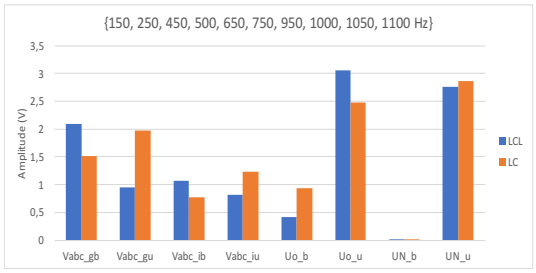


(a) Voltages

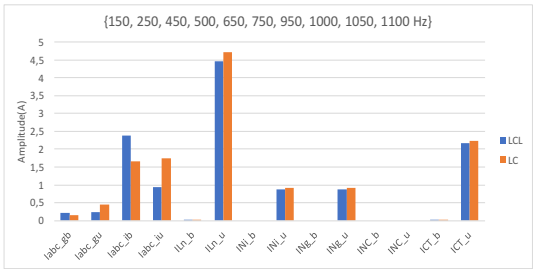


(b) Currents

Figure 4.4.20: Comparison of DC component: topology with four legs and split DC-link capacitors withouth the connectrion between the neutral path and the filter; zero sequence voltage control: PR_v+PR_i; Fouth leg control: PR_v+PI_i

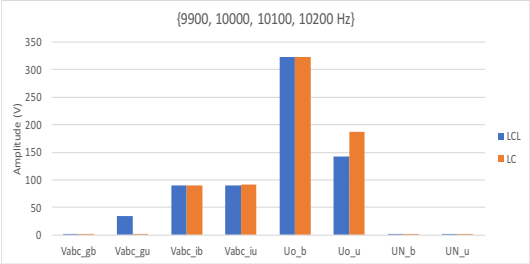


(a) Voltages

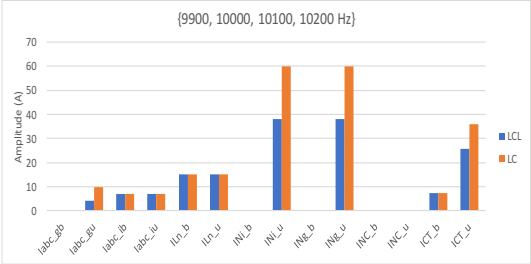


(b) Currents

Figure 4.4.21: Comparison of α_5: topology with four legs and split DC-link capacitors withouth the connectrion between the neutral path and the filter; zero sequence voltage control: PR_v+PR_i; Fouth leg control: PR_v+PI_i

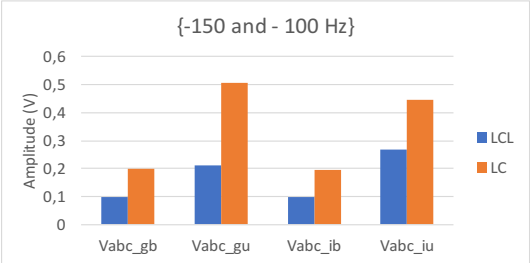


(a) Voltages

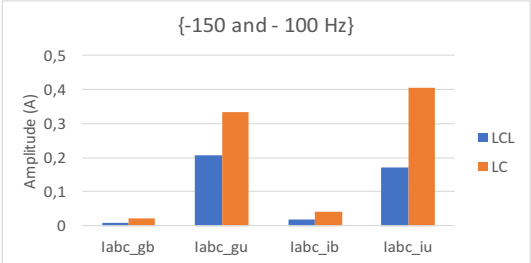


(b) Currents

Figure 4.4.22: Comparison of α_6: topology with four legs and split DC-link capacitors withouth the connectrion between the neutral path and the filter; zero sequence voltage control: PR_v+PR_i; Fouth leg control: PR_v+PI_i



(a) Grid and inverter voltage



(b) Grid and inverter current

Figure 4.4.23: Comparison of α_1: topology with four legs and split DC-link capacitors withouth the connectrion between the neutral path and the filter; zero sequence voltage control: PR_v+PR_i; Neutral current control: PR_i

The cases are:

- 49 with *LCL*-filter, color blue.
- 51 with *LC*-filter, color orange;

The -150, -100 Hz are again really small, as depicted in fig. 4.4.23, independently from the type of filter used. They don't affect the system.

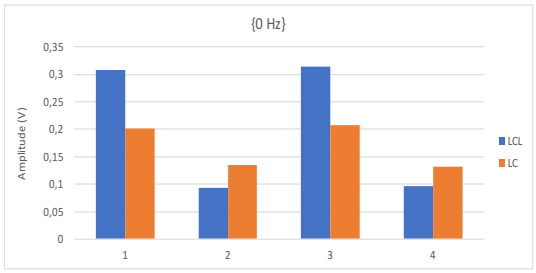
Once again, the DC component is not high, fig. 4.4.24.

In this case, the harmonic content with *LC*-filter is higher than with *LCL*-filter. In particular, the harmonic content with *LC*-filter is bigger with the control of the current flows through the split capacitors than with the control of the neutral voltage.

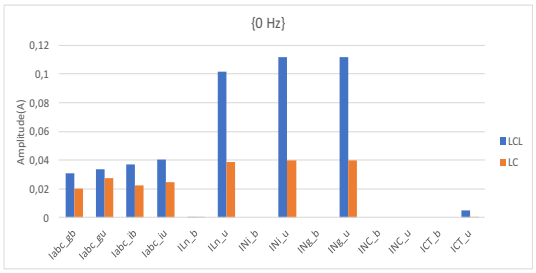
The high harmonic content, shown in fig. 4.4.26, is the same.

4.4.2 Open-loop vs Closed-loop: Operation for the zero sequence and neutral voltages

As just said in the section 3.2, there are two categories of control systems: open-loop (for example with duty of 50%) and closed-loop.

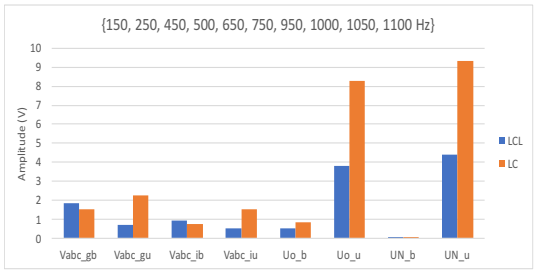


(a) Voltages

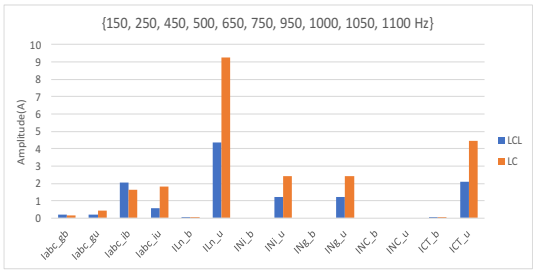


(b) Currents

Figure 4.4.24: Comparison of DC component: topology with four legs and split DC-link capacitors withouth the connectrion between the neutral path and the filter; zero sequence voltage control: PR_v+PR_i; Neutral current control: PR_i

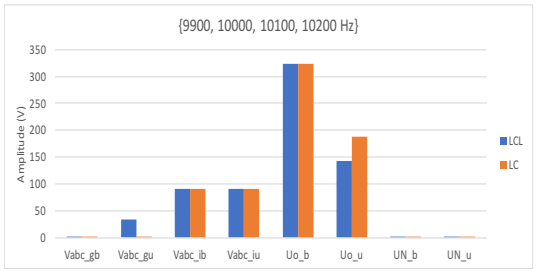


(a) Voltages

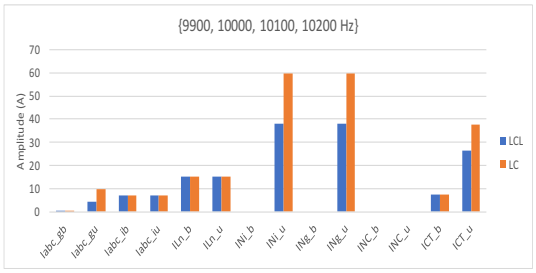


(b) Currents

Figure 4.4.25: Comparison of α_5 topology with four legs and split DC-link capacitors withouth the connectrion between the neutral path and the filter; zero sequence voltage control: PR_v+PR_i; Neutral current control: PR_i

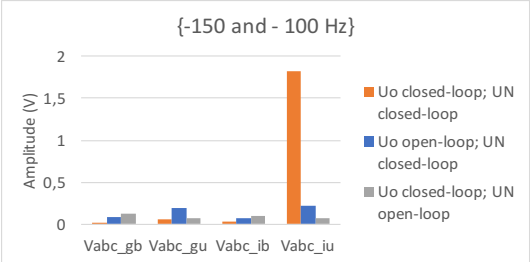


(a) Voltages

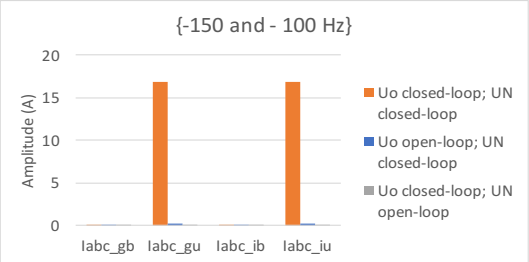


(b) Currents

Figure 4.4.26: Comparison of α_6 topology with four legs and split DC-link capacitors withouth the connectrion between the neutral path and the filter; zero sequence voltage control: PR_v+PR_i; Neutral current control: PR_i



(a) Grid and inverter voltage



(b) Grid and inverter current

Figure 4.4.27: Comparison of α_1: topology with four legs; Different operation for zero sequence and neutral voltages

Now the configurations with all the controls, not only of zero voltage sequence U_o but also of neutral voltage/current are considered. Escluding the configuration without the fourth leg studied in the section 2.2.2, there are three control systems, where all have the positive and negative sequence control:

- the first one is the closed-loop of the zero voltage sequence U_o control and the closed-loop of the neutral control;
- the second one is just the four leg control, leaving the zero voltage sequence control in open-loop;
- the last is just with the zero voltage control, leaving the fourth leg control in open-loop.

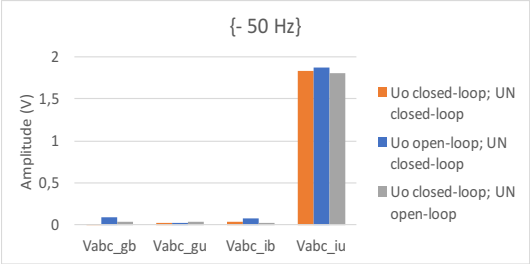
It could be interested to compare same configurations with different control systems.

Conventional Neutral leg

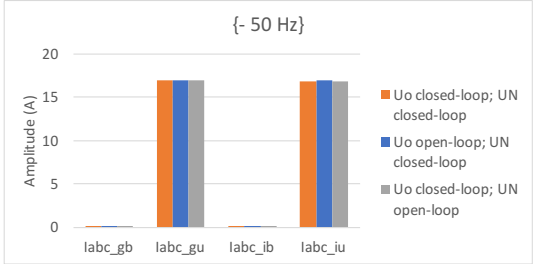
In the topology with just four legs, studied in section 2.2.1, the three control systems are analysed. The cases are:

- 23, where zero voltage control U_o and neutral control U_N are both in closed-loop, color orange;
- 24, where zero voltage control U_o is in open-loop neutral control U_N in closed-loop, color blue;
- 25, where zero voltage control is U_o in closed-loop neutral control U_N in open-loop, color grey.

As it's possible to note in fig. 4.4.27b, closing both the loops, with unbalanced load, the grid and inverter currents have a big peak of negative harmonics.

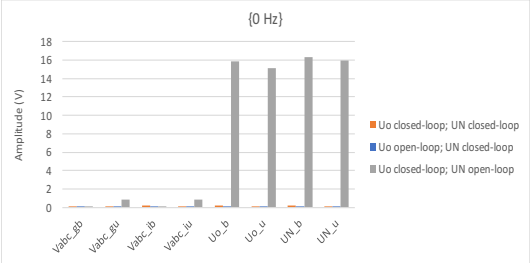


(a) Grid and inverter voltage

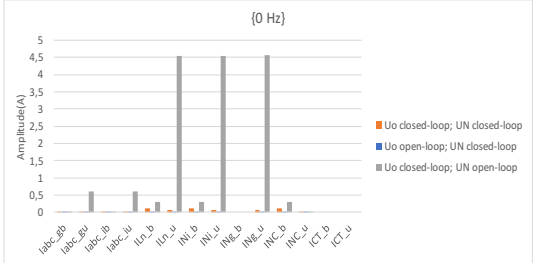


(b) Grid and inverter current

Figure 4.4.28: Comparison of -50 Hz: topology with four legs; Different operation for zero sequence and neutral voltages



(a) Voltages



(b) Currents

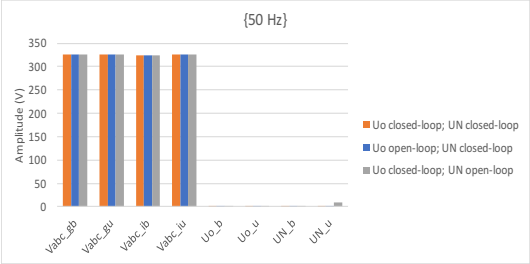
Figure 4.4.29: Comparison of DC component: topology with four legs; Different operation for zero sequence and neutral voltages

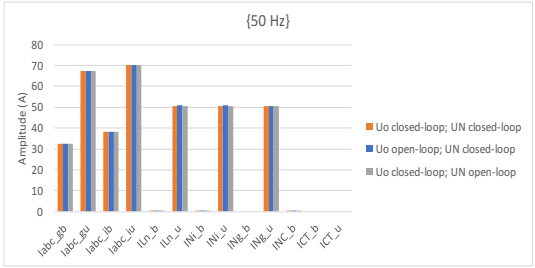
Obviously, the grid voltage doesn't present the negative sequence, as depicted in fig. 4.4.28a, thanks to negative sequence control which attenuates the unbalances due to the unbalanced loads. On the contrary, the input and output currents, independently the controllers, present -50 Hz, fig. 4.4.28b.

Not controlling the neutral voltage U_N, a high 0 Hz component is presented in zero voltage sequence and neutral voltage, independently the nature of the load as shown in fig. 4.4.29a. When the load is unbalanced, current flowing through the neutral path and also in the neutral inductor L_n present a pick of DC component, as shown in fig. 4.4.29b.

Another time, the 50 Hz of the grid voltage achieves the voltage target thanks to the positive sequence control, and the values are the same in each control strategy because the 50 Hz is not affected by the type of configuration and by the control of zero voltage sequence and neutral voltage, as depicted in fig. 4.4.30a. On the contrary, the 50 Hz will change in the U_o and U_N, with unbalanced load, dependently if they are controlled or not.

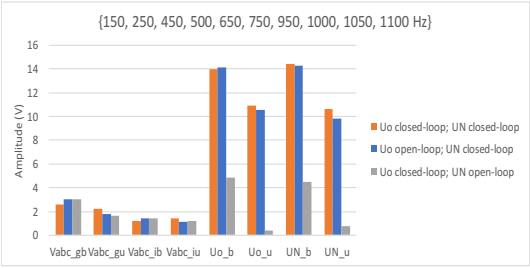
Generally, the harmonic content close to fundamental frequency in the voltage and in the current is lower when it's not used the neutral voltage control. In the other two cases the values are more or less similar, 4.4.31.

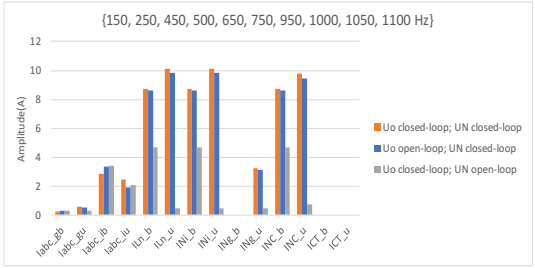




(a) Voltages **(b)** Currents

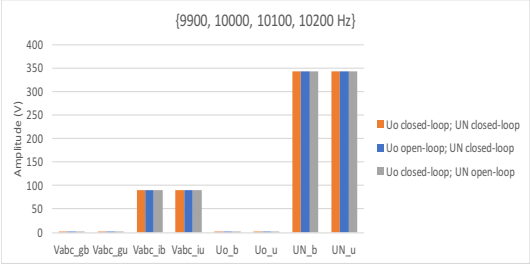
Figure 4.4.30: Comparison of 50 Hz: topology with four legs; Different operation for zero sequence and neutral voltages

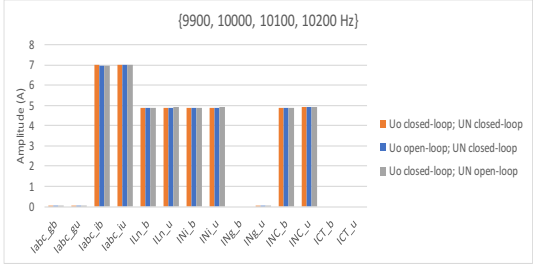




(a) Voltages **(b)** Currents

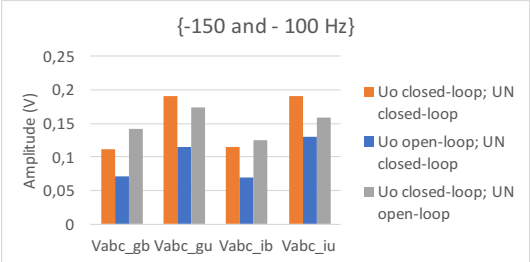
Figure 4.4.31: Comparison of α_5: topology with four legs; Different operation for zero sequence and neutral voltages



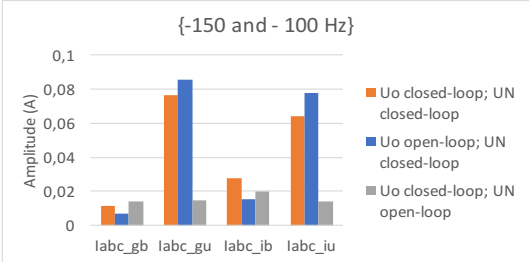


(a) Voltages **(b)** Currents

Figure 4.4.32: Comparison of α_6: topology with four legs; Different operation for zero sequence and neutral voltages

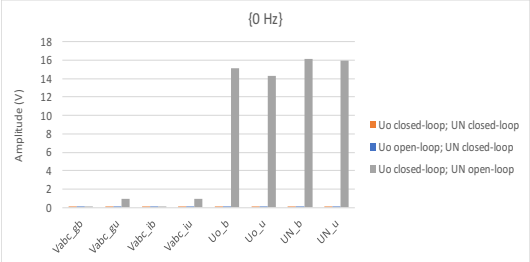


(a) Grid and inverter voltage

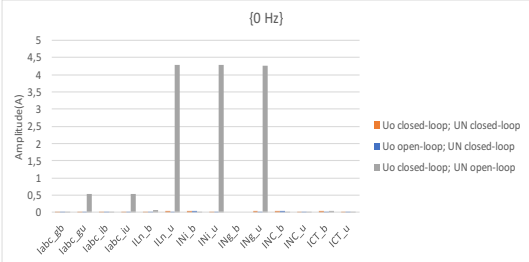


(b) Grid and inverter current

Figure 4.4.33: Comparison of α_1: topology with four legs and split DC-link capacitors; Different operation for zero sequence and neutral voltages



(a) Voltages



(b) Currents

Figure 4.4.34: Comparison of DC component: topology with four legs and split DC-link capacitors; Different operation for zero sequence and neutral voltages

As just said, the frequencies close to the switching frequency don't depend on the type of control, 4.4.32.

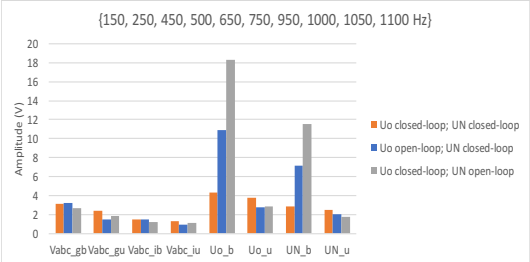
Independently Controlled Neutral Leg

Studying this topology, seen in section 2.2.3, with *LCL*-filter, the cases are:

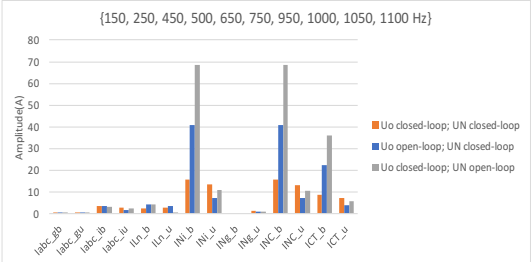
- 1, where zero voltage control U_o and neutral control U_N are both in closed-loop, color orange;
- 2, where zero voltage control U_o is in open-loop neutral control U_N in closed-loop, color blue;
- 3, where zero voltage control is U_o in closed-loop neutral control U_N in open-loop, color grey.

In this configuration voltages and currents don't have big negative components, like -150 Hz and -100 Hz, in each of the control possibilities, as shown in fig. 4.4.33a and 4.4.33b.

Regarding the DC component, the situation is the same of the previous configuration, namely, without the control of neutral voltage U_N,

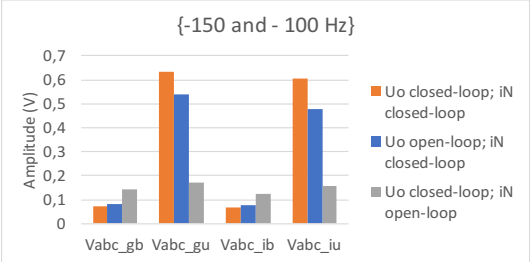


(a) Voltages

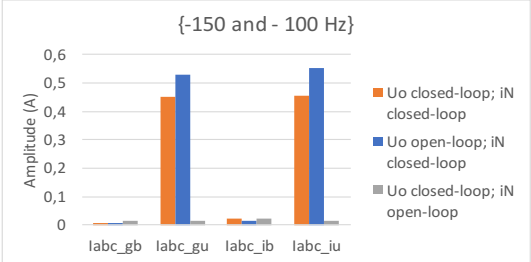


(b) Currents

Figure 4.4.35: Comparison of α_5: topology with four legs and split DC-link capacitors; Different operation for zero sequence and neutral voltages



(a) Grid and inverter voltage



(b) Grid and inverter current

Figure 4.4.36: Comparison of α_1: topology with four legs and split DC-link capacitors; Different operation for zero sequence voltage and neutral current

the variables in the system present a DC component, as depicted in fig. 4.4.34.

The harmonic content close to fundamental frequency is bigger when the neutral voltage control is not used, and the best situation is when both controls are applied, 4.4.35. However, the harmonic content in the grid and inverter voltage are similar in all the possibilities.

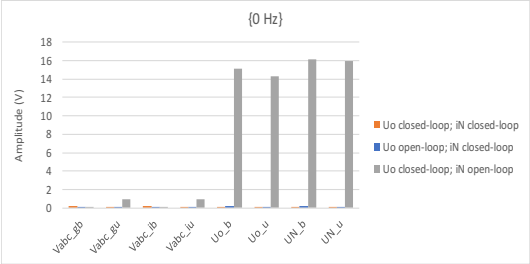
It could be interested to analyse also the neutral control with the control of the current through the DC-link capacitors. The cases are:

- 19, where zero voltage control U_o and neutral control i_N are both in closed-loop, color orange;
- 20, where zero voltage control U_o is in open-loop neutral control i_N in closed-loop, color blue;
- 3, where zero voltage control is U_o in closed-loop neutral control i_N in open-loop, color grey.

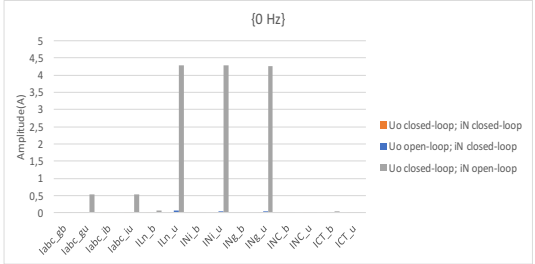
Independently the type of control, there isn't a big component of negative harmonic content in voltages and currents, as shown in fig. 4.4.36.

Regarding DC component, the situation is equal to 4.4.34.

The harmonic content close to fundamental frequency is generally lower using the current neutral control instead neutral voltage control.

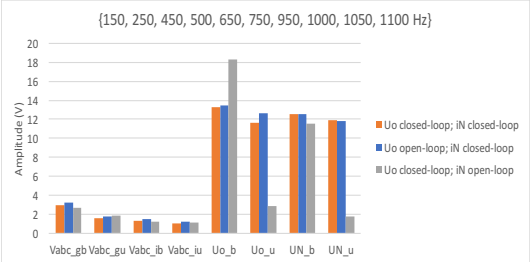


(a) Voltages

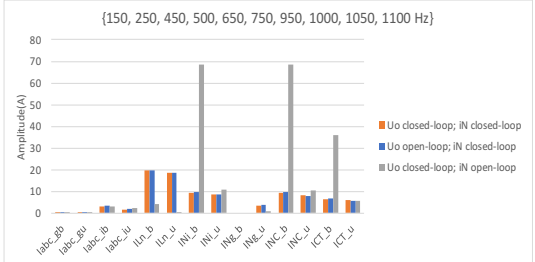


(b) Currents

Figure 4.4.37: Comparison of DC component: topology with four legs and split DC-link capacitors; Different operation for zero sequence voltage and neutral current



(a) Voltages



(b) Currents

Figure 4.4.38: Comparison of α_5: topology with four legs and split DC-link capacitors; Different operation for zero sequence voltage and neutral current

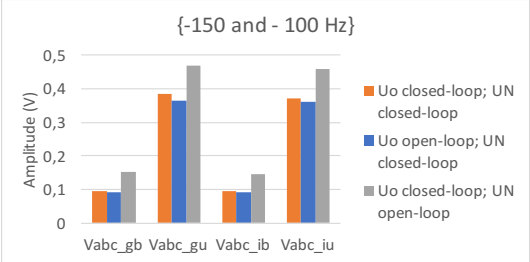
Once again it is the biggest when it's not used the neutral current control in the same before it was bigger without the control of neutral voltage. It is the lowest when both controls are applied, 4.4.38.

Independently Controlled Neutral Leg, without the connection between the filter and the neutral wire

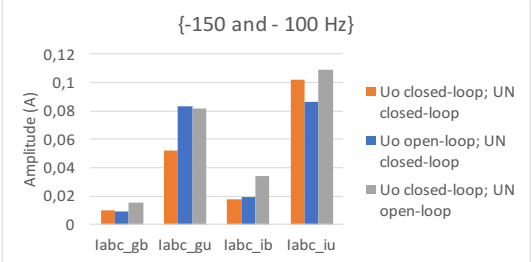
Regarding the topology studied in section 2.2.4, the cases are, with *LCL*-filter:

- 31, where zero voltage control U_o and neutral control U_N are both in closed-loop, color orange;
- 32, where zero voltage control U_o is in open-loop neutral control U_N in closed-loop, color blue;
- 33, where zero voltage control is U_o in closed-loop neutral control U_N in open-loop, color grey.

In this topology, fig. 4.4.39, the negative harmonics are irrelevant in all the control strategies adopted, independently from what is controlled.

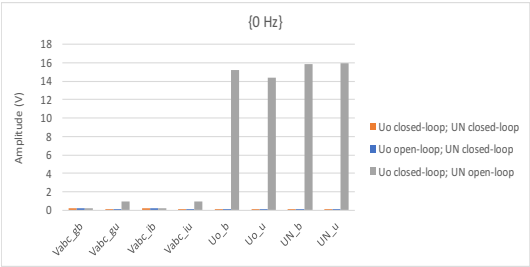


(a) Grid and inverter voltage

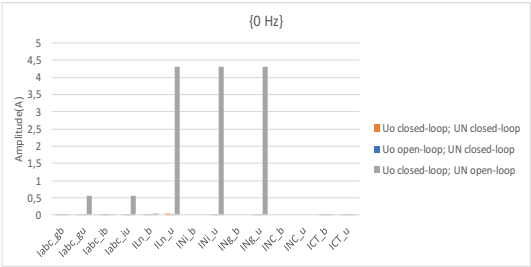


(b) Grid and inverter current

Figure 4.4.39: Comparison of α_1: topology with four legs and split DC-link capacitors without the connection between the neutral path and the filter; Different operation for zero sequence and neutral voltages

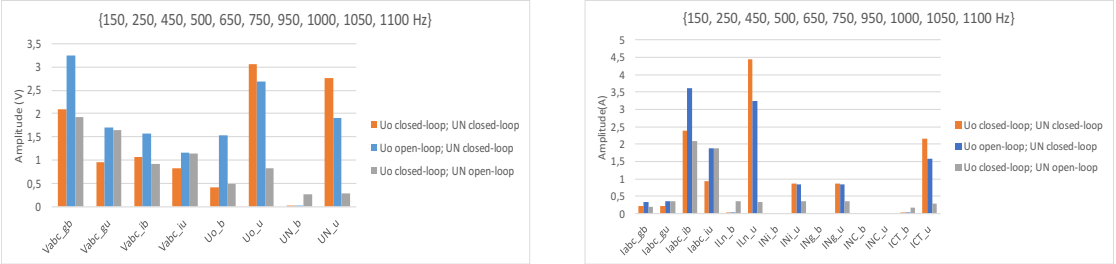


(a) Voltages



(b) Currents

Figure 4.4.40: Comparison of DC component: topology with four legs and split DC-link capacitors without the connection between the neutral path and the filter; Different operation for zero sequence and neutral voltages



(a) Voltages **(b)** Currents

Figure 4.4.41: Comparison of α_5: topology with four legs and split DC-link capacitors without the connection between the neutral path and the filter; Different operation for zero sequence and neutral voltages

Also in this configuration, not controlling the neutral voltage U_N, a high DC component is presented in zero voltage sequence and neutral voltage, fig. 4.4.40a. About the current, when the load is unbalanced, there is DC component in the current flows through the neutral path and also in the neutral inductor L_n, as shown in fig. 4.4.40b.

The harmonic content is more or less the same in all the three cases as shown in fig. 4.4.41.

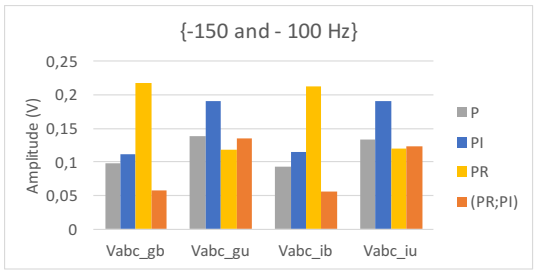
4.4.3 Four leg control: Different controllers in the inner current loop

Having seen that in the topologies with the fourth leg and split capacitors in the sections 2.2.3 and 2.2.4 is possible to use different controllers to achieve the same target studied in the section 3.5, now the results obtained are compared. Changing the current loop controller in the neutral leg control, four different possibilities are obtained. The possibilities depend on the type of the controller which could be P, PI, PR or PI and PR in parallel.

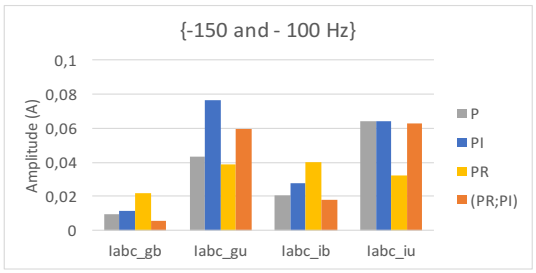
Focusing on the conventional three-phase power converter with four legs, split DC-link capacitors and *LCL* filter, with zero sequence control U_o and obviously, the neutral voltage U_N closed-loops, the cases are:

- 4, where a P is used, color grey;
- 1, where a PI is used, color blue;
- 8, where a PR is used, color yellow;
- 6, where a PR in parallel with a PI are used, color orange;

Controlling zero voltage sequence and neutral voltage, the utilization of different controllers changes the values of negative harmonics in voltages and currents, like -150 Hz and -100 Hz. However, the values are

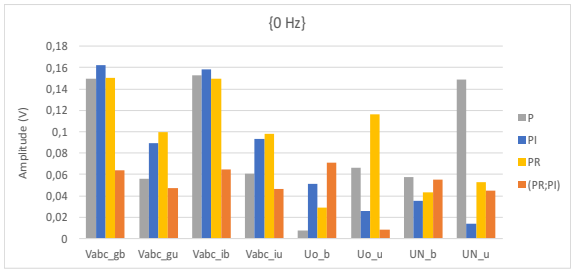


(a) Grid and inverter voltage

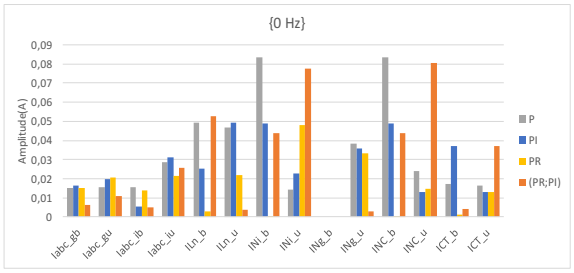


(b) Grid and inverter current

Figure 4.4.42: Comparison of α_1: topology with four legs and split DC-link capacitors; Different controllers in the inner current loop in the neutral voltage control



(a) Voltages

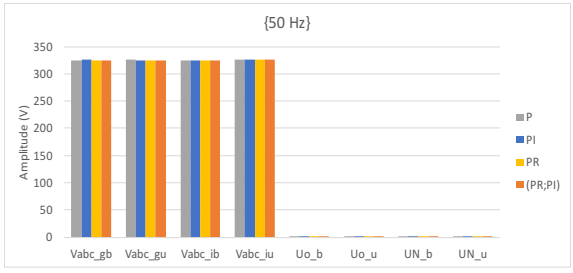


(b) Currents

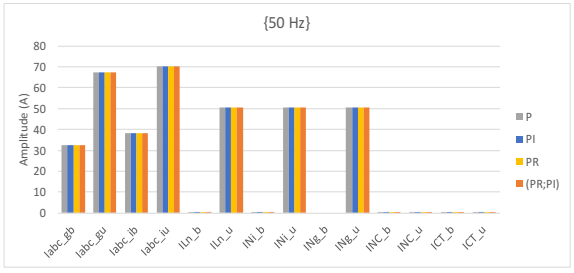
Figure 4.4.43: Comparison of DC component: topology with four legs and split DC-link capacitors; Different controllers in the inner current loop in the neutral voltage control

always small and they don't affect the system, fig. 4.4.42. It's possible to say the same for DC component, 4.4.43.

Obviously, the component at fundamental frequency of grid voltage and current, 4.4.44, is equal in all the different types of controllers because it depends only on the topology, the loads and the positive control. As is depicted in fig. 4.4.44a, U_o and U_N haven't 50 Hz component thanks to the control. In particular, changing the control of the inner current loop in the neutral control doesn't preclude to achieve the target.

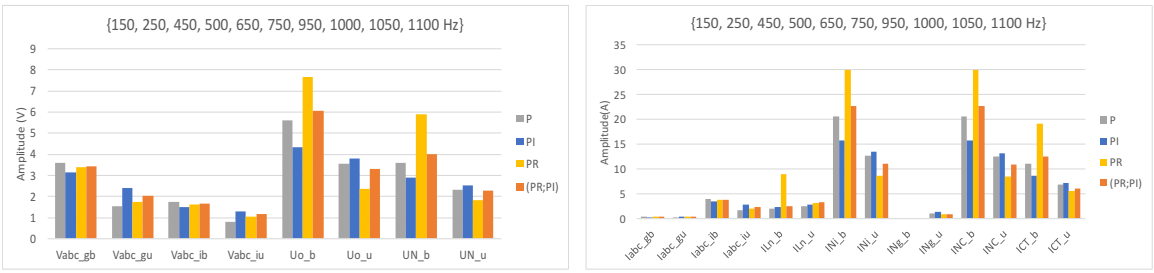


(a) Voltages



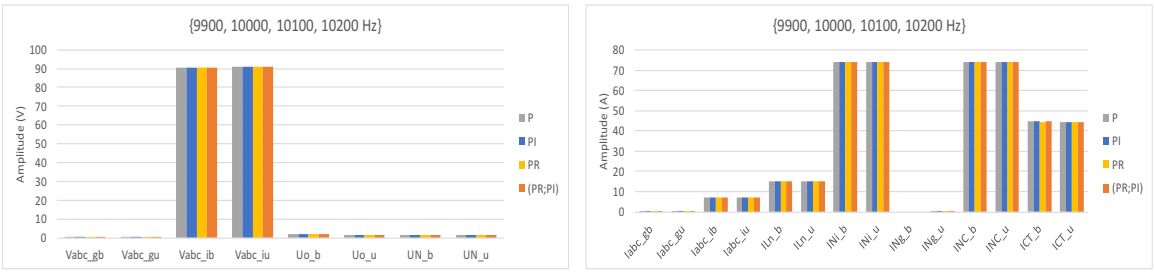
(b) Currents

Figure 4.4.44: Comparison of 50 Hz: topology with four legs and split DC-link capacitors; Different controllers in the inner current loop in the neutral voltage control



(a) Voltages **(b)** Currents

Figure 4.4.45: Comparison of α_5: topology with four legs and split DC-link capacitors; Different controllers in the inner current loop in the neutral voltage control



(a) Voltages **(b)** Currents

Figure 4.4.46: Comparison of α_6: topology with four legs and split DC-link capacitors; Different controllers in the inner current loop in the neutral voltage control

The harmonic distortion is strictly connected with the type of controllers used, in fact, as depicted in 4.4.45, it changes when the controllers change. In the voltages, fig. 4.4.45a, the change is big just comparing the behaviour of a PI and a PR in the zero and neutral voltages with balanced load. The same happens in the currents of the system, fig. 4.4.45b. The harmonic content is higher with the use of a PR, that for example in the current through the capacitors of the filter, is almost the double of the same current just using a PI.

The switching harmonic doesn't depend on the type of controllers, as depicted in fig. 4.4.46.

The bigger difference between the controllers used is the error. The error *e(t)* is obtained by the difference between the reference value, *r(t)*, and the real value *y(t)*, 4.4.47. Being the target, in this case, a sinusoidal reference, a P or a PI, which work with DC signals, will not

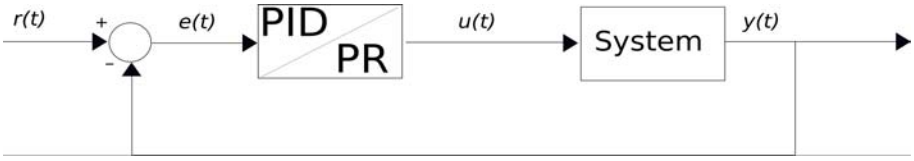


Figure 4.4.47: Scheme of a system with the control in closed-loop

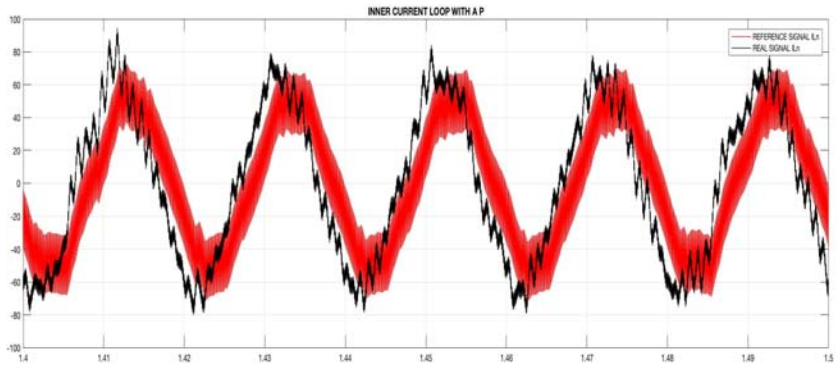


Figure 4.4.48: Inner current loop in the neutral voltage control using a P. The red signal is the reference of the current, which is the output command of the voltage loop; the black signal is the real value of the current i_{Ln}

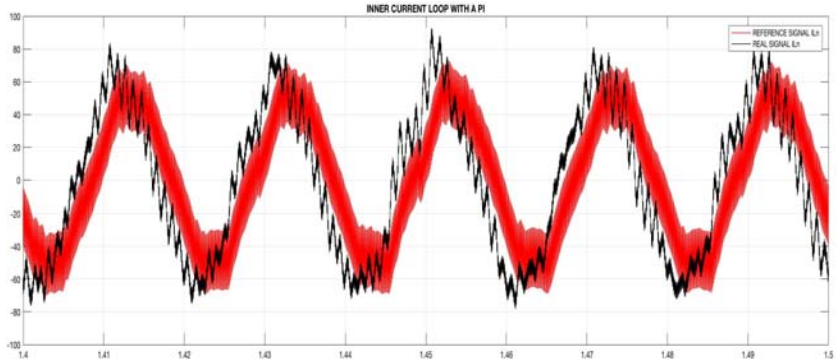


Figure 4.4.49: Inner current loop in the neutral voltage control using a PI. The red signal is the reference of the current, which is the output command of the voltage loop; the black signal is the real value of the current i_{Ln}

be able to follow the reference value. This means that the error will be always different from zero.

An example is shown following, where a three-phase power converter with four leg and split capacitors is simulated with unbalanced loads, just changing the controllers. Predictably, how is possible to see in the fig. 4.4.48 and 4.4.49, a Proportional and a PI are not able to follow an AC signal. Anyway, the system can work because the PR used in the voltage loop work perfectly, eliminating the frequency that is necessary to attenuate. Being the current used in the neutral voltage, the inductor flows through the neutral inductor L_n, the problem could be when the real current is almost big (the 50 Hz component) and it could damage the system.

The problem doesn't exist when a PR, or a PR in parallel with a PI, are used, because a PR is able to eliminate the error, which allows that the real current is equal to the reference value, as shown in fig. 4.4.50 and 4.4.51.

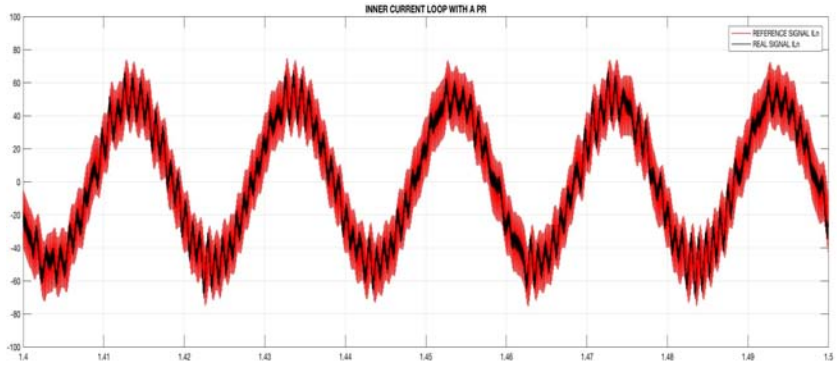


Figure 4.4.50: Inner current loop in the neutral voltage control using a PR. The red signal is the reference of the current, which is the output command of the voltage loop; the black signal is the real value of the current i_{Ln}

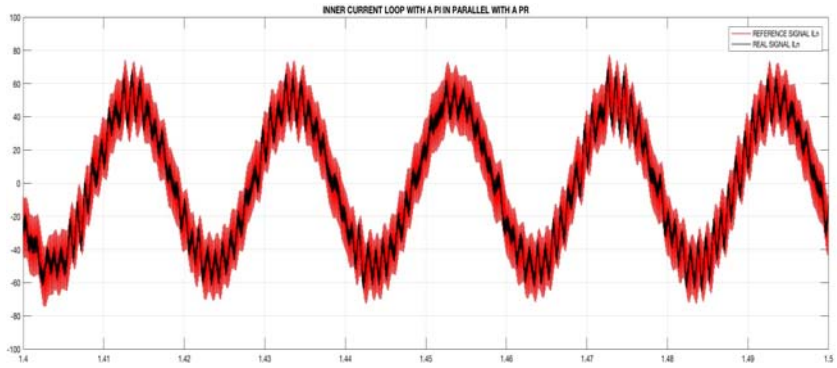
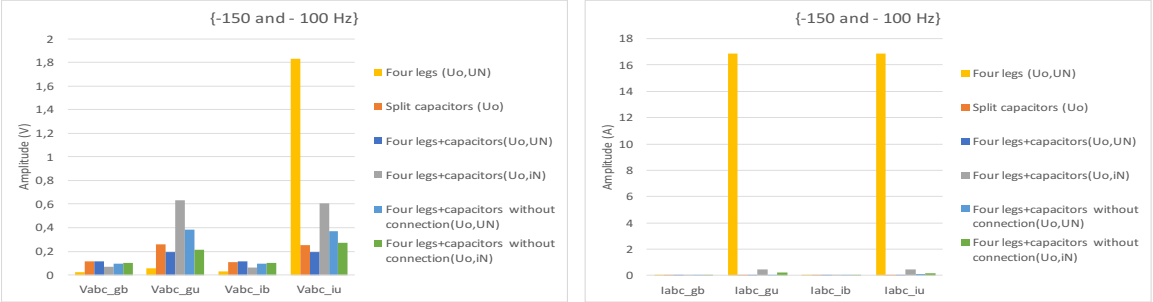


Figure 4.4.51: Inner current loop in the neutral voltage control using a PR in parallel with a PI. The red signal is the reference of the current, which is the output command of the voltage loop; the black signal is the real value of the current i_{Ln}



(a) Grid and inverter voltage **(b)** Grid and inverter current

Figure 4.4.52: Comparison of α_1: All the topologies

4.4.4 Comparison of harmonic content in the different topologies

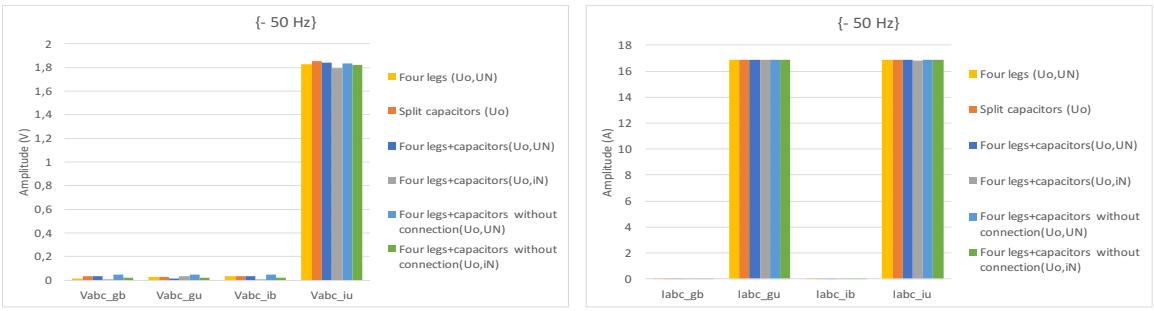
Using the same controller strategies, this means having positive, negative and zero voltage sequence controls and neutral voltage controls in closed-loops, with *LCL*-filter, it's interesting to compare directly the different configurations.

In this comparision, the two different types of neutral leg control studied in 3.5 are included. The cases are:

- 23, with four legs, controlling U_o and U_N, color yellow;
- 29, with split DC-link capacitors, controlling U_o, color orange;
- 1, with four legs and split DC-link capacitors, controlling U_o and U_N, color blue;
- 19, with four legs and split DC-link capacitors, controlling U_o and i_N, color grey;
- 31, with four legs and split DC-link capacitors without the path between the neutral wire and the filter, controlling U_o and U_N, color light blue;
- 49, with four legs and split DC-link capacitors without the path between the neutral wire and the filter, controlling U_o and i_N, color green.

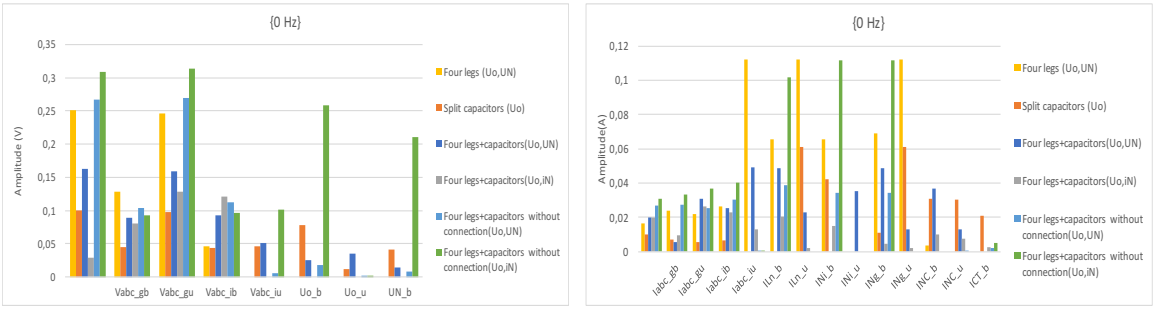
In fig. 4.4.52b, it's possible to see that the configuration with just only four legs has a big component of negative frequency in the output and input currents and in the input voltage when the load is unbalanced. Looking always the topology with four legs, in the fig. 4.4.52a, the negative component is high just in the inverter voltage with unbalanced load. In the other configurations, the negative component is irrelevant.

As predicted, looking at -50 Hz in the fig. 4.4.53, the negative sequence depends on:



(a) Grid and inverter voltage **(b)** Grid and inverter current

Figure 4.4.53: Comparison of -50 Hz: All the topologies



(a) Voltages **(b)** Currents

Figure 4.4.54: Comparison of DC component: All the topologies

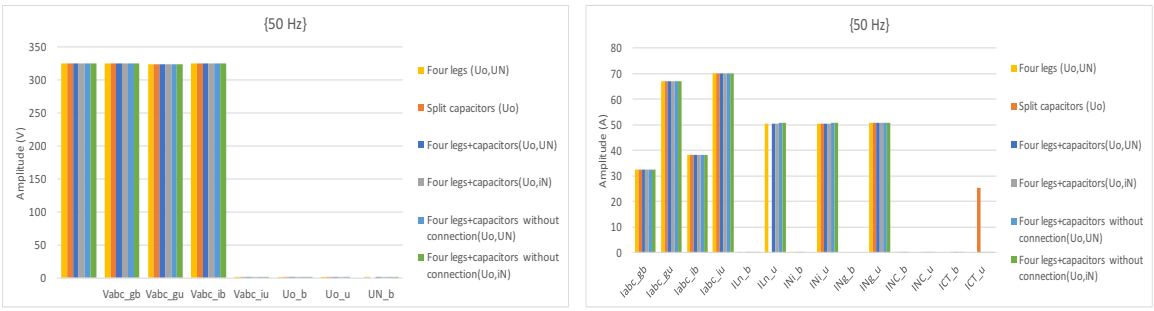
- the level of unbalances presents in the grid;
- negative sequence control.

This means that, despite the load is unbalanced, like in this case, the negative sequence control is controlling perfectly the grid voltage. As it's shown in fig. 4.4.53a, the grid voltage doesn't have -50 Hz with unbalanced load. On the contrary, in the fig. 4.4.53b, the current will present negative sequence due to the unbalances of the loads. The value of -50 Hz in the current are the same, independently the topology used.

The DC component is negligible in the voltages and in the currents because all the controllers are operated and they compensated the DC component, as depicted in fig. 4.4.54. Focusing now on 50 Hz and just looking at the voltages of the systems, 4.4.55a, it's possible to say:

- the value of grid voltage is fixed by the positive sequence control;
- the zero sequence and neutral voltages don't have component at fundamental frequency because in all the topologies they are controlled.;

About currents, 4.4.55b;



(a) Voltages **(b)** Currents

Figure 4.4.55: Comparison of 50 Hz: All the topologies

- grid current depends on the load, independently from the topology used. This means that with balanced load the current has just 50 Hz component, which is bigger than the case with unbalanced load, where grid current has always negative sequence (-50 Hz).

- Current in the neutral inductor L_n depends once again on the load. With balanced load, it doesn't have 50 Hz component because there isn't neutral current from the load. With unbalances, the current has 50 Hz equal to 50 Hz presents in the neutral path.

- Current in the neutral path, independently if it's in the inverter or grid side, has the same behaviour of i_{Ln}.

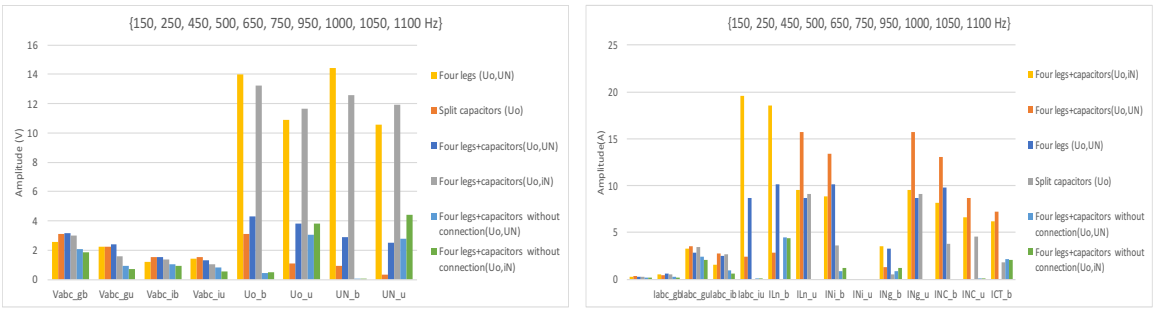
- Current flowing through the capacitors of the filter, independently the load and the configuration, doesn't have 50 Hz.

- Generally current flows through split capacitors doesn't have 50 Hz component, independently from the load. But in the topology with just the split DC-link capacitors, where the middle point of the capacitors in connected to the neutral path, with unbalanced load, there is a component at fundamental frequency due to the unbalances from the load.

The harmonic contents depend on the type of control and the configuration, 4.4.56. Changing the topology, the transfer function of the system changes and also the behaviour.

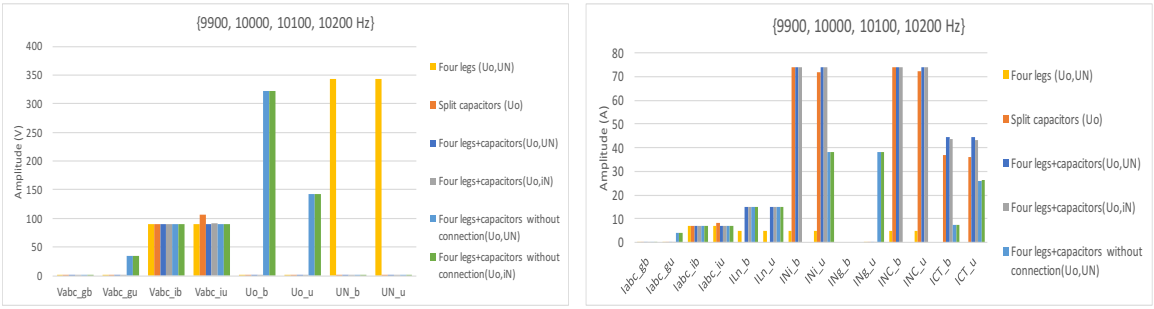
The figure 4.4.57 shows components at switching frequency. Comparison the component close to switching frequency of the voltages in all the topology, as shown in fig. 4.4.57a, it is possible to say:

- With balanced load, grid voltage doesn't have switching harmonics, independently from the topology. On the contrary, with unbalanced load, there is switching harmonic in the grid voltage just with the configuration without the connection between the neutral wire and



(a) Voltages **(b)** Currents

Figure 4.4.56: Comparison of α_5: All the topologies



(a) Voltages **(b)** Currents

Figure 4.4.57: Comparison of α_6: All the topologies

the filter. The lack of this connection causes a high switching harmonic in the grid voltage with unbalances.

- The switching harmonics of zero sequence and neutral voltages are strictly connected to the power converter topology. Just using the configuration with only four legs, the neutral voltage, independently from the type of load. This is due the lack of split DC-link capacitors. The zero voltage sequence has switching harmonics when there isn't the connection between the neutral path and the filter.

Now analysing the switching harmonics in the currents, 4.4.57b, the conclusions are:

- With balanced load, grid current hasn't component at switching frequency, independently from the configuration. With unbalanced load, grid current has switching harmonics just in the topology without the connection between neutral path and filter.

- The component at switching harmonic in current through the neutral path depends if current is in the inverter o grid side. Neutral current in the inverter side has the harmonic content of the neutral current in the grid side and the current flowing through capacitors of the filters, when it is available. When the load is balanced, there

isn’t the connection between the load and the neutral path. This implies that i_{Ni} is equal to i_{NC}, when the last one exist, with the same harmonic content. In the case i_{NC} doesn’t exist, with balanced load, also i_{Ni} is zero. When the load is unbalanced, the neutral current in the grid side has switching harmonic just in the configuration without the connection between neutral path and filter, because there isn’t the path through the filter.

- The current through the capacitors in the DC-bus has always harmonics at switching frequency. In the configuration with four legs and split capacitors, the values are the same, independently from the loads. On the contrary, the values increase in the topology without the connection between neutral path and filter when the load is unbalanced. It will be higher with unbalanced loads.

Chapter 5

Conclusions and possible solution

This chapter discusses the summary, conclusion and recommendation of the utilization of each topology.

5.1 Summary

The overriding purpose of this thesis was to compare the four types of four types of three-phase power converter, characterized by different control systems. The four topologies are:

- conventional neutral leg, which is a three-phase power converter with fourth leg;
- split DC-link capacitors, which is a three-phase power converter with split capacitors in the DC-bus and the neutral wire, tying the neutral point to the mid-point of the DC-link capacitors;
- independently-controlled neutral leg, which is the combination of the first two;
- independently-controlled neutral leg, without the connection between the mid point of the filter capacitors and the neutral wire.

The target of the control systems is the same for each configuration and are:

- to compensate the zero sequence voltage with a voltage loop control. The control changes according to the topology studied;
- to control the middle point of the four leg to eliminate the oscillation due the unbalances of the loads with different control strategies.

In order to achieve the targets followed, a control strategy equal for each configuration is used. The common control strategy used includes:

- the control of amplitude of the grid voltage, using a voltage loop control for positive sequence;
- the compensation of the unbalances due to the loads connected to the grid, using negative sequence control to eliminate the -50 Hz component.

Thanks to these, the grid voltage is perfectly balanced.

The methodology followed is: started with the physical model, then the study of the equivalent circuit to obtain the block diagram. Simultaneously, a simulink model for each configurations is built, adding the control blocks. At the end, after getting the results, a comparative analysis is developed and the results are shown. More specifically, the phases are:

1. **Physical Model**: The Physical models are discussed in 2.2 in such a way to compare all the components belong to. All the models can present two different filters: *LC* and *LCL*-filter, as studied in section 2.4. The models have the possibility to connect balanced and/or unbalanced loads to study the different behaviours.

2. **Equivalent circuit**: Having different targets and different topologies, in the chapter 3.4 and 3.5, the equivalent single-phase circuits are design for positive and negative sequences, firstly, and zero voltage sequence and neutral leg control, subsequently. In this way, being the physical model complex, the study of the voltages and currents behaviours will be easier.

3. **Block diagram**: To achieve the targets imposed, block diagrams are presented, including not only the equivalent circuit but also the control blocks. After a review of all the possible controllers in chapter 3.3, specific values of the controllers used are tuned according to each need. For example, using DC signals, a PI will be used to eliminate the error in the steady-state. On the contrary, a PR will be used with sinusoidal signal to attenuate particular frequency which is the resonant frequency of the controller.

4. **Simulink model**: Starting from the physical models, they are studied without any control, just to test the functions. After, all the control system is included in the model to achieve the targets imposed.

5. **Comparative analysis**: A criterion for compare the different topologies is discussed in chapter 4. Concepts as FFT, in the section 4.2, and THD, talked in section 4.3, are called.

6. **Results**: Comparing the results using same configurations with different filters or different control strategies, results are obtained in Chapter 4.2 looking at the harmonic spectrums.

5.2 Conclusions

From the analysis and simulations performed in this thesis, the following conclusions can be categorized as follows, in order of relevance of entrances:

- **Passive Filters**: Generally speaking, filters are used to attenuate the harmonic content of voltage and current which will inject in the grid. As studied in chapter 2.4, filters are a cheap solution for reducing the harmonic content. Adding another inductor to the *LC* filter, the signal should be cleaner than the use of just a *LC*. As seen in Chapter 4.4.1, the effect of the use of *LC* or *LCL* filter is felt in the harmonic content close to the fundamental frequency. However, the difference between the use of *LC* or a *LCL* filter is enough small, in such a way not to influence the functions of the power converters.

- **Use of P, PI, PR or PI in parallel with PR in the inner current loop of neutral leg control**: Focusing on just the two configurations with four legs and split DC-link capacitors, studied in section 2.2.3 and 2.2.4, and controlling the neutral voltage U_N, the controllers in the inner current loop can be differents, as just talked in the Chapter 4.4.3. The harmonic contents close to the fundamental frequency of voltages and currents in the system depend directly on the controllers.

  Anyway, the system works perfectly, independently the type of controllers used, as talked in the section 4.4.3, and the targets are achieved.

  Independently from the general behaviours, a problem could be the current which flows through the neutral inductor L_n, as shown in the fig. 4.4.48, 4.4.49, 4.4.50 and 4.4.51. Using a P or PI, the error ϵ_i, between the output of voltage controller and the real signal i_{LN}, will not be zero because they are not able to follow a sinusoidal reference. This means that if the current i_{Ln} is high, the controller will not be able to reduce its amplitude. On the contrary, a PR or PI in parallel with a PR can follow the sinusoidal reference, without any error ϵ_i, and regulating its amplitude.

- **THD**: The total harmonic distortion of grid voltage, seen in section 4.3, obviously depends on the type of filter, but in each configurations with different filter the value doesn't present a significant

change, independent from the nature of the loads. The total harmonic distortion remains inside the voltage distortion limits allowed by the IEEE, as shown in the table 4.9.

- **DC offset**: Regarding the topologies which include the fourth leg, there is the possibility to close or no the neutral voltage loop to control the neutral leg, as talked in section 4.4.2. Leaving the fourth leg in open-loop, zero voltage sequence U_o and neutral voltage $_N$ have a high DC offset independently from the nature of the loads. The DC component is not present in the other two options, which are: zero voltage sequence control and neutral leg control in closed-loop or zero voltage sequence in open-loop with four leg control in closed-loop.

  For example, considering the topology of three-phase power converter with four legs and split DC-link capacitors, the currents through in the neutral path and in the neutral inductor have a relevant DC component with unbalanced loads. With a lower amplitude, a DC offset is presented in the grid voltage and grid current with unbalanced conditions. Having a DC offset means that the average value of the periodic waveform is greater than zero, or equivalently, the value is positive more than it's negative. In general, DC offsets aren't accepted in a AC power distribution/transmission systems, as the systems aren't designed to handle them. For example, since DC doesn't pass through transformers, protective equipment that uses current transformers won't be able to detect a DC current offset.

Generally, it's possible to say:

- **Conventional Neutral Leg**: This topology has just four legs. Without split DC-link capacitors, the grid voltage and current don't have component at switching frequency, independently from the unbalances. This implies that it can be connected to the without any restriction due to particular load or requested from the grid. It has also a small switching frequency component in the current through the neutral path. A negative aspect could be the presence of a high value of switching frequency in the neutral voltage, which is the voltage used in the neutral leg control. It is more convenient to work with zero voltage sequence and neutral leg controls in closed-loop to avoid for example the problem of DC-component.

- **Split DC-link Capacitors**: The configuration without the fourth leg has just the complication of zero voltage sequence control. The negative aspect is that the neutral point of the inverter has oscillation, with unbalanced loads, and the voltage in capacitors in the DC-bus has 50 Hz component.

- **Independently Controlled Neutral Leg**: Using this configuration is possible to control, at the same time, zero voltage sequence and neutral leg. In this way, there will not be oscillation of the neutral point of the inverter in case of unbalanced load. The grid voltage and current don't have harmonic content at switching frequency. In this way, it can work with different type of loads, without any problems. The issue could be the choice of the controller in the inner current loop in the neutral voltage current.
- **Independently Controlled Neutral Leg, without the connection between the filter and the neutral wire**: The behaviour is similar to the previous one, just with switching harmonic in grid voltage and current with unbalanced load. This implies that this type of three-phase power converter isn't adapt to work with all type of loads. For example, connecting it to a motor doesn't affect the function of the motor. On the contrary, connected a single-phase load to this topology can affect the function of it due to the high component at switching frequency.

5.3 Recommendation

According to the results, in case of unbalanced loads connected to the power converter, the best configurations are which have the fourth leg, which are:

- Conventional Neutral Leg, studied in chapter 2.2.1
- Independently Controlled Neutral Leg, view in chapter 2.2.3
- Independently Controlled Neutral Leg, without the connection between the filter and the neutral wire, analysed in chapter 2.2.4.

Not controlling the fourth leg, generally, there is oscillation of mid point of the neutral point, as shown in Chapter 3.5, which could generate unbalanced/variable output voltage, DC component in the output, larger neutral current. For these reasons, there is often a need to have a neutral line to work with inverters. In the case with just split DC-link capacitors, 2.2.3, despite the control of zero sequence voltage, the middle point of the capacitors has oscillation at 50 Hz. On the contrary, this doesn't happen with the control of neutral leg.

Having the fourth leg and leaving it in open-loop is not sufficient to balance the grid voltage, because, as seen in 4.4.2, there will big a big DC-component, which disturb the system.

Regarding the topology which just four legs, 2.2.1, it's possible to control the fourth leg but not the current flowing through the neutral path, as seen in 3.5.

For this reason, the best configurations are which have split DC-link capacitors and four legs, 2.2.3 and 2.2.4, where controlling the fourth leg, also the current in the neutral path is controlled, including in the inner current loop of the neutral control a PR. In this way, the current i_{LN} flowing in the neutral inductor L_n will follow the reference, without risking having a high value.

Analysing the unbalanced load, if the load is for example a motor, the two topologies with split DC-link capacitors and four legs, 2.2.3 and 2.2.4 are usable, despite the grid voltage has component at 10 kHz, as shown in section 4.4.4. If the load is more sensitive to the variation of the voltage, the best configuration is the topology with split DC-link capacitors and four legs, 2.2.3, because thanks to the connection between the middle point of filter's capacitors, the grid voltage will be clear, without component at switching frequency.

Appendix A

Harmonic Spectrum

A.1 Conventional Neutral Leg with *LC*-filter

The topology is studied in the section 2.2.1.

A.1.1 c. balanced load with *LC*-filter

Starting with a balanced load, the results are A.1.1-A.1.9.

A.1.2 d. unbalanced load with *LC*-filter

Connecting an unbalanced load, the results are shown in fig. A.1.10-A.1.19.

A.2 Split DC-link Capacitors

The topology is studied in the section 2.2.2.

A.2.1 c. balanced load with *LC*-filter

With a balanced load the figures are A.2.1-A.2.9:

A.2.2 d. unbalanced load with *LC*-filter

With an unbalanced load the figures are A.2.10-A.2.18:

A.3 Indipendently Controlled Neutral Leg

This configuration is studied in section 2.2.3.

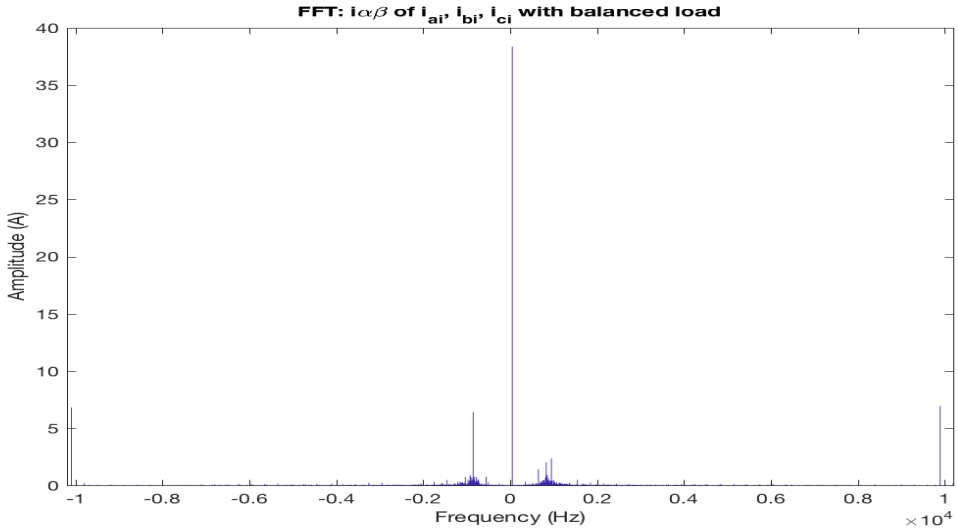


Figure A.1.1: Case 26: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Harmonic spectrum of inverter current

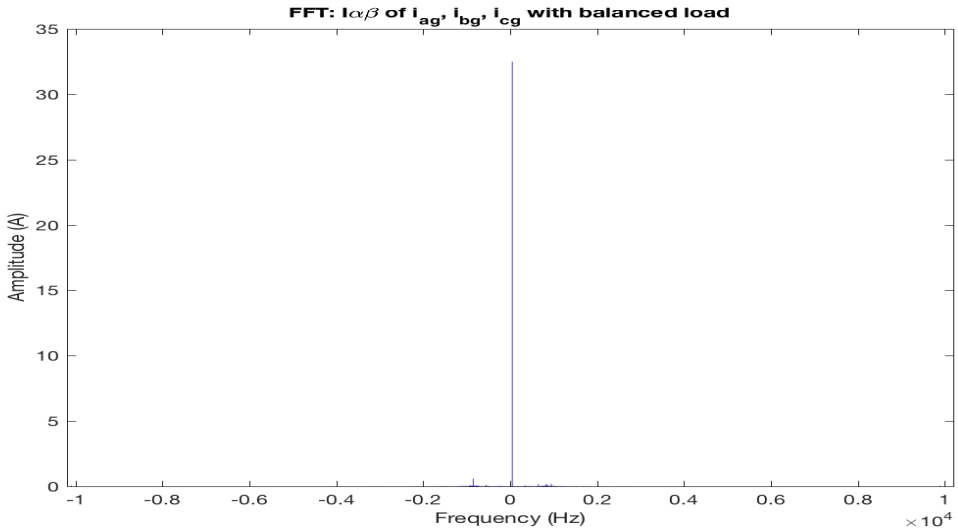
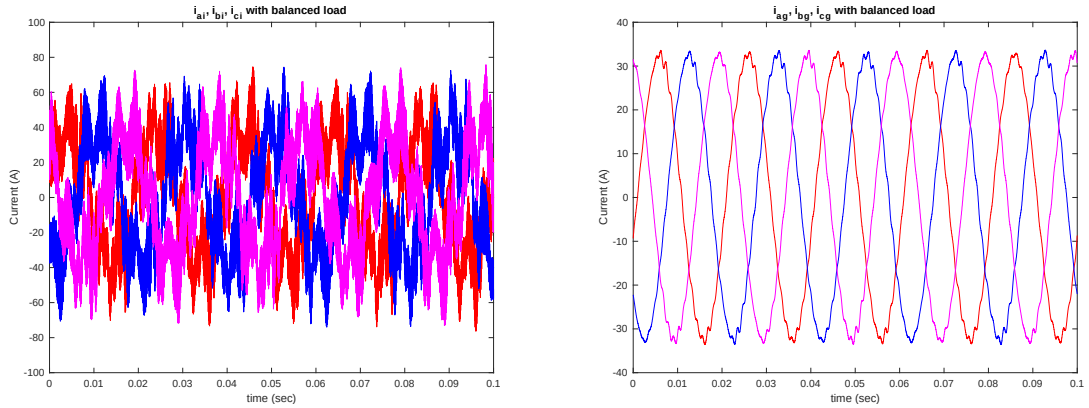


Figure A.1.2: Case 26: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Harmonic spectrum of grid current



(a) **(b)**

Figure A.1.3: Case 26: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) waveform of inverter current; fig. (b) waveform of grid current

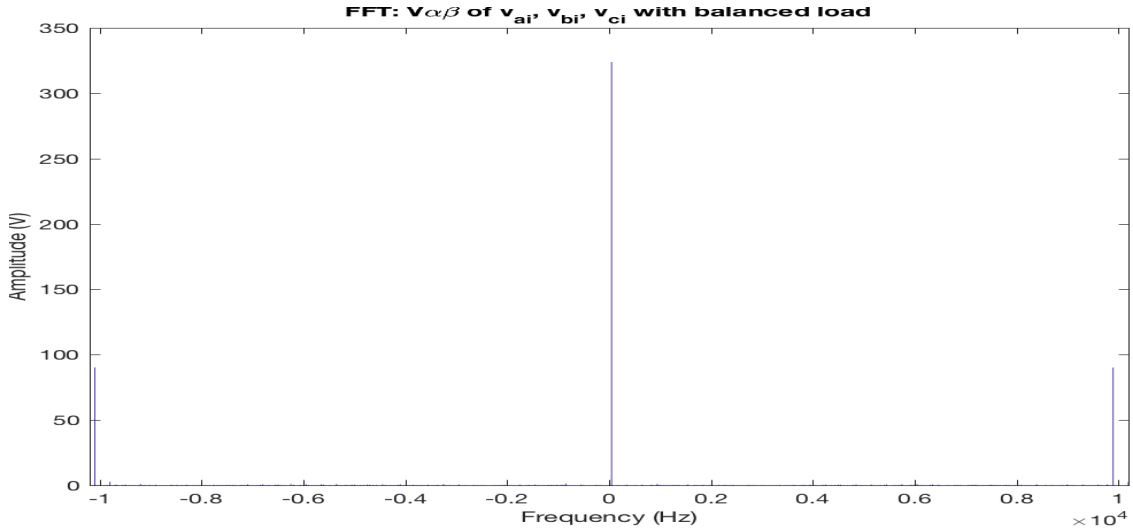


Figure A.1.4: Case 26: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of inverter voltage

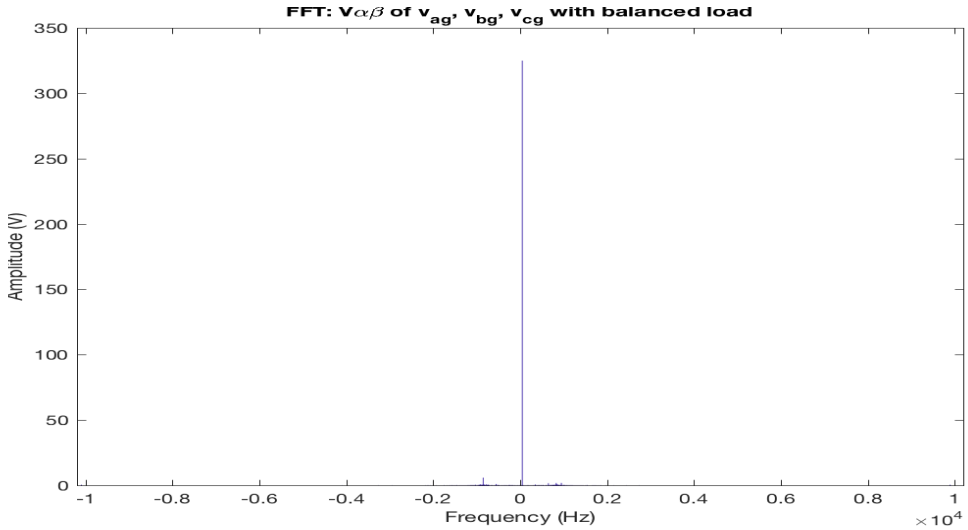
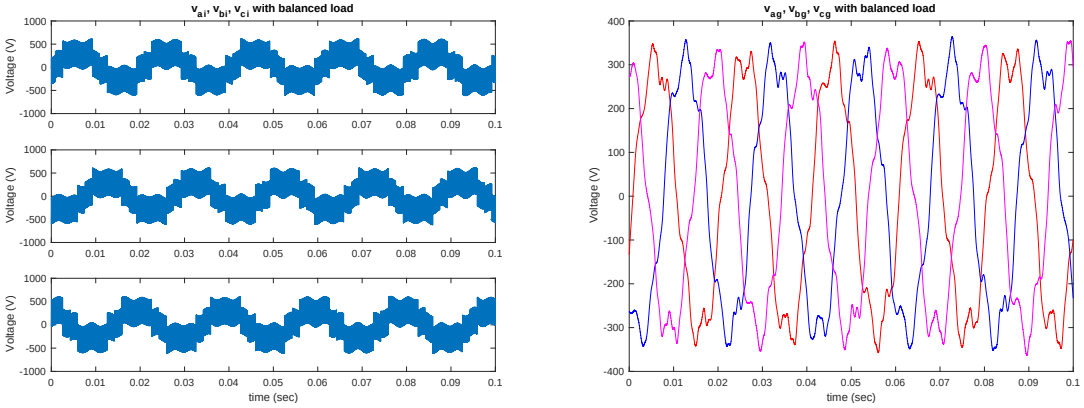


Figure A.1.5: Case 26: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of grid voltage



(a) **(b)**

Figure A.1.6: Case 26: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) inverter voltage; fig. (b) grid voltage

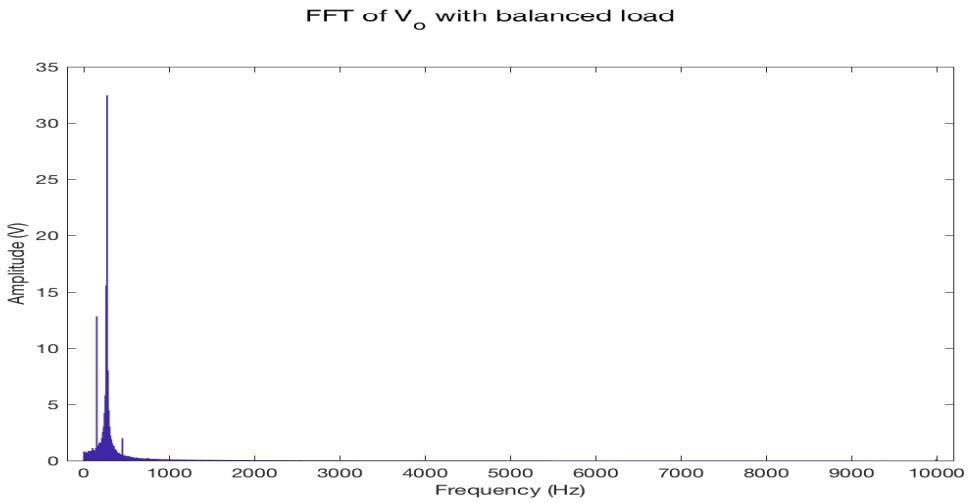


Figure A.1.7: Case 26: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Harmonic spectrum of zero voltage sequence

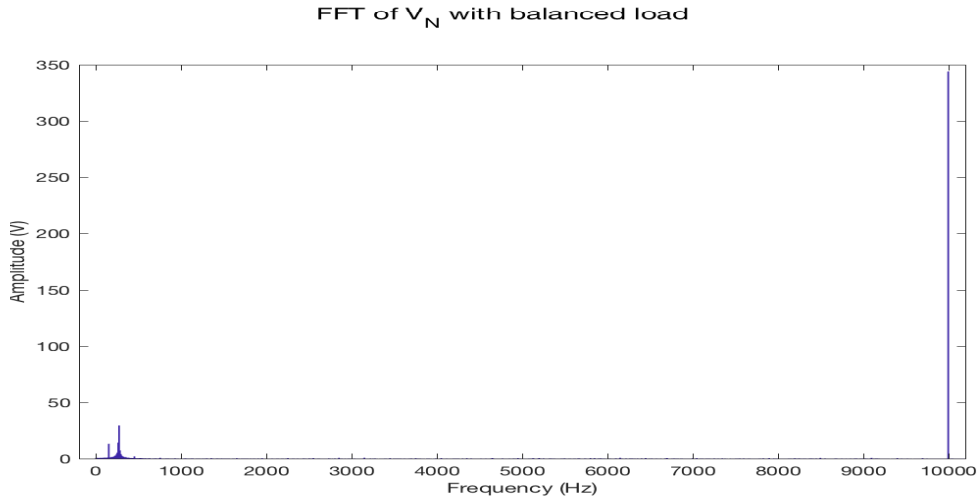
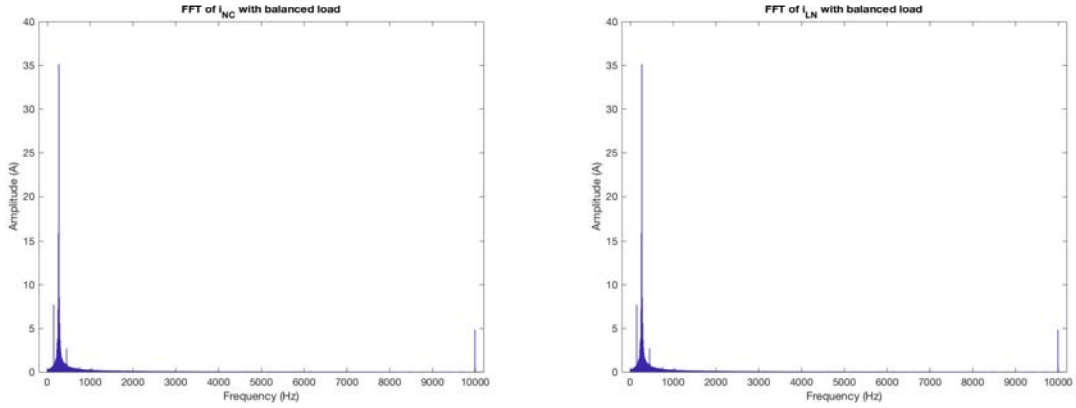


Figure A.1.8: Case 26: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Harmonic spectrum of neutral voltage



(a) i_{NC} **(b)** i_{Ln}

Figure A.1.9: Case 26: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) FFT of i_{NC}. Fig. (b) harmonic spectrum of i_{Ln}

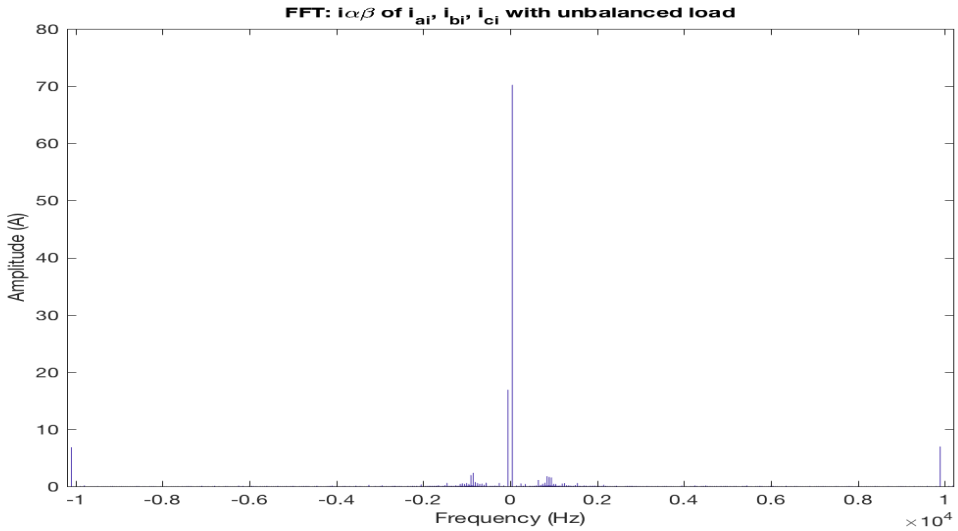


Figure A.1.10: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of inverter current

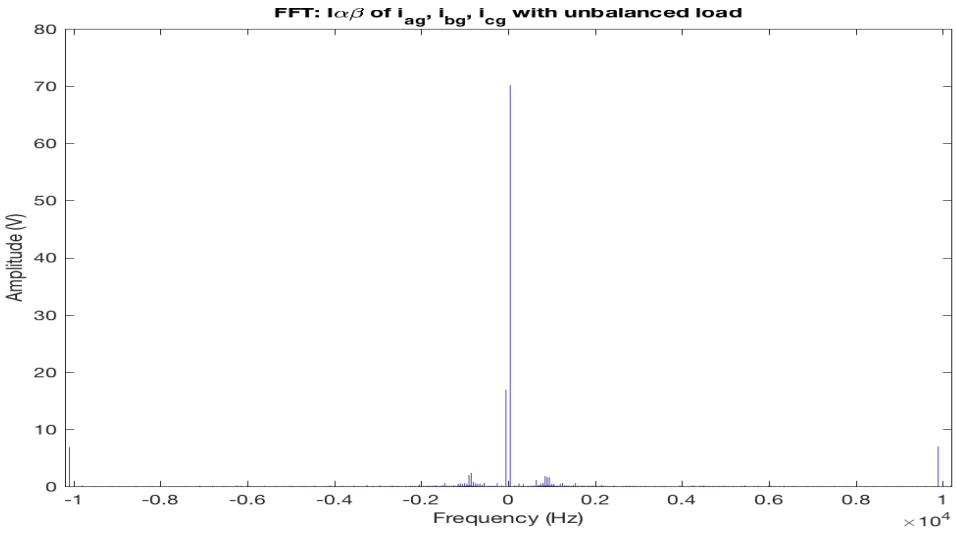
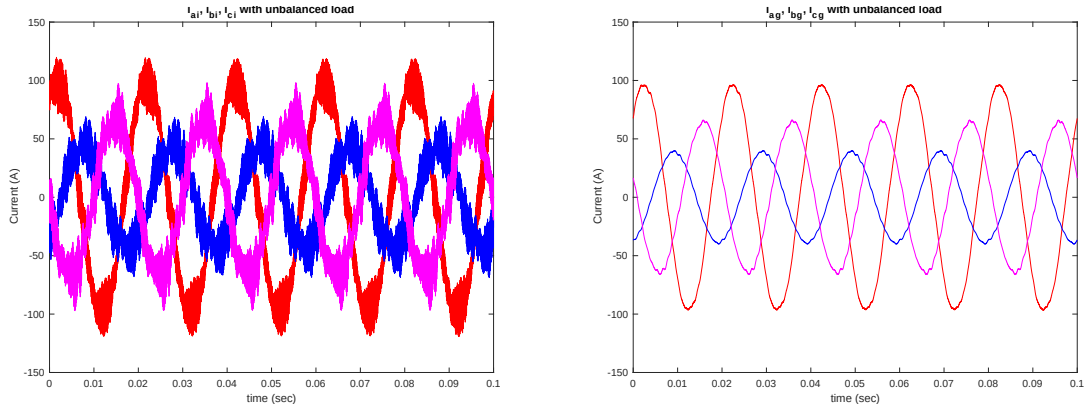


Figure A.1.11: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of grid current



(a) **(b)**

Figure A.1.12: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig.(a) waveform of inverter current current. Fig. (b) waveform of grid current

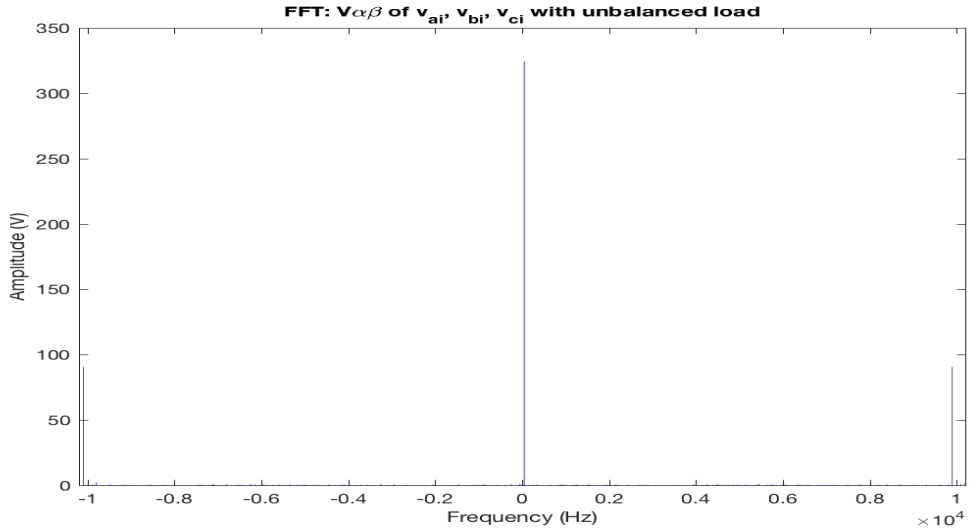


Figure A.1.13: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of inverter voltage

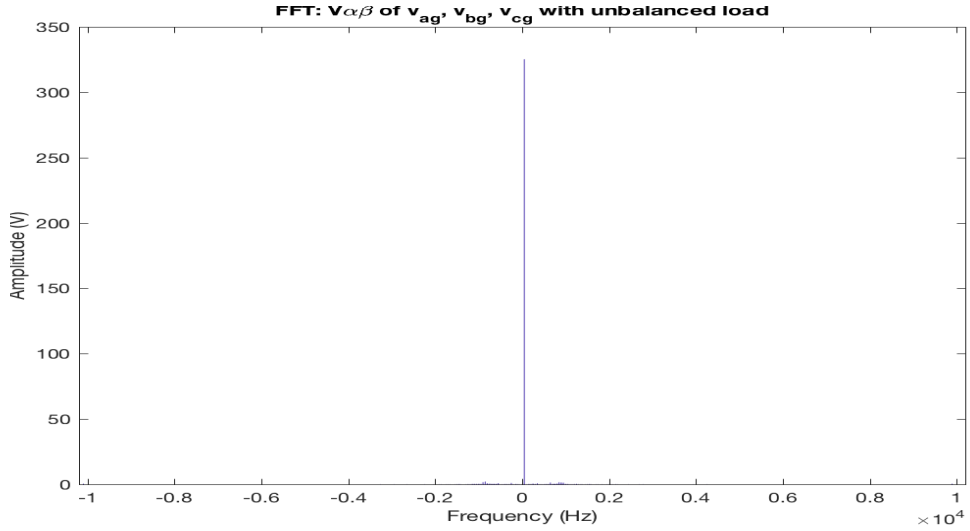
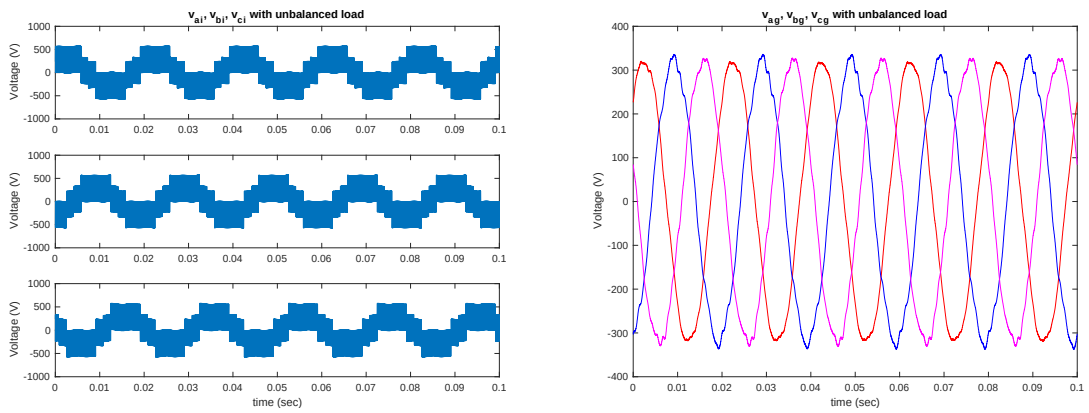


Figure A.1.14: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of grid voltage



(a) **(b)**

Figure A.1.15: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) waveform of inverter current. Fig. (b) waveform of grid voltage

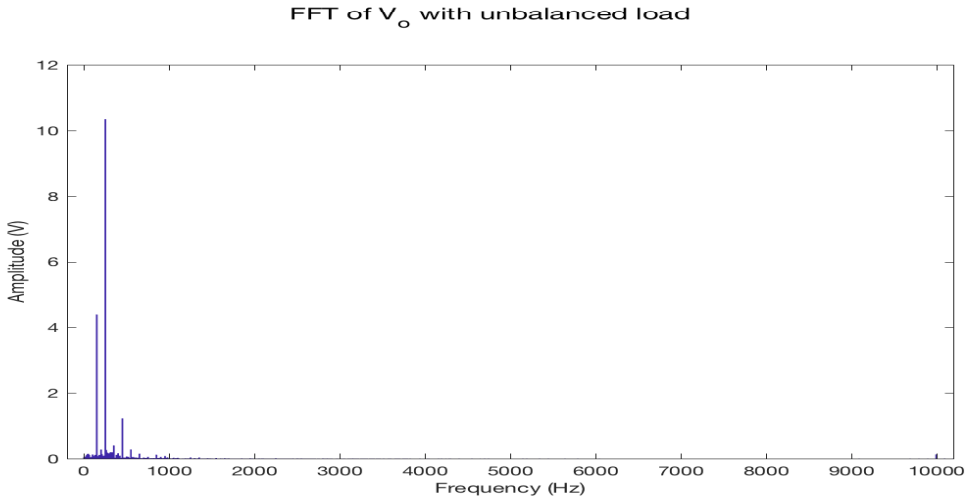


Figure A.1.16: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of zero voltage sequence of grid voltage

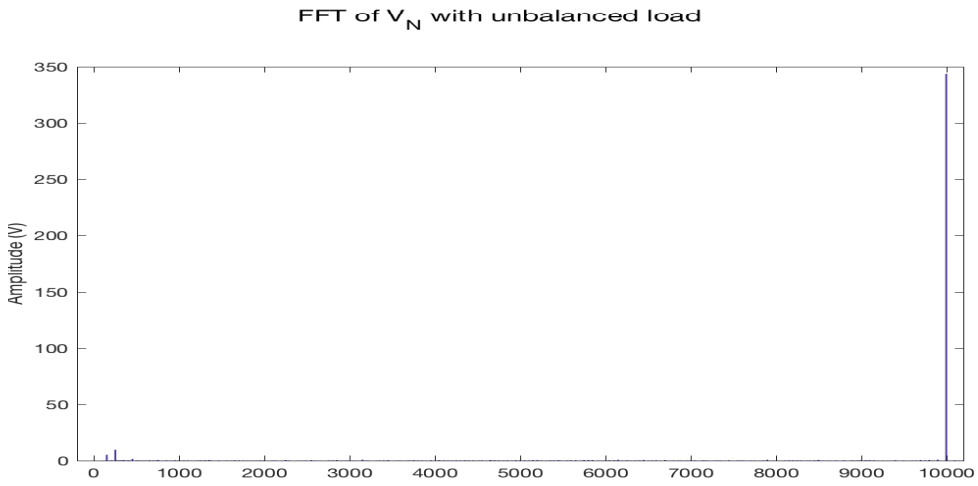
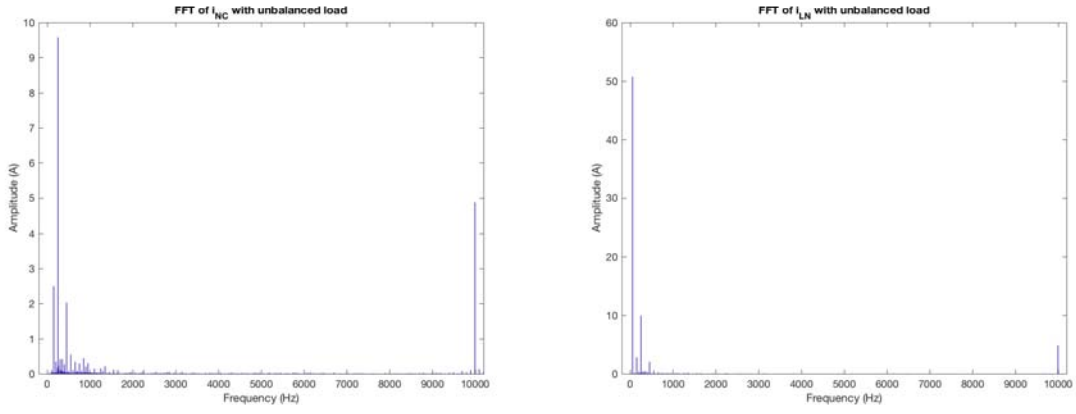


Figure A.1.17: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of neutral voltage



(a) i_{NC} **(b)** i_{Ln}

Figure A.1.18: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; Fig. (a) FFT of i_{NC}. Fig. (b) FFT of i_{Ln}

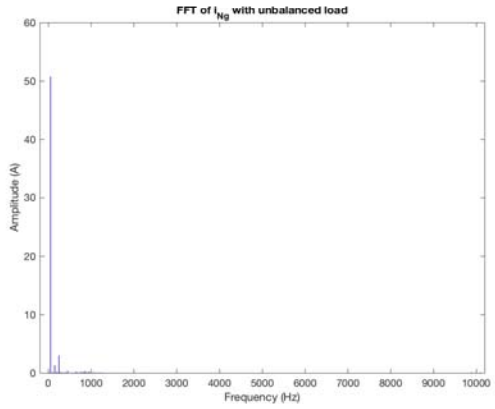


Figure A.1.19: Case 26: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v; FFT of i_{Ng}

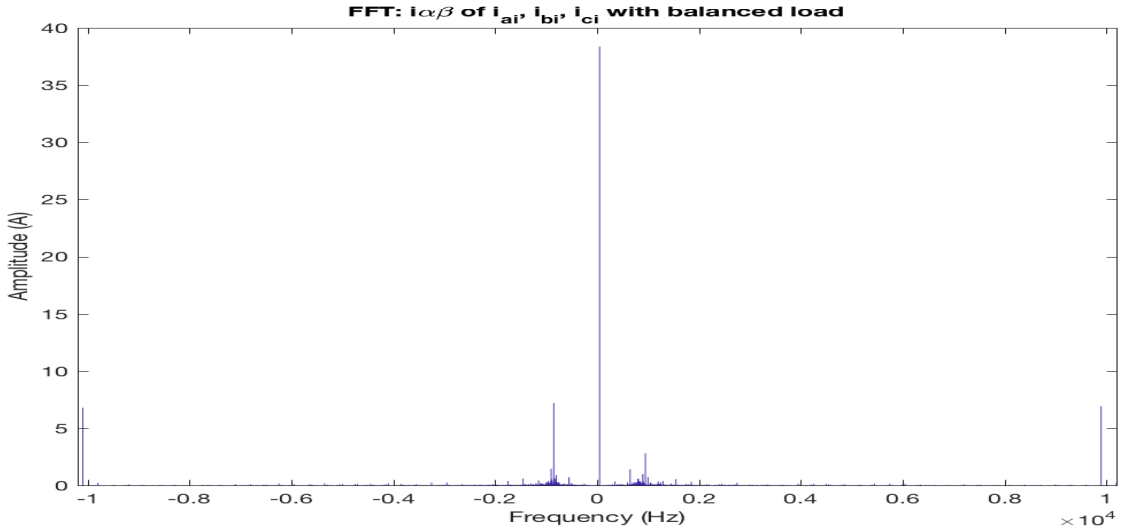


Figure A.2.1: Case 30: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of inverter current

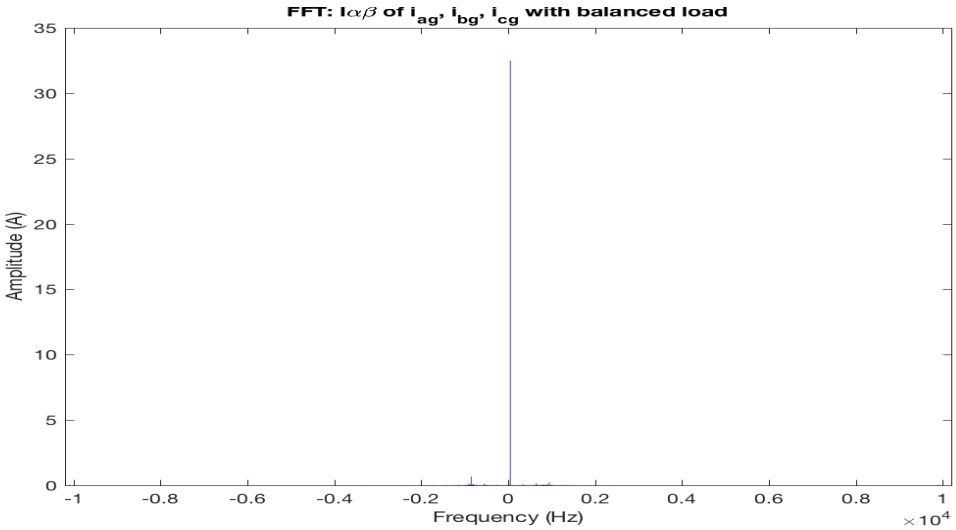
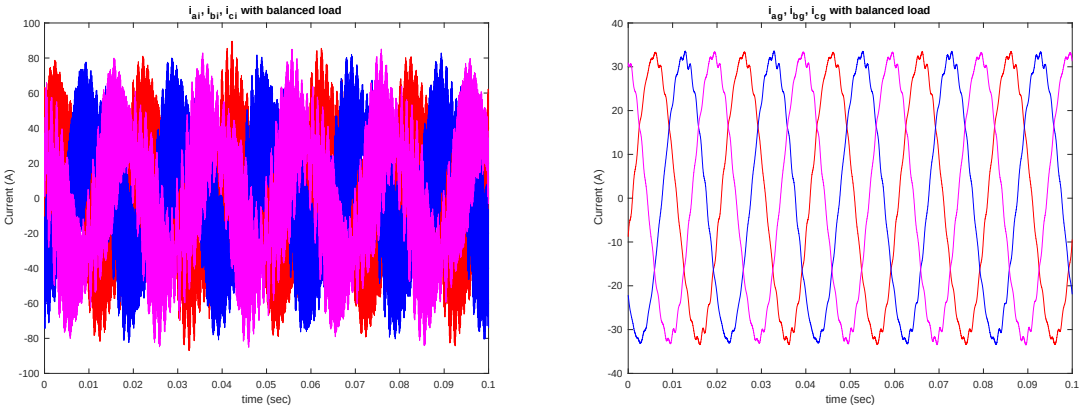


Figure A.2.2: Case 30: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of the grid current



(a) **(b)**

Figure A.2.3: Case 30: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) waveform of inverter current. Fig. (b) waveform of grid current

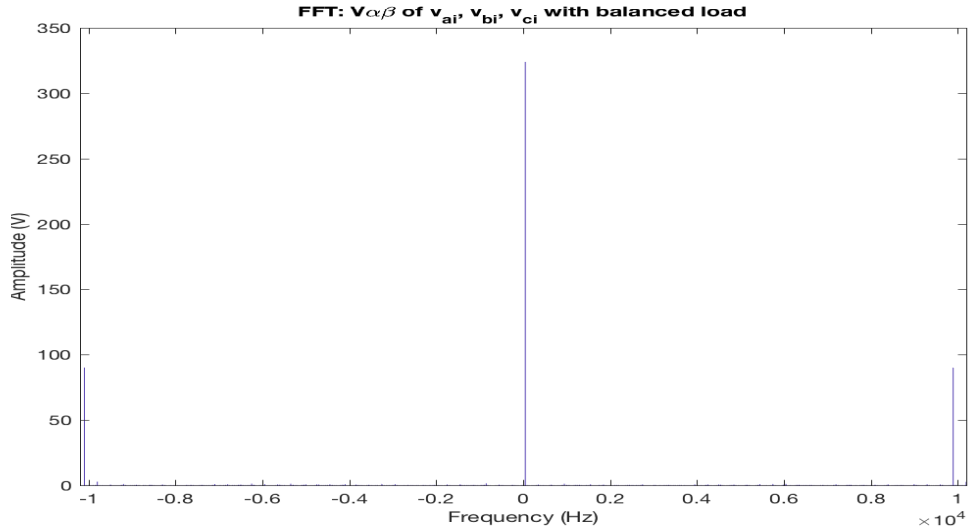


Figure A.2.4: Case 30: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of the inverter voltage

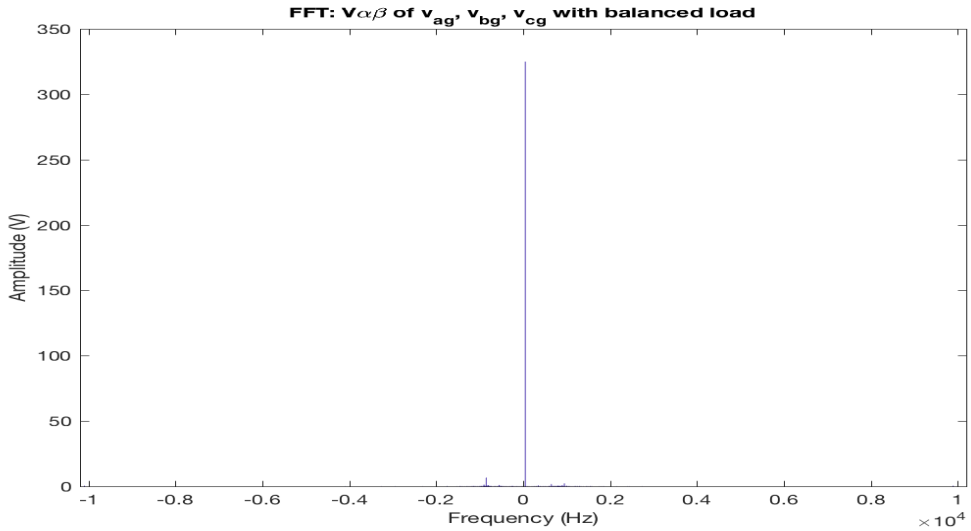


Figure A.2.5: Case 30: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of the grid voltage

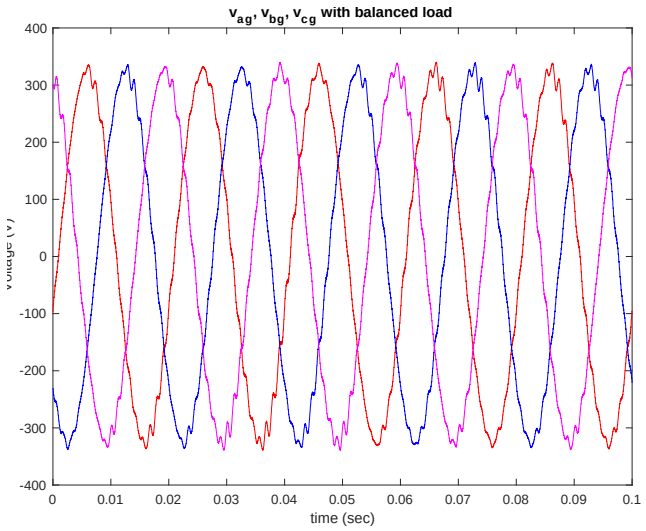


Figure A.2.6: Case 30: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) waveform of inverter voltage. Fig. (b) waveform of grid voltage

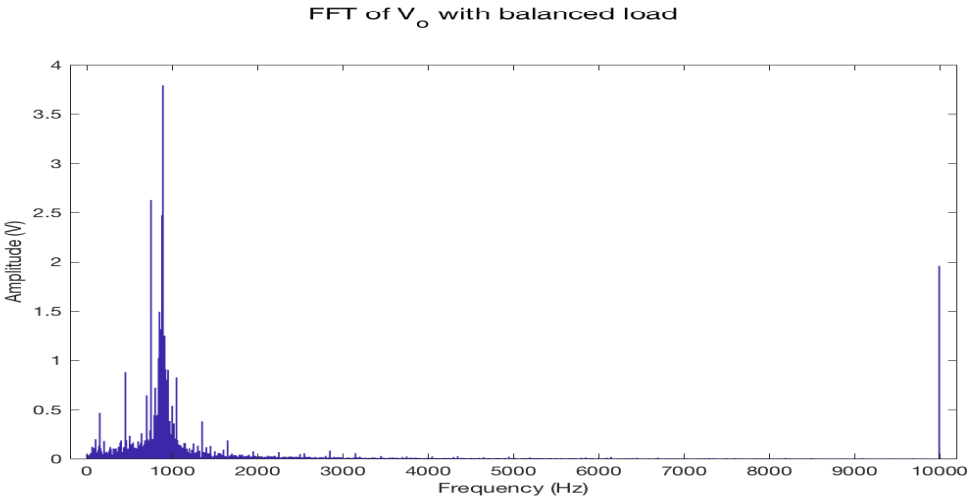
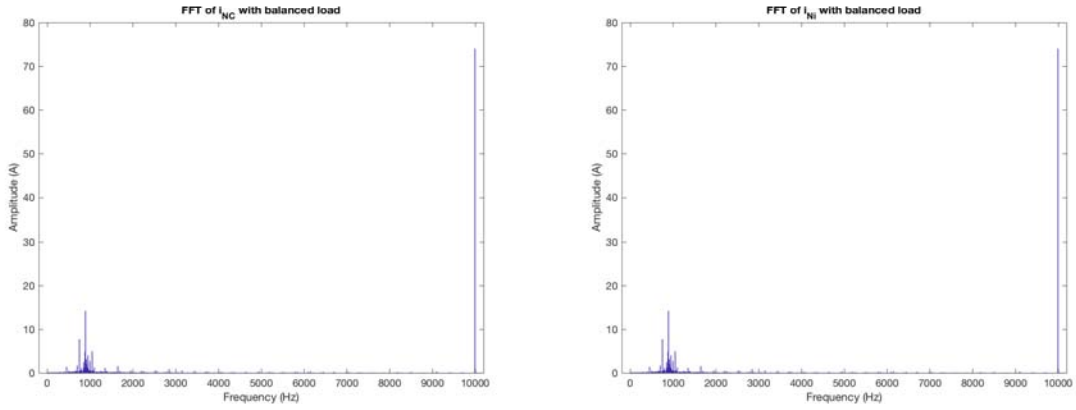


Figure A.2.7: Case 30: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of zero voltage sequence



(a) i_{NC} **(b)** i_{Ni}

Figure A.2.8: Case 30: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) FFT of i_{NC}; Fig. (b) FFT of i_{Ni}

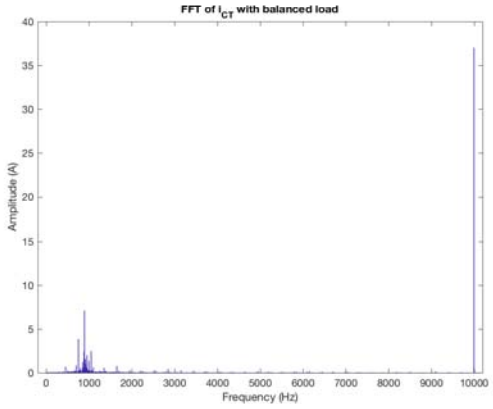


Figure A.2.9: Case 30: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; FFT of i_{CT}

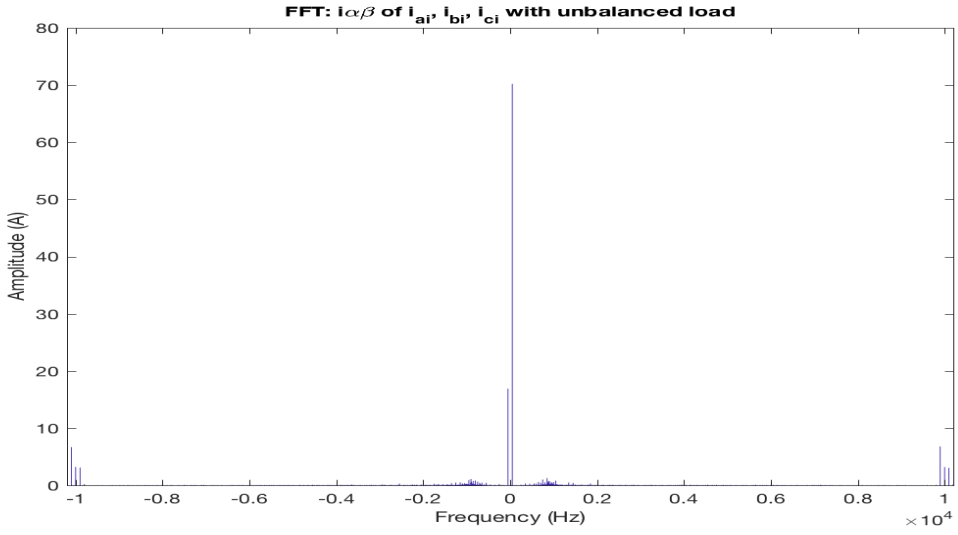


Figure A.2.10: Case 30: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; FFT of inverter current

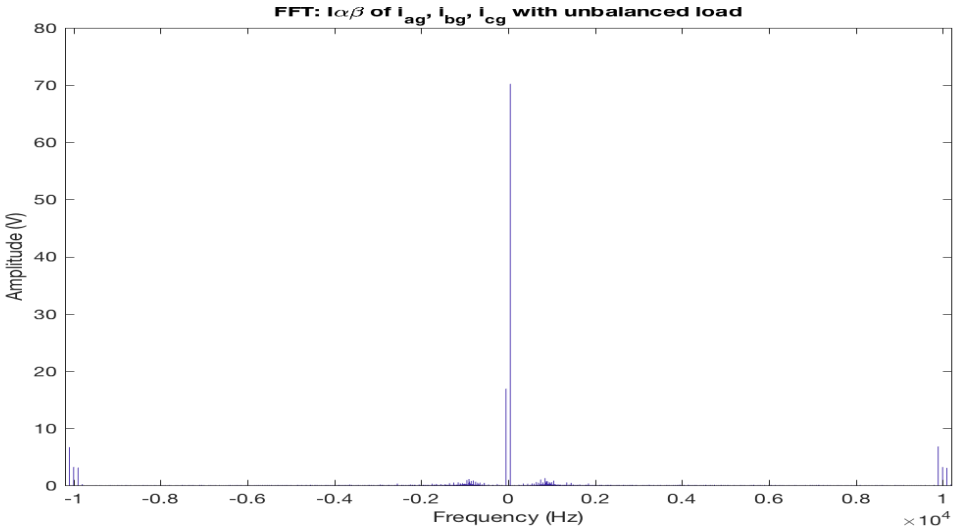
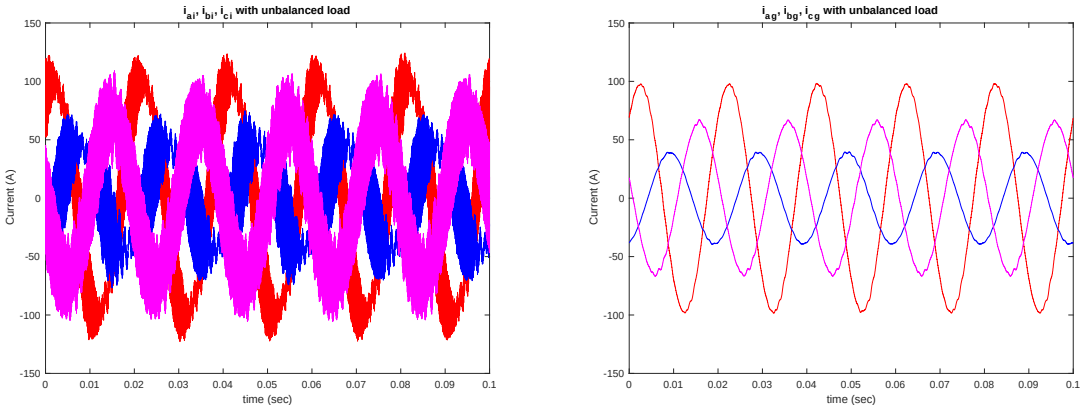


Figure A.2.11: Case 30: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; FFT of grid current



(a) **(b)**

Figure A.2.12: Case 30: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) waveform of inverter current; Fig. (b) waveform of grid current

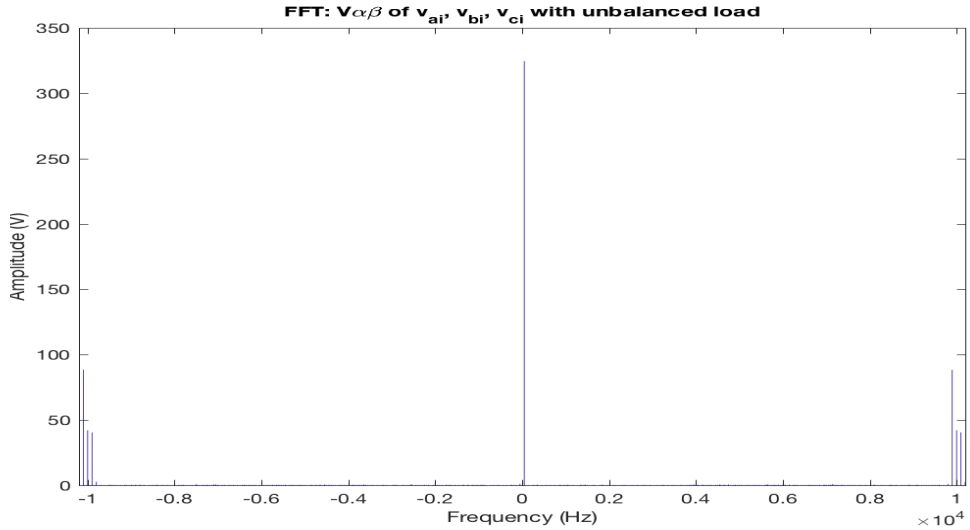


Figure A.2.13: Case 30: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; FFT of inverter voltage

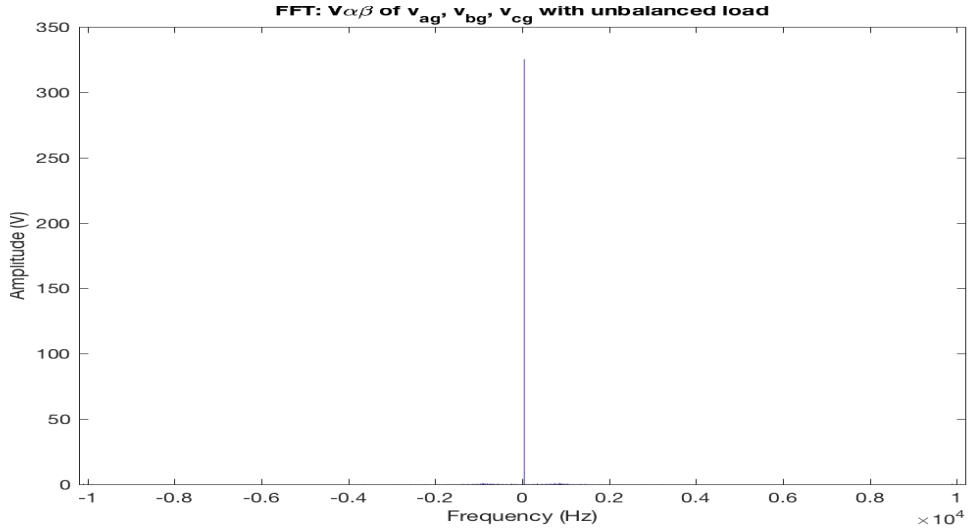


Figure A.2.14: Case 30: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; FFT of grid voltage

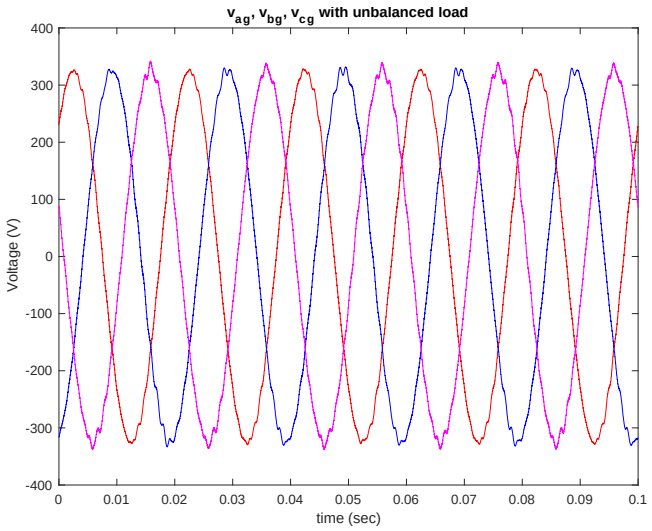


Figure A.2.15: Case 30: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Waveform of grid voltage

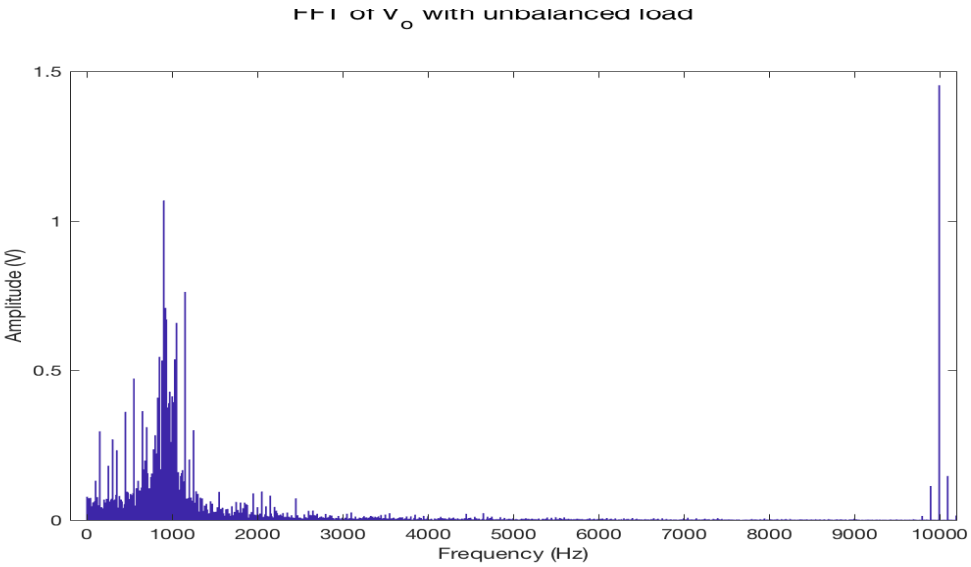
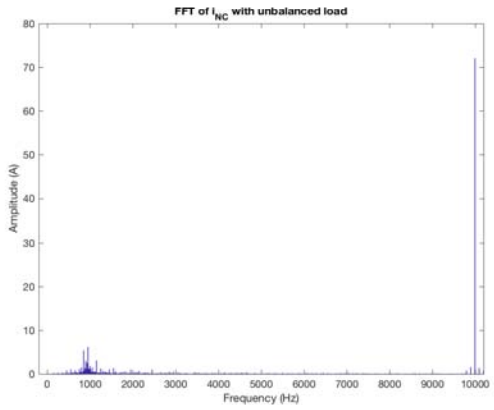
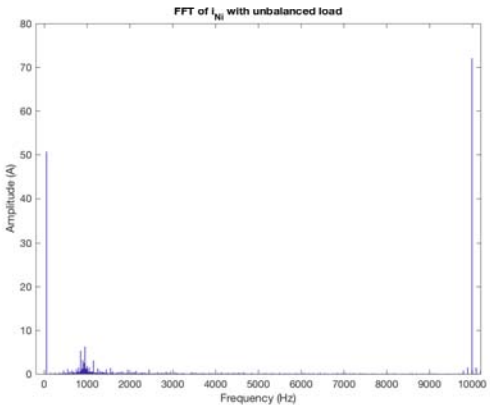


Figure A.2.16: Case 30: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; FFT of zero sequence voltage

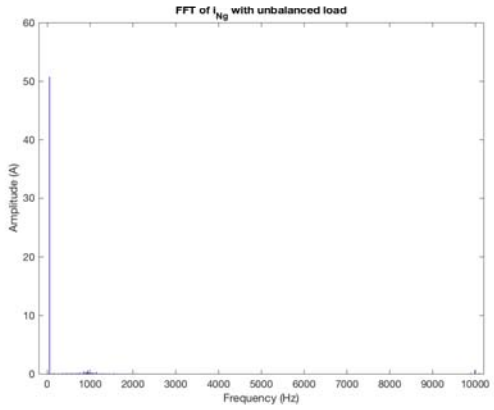


(a) i_{NC}

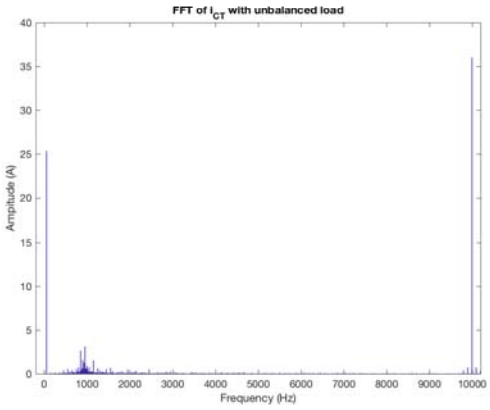


(b) i_{Ni}

Figure A.2.17: Case 30: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) FFT of i_{NC}: fig. (b) FFT of $_{Ni}$



(a) i_{Ng}



(b) i_{CT}

Figure A.2.18: Case 30: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fig. (a) FFT of i_{Ng}: fig. (b) FFT of $_{CT}$

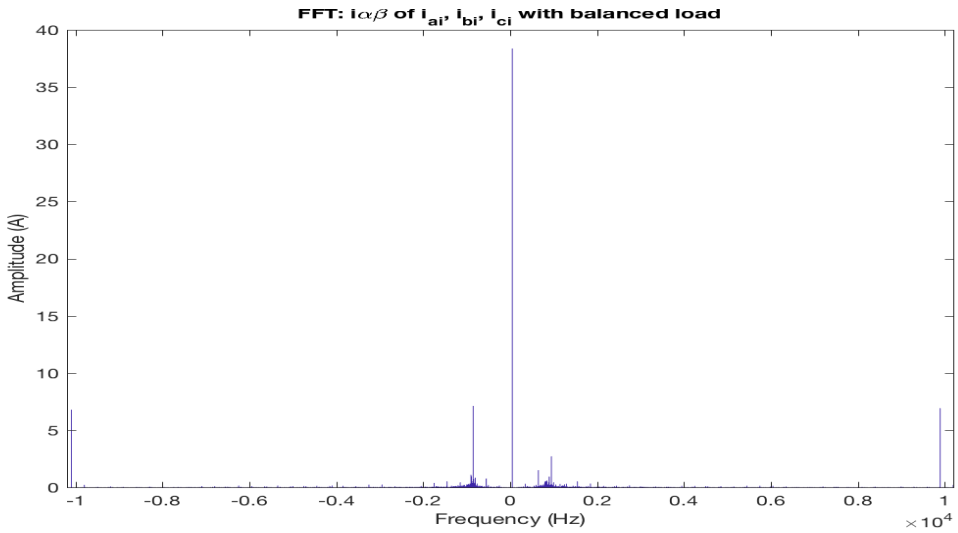


Figure A.3.1: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_V+PR_i; Fourth leg control: PR_V+PI_i; FFT of inverter current

A.3.1 c. balanced load with *LC*-filter

With balanced load, the results are A.3.1-A.3.10:

A.3.2 d. unbalanced load with *LC*-filter

Connecting now an unbalanced load, the results are depicted in fig. A.3.11-A.3.21.

Despite the imbalance, the voltage is balanced, A.3.14 and A.3.15, thanks to the positive and negative controllers.

A.4 Independently Controlled Neutral Leg, without the connection between the filter and the neutral wire

This topology is studied in section 2.2.4.

A.4.1 c. balanced load with *LC*-filter

With a balanced load are depicted in fig. A.4.1-A.4.9:

A.4.2 d. unbalanced load with *LC*-filter

With a unbalanced load are depicted in fig. A.4.10-A.4.20:

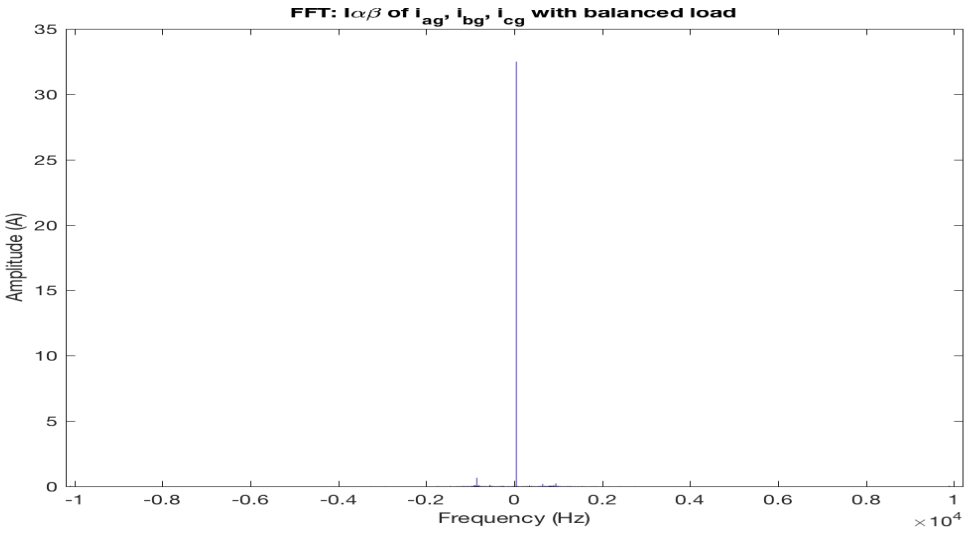
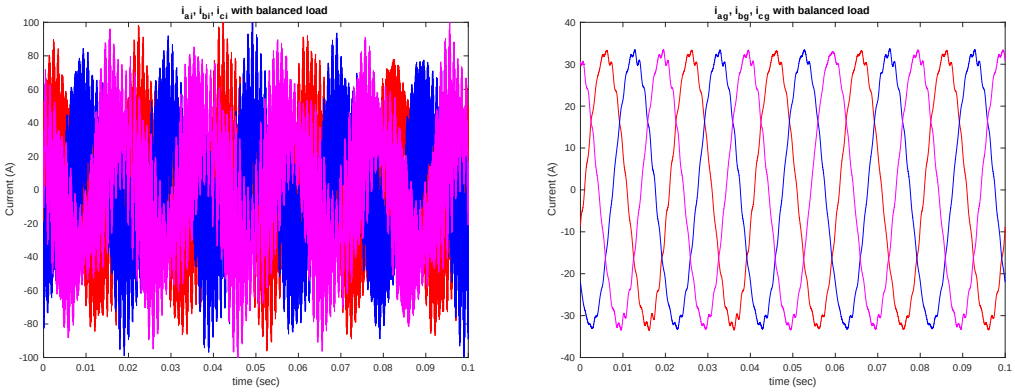


Figure A.3.2: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. FFT of grid current



(a) i_{Ng} **(b)** i_{CT}

Figure A.3.3: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) waveform of inverter current: Fig. (b) waveform of grid current

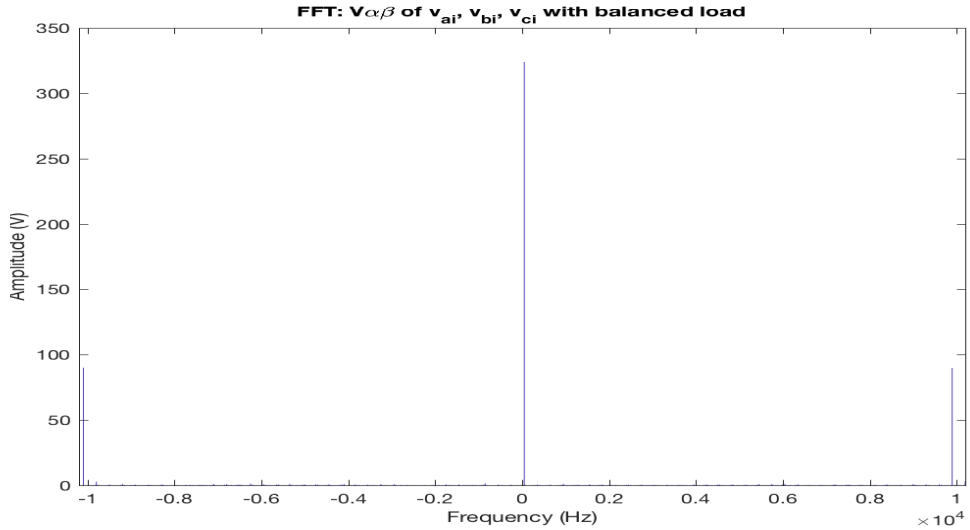


Figure A.3.4: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter voltage

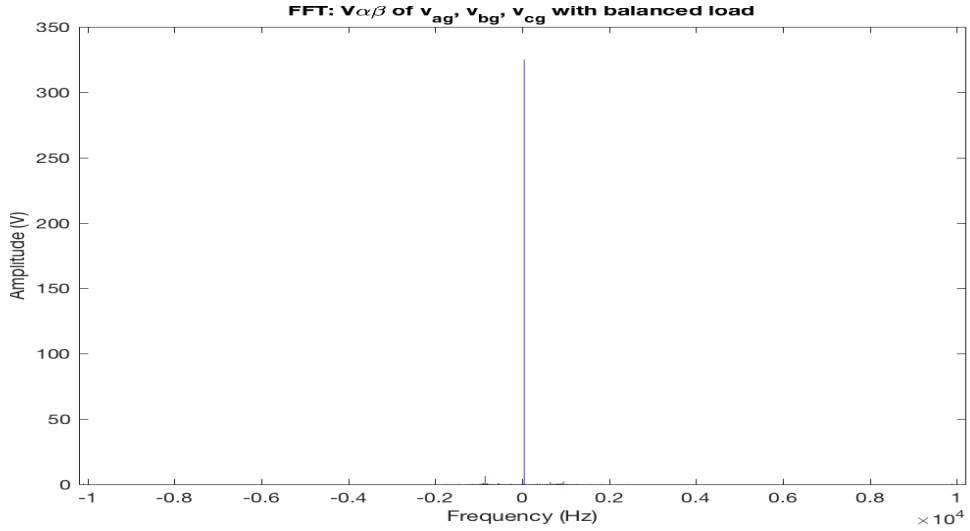


Figure A.3.5: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid voltage

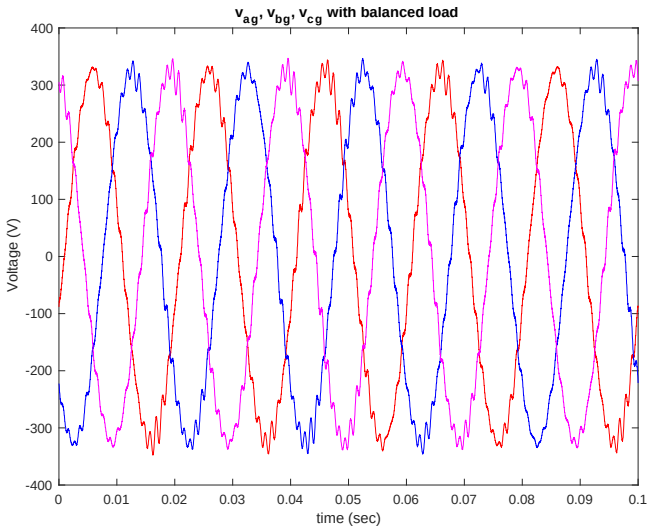


Figure A.3.6: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Waveform of grid voltage

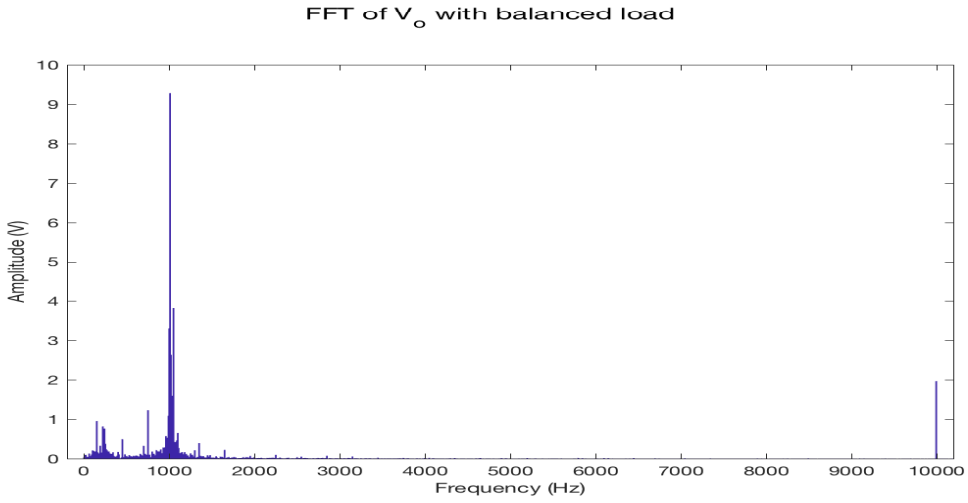


Figure A.3.7: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of zero voltage sequence

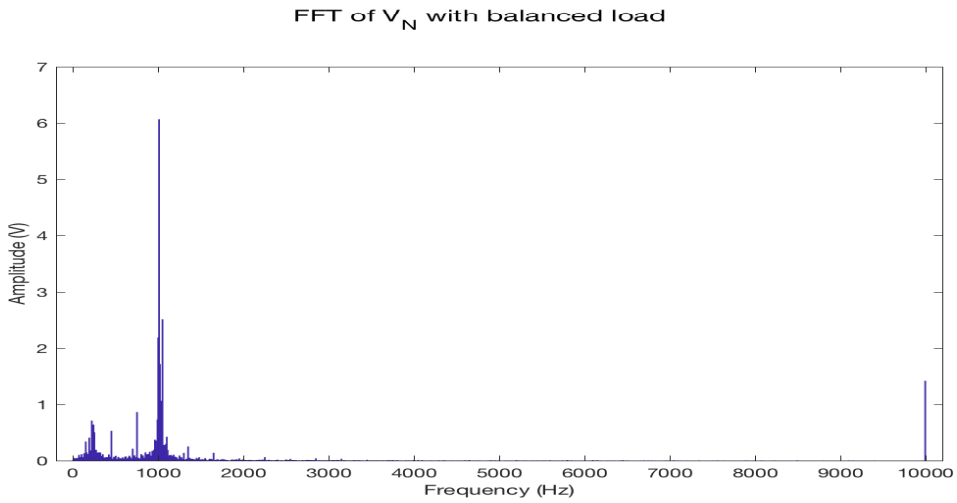
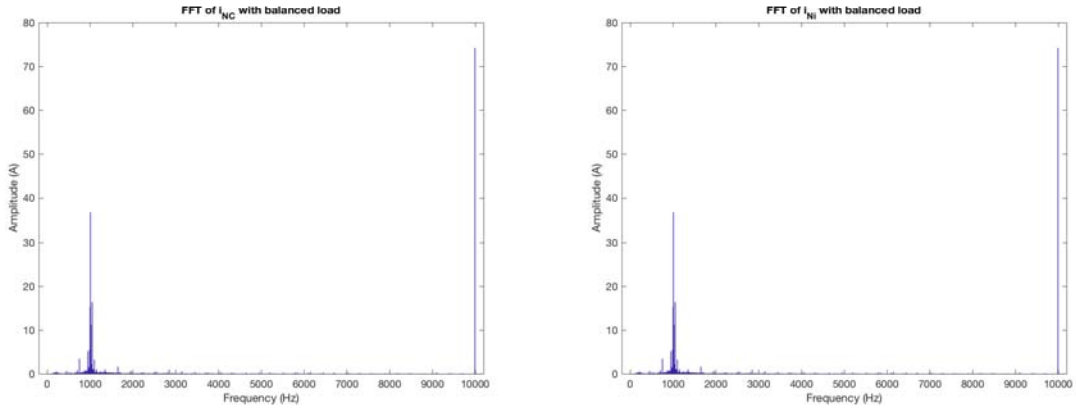
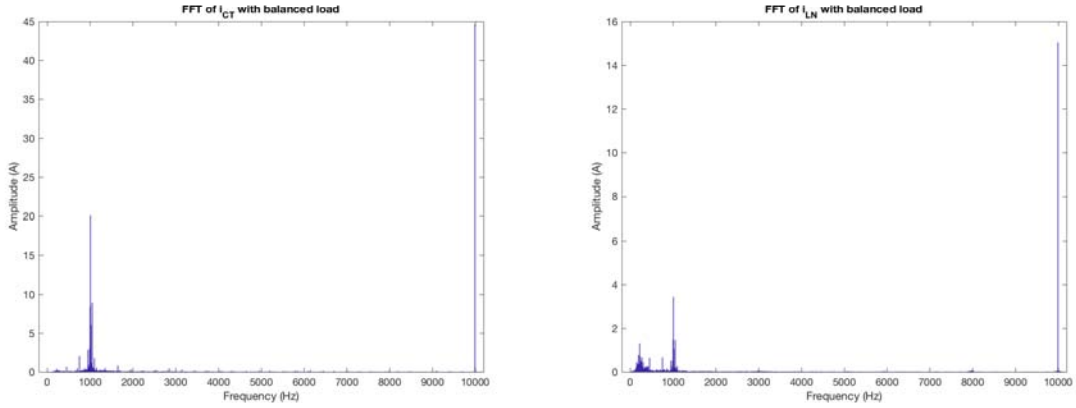


Figure A.3.8: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of neutral voltage



(a) i_{NC} **(b)** i_{Ni}

Figure A.3.9: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig.(a) FFT of i_{NC}; Fig (b) FFT of i_{Ni}



(a) i_{CT} **(b)** i_{Ln}

Figure A.3.10: Case 10: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{CT}; Fig. (b) FFT of i_{Ln}

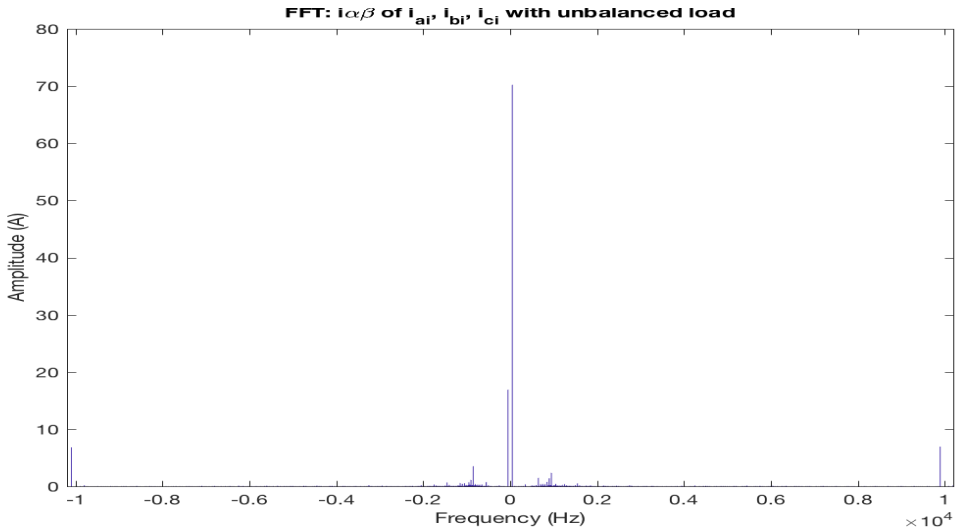


Figure A.3.11: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter current

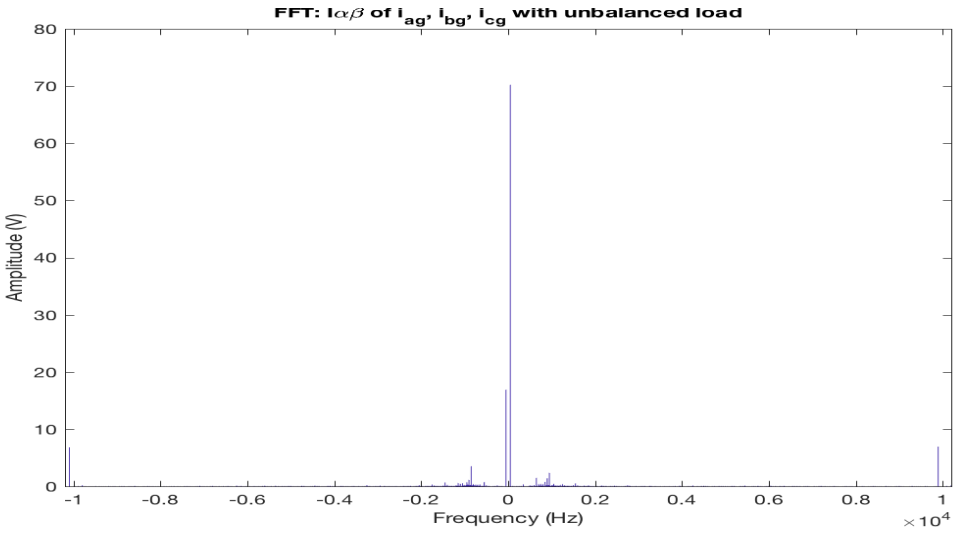
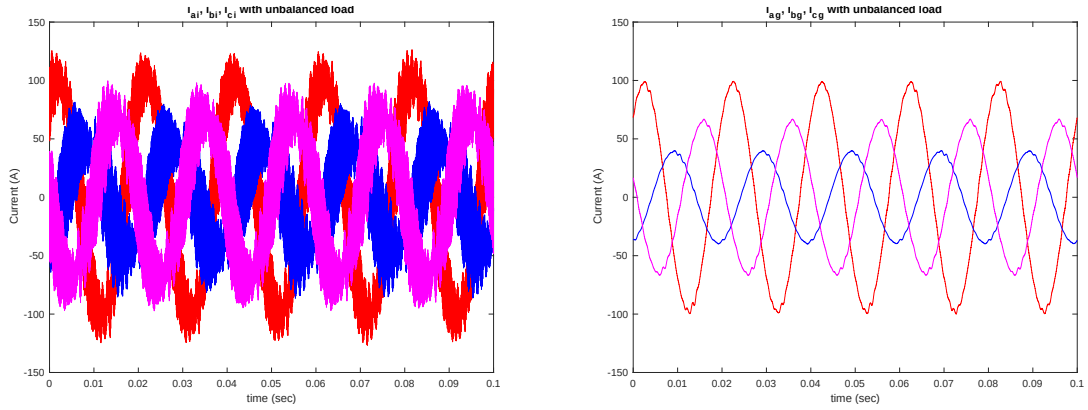


Figure A.3.12: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid current



(a) **(b)**

Figure A.3.13: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) waveform of inverter current; Fig. (b) waveform of grid current

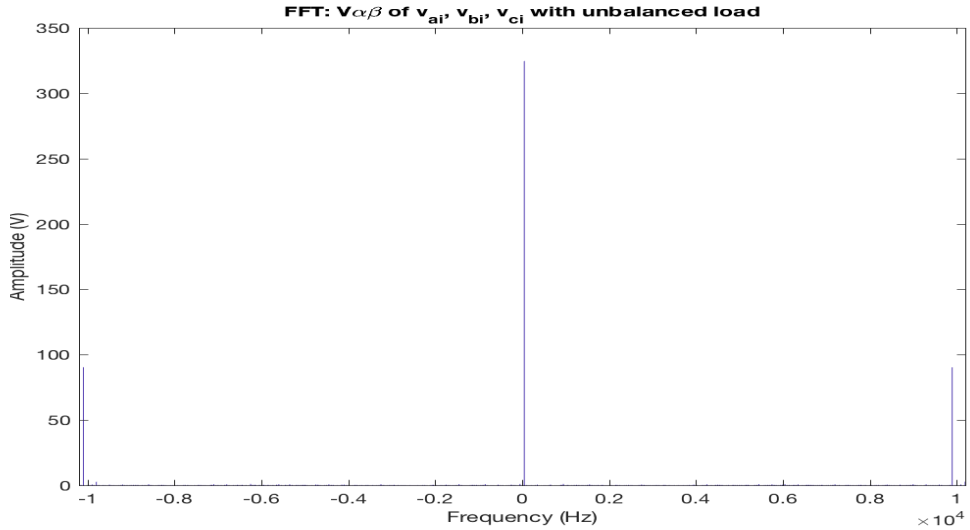


Figure A.3.14: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter voltage

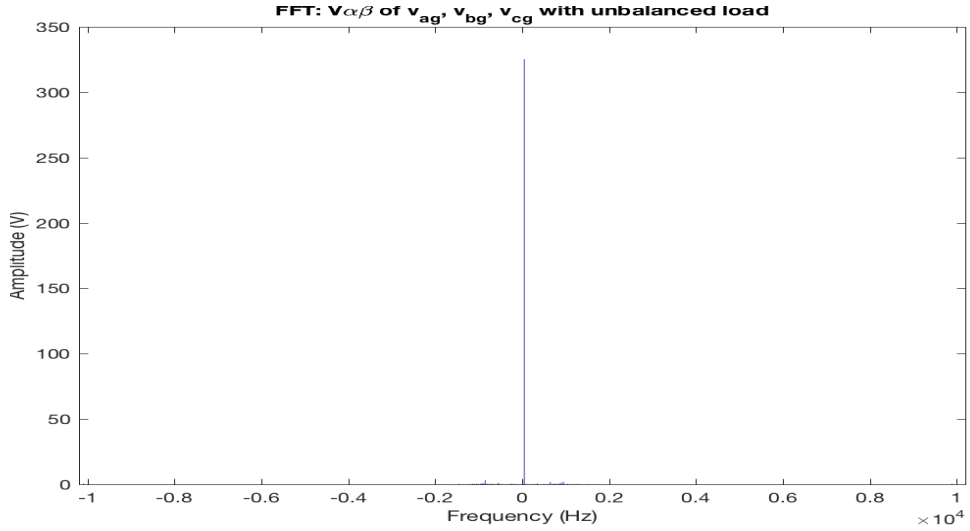


Figure A.3.15: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid voltage

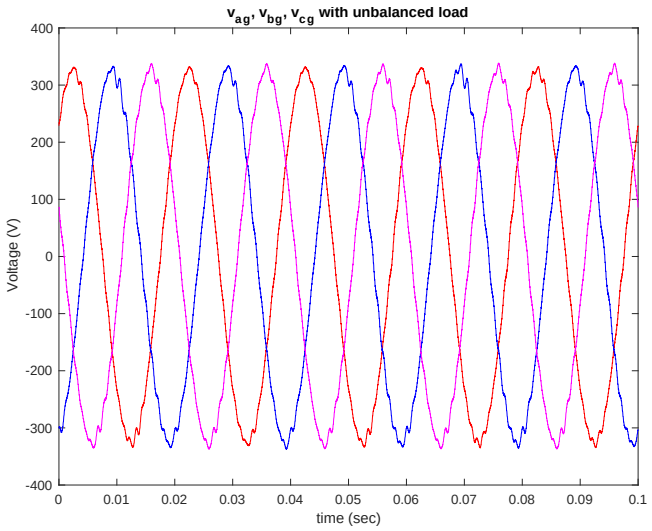


Figure A.3.16: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Waveform of grid voltage

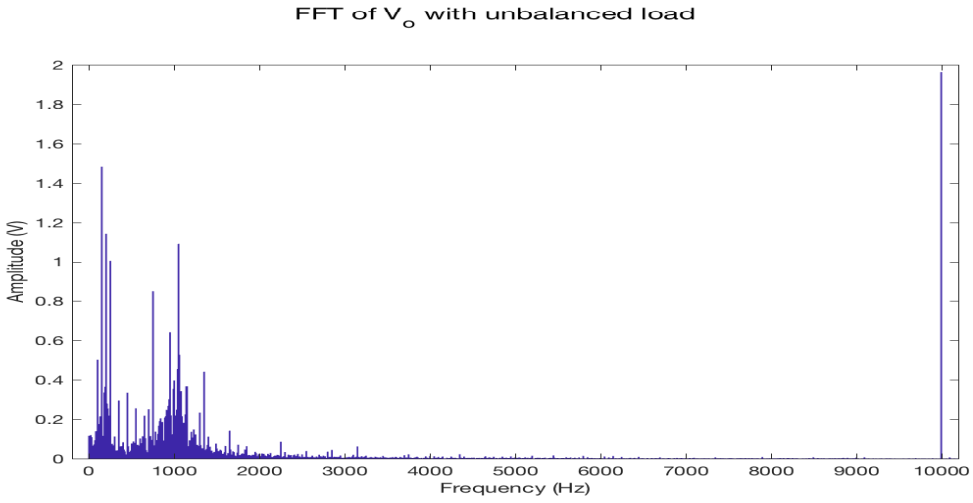


Figure A.3.17: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Harmonic spectrum of zero sequence voltage

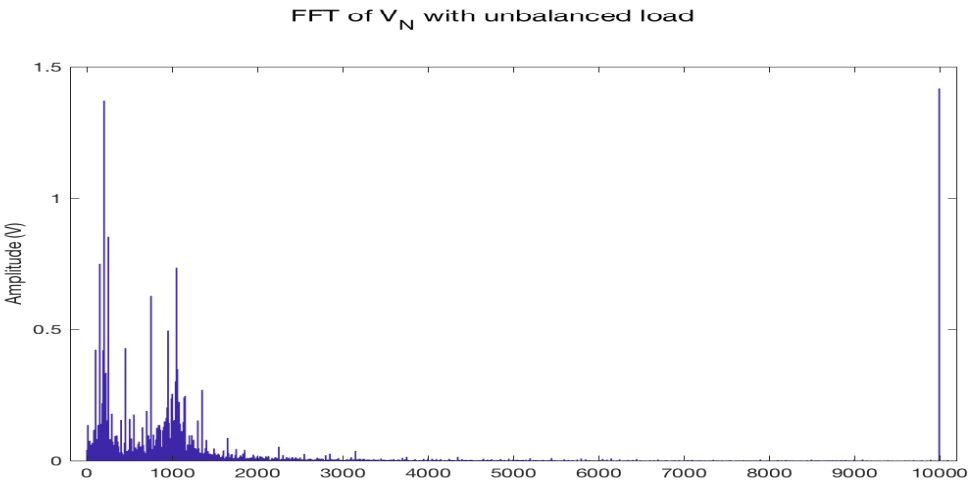
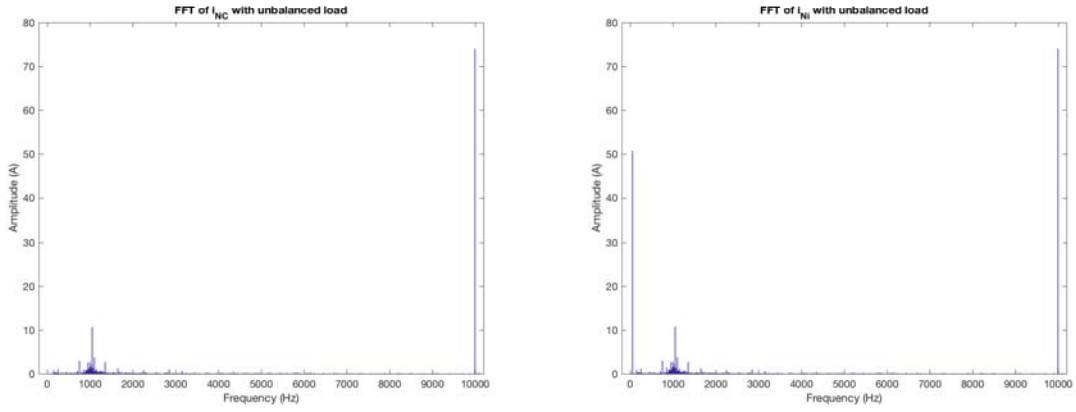
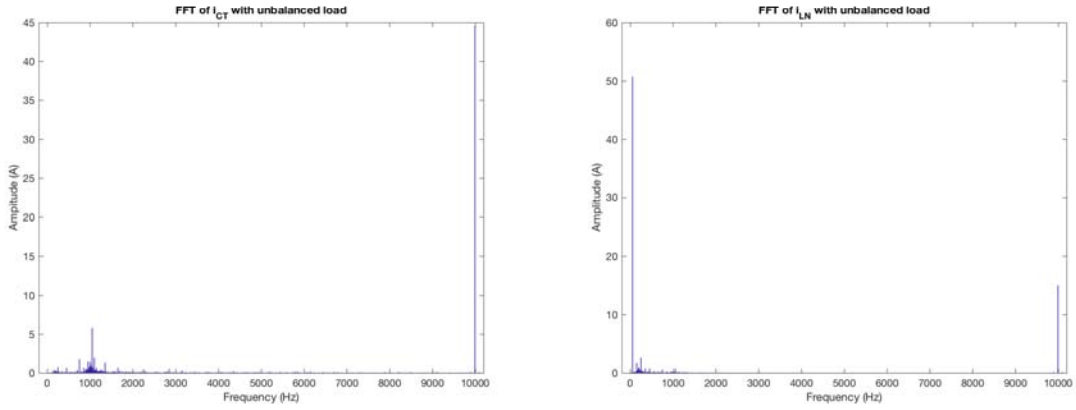


Figure A.3.18: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Harmonic spectrum of neutral voltage



(a) i_{NC} **(b)** i_{Ni}

Figure A.3.19: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{NC}; Fig. (b) FFT of i_{Ni}



(a) i_{CT} **(b)** i_{Ln}

Figure A.3.20: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{CT}; Fig.(b) FFT of i_{Ln}

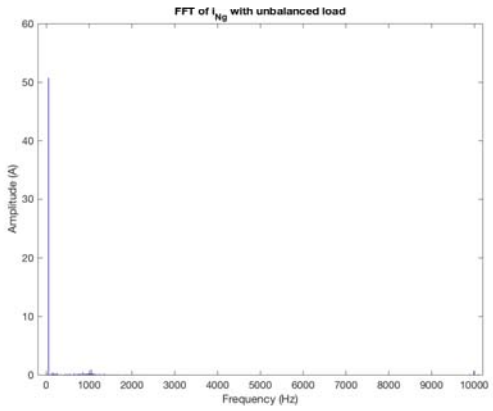


Figure A.3.21: Case 10: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of i_{Ng}

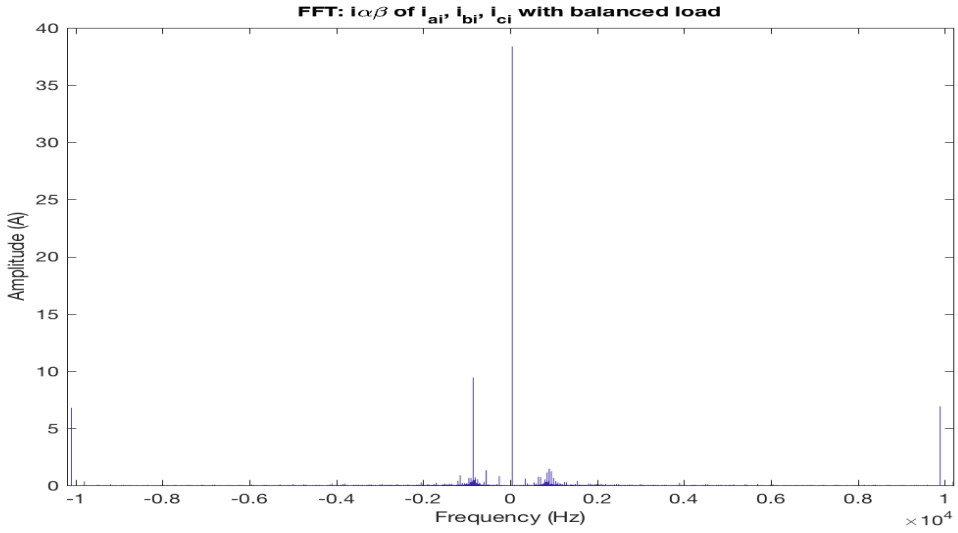


Figure A.4.1: Case 40: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter current

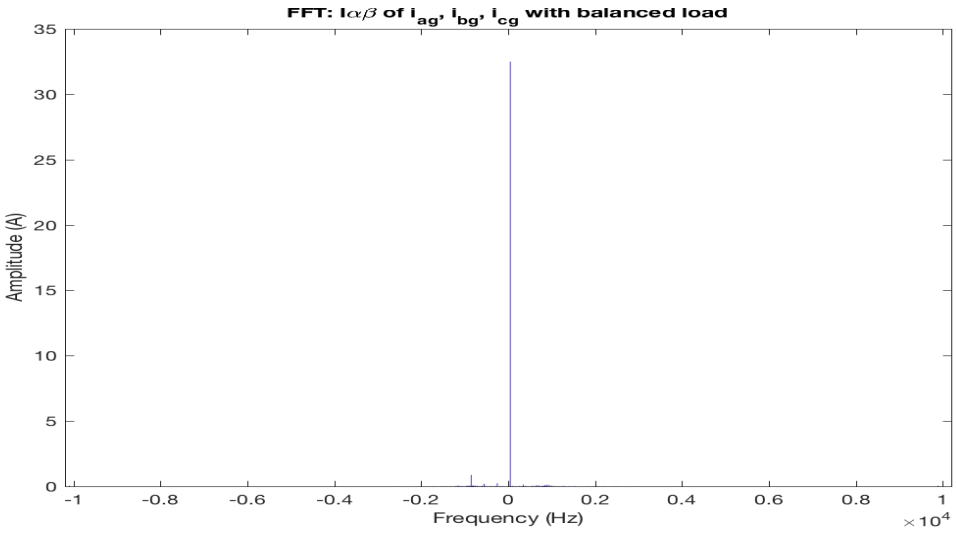
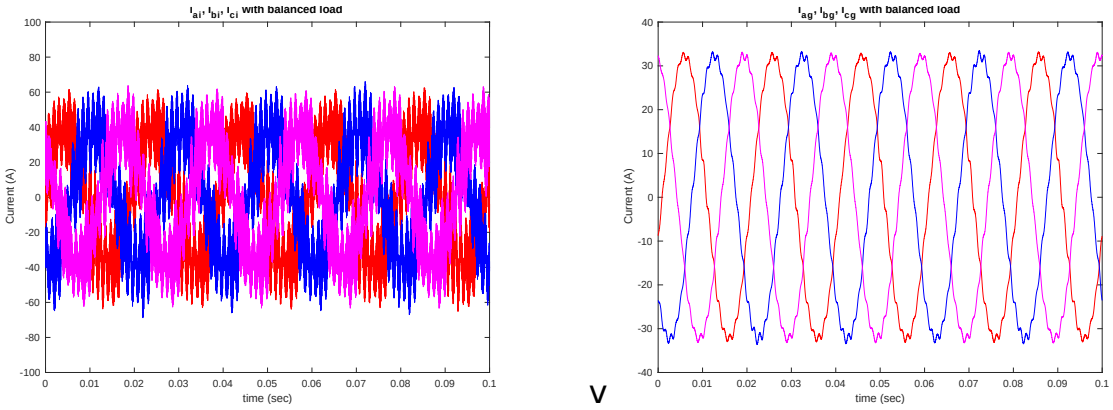


Figure A.4.2: Case 40: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid current



(a) **(b)**

Figure A.4.3: Case 40: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) waveform of inverter current; Fig. (b) waveform of grid current

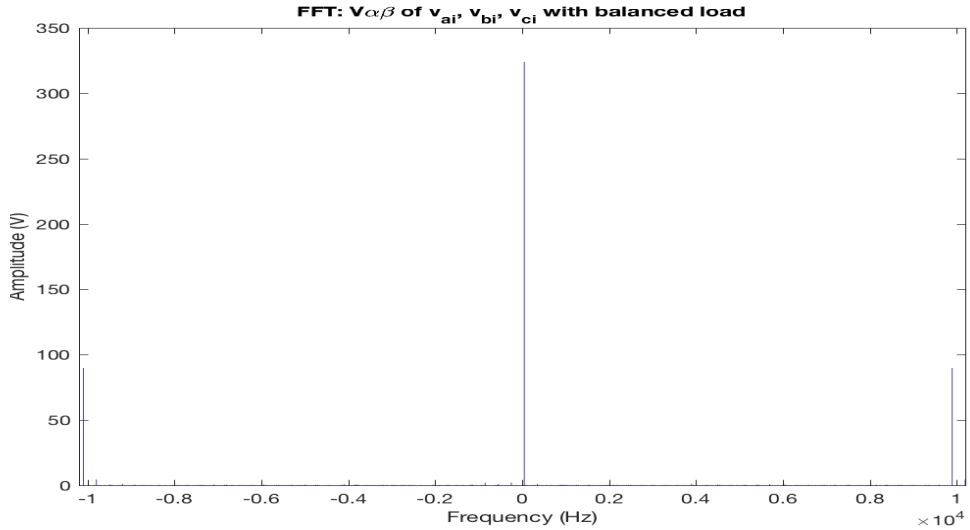


Figure A.4.4: Case 40: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter voltage

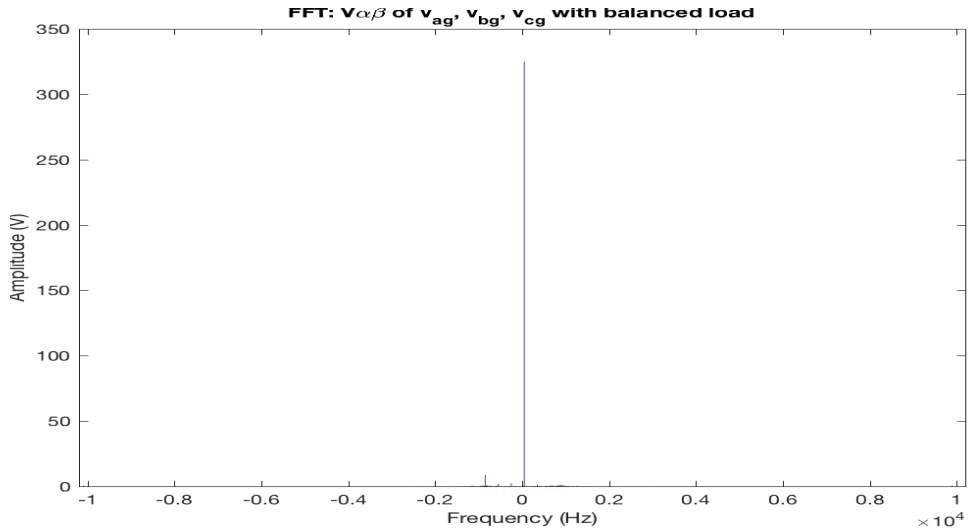


Figure A.4.5: Case 40: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid voltage

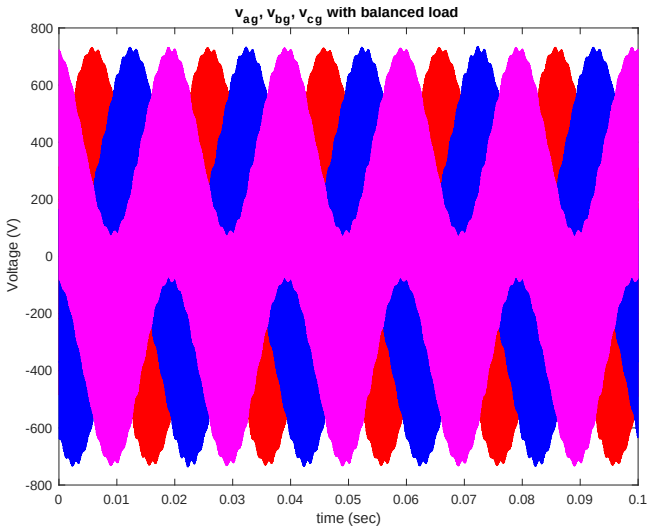


Figure A.4.6: Case 40: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Waveform of grid voltage

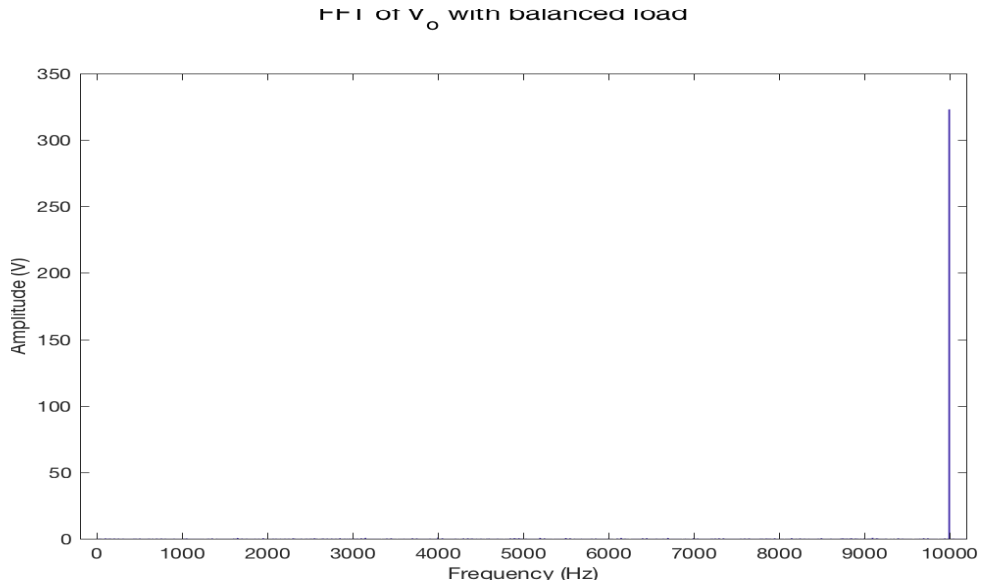


Figure A.4.7: Case 40: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of zero voltage sequence

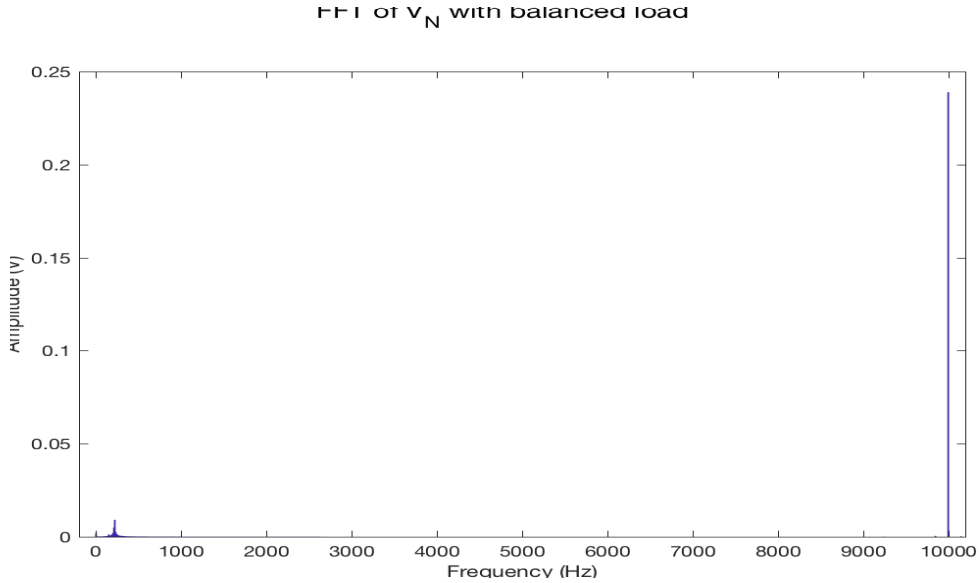
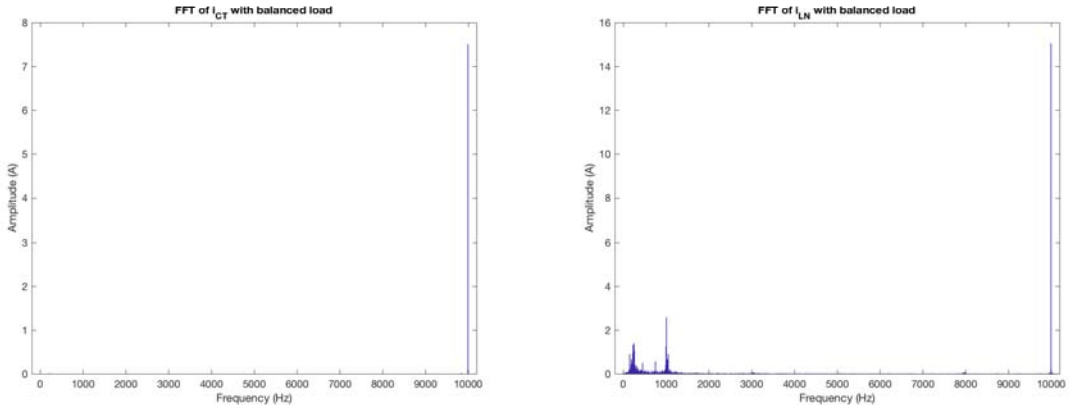


Figure A.4.8: Case 40: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of neutral voltage



(a) i_{CT} **(b)** i_{Ln}

Figure A.4.9: Case 40: *LC*-filter with balanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{CT}; Fig. (b) FFT of i_{Ln}

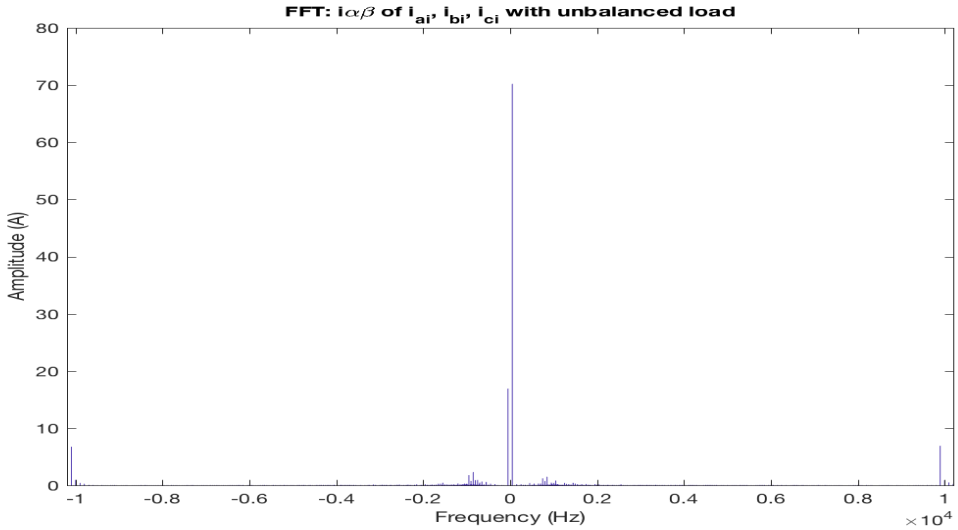


Figure A.4.10: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter current

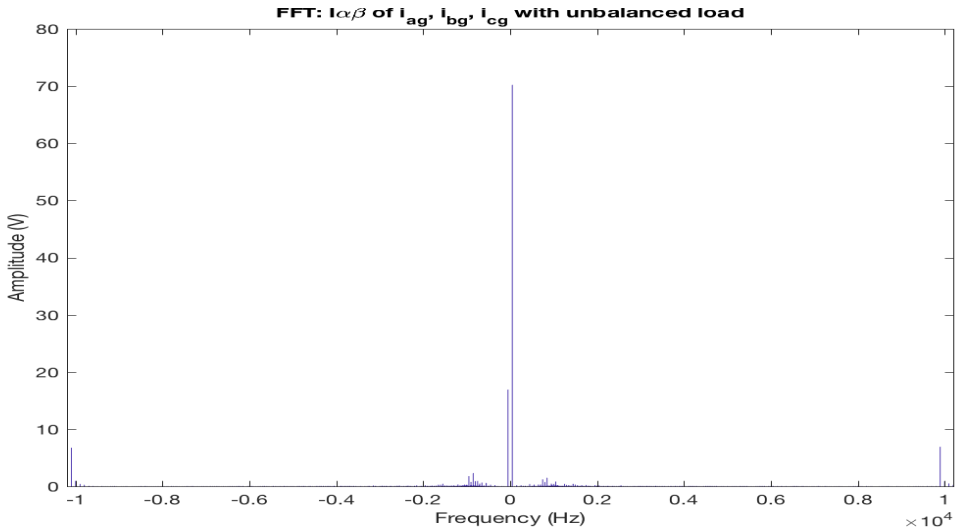
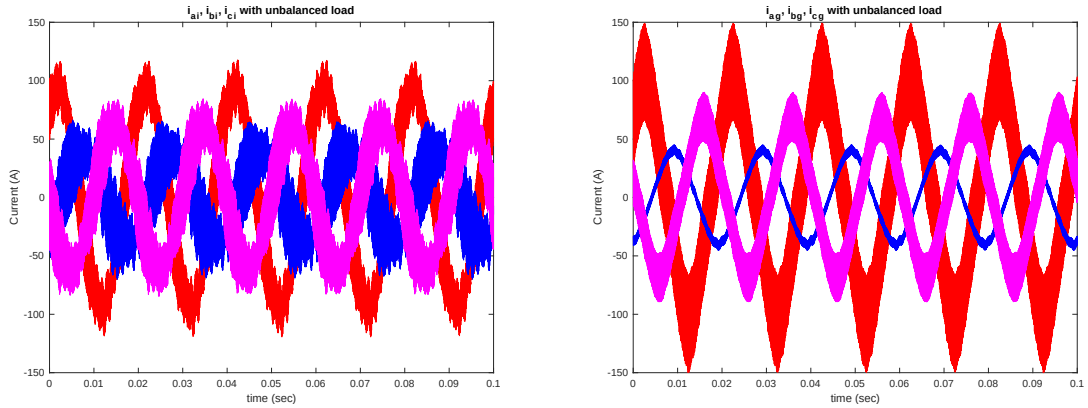


Figure A.4.11: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid current



(a) **(b)**

Figure A.4.12: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) waveform of inverter current; Fig. (b) waveform of grid current

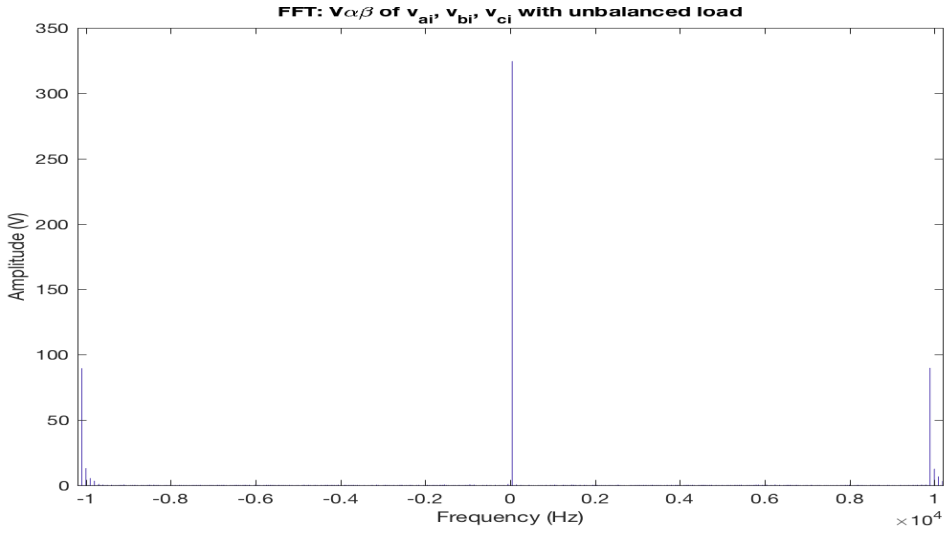


Figure A.4.13: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of inverter voltage

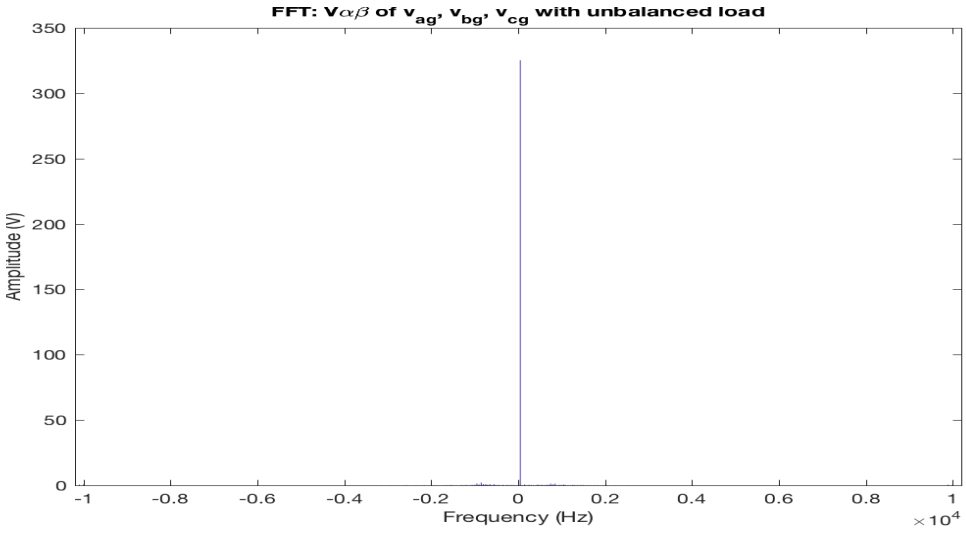


Figure A.4.14

Figure A.4.15: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of grid voltage

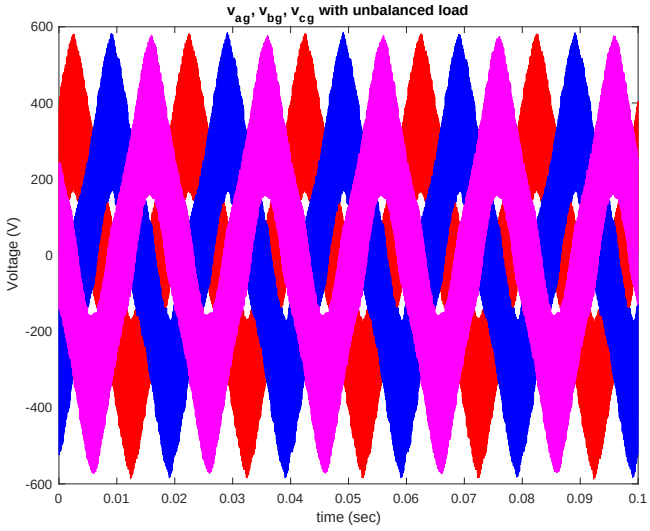


Figure A.4.16: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Waveform of grid voltage

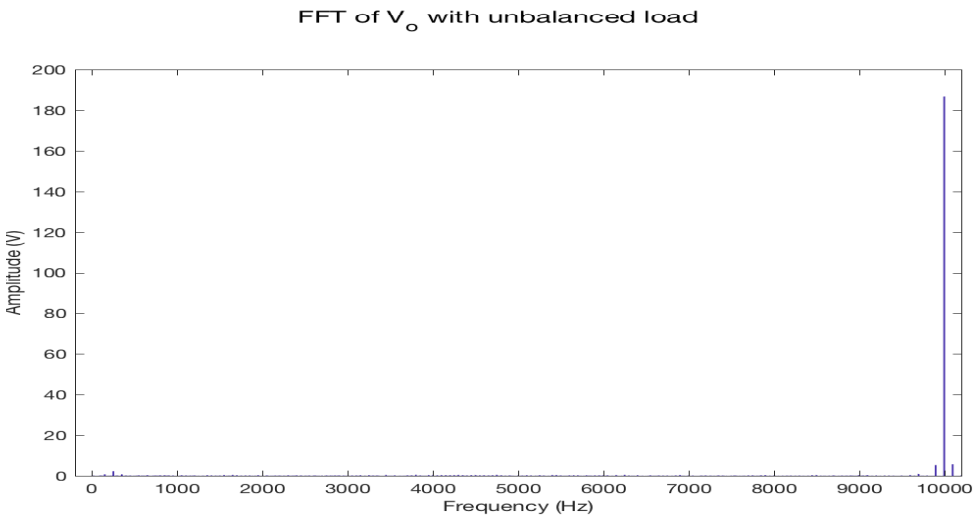


Figure A.4.17: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of zero sequence voltage

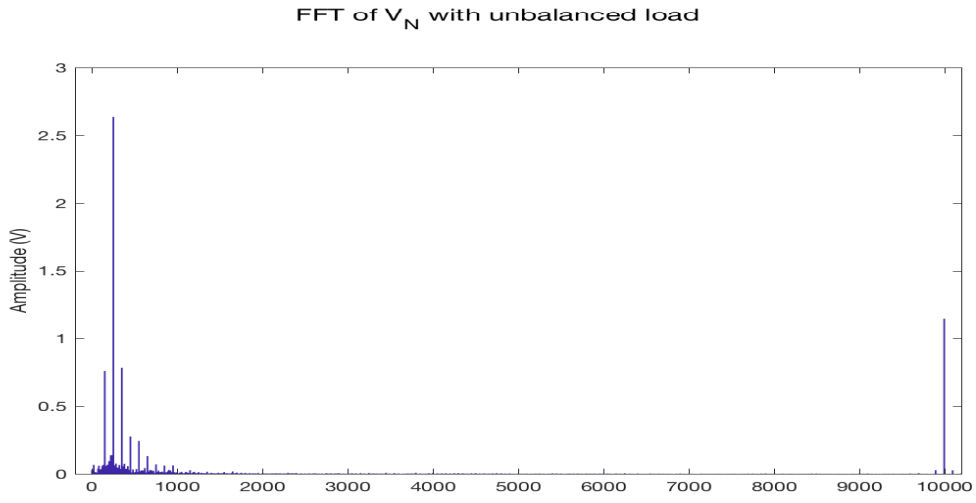


Figure A.4.18: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of neutral voltage

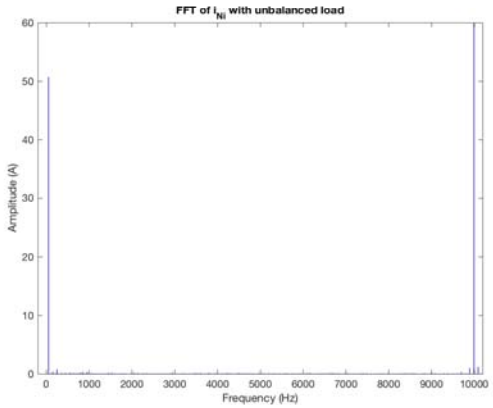
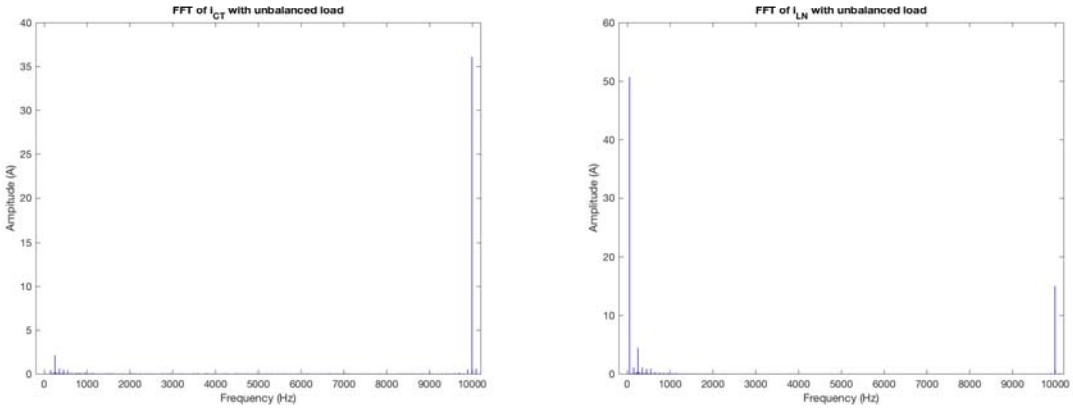


Figure A.4.19: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; FFT of i_{Ni}



(a) i_{CT} **(b)** i_{Ln}

Figure A.4.20: Case 40: *LC*-filter with unbalanced load; zero sequence voltage control: PR_v+PR_i; Fourth leg control: PR_v+PI_i; Fig. (a) FFT of i_{CT}; Fig.(b) FFT of i_{Ln}

As shown in fig. A.4.18, U_N has harmonic content and 10 kHz component. it doesn't have component at fundamental frequency thanks to the control.

Bibliography

[1] M Alsharif and Ali Omar. *Neutral point inverter controller using h infinity techniques*. PhD thesis, Universiti Tun Hussein Onn Malaysia, 2014.

[2] N Bianchi, S Bolognani, M Zigliotto, and MAZM Zordan. Innovative remedial strategies for inverter faults in ipm synchronous motor drives. *IEEE Transactions on energy conversion*, 18(2):306–314, 2003.

[3] William T Cochran, James W Cooley, David L Favin, Howard D Helms, Reginald A Kaenel, William W Lang, GC Maling, David E Nelson, Charles M Rader, and Peter D Welch. What is the fast fourier transform? *Proceedings of the IEEE*, 55(10):1664–1674, 1967.

[4] Richard C Dorf and Robert H Bishop. *Modern control systems*. Pearson, 2011.

[5] I F II. Ieee recommended practices and requirements for harmonic control in electrical power systems. 1993.

[6] Sampath Jayalath and Moin Hanif. Generalized lcl-filter design algorithm for grid-connected voltage-source inverter. *IEEE Transactions on Industrial Electronics*, 64(3):1905–1915, 2017.

[7] Meenakshi Jayaraman, VT Sreedevi, and Rajkiran Balakrishnan. Analysis and design of passive filters for power quality improvement in standalone pv systems. In *Engineering (NUiCONE), 2013 Nirma University International Conference on*, pages 1–6. IEEE, 2013.

[8] Mark McGranaghan. Active filter design and specification for control of harmonics in industrial and commercial facilities. *Knoxville TN, USA: Electrotek Concepts, Inc*, 2001.

[9] Ned Mohan and Tore M Undeland. *Power electronics: converters, applications, and design*. John Wiley & Sons, 2007.

[10] Aleksandr Reznik, Marcelo Godoy Simoes, Ahmed Al-Durra, and SM Muyeen. *lcl* filter design and performance analysis for grid-interconnected systems. *IEEE Transactions on Industry Applications*, 50(2):1225–1232, 2014.

[11] Joan Rocabert, Alvaro Luna, Frede Blaabjerg, and Pedro Rodriguez. Control of power converters in ac microgrids. *IEEE transactions on power electronics*, 27(11):4734–4749, 2012.

[12] Hong-seok Song and Kwanghee Nam. Dual current control scheme for pwm converter under unbalanced input voltage conditions. *IEEE transactions on industrial electronics*, 46(5):953–959, 1999.

[13] John Wang and Randy Hamilton. A review of negative sequence current. In *Protective Relay Engineers, 2010 63rd Annual Conference for*, pages 1–18. IEEE, 2010.

[14] Richard Zhang. High performance power converter systems for nonlinear and unbalanced load/source. *Virginia Tech*, 1998.

[15] Qing-Chang Zhong, Leslie Hobson, and Marcel G Jayne. Classical control of the neutral point in 4-wire 3-phase dc-ac converters. *Electrical Power Quality and Utilisation. Journal*, 11(2):73–81, 2005.

[16] Qing-Chang Zhong and Tomas Hornik. *Control of power inverters in renewable energy and smart grid integration*, volume 97. John Wiley & Sons, 2012.

List of Figures

List of Tables