Università degli Studi di Padova

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Tesi di Laurea in Ingegneria Elettronica

Modelling of a Buck converter with adaptive modulation and design of related driver stage

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I dedicate this work to my family and Martina

Abstract

This thesis concerns the modelling of a step-down (Buck) switching mode DCDC converter for automotive application and the design of its driver stage. The related controller accomplishes an adaptive control technique that automatically switches between peak current pulse-width modulation and constant ON-time pulse frequency modulation depending on the operative conditions of the converter.

The modelling activity provides a small signal model, derived from steady-state averaging, for all the operative regions of the converter and is supported by academic publications and by a validation through simulations in Matlab/Simulink environment. Finally, a gui tool is proposed for stability analysis and parametric optimization.

The design activity aims to build a driver stage for a given post-regulation point-of-load application, starting from efficiency considerations and gradually improving the driver with additional functions.

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Chapter 1

Infineon Switching Mode Post Regulator

This first chapter explains the functioning of a Buck power stage and shows common techniques of its control, included an innovative one that characterise an ®Infineon product that is entering the market. Some mathematical relations between electrical quantities in steady state condition are given and summarised at the end of this chapter in a graph that marks the operative conditions of the converter.

1.1 Introduction

DCDC converters are power suppliers that transform electrical energy from a continuous form into a continuous form. Since several loads require either constant voltage and variable current (e.g. uC) or vice-versa (e.g. LEDs), these converters are controlled in order to achieve voltage or current regulation respectively.

Conversion is called step-down or step-up according to whether the output voltage is lower or higher than the input voltage. In automotive sector the battery cell is the only electrical source available in a vehicle and supplies devices of different voltage classes. Step-down conversion is achievable both by linear regulators and by the Buck converter, which belongs to the switched-mode regulators family. While a linear regulator is less noisy compared to its switching counterpart, it becomes as less efficient as power losses, proportional to the input-output voltage drop, increase. Switched-mode power supplies (SMPS) are preferable whenever high voltage drop is needed, whereas linear regulators tend to be restricted on their low drop-out (LDO) version.

Buck SMPS placed right after the battery as pre-regulator appears to be an energy efficient solution to achieve a medium voltage power rail. Nowadays, Buck SMPS are replacing LDOs even for lower voltage rails because of their higher efficiency, especially when "OFF" mode is contemplated. In fact, this thesis concerns a Buck Switched-Mode Post Regulator (SMPR) supplied by an another Buck and configured to be a constant voltage - variable current power supply. However, theoretical analysis and results given are valid for the whole Buck topology, and not constrained to a particular application.

1.2 Basic functioning

A generic regulator consists of a power stage, which achieves the power conversion, and a controller, which controls the power conversion according to the power requested by the load.

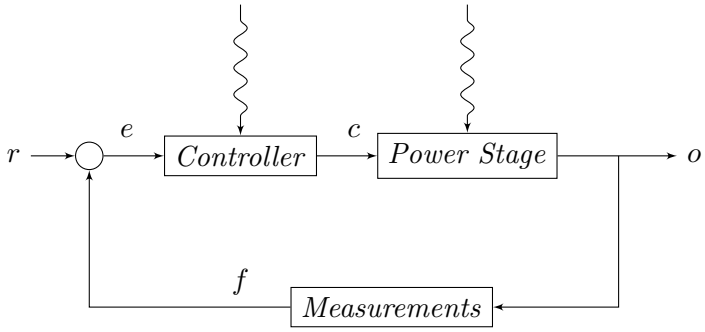


Figure 1.1: Simple and general block diagram of a converter.

A concept level architecture of voltage regulator is depicted in figure 1.1, where the Buck *power stage* is put in a closed loop with the *controller* and configured as a reference follower.

A reference r is externally generated and compared to some measurements f of the output o. The difference between r and f, called error e, is processed by the *controller* that commands, through the controlling variable c, the *power stage* in order to nullify e. The regulation is fast, precise and stable when f follows r dynamically and statically, under all sort of perturbations. In the case of switched-mode regulators, a little more in detail:

- *Power stage* basically includes a switching cell and a LC filter. Switching cell involves two switches that must be properly driven to convey power from source to load, while LC filter stores energy and soften switching frequency at the same time. Information related to energy transfer is sensed and reported to the controller in the form of *Measurements*.

- *Controller* processes information contained in *Measurements* and translates it into the duty-cycle, which is a pulsed signal that determines the phases of the switching cell and thus controls the energy transfer rate.

Before starting with mathematical results, a consideration has to be made. All the electrical signals in the loop inherit the switching frequency from the duty cycle signal. Such a frequency is due to how information is carried but does not carry information itself. Actually, in power converters significant information is energy which in DCDC converters is carried by average rather than instantaneous quantities. So, if each electrical signal $x(t)$ is averaged over its fundamental period T_s and transformed into $\bar{x}(t)$

$$x(t) \to \bar{x}(t) = \int_{t-T_s}^{t} x(\tau)\,\mathrm{d}\tau \tag{1.1}$$

switching frequency F_s is cut off whereas lower frequencies are only slightly altered by such a moving average filtering. Under the condition of periodic steady state equilibrium there is no transient and then the averaged quantity $\bar{x}(t)$ loses its dependency on time:

$$\bar{x}(t) \to \bar{x}(t) = X \tag{1.2}$$

Equivalently, in the relation:

$$x(kT_s) = x((k+1)T_s), k \in \mathbb{R} \tag{1.3}$$

k is not relevant and can be set to zero.

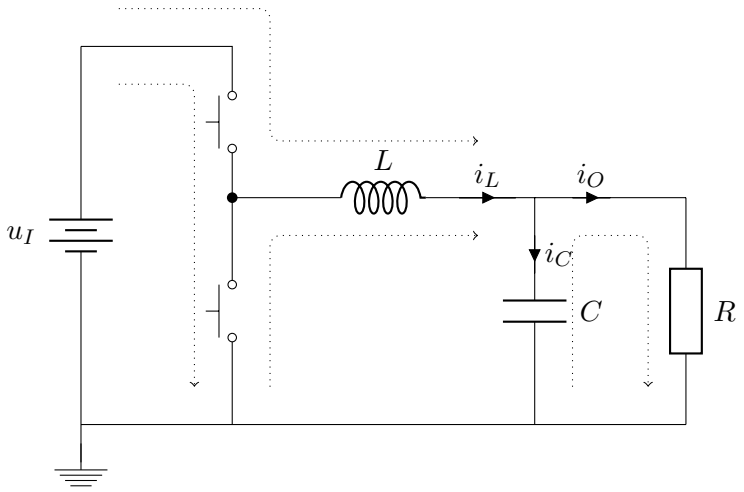


Figure 1.2: Buck power stage inspection. All devices are ideal. Current, or energy flows, are marked with dotted lines, for different phases.

In conclusion, under periodic steady state equilibrium, each signal $x(t)$ can be written as

$$x(t) = X + \tilde{x}(t) \tag{1.4}$$

where X is the average quantity while $\tilde{x}(t)$ is the static ripple that is cancelled by the averaging technique.

Note that in general

$$\overline{xy} \neq \bar{x}\bar{y} \tag{1.5}$$

but, under the hypotheses of small ripple $\tilde{x} \ll X$ the approximated relation:

$$\overline{xy} \approx \bar{x}\bar{y} \tag{1.6}$$

is valid.

1.2.1 Power stage

Depending on the state of the two switching elements, four phases are possible: *powering, free-wheeling, idling* and *shorting* (see fig. 1.2). It is clear that a synchronism is needed to avoid *shorting* as it is causes energy loss and at worst device damage. Depending on the current of the inductor, two combinations of the aforementioned phases are repeated in sequence every cycle. Continuous conduction mode (from now on, CCM) alternates *powering* and *free-wheeling* phases, while discontinuous conduction mode (DCM) alternates *powering*, *free-wheeling* and *idling* phases. A forced-CCM is also possible, which is similar to CCM mode, with the difference of allowing negative inductor current which constitutes an energy loss unless it is somehow stored in a capacitance. However only CCM and DCM are taken into account. In the following, some steady state relations are found for CCM and DCM, and in particular the conversion ratio $M := \frac{U_O}{U_I}$, where U_I and U_O are the average quantities of the input and output voltage u_I and u_O, respectively. Also, for these voltages small ripple hypotheses is valid, i.e. $\tilde{u}_I \ll U_I$, $\tilde{u}_O \ll U_O$, because battery and output voltage regulation are typically designed to achieve small ripple.

Continuous conduction mode

In CCM two phases are repeated every cycle: *powering* and *free-wheeling*. During *powering* phase, high side switch is on, low side switch is off and the inductor is connected

between battery and load. Conversely, during *free-wheeling* phase high side switch is off, low side switch is on and the inductor is connected between ground and load.

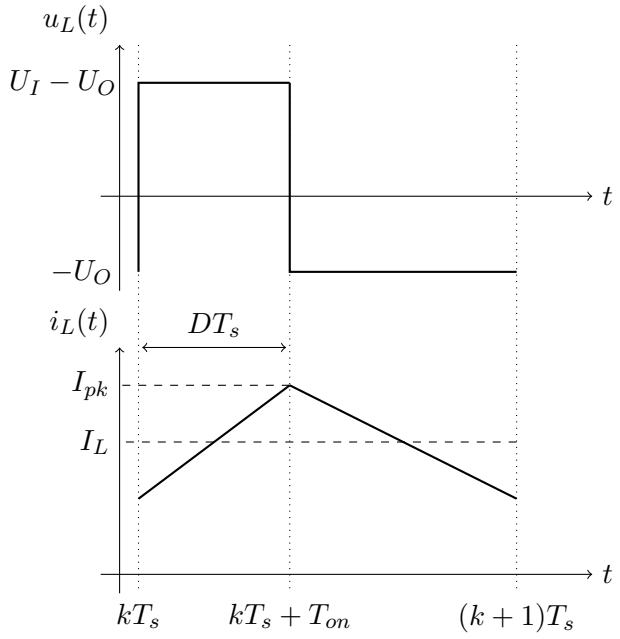


Figure 1.3: Inductor voltage and current wave during CCM operation.

Starting from the two instantaneous dynamics due to the inductance and the capacitance:

$$u_L = L\frac{di_L}{dt} \tag{1.7}$$

$$i_C = C\frac{du_O}{dt} \tag{1.8}$$

inductor current waveform is defined as

$$i_L(t) = i_L(0^-) + \int_0^t \frac{u_L(\tau)}{L}\,\mathrm{d}\tau. \tag{1.9}$$

with inductor voltage waveform:

$$u_L(t) = \begin{cases} u_I(t) - u_O(t) & \text{when } d(t) = 1 \\ -u_O(t) & \text{when } d(t) = 0 \end{cases} \tag{1.10}$$

and with duty-cycle waveform defined as:

$$d(t) = \begin{cases} 1 & \text{for } kT_s < t < kT_s + T_{on} \\ 0 & \text{for } kT_s + T_{on} < t < (k+1)T_s \end{cases}, k \in \mathbb{Z} \tag{1.11}$$

The average duty-cycle is then calculated:

$$D = \frac{T_{on}}{T_s} \tag{1.12}$$

Average capacitor current is null in periodic steady state equilibrium:

$$I_C = C\frac{dU_O}{dt} = 0 \tag{1.13}$$

so that:

$$I_L = I_O - I_C = I_O \tag{1.14}$$

As consequence,

$$U_L = \frac{dI_L}{dt} = D(U_I - U_O) + (1 - D)(-U_O) = 0 \tag{1.15}$$

Solving last equation yields:

$$M_{CCM} = D \tag{1.16}$$

This first important result states that conversion factor M is equal to duty-cycle D, so the duty-cycle regulates directly the output voltage in CCM, from zero up to input voltage value.

Discontinuous conduction mode

In DCM three phases are repeated every cycle: *powering*, *free-wheeling* and *idling*. The first two phases are the same as in CCM, while in *idling* phase both switches are off and the current and the voltage of the inductor are null.

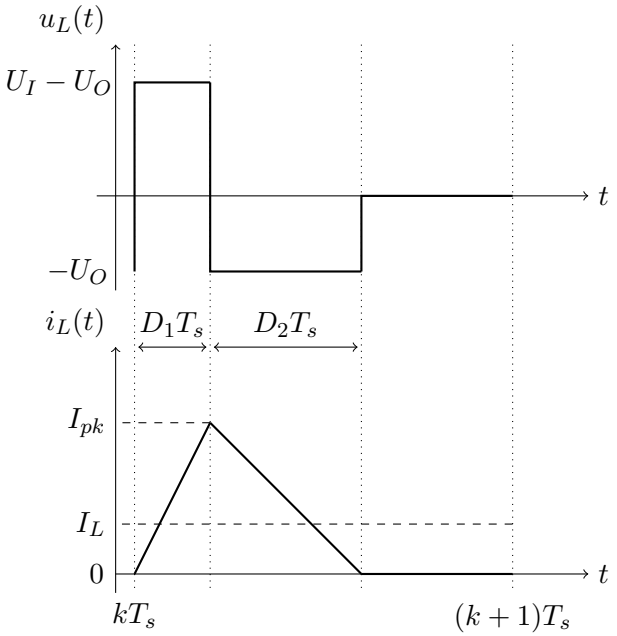


Figure 1.4: Inductor voltage and current waves during DCM operation.

The condition of equilibrium imposes:

$$U_L = (U_I - U_O) \cdot D_1 - U_O \cdot D_2 = 0 \tag{1.17}$$

By equating the area of the rectangle subtended by I_L and the area of the triangle subtended by i_L during the interval T_s in figure 1.4:

$$I_L \cdot T_s = \frac{1}{2} I_{pk}(D_1 + D_2)T_s \tag{1.18}$$

Reminding that

$$I_{pk} = i_L(kT_s + T_{on}) = \frac{U_I - U_O}{L} DT_s \tag{1.19}$$

and that, for Kirkhoff's law,

$$I_L = I_O - I_C = I_O \tag{1.20}$$

and combining 1.17 and 1.18 gives:

$$M_{DCM} = \frac{D^2}{D^2 - I_O 2LF_s/U_I} \tag{1.21}$$

This result states that conversion ratio in DCM, unlike CCM, depends also on the load.

Defining , $I_N = \frac{U_I}{2LF_s}$, 1.21 is simplified into:

$$M_{DCM} = \frac{D^2}{D^2 - I_O/I_N} \tag{1.22}$$

1.2.2 Controller features

Controller primary role is to produce a duty-cycle that commands the switching cell of the Buck power stage. Regulation error is translated into the duty-cycle by means of a modulation, which in this case is also a 1 bit AD conversion. Many types of digital modulation exist but they all basically intervene in the width or in the frequency of the digital pulses. For example, pulse density modulation involves a mixture of frequency and width modulation, with the advantage of distributing spectral power versus time and mitigating electromagnetic emissions. Pure pulse-width modulation (PWM) is more common because it requires a simple architecture and switching frequency is a known parameter. On the other side pure pulse-frequency modulation (PFM) is far more efficient at light load. Indeed Infineon SMPR uses an architecture that switches dynamically between PWM and PFM according to the power request, which is optimal in applications where energy efficiency is critical. For example, in automotive sector certain devices are working even when the vehicle is stopped and battery is not rechargeable. Finally, albeit only a voltage control is needed to regulate the load voltage to a given reference, also a current control is beneficial and sometimes introduced, or introduced and sometimes activated as in the case of Infineon SMPR. The system is said to be in *current mode* or in *voltage mode* whether the current loop is active or not, respectively.

Pulse Width Modulation

PWM involves a constant frequency, which is typically set to high values because filter size and cost decrease. A simple architecture of *voltage mode* control performing PWM is shown in fig. 1.5.

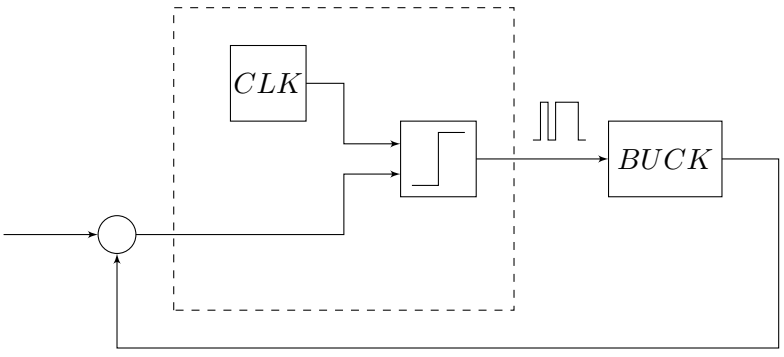


Figure 1.5: Inspection on controller generating duty-cycle

Basically an internal clock produces a ramp with reference frequency whereas a comparator sets the width of the duty-cycle according to whether the regulation error stays either over or below that ramp.

Peak Current Mode

In addition to *voltage mode* control sometimes also *current mode* is introduced because it offers some benefits:

- Softened stimuli response
- Easier loop compensation
- Better robustness against battery variation

Indeed when current control is active, the inductor behaves like a current generator and loses its natural dynamic, similarly to what happens in DCM. As consequences, LC natural filter resonance is damped, frequency compensation design becomes easier and the battery variation is rejected, while in *voltage mode* it has a direct impact on the output voltage. All these features are proved in chapter 3. Two types of current controls are commonly used: peak current mode (PCM) and average current mode. PCM brings all the current control advantages in voltage regulators and is indeed present in the Infineon SMPR. A basic PCM architecture is depicted in fig. 1.6

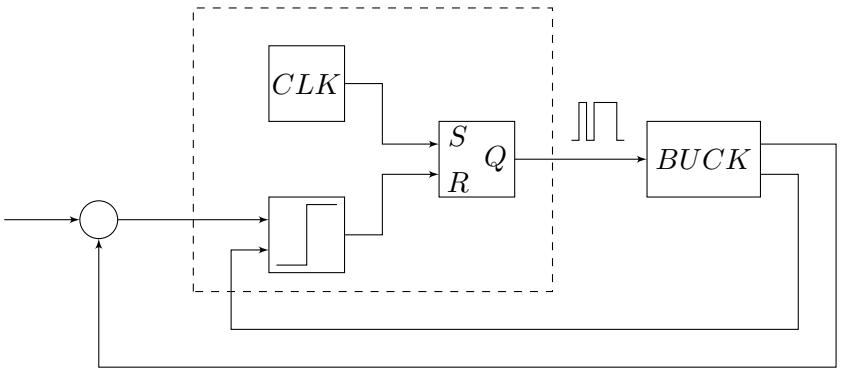


Figure 1.6: Peak current mode architecture, performing PWM by means of a S/R latch.

Basically for duty-cycle generation the SET is given by an internal clock, while the RESET is given by the comparison between the regulation error with the sensed current. In this manner the inductor current is supposed to stay always below the regulation error. In total there are two "reference follower" configurations nested to one another.

Pulse Frequency Modulation

High frequency is proved to achieve good efficiency at heavy load operation. Instead, at light load, reducing frequency F_s and thus frequency-dependent power losses, indicated as $P_{LOSS} \propto F_s$, increases efficiency η as suggested by equation 1.23:

$$\eta = \frac{P_O}{\underbrace{P_O + P_Q + P_{COND} + \underbrace{P_{DRV} + P_{SW}}_{\propto F_s}}_{P_{\text{LOSS}}}} \tag{1.23}$$

PFM is achieved by putting a Voltage-Controlled Oscillator (VCO) in the voltage loop as in fig. 1.7

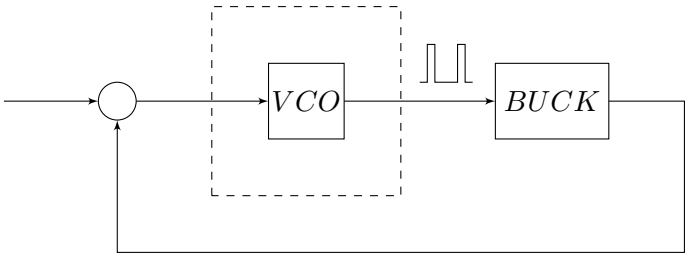


Figure 1.7: Voltage mode architecture, performing PFM by means of a voltage controlled oscillator.

Provided that such VCO produces pulses with fixed width, the frequency of the pulses and thus duty-cycle varies according to the controlling variable of the VCO, i.e. the regulation error.

Adaptive PWM/PFM

The preliminary consideration to be done is that a minimum duty-cycle D_{min} inherently exists in PWM functioning for two main reasons. First, because in PCM a blanking on time is introduced to mask the glitches on the transient of the current reconstruction. Second, because the turning on of the high-side switch requires a minimum on time T_{onMIN} to be effective, i.e. to allow power flow.

By the presence of D_{min}, output voltage increases - and thus regulation error decreases - when the duty-cycle exceeds the amount requested by the loop. In such situation, a switch to PFM seems to be convenient to achieve duty-cycle inferior than D_{min}, keeping a constant on time T_{onPFM} and increasing T_s.

The functioning principle of an adaptive modulation technique proposed and patented by Infineon is shown in fig. 1.8.

Basically, the clock is substituted by a controllable one, a VCO. When varying frequency, VCO is controlled by regulation error, otherwise, when saturated, it becomes an autonomous clock. Therefore, the switching from PWM to PFM is triggered when such VCO enter or leaves its saturation region, delimited by a threshold value called VCO_{th}.

An architecture that implements adaptive modulation is shown in fig. 1.9. Basically a controllable clock (VCO), inspected in fig. 1.10 gives a S=CLK to the S/R latch that generates the duty-cycle. CLK is also generated in turn by an S/R, internal to the VCO.

CLK set is generated when:

$$\frac{1}{T_{VCO}} \int_{t-T_{off}}^{t} error = V_{VCO} \tag{1.24}$$

CLK reset is generated after a fixed $T_{onMIN} := T_{onPFM}$.

Notice that also a T_{offMIN} is generated in order to achieve the saturation of VCO:

$$T_{sPWM} = T_{offMIN} + T_{onMIN} \tag{1.25}$$

In saturation zone, VCO produces a constant frequency S=CLK and normal PWM is active (reset R comes from PCM comparator).

In variability zone, VCO variates frequency of S but keeps its width constant and equal to T_{onPFM}. At this point S/R latch, which is S dominant, neglects R, so that Q=S, and achieves PFM.

Main waveforms related to CLK generation are shown in graph 1.11.

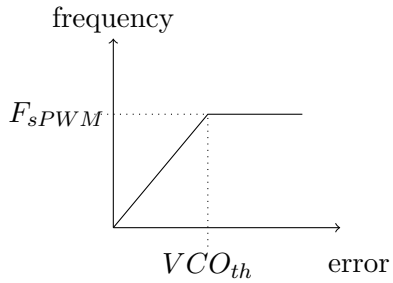


Figure 1.8: VCO charachteristics which underlies the concept of an adaptive modulation.

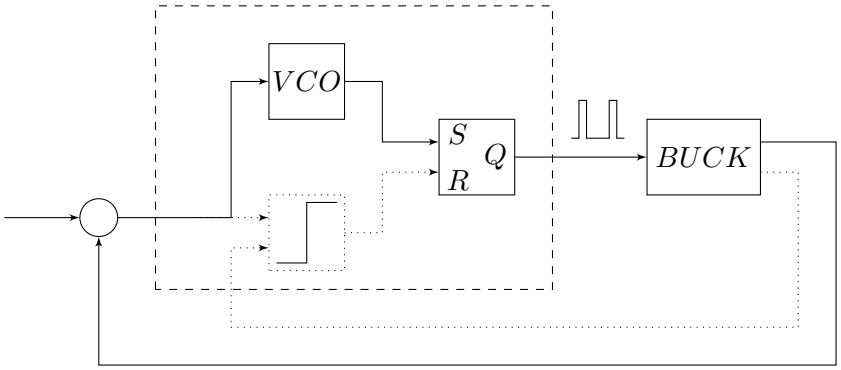


Figure 1.9: Infineon concept architecture. When PFM is activated, some circuitry is bypassed and can be disabled.

1.3 Resulting operative map

The substantial difference between PWM and PFM has been shown to reside in how the *duty-cycle* is modulated: keeping frequency constant and making T_{off} time (or, equivalently, T_{on} time) variable or vice versa. So, it is convenient to discriminate duty-cycle according to the two modulation types.

For PWM:

$$D_{PWM} := \frac{T_{on}}{T_{sPWM}} \tag{1.26}$$

and for PFM:

$$D_{PFM} := \frac{T_{onPFM}}{T_s} \tag{1.27}$$

Boundary equation that separates CCM and DCM regions, under PWM, is found by equating eq. 1.16 and 1.21 and combining with 1.27 :

$$I_O = \frac{U_O}{U_I}\left(\frac{U_I - U_O}{2LF_s}\right) \tag{A}$$

Boundary equation that separates CCM and DCM regions, under PFM, is found by equating eq. 1.16 and 1.21 and combining with 1.27:

$$I_O = \frac{U_I - U_O}{2L} T_{onPFM} \tag{B}$$

Boundary equation that separates PWM and PFM regions, under DCM, is found by equating the different duty-cycle definitions expressed in 1.26 and 1.27 and combining with 1.16:

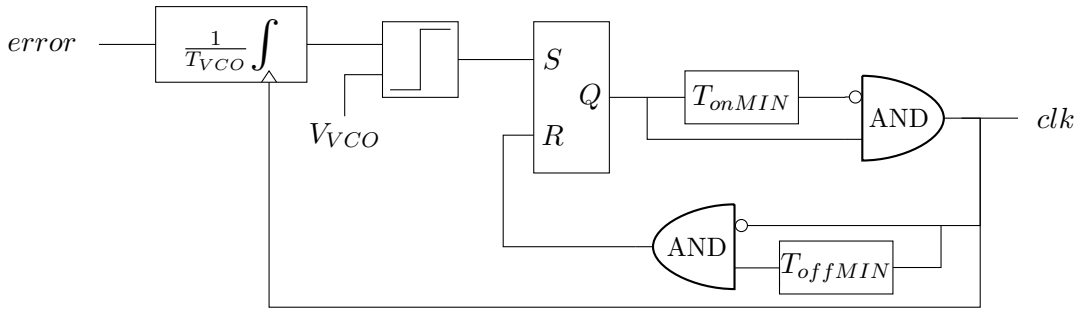


Figure 1.10: VCO clock generation concept architecture patented by Infineon

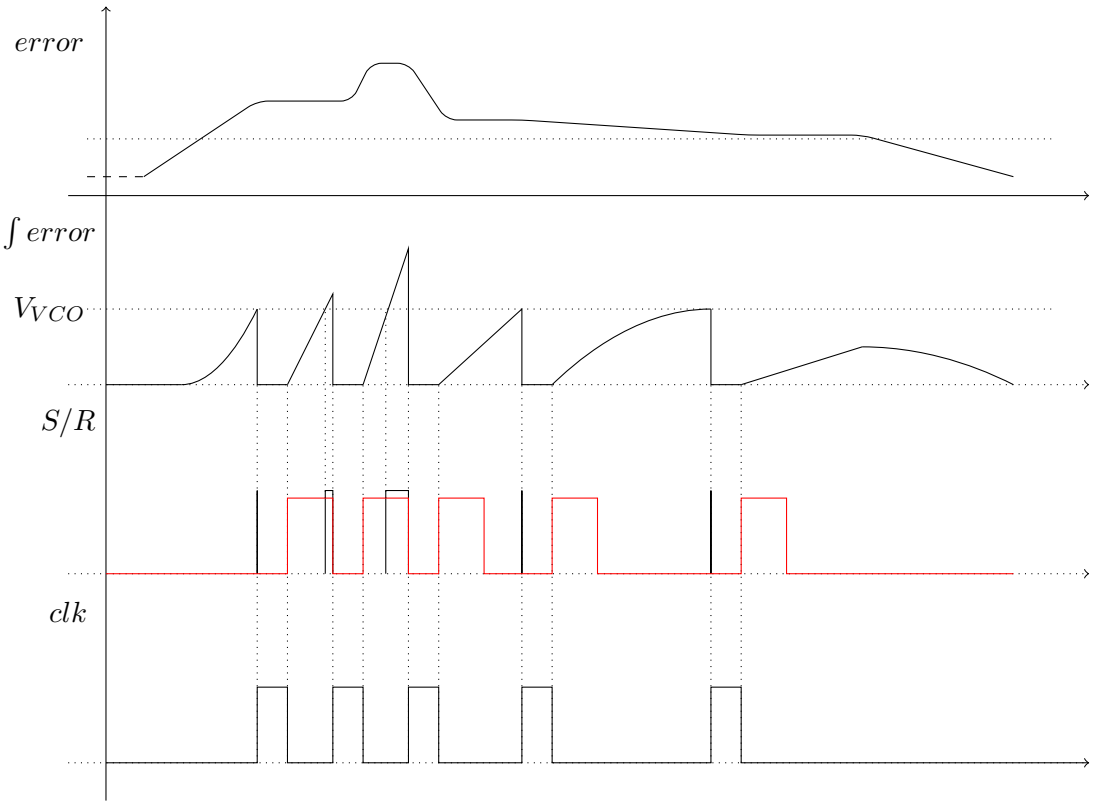


Figure 1.11: VCO clock waveforms.

$$I_O = \frac{U_I - U_O}{2L} \frac{U_I}{U_O} \frac{{T_{onPFM}}^2}{T_{sPWM}} \tag{C}$$

Boundary equation that separates PWM and PFM regions, under CCM, is found by equating the different duty-cycle definitions expressed in 1.26 and 1.27 and combining with 1.16:

$$U_I = U_O \frac{T_{sPWM}}{T_{onPFM}} \tag{D}$$

All the boundary equations are plot in a U_I-I_O graph (fig. 1.3). They delimit four operative regions, overall produced by the combination of the two operative regions of the power stage (CCM/DCM) and the types of modulations (PWM/PFM).

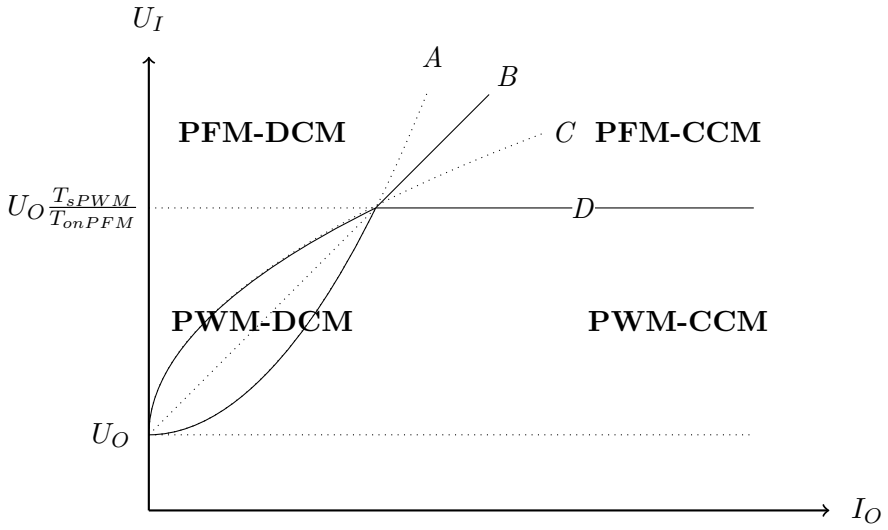


Figure 1.12: Operative map of the SMPR. Each boundary is determined by the correspondent equation and marked with dotted lines. Actual boundaries that delimit the operative regions are marked with solid lines.

Chapter 2

Modelling

Literature provides very rich documentation about the modelling of Buck converters and similar topologies (Boost, Buck-Boost). Accurate models for standalone power stages and for several controls have been conceived and validated, using different approaches and methods. As far as constant-frequency peak-current-mode control is concerned, one of the most popular model and widely used for system design is given by Ridley and his community. Following his guidelines [1, 2, 3, 5, 6], the Infineon SMPR that was presented in the previous chapter is about to be modelled. As a reminder, the SMPR basically admits CCM/DCM in its power stage, and an adaptive feedback control which selects between PCM combined to PWM and voltage mode combined to PFM with constant ON-time. The purpose of this chapter is to establish cause-effect relations between quantities involved in the dynamic system represented by the SMPR. With the usage of Laplace transformations, such relations are in the form of transfer functions that will be translated into the more appealing frequency and time domain in the next chapter.

2.1 Methods

Averaging technique

Averaging technique introduced in the previous chapter is explained again for convenience. Each signal $x(t)$ has the switching frequency F_s in its harmonic content due to the duty-cycle, which is a digital signal. Since F_s does not carry significant information, it is eliminated by means of a moving average filtering applied to each signal $x(t)$:

$$x(t) \to \bar{x}(t) = \int_{t-T_s}^{t} x(\tau)\,\mathrm{d}\tau \tag{2.1}$$

The new signal $\bar{x}(t)$ shares the same harmonic content of $x(t)$ for frequencies lower than F_s. The averaging method that leads to the average model consists of substituting each signal $x(t)$ with its averaged version $\bar{x}(t)$. The advantage is that the periodic steady state equilibrium becomes a steady state one and classic linearisation is applicable. The drawback is the loss of accuracy at frequencies next to and higher than F_s, but since the LC filter is designed to cut them off, such inaccuracy can be neglected.

Linearisation

Linearisation allows to split $\bar{x}$ into X, a state of equilibrium, and into $\hat{x}$, which is a small perturbation signal.

$$\bar{x}(t) \to \bar{x}(t) = X + \hat{x}(t) \tag{2.2}$$

Given the above equation, $\hat{x}(t)$ becomes the fundamental element of the linear small signal model and it is supposed to emulate the average dynamics of the instantaneous counterpart $x(t)$. On the contrary, X becomes a new parameter.

Note that

$$\bar{x}\bar{y} \to (X + \hat{x})(Y + \hat{y}) = XY + \hat{x}Y + X\hat{y} + \hat{x}\hat{y} \approx XY + \hat{x}Y + X\hat{y} \tag{2.3}$$

where the last term $\hat{x}\hat{y}$ is neglected because of the small signal hypotheses.

2.2 Power stage modelling

The previous chapter has shown the relations between the quantities of the power stage. In particular the outputs u_O and i_L are both functions of u_I and d, that are respectively the supply and the controlling input. Another input quantity, i_O, is introduced because it represents the power requested by the load. These $2 \times 3 = 6$ quantities are taken in their small signal form and put in a block diagram with proper connections:

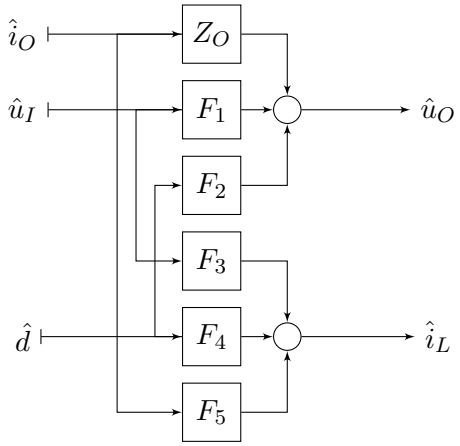


Figure 2.1: Power stage block diagram in open loop

Aim of this section is to find the transfer function contained in each block. The only non-linear device in the power stage is the switching cell, and it has to be linearised in both CCM and DCM operation.

2.2.1 CCM

The switching cell can be modelled as a two input - two output electrical port:

$$\begin{cases} u_1(t) = u_I(t) \\ i_1(t) = \begin{cases} i_L(t) & \text{when } d(t) = 1 \\ 0 & \text{when } d(t) = 0 \end{cases} \\ u_2(t) = \begin{cases} u_I(t) & \text{when } d(t) = 1 \\ 0 & \text{when } d(t) = 0 \end{cases} \\ i_2(t) = i_L(t) \end{cases} \tag{2.4}$$

Averaging the equations, the system 2.4 becomes:

$$\begin{cases} \bar{u}_1 = \bar{u}_I \\ \bar{i}_1 = \bar{d}\bar{i}_L \\ \bar{u}_2 = \bar{d}\bar{u}_I \\ \bar{i}_2 = \bar{i}_L \end{cases} \tag{2.5}$$

Time dependencies are not showed for simplicity. Note also that the two last equations of 2.5 are approximated, since $\overline{xy} \approx \bar{x}\bar{y}$ only under the hypotheses of low ripple (eq. 1.6).

Note that u_I is averaged into $\bar{u}_I$ even if it is independent from duty-cycle and, in principle, should not suffer directly from F_s.

Once averaged, the non-linear switching cell becomes a linear transformer with $\bar{d}$ as conversion ratio.

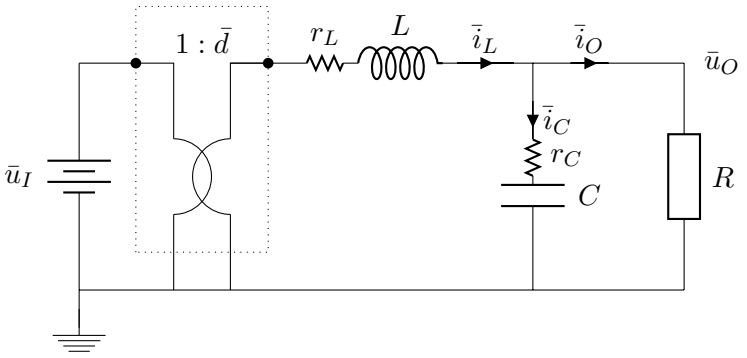


Figure 2.2: Averaged linear model of Buck power stage

The resulting fully linear model is depicted in fig. 2.2. Note that the transformer feeds a lossy 2nd order filter, which is in turn the modelling of the physical RLC filter applied to the Buck. However, it can be demonstrated that also for Boost and Buck-Boost the CCM model aspect is the same, that is a transformer plus a 2nd order filter, even if the RLC filter is not physically explicit in those topologies. For this reason, such model is said to be in a canonical form, with differentiated parameters according to the topology considered.

At this point all transfer functions Z_O, $F_{1,..,5}$ can be found. For example, once denoting the 2nd order filter transfer function as H_{RLC} it can be written that:

$$\bar{u}_O = \bar{d}\bar{u}_I \cdot H_{RLC} \tag{2.6}$$

At this point F_2 is easily obtained linearising and nullifying other inputs:

$$F_2 := \left.\frac{\hat{u}_O}{\hat{d}}\right|_{\hat{u}_I, \hat{i}_O = 0} = U_I \cdot H_{RLC} \tag{2.7}$$

Other transfer functions are reported in table 2.1. Note that to find Z_O, the load R of fig. 2.2 has to be substituted by a current generator that absorbs a small perturbation $\hat{i}_O$ at the output.

2.2.2 DCM

A special observation concerning the inductor effect in DCM is required. Provided that operative mode remains DCM before and after a perturbation, the inductor current comes to zero before the end of each cycle. The inductor shows a lack of memory and thus the current is not a state variable. In other words, the inductor acts like a controlled

current generator rather than an integrating impedance. So, the assumption $U_L = 0$ made in the previous chapter can be extended to $\bar{u}_L = 0$ and can simplify the model, eliminating the inductor dynamics after substituting it with a current generator. It can be demonstrated that such an approximation cannot predict current behaviour at high frequencies so, for the sake of completeness of analysis, a more precise second order model that takes inductor dynamics into account also for DCM has to be found. In the following, r_L is neglected to simplify analysis and spare calculations.

Averaged equations related to DCM are the averaged versions of the average eq. 1.17 and eq. 1.18.

$$\begin{cases} \bar{u}_L = (\bar{u}_I - \bar{u}_O)\bar{d}_1 - \bar{u}_O\bar{d}_2 \\ \bar{i}_L = \frac{1}{2}\bar{i}_{Lpk}(\bar{d}_1 + \bar{d}_2) \end{cases} \tag{2.8}$$

Note that $i_{Lpk}(t)$ is a sampled version of $i_L(t)$ but it can be averaged into $\bar{i}_{Lpk}$ nevertheless:

$$\bar{i}_{Lpk} = \frac{\bar{u}_I - \bar{u}_O}{2LF_s}\bar{d}_1 \tag{2.9}$$

The second equation of 2.8 can be rewritten accordingly:

$$\bar{i}_L = \frac{\bar{u}_I - \bar{u}_O}{2LF_s}\bar{d}_1(\bar{d}_1 + \bar{d}_2) \tag{2.10}$$

Substituting $\bar{d}_2$ found in the above equation, the first of 2.8 can be rewritten as:

$$\bar{u}_L = \bar{u}_I\bar{d}_1 - \frac{\bar{u}_O}{\bar{u}_I - \bar{u}_O}\frac{2LF_s\bar{i}_L}{\bar{d}_1} \tag{2.11}$$

Finally inductor and capacitor dynamics are introduced, in Laplace domain form ($D := D_1$):

$$\begin{cases} sL\bar{i}_L = \bar{u}_L \\ \dfrac{sC}{1 + sr_CC}\bar{u}_O = \bar{i}_C = \bar{i}_L - \dfrac{\bar{u}_O}{R} \end{cases} \tag{2.12}$$

$$\begin{cases} I_L = \dfrac{U_I}{2LF_s}\dfrac{D^2(1-M)}{M} \\ I_L = I_o \end{cases} \tag{2.13}$$

$$\begin{cases} sL\hat{i}_L = D\dfrac{2-M}{1-M}\hat{u}_I + 2U_I\hat{d} - \dfrac{D}{M(1-M)}\hat{u}_o - \dfrac{M}{1-M}\dfrac{2LF_s}{D}\hat{i}_L \\ \hat{i}_L = \dfrac{1 + s(R + r_c)C}{1 + sr_cC}\dfrac{\hat{u}_o}{R} \end{cases} \tag{2.14}$$

Results expressed in (2.13) match with those found in the previous chapter. What is new is the equations system (2.14) which has to be solved in order to find $F_{1,..,5}$. To find Z_O, the last equation of system (2.14) has to be substituted with:

$$\hat{i}_L = \frac{1 + s(R + r_c)C}{1 + sr_cC}\frac{\hat{u}_o}{R} + \hat{i}_O \tag{2.15}$$

Table 2.1: Buck power stage transfer functions in CCM-DCM

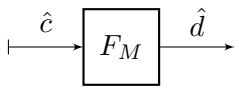
NAME	CCM	DCM
F_1	$D\frac{1+sr_cC}{\Delta(s)}$	$M\frac{1+sr_cC}{\Delta_1(s)}$
F_2	$U_I\frac{1+sr_cC}{\Delta(s)}$	$\frac{2U_o}{D}\frac{1-M}{2-M}\frac{1+sr_cC}{\Delta_1(s)}$
F_3	$\frac{D}{R}\frac{1+sRC}{\Delta(s)}$	$\frac{M}{R}\frac{1+s(R+r_c)C}{\Delta_1(s)}$
F_4	$\frac{U_I}{R}\frac{1+sRC}{\Delta(s)}$	$\frac{2I_o}{D}\frac{1-M}{2-M}\frac{1+s(R+r_c)C}{\Delta_1(s)}$
F_5	$\frac{r_L}{R}\frac{(1+sRC)(1+sL/r_L)}{\Delta(s)}-1$	$\frac{(1+sr_cC)}{\Delta_2(s)}$
Z_O	$r_L\frac{(1+sr_cC)(1+sL/r_L)}{\Delta(s)}$	$R(1-M)\frac{(1+sr_cC)\left(1+s\frac{L}{R}\frac{M}{D}\right)}{\Delta_2(s)}$
D	M	$M\sqrt{\frac{2LF_s}{R(1-M)}}$
$\Delta(s)$	$1+s\left(\frac{L}{R}+(r_c+r_L)C\right)+s^2LC$	
$\Delta_1(s)$	$1+s\left(\frac{L}{R}\frac{M}{D}\frac{1-M}{2-M}+RC\frac{1-M}{2-M}+r_cC\right)+s^2LC\frac{R+r_c}{R}\frac{M}{D}\frac{1-M}{2-M}$	
$\Delta_2(s)$	$1+s\left(r_cC+RC(1-M)\right)+s^2LC\frac{M(1-M)}{D}$	

2.3 Controller modelling

Albeit controller functionalities are numerous, the only one of interest for the model is the duty cycle generation. As anticipated, duty-cycle generation involves either a peak current detector or T_{ON} constant generator, both acting as modulators of the power request. These mechanisms that respectively intervene in the converter *control* or *voltage* mode, are about to be modelled in order to achieve a complete linear model of the SMPR system.

2.3.1 PWM - PCM Modulator

Modulators converts the controlling variable c into the duty cycle d.



Perturbing the control variable, geometrical considerations made on figure 2.4 lead to:

$$\hat{c} = (S_n + S_e)\hat{d}T_s \tag{2.16}$$

that is independent from the average current and thus is valid both in CCM and DCM. As a result:

$$F_M = \frac{\hat{d}}{\hat{c}} = \frac{1}{(S_n + S_e)T_s} \tag{2.17}$$

Another approach to find F_M starts from the averaged quantities relation:

$$\bar{c} = \bar{i}_L + \left(\frac{S_n}{2} + S_e\right)\bar{d}T_s \tag{2.18}$$

that through linearisation and subsequent superposition principle leads to:

$$F_M = \frac{\hat{d}}{\hat{c}} = \frac{2}{(S_n + 2S_e)T_s} \tag{2.19}$$

which is a different result also found in literature [1], but valid only in CCM.

2.3.2 PCM sampling action

Too see the effect of the PCM on the inductor current, the current loop is closed as in figure 2.3. PCM architecture is constructed to produce a PWM signal, so F_M is the one defined in 2.17.

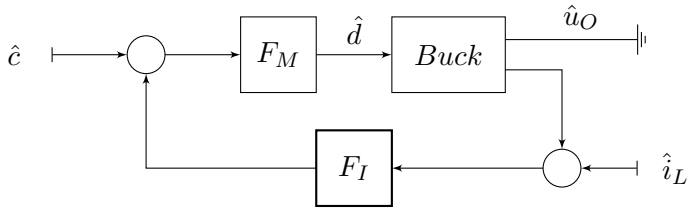


Figure 2.3: Blocks connection to find F_I that models PCM sampling action

- **CCM**

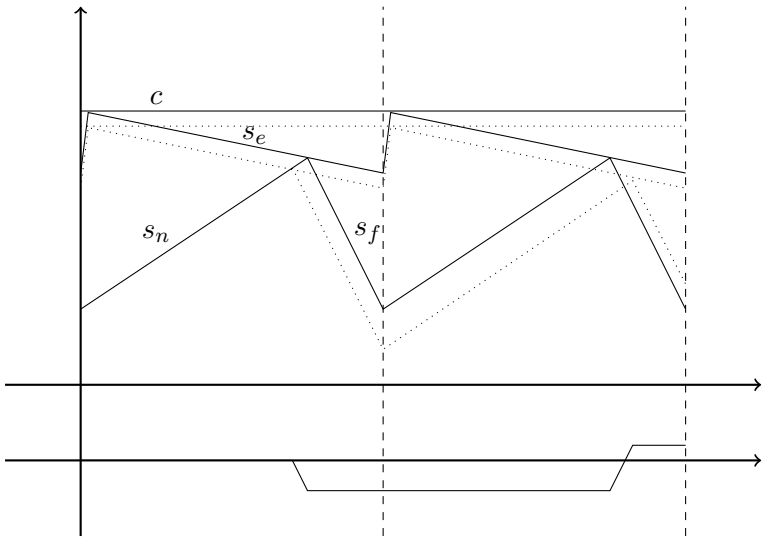


Figure 2.4: Natural response of the current error versus time during CCM operation, generated when either control or current itself is perturbed. From this waveform a sampled-data model can be found that predicts the effect of the peak detection on the averaged current dynamics, including sub-harmonic oscillations.

Be K_I the pure gain term of the current sensing F_I. The aim of this paragraph is to model the phase term H_I. Be S_n the sensed current slope during T_{ON}, S_f the sensed current slope during T_{OFF}, and S_e an external ramp slope, whose introduction is justified shortly, all taken in their average forms as both $\hat{u}_I$ and $\hat{u}_O$ are null. From geometrical consideration, a discrete time model can be found, involving i_L, the inductor current, and c, the reference that represents a threshold for the sensed current that triggers the fall edge of duty-cycle and, consequently, the change of the current slope. The discrete time relation between i_L and c descends from this equation:

$$\frac{\hat{i}_L(k+1) - \hat{i}_L(k)}{S_n + S_f} = \frac{\hat{c}(k+1) - \hat{i}_L(k+1)}{S_f - S_e} \tag{2.20}$$

Solving the equation and applying the Z transform lead to:

$$H(z) = \frac{\hat{i}_L(z)}{\hat{c}(z)} = (1+\alpha)\frac{z}{z+\alpha}, \quad \alpha = \frac{S_f - S_e}{S_n + S_e} \tag{2.21}$$

$H(z)$ represents a first order transfer function, with unique pole α that is located outside the unity circle when there is no external ramp ($S_e = 0$) and duty cycle exceeds 50% ($D > 0.5$), making the system unstable.

$$|\alpha| = \left|\frac{S_f}{S_n}\right| = \left|\frac{D}{1-D}\right| > 1 \Rightarrow \alpha \in RHP \tag{2.22}$$

This is a theoretical evidence of the so-called static instability, which in practice occurs even at duty-cycle lower than 50% when no sufficient external ramp, which now acts as a compensation ramp, is used. In order to obtain an equivalent continuous time model $H(s)$, two corrections are applied. First, a variable change $z = e^{sT_s}$ is needed to pass from Z to Laplace transform. Second, a convolution that models the action performed by an equivalent sample&hold filtering. Then, $H(s)$ comes to be:

$$H(s) = \frac{1+\alpha}{sT_s}\frac{e^{sT_s} - 1}{e^{sT_s} + \alpha} \tag{2.23}$$

Reminding its loop definition:

$$H(s) = \frac{F_M F_4^\star}{1 + F_M F_4^\star H_I(s)} \tag{2.24}$$

with $F_4^\star$ defined as

$$F_4^\star := \left.\frac{\hat{i}_L}{\hat{d}}\right|_{\hat{u}=0} = \frac{U_I}{sL} \tag{2.25}$$

$H_I(s)$ can be extracted combining 2.23 and 2.24:

$$H_I(s) = \frac{sT_s}{e^{sT_s} - 1} \tag{2.26}$$

Padé approximation decomposes the exponential term in a polynomial form such that:

$$H_I(s) = 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{{\omega_n}^2} \quad Q_z = -\frac{2}{\pi}, \omega_n = \frac{\omega_s}{2} \tag{2.27}$$

and this is the final result that models PCM sampling action.

• **DCM**

In DCM a perturbation $\hat{i}_L$ comes to zero within a cycle period so sampling action has no dynamics as evident in figure 2.5:

$$H_I = 0 \Longrightarrow F_I = 0 \tag{2.28}$$

• **PFM**

In PFM, circuitry related to peak current mode is bypassed and thus disabled such that current sensing is not effective and again:

$$K_I = 0 \Longrightarrow F_I = 0 \tag{2.29}$$

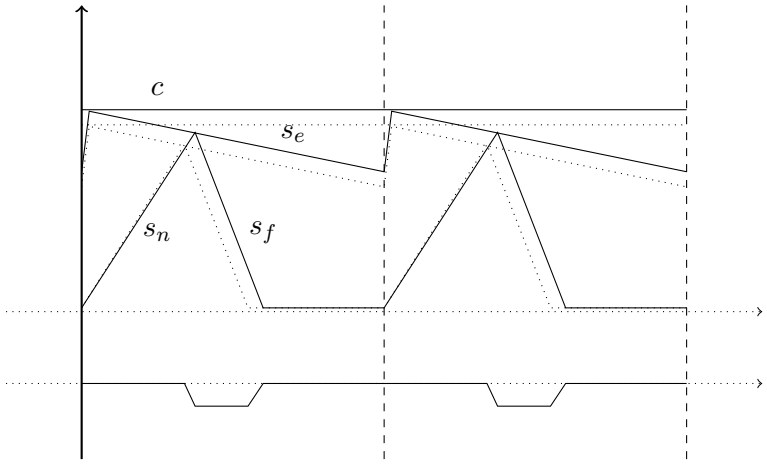


Figure 2.5: Natural response of the current error versus time during DCM operation, generated when either control or current itself is perturbed. Note that the error remains the same each cycle suggesting that no peak detection feedback is active.

2.3.3 PFM-T_{ON} constant Modulator

In the case of Infineon SMPR, PFM signal generation was explained in the previous chapter. Basically a threshold V_{VCO} and constant on time T_{onPFM} are set constants whereas the controlling variable c is the output voltage of the error amplifier:

$$\bar{d} = \frac{T_{onPFM}}{T_{onPFM} + \bar{t}_{off}} \tag{2.30}$$

$$\bar{t}_{off} = T_{VCO}\frac{V_{VCO}}{\bar{c}} \tag{2.31}$$

Approximating $T_{onPFM} \ll \bar{t}_{off}$ the eq. 2.30 becomes:

$$\bar{d} = \frac{T_{onPFM}}{\bar{t}_{off}} \tag{2.32}$$

and then, using 2.31:

$$F_M = \frac{\hat{d}}{\hat{c}} = \frac{T_{onPFM}}{T_{VCO}}\frac{1}{V_{VCO}} \tag{2.33}$$

In paper [2], also a phase term is introduced to model the phase lead characteristics of a constant-on time modulator. In this thesis it is neglected, though.

2.3.4 Other feedback/feedforward terms

The scope of this sections is to find the dependency of i_L from u_I and u_O existing when the peak current mode loop is active (figure 2.6). Note that in Infineon architecture PCM is combined with PWM modulation, so the correspondent F_M is considered.

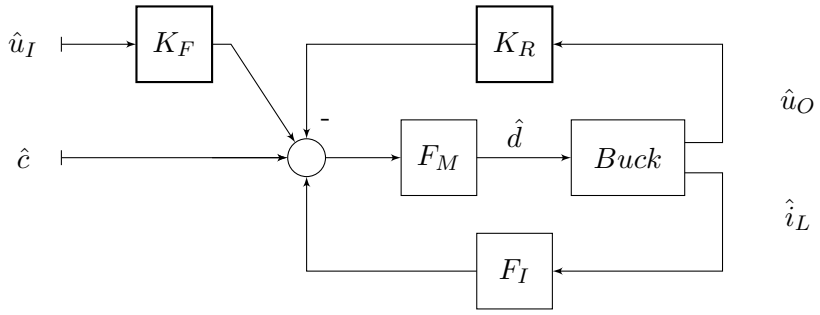


Figure 2.6: Blocks connection to find K_F and K_R.

Remember the definition of the falling slope of the sensed current:

$$\bar{s}_f = \frac{\bar{u}_O K_I}{L} \tag{2.34}$$

where K_I is the scale factor of the current sensor.

• **CCM**

As the perturbation involves either u_I or u_O while current i_L is in steady state, the following is valid:

$$F_I = K_I \tag{2.35}$$

Some relations can be established starting from geometrical consideration on the averaged quantities, from the small signal relations depicted in figure 2.6 and from the small signal CCM definition of d. These relations are put in a system:

$$\begin{cases} K_I \bar{i}_L = \bar{c} - S_e \bar{d} T_s - \frac{(1-\bar{d})T_s}{2} \bar{s}_f \\ \hat{d} = F_M \left(K_F \hat{u}_I - K_R \hat{u}_O + K_I \hat{i}_L \right) \\ \hat{d} = -\frac{D}{U_I} \hat{u}_I + \frac{1}{U_I} \hat{u}_O \end{cases} \tag{2.36}$$

where the last equation recalls the perturbed expression of the conversion factor in CCM, that in its averaged form is:

$$\bar{d} \bar{u}_I = \bar{u}_O \tag{2.37}$$

Solving the system 2.36 yields:

$$\begin{cases} K_F = -D \frac{K_I}{L F_s} \left(1 - \frac{D}{2}\right) \\ K_R = -\frac{K_I}{2 L F_s} \end{cases} \tag{2.38}$$

• **DCM**

Similarly, reminding that F_I is null in DCM, an equation system also for DCM is found:

$$\begin{cases} \bar{d} T_s \bar{s}_n = \bar{c} - S_e \bar{d} T_s \\ \hat{d} = F_M \left(K_F \hat{u}_I - K_R \hat{u}_O \right) \end{cases} \tag{2.39}$$

whose solution is:

$$K_F = K_R = -K_I D \tag{2.40}$$

• **PFM**

As mentioned, with PFM there is no current mode so neither u_I nor u_O intervene to the duty-cycle generation and:

$$K_F = K_R = 0 \tag{2.41}$$

2.3.5 Error amplifier and voltage sensing

Hereby voltage loop related blocks F_E and F_A, placed as in fig. 2.7, are to be found.

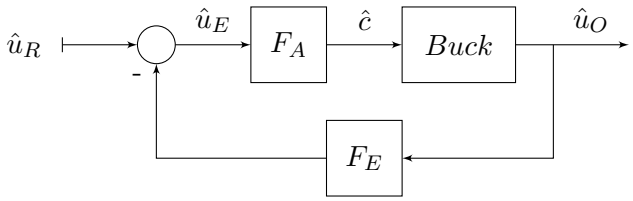


Figure 2.7: External loop, for voltage regulation, block diagram

Voltage sensing is performed by a passive divider made of resistors and capacitors as illustrated in 2.8 so:

$$F_E = \frac{Z_2}{Z_1 + Z_2} \tag{2.42}$$

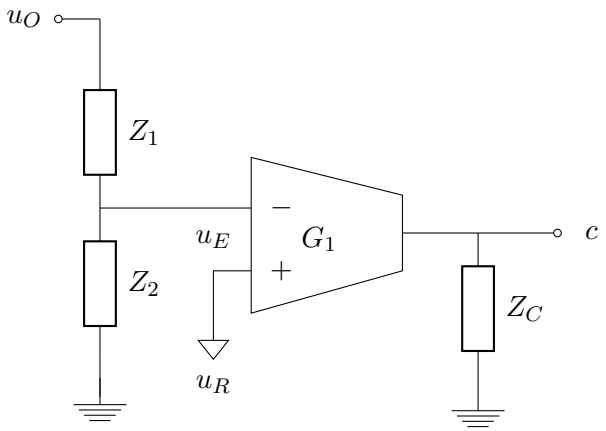


Figure 2.8: Circuitry scheme of the voltage sensor and the error amplifier. Z_2 includes the input impedance of the error amplifier. Similarly, Z_C includes the output impedance of the error amplifier.

Error amplifier is constructed with an Operational Transconductance Amplifier (OTA) with linearised transconductance G_1 and a load impedance Z_C which is used to compensate the loop in frequency. Error amplifier complete transfer function is:

$$F_A = G_1 Z_C G_2 \tag{2.43}$$

with G_2 as a further transconductance introduced in PCM where the controlling variable c is a current instead of a voltage.

Table 2.2: Control related transfer functions

NAME	PWM-CCM	PWM-DCM	PFM-CCM	PFM-DCM
K_R	$-\frac{K_I}{2LF_s}$	$-D\frac{K_I}{LF_s}$	0	0
K_F	$-\frac{K_I}{2LF_s}D\left(1-\frac{D}{2}\right)$	$-D\frac{K_I}{LF_s}$	0	0
F_I	$K_I\left(1+\frac{s}{Q_z\omega_n}+\frac{s^2}{{\omega_n}^2}\right)$	0	0	0
F_M	$\frac{1}{(S_e+S_n)T_s}$	$\frac{1}{(S_e+S_n)T_s}$	$\frac{T_{onPFM}}{T_{VCO}}\frac{1}{V_{VCO}}$	$\frac{T_{onPFM}}{T_{VCO}}\frac{1}{V_{VCO}}$
F_A	$G_1Z_CG_2$	$G_1Z_CG_2$	G_1Z_C	G_1Z_C
F_E	$\frac{Z_2}{Z_1+Z_2}$	$\frac{Z_2}{Z_1+Z_2}$	$\frac{Z_2}{Z_1+Z_2}$	$\frac{Z_2}{Z_1+Z_2}$

All the transfer functions related to the control of each operative region are summarized in table 2.2.

2.4 Resulting small signal model

The resulting small signal model is depicted in fig. 2.9 in the form of a block diagram while table 2.3 summarises all the transfer functions contained in each block.

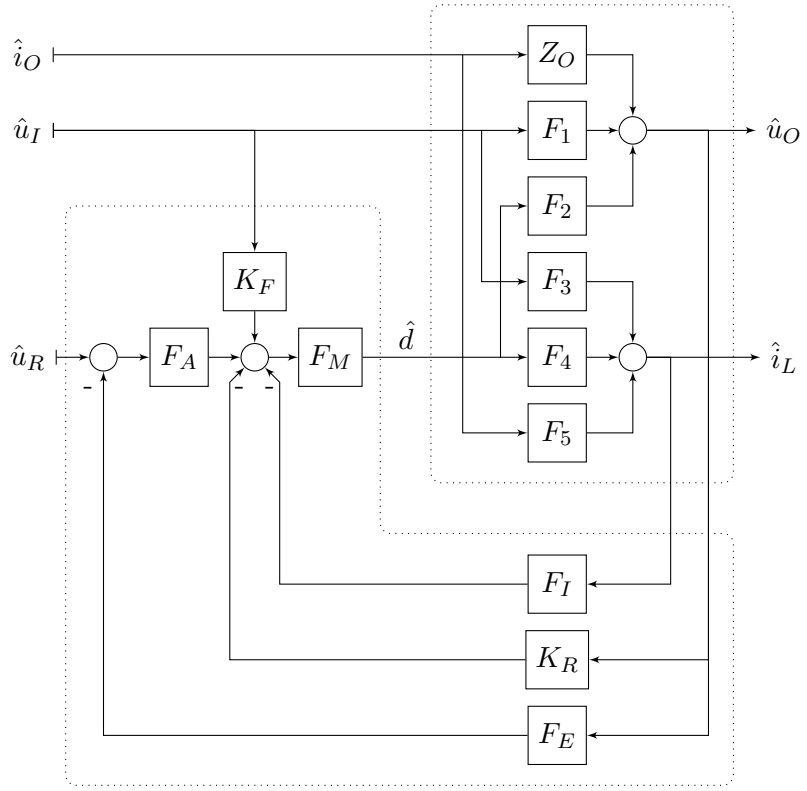


Figure 2.9: Block diagram of the converter. The blocks related to the power stage and to the control blocks are delimited by dotted lines.

Table 2.3: Transfer functions summary of the small signal model

NAME	PWM-CCM	PWM-DCM	PFM-CCM	PFM-DCM
F_1	$D\frac{1+sr_cC}{\Delta(s)}$	$M\frac{1+sr_cC}{\Delta_1(s)}$	$D\frac{1+sr_cC}{\Delta(s)}$	$M\frac{1+sr_cC}{\Delta_1(s)}$
F_2	$U_I\frac{1+sr_cC}{\Delta(s)}$	$\frac{2U_o}{D}\frac{1-M}{2-M}\frac{1+sr_cC}{\Delta_1(s)}$	$U_I\frac{1+sr_cC}{\Delta(s)}$	$\frac{2U_o}{D}\frac{1-M}{2-M}\frac{1+sr_cC}{\Delta_1(s)}$
F_3	$\frac{D}{R}\frac{1+sRC}{\Delta(s)}$	$\frac{M}{R}\frac{1+s(R+r_c)C}{\Delta_1(s)}$	$\frac{D}{R}\frac{1+sRC}{\Delta(s)}$	$\frac{M}{R}\frac{1+s(R+r_c)C}{\Delta_1(s)}$
F_4	$\frac{U_I}{R}\frac{1+sRC}{\Delta(s)}$	$\frac{2I_o}{D}\frac{1-M}{2-M}\frac{1+s(R+r_c)C}{\Delta_1(s)}$	$\frac{U_I}{R}\frac{1+sRC}{\Delta(s)}$	$\frac{2I_o}{D}\frac{1-M}{2-M}\frac{1+s(R+r_c)C}{\Delta_1(s)}$
F_5	$\frac{r_L}{R}\frac{(1+sRC)(1+sL/r_L)}{\Delta(s)}-1$	$\frac{(1+sr_cC)}{\Delta_2(s)}$	$\frac{r_L}{R}\frac{(1+sRC)(1+sL/r_L)}{\Delta(s)}-1$	$\frac{(1+sr_cC)}{\Delta_2(s)}$
Z_O	$r_L\frac{(1+sr_cC)(1+sL/r_L)}{\Delta(s)}$	$R(1-M)\frac{(1+sr_cC)\left(1+s\frac{L}{R}\frac{M}{D}\right)}{\Delta_2(s)}$	$r_L\frac{(1+sr_cC)(1+sL/r_L)}{\Delta(s)}$	$R(1-M)\frac{(1+sr_cC)\left(1+s\frac{L}{R}\frac{M}{D}\right)}{\Delta_2(s)}$
K_R	$-\frac{K_I}{2LF_s}$	$-D\frac{K_I}{LF_s}$	0	0
K_F	$-\frac{K_I}{2LF_s}D\left(1-\frac{D}{2}\right)$	$-D\frac{K_I}{LF_s}$	0	0
F_I	$K_I\left(1+\frac{s}{Q_z\omega_n}+\frac{s^2}{{\omega_n}^2}\right)$	0	0	0
F_M	$\frac{1}{(S_e+S_n)T_s}$	$\frac{1}{(S_e+S_n)T_s}$	$\frac{T_{onPFM}}{T_{VCO}}\frac{1}{V_{VCO}}$	$\frac{T_{onPFM}}{T_{VCO}}\frac{1}{V_{VCO}}$
F_A	$G_1Z_CG_2$	$G_1Z_CG_2$	G_1Z_C	G_1Z_C
F_E	$\frac{Z_2}{Z_1+Z_2}$	$\frac{Z_2}{Z_1+Z_2}$	$\frac{Z_2}{Z_1+Z_2}$	$\frac{Z_2}{Z_1+Z_2}$

Chapter 3

Model Validation

The small signal model found in the previous chapter needs a validation before proceeding to the stability analysis and the parameters optimization dealt in the next chapter. Validation is achieved through simulations in Matlab-Simulink environment, comparing the time responses of the small signal model with those of an another model which is hereby presented.

3.1 Simulink model

Simulink is a ®Matlab toolbox that allows to build a dynamic system by disposing and interconnecting in a graphical way elementary blocks like sums, amplifiers, integrators, comparators and logic gates and to simulate it with built-in solvers. By the composition of such elementary blocks it is possible to build more complex blocks in a modular way. Furthermore, the integration of Matlab functions and scripts makes Simulink a very useful tool for engineering. Using dynamic equations of chapter 1, it is very simple to create the instantaneous model of the Buck converter.

To give some details on the implementation, DCM operation on the power stage is easily obtained applying a floor saturation on the integrator associated to the inductor, so that the inductor current state variable clamps to zero without the need of explicit feedback control. Series resistances of the inductor and the capacitor are introduced by means of a local feedback or a local feed-forward, respectively. Concerning the models of the OTA, they are parametrised not only by their linearised gains but also by threshold levels in order to get values on the system simulations near to the reality. Obviously thresholds have effect only in the instantaneous model, and are not considered at all in the small signal model. Finally, an useful trick when evaluating signals with large ripples is to apply a moving average filtering on them, so that average quantities can be evaluated easily, e.g. I_L from i_L, even in DCM. No saturations i.e. limits on the headroom of the signals are set, in order not to ruin the successfulness of the models comparison.

The top level appearance of the Simulink model is shown in fig. 3.1, while the buck power stage in fig. 3.2 and the controller in fig. 3.3.

3.2 Validation

Simulink model is powerful albeit simple because it can approximately simulate the instantaneous quantities of the system spending a moderate CPU time. Small signal model, on the other part, is supposed to simulate the averaged quantities with almost zero CPU time, even if only in the neighbourhood of a parametric point.

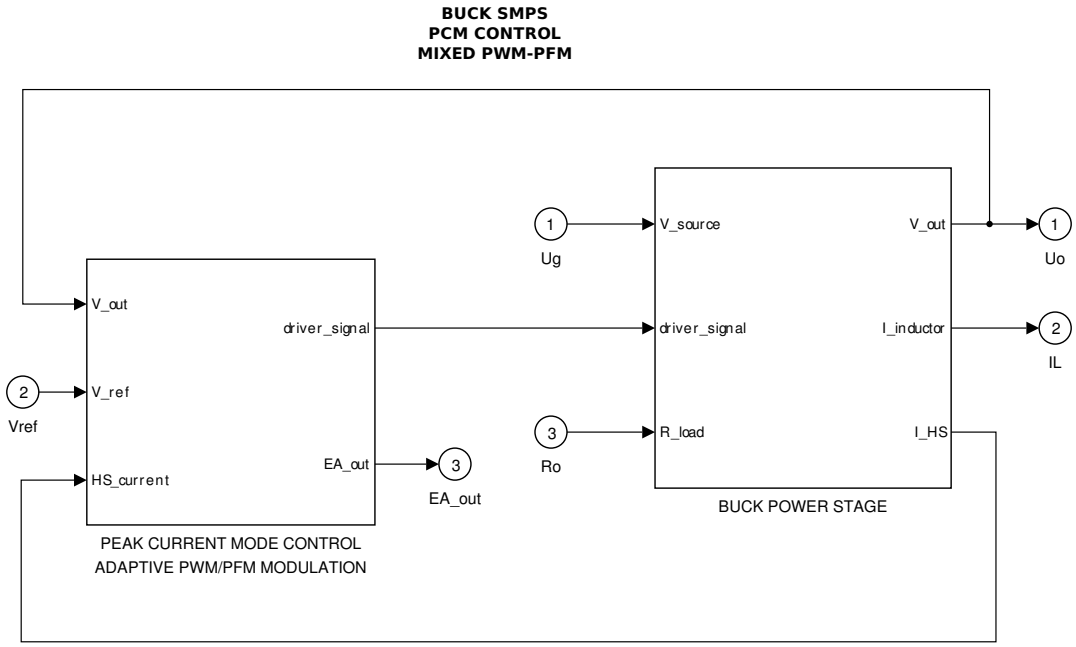


Figure 3.1: Simulink model appearance of the Buck SMPS, in the form of two major sub-blocks put in closed loop.

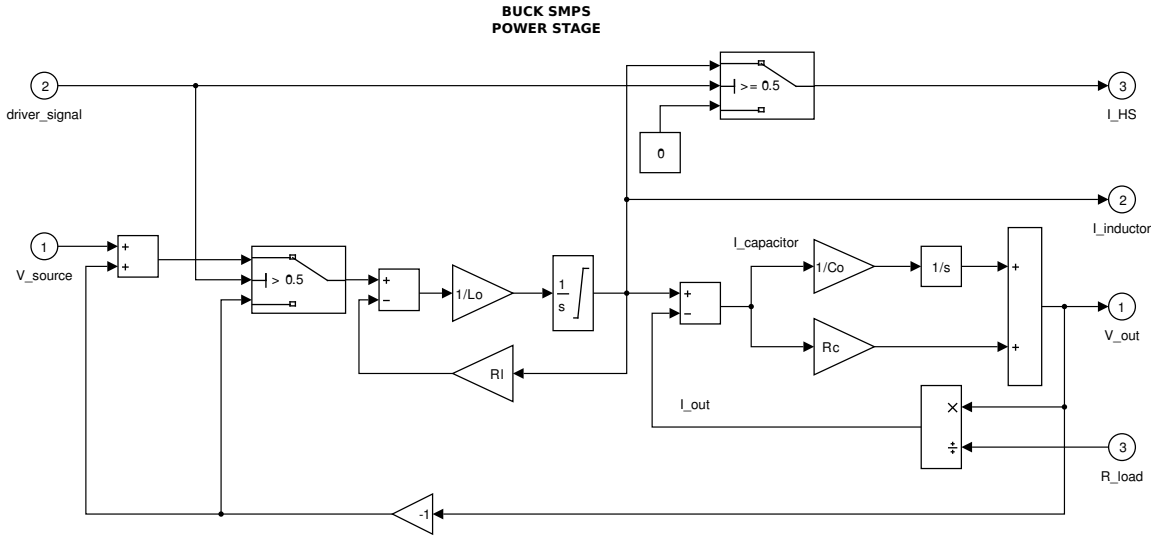


Figure 3.2: Simulink model inspection of the power stage.

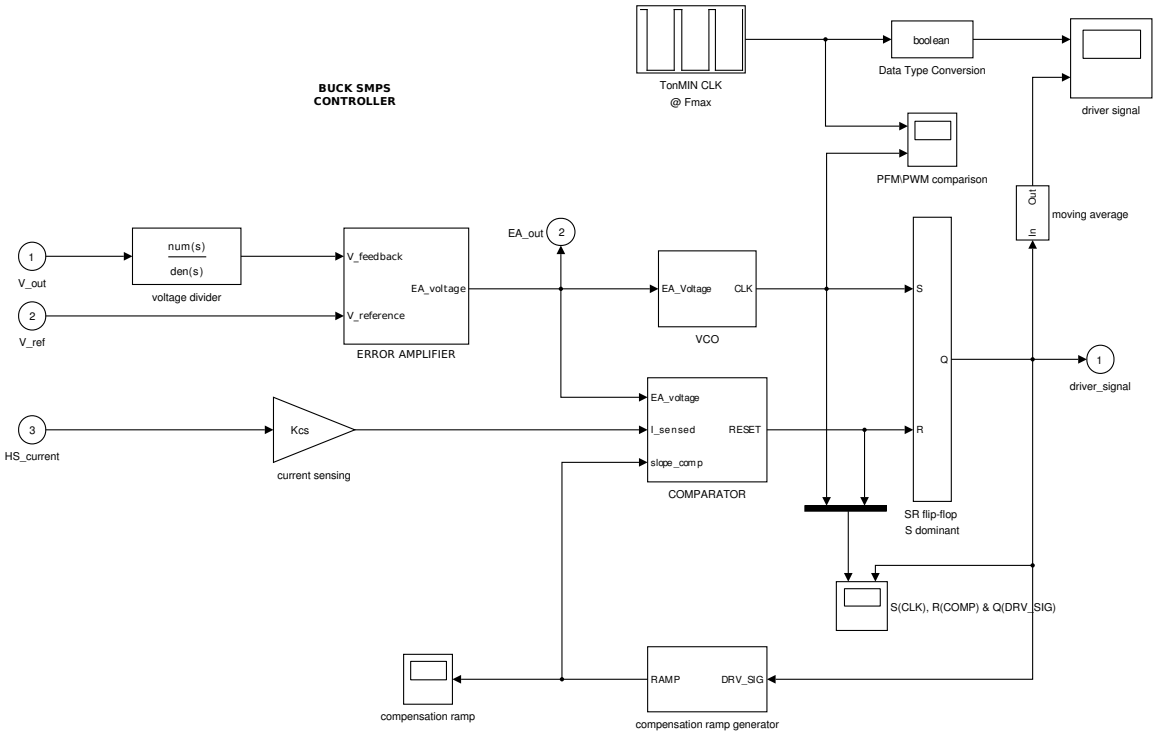


Figure 3.3: Simulink model inspection of the controller

It would be useful to rely on the small signal model for stability analysis without taking much time. The problem is that small signal model is theoretical and needs an empirical validation. Therefore, a test via simulations in Matlab environment is done in order to validate it.

Note that both models are characterised by a limited number of parameters but each of them varies in a dense interval. So, there are infinite combinations of parameters and validation as wide as it could be cannot cover 100 percent of cases.

Time response evaluation is done applying a stimulus on the main inputs, one at a time, of both systems and seeing what happens to the main outputs.

Inputs

- u_I battery line voltage
- u_R band-gap reference
- i_O load current or, equivalently, load resistance r_O

Outputs

- u_O load voltage
- i_L inductor current
- EA_{out} output voltage of the error amplifier

Step function is chosen to be the stimulus as usual practice in stability tests in which a point of equilibrium is perturbed and supposed to bring the system into another one. The amplitude of the step stimulus applied to the instantaneous Simulink (non-linear) model has to be small enough to respect linearisation hypotheses $\hat{x} \ll X$ and in order to keep the same operative mode before, during and after the perturbation. The perturbation amplitude has not to be too small otherwise the response dynamics is not visually discernible from the steady state ripple. For the (linear) small signal model instead the amplitude does not matter and is set to be equal to the one of the other model in order get a comparison on normalized scale.

Control theory states that a system is characterised by the loop rather than the variables themselves. Equivalently, the dynamic of a system is defined regardless which variable in the loop is input and which is output.

Therefore, one input - one output would be sufficient to get significant evaluation of the dynamic response of both the systems. u_O is definitely taken as output as it is the most important quantity to regulate.

Nevertheless, all three inputs $\{u_I, u_R, i_O\}$ are taken not only to strengthen the empirical evaluation but also because they are typically varied also in real case and their effect are figures of merit that are documented in product data sheet.

Given the previous motivations, $\{u_I, u_R, i_O\} \Rightarrow u_O$ step responses are evaluated and reported into graphs.

Other two outputs i_L, EA_{out} are observed as well since they determine the operative condition of the converter, respectively the power stage current conduction (CCM-DCM) and the modulation (PWM-PFM) type, and are monitored during the transient to ensure the persistence of such condition. Their associated time responses are not plotted in a graph, though, because dynamics entity can be easily covered by the static ripple thus making comparison difficult. In fact, EA_{out} waveform has shrink dynamic headroom, while i_L static ripple can overwhelm its average quantity especially in DCM.

To summarise, evaluated transfer functions under small perturbation are:

- $F_R := \frac{\hat{u}_O}{\hat{u}_R}$
- $F_1^{CL} := \frac{\hat{u}_O}{\hat{u}_I}$
- $Z_O^{CL} := \frac{\hat{u}_O}{\hat{i}_O}$

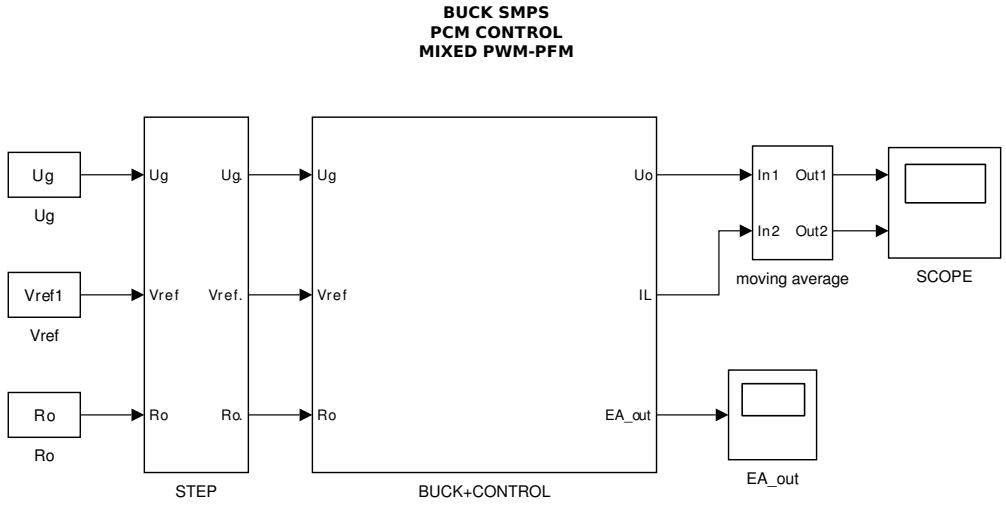


Figure 3.4: Simulink test-bench appearance

# Region		Operative mode	
		CCM	DCM
Modulation type	PWM	1	2
	PFM	3	4

where superscript CL on some functions specifies the closed loop version of them.

The comparison is desired to reveal the difference of both the dynamic and the static error between the two models. For this purpose, a Matlab script put together the responses of the average model and the instantaneous model, starting at the same time and at the same amplitude level. Same amplitude level of time responses just before perturbation is needed because small signal model cannot predict the precise DC operative point of the instantaneous model before perturbation, but only the differential DC point before and after perturbation.

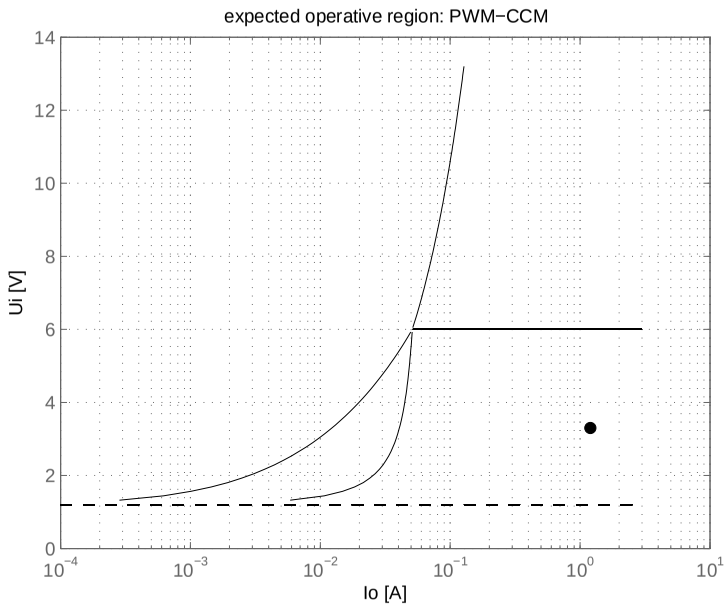
3.2.1 Results

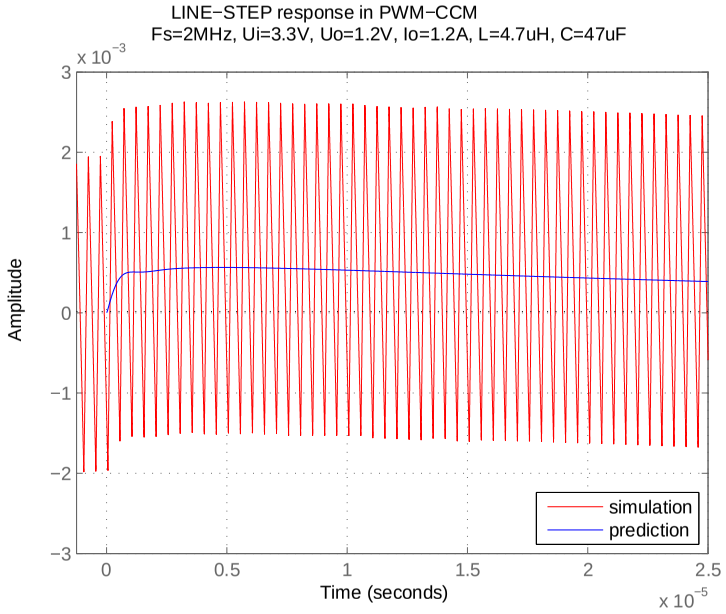
Hereby 4 examples are reported, each for the operative region of the converter.

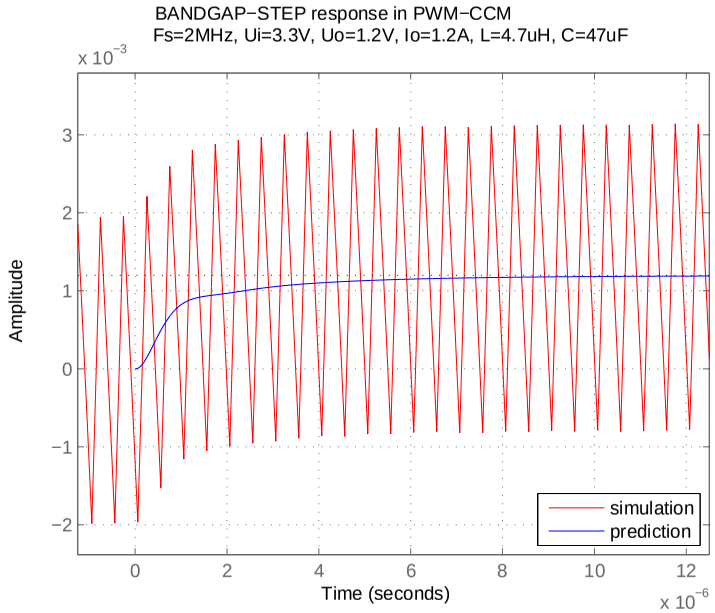
Each example includes the map with the operative point location and the three types of the time responses. Positive or negative stimulus lead to equivalent results, even if choice may be visually better if it leads to lower static ripple. For the examples given, these stimuli are considered:

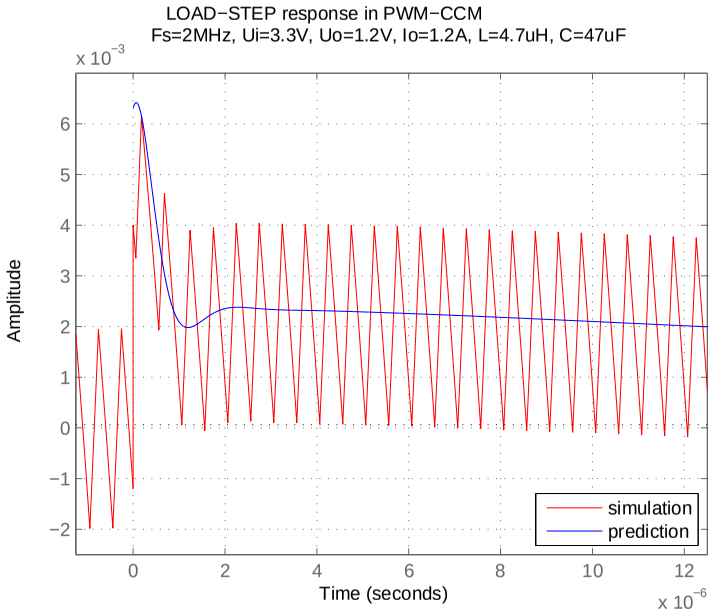
- $\hat{u}_I = +10\%U_I$
- $\hat{u}_R = +0.1\%U_R$
- $\hat{r}_O = +10\%R_O \Longleftrightarrow \hat{i}_O = -9\%I_O$

Region 1

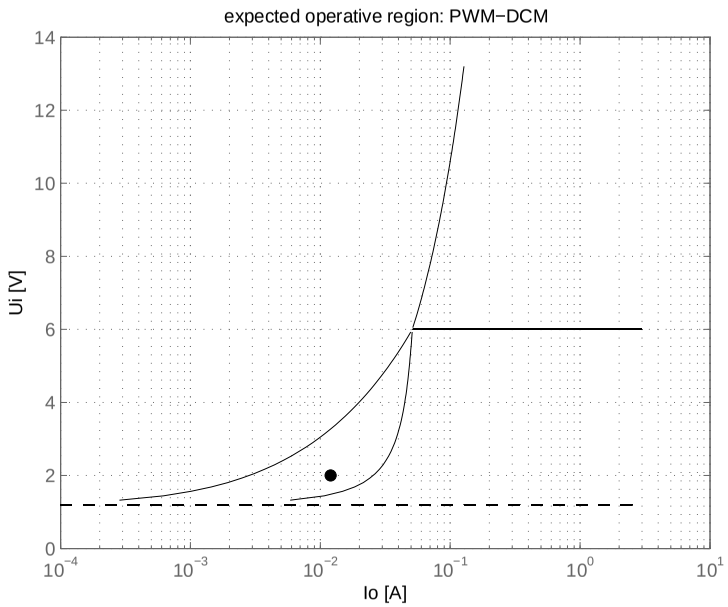

expected operative region: PWM−CCM
Ui [V]
Io [A]

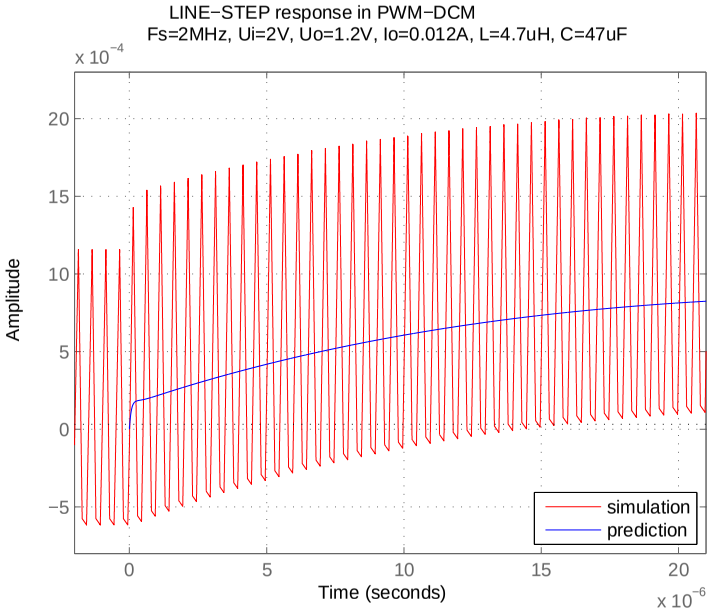

LINE−STEP response in PWM−CCM
Fs=2MHz, Ui=3.3V, Uo=1.2V, Io=1.2A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

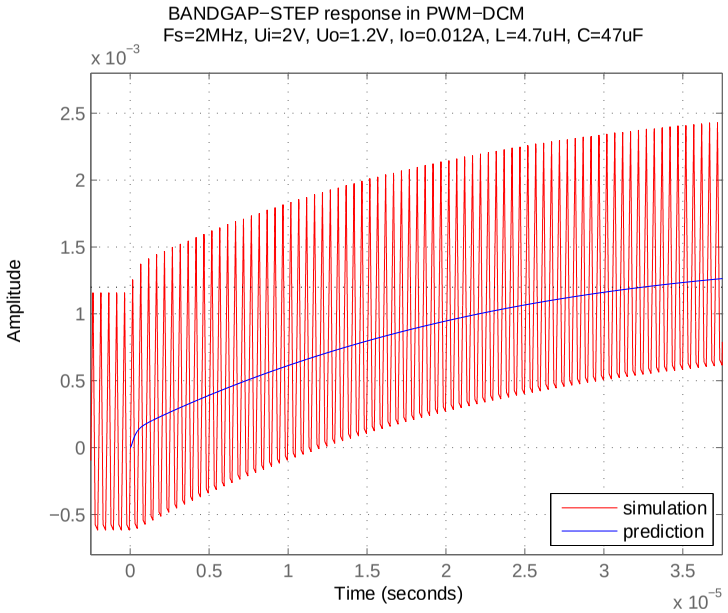

BANDGAP−STEP response in PWM−CCM
Fs=2MHz, Ui=3.3V, Uo=1.2V, Io=1.2A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

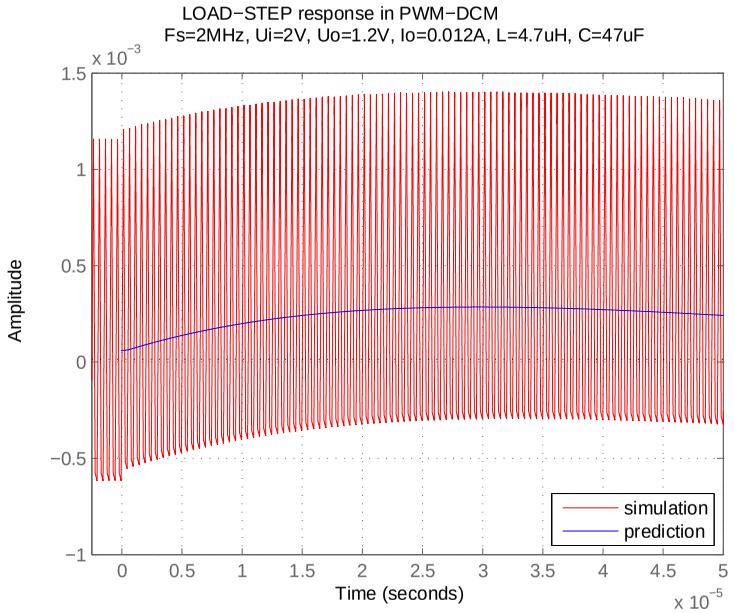

LOAD−STEP response in PWM−CCM
Fs=2MHz, Ui=3.3V, Uo=1.2V, Io=1.2A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

Region 2

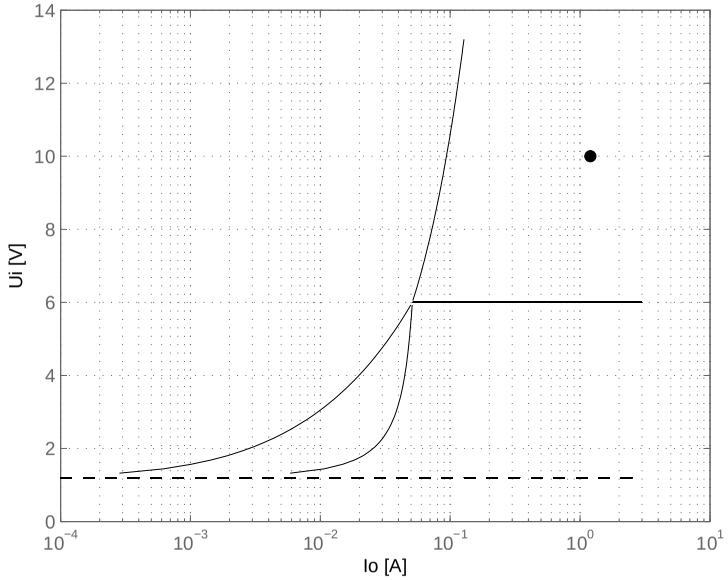

expected operative region: PWM−DCM
Ui [V]
Io [A]

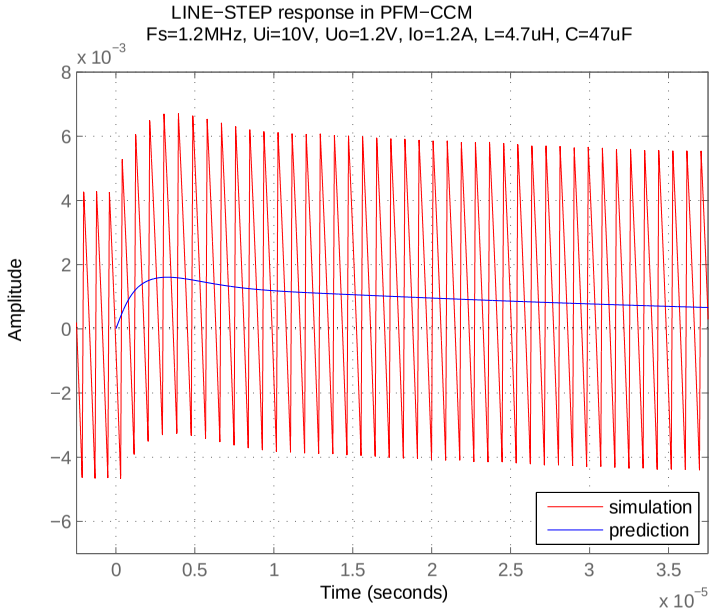

LINE−STEP response in PWM−DCM
Fs=2MHz, Ui=2V, Uo=1.2V, Io=0.012A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

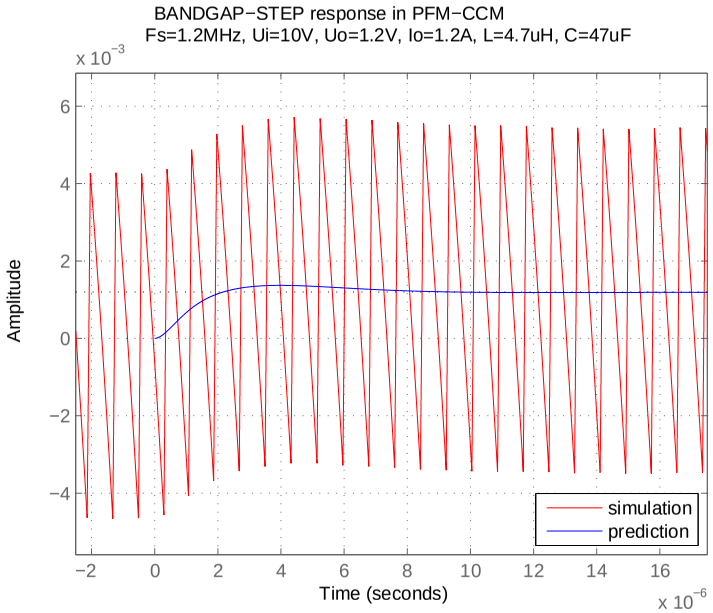

BANDGAP−STEP response in PWM−DCM
Fs=2MHz, Ui=2V, Uo=1.2V, Io=0.012A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

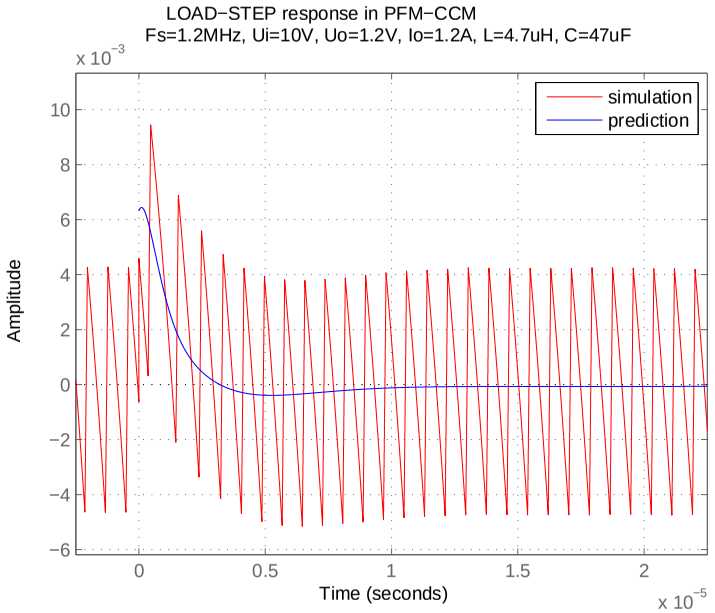

LOAD−STEP response in PWM−DCM
Fs=2MHz, Ui=2V, Uo=1.2V, Io=0.012A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

Region 3

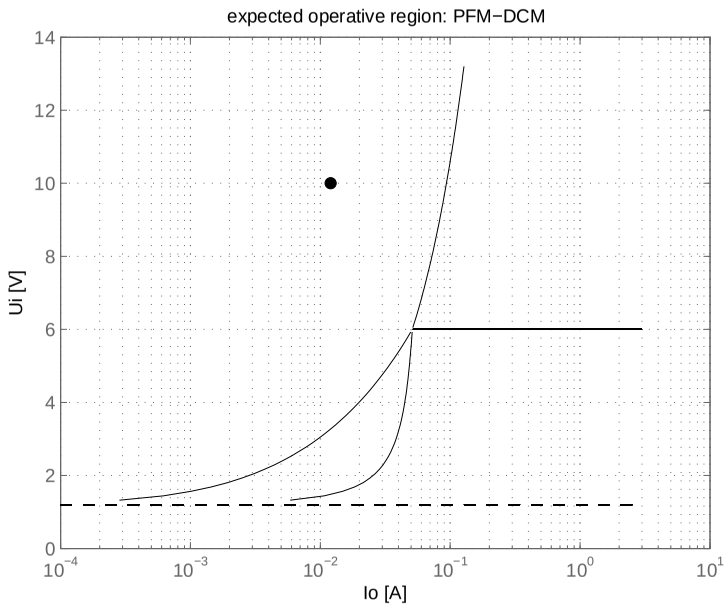

expected operative region: PFM−CCM
Ui [V]
Io [A]

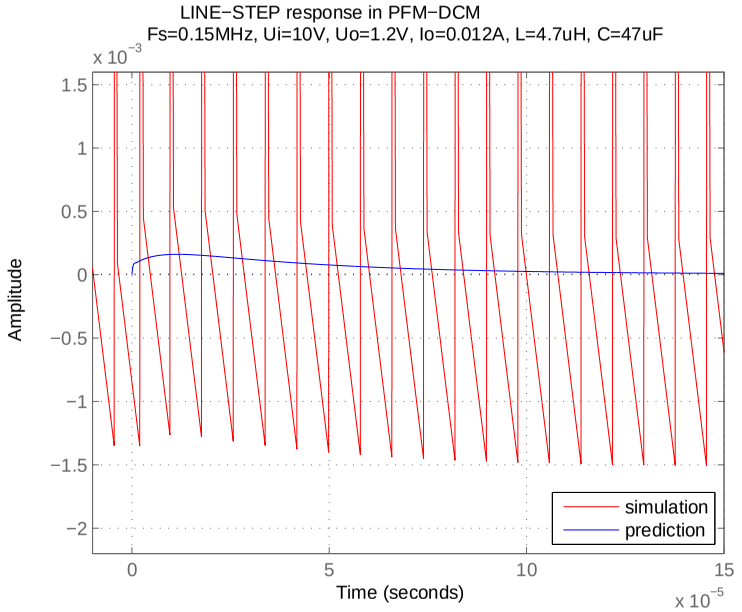

LINE−STEP response in PFM−CCM
Fs=1.2MHz, Ui=10V, Uo=1.2V, Io=1.2A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

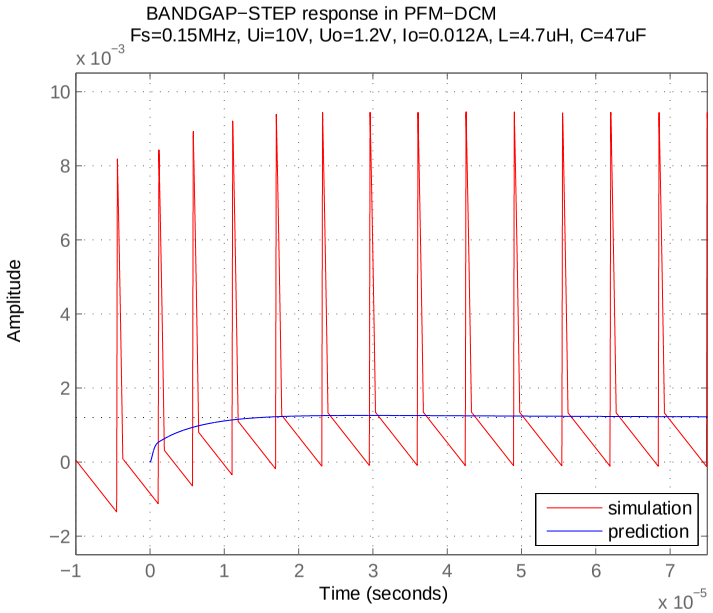

BANDGAP−STEP response in PFM−CCM
Fs=1.2MHz, Ui=10V, Uo=1.2V, Io=1.2A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

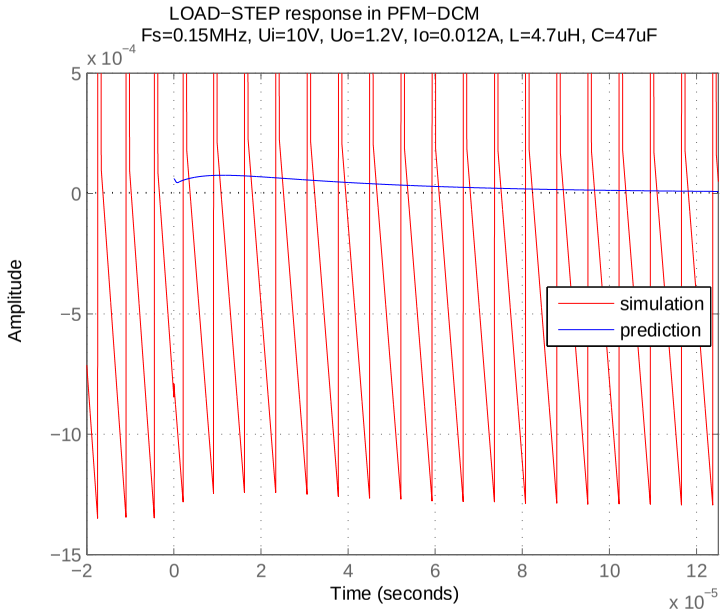

LOAD−STEP response in PFM−CCM
Fs=1.2MHz, Ui=10V, Uo=1.2V, Io=1.2A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

Region 4


expected operative region: PFM−DCM
Ui [V]
Io [A]


LINE−STEP response in PFM−DCM
Fs=0.15MHz, Ui=10V, Uo=1.2V, Io=0.012A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction


BANDGAP−STEP response in PFM−DCM
Fs=0.15MHz, Ui=10V, Uo=1.2V, Io=0.012A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction


LOAD−STEP response in PFM−DCM
Fs=0.15MHz, Ui=10V, Uo=1.2V, Io=0.012A, L=4.7uH, C=47uF
Amplitude
Time (seconds)
simulation
prediction

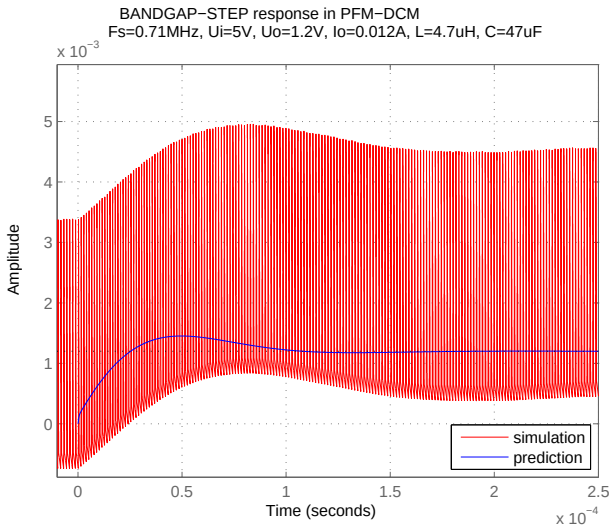


Figure 3.5: Inaccuracy example

The model seems to be accurate for the cases considered, but also for a wide amount of other cases. Although, inaccuracies are spotted in certain cases, especially at high duty-cycles of region 4, where the modelling of the PFM constant T_{ON} modulator possibly reveals its limits. An example of inaccuracy is reported in fig. 3.5, where there is a slight mismatch of the transient timings, but overshoots amplitudes are quite respected.

The overall impression is that small signal model accuracy is adequate for stability analysis.

Chapter 4

Stability

Stability in all automated system, electronic included, is a real matter of concern and needs appropriate study, as an overlook in this sense can virtually annihilate all the efforts put on other aspects of the system. A model from which to derive stability analysis is really useful at the beginning of a design activity, because it gives clues about the values the parameters can assume. As the problem is multivariate, a graphical interface program that gives a quick overview of the pass/fail check of these values is helpful. Nonetheless, theoretical modelling alone is not sufficient to guarantee stability and at the end a measurement through network analyser is required to reduce risks of failure [7].

4.1 Method

Small signal transfer functions of both power stage and controller of the SMPR have been found in chapter 2 and regrouped in four sets of transfer functions associated to the respective operative regions of the converter. The general block diagram containing the transfer functions is depicted again for convenience in fig. 4.1 and is valid for any operation mode (CCM and DCM) and modulation type (PWM and PFM).

Starting from the innermost, three loops are present:

1. $T_I := F_M F_4 F_I$
2. $T_V := F_M F_2 K_R$
3. $T_E := F_A F_M F_2 F_E$.

T_I and T_V are the inner loops, and related to the peak current mode. In particular, T_I models the current sampling action performed by PCM, and is effective only in region 1. In region 2, even if PCM is active, T_I is null and so it is in region 3 and 4 since PCM is disabled (see chapter 2). On the other side T_V is an intrinsic voltage loop, related to the effect of the output voltage on the current loop. It is present in region 1 and 2 while in regions 3 and 4 is null. Finally, T_E is the explicit voltage loop and is never null since it is necessary for voltage regulation.

Control theory states that all the variables of a closed loop system share the same, significant to stability, portion of dynamics. Or, independently from where and how

# Region		Operative mode	
		CCM	DCM
Modulation type	PWM	1	2
	PFM	3	4

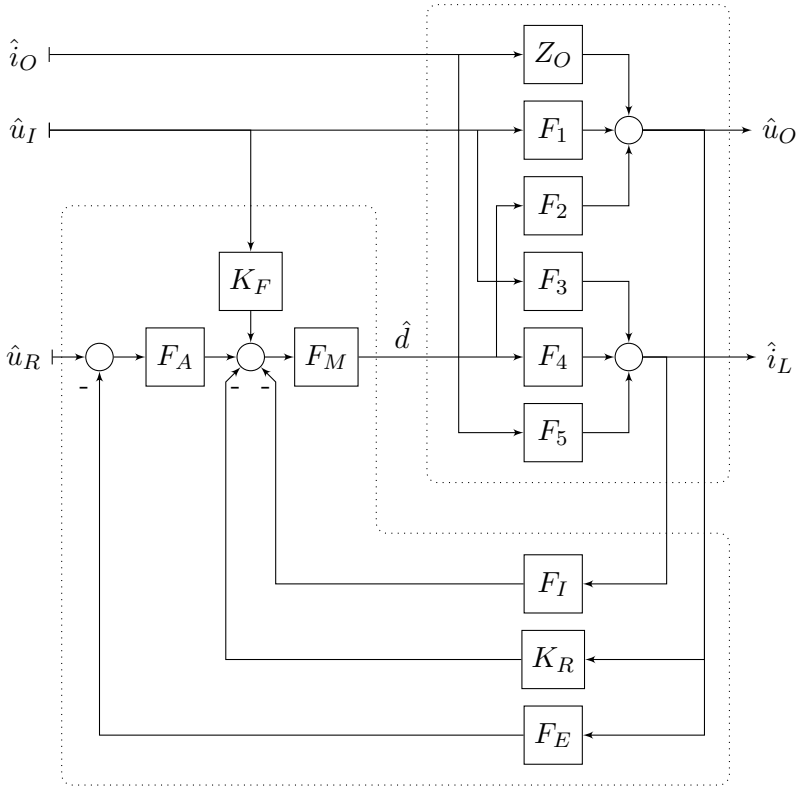


Figure 4.1: Multi-loop block diagram of the converter.

strongly the input is and, by extension, in absence of external stimuli, the state of the system evolves naturally as if it were a single entity. Therefore, when it comes to stability analysis the multi-loop system can be "compressed" to a single-loop, called regulation loop and denoted as T_R, simply enclosing inner loops T_I and T_V, provided that also associated subsystems are stable. The subsystem composed by F_M, F_2, F_4 with feedbacks F_I K_R active (i.e. with loops T_I and T_V closed) is called control-to-output transfer function, denoted as F_H and found in literature in its approximated and factorised version (see table 4.1).

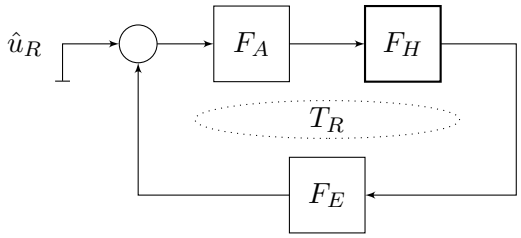


Figure 4.2: Single loop representation obtained from enclosing inner loops of the multi-loop block diagram.

At this point regulation loop t.f. is defined as:

$$T_R := F_A F_H F_E \tag{4.1}$$

where F_H is the already defined control to output transfer function related to the controlled Buck converter, F_A to the error amplifier, F_E to the voltage sensing.

Scope of this section is to analyse F_H for each operative region of the converter and to decree the critical situations for stability, then to propose a compensation on the

Table 4.1: Transfer functions of the filter loop

Region	Loop Definition	Factorised Expression
1	$\frac{F_M F_2}{1+T_I+T_V}$	$\frac{R}{K_I}\frac{1}{\frac{R}{LF_s}(m_C(1-M)-0.5)+1}\frac{1+s/\omega_z}{1+s/\omega_p}\frac{1}{1+\frac{s}{\omega_n Q_n}+\frac{s^2}{\omega_n^2}}$
2	$\frac{F_M F_2}{1+T_V}$	$F_M\frac{2m_C U_O}{D}\frac{1-M}{2m_C-(2+m_C)M}\frac{1+s/\omega_z}{\left(1+s/\omega^\star_{p1}\right)(1+s/\omega_{p2})}$
3	$F_M F_2$	$F_M U_I\frac{1+s/\omega_z}{1+\frac{s}{Q_o\omega_o}+\frac{s^2}{\omega_o^2}}$
4	$F_M F_2$	$F_M\frac{2U_O}{D}\frac{1-M}{2-M}\frac{1+s/\omega_z}{(1+s/\omega_{p1})(1+s/\omega_{p2})}$

$$\omega_z = \frac{1}{r_C C}$$
$$\omega_n = \frac{\omega_s}{2} = \pi F_s$$
$$\omega_p = \frac{1}{RC} + \frac{2}{\omega_s LCQ_n}$$
$$\omega_{p1} = \frac{2-M}{RC(1-M)}$$
$$\omega^\star_{p1} = \frac{2m_C-(2+m_C)M}{RCm_C(1-M)}$$
$$\omega_{p2} = \frac{R(1-M)}{L} = 2F_S\left(\frac{M}{D}\right)^2$$
$$\omega_o = \frac{1}{\sqrt{LC}}$$
$$Q_o = \frac{R\sqrt{L/C}}{L/C+(r_L+r_C)R}$$
$$\omega_n = \frac{\omega_s}{2}$$
$$Q_n = \frac{1}{\pi(m_c(1-D)-0.5)}$$

regulation loop T_R that covers them all.

Compensation on T_R means that its frequency response $T_R(j\omega)$, plot in Bode diagrams, must have a proper phase margin Φ_M (e.g.$\Phi_M > 40\,\text{deg}$) in correspondence with its crossover frequency F_c, also called unity gain bandwidth, according to the Bode criteria statement. Crossover frequency F_c is set minor than F_s not only to eliminate switching frequency signals (i.e. attenuating ripple) but also because in proximity of F_s certain phase lags introduced by parasitic elements, propagation delays, and other effects that are not predicted by the model may be critical for stability.

Bode diagram is a suitable xy graph since it renders the operation of "compensation" into moving $T_R(j\omega)$ vertically by changing its gain, and into moving phase contributes (lags or leads) in a horizontal sense.

4.1.1 Internal loop compensation

In regions 1 and 2, PCM introduces internal feedback loops that add degrees of freedom and make overall compensation easier, but that in turn must be analysed. In fact, as explained in chapter 2, PCM control is known to suffer from static instability when no sufficient compensation ramp slope S_e is used and for duty-cycle D higher than 50%. Actually static instability appears even for inferior duty-cycle, as shown in fig. 4.3. In the example given, with insufficient compensation current waveform is apparently stable but suffers from sub-harmonics, for example those with period $2T_s$. With adequate compensation instead, sub-harmonics disappear and waveform is mono-periodic with period T_s.

In region 2 and 3, PFM with constant T_{on} control does not introduce internal nested loops. Therefore, compensation has less degrees of freedom, and has to be made on the only loop present, the external loop T_E which in this case coincides with the regulation

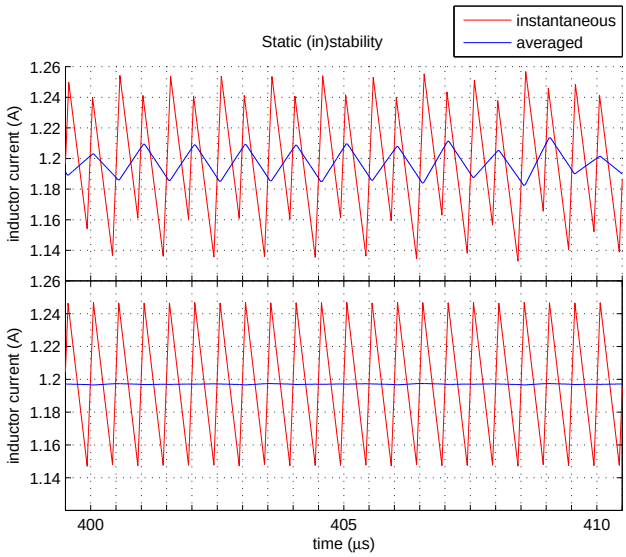


Figure 4.3: Inductor current waveforms under periodic ($T_s = 0.5\mu s$) steady state equilibrium, for insufficient (top) and adequate (bottom) current loop compensations.

loop T_R.

Region 1

Consider F_H of region 1:

$$F_H = F_H(0)\frac{1 + s/\omega_z}{1 + s/\omega_p}\frac{1}{1 + \frac{s}{\omega_n Q_n} + \frac{s^2}{\omega_n^2}} \tag{4.2}$$

F_H shows a zero at frequency

$$\omega_z = \frac{1}{r_C C} \tag{4.3}$$

a real pole at frequency

$$\omega_p = \frac{1}{RC} + \frac{2}{\omega_s LCQ_n} = \frac{1}{RC} + \frac{\omega_o^2}{\omega_n Q_n} \tag{4.4}$$

and a poles pair, which are real or complex according to the damping factor Q_n:

$$Q_n = \frac{1}{\pi\left(m_c(1-D) - 0.5\right)} \tag{4.5}$$

and natural frequency $\omega_n = \frac{\omega_s}{2} = \pi F_s$.

So, provided that all poles are in the LHP, total phase lag is 180 deg.

$m_c := 1 + \frac{S_e}{S_n}$ is the key element for current loop compensation since it allows to obtain lower resonance of the complex poles pair, and possibly splitting into real poles, when this practical condition is met:

$$0 < Q_n < 1 \tag{4.6}$$

At this point S_e can be derived imposing a desired value of Q_n. In another way, to reveal static instability causing sub-harmonic oscillations, consider parameter α, which is the pole in Z domain of the Ridley's discrete model described in chapter 2 :

$$\alpha = \frac{S_f - S_e}{S_n + S_e} \tag{4.7}$$

Imposing its location inside the unity circle:

$$|\alpha| = \left|\frac{S_f - S_e}{S_n + S_e}\right| < 1 \tag{4.8}$$

two sets of solutions are found:

$$\begin{cases} S_e < S_f \\ S_e > 0.5(S_f - S_n) \end{cases} \vee \begin{cases} S_e > S_f \\ S_f + S_n > 0(true) \end{cases} \tag{4.9}$$

Usually [6, 8] S_e is chosen from the first set of solutions of eq. 4.9:

$$\frac{S_f - S_n}{2} < S_e < S_f \tag{4.10}$$

.

For SMPR application, in which S_n and S_f have a significant variability, a solution taken from the second set is more convenient:

$$S_e > max\{S_f\} \tag{4.11}$$

.

So, to eliminate static instability, m_c or, equivalently, S_e, must be high. Also, the effect of increasing m_C is directly visible on F_H, because the factor Q_n is lowered down and pole splitting occurs. In this manner phase lag is flat over a wide range of frequencies instead of appearing abruptly at ω_n.

Although, m_c must not be too high otherwise current loop T_I is not effective. In fact, a huge compensation ramp eliminates at once (i.e. within the next cycle period) current error and kills the info related to the average current fed-back to the loop. In other words, when compensation ramp overwhelms the control signal, the former becomes a constant controlling reference whereas the latter loses its controlling capability, making the closed loop system an internal autonomous subsystem rather than a nested and controlled one. Three usages of S_e are depicted in fig. 4.4: a too small S_{e1} produces a resonant system, whereas a too big S_{e3} produces an over-damped one.

Another parameter to manipulate is K_I, the current sensing gain, that alters the DC gain of F_H:

$$F_H(0) = \frac{R}{K_I} \frac{1}{\frac{R}{LF_s}(m_C(1-D) - 0.5) + 1} \tag{4.12}$$

But since DC gain compensation can be done by means of other parameters, a correct K_I choice takes into account noise and consumption issues prevalently, rather than stability.

Region 2

Consider F_H of region 2:

$$F_H = \frac{LF_s}{m_c K_I U_I (1-M)} \frac{2m_C U_O}{D} \frac{1-M}{2m_C - (2+m_C)M} \frac{1 + s/\omega_z}{\left(1 + s/\omega_{p1}^{\star}\right)(1 + s/\omega_{p2})} \tag{4.13}$$

with first pole at low frequency

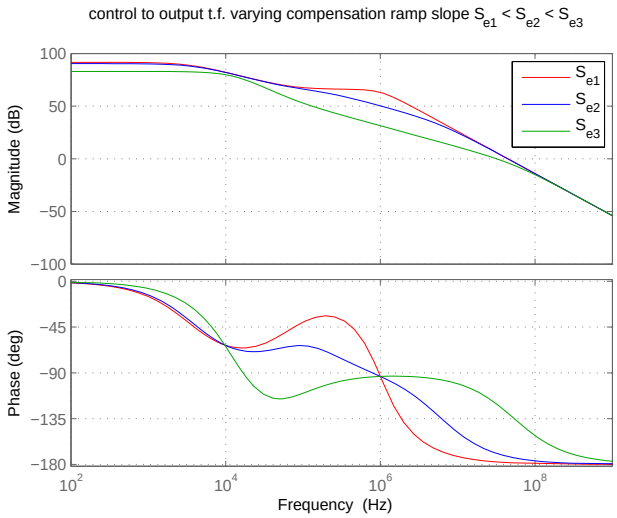


Figure 4.4: control to output t.f. F_H for different compensation ramp slopes

$$\omega_{p1}^{\star} = \frac{2m_C - (2 + m_C)M}{RCm_C(1 - M)} \tag{4.14}$$

and second pole at high frequency

$$\omega_{p2} = \frac{R(1 - M)}{L} \tag{4.15}$$

in addition to the usual zero at frequency

$$\omega_z = \frac{1}{r_C C} \tag{4.16}$$

Potentially also in DCM instability may occur. For example, with no compensation ramp $S_e = 0 \Longleftrightarrow m_C = 1$, first pole goes into RHP for $M > \frac{2}{3}$.

The zero and the two poles, provided that the first pole is in LHP, lead to 90 phase lag.

Region 3

Consider now F_H of region 3:

$$F_H = F_M U_I \frac{1 + s/\omega_z}{1 + \frac{s}{Q_o \omega_o} + \frac{s^2}{\omega_o^2}} \tag{4.17}$$

with

$$\omega_z = \frac{1}{r_c C} \tag{4.18}$$

$$\omega_o = \frac{1}{\sqrt{LC}}, \quad Q_o = \frac{R\sqrt{L/C}}{L/C + (r_L + r_C)R} \tag{4.19}$$

F_H shows a zero and a complex poles pair that overall lead to a 90 deg phase lag.

Note that resonance factor Q_o increases with equivalent load resistance R. Indeed the higher the R is, the less the current absorption, and at this point the tank becomes a pure LC.

As a result, region 3 has a second order dynamic behaviour that makes compensation tricky.

Region 4

Consider now F_H of region 4:

$$F_H = F_M \frac{2U_O}{D} \frac{1-M}{2-M} \frac{1+s/\omega_z}{(1+s/\omega_{p1})(1+s/\omega_{p2})} \tag{4.20}$$

It presents a pole at low frequency:

$$\omega_{p1} = \frac{2-M}{RC(1-M)} \tag{4.21}$$

a pole at high frequency:

$$\omega_{p2} = \frac{R(1-M)}{L} \tag{4.22}$$

and the usual zero at frequency

$$\omega_z = \frac{1}{r_C C} \tag{4.23}$$

Overall, they lead to a 90 deg phase lag.

Summary

Region 1 is not problematic, since current loop forces the system to assume a dominant first order behaviour. However, a compensation ramp is needed to eliminate sub-harmonic oscillations. Region 2 and 4 are not problematic either, since the converter naturally assumes a first order behaviour, tied to DCM operation rather than the type of control. Nonetheless region 2 needs a compensation ramp to eliminate sub-harmonic oscillations inherited by the static instability due to PCM control, exactly like region 1. Region 3 instead represents a critical situation for stability since in it the converter shows a second order dynamic behaviour, that is even more accentuate for low output currents.

4.1.2 External loop compensation

Compensation on the external loop is actually the main compensation, since it is shared by all the functioning modes, and thus should suffice for all the dynamic behaviours of the converter, in all the operative regions. It is mainly made by acting on the parameters of the error amplifier and the voltage sensor transfer functions F_A and F_E, respectively.

Voltage sensor is basically a resistor divider with a by-pass capacitor and modelled by F_E which is this defined:

$$F_E := \frac{R_2}{R_1+R_2} \frac{1+sR_1C_1}{1+s\frac{R_1R_2}{R_1+R_2}(C_1+C_2)} \tag{4.24}$$

$K_E = \frac{R_2}{R_1+R_2}$ is fixed, because determines U_O since the error amplifier imposes $U_R - K_E U_O \approx 0$. So once either R_1 or R_2 is chosen, the other is set. A proper choice takes into account power consumption of the bleeding resistor $R_1 + R_2$ and the noise generated by it. C_1 is the key element that introduces a zero that can improve phase margin of T_R . Indeed, considering $C_1 + C_2 \approx C_1$ since C_2 is parasitic and the definition of K_E, F_E of eq. 4.24 becomes:

$$F_E = K_E \frac{1 + s/\omega_z}{1 + sK_E/\omega_z} \tag{4.25}$$

The bigger K_E, the more the distance between the frequencies ω_z and ω_z/K_E, and the more effective is the phase lead improvement at intermediate frequencies. Overall F_E introduces a null phase lag.

Error amplifier and compensation load on the other part are modelled into F_A, which is this defined:

$$F_A := G_1 * Z_C = G_1 R_p \frac{1 + sR_zC_z}{1 + s\left(\left(R_p + R_z\right)Cz + R_pC_p\right) + s^2R_zR_pC_zC_p} \tag{4.26}$$

plus an additional transconductance gain term G_2 for region 1 and 2 that produces a current type controlling reference for PCM. G_1R_p is the DC voltage gain of the error amplifier, mainly set according to the desired precision of the loop. Basically G_1 is related to the static consumption of the OTA whereas R_p to its topology.

For phase compensation, consider the elements Z_C is composed of.

C_p stands for parasitic capacitance and it cannot be varied. Actually, it should not be varied because it helps filtering high frequency noise, included F_s tone.

R_z and C_z introduce a zero that recover the phase lag of the first pole. A proper choice of C_z allows to increase the interval of frequencies for which phase lag is reduced to the minimum (see fig. 4.5). Overall, F_A introduces a 90 phase lag.

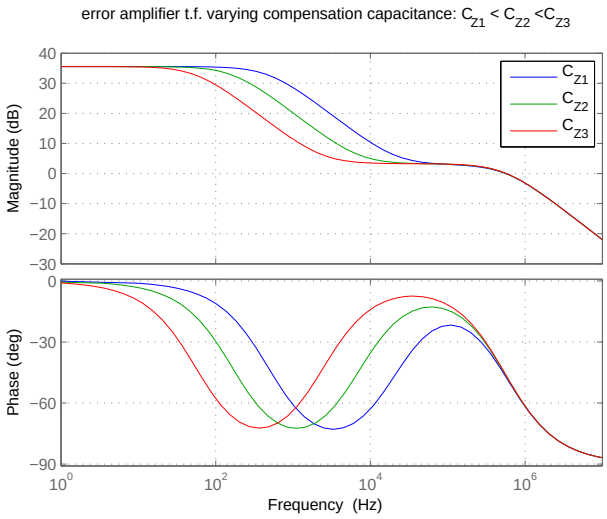


Figure 4.5: Error amplifier t.f. F_A varying compensation load capacitance C_Z

As anticipated, among the 4 regions of the converter and their respective dynamic behaviours, one is particularly critical from a stability perspective. Region 3 presents a resonance at RLC natural frequency that is not damped by a current loop. Therefore, compensation can be applied to the external loop, by:

- shifting the DC gain and thus the crossover frequency
- reducing phase lag on the surroundings of the crossover frequency.

An example of region 3 compensation is depicted in fig. 4.6.

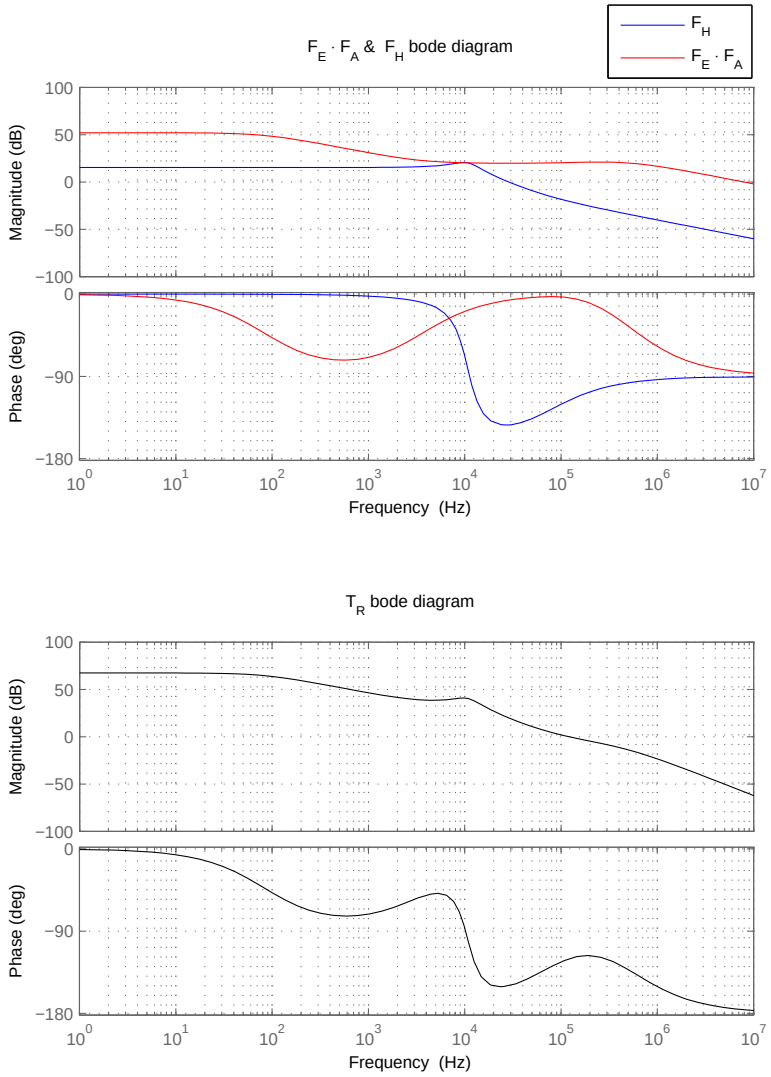


Figure 4.6: Example of F_H compensation in region 3.

4.2 Proposed Stability Tool

Finally, a stability tool is proposed to assist the designer during his design activity. This tool is provided with a graphical interface, made with the help of ®Guide which is a GUI maker in Matlab.

The appearance is given at the end of this section, but first the logical procedure to create it is presented, without entering in technical details. Basically procedure can be divided into 3 steps: data management, data processing and data visualisation.

Data management

Data management consists on arranging p_i, $i = 1, .., N$ parameters in a user-friendly data structure that is easily visualised and editable, like in fig. 4.2

All the parameters are put in rows numerically sorted, while in columns some fields like: *name*, *nominal*, *min* and *max* values, number of *points* to calculate in the interval min-max (if 1, then the nominal value is taken), *unit* and *scale* of measure, verbose

#	name	value	min	max	points	unit	description
1	U_I	3.3	2.7	7	10	V	battery voltage
2	I_O	1	0.001	3	10	$A[log]$	load current
3	U_O	1.2	1	1.5	3	V	load voltage
4	L_O	4.7	2	10	1	μH	filter inductance
5	C_O	22	10	100	1	μC	filter capacitance
6	R_C	40	20	100	1	$m\Omega$	filter capacitor resistance
...	...	...	...	...	...	...	...

Table 4.2: Data table containing all parameters

description.

Data processing

Processing converts the data structure into a N-dimensional matrix, which is more suitable for Matlab calculations, that is generated through the combinations of the parameters:

$$P =< p_1, p_2, .., p_N > \tag{4.27}$$

P has $\prod_{i=1}^{N} \overline{p}_i$ elements, that is the product of the column *points* of the data structure.

Now, for each element $p \in P$ a correspondent function $F(p)$ is calculated. Clearly the CPU time spent for calculations is proportional to the elements of P.

Data visualisation

Data visualisation consists in plotting a chosen function $f(p) \in F(p)$ into an xy graph.

These functions are mainly (for definition, see chapter 3):

- T_R overall regulation loop
- F_R reference to output transfer function
- F_1^{CL} audio-susceptibility or line rejection or battery to output transfer function
- Z_O^{CL} closed loop output impedance

For system stability, the function $f(p)$ of interest is T_R. For system performances, functions like F_1^{CL}, Z_O^{CL} ,F_R can be calculated as well. For all these functions, a suitable plot is the Bode diagram.

The proposed stability tool manages to plot multiple Bode diagrams of the aforementioned $f(p)$, for arbitrary $p \in P$.

Evaluating many of them at the same time is difficult, though. Evaluating a figure of merit instead of the whole function is more convenient since it is numerical and requires just a quick pass/fail check. Therefore for stability analysis the figure of merit to consider is the phase margin, which is extracted from T_R:

$$T_R \rightarrow \Phi_M \tag{4.28}$$

Φ_M is still N-dimensional and has to be plotted in a 2-d graph. A permutation is sufficient to choose which parameter is mapped into x and which into y, while the others into z axis.

$$\Phi_M(p_1, p_2, .., p_N) \xrightarrow{permutation} \Phi_M(p_x, p_y, p_{z1}, .., p_{z(N-2)}) \tag{4.29}$$

Now the N-dimensional matrix is broken into slices $f_{zj}(p_x, p_y)$ that can be mapped in a xy plan. Each point of $f_{zj}(p_x, p_y)$ is marked by a color, and in total there are $\prod_{j=1}^{N-2} \overline{p}_i$ slices. The result is a sliding coloured slice. At this point it is convenient to compress the slices pack along z through the *min* function, obtaining a worst case scenario. So, in formula:

$$\Phi_M \rightarrow min|_z \{\Phi_M\} = \Phi_{M_{worst}}(p_x, p_y) \tag{4.30}$$

Similarly to phase margin, crossover frequency can be evaluated in graphical way.

With a small add-on applied to the Matlab code, other figures of merit can be extracted from F_1^{CL}, Z_O^{CL} ,F_R and evaluated in a graphical way. For example the frequency of the dominant poles which determine the decay speed of their associated time responses.

Appearance

Finally the appearance of the stability tool is given, with an evaluation of the phase margin at varying battery voltage and output current as example. This example shows clearly the boundaries of the operative regions of the converter.

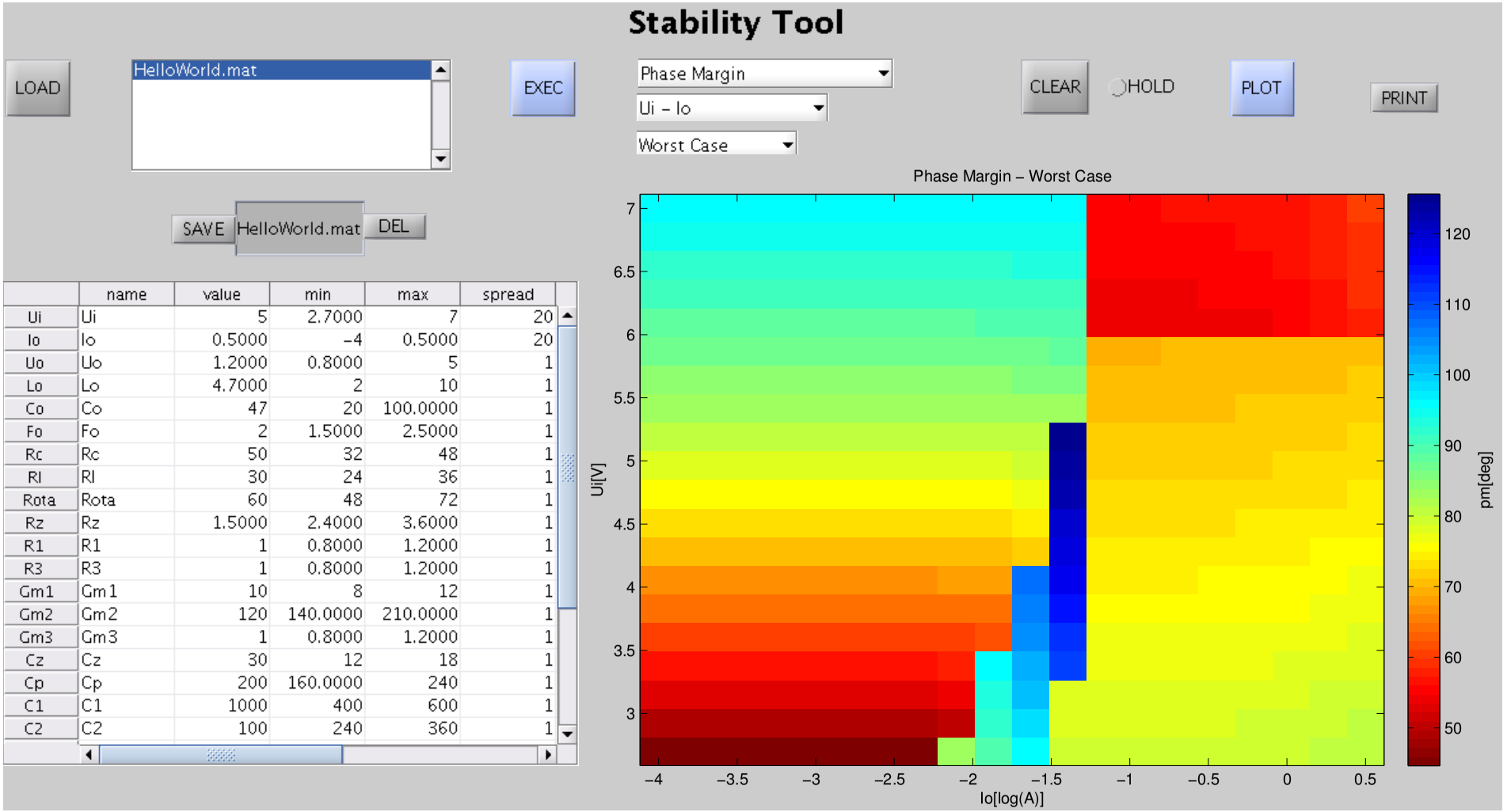


Figure 4.7: Proposed stability tool appearance

4.3 Parametric Optimization

The tool just created is used to visualize the space of parameters that guarantee stability. Parameters can be conveniently categorised in 3 groups:

Parameters categories

- Operative: U_O, I_O, U_I set up by environment. Also, the ultimate input variables of the system.
- Custom: L, C, r_C, F_s mainly related to LC filter and configurable by the customer.
- Design: various G, R, C, V that in the complex form the architecture of signals processing and are set up by the designer.

It is clear that parameters sensitivity is the critical aspect that the stability tool has to highlight.

Operative and custom parameters should have a as widest as possible variability range, since the wider the values range is, the less constraints for the customer and for the applications. Similarly, design parameters variation around the nominal values, due to process and mismatch of silicon lithography, should have as less impact on the functioning as possible.

For this purpose, an example of the use of stability tool is given, starting from specifications on the operative parameters, and adjusting the design parameters until a target on custom parameters is satisfactorily reached.

At the end of the day the tool does not make distinction between the 3 parametric categories since statistical deviation and deterministic interval of variability are treated as the same object, i.e. with uniform distributions.

Specs

- $U_O = 1.2\,V$
- $U_I \in [2.7, 7]\,V$
- $I_O < 3\,A$
- $F_s = [1.5, 2.5]\,MHz$

Target

- $L_O \in \{3.3, 4.7, 6.8, 10\}\,\mu H$
- $C_O \in \{22, 33, 47, 68\}\mu H$
- $r_C \in [30, 90]\,m\Omega$

4.3.1 Results and comments

Results as appear in the stability tool are reported in figure 4.8. The figure shows the $L_O \times C_O$ map across $r_C \times U_I \times I_O \times F_S$ space at the top, while the $r_C \times C_O$ map across $L_O \times U_I \times I_O \times F_S$ space at the bottom. First observation is that r_C plays a big role on phase margin since together with C_O it introduces a zero and a phase lead in the surroundings of the crossover frequency. This actually might be unwelcome, since it is hazardous to rely on a parasitic parameter to guarantee stability. Anyway, the lower the L value is, the wider becomes the area $C_O \times r_C$ and the more relaxed the constraint on the capacitor. If freedom on LC values is more preferred, then r_C must be $50m\Omega$ at least. Overall, results suggest the usage of big capacitors with not null ESR in the LC filter construction.

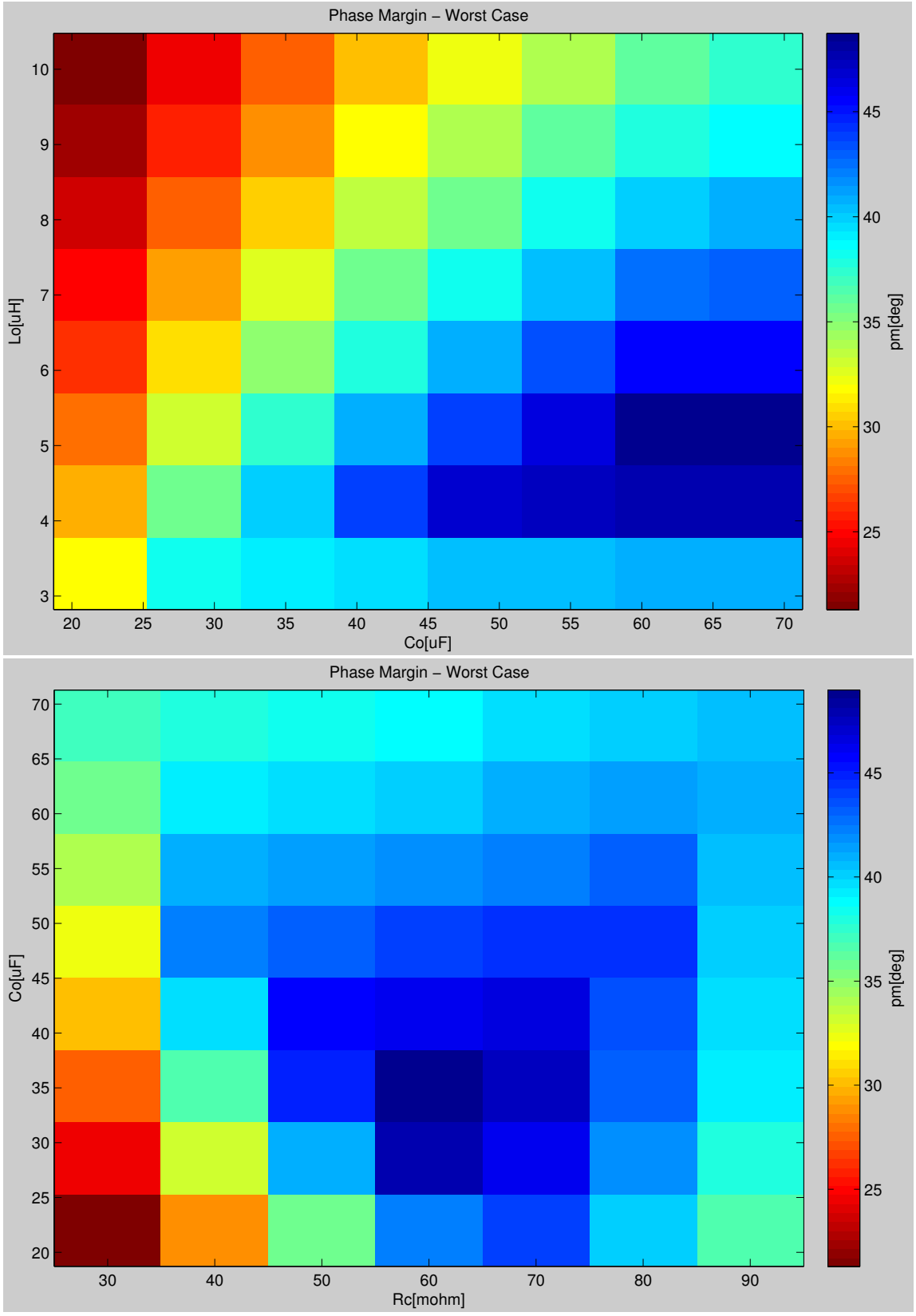


Figure 4.8: Phase margin map versus $L_O \times C_O$ (top) and $C_O \times r_C$ (bottom) parameters space in a worst case scenario overall produced by $U_I \times I_O \times F_s \times L_O \times C_O \times r_C$.

Chapter 5

Driver Stage Design

This chapter regards the design of the driver stage that interfaces the Buck power stage and its controller, including the implementation of some essential functionalities. At the beginning a theoretical analysis of energetic efficiency is made, trying to give once again a parametric panorama similarly to what was done for stability in chapter 4. In fact, focusing on the target of efficiency, some design choices and techniques to improve it are proposed. Finally, schematics at transistor level and some significant waveforms obtained by simulations are shown.

5.1 Efficiency

The switching cell presented in chapter 1 is obviously the ideal and lossless counterpart of a real half bridge, whose switches are actually transistors that consume power while being driven, while changing their state and while conducting.

For the power application considered in this thesis, CMOS devices seem to be adequate switches being able to convey a modest amount of power. With some adjustments on the channel length and consequently the supportable electric field, MOS derived from CMOS process can supply enough power to feed a micro-controller. On the contrary, in high voltage applications usually CMOS technology is not sufficient to realize switches and therefore DMOS or IGBT devices are used.

The half bridge that is about to be built, is composed of a pull up pmos transistor at the high side, that connects battery (VDD) to the switches output node SWO, and a pull down nmos transistor at the low side, that connects SWO to ground GND. Remember that this half bridge sees an inductor as load, which in turn can be modelled as a current generator since an inductance tends to keep its current flowing, having an high impedance in the short interval. Low side (LS) and high side (HS) transistors alternatively turn on for the correct current flowing phases, and in this case the half bridge is said to work synchronously. However, the LS transistor naturally has an anti-parallel body diode. Therefore when the LS body diode is crossed by the free-wheeling current and LS transistor is not, at this very moment the synchronism is broken and the half bridge is said to work asynchronously.

The post regulator dealt in this thesis is desired to work in synchronous mode for the as longest as possible time for efficiency reasons, since the body diode is parasitic and not designed to be as well conductive as the LS transistor.

In the following efficiency analysis, some parameters are about to be found in order to identify the origin of losses and related countermeasures. As anticipated, efficiency η of a switched mode converter, excluding losses of output LC filter, assumes this form:

$$\eta = \frac{P_O}{P_O + \underbrace{P_Q + P_{COND} + P_{DRV} + P_{SW}}_{P_{\text{LOSS}}}} \tag{5.1}$$

Each term is the average power lost in a period under steady state condition:

$$P = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} v(t)i(t)dt \tag{5.2}$$

Consider an a-synchronous (i.e. without LS transistor turning on) converter working at constant load current I_O and voltage U_O, with ideal LS body diode, i.e. with null voltage drop $V_D = 0$. Then, contributes composing eq. 5.1 calculated using 5.2 can be expressed each as a parametric function.

- $P_O = U_O I_O$ is the power transferred to the load.
- P_Q is the power overall consumed in idle mode (i.e. $I_O = 0$) by the controller
- $P_{DRV} \approx C_{GG} V_{GG}^2 F_s$ is the power consumed for driving the switch input capacitance C_{GG} up to voltage V_{GG}. The capacitance is not a constant though, so the relation is approximate but significant nonetheless because it states that P_{DRV} depends on frequency rather than timings.
- $P_{SW} = U_I I_O \left(T_{swON} + T_{swOFF}\right) F_s$ is the power consumed inside the switch during its transition from off to on state and vice-versa, and depends on both timings and frequency. Given $T_{swON} \approx T_{swOFF}$, then $P_{SW} \approx U_I I_O 2 T_{sw} F_s$.
- $P_{COND} = R_{ON} I_O^2 D$ is the power loss due to the limited conductivity of the switch. It depends on its duty-cycle rather than frequency.

Parameters

It is evident that battery voltage U_I, output current I_O, maximum driver voltage V_{GG}, switching timing T_{sw}, fundamental frequency F_s, switch input capacitance C_{GG} and minimum output resistance R_{ON} are the main parameters that determine efficiency.

In addition, power losses due to LS body diode voltage drop V_D and parameters related to LS transistor can be included for a more complete analysis of a synchronous half bridge. Note that V_D diode parameter intervene during diode conduction interval, denoted as T_D, which is also the overall dead time in a period of the half bridge. Temperature and process dependencies are not taken into account, but are included in the models of cad programs and therefore their effects are shown in simulations. Sufficient to know is that silicon resistances are strongly dependant on temperature. For example, a transistor R_{ON} can double its value passing from -40 to 150 ° C.

- V_{GG} determines the overdrive voltage $V_{OV} := V_{GG} - V_{th}$. The more the overdrive, the smaller the form factor has to be for the transistors to be well conductive, and less the area. For the application considered it fortunately coincides with the battery voltage $V_{GG} = U_I$. Nonetheless, some publications [13] show a segmentation of V_{GG}, and the controller dynamically selects the portion of V_{GG} allowing to reach the maximum point in the theoretical curve of efficiency.
- U_I is an operative rather than a design parameter, and the design is desired to be flexible for various battery voltages.
- I_O is the main operative parameter for which efficiency is evaluated, i.e. $\eta = \eta(I_O)$

- F_s has already been shown to being changed by adaptive modulation technique. PFM decreases frequency and those losses dependent on it, thus increasing efficiency, when P_O is low, i.e. at light load operation.
- C_{GG}, input capacitance, is mainly determined by the size of transistors, i.e. $C_{GG} \propto WL$, but is DC point dependant as later explained.
- R_{ON}, output resistance of transistors in ohmic region, is determined by its form factor and by overdrive voltage: $R_{ON} \propto \frac{L}{WV_{OV}}$.
- T_{sw}, switching on/off timing, is not trivial to be determined. This parameter needs a deeper analysis, as in the following.

The transient waveforms are the keys to understand which parameters determine T_{sw}. Consider T_{swON}, related to HS switch turning on thanks to a driver attached to its gate. In general the driver acts like a quasi-constant current generator I_{GG} apart from the very last period in which acts like a resistance. On the other hand, the load to drive is the capacitance C_{GG} seen at the gate, which is not constant though, as explained in the following.

A current generator I_O is attached to the drain node, which corresponds to SWO, to model the inductor, which indeed forces a constant current (ripple due to charging and discharging is neglected). Obviously when the HS is supposed to be interdicted, current forced by I_O flows in the LS free-wheeling diode.

Remember that differential voltages v_{GS} and v_{DS} sweep from minimum to maximum. $v_{DS} \in [0, V_{DD}]$ $v_{GS} \in [0, V_{DD}]$

Actually, $max\{v_{DS}\} = V_{DD} + V_D$, but body diode voltage drop is neglected in this analysis.

Four transitions are shown, and described in the following analysis.

$0 \rightarrow 1$ Before its turning on, HS mos is in interdiction zone ($v_{DS} = V_{DD}, v_{GS} < V_{th}$), then passes through sub-threshold zone and heads to the turning on zone (point 1 $v_{GS} > V_{th}$), while being driven by I_{GG}. Therefore, v_{GS} grows linearly with a slope

$$\frac{dv_{GS}}{dt} \sim \frac{I_{GG}}{C_{GG}} \tag{5.3}$$

with $C_{GG} = C_{GS} + C_{GD} \approx C_{OX}$. This transition requires an interval of time that contributes to form the overall T_D dead time.

$1 \rightarrow 2$ At the beginning of the turning on, mos leaves sub-threshold zone and enters saturation zone (point 1), while it is still driven by a I_{GG}. Therefore, v_{GS} grows linearly with an approximatively linear slope

$$\frac{dv_{GS}}{dt} \sim \frac{I_{GG}}{C_{GG}} \tag{5.4}$$

with $C_{GG} = C_{GS} + C_{GD} \approx \frac{2}{3} C_{OX}$. Although simulations show that slope is slightly inferior than one of transition $0 \rightarrow 1$. This transition lasts for the period T_{Irise}

$2 \rightarrow 3$ During the turning on, mos gradually passes from saturation zone into linear zone, crossing many DC curves between the two depicted in fig. 5.1. At this point, Miller effect intervenes and v_{GS} slope is approximatively linear

$$\frac{dv_{GS}}{dt} \sim \frac{I_{GG}}{C_{GG}} \tag{5.5}$$

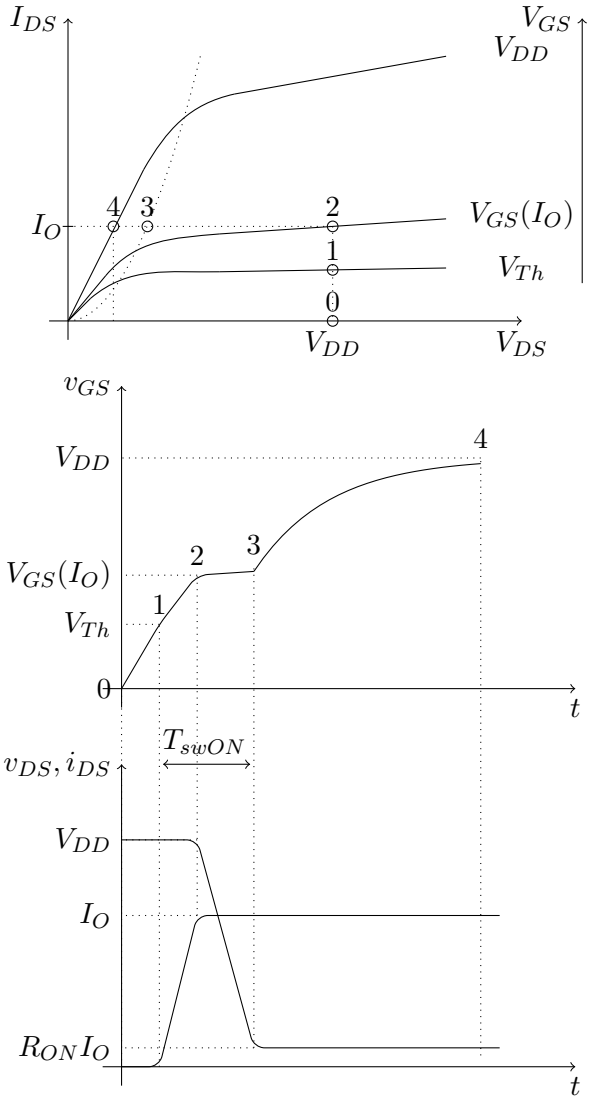


Figure 5.1: DC points and transient waveforms of a mos power switch, during off → on transition.

with $C_{GG} \approx C_{GS} + \mu_o C_{GD}$, where μ_o indicates the linearised intrinsic gain of a transistor, which depends on Early effect V_A and V_{OV} ($\mu_o = g_m \cdot r_o = \frac{2I_{DS}}{V_{OV}} \cdot \frac{|V_A|}{I_{DS}} = \frac{2|V_A|}{V_{OV}}$).

Because C_{GG} is much bigger than in the previous one, $v_{GS} \approx V_{GS}(I_O)$ is approximatively flat and thus this transition is called *plateau*, which lasts T_{Vfall}.

$3 \rightarrow 4$ Finally, just before reaching the point 4 of DC char, the driver acts like a resistance R_{GG} rather than a current generator and the decay assume an exponential form :

$$v_{GS} \sim \left(1 - e^{t/R_{GG}C_{GG}}\right) [V_{DD} - V_{GS}(I_O)] \tag{5.6}$$

with $C_{GG} \approx C_{GS} + C_{GD}$. This final timing is not so important because during this transition HS has already reached its maximum conductive capability i.e. $R_{ON} \approx \frac{1}{KV_{OV}}$.

It has been demonstrate that $T_{swON} = T_{Irise} + T_{Vfall}$ mainly depends on the driver strength I_{GG}. For HS turning off timing $T_{swOFF} = T_{Vrise} + T_{Ifall}$, the situation is symmetric: the driver that turns it off is a pull-up pmos, and the order of the transitions is inverted.

As far as LS is concerned, analysis is different because of the dead time period just before LS turning on. During dead time, LS body diode starts free-wheeling phase even before LS mos turns on and lowers down LS v_{DS} voltage drop. Therefore, *plateau* transition does not appear and T_{Vfall} is dependant on diode intrinsic dynamics rather than by the driver strength. Since usually $T_D > T_{Vfall}$, actually LS turns on when V_{DS} has already reached its minimum value, and does not speed up the timings significantly, since controls T_{Irise} only, or the speed with which it grabs all the current from the diode.

5.2 Half Bridge and Driver

Like stability, also efficiency is a multi-variate problem and a graphical tool comes in handy to see the effect of the overall parametric pool.

To maximise efficiency in all the operation, that is to get a flat curve of efficiency at varying output current, several methods have been conceived, more or less complex.

The methods proposed in this thesis, in addition to PFM already presented in chapter 1, are the segmentation of the half bridge into modules, the segmentation even of the driver into modules and the dead time control inside each driver module, in addition to the dead time control applied to each half bridge module.

5.2.1 Half bridge segmentation

Some assumptions or specifications act as constraints for the efficiency optimization and can be a good starting point to solve it. Two in particular are introduced:

- $R_{ON}I_O < 200mV$ for HS. Under this condition a given battery-to-load low-drop of $U_I = 2.7V \rightarrow U_O = 2.3V$ is possible, under worst case condition given by $I_O = 2A$ and $T = 150\,\text{deg}$ and assuming also a bonding resistance of $100m\Omega$.

- $R_{ON}I_O < 300mV$ for LS. Under this condition, LS body diode is unlikely to turn on during LS mos conduction, even if LS body diode is not accurately modelled so an assumption of its conductivity is made.

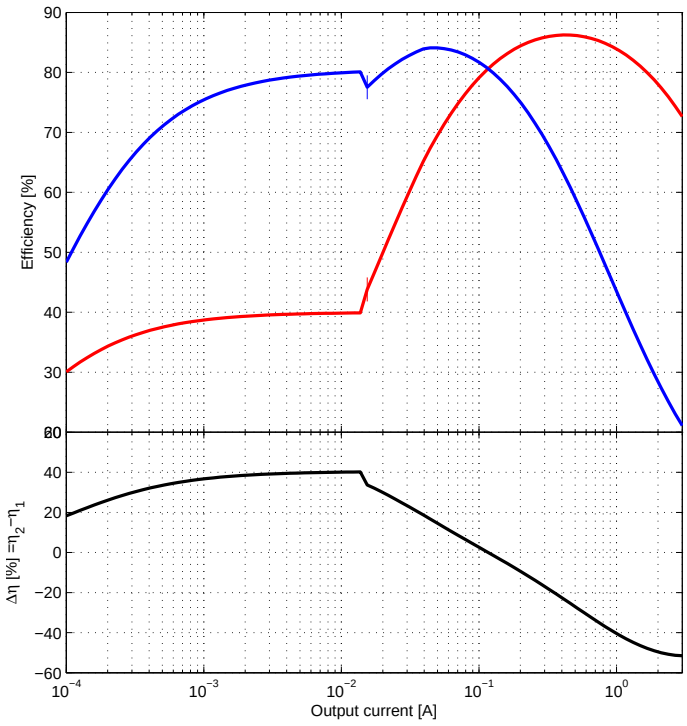


Figure 5.2: Theoretical efficiency curves of a SMPR with adaptive modulation and at varying the portion of activated half bridge modules: 100% (red); 5% (blue) .

These constraints determine a minimum size of the half bridge. Size can be adjusted according to particular requirements for maximum current flowing, where P_{COND} is dominant over other losses the main parameter to set is R_{ON}. At this point the above-mentioned graphical tool is very useful in this procedure because it can map η across load current I_O and for various dimensions of the half bridge. At this point the half bridge can be segmented so that each segment corresponds to a curve. A final size of R_{ONmin}, C_{GGmax} produces a curve that is good at heavy load, but bad at light load, since it leads to the maximum current capability but also to the maximum driver effort. The idea is to produce a curve that is optimal at light load, producing a small segment equal to $\frac{s}{100}\%$ of the half bridge that corresponds to $R_{ON} = \frac{R_{ONmin}}{s}$ and $C_{GG} = s \times C_{GGmax}$. Together with other typical parameters and the adaptive modulation technique, the half bridge segmentation 5/100% lead to efficiency curves depicted in fig. 5.2. Overall, half bridge is partitioned into three modules $\{HB_I\}_{I=1,2,3}$, to get an even more flat curve, and each one is selectable so that the half bridge can work at 5/50/100 % capability.

Each module is supposed to be dynamically selected according to the output current value in order to choose optimally the curve associated to a load. This operation of selection implies that an appropriate circuit senses the load current, processes the information contained in the sensed current, and finally makes a decision of the number of modules to activate, producing a selection bit vector $\{EN.HB_I\}$. This part has not been implemented, though.

5.2.2 Drivers segmentation

The half bridge modules just sized need a proper driver that injects current in their input capacitances each denoted as C_{GG}, one at a time. The driver for each half bridge

module is chosen to be a double inverter chain with an half bridge, i.e. a pull-up pmos and pull-down nmos, as output stage, as depicted in fig. 5.3.

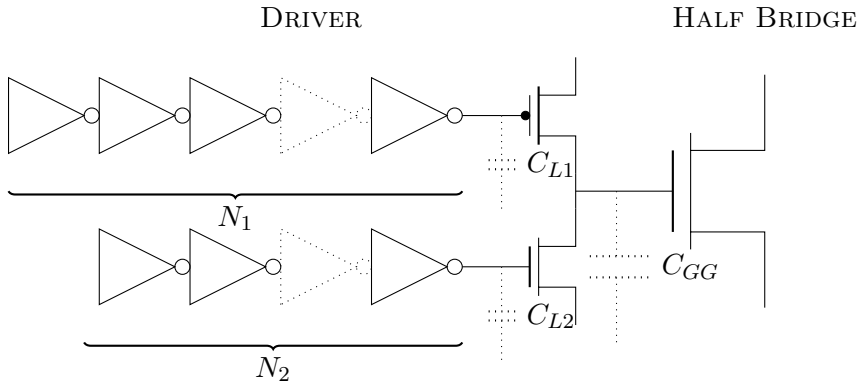


Figure 5.3: Driver inspection. Two inverter chains work as pull-up and pull-down buffers for an half bridge that is the output stage of the driver.

The pull-up and the pull-down are sized to supply an I_{GG} saturation current (that varies with V_{GG}, though) and they behave each as a load capacitances C_L with respect to the inverter chains that have to drive them.

For inverters chain sizing, there is a optimal rule [12] to follow and achieve minimal propagation delays when loading C_L. It involves an exponential growth of the N inverters, by a factor u that is chosen between 3 and 4. A proper choice of the pair $\{u, N\}$ also takes into consideration the wanted sign of the inverter chain $(-1)^N$ and the area $A \propto \sum_i^N u^i = \frac{u^N-1}{u-1}$. Also, $u = 3$ can be a good choice if modularity is an important aspect, because it can lead to replicated chains, plus one additional inverter applied to the pull-up chain ($N_1 = N_2 + 1$), that drives C_{L1}. Indeed the latter is approximatively 3 times bigger than C_{L2}, provided that pull-up and pull-down are sized to be matched in conductivity. This architecture allows to control the pull-up and the pull-down chains separately, allowing the tristate mode of the driver, which grants an high output (capacitive) impedance. Tristate mode is useful if a DTC also for driver stage is desired, and actually necessary if more driver modules are put in parallel, i.e. attached to the same output node, and are supposed to be enabled or disabled separately. Indeed, in addition to half bridge segmentation, also a segmentation into M drivers modules is proposed to control radiated/conducted electromagnetic emissions, that are important aspects for electromagnetic compliance (EMC).

In fact, the current absorbed by the power stage from battery has a trapezoidal shape, with lateral edges determined T_{Irise} and T_{Ifall}, that are in turn both determined by the "strength" of the driver I_{GG}. If the latter is segmented into M portions, then the pole of the spectrum of the trapezoidal waveform associated to the lateral edge of the trapezoid can be moved by a factor M as well. Number of modules is chosen to be $M = 3$, a compromise between EMC variability (half decade of pole shift) and efficiency constraints ($1/M$ of driver strength is likely to decrease efficiency if $M \gg 1$).

Similarly, the same effect is visible on the phase node SWO, whose fast moving can make the inductor behave like a radiating antenna and produce radiated emissions. Its moving is again modelled by a trapezoidal waveform, with lateral edge slopes determined by T_{Vfall} and T_{Vrise}, that are indeed modified by the driver strength, too.

Note that this EMC control is very basic and statical, i.e. the driver strength selection is done beforehand. More complicated dynamic EMC control involve the spread-spectrum technique applied to the duty-cycle modulation.

5.3 Logic of control

As seen, both half bridge and drivers are segmented. A controller is needed to select the desired modules and sub-modules, activating or inactivating them. Also, other important functionalities to implement are listed below.

- Dead Time Control (DTC) prevents the cross conduction that may happen in half bridges that work in synchronous mode. At the same time, it must ensure the shortest as possible dead time because the latter represents either a delay or a power loss. Three types of DTC are mentioned in order of complexity: fixed, adaptive and predictive.
  - Fixed dead time control sets a dead time that is fixed beforehand. Indeed since the control is open-loop, dead time is subjected by variability or ageing drift that are not correctable.
  - Adaptive dead time control, on the other hand, is a loop based control and is more likely to prevent cross conduction because of the sequentiality introduced by a feedback loop. Indeed adaptive DTC reads the state of the pull-up element before activating the pull-down one, and vice-versa.
  - More sophisticated dead time controls use a sort of prediction by means of a finite state machine that sets the length of the dead time according to the body diode conduction and past decisions.
- Current Sensing (CS) reconstructs the inductor. To save some pins, the current sensor is not applied in series with the inductor. Instead, current is reconstructed in partial periods, applying a sensor both on the HS and the LS switch. The HS-CS is needed for PCM loop, over-current detection and half bridge modules selection, while the LS-CS is not mandatory (unless a so-called valley peak control is implemented) but introduced because it can yield information both for zero cross and overload detection all at one time.
- Zero Cross Detection (ZCD) is another important functionality that prevents the inductor current flowing to ground across the LS switch. In other words, it breaks the synchronism of the half bridge and allows the DCM of the converter.
- Over-current (OVC) protection is self explained: it disable the HS switch when the amount of current flowing can lead to overheat and device damage.
- Over-load (OVL) protection is similar and complementary to OVC, since it must detect the very same event but at the load side, detectable when current is flowing current across LS switch.

To manage all these binary events (bits), a logic of control must be implemented. Imagine that a PWM controlling signal is given. Scope of the logic of control is to make a replica of PWM at the SWO node (see fig. 5.5), apart from the alterations due to dead time control and zero cross detection. Two preliminary choices related to logic circuitry design are made:

1. Usage of battery voltage to feed logic circuitry instead of a dedicated one: $V_{DD} = U_I$. The advantage is that no level shifters (both bottom-up $V_{DD} \rightarrow U_I$ and top-down $U_I \rightarrow V_{DD}$) to change voltage domain are needed. This choice makes things simple since level shifters are not trivial to design because of their latch-up nature. The first drawback is that propagation delays are widely dependant on battery voltage. The second drawback is that power consumption to drive

capacitances increases ($\propto V_{DD}^2$), but it can be neglected if compared to that of the buffers, that involve bigger capacitances (as seen, exponentially increasing towards SWO node).

2. Usage of elementary 2-inputs NAND/NOR gates (obviously in addition to NOT gates). The advantages are the modularity and the immediate identification of the fan-in and fan-out of the logic gates. Also, because in an elementary gate V_{DD} to GND path is crossed by 3 transistors at most, effects that have impact on propagation delay (e.g. making it more sensitive on the input configuration) like Body effect and intrinsic capacitances can be overseen. Therefore each logical relation is the composition of binary relations. The properties of distributivity, associativity and commutativity of boolean algebra reflect themselves into the length of the signal paths, because the N-input gate is converted to a N-children binary tree.

Synthesis example

Now an example of logical synthesis is made. Obviously, voltage levels are mapped into the field $\{0, 1\}$, i.e. $V_{DD} \iff 1$, $GND \iff 0$. Two equivalences, called *De Morgan* theorem, are reported because of their importance:

$$A = B \vee C \iff A = \neg(\neg B \wedge \neg C) \tag{5.7}$$

$$A = B \wedge C \iff A = \neg(\neg B \vee \neg C) \tag{5.8}$$

The properties of associativity, commutativity, distributivity of field $\{0, 1\}$ are commonly found in algebra books.

A verbal proposition like:

Low side switch of the first half-bridge module is on
if and only if
controller commands a duty-cycle off phase, high side switches of the HB modules are all off, there is no zero cross detection and half bridge module 1 is enabled

is translated into algebra syntax:

$$LG_1 = 1 \iff (PWM = 0) \wedge (HG_1 = 1) \wedge (HG_2 = 1) \wedge (HG_3 = 1) \wedge (ZCD = 0) \wedge (EN.HB_1 = 1) \tag{5.9}$$

where signals names are those of fig. 5.5. In particular, $EN.HB_1$ is a bit that sets the tristate mode for the half bridge module 1. Using truth table, it is shrunk into:

$$LG_1 = \neg PWM \wedge HG_1 \wedge HG_2 \wedge HG_3 \wedge \neg ZCD \wedge EN.HB_1 \tag{5.10}$$

Because of the driver structure presented, which has a separate control of the driver pull-up and the pull-down, the above becomes:

$$\neg LG_1.hg_1 = \neg PWM \wedge HG_1 \wedge HG_2 \wedge HG_3 \wedge \neg ZCD \wedge EN.HB_1 \tag{5.11}$$

With the further DTC loop of the driver, the above becomes:

$$\neg LG_1.hg_1 = \neg PWM \wedge HG_1 \wedge HG_2 \wedge HG_3 \wedge \neg ZCD \wedge EN.HB_1 \wedge \neg LG_1.lg_1 \tag{5.12}$$

In the opposite case (duty-cycle up phase, i.e. PWM=1):

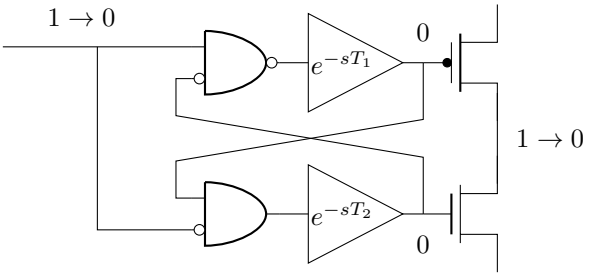


Figure 5.4: Simplified representation of dead time control.

$$\neg LG_1 = (PWM \wedge \neg HG_1 \wedge \neg HG_2 \wedge \neg HG_3 \wedge ZCD) \vee \neg EN.HB_1 \tag{5.13}$$

Note that the grouping between brackets recalls a correct usage of distributivity, otherwise some undesired issues can occur. Similarly, the driver segmentation imposes a new writing:

$$LG_1.lg1 = (PWM \wedge LG_1.hg_1 \wedge \neg HG_1 \wedge \neg HG_2 \wedge \neg HG_3 \wedge ZCD) \vee \neg EN.HB_1 \tag{5.14}$$

For hi-side switches $\{HG_I\}$, the relations are similar apart from the presence of the driver selection bits $EN.\{DRV_I\}$ which allows to enable the driver modules and allows the tristate mode for the driver module output stage when the driver is disabled. Also, other selection bits like OVL and OVC can intervene to avoid HG turning on.

At this point the properties of associativity, commutativity, distributivity allow to construct the binary tree starting from relations like eq. 5.14

An example on the typical waveforms related to the half bridge functioning after introducing the logic of control is depicted in fig. 5.7, where also dead time effect at node SWO can be seen. Introducing the dead time control also for the drivers (DTC2 loop), dead time is almost doubled, as shown in table 5.1. The quick explanation comes from fig. 5.4, that represents a simplified architecture of dead time control, when the controlling input is a square wave. Without the DTC loops (i.e. breaking the loops so that fed-back input at each port is floating, then setting it as the identity element of the binary operation associated to that port), the architecture would be very similar to a classic inverter, that is known to suffer from cross conduction. Provided that both delay times are approximatively the same ($T_1 \approx T_2$), there is a short dead time and a short cross-conduction according to controlling input transition (i.e. $0 \rightarrow 1$ or vice-versa). Instead with the logic ports, implementing the dead time control in a simplified way, the controlling input must wait for both the propagation delays of the the feedback path and the feed-forward path before having effect at the output. In this way cross conduction is avoided but propagation delay is increased. If two of this structure are nested each other, then the second (internal) DTC2 lead to larger dead time for the entire structure i.e. DTC1+2. In order to establish the convenience of DTC2, the amount of power spared thanks to driver cross conduction cancellation has to be compared to the amount of power lost due to half-bridge dead time worsening. It is not trivial to calculate the amount of power lost in cross conduction, under deviation around the nominal values of T_1 and T_2 especially due to distributed RC paths in the layout.

5.3.1 Results

$U_I[V]$	$T_{DTC1}\,[ns]$	$T_{DTC1+2}\,[ns]$
3	22	36
5	8	15
7	4	8

Table 5.1: Average dead times measurements in a switching cycle, for one (DTC1) and both (DTC1+2) loops enabled, at varying battery voltages.

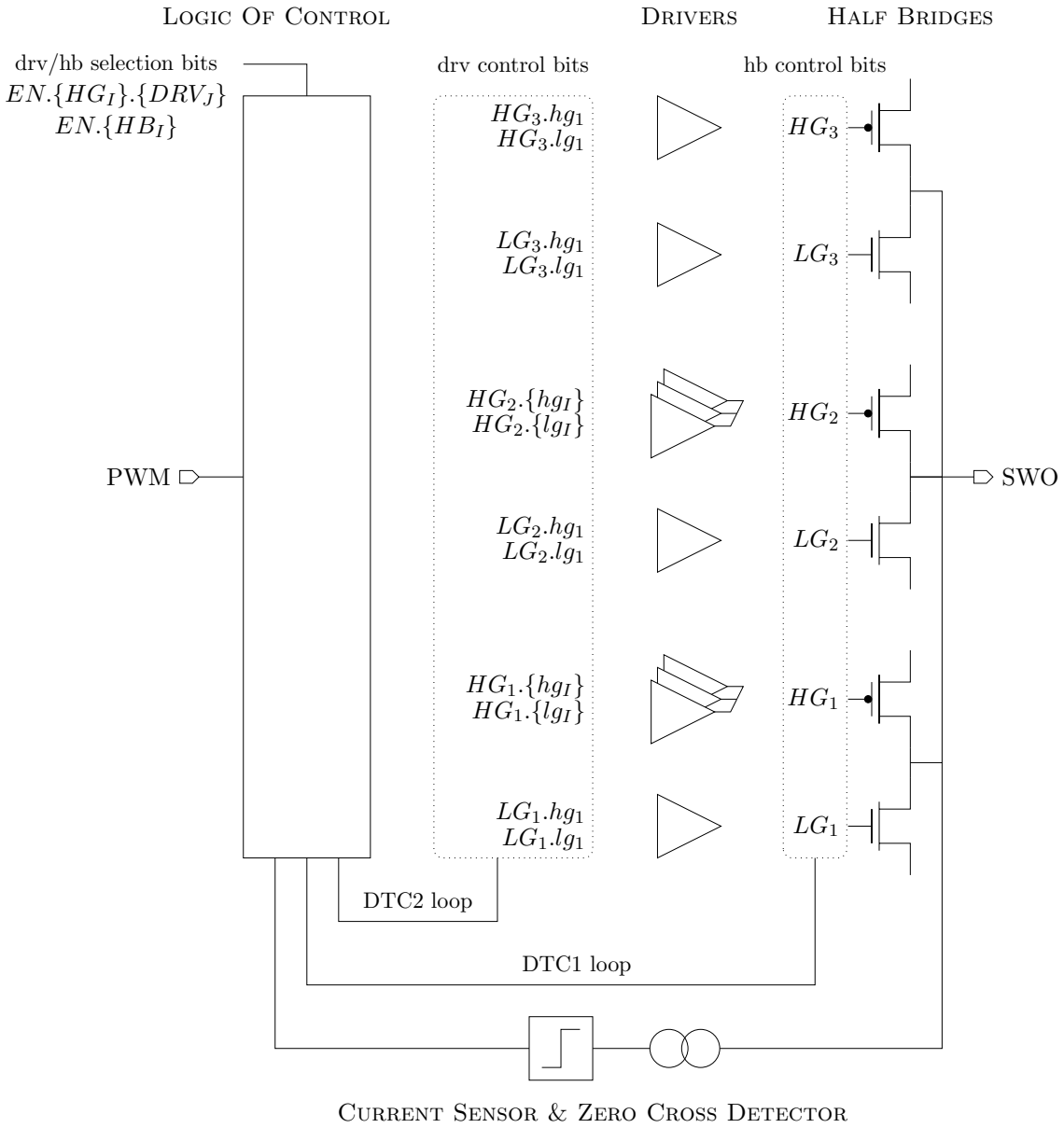


Figure 5.5: Overview of the driver stage functional blocks implemented. Significant signals for dead time control are grouped by dotted lines.

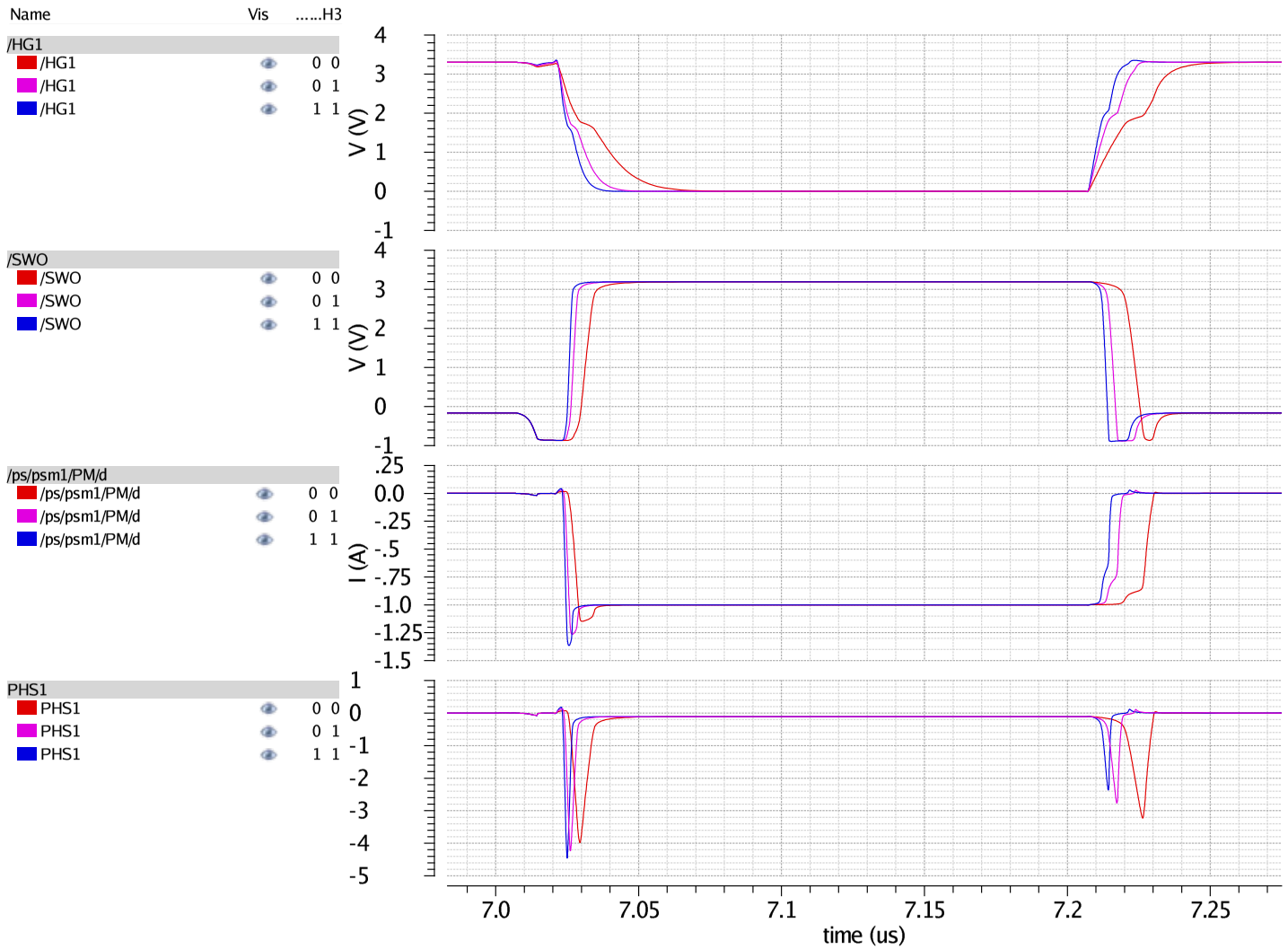


Figure 5.6: Waveforms related to the half bridge conducting phases at varying driver strength (100/66/33%)

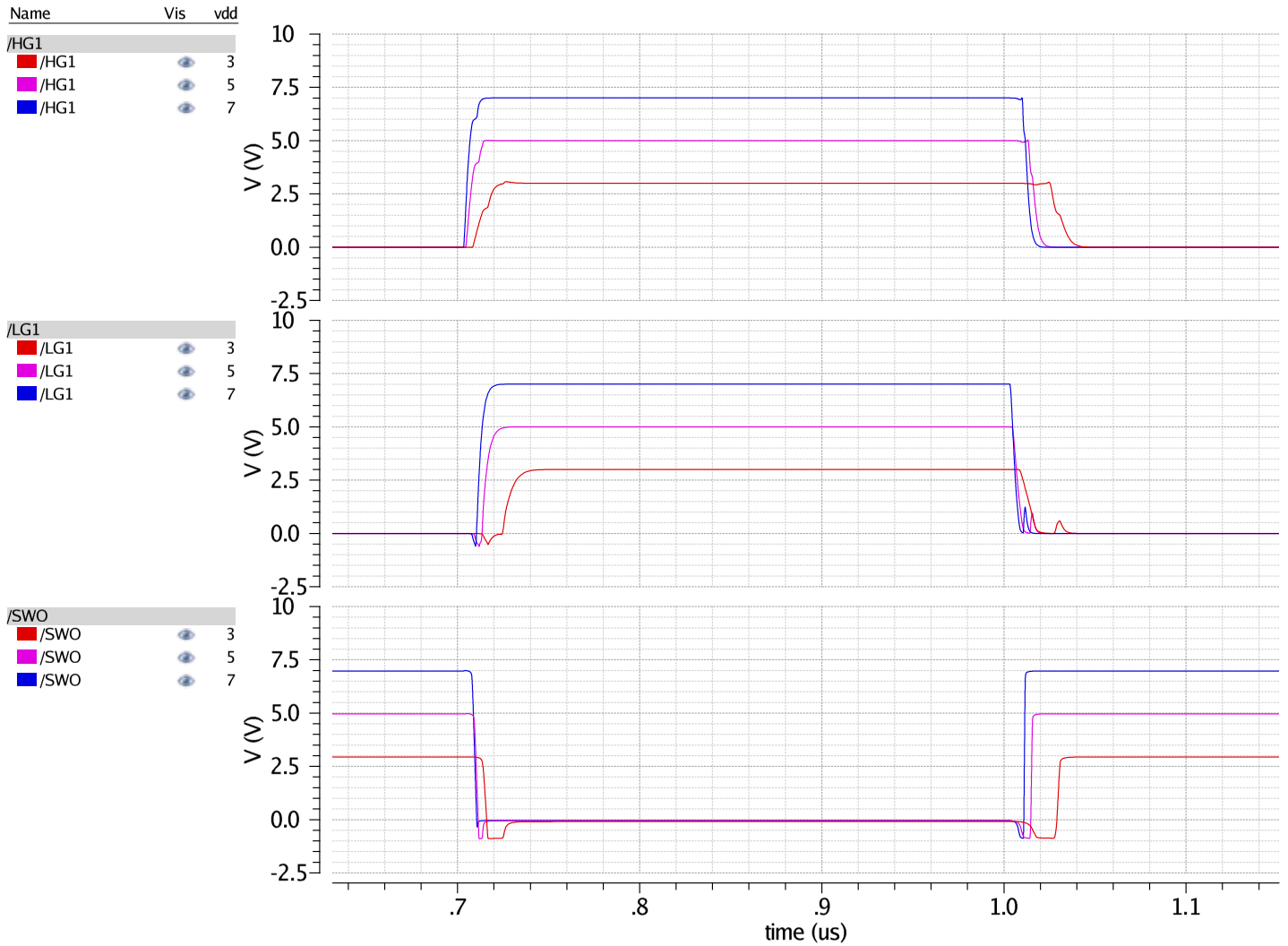


Figure 5.7: Waveforms related to the half bridge conducting phases at varying battery voltage (7/5/3V)

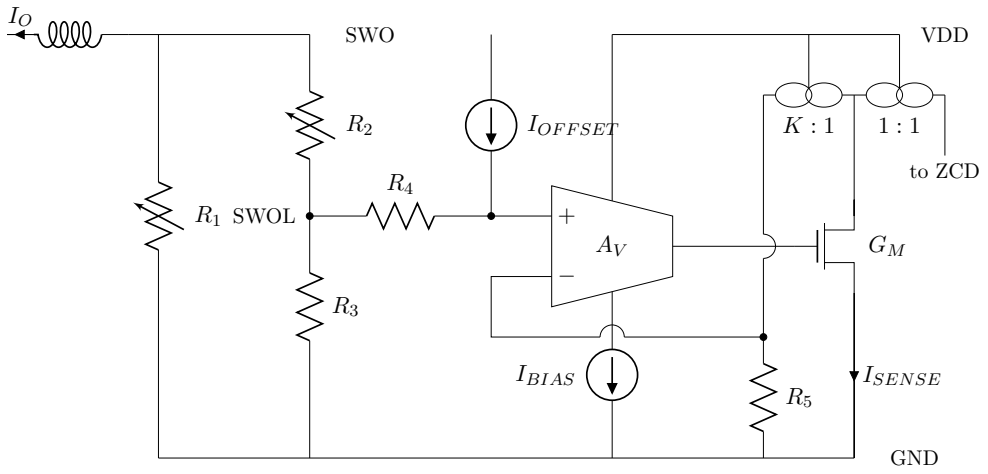


Figure 5.8: Low side current sensor schematic.

5.4 Current Sensor and Zero Cross Detector

This section concerns the design of the low-side current sensor and the zero cross detector, that overall allow automatic DCM for a synchronous Buck power stage. Low side sensor produces a scaled version of the current flowing across the low-side switch during free-wheeling phase. A particular topology is proposed that achieve good static precision against battery and temperature variation. Sensed current is compared to a given current reference by means of a simple current comparator, that once triggered produces the bit of zero cross detection ZCD. Similarly, the same comparator topology can be replicated to produce an overload detection OVL, provided a different current reference. ZCD signal is regenerated by a buffer and fed-back to the control logic presented in the previous chapter, in order to avoid LS turning on and allow DCM operation when current flows in the wrong direction. Finally, some simulation results are shown, and some considerations on the intrinsic flaws of the implementation are done, proposing future developments to improve it.

5.4.1 LSCS

Low side current sensor (LSCS) schematic is depicted in fig. 5.8, where resistances, current generators, the differential amplifier and the current mirrors are all made of mos transistors. In particular, consider this correspondence between transistors biased in linear region and their respective resistances $R_I \Longleftrightarrow M_I, \forall I = 1, .., 5$. LSCS comprises a current divider as input stage, then a feedback-loop structure composed of an OTA, a common source transistor and a current mirror. Overall, this last structure recalls a non-inverting configured amplifier stage.

In detail, the function of each element is explained.

- R_1 corresponds to the LS transistor. Since LS is segmented into 3 selectable cells, also R_1 is the parallel of 3 selectable transistors
- R_2 corresponds to a transistor that must be turned off at the same time of LS, to avoid waste of power (remember that SWO node reaches V_{DD} voltage). This is the reason why it must be a transistor. For matching reason under process variation (resistors and transistors have different temperature and voltage deviation coefficient), also other resistances must correspond to transistors.
- R_3 completes the resistor divider made by $R_{1,2,3}$ such that $V_{SWOL} = \frac{R_1 R_3}{R_1+R_2+R_3} I_O$.

- R_4 together with I_{OFFSET} produce a voltage offset V_{OFFSET} applied to SWOL node, making the differential amplifier work.
- R_5 is the resistor that sees the injection of KI_{SENSE} and produces a voltage drop to feed-back to the inverting pin of the differential amplifier.
- A_V drives G_M to produce a I_{SENSE} such that$V_- = R_5 K I_{SENSE}$ tries to follow $V_+ = V_{SWOL} + V_{OFFSET}$, because of the negative feedback configuration.
- I_{BIAS} supplies A_V
- current mirrors $1 : K$ and $1 : 1$ provide a scaled version of I_{SENSE}, to feed-back to the loop and to feed-forward for the comparator, respectively.

For sufficiently high A_V and at low frequency (i.e. neglecting parasitic capacitances) the virtual ground is applicable, and this approximate relation is valid:

$$I_{SENSE} \approx -\frac{1}{K}\frac{R_3}{R_5}\frac{R_1}{R_1+R_2+R_3}I_O + \frac{[R_3||(R_1+R_2)]+R_4}{R_5}I_{OFFSET} \tag{5.15}$$

The target for the moment is a precise DC characteristics. The relation expressed in eq. 5.15 shows that the precision is mainly given by ratios of resistances $\{R_I\}$, the mirroring ratios and the precision of I_{OFFSET}, while A_V and G_M have less impact on static precision.

R_3 is chosen to be small in order to soften Body effect of transistors M_3 and M_4 but especially overdrive voltage mismatch of M_3 with other transistors. So, relation $R_1 \ll R_3 < R_2$ leads to a further approximation of eq. 5.15:

$$I_{SENSE} \approx -\frac{1}{K}\frac{R_3}{R_5}\frac{R_1}{R_2}I_O + \frac{R_4}{R_5}I_{OFFSET} \tag{5.16}$$

Current mirrors $K : 1$ is configured as cascode in order to get an high output impedance and thus less influence by their load. Indeed, there is a natural mismatch between the loads R_5 and G_M, since respective transistors work in different operative zones. Overall, LSCS presents a precise characteristics along with battery and temperature variation, as suggested by fig. 5.9. The implementation is not ultimate though, because the current-current gain is quite low ($\sim \frac{100nA}{1A} = 10^{-7}$), and therefore low signal-to-noise ratio is expected. Limited gain or, equivalently, limited output headroom is the price for a pretty linear characteristics.

5.4.2 ZCD

Now that a current sensor has just been created, it is time to make a current comparator that triggers events according to the sensed current. Provided that a precise I_{REF} is available, it is not difficult to create a comparator that compares it with I_{SENSE} and trigger in correspondence with $I_{SENSE} = I_{REF}$.

A zero cross detector schematic is depicted in 5.10.

Low side current sensor and zero cross detector in cascade produce a DC characteristics (fig. 5.11) that is strongly dependant on V_{DD}, because the comparator created inherently has a low battery rejection, being not a differential structure. Therefore, for this but also for other reasons later explained, the implementation needs an overall improvement, for example using a dedicated battery.

At this point the LSCS+ZCD structure are connected in closed loop with the half bridge, the drivers, and the control logic in order to study the overall dynamic behaviour.

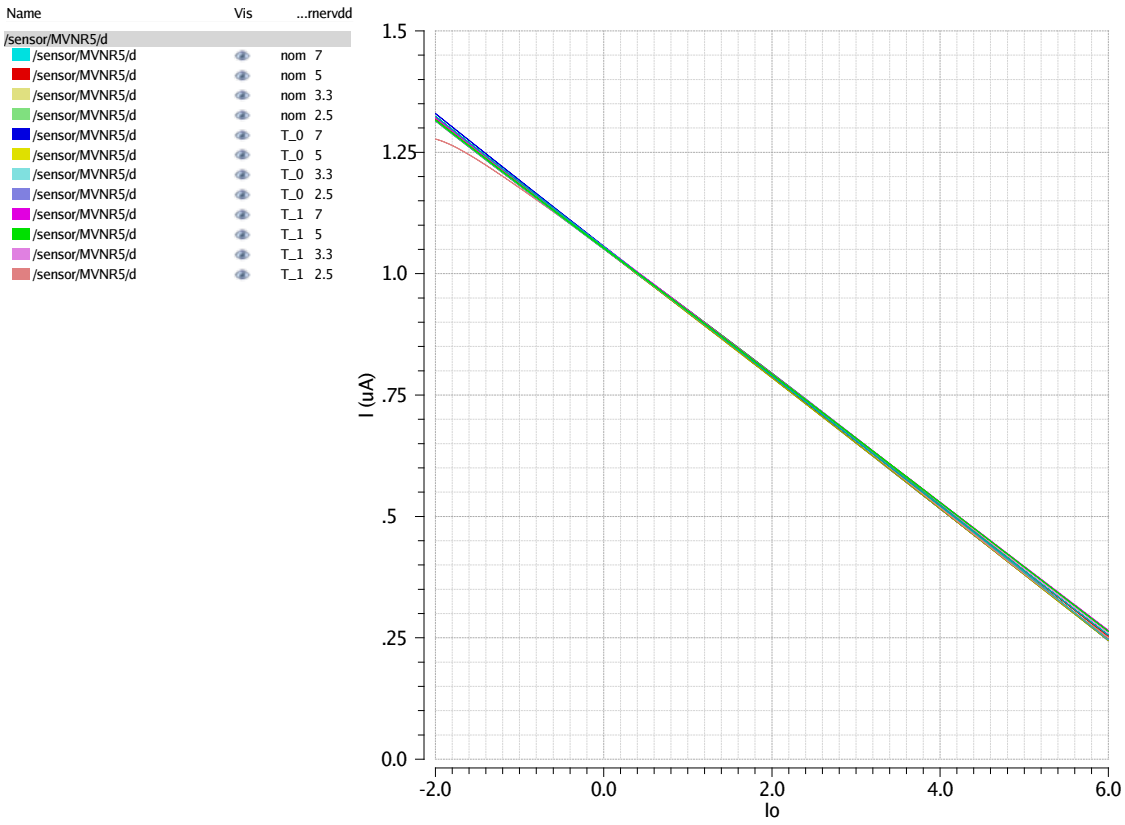


Figure 5.9: Low side current sensor DC characteristics at varying battery voltage and temperature.

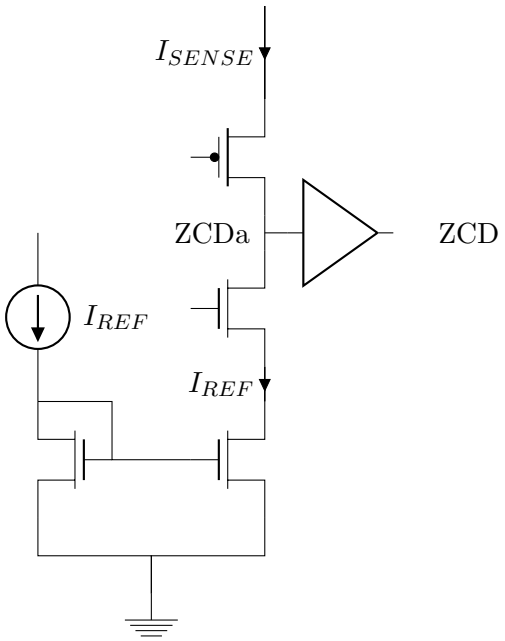


Figure 5.10: ZCD schematic

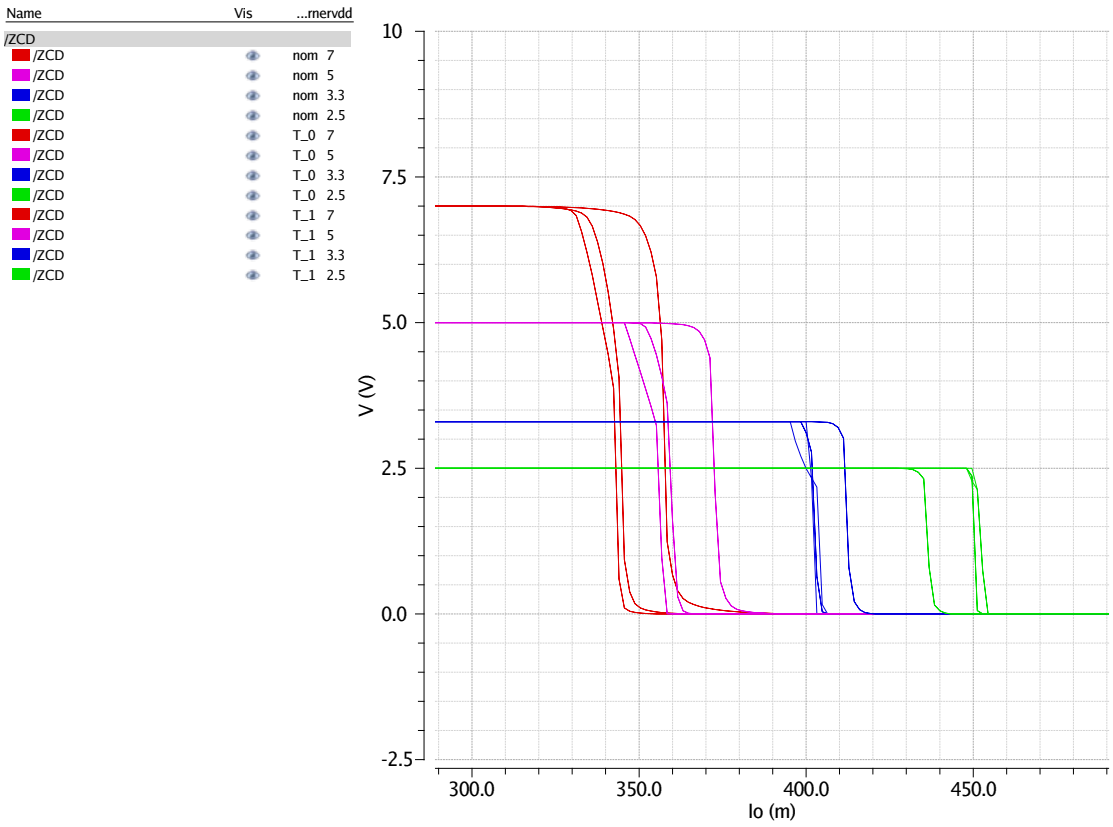


Figure 5.11: Low side current sensor and zero cross detector DC characteristics, at varying battery voltage and temperature.

Also the main external regulation loop, built with an ideal PWM modulator, is introduced in order to reach a configurable point of load U_O. In this manner the parameters U_I,U_O,L_O,I_O can be changed and set up different situations. For example, changing U_I, L and U_O allows to set up inductor current slopes.

5.4.3 Results and issues

The main objective, that is introducing DCM operation, is verified by simulations. Also the phenomena of energy bouncing between the capacitance at node SWO C_{SWO} and the inductance L_O, in the form of a resonant waveform i_L, is observed. Although, some issues affect the desired results:

- DCM is bound to asynchronous mode (top fig. 5.12). In fact, ZCD enters state 1 correctly, activating DCM operation, but does not leave that state from that moment onwards. Therefore, during free-wheeling phase of each cycle the half bridge works with the LS body diode instead of the LS switch.
- Back-powering, i.e. wrong direction of the inductor current, when current is steep at falling slope. (bottom fig. 5.12)

They are both caused by the finite responsiveness of the zero cross detection. A possible solution to these problems is increasing I_{SENSE} (and consequently I_{REF}) by a factor H. In this manner, the node $ZCDa$ moves faster in turn, along with ZCD, by a factor H. This operation can be done to the current mirrors mirroring ratios or the the ratio of the resistances of the LSCS.

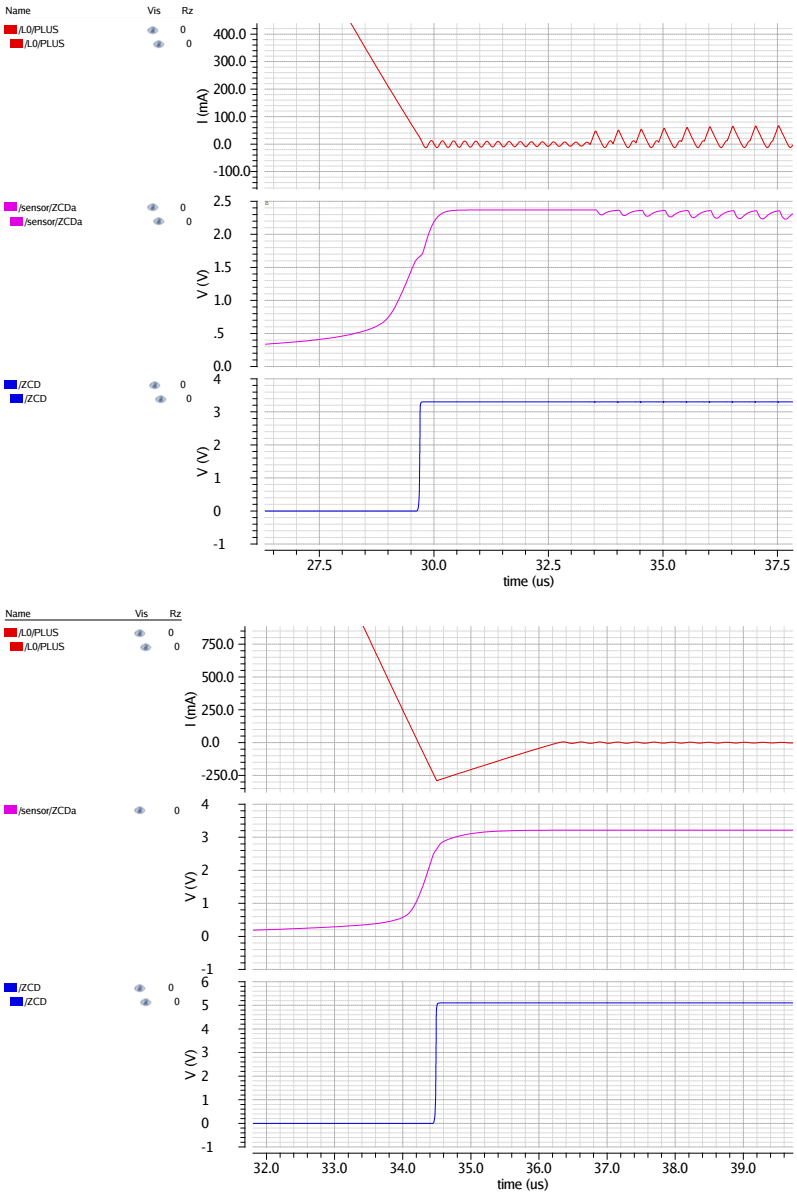


Figure 5.12: Example of correct zero cross detection, but undesired permanence of ZCD state (top). Example of flawed zero cross detection that causes wrong current flow for a certain interval of time (bottom).

Conclusions

In synthesis, this thesis has presented some theoretical results that underlie the problems of stability and energetic efficiency of a Buck switched mode converter, and has shown solutions that are commonly adopted, some at the state of art. The thesis work gives a practical contribute on solving stability issue and proposes a partial circuitry implementation of a converter driver stage given a particular point of load for a post regulation application.

More in detail, the Buck converter concerned achieves peak current mode control and adaptive modulation technique, and has been parametrized in its fundamental functioning to form a system of mathematical equations. Then, an operative DC map and a small signal model have been produced, using the steady state averaging technique and following guidelines found in several academic publications. Such a model, supposed to simulate the averaged quantities of the system, has been successfully validated comparing its time responses with those of a purposely made instantaneous model. In this manner, the small signal model is likely to give useful information about dynamic behaviours and, in particular, criteria for stability. Indeed, to conclude the modelling activity, the results obtainable by such model are put into a graphical user-friendly interface tool to support the designer during parametric optimizations and customizations that ensure stability at the same time.

The last part of the work aimed to design some circuitry parts of the regulator driver stage, in particular the half bridge, the drivers, the logic of control and the zero cross detector. Starting from graphically evaluable theoretical efficiency curves, an adequate sizing of the power switches that form the half bridge is proposed, together with their partitioning into sub-modules. Then, associated drivers are built and provided with a modularity that allows a basic control of electromagnetic conducted emissions. Finally, a functional circuitry of a current sensor is built together with a comparator to detect zero crossing and allow the correct functioning of the converter. Obviously the proposed circuital implementations, especially that related to the zero cross detection, are not ultimate and require further improvements.

Future developments include a deeper analysis of the zero cross detection, and consequently design improvements on the circuitry dedicated to this functionality. Then, some circuital topologies can be replicated in order to introduce missing functionalities and overall obtain a complete driver stage. Eventually, theoretical efficiency curves can be compared to the ones found in simulations, for completeness of analysis.

Appendix A

Typical Step Response

This appendix shows the preliminary work of the modelling activity, described in chapter 3, in which many time responses of a Buck system were evaluated. Nonetheless, the following considerations are general and not bound to the particular system.

Consider a single-loop T block diagram where a is the controlling (usually the reference) input and b is a secondary input (usually a disturbance) injected in another point of the loop. c is the evaluated output.

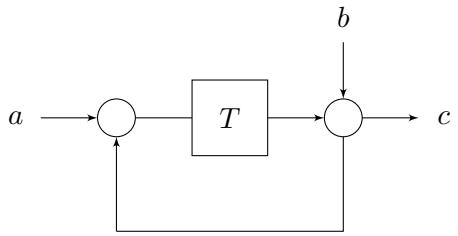


Figure A.1: Typical points of injection in a closed loop system.

For typical cases, T assumes this form:

$$T := \frac{Q\omega_o}{s}\frac{1}{1+sQ/\omega_o} \tag{A.1}$$

Input a transfers to c, seeing a low pass filtering:

$$L = \frac{T}{1+T} = \frac{\omega_o^2}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{A.2}$$

Input b transfers to c, seeing an high pass filtering:

$$H = \frac{1}{1+T} = \frac{s(1+sQ/\omega_o)}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{A.3}$$

Time responses can be extracted starting from the closed loop system t.f. L and H and applying Laplace anti-transform.

Graphical evaluation of T, L, H, at varying Q (and consequently phase margin Φ_M) are reported in fig. A.2.

It can be demonstrated that similar results are obtained starting from a slightly different T:

$$T' = \frac{{\omega_o}^2}{s^2}\left(1 + \frac{s}{Q\omega_o}\right) \tag{A.4}$$

$$L' = \frac{T'}{1+T'} = \frac{\omega_o^2\,(1+s/Q\omega_o)}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{A.5}$$

$$H' = \frac{1}{1+T'} = \frac{s^2}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} \tag{A.6}$$

This analysis shows typical time responses of systems L and H, obtained for a quite simple realization of system loop T. Such responses have a brief-period speed dependant on F_C while having the very same long-period recovery time. With respect to the system concerned in this work, L corresponds to the reference-to-output F_R, whereas H to either the closed-loop output impedance Z_O^{CL} or to the line rejection F_1^{CL}, both seen as disturbances, while T correspond to the regulation loop T_R.

The correspondence is approximately valid for typical cases. Although, it can be demonstrated that a further low frequency zero ω_z applied to T_R can show up as a dominant pole in Z_O^{CL} and determine its timings, while in F_R it does not have significant influence.

As consequence, when ω_z is present, high F_c does not necessarily mean short recovery time from a disturbance stimulus.

Designer must keep in mind this fact because it can be experienced in a Buck converter, where a DCM system can have the very same line/load jump recovery time of a CCM one, despite having a far lower loop crossover frequency. For example two systems may have with different $F_{c1} = 250KHz \ll F_{c2} = 20KHz$) but quite the same full recovery time ($\sim 120\mu s$) of their load-jump time responses, as shown in fig. A.3.

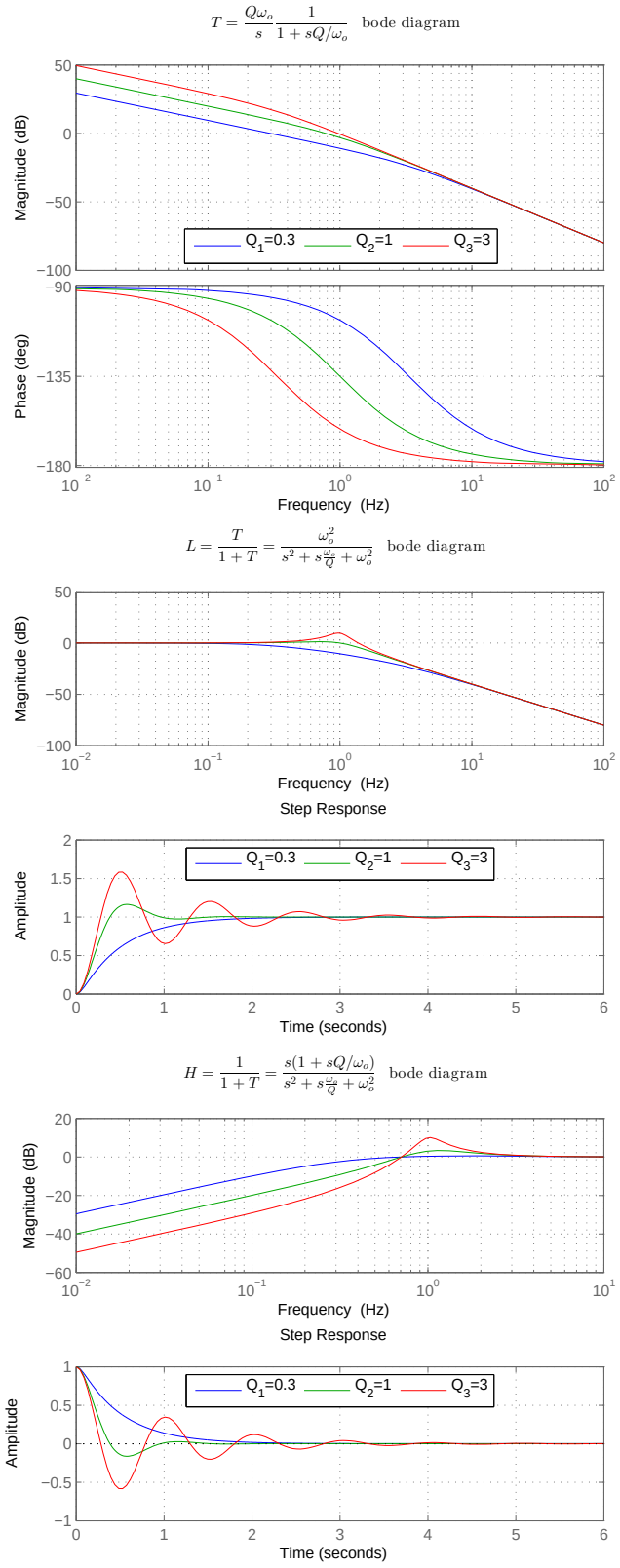


Figure A.2: Bode diagrams and correspondent step time responses of systems that are typically similar to Buck response to reference and disturbance stimuli.

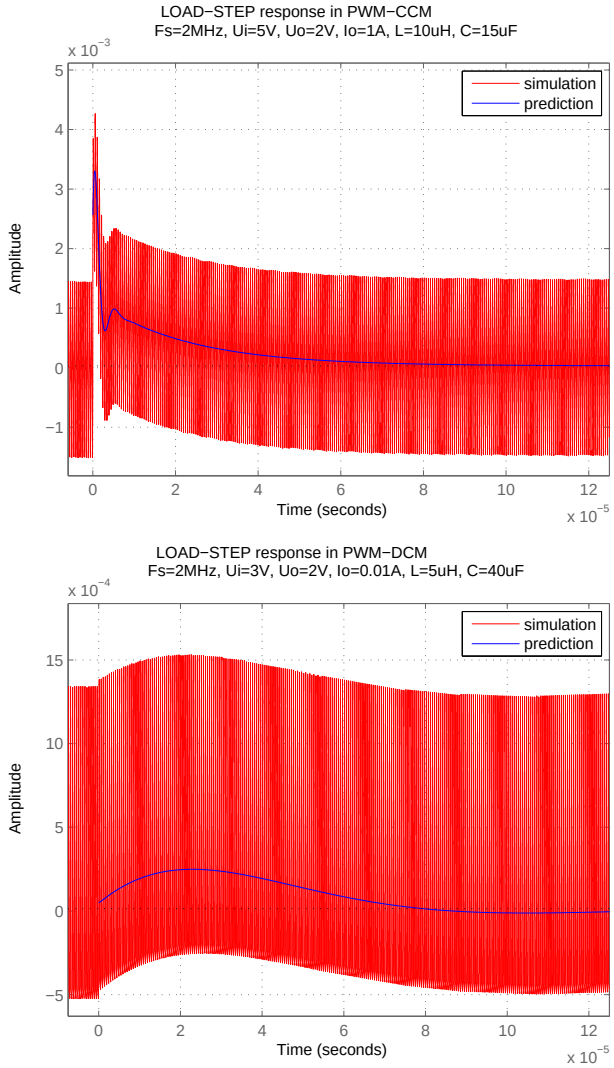


Figure A.3: Example of $F_c \leftrightarrow BW$ misconception. Two Buck systems may have very different crossover frequency but quite the same recovery time at load-jump response.

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