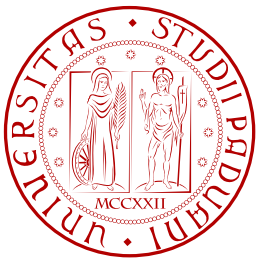

Università degli Studi di Padova

SCUOLA DI INGEGNERIA

Corso di Laurea Magistrale in Ingegneria Elettronica

Tesi di laurea magistrale

Design of Programmable Phase Shifters and Attenuators in 130nm CMOS Technology

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To my family

Abstract

This thesis proposes the analysis and design of two important circuits, often used in radio frequency (RF) systems: the phase shifter and the programmable attenuator.
The control of phase and amplitude of signals is important in many applications. Phased arrays, an example of adaptive antenna systems, base their operation on phase shifters to electronically steer the beam and obtain an overall antenna with a programmable radiation pattern. Another example is the Doherty Power Amplifier (DPA), an architecture often used in nowadays cellular base-stations. Phase and amplitude control circuits are used in DPA systems to optimize its efficiency.
The thesis starts with an introduction chapter which presents more in detail phased array and DPA systems and explains how they can take benefit from circuits like phase shifters and attenuators.
The core of the work is represented by the second and the third chapters which present the analysis and design of, respectively, a phase shifter and an attenuator for DPA application, using the Infineon 130nm CMOS technology. The respective chapters start with an overview of the possible solutions and continue with a detailed analysis of the differential π-network topology, which has been chosen for both phase shifter and attenuator. The final parts describe the design procedure.
After a brief description of the full-custom layout, the thesis concludes with the presentation of the simulation results, including parasitic extraction. In particular the two blocks are realized using only passive elements and cover the frequency band from $1GHz$ to $3GHz$. The phase shifter shows an insertion loss of $1.8dB$ and a delay range of $76.5ps$ ($52°$) at $2GHz$. This result

is obtained with an average step of $4.8ps(3.25°)$. The attenuator shows an Insertion Loss (IL) of $1.3dB$ and an attenuation range of $15.2dB$ at $2GHz$. This result is obtained with an average step of $0.49dB$.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Phase shifters and attenuators are important RF building blocks used in different kind of systems. The aim of this chapter is to explain their usefulness through some practical applications.
Afterwards, the goal of this work is presented, that is the target specifications for the design of the two circuits.
The chapter concludes with the recall of some basic concepts which will be often used in the rest of the thesis for the network analysis.

1.1 Applications

Phase shifters are circuits able to introduce a controllable phase shift in a signal path. Probably its major use is in adaptive antenna systems where they allow to control the phase of each path and change the radiation pattern of the overall antenna system([9]).
Programmable attenuators, instead, are circuits which permit to control the amplitude of a signal lowering its amplitude. They are required in a variety of applications such as the automatic gain control of transmitter/receiver systems, amplitude weighting in phased-array radars and temperature compensation of power amplifiers ([41]).
To get more insight about these blocks two applications are presented in this section, that is phased array and Doherty Power Amplifier systems. In the

former they are used to electronically steer the beam of the multiple antenna system, increasing hence the overall antenna gain. In the latter, instead, they are used to calibrate the amplifier, allowing hence an efficiency optimization.

1.1.1 Phased Array

Antennas are key components of any wireless communication system. In the transmitting process, these devices permit the transmission of an electrical signal in the form of electromagnetic radiation. This radiation propagates through space and can be received by other antennas which in this case do the reciprocal process, that is turning an electromagnetic wave into an electrical signal which can then be elaborated by the processing circuits.
The dipole antenna is the simplest and probably the most used type of antenna. It consists of two identical conductive elements which are usually bilaterally symmetrical. However, its simplicity results also in limited performances. For example, once the length of the antenna has been set, also the current distribution on it is set, which results in a fixed radiation pattern that cannot be changed any more [7].
To overcome this limit and enhance system performance a solution, which is often used in practice, is the multiple antenna system. These systems are often made of different dipole antennas, arranged in a determined manner and fed by independent currents. By a proper choice of the number of these elements, the geometry and the excitations, it is possible to obtain a variety of radiation patterns.
A special case of such systems is the adaptive antenna([9]). In a receiver, for example, the primary function of any adaptive antenna system is to maximize the received power from one particular direction while suppressing undesired signals coming from other directions. From the transmitter side, instead, the task is to focus almost all the irradiated energy in a determined direction. This concept can be represented by the radiation patterns shown in figure 1.1. Here it can be seen that an adaptive antenna is able to change its radiation pattern and hence to steer the beam in the desired direction. The steer of the beam can be realized both mechanically and electronically.

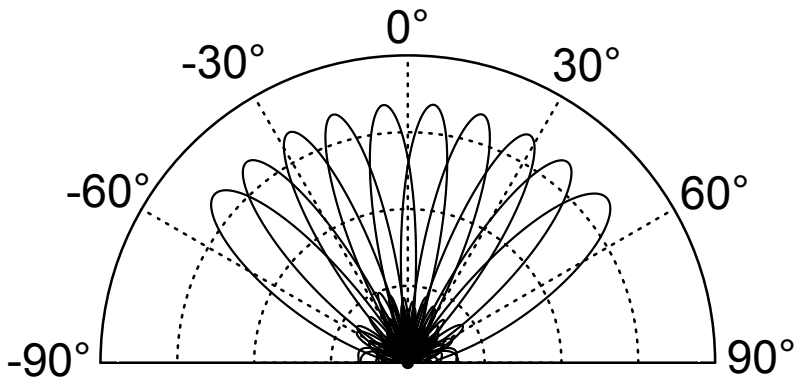


Figure 1.1: Adaptive antenna concept. Beam steered from $-50°$ to $50°$

An example of an adaptive antenna system, where the beam steering is done electronically, is the phased array configuration. Basically, the phased array antenna is composed of a group of individual elements, which are distributed and oriented in a linear one(or two)-dimensional spatial configuration. The amplitude and phase excitations of each element can be individually controlled to form the desired radiation pattern. The beam steering is controlled electronically by adjusting the phase of the excitation signals at the individual elements. This task is accomplished with the antenna aperture remaining fixed in space without the involvement of mechanical motion.
To get more insight about these systems, a complete block diagram of a phased array receiver is reported in figure 1.2. For a deeper analysis see [8]. It is worth to notice that all the considerations which will be hereafter made are also valid for the transmitter. In this example, the system is made by a linear antenna array composed by N equally spaced antennas. For simplicity, it is supposed that every antenna is followed by a programmable attenuator and a phase shifter; in practical applications also a low noise amplifying stage is typically present. The attenuator is usually used to correct the amplitude errors between the various paths, which are inevitably present due to manufacturing variations and design techniques. The phase shifter is used instead to realign the signals from the various paths, considering that the electromagnetic wave arrives in different time instants on each antenna. The output signal is finally obtained summing together the contributions of each

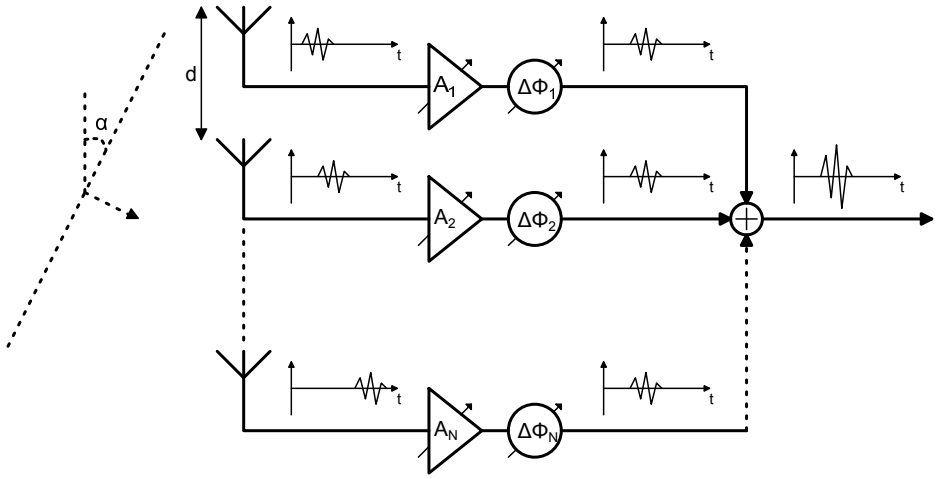


Figure 1.2: Phased array receiver

path.

When a plane electromagnetic wave arrives at the antenna array at an angle α between the wave front and the array, the received signals by the various antennas experience a phase shift difference due to the difference in the propagation paths length. If d is the distance between adjacent antennas, v the propagation speed of the electromagnetic wave in the medium and ω the angular frequency of the signal, the phase difference $\Delta\phi$ between the signals in two adjacent antennas is

$$\Delta\phi = \frac{d\sin(\alpha)}{v}\omega \tag{1.1}$$

Considering that the array is made of N antennas, the total phase shift $\Delta\phi_{tot}$ experienced by the signal in the last antenna compared to the one received from the first antenna is

$$\Delta\phi_{tot} = (N-1)\frac{d\sin(\alpha)}{v}\omega \tag{1.2}$$

Adjusting the phase shift introduced by each path in a proper way, a phase realignment of the various signals can be obtained. With sufficient antenna spacing, the noise of each antenna is uncorrelated to the noise of the other antennas in the array. Hence, the noise in each signal path before sum-

mation are independent. As a result, the shifted signals from the various antennas sum coherently while the noise sums incoherently. This results in an improvement of $10\log(N)[dB]$ in the SNR at the output of the N-element phased array receiver ([23]).
From another point of view, a phased array architecture can be seen as a system which permits to change the radiation pattern of the antenna array. With a certain phase setting for each path the system can be programmed to accept signals coming from one direction while rejecting signals coming from other directions.
Phased arrays have been traditionally used for military RADAR (RAdio Detection And Ranging) applications for many decades. The electronic beam steering of the phased array radar is orders of magnitude faster than the traditional radars based on mechanical rotation, which results in higher scanning speeds and lower profile for the system.
Although the first use of phased array RADARs was for military applications, nowadays its use is extended beyond this context. Other important applications can be easily find in the automotive. In this context driving-aid functions such as collision avoidance radar, automatic cruise control technology, parking aid and side collision warning can make safer and easier the driving experience ([10]).
Phased arrays are also used in wireless communication systems and in particular in cellular base-stations to enhance the signal coverage in the area of interest.
Biomedical applications are among the emerging applications that can take advantage of phased-array systems. For instance, phased array can be used in microwave imaging to detect early stage breast cancer ([8]).

1.1.2 Doherty Power Amplifier (DPA)

The market of wireless communication increased dramatically in the last 20 years, and the high demand in the network access has led many service providers to investigate digital technology to satisfy all the users ([6]).

These investigations brought to the development of complex digital modulation schemes such as Orthogonal Frequency-Division Multiplexing (OFDM), used in several 4G networks. These modulation schemes use amplitude modulated (AM) signals with high peak-to-average ratio (PAR), making more challenging the design of the electronic circuits and in particular power amplifiers ([11]).

The power amplification of amplitude modulated RF signals has mainly two problems. The first is that the envelope, and hence the modulating signal, will be distorted if the amplifier is used at its full nominal power level. The second is that conventional power amplifier designs only give maximum efficiency at a single power level, which is dependent on the circuit design but it is usually near the maximum nominal power for the device. As the input power is backed off from this point, the efficiency drops quickly and the heat dissipation can increase. The overall effect is therefore that the mean efficiency, which is much lower than the efficiency at the maximum power level, must be considered ([5]).

Several efficiency enhancement techniques were invented over the years and among them three classical techniques are worth to be mentioned: the Envelope Elimination and Restoration (EER), the Envelope Tracking(ET) and the Doherty Amplifier. In this example the Doherty PA technique is presented.

The Doherty amplifier configuration is realized using two power amplifiers, called the main (M) and the peak (P) amplifiers. This technique allows to realize an amplification process with higher efficiency over a wide range of output power with respect to a classic linear amplifier configuration. The peak amplifier is turned off for low power levels, while the main amplifier alone provides the power to the load. The peak amplifier starts to conduct only when the output power exceeds a certain amount, defined as the output power back-off, and together with the main amplifier provides the necessary power to the load. The main amplifier is often biased in class AB while the peak amplifier in class C. The typical DPA efficiency in function of the output power is reported in figure 1.3. The curve of an AB class amplifier is also reported in the figure and as it can be seen the efficiency of the Doherty

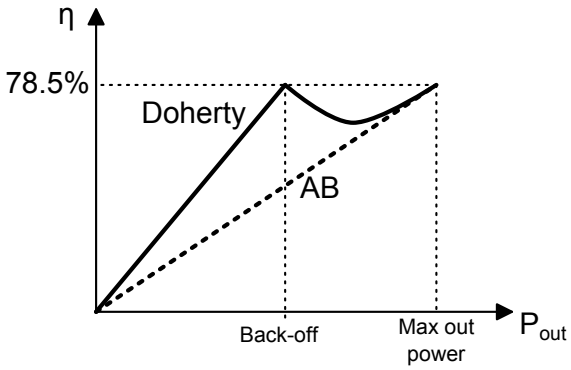


Figure 1.3: Dohery amplifier versus standard class AB amplifier efficiency (dashed line)

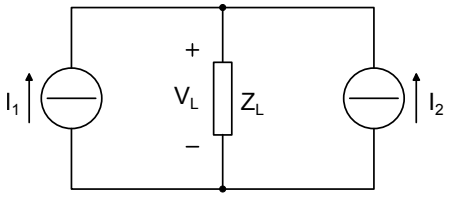


Figure 1.4: Active load-pull concept used in the DPA architecture

amplifier is clearly better ([13]).

The DPA configuration makes use of the active load-pull technique, i.e. the concept that the impedance of an RF load can be modified by applying a current from another phase coherent source ([5]). To fully understand the DPA behaviour it is then useful to introduce first this concept(Fig. 1.4). Considering that the load voltage is $V_L = Z_L(I_1 + I_2)$ it is than easy to calculate the load impedance Z_1 seen from the current generator I_1, that is

$$Z_1 = Z_L\left(1 + \frac{I_2}{I_1}\right) \tag{1.3}$$

A similar expression can be found for the load impedance seen from the generator I_2. From equation 1.3 in can be seen that the impedance seen from one generator can be modulated by the current of the other generator. In particular, the impedance Z_1 can be increased if I_2 is in phase with I_1, while it can be decreased if I_2 and I_1 are in anti-phase.

The Doherty amplifier uses this concept with some small modifications and

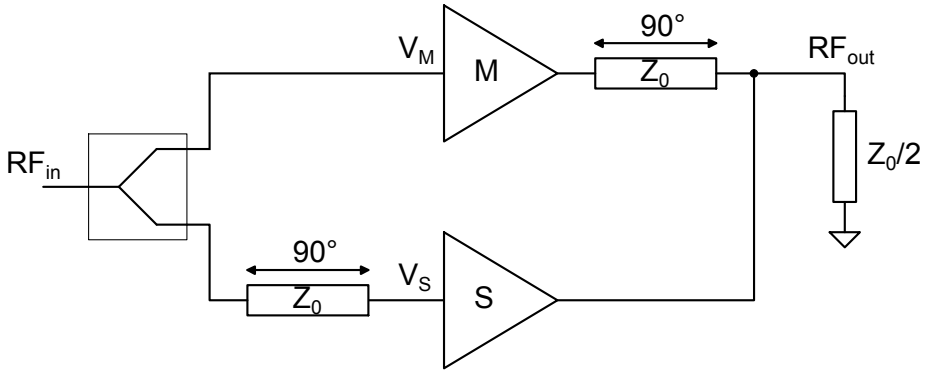


Figure 1.5: Doherty power amplifier

a practical implementation diagram is usually similar to the one reported in figure 1.5. As it can be seen it is made of two amplifiers which contribute is combined through an impedance inverting network.

For small input power levels the DPA acts as a typical PA, since the main device is conducting while the auxiliary is turned off due to its Class C bias condition. Assuming that the auxiliary PA's output is an open-circuit in this case, it is straightforward to deduce that the output impedance Z_M of the main amplifier is $2Z_0$.

Increasing the input power level, the current supplied by the main amplifier to the load increases reaching the device saturation, hence the maximum efficiency condition. The key action of the Doherty amplifier occurs in this moment; in fact, for higher input power level the auxiliary device automatically turns on, injecting current into the output load. This current increases the output voltage and modulates the impedance Z_M seen by the main device which, thanks to the impedance inverting network, becomes lower than $2Z_0$. In this way the main device is maintained in a constant maximum output voltage, and thus maximum efficiency condition. When both amplifiers contribute their maximum power, each device sees a load impedance of Z_0 and contributes equally to the overall output power.

It is worth to notice that another inverting network is present on the signal path of the auxiliary amplifier. It is, in fact, necessary to compensate the presence of the inverting network at the output of the main device and allow

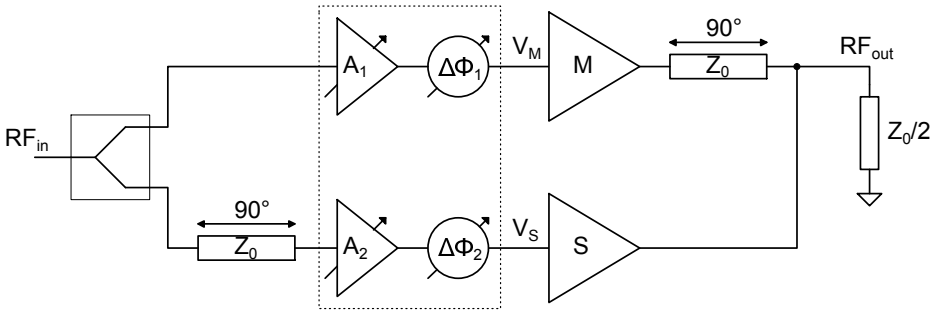


Figure 1.6: Doherty Power amplifier with the amplitude/phase control circuit

the in phase sum of the signals on the load impedance.
In practical implementations of the Doherty amplifier some important considerations must be made. A key design constraint in any DPA is to match the amplitude and phase of the signals at the input of the main V_M and peaking V_P amplifiers such that the desired load modulation is achieved and the output signals are combined as expected at the summing node. Independent variations in amplitude and/or phase of these signals, which may arise for example from small variations in the manufacturing of the packaged transistor, PCB tolerances and tolerances in surface mounted capacitors can result in large performance differences for the Doherty amplifier. Phase and amplitude control of the incident signals enables significant performance improvement of the DPAs [14].
This is why phase shifters and attenuators are important in this system. In fact, putting a cascade of an attenuator and a phase shifter in each of the two paths of the Doherty configuration enables the control over the amplitude and phase imbalances optimizing hence the signals combining at the output node (fig.1.6). This results in an optimization of the amplifier efficiency.

1.2 Target Specifications

In the previous section two examples where phase shifters and attenuators are used have been given. In particular, the aim of this thesis is the design of these two blocks for the Doherty power amplifier application ([15]) using the Infineon 130nm CMOS technology with a high resistive substrate [16].

The tentative target specifications for the phase shifter are reported in table 1.1, while those for the programmable attenuator are reported in table 1.2. The target specifications listed in the two tables are intended in the

$f[GHz]$	$S11[dB]$	$IL[dB]$	$\Delta\phi[^\circ]$	$Step[^\circ]$	$P1dB[dBm]$
2	< -10	< 3	> 45	< 6	> 20

Table 1.1: Phase shifter target specifications

$f[GHz]$	$S11[dB]$	$IL[dB]$	$\Delta S_{21}[dB]$	$Step[dB]$	$P1dB[dBm]$
2	< -10	< 1.5	> 15	0.5	> 20

Table 1.2: Attenuator target specifications

frequency range from $1GHz$ to $3GHz$. This means that the unitary fractional bandwidth is required. The two blocks must handle and have linear behaviour for high input powers; the 1-dB compression-point $P1dB$ should be higher than $20dBm$. Moreover, they have to be realized with only passive components, and hence they should not consume power.
From table 1.1 it can be seen that the phase shifter should have an Insertion Loss (IL) lower than $3dB$ and a phase shift range of at least 45° with steps of 6°. Moreover it should achieve this task with an as low as possible insertion loss variation over different phase shift configurations.
From table 1.2, instead, it can be seen that the attenuator should have an attenuation range ΔS_{21} of at least $15dB$ with steps of $0.5dB$. Furthermore the attenuator should show a phase variation $\Delta\phi$ over different attenuation settings less than 3°.

1.3 Network Analysis Basics

The aim of this section is to recall some basic tools for network analysis which have been often used in this work and which can be useful to more

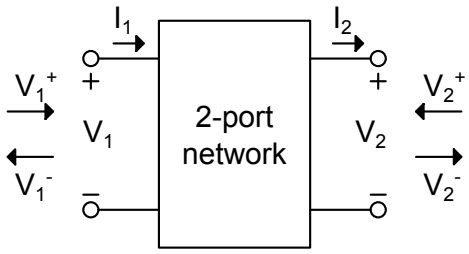


Figure 1.7: 2-port network

easily understand all the presented concepts. For a deeper discussion refer to [1],[2].

1.3.1 The Scattering Matrix

Almost all circuits analysed in this thesis can be seen as passive linear two port networks (Fig. 1.7). This kind of circuits can be characterized in various ways. To simplify the analysis and also emphasize important design criteria, it is often useful to use higher-level descriptions which mainly focus on the input-output behaviour but neglect details of the internal circuit structure. At lower frequencies the most common representations are the *impedance* and *admittance matrices*, or a mixture of them.

A different way to describe a network, especially useful when dealing with circuits at radio frequencies, is the *scattering matrix*. This matrix relates the voltage waves incident on each ports to the voltage waves reflected from each port. If V_i^+ is the amplitude of the voltage wave incident on port i and V_i^- is the amplitude of the voltage wave reflected from port i, the scattering matrix $[S]$ of a 2-port network is defined as:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix} \tag{1.4}$$

where each specific element S_{ij} is defined as:

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k=0 \, for \, k \neq j} \tag{1.5}$$

In words, the last equation says that S_{ij} is found by driving the port j with an incident wave of voltage V_j^+ and measuring the reflected wave amplitude V_i^- coming out of the port i while all the other ports are terminated in matched loads to avoid reflections.
The use of S-parameters is mainly due to practical measurement reasons. In fact, at radio frequencies it is difficult to provide adequate short- or open-circuits which would be necessary to measure impedance ad admittance parameters. To measure S-parameters, instead, it is necessary to provide an adequate matching condition at ports and this is much easier to do.
An interesting property of the scattering matrix, which will be used subsequently, is worth to be reminded. It regards reciprocal networks and states that the scattering matrix in this cases is symmetric, i.e.:

$$S = S^T \tag{1.6}$$

where T stands for transpose of the matrix.

1.3.2 The ABCD Matrix

Another convenient network description used to represent (only) two port networks is the *transmission*, or *ABCD*, *matrix*. The input port voltage and current are related to the output port voltage and current through the next equations:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{1.7}$$

where the A, B, C and D parameters made the transmission matrix. These coefficients can be found short-circuiting or open-circuiting the output port, obtaining:

$$A = \left.\frac{V_1}{V_2}\right|_{I_2=0} \qquad B = \left.\frac{V_1}{I_2}\right|_{V_2=0} \qquad C = \left.\frac{I_1}{V_2}\right|_{I_2=0} \qquad D = \left.\frac{I_1}{I_2}\right|_{V_2=0} \tag{1.8}$$

This model is particularly useful when dealing with the cascade of two or more 2-port networks. In fact the ABCD matrix of this kind of system

can be found by multiplying the ABCD matrices of the individual 2-port networks. This is the reason why the sign convention of I_2 has been chosen to flow out of port 2 (see Fig. 1.7). In fact putting two stages in cascade the current flowing out from the first stage goes inside the second stage and the sign conventions agree.

Relation to S-Matrix

Even though the ABCD-parameters are difficult to measure in practice, they are extremely useful for network analysis. Moreover, once the ABCD-matrix coefficients are known, the S-parameters can be easily calculated from them through the next expressions:

$$S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D} \tag{1.9}$$

$$S_{12} = \frac{2(AD - BC)}{A + B/Z_0 + CZ_0 + D} \tag{1.10}$$

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} \tag{1.11}$$

$$S_{22} = \frac{-A + B/Z_0 - CZ_0 + D}{A + B/Z_0 + CZ_0 + D} \tag{1.12}$$

It is important to underline that these expressions are valid as soon as the characteristic impedances are the same on all the ports (equal to Z_0). Otherwise different equations must be used (see [1]).

1.3.3 Mutual Inductors

Another element which is widely used in this work and which is worth to be recalled is the transformer. As an anticipation the transformer will be used instead of two uncoupled inductors exploiting the mutual inductance to increase the effective inductance. In the appendix B it is shown how this fact can be achieved.
A transformer, which electrical representation is reported in figure 1.8, can be mathematically described through the following equations:

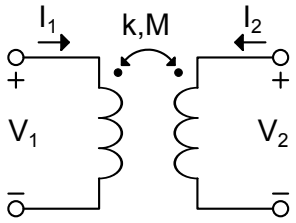


Figure 1.8: A transformer representation

$$\begin{cases} V_1 = i\omega L_1 I_1 + i\omega M I_2 \\ V_2 = i\omega M I_1 + i\omega L_2 I_2 \end{cases} \tag{1.13}$$

The coefficient M is called *mutual induction coefficient* and it takes into account the interaction between inductors and it can be both positive and negative. The mutual induction coefficient is positive ($M > 0$) if the magnetic field lines generated from the coils have the same direction when concatenated to each other; the mutual induction coefficient is negative ($M < 0$) otherwise. Moreover, higher M coefficient means that higher is the quantity of the magnetic field lines generated from one inductor that are concatenated with the other.

Another parameter often used and closely related to M is the *coupling coefficient* k, defined as:

$$k = \frac{M}{\sqrt{L_1 L_2}}, \qquad |k| \leqslant 1 \tag{1.14}$$

The coupling coefficient is null ($k = 0$) when no interaction between inductors is present; instead, its magnitude is unitary ($|k| = 1$) when all the magnetic field lines generated from one inductor are concatenated with the other. Moreover, it is worth to observe that the mutual induction and the coupling coefficients have the same sign, hence the considerations made for M are valid also for k.

1.3.4 Linearity - P1dB

The distortion is a phenomenon related to the fact that real devices (transistors, diodes etc..) are non linear, and this origins spurious frequency contributions. Any difference in the shape of the input and the output waveforms versus time, not considering scaling factor and time translation, is called distortion. For example, MOSFETs are often used as switches and when they are in the closed state they can be represented with a series resistance, which is due to the channel resistance of the MOS. For small signals this resistance can be assumed linear and the overall system is not affected. However, when the signal amplitude increases, the channel resistance starts to deviate from the linear behaviour and the overall system linearity is affected.
For a memoryless non-linear system the input/output characteristic can be approximated with a polynomial ([4]):

$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \cdots \tag{1.15}$$

where $x(t)$ and $y(t)$ are, respectively, the input and output signals while a_i coefficients represent the response of the system. The coefficient a_0 represents the dc component of the output signal, a_1 is the linear gain of the system, whereas a_2, a_3, ..., describe the distortion of the system.
Assuming that the input signal is a pure sinusoid $x(t) = A\cos(\omega t)$, and remembering the trigonometric relations $\cos^2(x) = (1+\cos(2x))/2$ and $\cos^3(x) = (3\cos(x) + \cos(3x))/4$, the output signal of equation 1.15, truncated at the third order, can be expressed as:

$$\begin{aligned} y(t) &= a_0 + a_1 A\cos(\omega t) + a_2 A^2\cos^2(\omega t) + a_3 A^3\cos^3(\omega t) \\ &= \left(a_0 + \frac{a_2 A^2}{2}\right) + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \\ &\quad + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) \end{aligned} \tag{1.16}$$

It can be seen that due to non-linearities in the system, even if at the input a single-tone signal is applied, higher order harmonics are present at the output. Moreover, the second order distortion causes a DC offset, while the

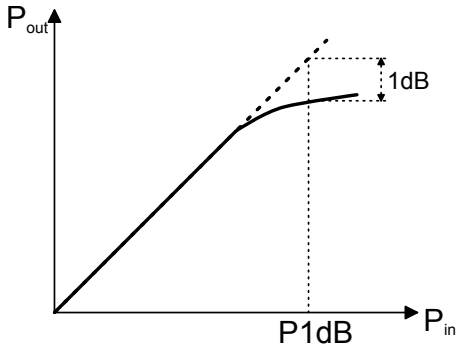


Figure 1.9: 1-dB compression-point

third order distortion produces a gain variation.
Different figures of merit exist to quantify the harmonic distortion of a system ([4]). In this work the 1-dB compression-point (P1dB) will be prevalently used. Looking at the fundamental tone term in Eq. 1.16

$$y(t) = \cdots + \left(a_1 A + \frac{3a_3 A^3}{4} \right) \cos(\omega t) + \cdots \tag{1.17}$$

it can bee seen that it depends on the third order distortion. Often $a_3 < 0$ which leads to a gain reduction (or compression). This gain compression affects the system for higher amplitudes A of the input signal. The *1-dB compression-point* is defined as the input amplitude (or power) value which causes the gain to drop by 1dB compared to the ideal case. This concept is represented in figure 1.9.

It is worth to notice that here, for simplicity, it has been assumed a maximum 3rd order distortion. In general higher order distortions can be present in the system and they also influence the gain variation, as well as the DC signal value.

Chapter 2

Analysis and Design of a Phase Shifter

In the previous chapter some of the applications where phase shifters can be used have been presented. In phased arrays, for example, they are used to change the pattern of a multiple-antenna system while in the Doherty Power Amplifiers they are used to compensate the parasitics effect and hence optimize the power amplifiers efficiency.
In this chapter, phase shifters will be discussed more in detail. Different possible ways in which they can be realized are presented and among them the π-network topology is chosen for a deep analysis and a successive design of a phase shifter for DPA application.
Finally, an alternative topology, which has been explored trying to obtain better circuit performance mainly in terms of insertion loss, is presented.

2.1 Introduction to Phase Shifters

A phase shifter is a two port network which permits the control of the phase difference between the output and the input signals by means of a control signal (DC voltage). In other words, considering the notation reported in figure 2.1, it is possible to control the parameter $\Delta\phi$. Ideally this phase shift should be achieved without losses.

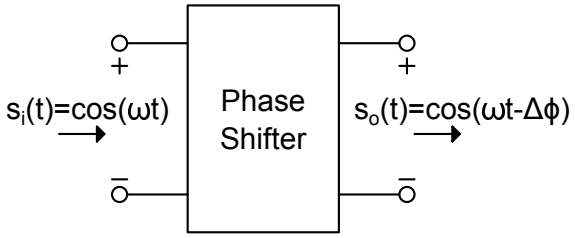


Figure 2.1: 2-port phase shifter

Different phase shifter types have been presented over the years and the choice of which one to implement depends on the available technology and the application. One first distinction that can be made is between analog and digital phase shifters. In *analog* phase shifters the phase difference can be varied in a continuous manner by means of a continuous variation of the control signal. On the other hand, in *digital* phase shifters, the phase difference can be changed only within a finite set of values; in many applications, however, it is enough.

From the technology point of view, semiconductor phase shifters are here considered. They can be made in mainly two different ways: the first one is based on the use of Micro Electro-Mechanical Systems (MEMS) ([18]) while the second on semiconductor devices(pin diodes, MOSFETs) ([24] - [31]). The former technology basically makes available less lossy switches compared to the latter one, however it is not always available. With regard to the latter one, the choice is often between gallium arsenide (GaAs) and silicon (Si) technologies and it is based on the compromise between performances and costs. The goal of this work was to design a state of the art circuit, using a CMOS process.

Phase shifters using semiconductor devices can be mainly of the reflection or transmission type. A *reflection-type* phase shifter (RTPS) consists of a hybrid 90° coupler combined with two reflective loads [31]. Its operation is reported in figure 2.2. The input signal is split in two equal parts which reach the loads with a 90° phase difference between them. Each part is then reflected again by a load with an input impedance (Z_L) which is different from the characteristic impedance of the coupler (Z_0). This impedance difference

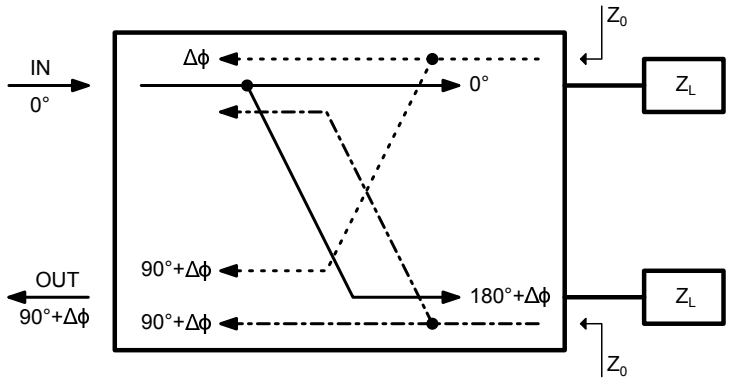


Figure 2.2: Operation of a reflective-type phase shifter

introduces a phase shift ($\Delta\phi$) which is equal to the phase of the reflection coefficient ρ:

$$\rho = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.1}$$

The reflected signals are then split and phase shifted again by the coupler, obtaining that signals arriving at the input are in opposition of phase and they cancel each other, while the signals arriving at the output are in phase and sum constructively with a total phase shift (compared to the input) of $90° + \Delta\phi$. Changing hence the load impedances it is possible to change the phase difference between output and input. This can be done, for example, by varying the load capacitance with a simple varactor. The choice of the reflective load depends on the required phase shift and allowable losses. In fact, the use of a complex load can give a high phase shift from one side, but from the other it gives also high losses. Hence a compromise for a specific application should be found.

The other type of phase shifters, *transmission-type*, can be further divided into two groups: switched-line and loaded-line phase shifters. The *switched-line* phase shifter is, conceptually, the simplest one. The basic configuration for a 1-bit phase shifter is shown in figure 2.3. As it can be seen, two signal paths for the signal are possible and the two Single-Pole-Double-Throw (SPDT) switches are used to chose one of them. The two paths are usually realized with transmission lines having a different length. When the signal passes through the longest path it experiences an additional phase delay

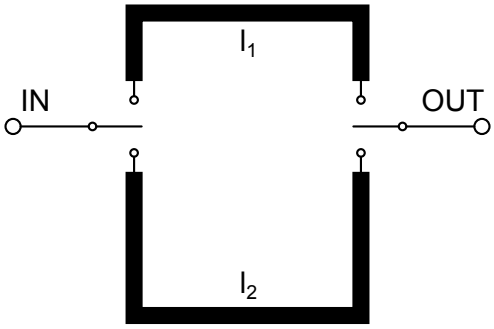


Figure 2.3: Switched-line phase shifter

compared to the other path of:

$$\Delta\phi = \frac{2\pi f}{v_p}\Delta l \tag{2.2}$$

where v_p is the phase velocity. In this type of phase shifter the insertion loss is mainly due to the switches, hence the use of this solution is legitimate only if a technology with good switches is available.
An interesting thing which can be observed in switched-line phase shifters is that the phase shift $\Delta\phi$ is proportional to the frequency. This is actually obvious, since transmission lines introduce a constant time delay. Hence the time delay difference between the two paths can be expressed as:

$$\Delta\tau = \frac{\Delta l}{v_p} \tag{2.3}$$

Because of this feature, switched-line phase shifters are also called *switched delay lines*. This concept is presented in detail in the next subsection, where the difference between constant phase shift and constant time delay will be explained.
The other type of phase shifters is the *loaded-line* phase shifters. It is mainly based on a uniform transmission line which is periodically loaded with small reactive impedances. A simple example, to better explain this concept, is shown in figure 2.4. It can be shown ([3]) that if Y_L is the susceptance of the loaded impedance and Z_0 is the characteristic impedance of the transmission line, then the phase shift introduced by the phase shifter can be expressed

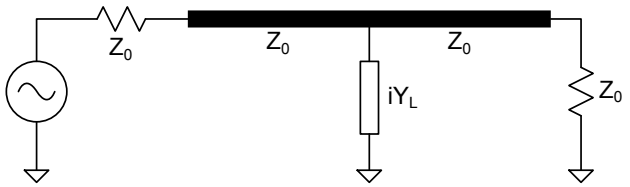
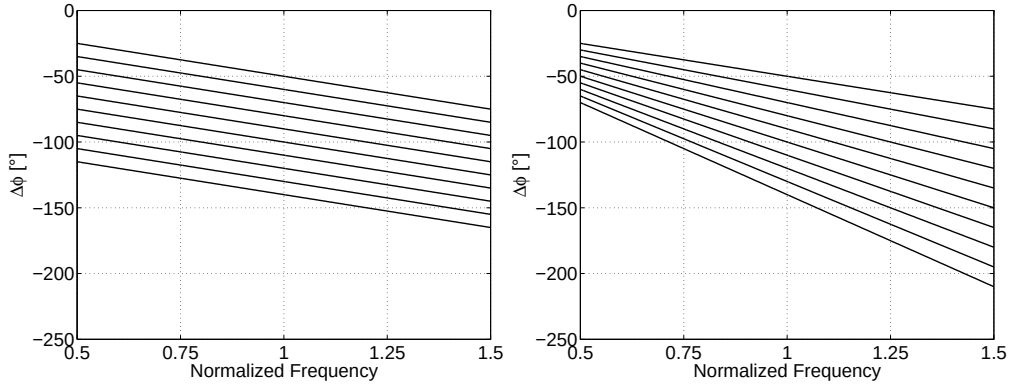


Figure 2.4: Loaded-line phase shifter



(a) Phase Shifter (b) True Time Delay

Figure 2.5: Ideal phase response of a Phase Shifter and a True Time Delay for different phase shift configurations

as:

$$\Delta\phi = \tan^{-1}\left(\frac{Y_L Z_0}{2}\right) \tag{2.4}$$

This topology is the basic idea of this work, hence it will be deeply analysed in this chapter.

2.1.1 Phase Shifter vs True Time Delay (TTD)

In section 2.1 it has been seen that switching between two transmission lines introduces a constant time delay difference instead of a constant phase shift difference. Actually this type of circuits should be rather called delay lines, or also *True Time Delay (TTD)* phase shifters.
To better explain this concept the ideal phase shift response for both phase shifter and TTD is reported in figure 2.5. From the figure it can be seen that, for both of these elements, it is possible to change the desired phase shift.

However, the various shifting configurations are different between them in the two cases. In the phase shifter different configurations have the same slope and hence the phase difference between two different configurations is constant over frequency. In the TTD, instead, different configurations have different slope and the phase difference between two different configurations is not constant over frequency. What is constant in this case is the group delay difference between various configurations, which is defined as:

$$\tau_g = -\frac{d\phi}{d\omega} \tag{2.5}$$

The choice of which of the two types to use depends mainly on the application. In narrow band systems the two solutions usually have similar behaviour. In wide band systems, for example timed arrays, the TTD should be used otherwise the presence of signal dispersion could worsen degrades the system performances ([23]).

2.1.2 Specifications in the Time Domain

The initial specifications have been set considering the phase of the signal and hence the desired phase shift. As it has been shown previously a TTD phase shifter has a constant time delay instead of the phase shift. In this work, after an accurate analysis of the system, it has been decided to implement a TTD phase shifter. Therefore, the specifications have been translated in the time domain and are reported in table 2.1, for convenience. The targets

$f[GHz]$	$S11[dB]$	$IL[dB]$	$\Delta\tau_g[ps]$	$Step[ps]$	$P1dB[dBm]$
2	< -10	< 3	> 65	< 8	> 20

Table 2.1: Phase shifter TTD target specifications

reported in table 2.1 are intended for a frequency range of $1 \div 3GHz$. They have been obtained expressing in time the specifications presented in the table 1.1. The conversion phase-time has been made considering a frequency

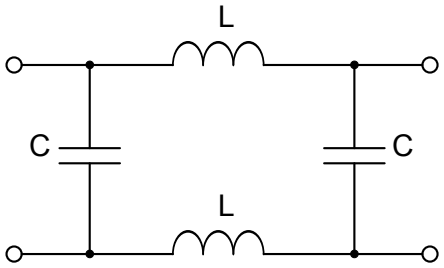


Figure 2.6: Lumped delay line, topology also called $\pi - network$

of $2GHz$. For example the specification on the step comes from the fact that $6°$ corresponds to $6/360 \cdot 1/(2GHz) \simeq 8ps$.

2.2 Tunable Delay Line

Phase shifter topologies presented so far mainly use transmission lines. Considering that the center frequency of the phase shifter designed in this work is $2GHz$, the use of one of these solutions would probably complicate the design. In fact, a signal at this frequency has a wavelength λ of about $4cm$ in the used CMOS technology and a phase shift $\Delta\phi$ of $45°$ would require a transmission line of at least $0.05cm$ length for the switched line topology. Implementing a line of this length in the CMOS technology would mean to accept a circuit with high losses; this is unacceptable considering that one of the requirement is to minimize the losses as much as possible.
Even though transmission lines offer wide bandwidth, for applications under $4 - 5GHz$ an often used concept is *lumped delay lines*. Considering the network in figure 2.6, it is made using lumped elements and it can be seen as an approximation of a transmission line with characteristic impedance Z_0 over a finite bandwidth, that is for frequencies lower than the *cut-off frequency* f_c; these parameters, as will be shown soon, are related to the circuit elements through the following expressions:

$$Z_0 = \sqrt{\frac{L}{C}}, \qquad f_c = \frac{1}{2\pi\sqrt{LC}} = \frac{\omega_c}{2\pi} \tag{2.6}$$

Moreover, a signal which goes through this circuit undergoes a group delay of:

$$\tau_g = 2\sqrt{LC} \tag{2.7}$$

Even though this solution has a finite bandwidth, it allows to have a greater control over the line parameters. In fact, for example, varying the inductance or the capacitance value it is possible to vary the delay. It is true that also the characteristic impedance and the cut-off frequency vary but this is not necessarily a problem, as will be seen soon.

The equations just presented are valid for frequencies much smaller than the cut-off frequency; a deeper analysis of the π-network of figure 2.6 is now made with the aim to extract the equations which completely describes the circuit behaviour, even for frequencies higher than the cut-off frequency. Exploiting the calculus reported in the appendix A for the generic π-network, the ABCD-matrix of the lumped delay line results:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1-\omega^2 2LC & i\omega 2L \\ i\omega 2(1-\omega^2 LC^2) & 1-\omega^2 2LC \end{bmatrix} \tag{2.8}$$

Remembering the equations 1.9 and 1.11, reported in the introduction, which relates the ABCD parameters to the S-parameters, it is possible to calculate the reflection coefficient S_{11} and the transmission coefficient S_{21} as:

$$S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D} \tag{2.9}$$

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} \tag{2.10}$$

The coefficients S_{22} and S_{12} are not reported since the network is symmetric and they are equal to S_{11} and S_{21}, respectively.

Let's consider for a moment the first expression. When a generator with internal impedance Z_g drives a transmission line, the latter has to have a characteristic impedance $Z_0 = Z_g$ to satisfy the matching condition. This matching consideration derives from the condition that no reflections occur at the input port, that is $S_{11} = 0$. Applying the same condition to the first

equation allows to extract the characteristic impedance associated to the π-network (which will be called *cell* in this context):

$$S_{11} = 0 \quad \Rightarrow \quad Z_{0c}(\omega) = \sqrt{\frac{L}{C}\left[1 - \left(\frac{\omega}{\omega_c}\right)^2\right]^{-1}} \tag{2.11}$$

where $\omega_c = 1/\sqrt{LC}$ is the cut-off angular frequency and represents the frequency at which the characteristic impedance becomes imaginary. Notice that in the last expression Z_{0c} notation has been used instead of Z_0 with the aim to emphasize the fact that the characteristic impedance of the cell is considered.
Focusing now on the equation 2.10 and substituting the ABCD parameters, the transmission coefficient S_{21} is obtained:

$$S_{21}(i\omega) = \frac{1}{(1 - 2\omega^2/\omega_c^2) + i[\omega(L/Z_0 + CZ_0) - \omega^3 CZ_0/\omega_c^2]} \tag{2.12}$$

Note that S_{21} mostly influences the insertion loss of the cell. However, in these expression only the finite bandwidth is taken into account since the inductor and capacitor are assumed to be ideal (infinite quality factor Q). The introduction of parasitics would heavily complicate the discussion and increase the risk to ignore more important things for the design. This task is left to the simulators.
The phase difference introduced by the cell can be calculated now, looking at the phase of the transmission coefficient S_{21}

$$\phi_{21}(\omega) = -\arctan\left[\frac{\omega(L/Z_0 + CZ_0) - \omega^3 CZ_0/\omega_c^2}{1 - 2\omega^2/\omega_c^2}\right] \tag{2.13}$$

Finally, the group delay of the cell, defined as the derivative of the phase with respect to frequency, can be calculated from the last equation and results:

$$\tau_g(\omega) = -\frac{d}{d\omega}[\phi_{21}(\omega)] = \frac{(L/Z_0 + CZ_0)(1 + 2\omega^2/\omega_c^2) - \omega^2 CZ_0(3 - 2\omega^2/\omega_c^2)/\omega_c^2}{(1 - 2\omega^2/\omega_c^2)^2 + \omega^2(L/Z_0 + CZ_0 - \omega^2 CZ_0/\omega_c^2)^2} \tag{2.14}$$

Supposing now that the matching condition is satisfied, i.e. $Z_{0c} = Z_0$, the last equation can be written in a simple way for frequencies much smaller than the cut-off frequency as:

$$\tau_{g,DC} = \tau_g(0) = 2\sqrt{LC} \tag{2.15}$$

As expected this equation coincides with the equation 2.7 introduced at the beginning of this section, when the lumped delay network has been introduced. It gives a rule of thumb on the selection of the component values. Note also that from the last equation it can be seen that:

$$\tau_{g,DC} = 2\sqrt{LC} = \frac{2}{\omega_c} \tag{2.16}$$

which means that there is a limit on the maximum delay which can be introduced from a single cell for a specific bandwidth. In fact, as it will be seen later, higher delays can be obtained by the cascade of more cells.
A variable delay element is able to change the group delay depending on the value of the control signal. The last equation suggests that this can be done by simply changing the capacitance or the inductance value. In passive circuits a variable capacitance is much easily done, for example with varactors. Hence, replacing the capacitors in the schematic of figure 2.6 with varactors, a variable delay element can be obtained. However, the change of the capacitance values leads to a change of the characteristic impedance of the cell Z_{0c}. Since the source and load impedances are fixed and equal to Z_0, the cell cannot be perfectly matched both when the capacitance is minimum C_{min} and maximum C_{MAX}. Therefore the *group delay difference* $\Delta\tau_g$ between maximum and minimum capacitance configurations must be derived from the general $\tau_g(\omega)$ equation:

$$\Delta\tau_{g,DC} = \tau_{g,DC}|_{C=C_{MAX}} - \tau_{g,DC}|_{C=C_{min}} = (\alpha - 1)C_{min}Z_0 \tag{2.17}$$

where $\alpha = C_{MAX}/C_{min}$. Considering that a capacitance variation results in a characteristic impedance variation, a good matching condition for both the maximum and minimum capacitance cases is when the source/load impedance

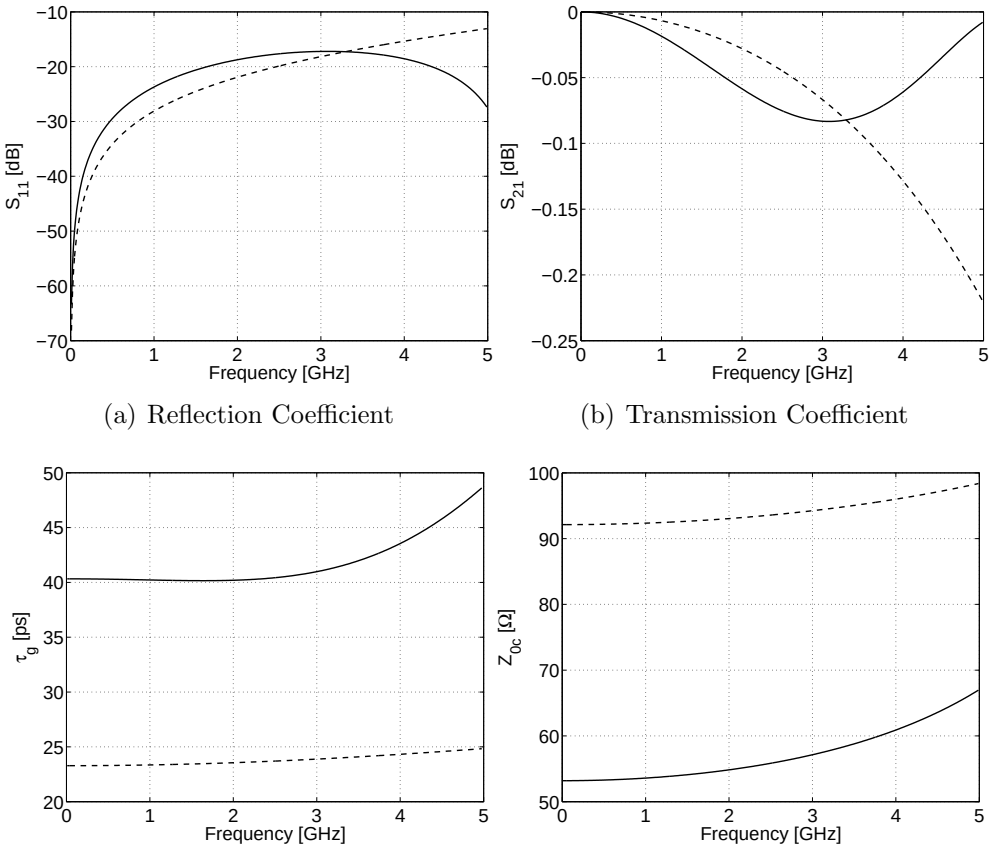
Z_0 is equal to the geometrical mean of the minimum $Z_{0c,min}$ and maximum $Z_{0c,MAX}$ characteristic impedance of the cell ([8]), i.e.:

$$Z_{0c,opt} = \sqrt{Z_{0c,min} Z_{0c,MAX}} \tag{2.18}$$

In this condition the group delay difference of the cell can be expressed as:

$$\Delta\tau_{g,DC} = \frac{(\alpha - 1)}{\sqrt[4]{\alpha}} \sqrt{LC_{min}} \tag{2.19}$$

From the last equation it can be seen that the α coefficient results in a larger delay variation per cell. However, as it has just been shown, the change of the capacitance leads to a change of the characteristic impedance of the cell. As a result, a higher α causes a higher Z_{0c} variation and hence a lower input matching which is associated with a higher insertion loss.
To better explain the concept on which is based this delay element, an example of design is reported in figure 2.7. Some of the parameters, introduced in the previous discussion, are shown in this figure with two curves per plot which represents the maximum and minimum capacitance cases. The cell has been designed to have a group delay difference $\Delta\tau_g$ of $17ps$ and characteristic impedance Z_{0c} is 70Ω. These values are similar to the values of the finally designed delay line and they can already give some clues on its behaviour.
The figure 2.7(a) shows that the reflection coefficient S_{11} is lower than $-17dB$ over all the band. A rule of thumb usually used is $S_{11} < -10dB$, which means that less than 10% of the power is reflected from the cell. Hence, in this case, even if the characteristic impedance of the cell (Fig. 2.7(d)) is not constant, this is not a problem. It could become important if the delay difference asked to the cell is substantially higher than $17ps$; however in this case even the finite bandwidth would become a problem. In fact, as it can be seen from the figure 2.7(c), the maximum capacitance case curve starts to increase around $3.5 - 4GHz$ and this is due to the finite bandwidth. This increase introduces delay error in the cell which, for low bandwidth values, can become important. Observe that, as it can be seen easily from the formulas previously derived, higher capacitance C means higher group delay τ_g but also



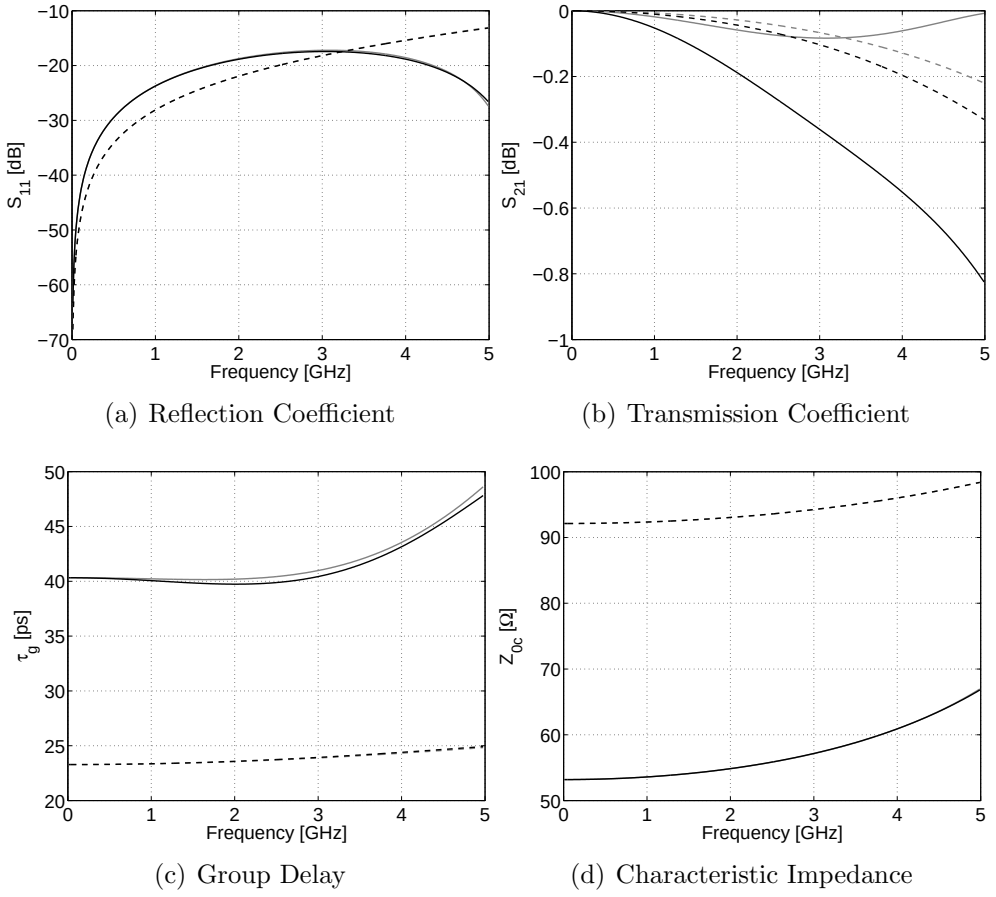
(a) Reflection Coefficient

(b) Transmission Coefficient

(c) Group Delay

(d) Characteristic Impedance

Figure 2.7: Tunable delay element concept. In figure are reported graphics for the C_{MAX} and C_{min} (dashed line) cases



(a) Reflection Coefficient (b) Transmission Coefficient

(c) Group Delay (d) Characteristic Impedance

Figure 2.8: Comparison between infinite quality factor of the components (grey lines) and finite quality factor. Dashed lines represent the C_{min} case

lower characteristic impedance Z_{0c} and cut-off frequency f_c. This fact sets the limit on the maximum delay variation obtainable from a single cell.
In this example ideal components have been assumed, that is infinite quality factor for both capacitor and inductor. If parasitics are introduced, which means to consider the finite quality factor of the reactive elements, the cell behaves slightly different. Figure 2.8 shows the comparison between the ideal case (dashed line) and a more realistic case where the inductor and the capacitor have finite quality factors of, respectively, $Q_L = 10$ and $Q_C = 20$. It can be observed that the most remarkable changes concern the transmission coefficient and the group delay difference, while the other two parameters do

not change significantly.

2.3 Cell Design

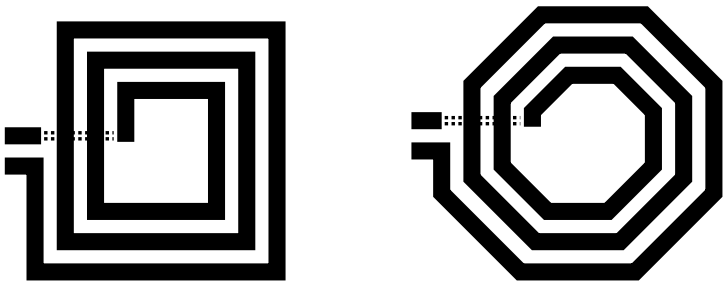
The π-network topology previously introduced and used to realize the phase shifter is a passive network and it is basically made of inductors and capacitors. As it has been seen from the last examples these elements have a finite quality factor Q, which means that some parasitic series resistances are present in the circuit. The main effect of these resistances, as it can be seen from the figure 2.8(b) is to introduce additional losses and they should be made as low as possible with an accurate design of the reactive elements. In this section some guidelines for the optimal design of these components are presented, starting from the inductor.

2.3.1 Inductors Design

An often used method to realize on-chip inductors is the planar spiral. Figure 2.9 shows some possible shapes. In terms of the inductance and the quality factor values, different shapes have different characteristics. A circular shape is usually better than the square one in terms of the quality factor Q and the choice of which one to implement mainly depends on the available technology. On the other hand, the characteristics of the inductor like the area, number of turns, width of the strips etc. are usually influenced by the application. For a detailed discussion about IC inductors see [2],[19].

Another possibility to realize on-chip inductors is to use active circuits to synthesize the equivalent of an inductor. These circuits, however, introduce more distortion and power consumption than a passive implementation and considering that in this work it is required no power consumption, the passive solution has been chosen.

When more than one inductor is required from the circuit topology, as it is the case in the π-network presented previously, another possibility is to use a transformer instead of uncoupled inductors. An example of a possible implementation as a planar spirals is shown in figure 2.10 for the case of two



(a) Rectangular (b) Octagonal

Figure 2.9: Possible inductor shapes

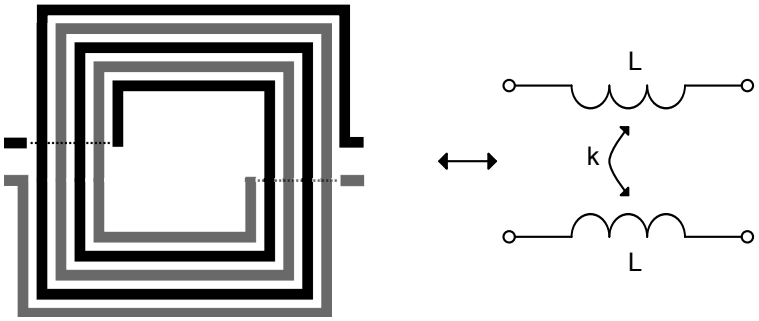


Figure 2.10: Interleaved transformer

inductors. In fact, exploiting the coupling between inductors, it is possible to obtain higher effective inductances value for the same on-chip area. Or, from the other point of view, the same inductances value can be implemented in a smaller area. It is important to notice that this is not a general rule; in this case the higher inductance is obtained because of the differential driving signals. This concepts are better explained in the appendix B. Furthermore it is shown that the increase is closely related to the coupling coefficient k. Higher k means also higher increase in the effective inductance. The transformer in figure 2.10, usually called interleaved transformer, is well suited for four-port applications that demand symmetry. For this reason it is a good solution to be used in the π-network topology.

The inductors are mainly described by two parameters, that is the inductance

value L and the quality factor Q. The quality factor is defined as:

$$Q(\omega) = \frac{\omega L(\omega)}{R_s(\omega)} \tag{2.20}$$

where R_s is the series parasitic resistance. It is worth to notice that all the parameters are frequency dependent. However focusing on a sufficiently finite bandwidth they can be considered almost constant. Usually the inductance and the quality factor values are specified at a determined frequency.
Another important parameter to be considered are the parasitic capacitances. In an inductor they mainly account for the existing capacitance between the coils and the substrate. In the transformer also a capacitance between different coils is present. Considering that in the differential π topology used in this work this parasitic capacitance goes in parallel to the external capacitor, it should be taken into account in the design. Its presence results in a lower overall α coefficient and hence lower delay, which should be compensated with a proper design of varactors.
From all these considerations it is clear that an accurate design of the inductors is important to achieve better performance. Some important guidelines which have been taken into account for this purpose are here reported:

- The strip width (spiral width) leverages the series resistance and parasitic capacitance towards substrate. Lower width means lower capacitance but higher resistance. On the other side, however, higher width means higher capacitance but lower resistance only if the skin effect is negligible. Considering that this effect depends on the frequency, increasing the width to reduce the series resistance, hence increasing the quality factor, brings benefits up to a certain point.

- The inductor should not be filled up to the center. In fact, the most inner turns would give a high resistive but a limited inductive contribution which results in an inductance reduction, and hence a quality factor reduction.

- The distance between coils leverages the parasitic capacitances between coils. Higher distance means lower capacitance but also lower coupling

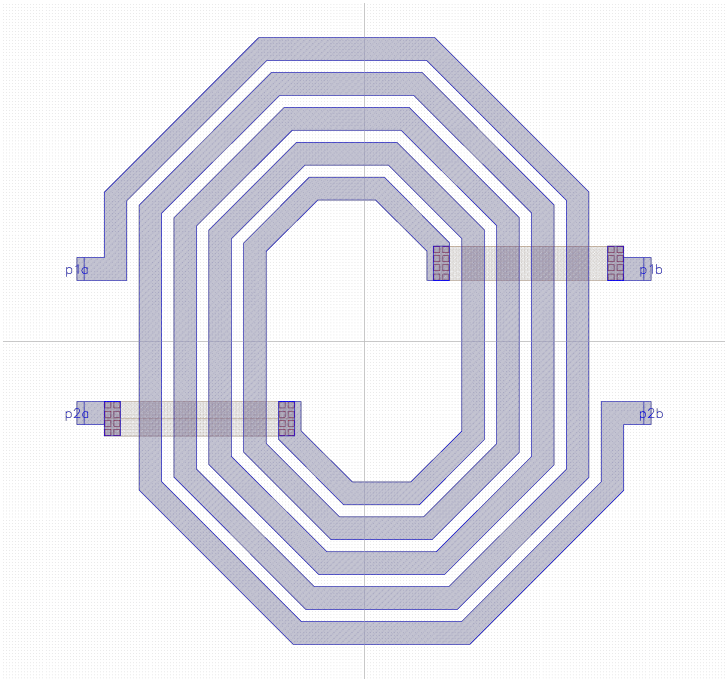


Figure 2.11: Designed transformer

coefficient. On the other side lower distance results in an increasing of both k and capacitances. Considering that this parasitic capacitance goes in parallel with the external one, it should be minimized in order to improve the delay tuning capacity of the cell.

Taking into account the last observations and the design specifications, the transformer has been fully designed on the higher metal layer to maximize the quality factor (lowest sheet resistance). Considering that the technology allows 45° strips it has been designed having an octagonal shape; the oval form has been used to save some horizontal space. The optimal value of the strips width has been found to be $7.5\mu m$. Moreover, the optimal distance between strips, which has permitted to keep low parasitic capacitances while maintaining a good coupling coefficient, has found to be $4\mu m$. With an area of $160 \times 200\mu m^2$ and 2.5 turns the resulting transformer layout is reported in figure 2.11. The transformer presents an effective inductance value of $1.7nH$ and a quality factor of 10 at the frequency of $2GHz$. This is achieved through a 0.61 coupling coefficient. For convenience, some of the transformer

$A[\mu m^2]$	$Coil\,turns$	$L_{eff}[nH]$	$R_s[\Omega]$	k	Q	$C_p[fF]$
160×200	2.5	1.7	2.1	0.61	10.1	83

Table 2.2: Designed transformer characteristics at $2GHz$

characteristics are reported in table 2.2. The capacitance C_p considers the parasitic capacitance between the inductors and toward substrate. Its effect is to increase the overall cell capacitance C.

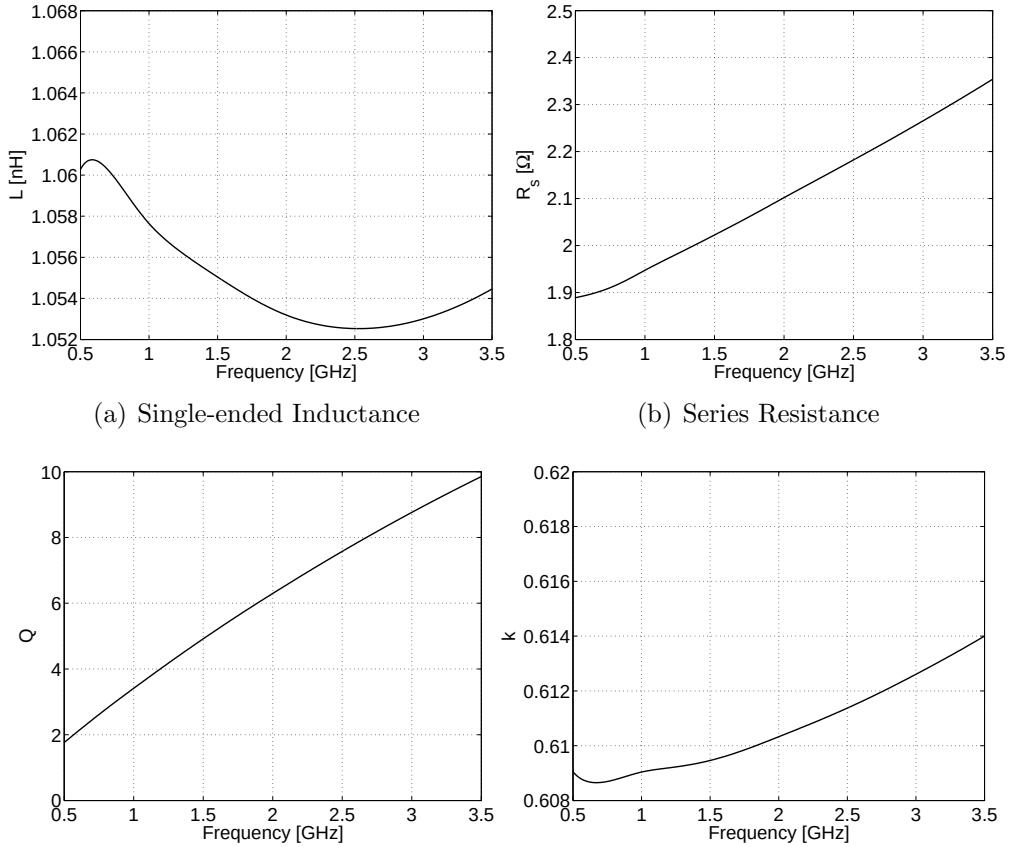
A different solution which could come in mind to save some area is to put the coils on different metal layers. In this case, however, a substantially higher sheet resistance of the lower metal layer would lead to an asymmetric transformer which in this case is an unwanted effect.

It is important to underline that the transformer has been accurately simulated with an EM simulator. In fact all the parameters here reported have been extracted from this simulation results, which are reported in figure 2.12. An important thing to observe is that the figures 2.12(a) and (c) do not take into account the coupling. So they represent the inductance and quality factor values of one inductor while the other is an open-circuit. The effective values are increased by the $(1 + k)$ factor.

2.3.2 Varactors Design

In the previous section the transformer has been analysed. The other important elements are the variable capacitors, which will be analysed here.

As anticipated, a variable delay element is able to change its delay configuration and this can be done replacing the capacitors with varactors. A varactor is a component which offers a variable capacitance depending on the voltage of the control signal (DC bias). Different possible configurations exist to obtain a varactor in CMOS technology (see [20, 21]). The configuration used in this work is the differential nMOSFET varactor reported in figure 2.13. As it can be seen the signal in this case is applied to the gates terminal while the control signal is applied to the drain/source terminals (the bulk terminal is grounded). The common mode voltage is put to V_{DD} in order to have a



(a) Single-ended Inductance

(b) Series Resistance

(c) Quality Factor

(d) Coupling Coefficient

Figure 2.12: Sonnet simulations results

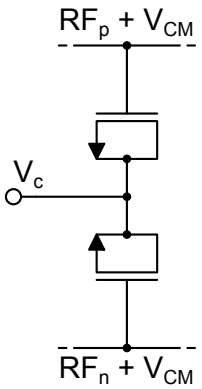


Figure 2.13: Differential MOS-varactor

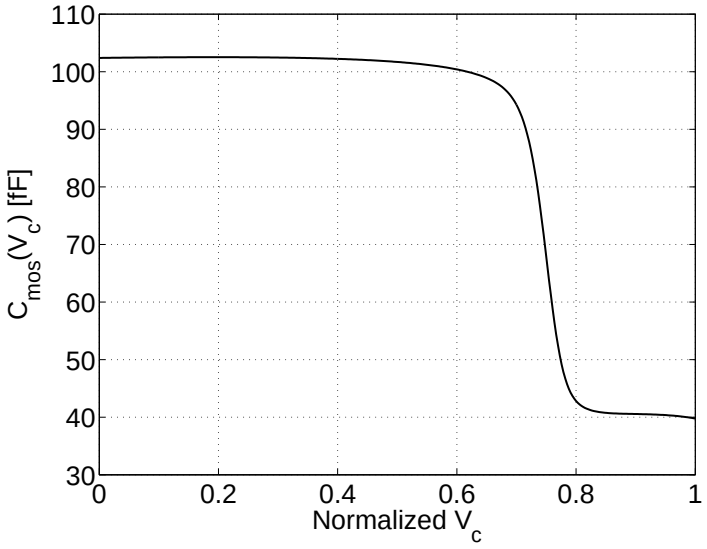


Figure 2.14: C_{mos} as a function of $\frac{V_c}{V_{DD}}$

positive control signal voltage $V_c \in \{0, V_{DD}\}$.
When the control voltage is 0 the gate-source voltage is greater than the threshold voltage of the MOS and the channel is formed; the varactor is in the maximum capacitance configuration

$$C_{MAX} = \frac{1}{2}(C_{gc} + C_{ol(s)} + C_{ol(d)}) \tag{2.21}$$

Note that the 1/2 factor is present because the differential capacitance is considered.
On the other hand, when the control voltage is V_{DD} the gate-source voltage is lower than the threshold voltage; the varactor is in the minimum capacitance configuration

$$C_{min} = \frac{1}{2}(C_{gb} + C_{ol(s)} + C_{ol(d)}) \tag{2.22}$$

The resulting differential varactor capacitance is reported in figure 2.14, in function of the control signal. The asymmetry (the transition from the maximum to the minimum capacitance value is around $0.8V_{DD}$ and not $0.5V_{DD}$) comes from the fact that the common mode voltage is set to V_{DD}. It can be made symmetric lowering the common mode, however this is not necessary

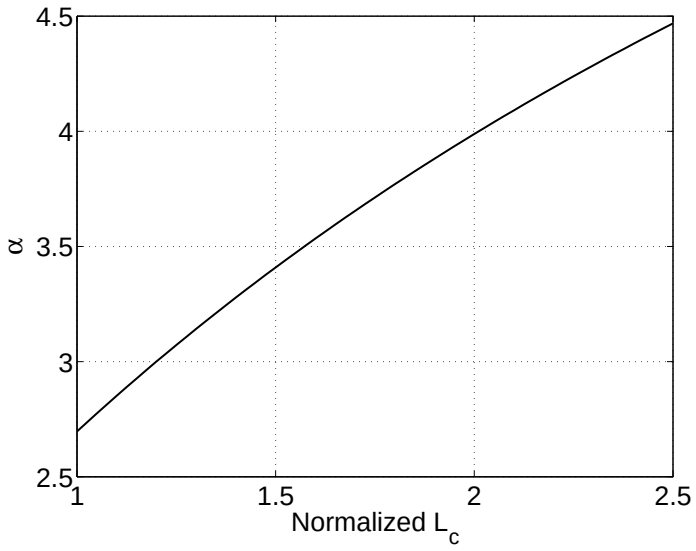


Figure 2.15: α in function of $\frac{L_c}{L_{min}}$

in this case. Furthermore, a voltage reference would be needed in this case. From the design point of view, as it has already been seen, the ratio between the maximum and minimum capacitance is also important:

$$\alpha = \frac{C_{MAX}}{C_{min}} \tag{2.23}$$

In fact, the delay difference depends directly on it. It can be shown that this coefficient depends only on the channel length, at least as soon as the channel width W is much higher than the channel length L_c. This fact is shown in the appendix C. In figure 2.15 the α coefficient is plotted in function of L_c and this plot is very useful for the design. Note that this curve does not take into account the parasitic capacitances due to the layout, which are inevitably present. Their presence results in an α coefficient reduction which depends on the transistors dimensions and should be taken into account during the design.

Another important parameter is the quality factor of the varactor and it

$W[\mu m]$	$L_c[\mu m]$	nf	$C_{min}[fF]$	$C_{MAX}[fF]$	α	$R_g[\Omega]$	$Q(2GHz)$
$116.3L_{min}$	$1.22L_{min}$	9	40	104	2.6	10.2	48

Table 2.3: Characteristics of the nMOSFETs used to realize the varactor

basically depends on the parasitic gate resistance R_g. It is defined as:

$$Q = \frac{1}{\omega C R_g} \tag{2.24}$$

and considering that two possible configurations are present the maximum capacitance case is usually considered, which represents the worst case for Q. The gate resistance depends on mainly two factors in this case: the layout and the channel resistance [21]. A poorly edited layout can heavily influence the quality factor of the varactor so it is important not to neglect this fact. For example, a multi-finger transistor helps to keep low this contribute because it shorten the connections. The channel resistance, instead, is a function of the ratio between the channel length and width. Therefore a lower channel length means lower channel resistance. On the other hand, however, the α coefficient is proportional to the channel length and a low α value means less delay per cell. In this case, to keep the delay constant, bigger components should be used and this results in a lower bandwidth. It is thus important to find a compromise between α and the channel resistance.
The characteristics of the nMOSFETs used to realize the final varactor are summarized in table 2.3.

2.3.3 Design Summary

In the previous two sections the design of the passive elements has been analysed in detail. The summary of the designed cell characteristics is here reported.
The final cell is represented in figure 2.16. It has been designed to obtain a

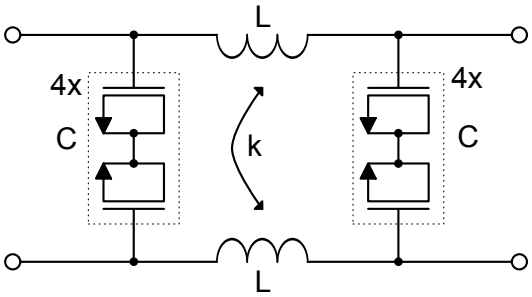


Figure 2.16: Final cell

variable delay of $17ps$ and exhibits a characteristic impedance from $Z_{0c,min} = 59\Omega$ to $Z_{0c,MAX} = 84\Omega$; hence, the optimal characteristic impedance is 70Ω. From the figure, it is also visible that the capacitor has been replaced with the parallel of four varactors and each varactor is driven by a different control signal. Thus 4-bits are necessary to chose the desired delay with steps of $4.25ps$. This results in a total area of $270 \times 250\mu m^2$.

2.4 Delay Extension and Control

In the previous section the design of the cell which presents a delay variation of $17ps$ has been done. The total delay variation of $68ps$ has been obtained by the cascade of four of this cells fulfilling hence the specifications.
Each cell has four different delay configurations and to achieve this a 4-bit control signal is necessary. With four cells a 16-bit control signal is required. A simply way to do this is with a Serial-Parallel Interface (SPI), for example a shift register.
An important issue rises at this point and it regards the manner in which should be controlled the delay. In fact many different ways exists to program a specific delay; for example, a delay of $2 \times 4.25ps = 8.5ps$ can be obtained turning on two couples of varactors in the same cell but also turning on two couples of varactors in two different cells (one per each cell).
Considering a single cell, it has been seen that different delay configurations results in a different characteristic impedance Z_{0c}. Hence, considering the cascade of cells, a different delay configuration means also that the charac-

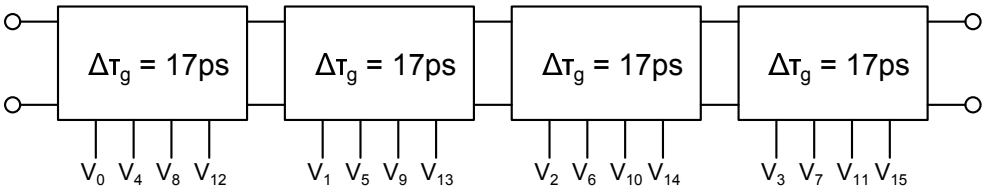


Figure 2.17: Delay extension with an optimal delay control solution

teristic impedance between cells are different. Higher is this difference higher are the reflections between cells, which results in higher losses.
In this work an optimal solution has been implemented turning on as first a couple of varactors per each cell, then the second one and so on. In this way the difference in characteristic impedance between cells is minimized and hence also the losses. The block diagram of this solution is reported in figure 2.17. The whole delay line occupies an area of $1080 \times 250 \mu m^2$, excluding the shift registers which, as will be seen in the layout chapter, requires a small amount of area.

2.5 Another Explored Topology

During the the design of the phase shifter, besides the finally implemented loaded-line solution, another topology which is worth to be mentioned has been analysed. The technology used in this work has a high resistive substrate which makes available good RF switches. In this explored solution it has been tried to exploit these devices to obtain better performances compared to loaded-line case, especially concerning the insertion loss.
The circuit which has been tried to implement is based on the reduction of the number of stages used, thus reducing the parasitic resistances due to the inductors and hence potentially decreasing the insertion loss ([32]). It is based on the two stages block diagram reported in figure 2.18. The first stage is a fine delay element (FDE) and it gives the fine tuning of the total delay. It can be realized with the π-network topology previously used for the final design of the delay line. The second stage, instead, is made of a coarse delay element (CDE) and it covers much more delay than the FDE

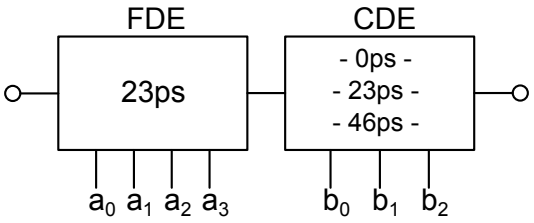


Figure 2.18: Fine - Coarse tuning concept

but with a lower resolution (delay step variation). The choice between the various path in the CDE is made with switches put at both input and output, in a similar way it is done in the switched-line phase shifter previously presented, but with 3 possible signal paths. The CDE can be seen as made of more switched-line topologies put in parallel to give more delay configurations. The various paths can be also realized with a π-network topology, but with a fixed time delay. To have a consistent comparison it has been tried to achieve the same delay of the delay line previously analysed ($68ps$). This can be obtained with a FDE with a total delay variation of $23ps$ and a CDE with a total delay variation of $46ps$ with a resolution of $23ps$ (2 possible steps). The choice of this configuration derives from the fact that more than one stage of CDEs increases proportionally the number of switches and hence the losses. On the other hand, more paths in the single CDE increase the parasitic capacitances at the nodes and hence reduce the bandwidth. In fact, to compensate the presence of these capacitances, which results in a higher delay for the reference case, more delay is required from the other paths, which results in a reduction of the bandwidth.
Different simulations have been done trying to make better this circuit compared to the loaded-line but the insertion loss was still higher. Moreover some other problems have been encountered. One of them is the fact that the FDE should have a higher delay than the $23ps$; in fact, it should cover a $15 \div 20\%$ more than the CDE step to cover PVT variations. This results in an even more reduction of the bandwidth which could be overcome by realizing the FDE with two cells; in fact lower delay per cell means higher bandwidth as it has been shown in equation 2.16. However, this solution would increase the losses. Another problem was the different behaviour of

the various delay curves due to the differences between the bandwidths of the FDE and CDE. In fact, a FDE has a definitely lower bandwidth than the CDE for the same total delay variation. This resulted in the crossing of some of the delay curves, even in the bandwidth of interest. The problem is again due to the FDE which has a low bandwidth. All these considerations brought to prefer the loaded-line solution instead of the fine-coarse concept here presented.

2.6 Summary

In this chapter different types of phase shifters have been presented and among them the lumped transmission line has been deeply analysed and used to design a TTD phase shifter (delay line).
The design started from the single cell delay line, which has been made to give a delay variation of $17ps$. 4 of this cell have been then put in cascade to obtain an overall delay line with a total delay variation of $68ps$. It exhibits a characteristic impedance which varies from $Z_{0c,min} = 59\Omega$ to $Z_{0c,MAX} = 84\Omega$; hence, the optimal characteristic impedance is 70Ω. It is controlled by a shift register with 16-bits which give a resolution of $4.25ps$. This results in a total area of $1080 \times 250\mu m^2$.

Chapter 3

Analysis and Design of an Attenuator

In the introduction some of the applications in which attenuators can be used have been presented. In phased arrays, for example, it can be used with a phase shifter to the change the pattern of a multiple-antenna system while in the Doherty power amplifiers it is used to compensate for the mismatch between different stages and hence optimize the power amplifier efficiency.
In this chapter, attenuators are discussed more in detail. Different possible ways in which they can be realized are presented and among them the π-network topology is chosen for the design of a variable attenuator for DPA application. The topology is analysed in detail deriving all the necessary equations and the design is then performed to satisfy the target specifications.

3.1 Introduction to Programmable Attenuators

An attenuator is a passive two port network which permits the control of the amplitude of the input signal by means of a control voltage (DC bias). In other words, considering the notation reported in figure 3.1, it is possible to control the parameter A. In an attenuator this value is lower or equal than 1 ($|A| \leq 1$) while in an amplifier it is higher or equal than 1 ($|A| \geq 1$). More-

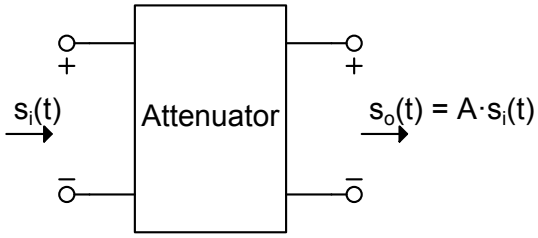


Figure 3.1: 2-port attenuator

over this attenuation should be, ideally, achieved without phase shifting. In fact, attenuators are usually realized with resistors which ideally should not introduce phase differences between output and input. In practice, however, parasitic capacitances are associated with these resistors and hence phase shifting is present. In this case, depending on the application, it could be desirable to have a constant phase shift over different attenuation configurations (e.g. phased arrays).

From the technology point of view, attenuators are often made in GaAs ([34]-[37]) which makes available good performance RF switches, resulting thus in low insertion loss circuits. However this technology is quite expensive and often a cheaper solution is wanted. In these cases CMOS technologies ([38]-[41]) are used at the expense of higher losses. However, if a high resistive substrate process is available, good RF switches can also be obtained in CMOS technologies. Fortunately this process has been available for this work and it has been fully exploited.

Attenuators can be distinguished in analog and digital ones. In *analog attenuators* ([37]-[40]), the attenuation can be varied in a continuous manner by means of a continuous variation of the control signal. For example, a continuous current bias is used in circuits made of pin diodes to change their resistance while a continuous voltage bias is used in circuits containing FETs. In *digital attenuators* ([34]-[36],[43]), instead, the attenuation can be programmed within a finite set of values. The latter ones are covered in this work.

Several designs of digital attenuators have been demonstrated in literature, and almost all of them can be placed in one of the following groups: switched-

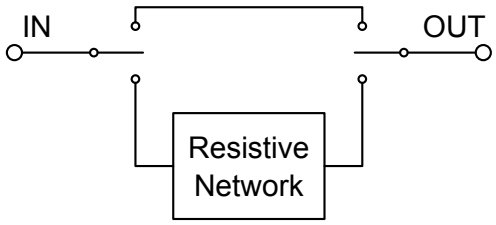


Figure 3.2: Switched-path topology

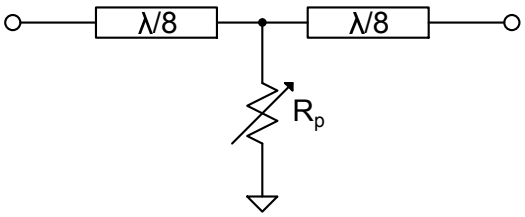
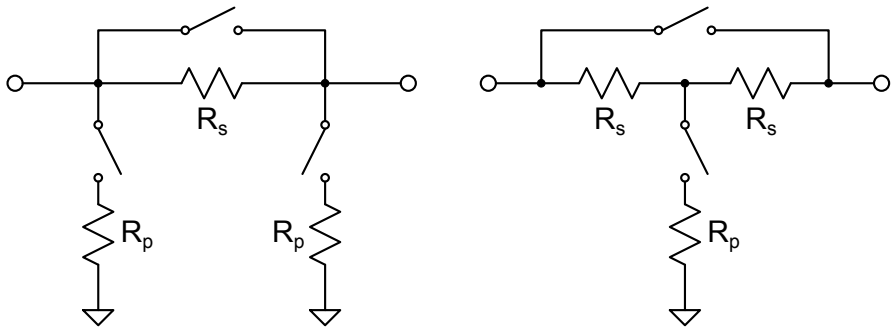


Figure 3.3: Distributed attenuator

path attenuators (Fig. 3.2), distributed attenuators (Fig. 3.3) and switched-π/T attenuators (Fig. 3.4). *Switched-path attenuators* ([34]) consist mainly of a cell with two possible path for the signal. One path is the reference case and it should, ideally, have no losses; the other path is a resistive network and it determines the attenuation of the cell. The resistive network is usually realized with one of the topologies in figure 3.4 where the switches are removed and replaced by a short-circuit if they are shunt switches or by an open-circuit if they are series switches. The choice of the path is made by SPDT switches and two of them are needed for each cell, hence the insertion loss of this type of attenuators is usually high. It requires a large chip area but shows low phase variation over different attenuation states.

In *distributed attenuators* ([42],[43]), instead, the concept is to use transmission lines loaded with a variable resistor. In this way, considering that no series switches in the signal path are present, they have the advantage of low insertion loss. However, the number of variable resistors and transmission lines increases linearly with the number of attenuation states. Hence if the design requirements are both high resolution and low attenuation this topology will occupy a large chip area.

Switched π-T attenuators ([36]-[41]) are somewhere in the middle between



(a) Switched π-Network (b) Switched T-Network

Figure 3.4: Switched π/T networks

the previous two solutions in the sense that a single series switch is used. Two basic circuits are reported in figure 3.4 and other variants slightly differ from these ones. The concept here is that the circuit presents two different topologies. In the reference case (low insertion loss) the series switches are in the closed state to bypass the network while the shunt switches are in the open state. In the attenuation case, instead, the shunt switches are in the closed state while the series switches are in the open state. The desired attenuation is obtained with a proper design of the resistors. The choice of which one of the two networks to use depends mainly on the resistors feasibility (see [33]). In fact, considering that different networks gives different resistors values, it could be convenient to chose one instead of the other. These topologies have a single series switch which allows to keep the insertion loss low. However, the switches parasitic capacitances are dependent on its open/closed state which causes a different phase shift in the two cases and sometimes it could be a problem.

In all of these topologies a single cell has been described which gives one possible attenuation state (besides the reference state), that is a 1-bit attenuator. N-cells should be put in cascade to obtain an overall N-bit attenuator.

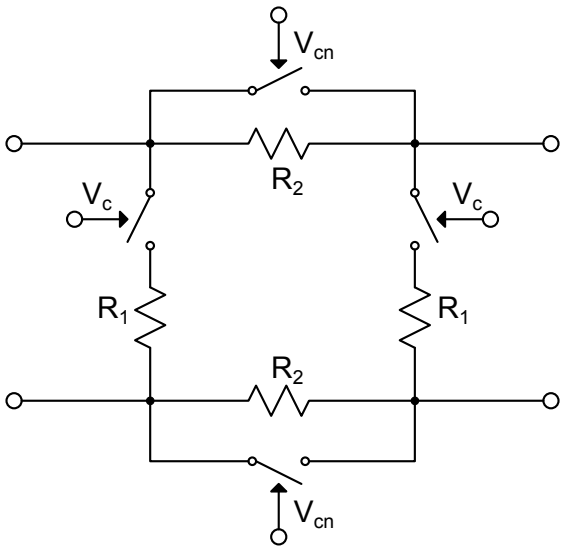
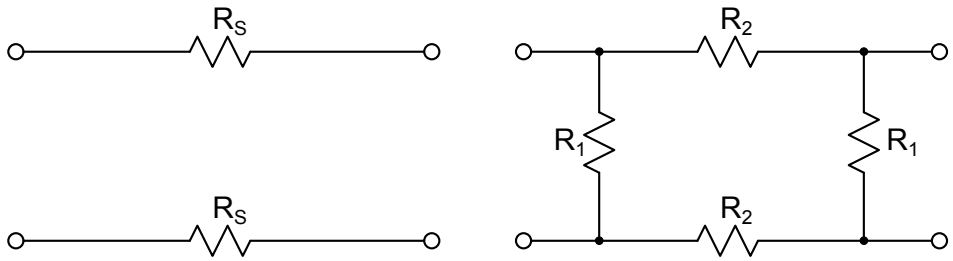


Figure 3.5: Designed cell. V_{cn} is the inverted V_c signal

3.2 π-Network Attenuator

In the previous discussion different types of attenuators have been presented. Among them the switched π-network has been chosen for this work. It gives a good compromise between loss, phase variation and resistors feasibility. It is here deeply analysed extracting the equations which will be then used for its design.

The complete schematic of the switched π-network cell is reported in figure 3.5. This network is the differential version of the single-ended π-network reported in figure 3.4(a). Depending on the control signal V_c two different topology states are possible for this circuit and they are reported in figure 3.6. When the control signal is low ($V_c = 0$), the shunt switches are in the open state while the series switches are in the closed state and they bypass the R_2 resistors minimizing the insertion loss and maximizing the input/output matching. In this case the topology of figure 3.6(a) should be considered and it represents the reference case. The R_s resistors represents the series resistances due to the switches, which in this case are implemented with MOSFET devices. These resistances directly leverage the insertion loss of the cell, hence they should be as low as possible. Attention must be paid



(a) Reference state (b) Attenuation state

Figure 3.6: The 2 possible topologies

on the fact that to obtain a lower resistance, bigger transistors are needed, which results in higher parasitic capacitances associated to the transistors. As it will be seen later, they can degrade the performance of the circuit in terms of bandwidth and phase variation. It is important to notice that here, and in the following discussion, it has been assumed that $R_s \ll R_2$. This will be mainly satisfied. If it is not then also the effect of the R_2 resistance should be considered, which presence results in a lower insertion loss.
When the control signal is high ($V_c = V_{DD}$), the series switches are in the open state while the shunt switches are in the closed state and the resulting topology is represented in figure 3.6(b). In this case both R_1 and R_2 resistances are present and their purpose is to ensure both the desired attenuation and input/output matching.
In the following discussion the equations representing the behaviour of the two circuits are found. They will be then used for the design of the various cells in the next section. First of all it is assumed that the source and load impedances are the same and equal to Z_0. Starting then from the reference case (Fig. 3.6(a)) the ABCD-matrix is easily calculated from the generic ABCD-matrix, which has already been calculated in the appendix A, and results:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 2R_s \\ 0 & 1 \end{bmatrix} \tag{3.1}$$

Remembering the equations 1.9 and 1.11, reported in the introduction, which relates the ABCD-parameters to the S-parameters, it is possible to calculate

the reflection coefficient S_{11} and the transmission coefficient S_{21} as:

$$S_{11} = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 + D} \tag{3.2}$$

$$S_{21} = \frac{2}{A + B/Z_0 + CZ_0 + D} \tag{3.3}$$

The coefficients S_{22} and S_{12} are not reported since the network is symmetric and they are equal to S_{11} and S_{21}, respectively. This is true as soon as the source and load impedances are the same.
Starting from the first expression and looking for the matching condition which, as it has been seen in the phase shifter chapter, derives from the request for the absence of reflections at input (output) $S_{11} = 0$ it can be found that:

$$S_{11} = 0 \quad \Rightarrow \quad R_s = 0 \tag{3.4}$$

This equations says that the matching condition is satisfied when the series resistance associated to the switches is zero which actually is easy to see considering also that the input impedance of this network is $Z_i = Z_0 + 2R_s$. This task, however, is impossible to achieve in practice, but nevertheless it is not a problem. In fact if R_s is small enough compared to Z_0, the matching still remains acceptable. For example, if $R_s = 1\Omega$ and $Z_0 = 50\Omega$ the reflection coefficient is smaller than $-34dB$ which is anyway a good value.
From the equation 3.3, instead, it is possible to calculate the transmission coefficient S_{21}, which results:

$$S_{21ref} = \frac{Z_0}{Z_0 + R_s} \tag{3.5}$$

When the matching condition is fairly satisfied, the insertion loss is mainly due to the losses introduced by the transmission coefficient S_{21ref}. This is the reason way it should be minimized. Looking into the last equation it is clear that also this task is achieved when $R_s \to 0$. Hence, to optimize the performance of this network, the MOSFETs should be made as big as possible, at least as soon as the bandwidth and phase variation do not become a problem.

Considering now the attenuation case topology (Fig. 3.6(b)) the ABCD-matrix is again calculated from the generic ABCD-matrix in the appendix A and results:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{R_1+2R_2}{R_1} & 2R_2 \\ \frac{2(R_1+R_2)}{R_1^2} & \frac{R_1+2R_2}{R_1} \end{bmatrix} \tag{3.6}$$

As done for the reference case, this matrix can be used to calculate the S-parameters. Starting from the reflection coefficient equation and looking for the matching condition (absence of reflections) it can be found that:

$$S_{11} = 0 \quad \Rightarrow \quad R_1^2 R_2 = Z_0^2 (R_1 + R_2) \tag{3.7}$$

An interesting observation can be made if the impedance Z_0, which in this case represents the source and load impedances, is written in function of the other two resistances:

$$Z_0 = R_1 \sqrt{\frac{R_2}{R_1 + R_2}} \tag{3.8}$$

This equation says that if the source/load impedance is equal to the expression on the right side then the matching condition is satisfied. But considering that the matching condition is satisfied when the source and input impedances are equal ($Z_0 = Z_i$) then the last expression represents also the input/output impedance of the circuit.
Focusing now on the transmission coefficient S_{21} it can be found that:

$$S_{21att} = \frac{R_1^2 Z_0}{Z_0 R_1 (R_1 + 2R_2) + R_1^2 R_2 + Z_0^2 (R_1 + R_2)} \tag{3.9}$$

From the design point of view the transmission coefficient S_{21att} is a fixed parameter and depends on the desired attenuation. The source/load impedance, instead, is often decided based on the interfacing circuits. Hence, the two resistances are the variables which should be determined in function of the other two parameters (S_{21att}, Z_0). Considering the system made of the last two equations (3.8, 3.9), which means looking for solutions which satisfy both the matching condition and desired attenuation, the resistances R_1 and R_2

can be expressed in function of S_{21att} and Z_0 as:

$$R_1 = Z_0 \frac{1 + S_{2att1}}{1 - S_{21att}} \tag{3.10}$$

$$R_2 = Z_0 \frac{1 - S_{21att}^2}{4S_{21att}} \tag{3.11}$$

It can be seen that to have meaningful solutions the transmission coefficient should be $0 < S_{21} < 1$ which is in agreement with the fact that a passive circuit is used.

For the correct cell design, the equations 3.10 and 3.11 should be used together with the transmission coefficient equation 3.5 of the reference case topology. In fact, if the transmission coefficient in the reference case topology is for example $S_{21ref} = -0.1dB$, and an attenuation step of $A = 0.5dB$ is wanted, then the transmission coefficient in the attenuation case topology should be $S_{21att} = -0.6dB$ to make the difference $0.5dB$. This consideration can be represented through the following equation:

$$S_{21ref,dB} - S_{21att,dB} = A_{dB} \tag{3.12}$$

It is worth to notice that the attenuators are usually designed referring to the logarithmic scale. Hence, for example, a possible specification for the desired attenuation step can be $0.5dB$ or $1dB$. Expressing then the last equation in the linear scale it results:

$$S_{21att} = 10^{(S_{21ref,dB} - A_{dB})/20} \tag{3.13}$$

This is hence the transmission coefficient in function of the desired cell attenuation which also takes into account the losses due to the reference case and it should be used in the R_1 and R_2 equations during the design. Now that all the necessary tools for the design have been found, the design of the cells can be done in the next section.

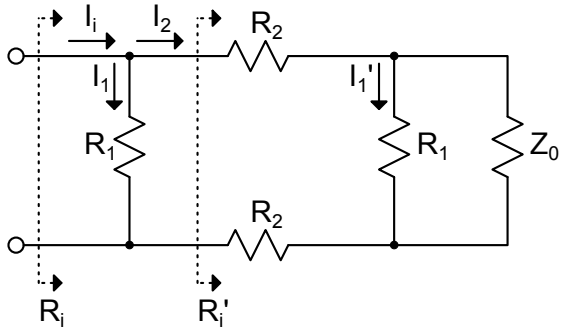


Figure 3.7: Attenuator current limits analysis

3.2.1 Current Limits

Another important thing which must be considered in this kind of circuits, especially when they have to handle high input powers, is the power dissipation capability of the resistors, usually expressed in terms of the maximum current density. This limit sets the dimension of the resistors and must be taken into account.
If P_i is the input power which should be handled by the attenuator and R_i is its input impedance (in this calculus it is supposed to be only resistive), then the input current which goes inside the attenuator is:

$$I_{i,rms} = \sqrt{\frac{P_i}{R_i}} \tag{3.14}$$

If the attenuator is in the reference state, the shunt MOSFET switches are open and the series MOSFETs carry almost all the current. If the attenuator is in the attenuation state, instead, both R_1 and R_2 carry current. It is clear that this second case must be considered to calculate the maximum currents which must be handled by the various resistors. Considering the notation reported in figure 3.7, the only currents of interest are I_1 and I_2. In fact, the current I_1' flowing through the right R_1 resistor is not important considering that it is surely lower than the current I_1 flowing through the left R_1 resistor. The currents I_1 and I_2 can be calculated through the current divider formula

and they result:

$$I_{1rms} = I_{irms}\frac{R_i'}{R_1 + R_i'} \tag{3.15}$$

$$I_{2rms} = I_{irms}\frac{R_1}{R_1 + R_i'} \tag{3.16}$$

where the resistance R_i' can be found as:

$$R_i' = 2R_2 + (R_1||Z_0) \tag{3.17}$$

Once the design has been done and all the resistances values are known, the equation presented in this section can be used to calculate the maximum currents which have to be handled by the resistors and then finally decide their dimensions.
Finally, it is worth to notice that the worst case current for the single cell is when all the other cells are in the reference state. In this case, in fact, there are no losses of current in the shunt resistors others than those of the considered cell.

3.3 Design

In the previous chapter the switched π-network topology has been analysed and all the equations describing the network have been found. In particular, equations 3.5, 3.10, 3.11 and 3.13 will be used in this section to design the cells and satisfy the target specifications presented in the introduction chapter and reported here (see table 3.1), for convenience.

From the specification table it can be seen that it is required an overall at-

$f[GHz]$	$S11[dB]$	$IL[dB]$	$\Delta A[dB]$	$Res.[dB]$	$P1dB[dBm]$
2	< -10	< 1.5	> 15	0.5	> 20

Table 3.1: Attenuator target specifications

tenuator with at least $15dB$ of attenuation and $0.5dB$ resolution. This tasks have been achieved putting in cascade 5 switched π-network cells realized in

$A[dB]$	$R_1[\Omega]$	$R_2[\Omega]$
0.5	1360	1.85
1	750	3.5
2	400	6.3
4	211	12.6
8	113	27.5

Table 3.2: Design resistances values for each stage

a binary-weighted fashion, that is the cells are made to give attenuations of $0.5dB$, $1dB$, $2dB$, $4dB$ and $8dB$ achieving an overall attenuation of $15.5dB$. Concerning the reference state, the series MOSFET switches have been designed to give a series resistance of 1Ω. This value is small enough to satisfy the requirement on the insertion loss and to keep low parasitic capacitances due to the MOS dimensions. Considering that the source and load impedances are $Z_0 = 50\Omega$, it is then possible to calculate the losses of a single cell through the equation 3.5 and the resulting transmission coefficient in this case is $S_{21att} = -0.17dB$. This value can be then used, together with the equations 3.10, 3.11 and 3.13, to calculate the values of the resistances for every stage. S_{21att} can also give an indication of the overall attenuator insertion loss if multiplied for the number of cells, that is $0.85dB$. The calculated values, for each cell, are reported in table 3.2.

Some considerations should be made now concerning the design of the R_2 resistors. In the design of the R_2 resistances the effect of the parallel switches has been taken into account. The switches have been realized with a stack of three MOSFETs that allow an increase of linearity (see [44]) and an achievement of the required 1dB-compression-point. Moreover they have an overall 10Ω resistance which in the most of the stages is negligible compared to the overall resistance. The purpose of the choice to make the shunt switches resistance negligible is twofold: (1) increase the linearity and (2) increase the matching between the R_1 and R_2 resistors. Concerning the first purpose, it is based on the fact that a lower voltage drop across the MOSFETs drain-source means that they work more toward the linear region. Putting

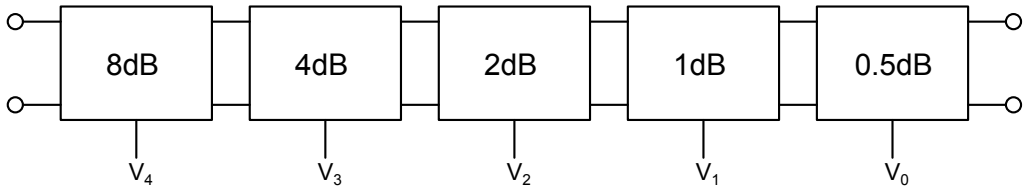


Figure 3.8: Overall attenuator

hence three transistors in series, the voltage drop between drain and source of each transistor is 1/3 compared to the case when only one transistor is present. Concerning the second purpose, instead, it derives mainly from the technology considerations. In fact, considering that R_2 resistors were made in poly-silicon, a better matching is achieved if also the R_1 resistor are made in poly-silicon.
The overall attenuator made by the cascade of the 5 cells is shown in figure 3.8. Different possible cells ordering have been tested and substantial differences have not been found between them. In this work it has been chosen to put first the stages with higher attenuation with the aim to improve the linearity of the successive stages, at least when the firsts are in the attenuation state.

3.4 Summary

In this chapter different types of programmable attenuators have been presented and among them the switched π-network has been analysed deriving all the necessary equations for the design. A cascade of 5 of this network topologies have been used to realize an overall attenuator which has a total attenuation of $15.5dB$ with the resolution of $0.5dB$. It has been designed for a 50Ω source and load impedances and shows an insertion loss of $0.85dB$. This results in a total area of $400 \times 200\mu m^2$.

Chapter 4

Layout

After the analysis, schematic-design and simulation of a circuit, another important step is the layout-design.
The layout-design consists in a creation of a physical representation of the schematic-design which must meet the requirements imposed by the manufacturing process (strip width, distance between strips, etc.); this task should be achieved trying to minimize the parasitics. In fact, the layout is a process which inevitably introduce these components, which can make the circuit work in a way not predicted by simulations.
In this chapter the layout of the schematic-designed phase shifter and attenuator is presented, with some brief considerations. The layout has been designed using Cadence Virtuoso Layout Suite. It includes tools such as Design Rule Check (DRC) and Layout Versus Schematic (LVS), which have been used to verify, respectively, that the manufacturing process requirements are satisfied and that there were no discrepancies between the schematic and the layout. Subsequently, resistive, capacitive and inductive parasitic components have been extracted from the layout using the QRC extraction functionality; then, the phase shifter and the attenuator have been simulated again, including these parasitics. These steps have been repeated some times until satisfactory performance layouts have been obtained; they are presented in the next two sections.

4.1 Delay Line

The layout of the single-cell delay line is reported in figure 4.1. Considering that the a differential topology has been used the layout has been made as symmetrical as possible. As it can be seen the varactors have been put close to the transformer, minimizing the distance between different cells and hence the losses. However, they have not been put under it because it would have increased the parasitic capacitances and hence lower the α coefficient. The cell has a dimension of $270 \times 250 \mu m^2$.
The overall delay line is obtained by the cascade of four of this cell. It results in a total area of $1080 \times 250 \mu m^2$.

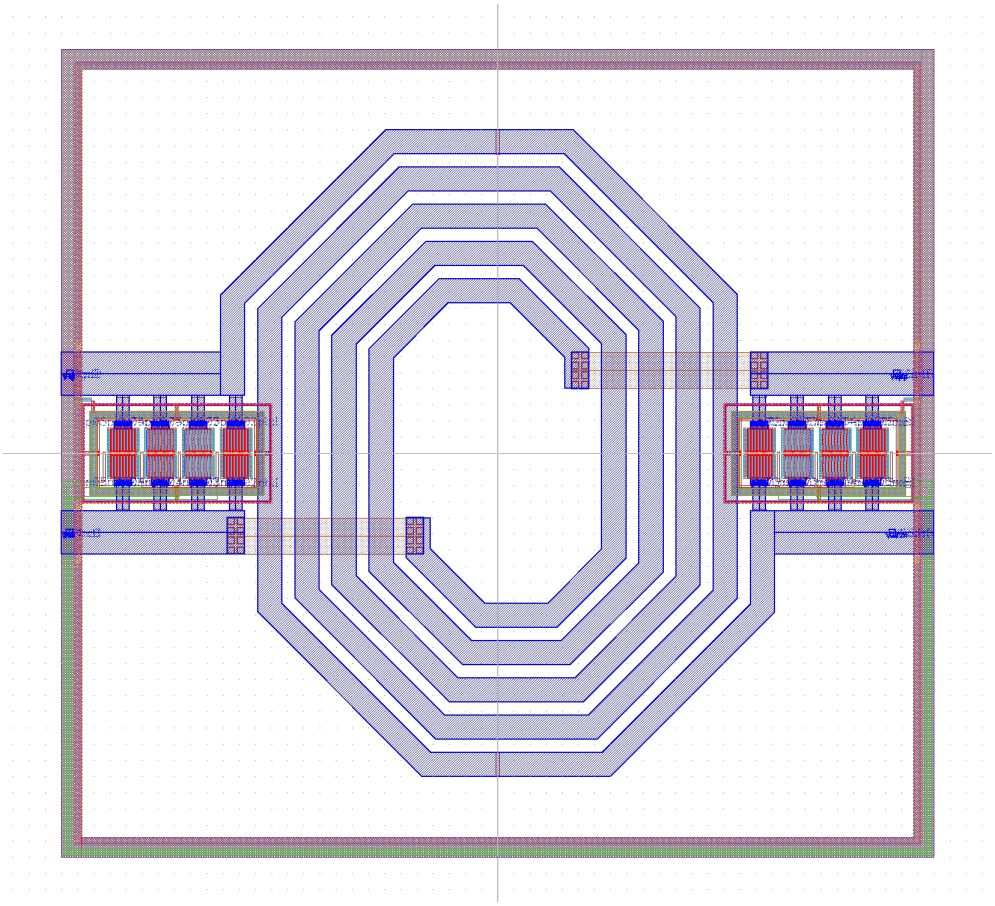


Figure 4.1: Delay line cell layout

4.2 Attenuator

The layout of the overall attenuator, obtained by the cascade of 5 π-network cells is reported in figure 4.2. Also in this case the layout has been made as symmetrical as possible. The distance between cell has been minimized, hence lowering the losses. It can be seen that the cells are different between them, especially concerning the dimensions of the poly-silicon resistors. This is due to the different attenuation steps introduced by each cell. In particular, the shunt resistor of the first stages, which have higher attenuation, have also larger dimensions because of higher currents.
The attenuator occupy a total area of $400 \times 200 \mu m^2$.

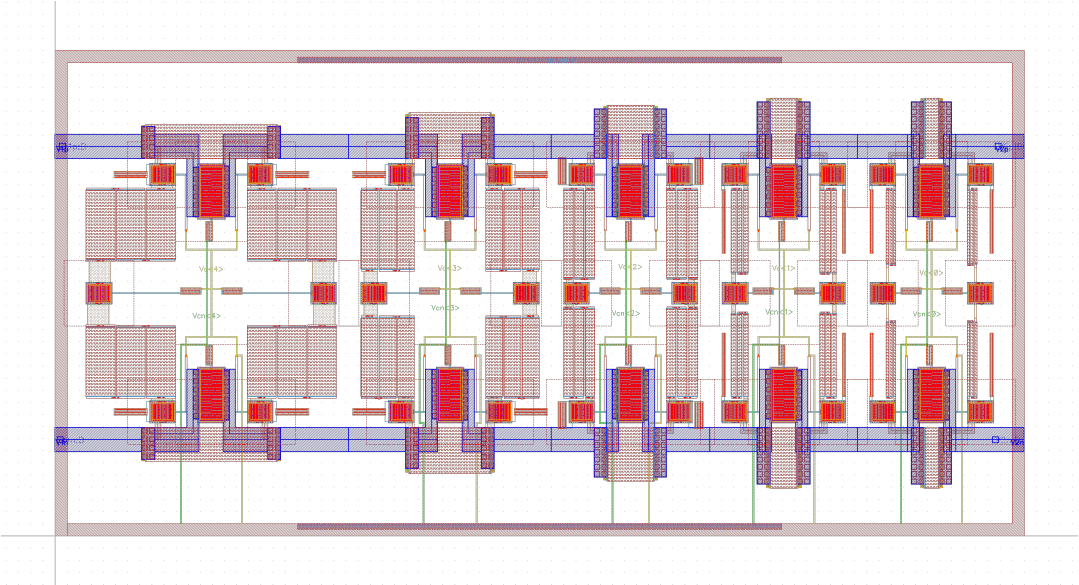


Figure 4.2: Attenuator layout

4.3 Test Chip

The layout of the test chip is reported in figure 4.3. The delay line can be seen in the upper half with the SPI used to control the delay. The attenuator can be seen in the lower half with the 5 inverters, which provide the necessary signals for the attenuation control. The total area is $1.45 \times 0.93 mm^2$.

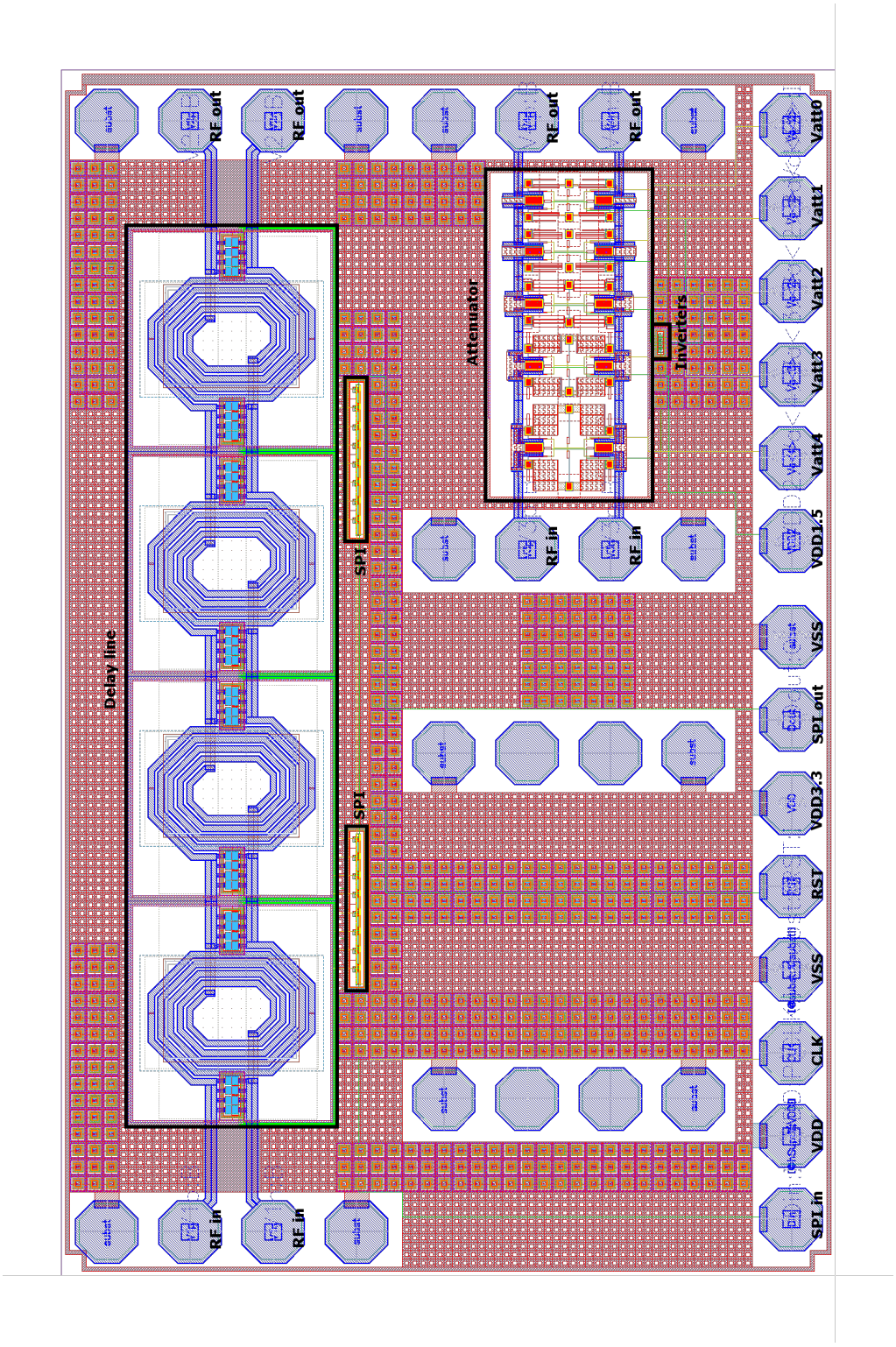


Figure 4.3: Test chip layout

Chapter 5

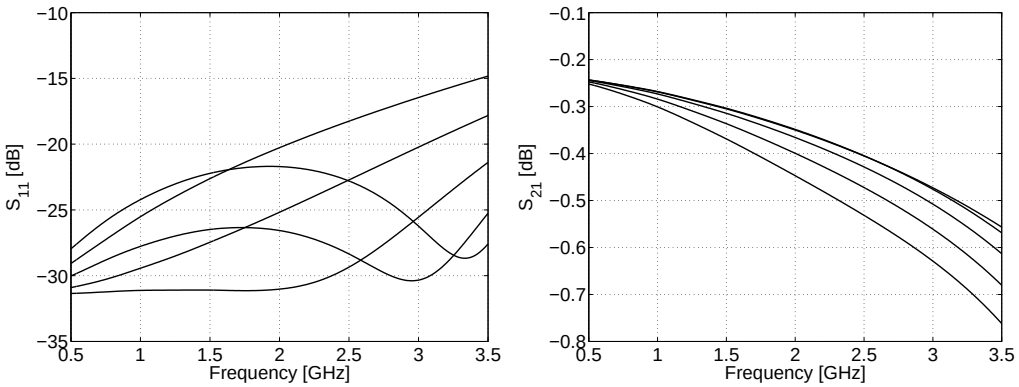
Simulation Results

In this chapter a list of results is reported with the aim to illustrate the characteristics and the behaviour of the two designed blocks. Although the results refer to simulations, they take into account the post-layout parasitic extraction.
The chapter is made of two sections: the first regards the delay line while the second the attenuator. The structure of the sections is similar and can be divided in mainly three parts. In the first part nominal simulations are reported for the two circuits. In the second part, instead, the impact of the power supply variations and temperature variations on the circuits performance is presented. Moreover, in the delay line section, results regarding the interaction between transformers are shown. The final part shows some figures extracted from Monte-Carlo simulations with the aim to quantify mismatch and process variations.

5.1 Delay line

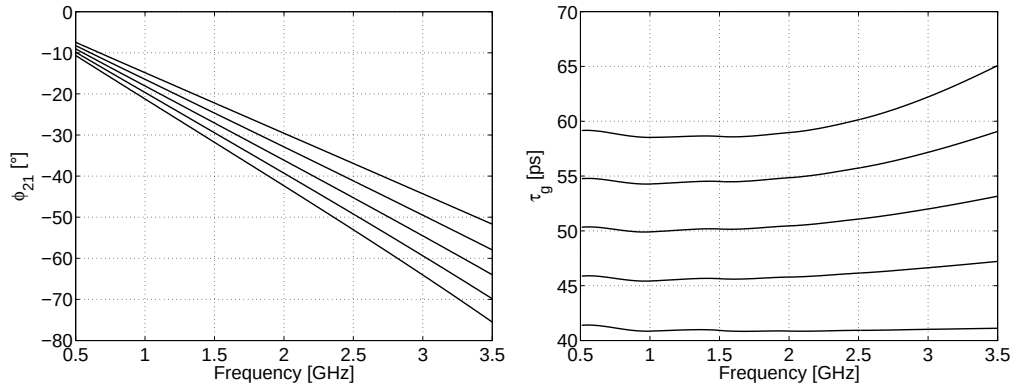
5.1.1 Nominal Simulations

Singe-cell



(a) S_{11} (b) S_{21}

Figure 5.1: S_{11} (a) and S_{21} (b) for the single cell

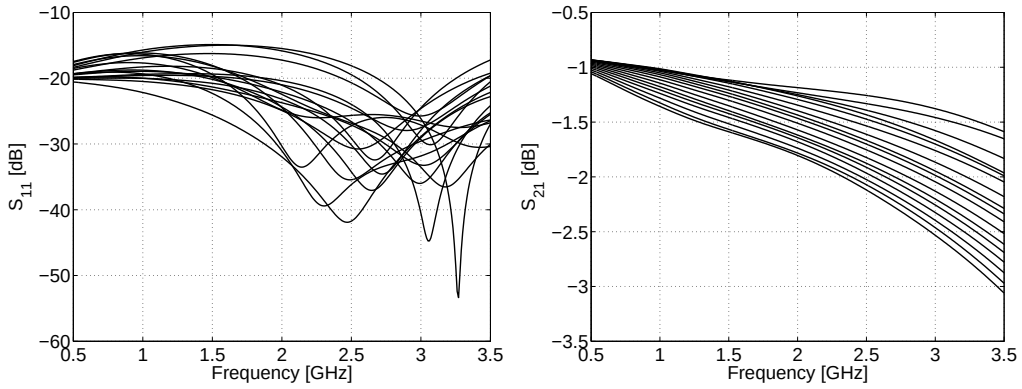


(a) $\phi(S_{21})$ (b) τ_g

Figure 5.2: $\phi(S_{21})$ (a) and τ_g (b) for the single cell

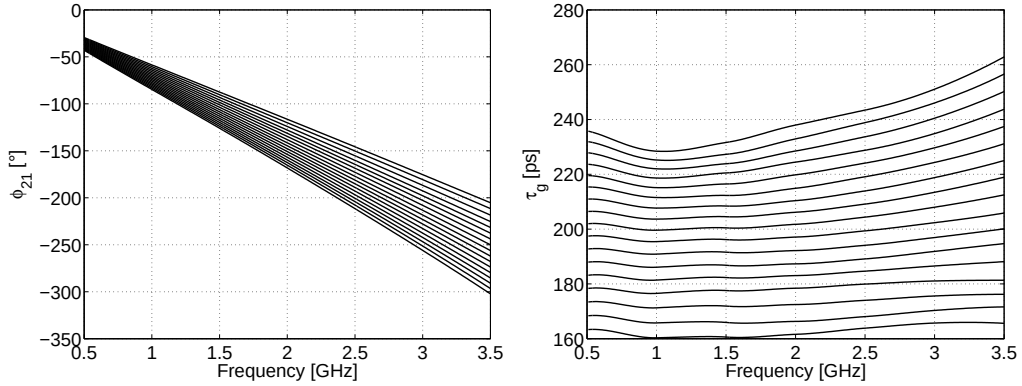
Figure 5.1, 5.2 show the behaviour of the single cell. The input(output) matching is satisfactory in the entire frequency range of interest ($S_{11} < -14.5$). The cell shows an insertion loss of $0.45dB$ and a group delay variation of $18.1ps$, at $2GHz$.

Cascade of Cells



(a) S_{11} (b) S_{21}

Figure 5.3: Input matching (a) and transmission coefficient (b) of the delay line



(a) $\phi(S_{21})$ (b) τ_g

Figure 5.4: Transmission coefficient phase (a) and group delay (b) of the delay line

Figure 5.3, 5.4 show the behaviour of the delay line, obtained with the cascade of four cells, with all possible 17 configurations (including the reference case). The input(output) matching is satisfactory in the entire frequency range of interest ($S_{11} < -14.5dB$). The cell shows an insertion loss of $1.81dB$ and a group delay variation of $76.5ps$, at $2GHz$.

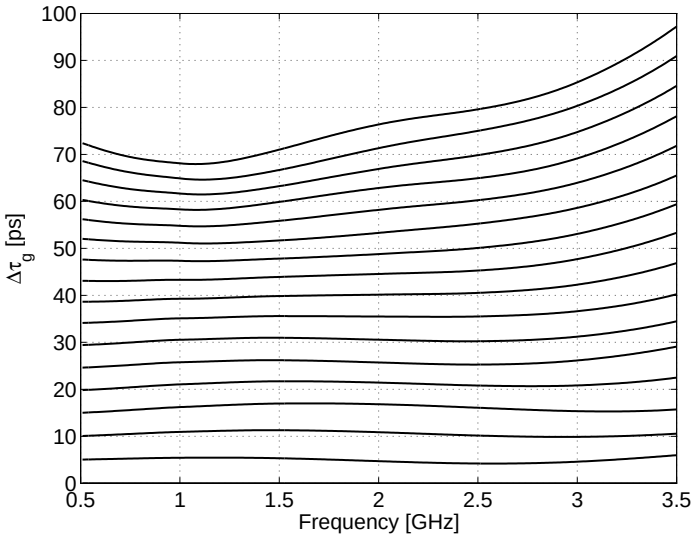
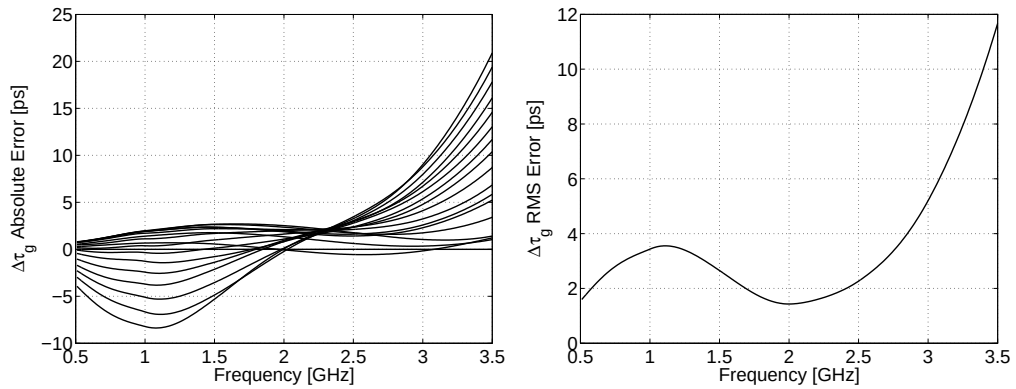


Figure 5.5: Group delay difference $\Delta\tau_g$ of the delay line



(a) $\Delta\tau_g$ absolute error

(b) $\Delta\tau_g$ RMS error

Figure 5.6: $\Delta\tau_g$ absolute error (a) and $\Delta\tau_g$ RMS error (b)

Figure 5.6 shows the absolute and RMS $\Delta\tau_g$ errors. They have been calculated with respect to an ideal delay line with the same number of steps and with the delay variation of $76.5ps$, which corresponds to the delay variation of the designed cell at $2GHz$ (as it can be seen from fig.5.5). Concerning the 1-dB compression point, it results higher than $25dBm$.

5.1.2 Power Supply Variations

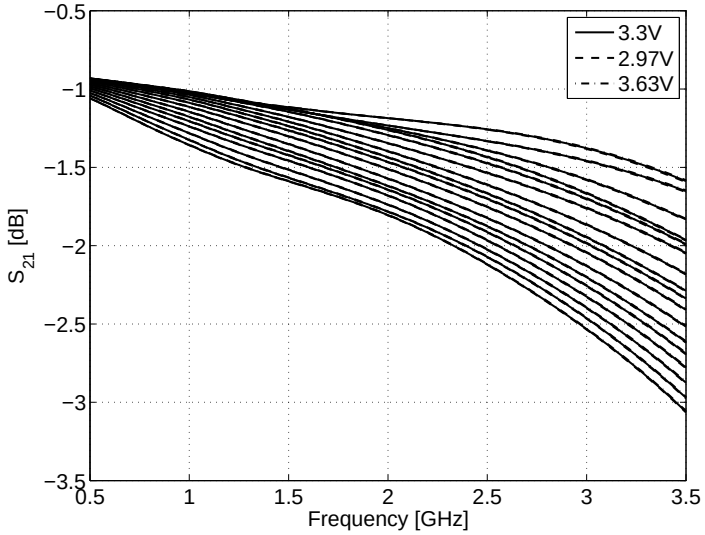


Figure 5.7: S_{21} sensibility to power supply variations

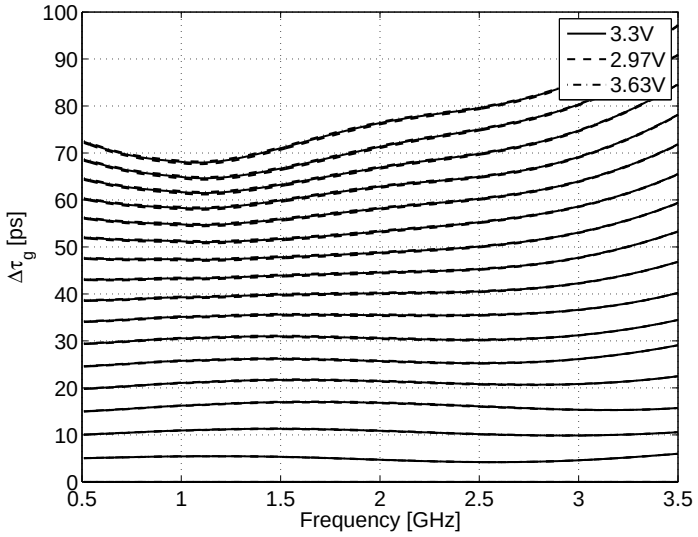


Figure 5.8: $\Delta\tau_g$ sensibility to power supply variations

Figures 5.7, 5.8 shows the sensibility of the transmission coefficient and the group delay difference to power supply variations of ±10%. The variations are minimal and almost imperceptible.

5.1.3 Temperature Variations

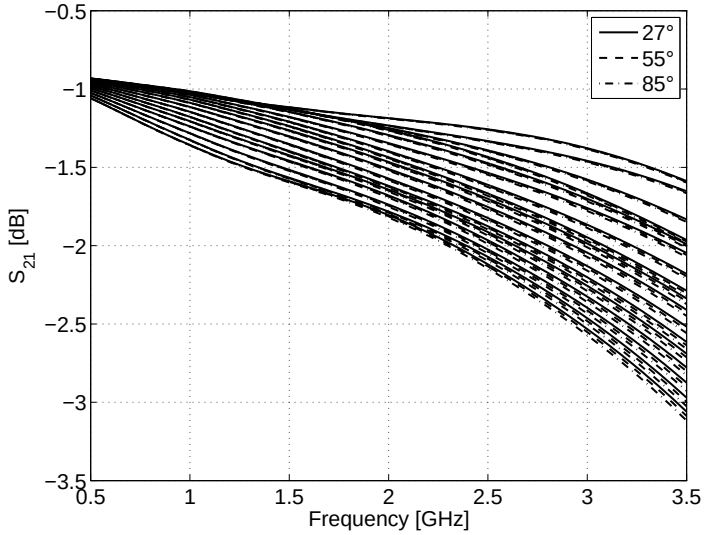


Figure 5.9: S_{21} sensibility to temperature variations

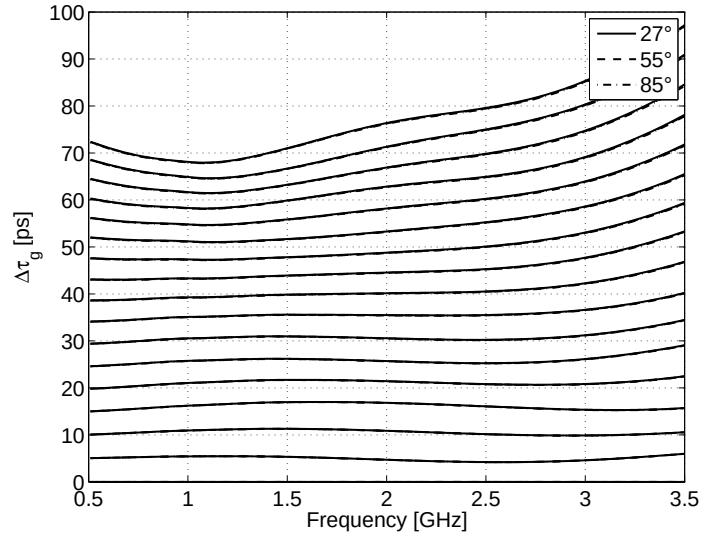


Figure 5.10: $\Delta\tau_g$ sensibility to temperature variations

Figures 5.9, 5.10 shows the sensibility of the transmission coefficient and the group delay difference to temperature variations. A subtle variation can be seen concerning the transmission coefficient.

5.1.4 Interactions Between Transformers

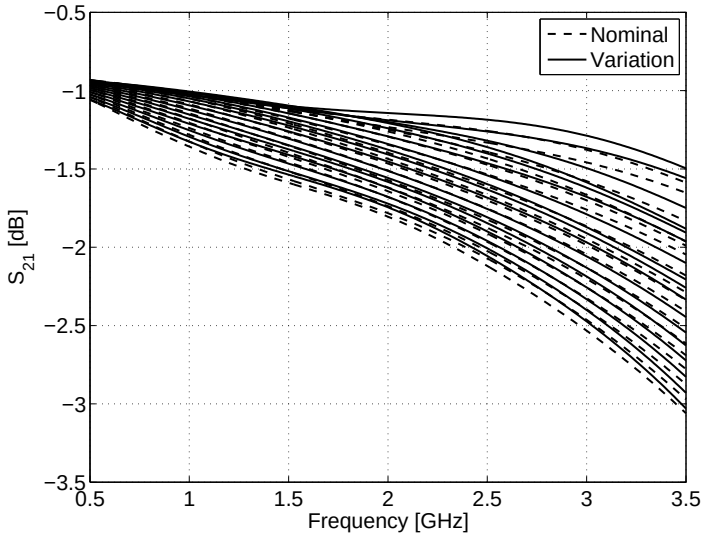


Figure 5.11: S_{21} variation due to transformers interaction

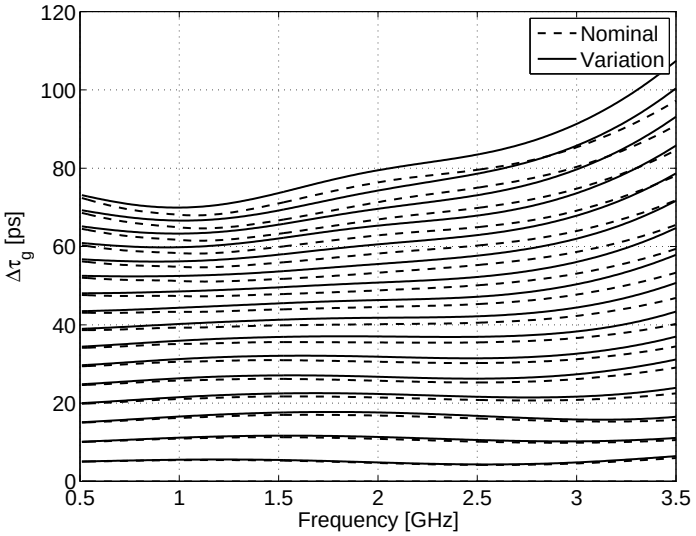


Figure 5.12: $\Delta\tau_g$ variation due to transformers interaction

Figures 5.11, 5.12 show the variations when interaction between adjacent transformers exist. In fact, the results presented so far does not take it into account because the EM simulation has been done for the single cell.

5.1.5 Monte-Carlo Simulations

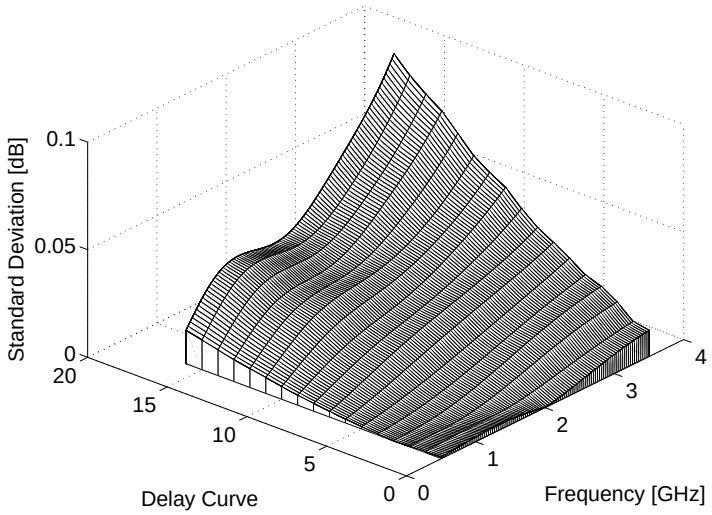


Figure 5.13: S_{21} standard deviation

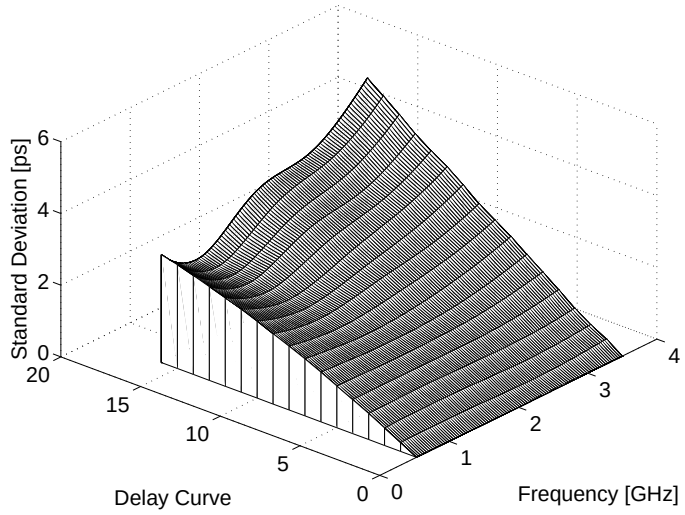


Figure 5.14: $\Delta\tau_g$ standard deviation

Figures 5.11, 5.12 show the standard deviations of the transmission coefficient and the group delay difference in function of the frequency and delay configuration, due to mismatch and process variations. Delay axis goes from 0, which represents the reference delay curve, to 16, which represents the maximum delay curve.

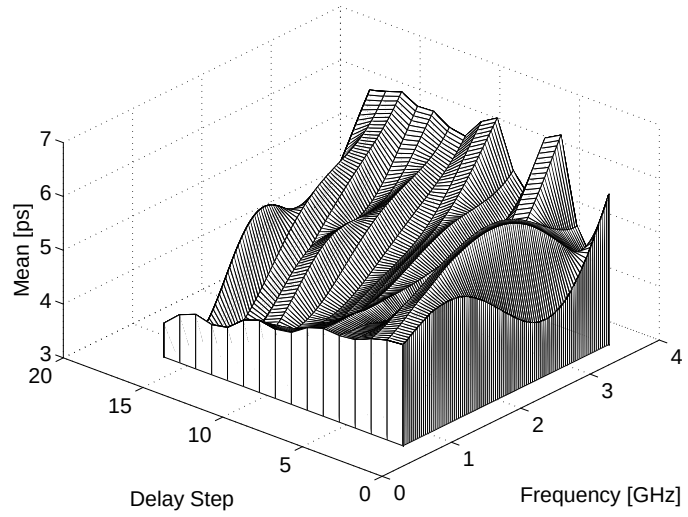


Figure 5.15: Mean of the distance between adjacent delay curves

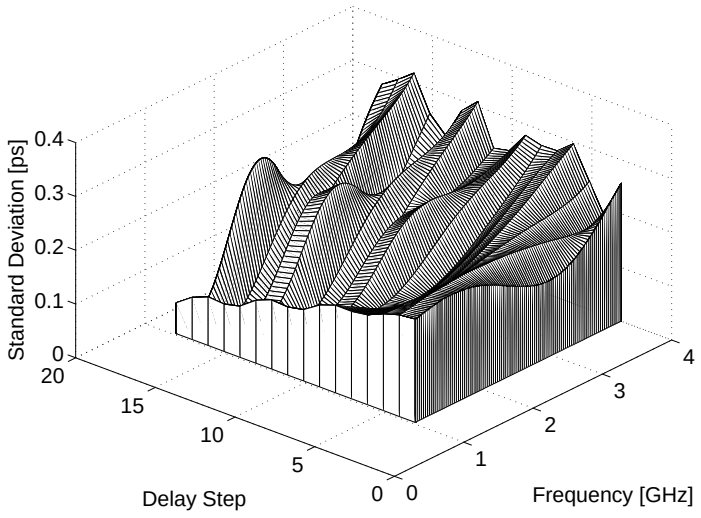
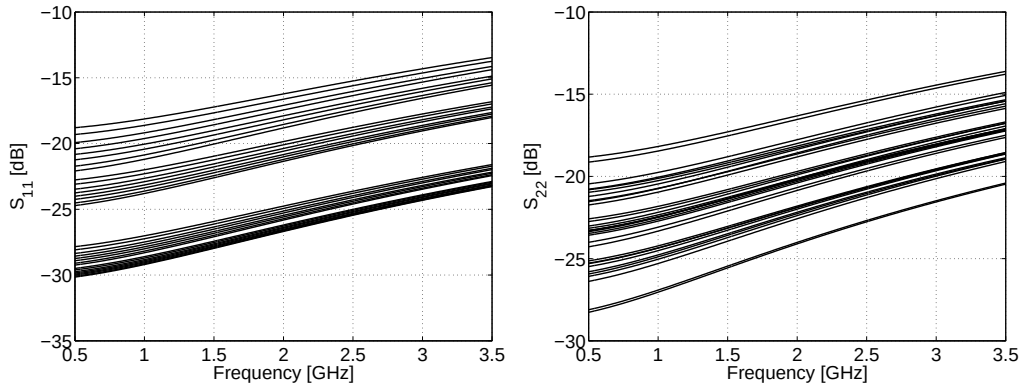


Figure 5.16: Standard deviation of the distance between adjacent delay curves

Figures 5.11, 5.12 show, respectively, the mean and standard deviation of the distance between two adjacent delay curves in function of the frequency and delay configuration, due to mismatch and process variations. Delay axis goes from 1, which represents the distance between the first two curves, to 16, which represents the distance between the last two curves.

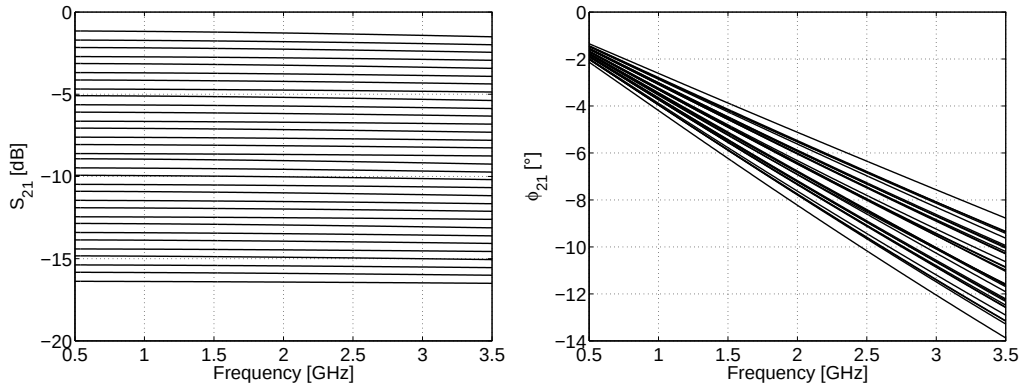
5.2 Attenuator

5.2.1 Nominal Simulations



(a) S_{11} (b) S_{22}

Figure 5.17: Input matching (a) and output matching (b) of the attenuator



(a) S_{21} (b) $\phi(S_{21})$

Figure 5.18: Transmission coefficient (a) and transmission coefficient phase (b) of the attenuator

Figure 5.17 shows the input/output matching of the attenuator. As it can be seen it is satisfactory over all the frequency range of interest, being lower than $-14dB$. The ransmission coefficient and transmission coefficient phase curves are shown in figure 5.18. The insertion loss and worst case phase variation are, respectively, $1.27dB$ and $3.1°$ at $2GHz$.

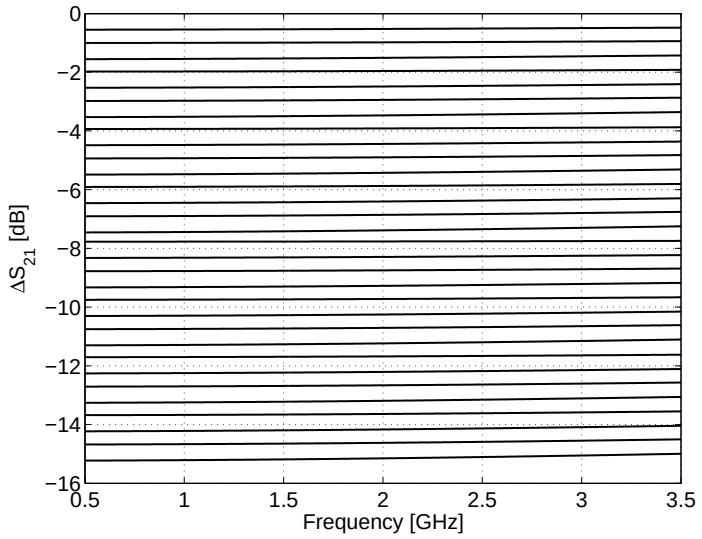
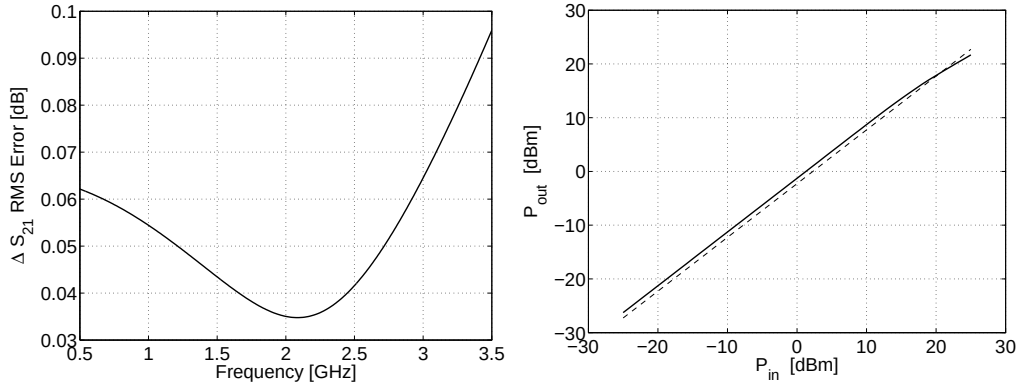


Figure 5.19: Transmission coefficient difference ΔS_{21}



(a) ΔS_{21} RMS error (b) $P1dB$

Figure 5.20: ΔS_{21} RMS error (a) and 1-dB compression point (b)

Figure 5.20(a) shows the RMS ΔS_{21} error. It has been calculated with respect to an ideal attenuator with the same number of steps and with the attenuation range of $15.15dB$, which corresponds to the attenuation range of the designed block at $2GHz$ (as it can bee seen in fig.5.19). Figure 5.20(b) shows the output power in function of the input power for the reference attenuation case. It represents the worst case concerning the 1-dB compression point, which results $20.6dBm$.

5.2.2 Power Supply Variations

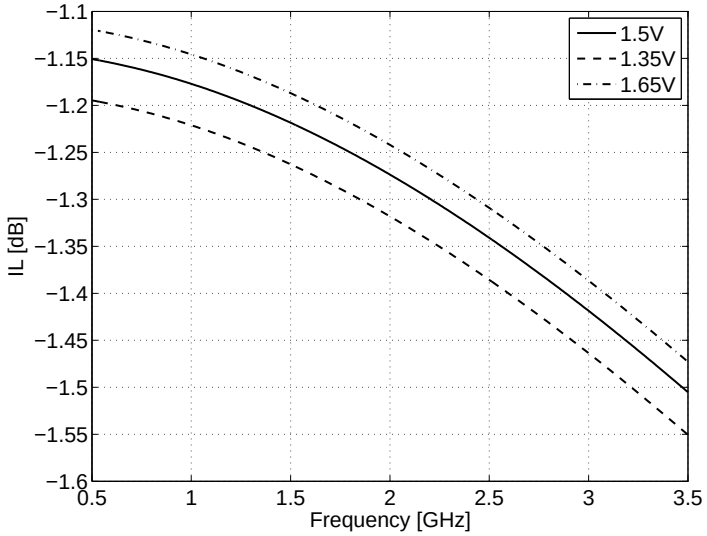


Figure 5.21: Insertion loss IL sensibility to power supply variations

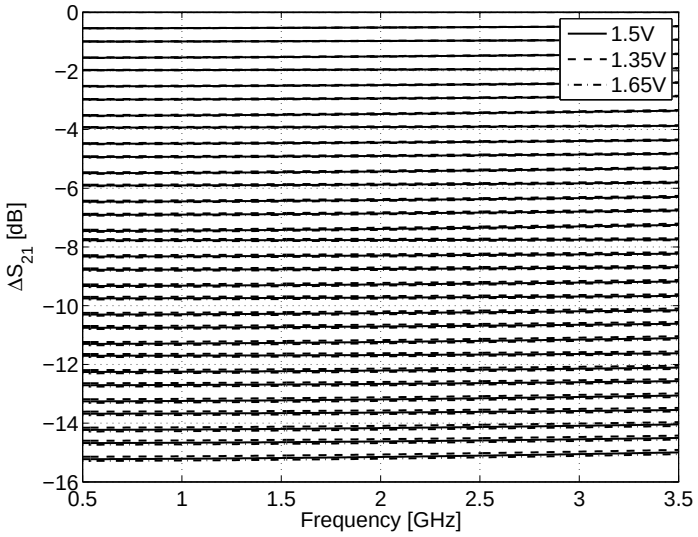


Figure 5.22: ΔS_{21} sensibility to power supply variations

Figures 5.21, 5.22 show that an increase in the power supply voltage results in a reduction of the insertion loss and in a subtle increase of the attenuation range, while a reduction in the power supply voltage has the opposite effect.

5.2.3 Temperature Variations

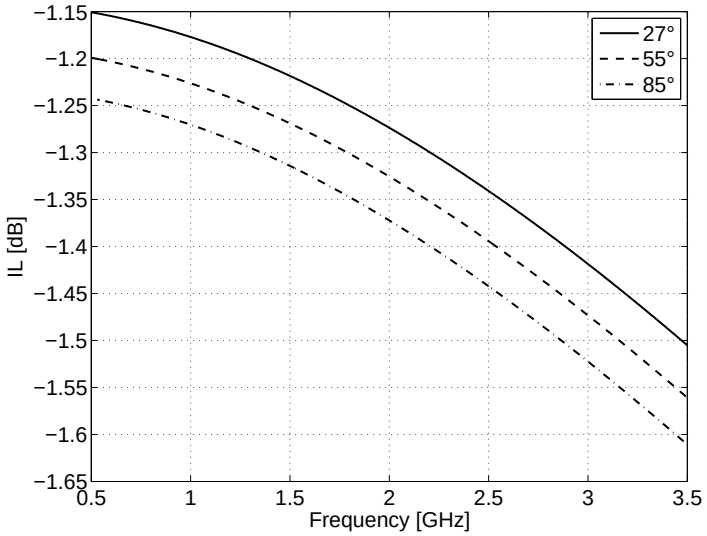


Figure 5.23: Insertion loss IL sensibility to temperature variations

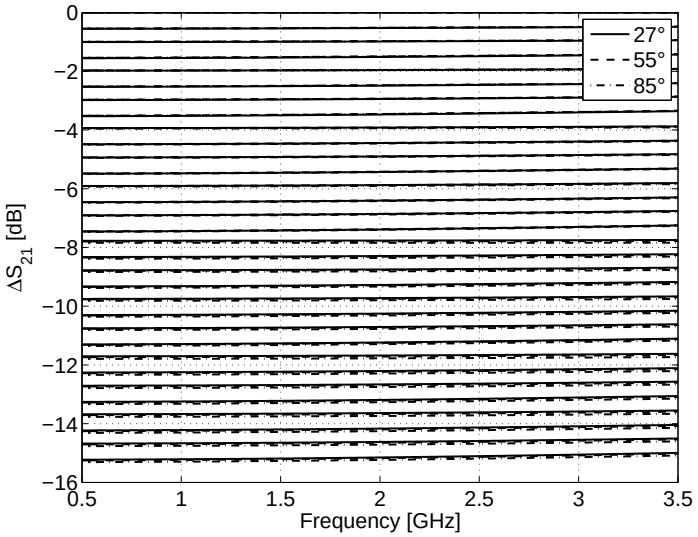


Figure 5.24: ΔS_{21} sensibility to power supply variations

Figures 5.23, 5.24 shows the sensibility of the insertion loss and the attenuation to temperature variations. A temperature increase corresponds to both insertion loss and attenuation increase.

5.2.4 Monte-Carlo Simulations

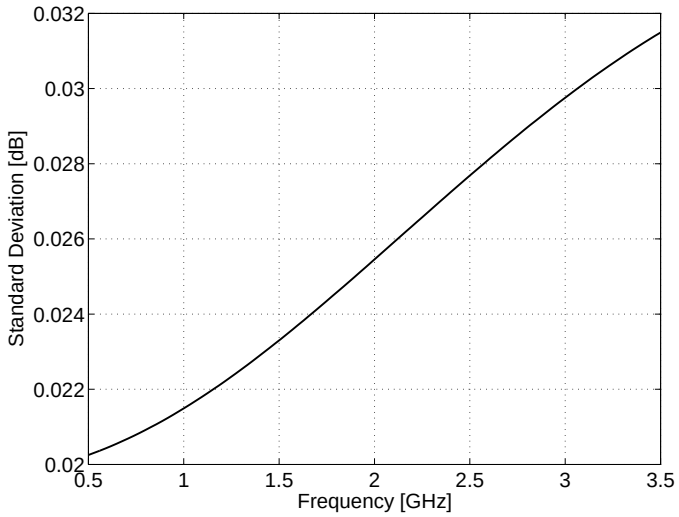


Figure 5.25: Insertion loss standard deviation

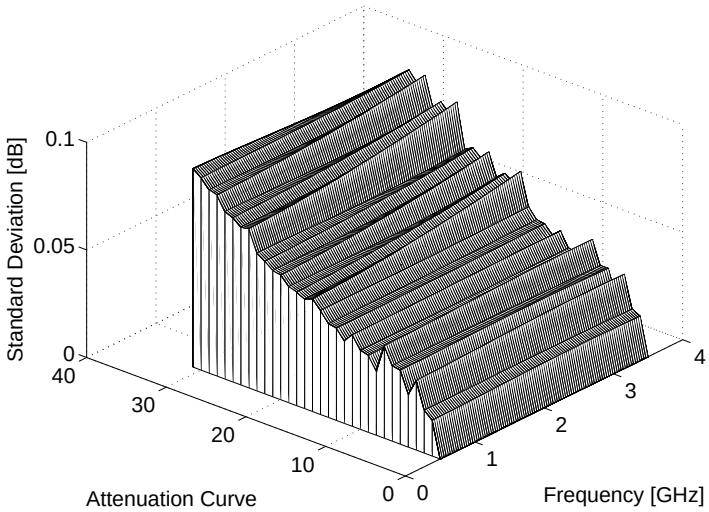


Figure 5.26: ΔS_{21} standard deviation

Figure 5.25 shows the standard deviation of the insertion loss in function of frequency, due to mismatch and process variations. Figure 5.26 shows the standard deviation of the transmission coefficient difference in function of the frequency and attenuation configuration. Attenuation axis goes from 0, reference attenuation curve, to 31, maximum attenuation curve.

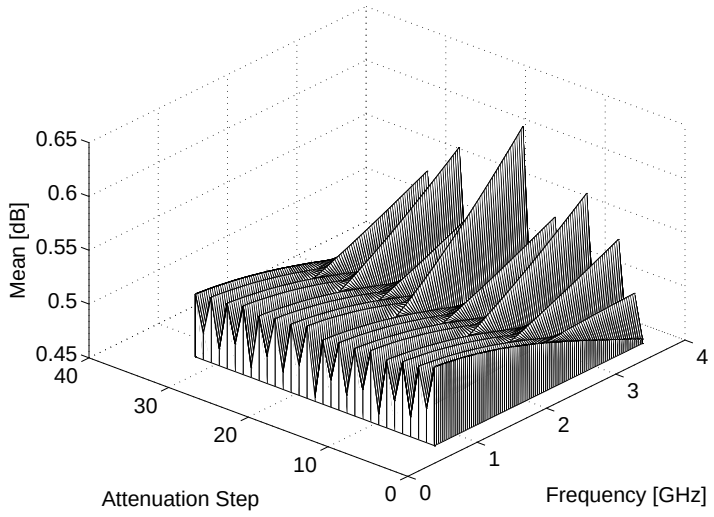


Figure 5.27: Mean of the distance between adjacent attenuation steps

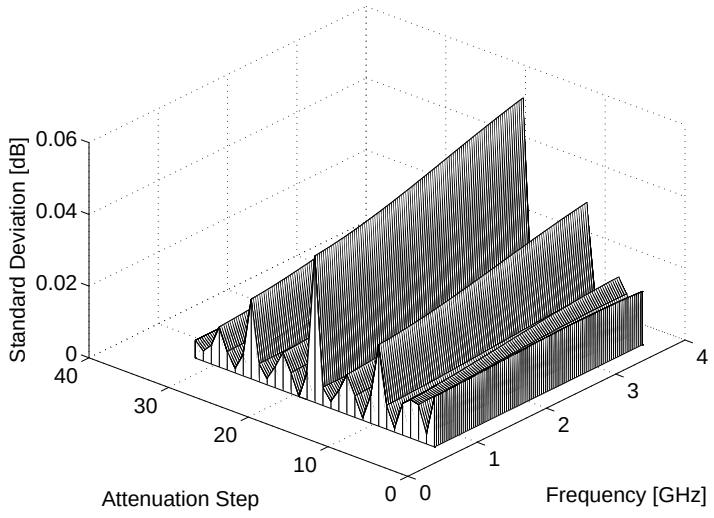


Figure 5.28: Standard deviation of the distance between adjacent attenuation steps

Figures 5.27, 5.28 show, respectively, the mean and standard deviation of the distance between two adjacent attenuation curves in function of the frequency and attenuation configuration, due to mismatch and process variations. Attenuation axis goes from 1, which represents the distance between the first two curves, to 31, which represents the distance between the last two curves.

Chapter 6

Summary

In this work, the design of a phase shifter and a programmable attenuator for DPA application has been presented.
The thesis has started with an overview of applications where these blocks are used, with the particular focus on phased array and DPA systems. It has been shown how these systems can benefit from the two RF building blocks. Moreover, some network analysis tools have been recalled to facilitate the understanding of the concepts presented in the rest of the thesis.
The focus of the second chapter has been the design of a phase shifter. It has started with an overview of the most used topologies and with the explanation of the difference between a phase shifter and a delay line (or TTD). It has been shown that both of them introduce a variable phase shift but, while in the former the phase shift difference is constant over the frequency, in the latter the group delay difference is constant over the frequency. Afterwards a detailed analysis and design of the differential π-network, used to realize a delay line, has been presented. In the final part of the chapter an alternative topology, which has been explored trying to improve the performance in terms of insertion loss, has been discussed.
The focus of the third chapter has been the design of the attenuator. It has started with an overview of the most used topologies and also in this case the differential π-network has been chosen. It has been analysed in detail, with particular attention on current limits, and finally designed to satisfy the

required specifications.

After a brief chapter about the layout, the simulation results have been presented for the delay line and the attenuator. Both the circuits have been designed to operate in the frequency range from $1GHz$ to $3GHz$, using only passive devices. The delay line shows an insertion loss of $1.81dB$ and a delay range of $76.5ps$ at $2GHz$. The delay tuning is done with a 16-bit control signal, and results in a delay step of $4.8ps$, at $2GHz$. The attenuator shows an insertion loss of $1.3dB$ and an attenuation range of $15.2dB$ at $2GHz$. The attenuation is controlled, in a binary way, with a 5-bit control signal and gives 32 different attenuation configurations, which results in a $0.49dB$ average step at $2GHz$. Both delay line and attenuator have been put on the same test chip which results in a total area of $1.45 \times 0.93mm^2$, including pads and digital parts for the control.

Appendix A

Generic π-network ABCD-Matrix

In both delay element and attenuator a differential π-network topology has been used (Fig. A.1). The calculation of the ABCD-matrix is done here for the general case while the specific results, obtained choosing different impedances for Z_1 and Z_2, will be reported in the respective chapters. The A, B, C and D coefficients are:

$$A = \left.\frac{V_1}{V_2}\right|_{I_2=0} = V_1 \cdot \left(\frac{V_1}{Z_1 + 2Z_2} \cdot Z_1\right)^{-1} = \frac{Z_1 + 2Z_2}{Z_1} \tag{A.1}$$

$$B = \left.\frac{V_1}{I_2}\right|_{V_2=0} = V_1 \cdot \left(\frac{V_1}{2Z_1}\right)^{-1} = 2Z_1 \tag{A.2}$$

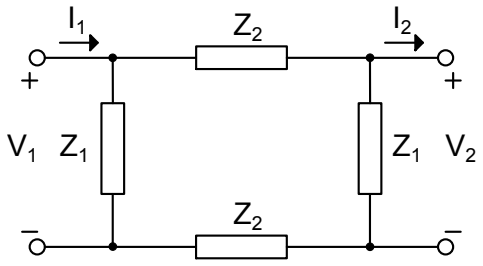


Figure A.1: Generic π-network

$$C = \left.\frac{I_1}{V_2}\right|_{I_2=0} = I_1 \cdot \left(I_1 \frac{Z_1}{Z_1 + (Z_1 + 2Z_2)} \cdot Z_1 \right)^{-1} = \frac{2(Z_1 + Z_2)}{Z_1^2} \tag{A.3}$$

$$D = \left.\frac{I_1}{I_2}\right|_{V_2=0} = I_1 \cdot \left(I_1 \frac{Z_1}{Z_1 + 2Z_2} \right)^{-1} = \frac{Z_1 + 2Z_2}{Z_1} \tag{A.4}$$

and hence the ABCD-matrix is:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{Z_1+2Z_2}{Z_1} & 2Z_2 \\ \frac{2(Z_1+Z_2)}{Z_1^2} & \frac{Z_1+2Z_2}{Z_1} \end{bmatrix} \tag{A.5}$$

One particular case of this network, which will be useful particularly in the attenuator design, is when $Z_1 \to \infty$. In this case the ABCD-matrix becomes:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 2Z_2 \\ 0 & 1 \end{bmatrix} \tag{A.6}$$

Appendix B

Effective Inductance in Coupling Presence

Consider the transformer in figure 1.8. Suppose that: (1) the two inductors have the same geometrical properties ($L_1 = L_2 = L$), (2) the concatenated magnetic flux have the same direction of the self-generated magnetic flux ($k > 0$) and (3) the inductors are crossed by the same current $I_1 = I_2$. The transformer equations can then be rewritten as follows:

$$\begin{cases} \frac{V_1}{I_1} = i\omega L_1 + i\omega M \frac{I_2}{I_1} = i\omega(L + M) \\ \frac{V_2}{I_2} = i\omega M \frac{I_1}{I_2} + i\omega L_2 = i\omega(M + L) \end{cases} \tag{B.1}$$

Considering that the ratio V_i/I_i represent the impedance seen from the ports and that, due to the three assumptions made, the mutual induction coefficient can be expressed as $M = kL$, it is obtained that:

$$\begin{cases} Z_1 = i\omega(1 + k)L = i\omega L_{eff} \\ Z_2 = i\omega(1 + k)L = i\omega L_{eff} \end{cases} \tag{B.2}$$

In other words, the *effective inductance* seen from the two ports is $L_{eff} = (1+k)L$ and if the coupling coefficient is greater than zero then the effective inductance is greater than the inductance associated to an uncoupled inductor, as stated at the beginning of the section.

From the practical point of view two things are needed to achieve this target: (a) the transformer must be designed to satisfy the first two assumptions ($L_1 = L_2 = L$, $k > 0$); (b) the topology should be such that the last assumption is satisfied ($I_1 = I_2$).
In this work both of the requests are satisfied and the transformer is used to increase the effective inductance. It is worth to notice that also that the negative coupling coefficient is used in practice ([17]).

Appendix C

Alpha is a Function of the Channel Length Only

In the phase shifter chapter, during the presentation of the varactors design, it has been stated that the α coefficient is a function of only the channel length L_c. Considerations which have brought to that assertion are discussed here. The equation of the maximum and minimum capacitances are here reported:

$$\begin{cases} C_{MAX} = \frac{1}{2}C_{gc} + C_{ol} \\ C_{min} = \frac{1}{2}C_{gb} + C_{ol} \end{cases} \tag{C.1}$$

where it has been assumed that the overlap capacitances associated to the drain and the source are the same. It is known that the gate-channel capacitance C_{gc} is proportional to the product WL_c through a proportionality constant, which in this case is the oxide capacitance per area (called here K_{ox}). The same thing can be said about the gate-bulk capacitance[1] and in this case the constant will be called K_{bulk}. Finally, the overlap capacitances are proportional to the channel width through the constant K_{ol}. Taking into

[1]It is worth to remind that the gate-bulk capacitance can be expressed as $C_{gb} = WL_c(q\epsilon_{Si}Nbulk/(4\phi_F))^{1/2}$

account all these considerations the previous equations can be rewritten as:

$$\begin{cases} C_{MAX} = \frac{1}{2} W L_c K_{ox} + W K_{ol} \\ C_{min} = \frac{1}{2} W L_c K_{bulk} + W K_{ol} \end{cases} \tag{C.2}$$

As it can be seen the channel width is a common factor of both the maximum and minimum capacitances and in the ratio it vanishes, obtaining:

$$\alpha = \frac{\frac{1}{2} L_c K_{ox} + K_{ol}}{\frac{1}{2} L_c K_{bulk} + K_{ol}} \tag{C.3}$$

The result is that the α coefficient is a function of the channel length only.

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