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Ultra low phase noise 19 GHz VCO design in bipolar technology

Relatore:
Ch.mo Prof. Andrea Bevilacqua
Correlatore:
Dr. Ing. Marc Tiebout

Laureando:
Fabio Padovan

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Abstract

A tremendous development of RF circuits occurred in recent decades, but the market requires even more efficient and powerful telecommunication systems providing more bandwidth at a lower power consumption and lower cost. Oscillators are very essential components for all telecommunication systems. In RF transmitters and receivers, oscillators provide the signal to mixers allowing a downconversion and upconversion of the signals. Furthermore they provide high purity clocks signal for analog to digital and digital to analog conversions as well as to the digital processing. Whereas in the past years, a large focus of research and development was placed on improving the performance of oscillators for mobile battery operated systems in terms of phase noise and power consumption, in this work the focus is purely set to low phase noise operation for oscillators to be used in non-mobile backhaul or basestation applications. Two VCO-circuits have been designed for a frequency of 19 GHz with a tuning range of more than 10% and a phase noise below -120 dBc/Hz at an offset frequency of 1 MHz. Both circuits use INFINEON's bipolar SiGe process offering high speed transistors, a high-Q varactor and a thick top metal level. One VCO circuit uses the varactor directly coupled to the integrated inductor requiring a tuning voltage up to 10 V. Although also comparable phase noise commercial products from HITTITE require such unconvenient high tuning voltages. A second version was implemented based on an integrated transformer and operating with a tuning voltage between 0 and 3.3 V. The power consumption of both implemented VCOs is 20 mA from a single 3.3 V supply voltage.

Chapter 1

Introduction

1.1 Presentation

Initially, oscillators were made with vacuum tube, frequencies were very low. When the transistors were born, they were used to make oscillator using capacitors and inductors; due to the high Q of these resonators and the large voltage swing, the phase noise was never an issue. Later there was the need to made synthesizers and to increase the frequency of work, then the phase noise was becoming more and more important in the realization of oscillators.
In the last few years the specifications on phase noise have been becoming more and more stringent due to the high speed transmission, with the request to transport a lot of data with as little interference as possible and the work of many researchers is based on an accurate study of the behaviour of the oscillators in order to obtain low phase noise VCO resulting in an increase of systems performance. Below is the resume of the design characteristics.

- **Application:** LTE backhaul wireless point-to-point Gbit communication 81-86GHz
- **Technology:** 200GHz SiGe bipolar Process of INFINEON
- **Specification:**

Frequency range	17.75-19 Ghz
Phase noise at 1 MHz offset	$< -120 dBc/Hz$
Vsupply	3.3 V

- **Tasks:**
  -Inductor design with EM-simulators SONNET and MOMENTUM
  -Circuit design using CADENCE spectre and AGILENT ADS
  -Full Custom layout CADENCE Virtuoso

The most important requirement of this design is low phase noise, there aren't specifications about power consumption (it is not a mobile application).
In order to make some comparison with the products currently in the market, it is possible to have a look at Hittite designs, [20] focus on the VCOs designs that present best results in order of phase noise.
It is difficult to have a good comparison because the objectives and specification of various designs are different, in fact Hittite use different technology [20] based on GaAs InGaP Heterojunction Bipolar Transistors (HBT). It is important to have an idea of the possible goal. Some comparable VCOs are [22], [21] and some features are inserted in the table 1.1:

Model	**Frequency [GHz]**	**Function**	**Output power [dBm]**	**10kHz SSB PN [dBc/Hz]**	**100kHz SSB PN [dBc/Hz]**
HMC738LP4	20.9-23.9	VCO with Fo/2 ÷16	9	-65	-95
HMC398QS16G	14-15	VCO with Fo/8	6	-75	-110

Tab. 1.1: Hittite VCOs

Data sheets of these devices are in [22], [21]; according with the phase noise formula [13] it's possible to extract the phase noise at the same offset frequency which is 1 MHz. The device HMC738LP4 has a phase noise approximately of -115 dBc/Hz at 1MHz offset, considering that the center frequency is 22 GHz.
The model HMC398QS16G has a phase noise approximately of -130 dBc/Hz at 1 MHz offset, but the operating frequency is lower, about 14-15 GHz, therefore the value is some dB more than the corresponding result at 19 GHz [13]. These two examples are a good goal for the comparison of the results, obviously considering the different technologies used, different voltage supply and different power consumption.
In the section 1.2 there is the description of the applications of oscillators with low phase noise, after that there is a small description of the theory of oscillators and phase noise.
In the chapter 2 the design describing each block of the system will be presented in detail.
In chapter 3 there are some issues regarding the layout and in chapter 4 all result of the simulation after the layout operation will be shown.
Finally we will summarise the work with the conclusion.

1.2 Applications

In this section, the applications of low phase noise VCO are explained in order to understand the importance of the design and its contributions to the other blocks of the global projects. Generally, most important applications of VCO can be divided in two part, *mobile telecommunications* and *clock generation, data recovery*:
Mobile telecommunications:

- Cellular :GSM, DCS1800, UMTS, LTE
- DECT
- Bluetooth
- Wireless LAN
- Home RF
- Remote Keyless Entry, ...

Clock generation, data recovery:

- Wireline Data-communication: Ethernet,...
- CPUs
- ADCs/DACc

Global application of the project documented here is LTE backhaul wireless point to point Gbit communication in the frequency band 81-86 GHz. LTE i.e. long term evolution, is a new standard for wireless communication of high-speed data for mobile phones and data terminals; of the three main transport technologies in the backhaul arena, fiber, copper and wireless point to point communication microwave, the latter is the most important to look at. Used in over 50% of all mobile backhaul deployments worldwide (70 % in USA), point to point microwave systems offer simple and cost efficient backhauling for voice and high speed data services, in fact it supports higher data rates than copper T1/E1 lines and obviously the cost is less than optic fiber.
Anyway the fibers are used a lot in the backaul network with this standard due to their high data−rate availability.
The backaul environment represent the part of the mobile network that connect base stations to network controllers within a coverage area, [15]. Sometimes it is said that backaul is referred as first mile and last mile of a network.
Due to an increase of users, LTE is promising to provide an evolution path for mobile technology and the delivery of faster data speeds and new services.

LTE utilizes a new radio access technology that is optimized for IP-based traffic and offers operator a simple update path from 3G networks,[11].

Application of this design operates in the E-band, i.e. 71-76 GHz, 81-86 GHz [31].

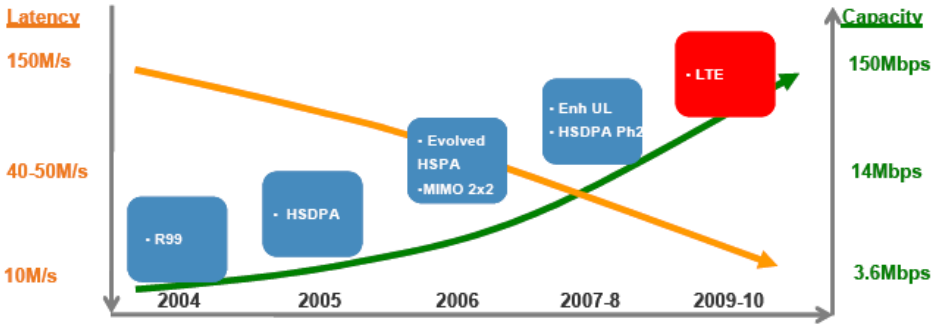


Fig. 1.1: 3G and LTE Capacity & Latency Requirements

The two allocated bands, each boasting a 5 GHz bandwidth, are much wider than most cellular and microwave bands, making them suitable for high data-rate communications i.e. at least 10 Gbps, while utilizing low complexity modulation schemes and cost effective system architectures.

This are the advantages resume of E-band application:

- Very high data-rate, at least 10 Gbps;
- Long-distance communication links;
- Rapid and cost effective deployment;
- 99.99% all-weather availability;

Due to the increment of demand for high bandwidths and high data rates, telecom companies need to have multi giga bit backhaul links.

The high costs of installing fiber over long distances has been an obstacle in scaling existing networks to meet the requirements of emerging applications, such as 3G/4G and LTE. A cost effective wireless technology can provide a highly scalable backhaul solution for 3G/4G carriers, enterprise internet access providers, and other applications. All these features has made E-band communication links an attractive solution for gigabit backhaul applications:

- **WiMAX/LTE/4G backhaul** (explained before)
- Ethernet connectivity
- Remote storage acces

- Redundant Acces/Network Diversity
- Local Area Network Extension
- Wide Area Networks
- Metropolitan Area Networks (MAN)

Recently, E-band had employed more complex modulation schemes (like 16 QAM , 64 QAM ..) with the expense of more complicated transceiver modem and significantly higher power consumption but very high data rates.
Below there are some block diagrams that shows RX and TX systems used in the above-described application and the modulation scheme used is 64 QAM. In Figure 1.2 is depicted the simplified block diagram of the receiver. The VCO highlighted in Figure 1.2 has been designed in this work to generate 19 GHz signal to be then multiplied by four to arrive at 70 GHz. This 70 GHz frequency will then go to the LO port of the mixer.
The quality factor of the varactor diode become very low at high frequencies resulting in a degradation of phase noise. Furthermore the layout at high frequency is hard because the connection present high resistance that affect Q of the tank. For this reason the oscillator is designed for 19 GHz rather than 70 GHz.

As can be seen in the block diagrams in Figures 1.2 and 1.3, oscillators is a fundamental

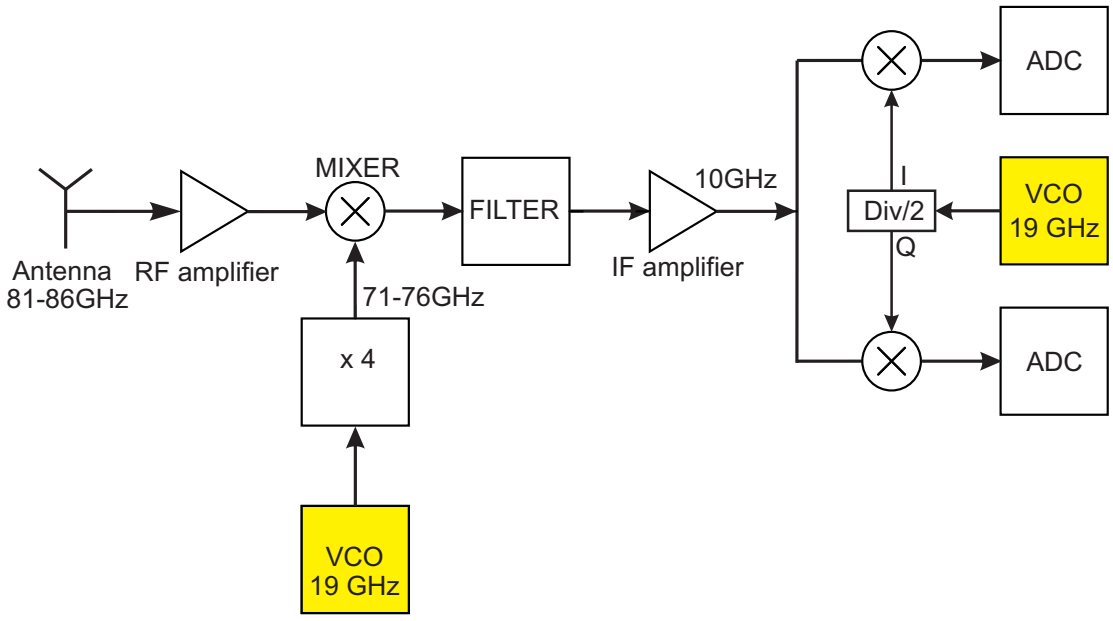


Fig. 1.2: RX Block Diagram

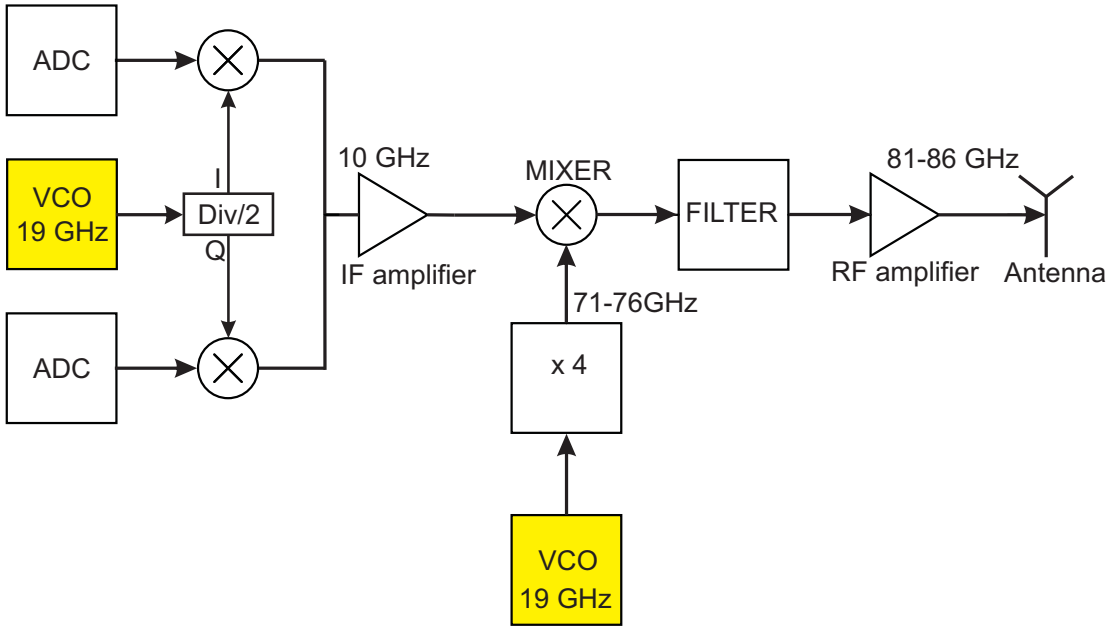


Fig. 1.3: TX Block Diagram

part of the systems, it provides to mixer the signal for the frequency conversion, thus it is convenient that the local oscillator signals be perfectly periodic and give a precise time reference, [18]. Find a good way to characterize instability in time i.e. timing jitter is very important: phase noise is a characterization of this instability. Farther implication of this can limit the operative range of a radar, reduce the quality of television image, reduce the precision in satellite position and degrade the quality in data transmission.

Phase noise effects in RF Communications

Phase noise is responsible of quality degradation of transmission data and decrease accuracy of frequency conversion operation. It afflicts both, analogue transmission with angular modulation and digital transmission. In the first, it degrades signal to noise ratio, in the second it is responsible of jitter in the information, varying symbol duration and increasing error probability per bit (BER). In order understand better the importance in wireless communications, consider a generic transceiver as depicted in Figure 1.4 where the receiver consist of low noise amplifier, a band pass filter, and a downconversion mixer, and the transmitter has an upconversion mixer, a bandpass filter and a power amplifier. The LO provides signal to both the systems and he is in a frequency synthesizer. We can see in the Figure 1.5 that both, downconverted and upconverted signal are corrupted if LO has phase noise, [30]. If the LO has not phase noise, he converts

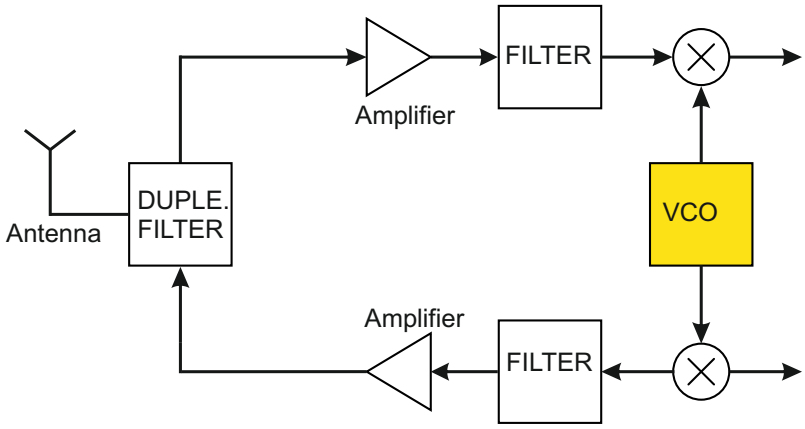


Fig. 1.4: Wireless transceiver

the signal multiplying it by an impulse, therefore there are no change in the shape of the signal. Adding the noise, the signal has a large interferer in adjacent channel. When the two signal are mixed with LO, the downconverted band consist of two overlapping spectra, with the wanted signal suffering from significant noise from the interferer of adjacent signal (reciprocal mixing), [30].

On the transmit path the effect is slightly different; receiver detect signal at ω_2 while a powerful signal is transmitted at ω_1 then the wanted signal is corrupted by ω_1 phase noise tail. See Figures 1.5, 1.6. If the tail shape of the LO is narrow, the nearby channel are less affect by other contribution. For this reason is important to have VCO with low phase noise in the transmission systems.

Telecommunication growth implies the availability of more and more transmission chan-

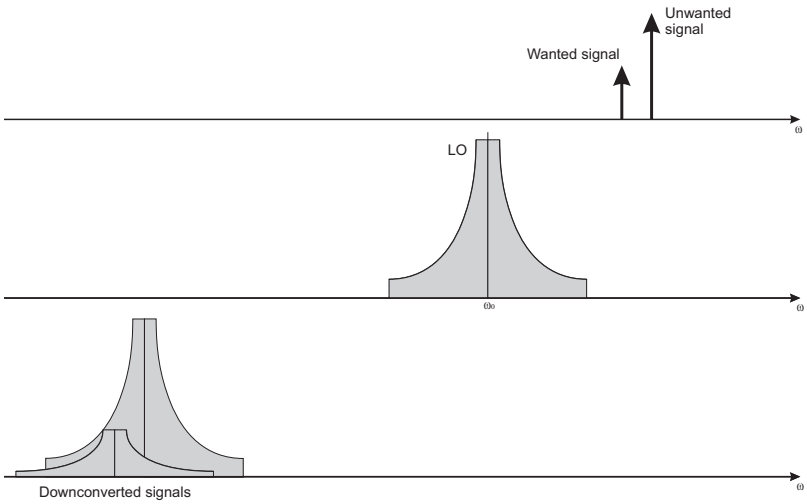


Fig. 1.5: Phase noise effect on receive path

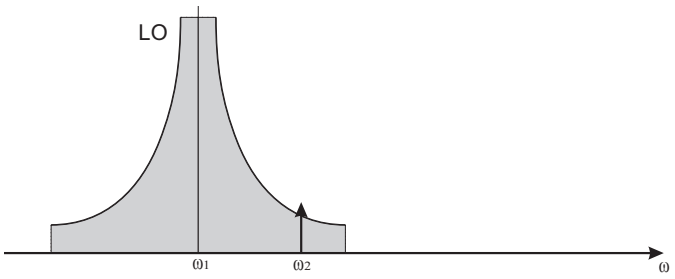


Fig. 1.6: Phase noise effect on transmission path

nels in the same bandwidth, this requires more stringent limits for VCO performance. Into QAM and PSK modulation systems, phase noise is the first cause of BER increase. For example in the Figure 1.7, there is th representation of I-Q signals of 16-QAM modem, there are 16 symbols, each one with a string of 4 bit. Phase noise acts on the phase of all these vectors, then it causes the release from the region, that implies more error probability.

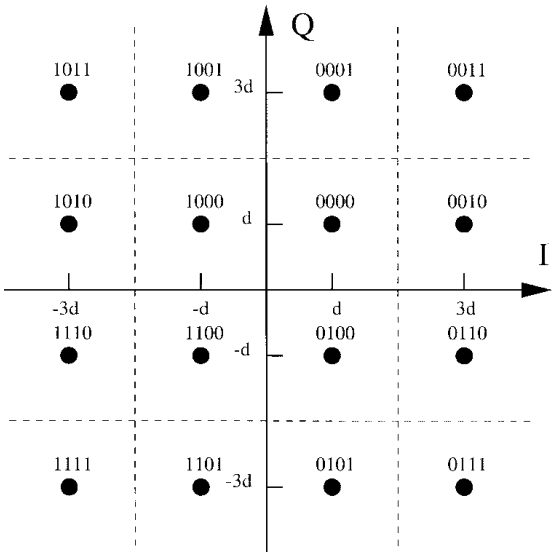


Fig. 1.7: 16 QAM

1.3 Theory

1.3.1 Oscillators

An oscillator is a system that generates a signal (normally a sinusoidal signal) without input and it generally consists of a resonator element and an amplifier, as well as a feedback circuit. Oscillator can also be seen like a DC-RF converter where the input is the DC supply power. The amplifier contrasts resonant part losses giving the wanted signal and the resonant part give the frequency of the oscillation in the point of his resonant peak, where there is less impedance. The requirement of high data rate in the transmission implies to made component more and more small up to integrate the resonant part too; in this way it is possible to reach very high frequencies oscillators like tens of GHz. VCO is an oscillator that varies output frequency according to an input voltage i.e. Vtune. The main parameters of a VCO are:

1. **Tuning range:** the difference between minimum and maximum frequency value al the output. In this range, amplitude and jitter variation should be minimum. Tuning range has to be sufficient to ensure compensation of parameters due to technological spreads and temperature variation that produce frequency variation.

2. **Jitter and phase noise:** it is related to having pure spectral signal and it is examined in the subsection 1.3.2

3. **I/O VCO characteristic:** A voltage controls variation of output frequency; this curve should be more linear as possible to avoid distortion for example if the VCO is used in a receiver system.

4. **Power consumption:** Should be as little as possible to allow for example long battery life in the portable element.

5. **Supply sensitivity (PUSHING):** Variation of the frequency due to variation of Voltage supply.

The category of VCO can be divided in two main types:

1. Ring-Oscillators

2. LC-VCO's (negative resistance)

The main Ring-Oscillators idea is to put more cells one after the other in order to generate oscillation, as it can be seen in Figure 1.8 . In order to generate the oscillation, Barkausen criteria [17] has to be satisfied, whereby loop gain must be 1 and total phase shift of 360. Advantages of this circuit are very wide tuning range, multiphase output and little usage of area because there isn't passive resonant circuit. The disadvantage is

high phase noise because there aren't selective frequency devices (resonator) with high Q; for this reason in this design LC-VCO is used.

Negative resistor oscillator can be modelled with an active port (negative resistance)

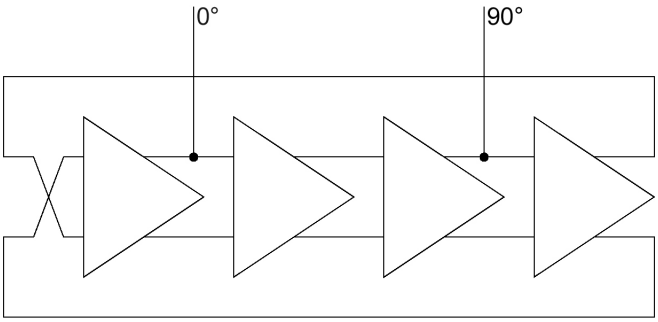


Fig. 1.8: Example of differential ring-oscillator

and a frequency selective port like in Figure 1.9. The frequency of the output signal is $\omega_0 = \frac{1}{\sqrt{LC_{tot}}}$ where L is the inductor part of the resonant circuit and C is the total capacitance of the circuit. Ideally, resonant system has not equivalent resistance, then the oscillation shouldn't degrade; actually the resonant circuit present losses (equivalent resistance as in Figure 1.9) therefore it need an amplifier to compensate this loss and keep oscillation constant.

Considering two port, passive port and negative port, we can write the impedance equation:

- $Z_a(s) = R_a + jX_a$, active port;
- $Z_f(s) = R_f + jX_f$, passive port;
- $Z_f(s) + Z_a(s) = 0$, oscillator equation

Imaginary part must be 0 for the resonance of the circuit and real part of the active port must compensate real part of passive port:

- $R_a(\omega_0) + R_f(\omega_0) < 0$
- $X_a(\omega_0) + X_f(\omega_0) = 0$

This indicate that the entire system has poles with positive real part, therefore should appear divergent oscillations. Actually oscillator are not linear system, amplifier doesn't increase the input signal in the same way for each input amplitude, then this non linearity compensate the divergent mode, practically, at a certain moment transistors enter in saturation zone and the value of the negative resistance decrease in absolute value, stopping the divergence.

VCO with LC network are made using varactor, that is a diode that vary his equivalent

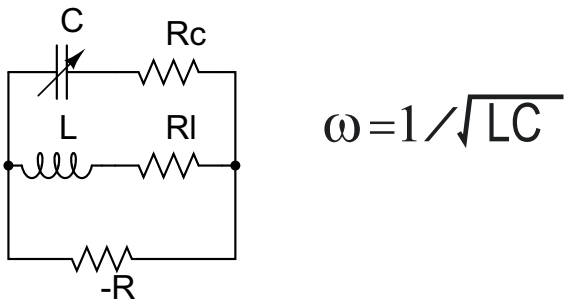


Fig. 1.9: LC oscillator model

capacitance varying Vtune. LC oscillator has excellent result on phase noise due to high Q resonant circuit but it has disadvantage, the tuning-range is not very wide. The main specification of this design is the Phase noise, so we focus on this kind of VCO.
A circuit with negative resistance is the differential cross coupled, Figure 1.10. The initial analysis is the study of a linear model that is useful for the start up condition.

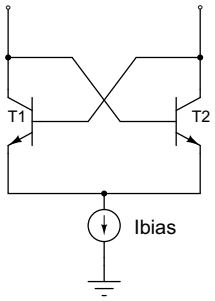


Fig. 1.10: Differential cross couple

Linear model differential cross couple

Focus on the differential cross couple system, [34] it is easy to extract the equation of the oscillator considering the linear model, that is right only for small signals. The system is considered like a typical closed loop system in Figure 1.11, the equation relative at this block diagram is:

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{A(s)}{1 + A(s)H(s)} \tag{1.1}$$

Then, to have $V_{out} > 0$ without input signal, $1+A(s)H(s)$ must be 0 and the system must have pole with positive real part. The electrical model is in Figure 1.12 and is easy to calculate the transfer function of the linear system in order to obtain start up condition.

As we can see, comparing Figure 1.11 with Figure 1.12, $A(s) = Z(s) = \frac{sRL}{s^2CL+SL+R}$ and

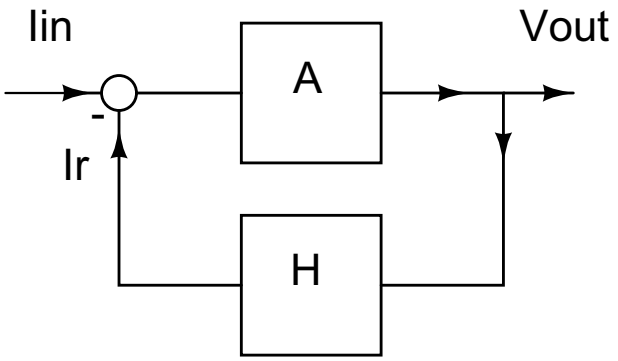


Fig. 1.11: Closed loop sistem

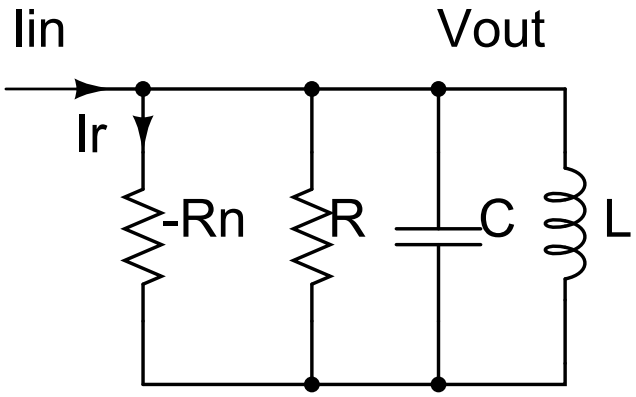


Fig. 1.12: Electric model of negative resistance oscillator

$H(s) = \frac{1}{-R_n}$ Equations of the system are:

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{Z(s)}{1 + \frac{Z(s)}{-R_n}} \tag{1.2}$$

We can export the denominator of this equation and calculate where the poles have positive real part, D(s) is the denominator of equation 1.2, $p_{1,2}$ are the poles:

$$D(s) = s^2CL + s(L - \frac{R}{R_n}L) + R \tag{1.3}$$

$$p_{1,2} = \frac{-(L - \frac{R}{R_n}L) \pm \sqrt{\Delta}}{2CL} = R_e \pm jIm \tag{1.4}$$

$$R > R_n \tag{1.5}$$

Since, from the model of the cross differential couple, $R_n = \frac{2}{gm}$ where gm is the transconductance of the transistors model, then the START UP condition is:

$$g_m > \frac{2}{R} \tag{1.6}$$

where as it has been seen, R is the global losses of the tank circuit. The equivalent R of the thank is easily calculable at oscillation frequency knowing the inductor and varactor series resistive loss. For example, if the resistance of a coil is R_s and the inductance is L, the parallel resistance is $R_p = \frac{\omega^2 L^2}{R_s}$, for the capacitance the equation is $R_p = \frac{1}{\omega^2 C^2 R_s}$, where ω is the oscillation frequency, or rather the working frequency of the inductor and capacitor. From here is trivial to extract the global parallel resistance of the tank. As it has been seen in the Equation 1.6, BJT's transconductance has to be large enough to compensate this resistance in order to ensure START UP. This condition indicates that the system has poles in the half-plane with positive real part then the oscillation starts from an initial noise in the circuit.

Non-linear behaviour

Linear model is adopted mainly for the start-up condition and to understand the behaviour of the oscillator; as discussed above, if the closed loop gain has a pair of complex-conjugate poles in the right half of the s-plane, a growing, near sinusoidal voltage appears. As the oscillation amplitude grown, due to the limitation of real transistors, the large signal transconductance G_m become different from small signal one g_m, therefore the complex conjugate poles move towards the imaginary axis until they are very closed to imaginary axis "*steady-state behaviour*" [35]; at this time, oscillation amplitude keeps more or less constant.

Time domain

Non-linearity in the circuit produces this limitation amplitude and harmonics in the output signal. BJT transistor has a non linear exponential relationship between base voltage and collector current:

$$i(t) = I_s \exp(\frac{qv(t)}{kT}) \tag{1.7}$$

where I_s is the device saturation current, $v(t)$ is the voltage drive, k is the Boltzman's constant, q the electronic charge and T is the temperature in kelvin.

$$v(t) = V_{dc} + V_1 cos(\omega t) \tag{1.8}$$

If the driven voltage grows enough across base-emitter junction, the resulting current is a periodic series of pulses like it is seen in [35]. This leads to strong harmonic generation, at the end, the final equation is:

$$i_e(t) = I_{dc}\Big[1 + 2\sum_1 \inf \frac{I_n(x)}{I_0(x)} \cos(n\omega t)\Big] \qquad V_{dc} = V_{dcQ} - \frac{kT}{q} \ln I_0(x) \tag{1.9}$$

V_{dcQ} and I_{dc} are the operating DC bias voltage and the DC value of the emitter current. $I_n(x)$ is the n-Fourier coefficient and $x = \frac{qV_1}{kT}$ is called drive level. The Fourier transform of $i_e(t)$, a current pulse or series of pulses in the time domain, yields a number of frequency harmonics common in oscillator circuit designs using non-linear devices.
Other elements of the oscillators theory will be discussed in the Chapter 2

1.3.2 Phase Noise

Phase noise measurement is very important for the performance of the component, in this case, oscillator. Phase noise of a real system is the total result of more contributions noise overlap present into the circuit. In order to quantify phase noise, we consider a unit band width at an offset frequency $\Delta\omega$ with respect to ω_0, calculate the noise power in this bandwidth, and divide the result by the carrier power. A simple model to extract phase noise is in Leeson analysis, [13] and in the following section there are some signs of calculations.
In practise, all frequency sources are characterized by an undesirable phase modulation due to the internal noise. This is not good for all applications that require stable time signal. Phase noise affect regularity of 0 passage of the wave, in other words, phase noise affect jitter of periodic signals. [2]

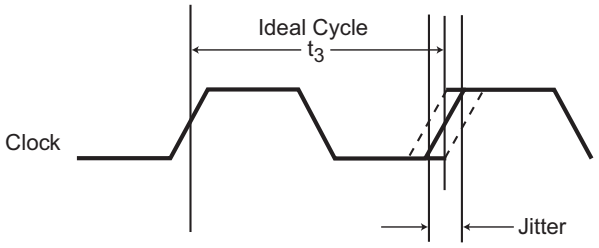


Fig. 1.13: Jitter in a clock signal

Elements of calculation

As it has been said in Leeson model [13], phase noise in an oscillator depends on the power output near the desired frequency. Considering an oscillator like a system with amplifier and feedback, it is possible to define the noise factor F, [35]

$$F = \frac{(S/N)_{in}}{(S/N)_{out}} = \frac{N_{out}}{GkTB} \tag{1.10}$$

Where N is the noise, G is the amplifier gain, B is the bandwidth where the noise is calculated. The input phase noise with 1 Hz bandwidth produces a phase deviation [35].

$$\Delta\theta_{RMS} = \frac{1}{\sqrt{2}}\sqrt{\frac{FkT}{P_{sav}}} \tag{1.11}$$

From Leeson model [13] it has been extracted the spectral density of phase noise:

$$\Delta\theta_{RMStotal} = \frac{1}{\sqrt{2}}\sqrt{\frac{FkT}{P_{sav}}} \tag{1.12}$$

$$S_\theta(f_m) = \Delta\theta^2_{RMS} = \frac{FkT}{P_{sav}} \tag{1.13}$$

where f_m is the offset frequency. This is the theoretical noise floor of the amplifier. For a modulation frequency close to the carrier [13] $S_\Phi(f_m)$ shows a flicker component $\frac{1}{f}$, empirically described by the frequency corner f_c then the phase noise now can be described by:

$$S_\theta(f_m) = \Delta\theta^2_{RMS} = \frac{FkT}{P_{sav}}\Big(1 + \frac{f_c}{f_m}\Big) \tag{1.14}$$

In this formula, there are no AM to PM noise conversion and the presence of resonator is not considered.

If the transfer function of resonator is added, [13] at the and the formula for the phase noise SSB is:

$$\mathcal{L}(f_m) = 1/2\Big[1 + \frac{1}{f_m^2}(\frac{f_0}{2Q_L})^2\Big]S_\theta(f_m) \tag{1.15}$$

where Q_L is the quality factor of the inductor. Now there are 2 different cases: for low Q, the band of the resonator is bigger than f_c, then spectral density will show a $\frac{1}{f^3}$ and $\frac{1}{f^2}$ dependence close to the carrier; for high Q, there is before $\frac{1}{f^3}$ region and then $\frac{1}{f}$ region, [35].

At the end the global formula is:

$$\mathcal{L}(f_m) = \frac{FkT}{2P_{sav}}\Big[\frac{f^2 f_c}{f_m^3 4Q_L} + \frac{1}{f_m^2}(\frac{f_0}{2Q_L})^2 + (1 + \frac{f_c}{f_m})\Big] \tag{1.16}$$

This indicates the four causes of phase noise:

- flicker FM noise
- thermal FM noise
- thermal noise floor
- flicker phase noise

In the calculations introduced above, an LTI (linear time invariant) model is used, actually oscillators are not linear model and also time invariant, therefore the systems doesn't give a correct representation of the noise in these systems.

There is another phase noise calculation model "Hajimiri and Lee", [3] that is based on the non linear time-varying properties of the oscillator current waveform. This model is based on the effect of noise impulse on a periodic signal, as it can be seen in Figure 1.14 and 1.15; if an impulse is injected at the peak of the signal, it causes maximum amplitude

modulation and no phase modulation, if an impulse is injected at the zero crossing of a signal, only maximum phase modulation will be seen; variation in amplitude are not important due to the limitation of the amplitude gain of oscillators therefore the important point is the zero crossing. Hajimiri and Lee introduced an impulse sensitivity function (ISF) Γ, which is different for each topology of the oscillator and it is periodic [3]. It has the maximum value when phase modulation of the noise has his maximum, hence near the zero crossing of the output voltage.

Based on this theory [3] the phase noise formula is in equation 1.17.

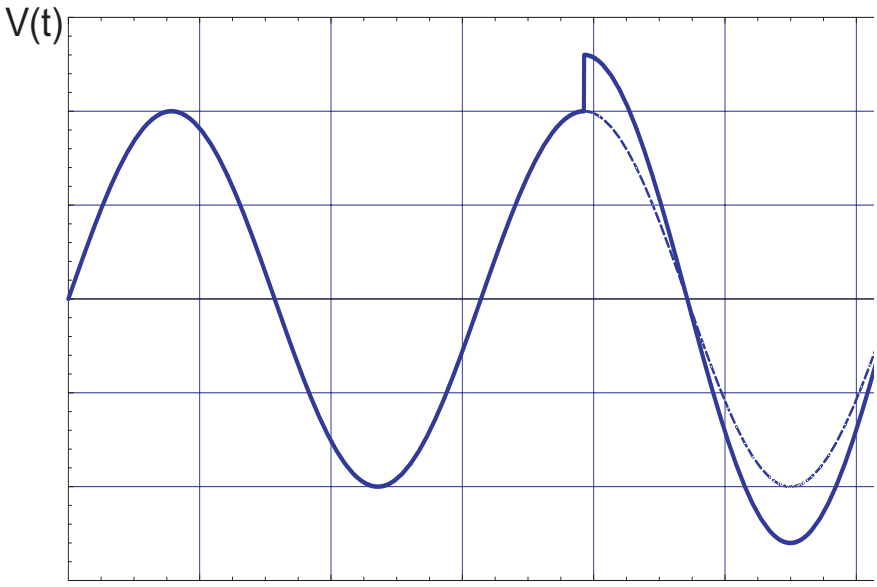


Fig. 1.14: Effect of injection at the maximum of the amplitude

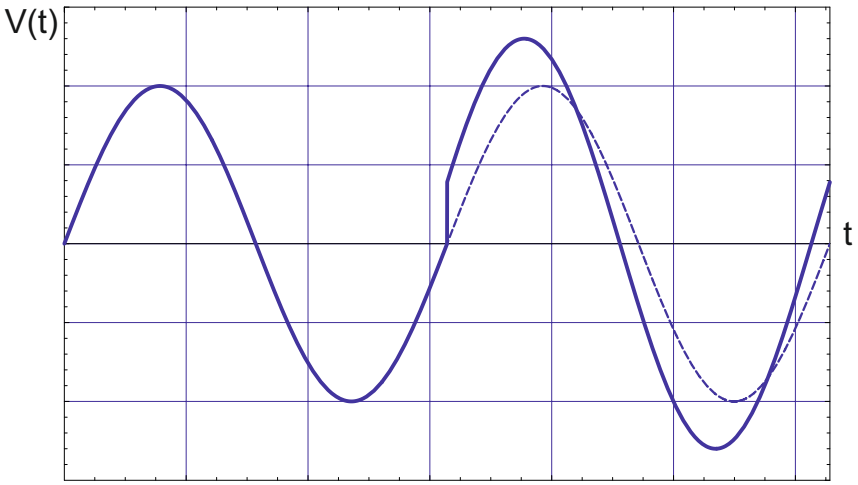


Fig. 1.15: Effect of injection at the 0 crossing

$$\mathcal{L}(f_m) = 10\log\Big[\frac{C_0}{q_{max}^2}\frac{i_n^2}{\Delta f}8f_m^2\frac{\omega_{1/f}}{f_m}\Big] \qquad \frac{1}{f^3} \rightarrow region \tag{1.17}$$

$$\mathcal{L}(f_m) = 10\log\Big[10\log\Big[\frac{\Gamma_{rms}^2}{q_{max}^2}\frac{\frac{i_n^2}{\Delta f}}{4f_m^2}\Big]\Big] \qquad \frac{1}{f^2} \rightarrow region \tag{1.18}$$

where:

- $i_n^2/\Delta f$= noise power spectral density
- Δf= noise bandwidth
- $\Gamma_{rms}^2 = \sum_{n=0}^{\infty} C_n^2$=root mean square (RMS) value of $\Gamma(x)$
- $\Gamma(x) = C_0/2 + \sum_{n=1}^{\infty} C_n \cos(nx + \theta_n)$=ISF
- C_n=Fourier series coefficients
- C_0=0th order of the ISF
- θ_n= phase of the nth harmonic
- f_m= offset from the carrier
- $\omega_{1/f}$= flicker corner frequency of the device
- q_{max}=maximum charge stored across the capacitor in the resonator

If the same simplifying Leeson assumptions are made (LTI model, stationary noise, noise-free wave form is a sinusoid), [3] the equations for the phase noise become similar:

$$\mathcal{L}(\Delta\omega) = 10\log\Big[\frac{1}{2}\frac{kT}{V_{max}^2}\frac{1}{R_p(C\omega_0)^2}\Big(\frac{\omega_0}{\Delta\omega}\Big)^2\Big] \tag{1.19}$$

where R_p is the equivalent tank parallel resistor, and the relative quality factor is $Q = R_p\sqrt{\frac{C}{L}}$. **Therefore is very important to have large voltage output, and to design an inductor with high quality factor that it means to have high value of equivalent R_p.**

Insights on oscillator's phase noise

In this paragraph there is a discussion of generation of phase noise in the cross-couples differential pair oscillator in order to improve the design for low phase noise VCO. It has been seen that the shape of the current waveforms is very important to have low phase noise, [12].

Phase noise in bipolar cross-coupled differential pair oscillator The study of phase noise in cross-coupled differential pair oscillator can be made using the schematic depicted in Figure 1.16 and remanding at the [6] for a rigorous discussion. We can see that the bias of transistors is decoupled from the DC voltage source to avoid forward biasing in the transistors base-collector junctions which would increase phase noise as consequence [6]. For this reason, the bases of bipolar transistors are biased at $V_B < V_{cc}$ and only a fraction of the tank amplitude is fed back into the cross coupled base, this fraction derives from the capacitor divider $n = \frac{C_1}{C_1+C_2}$. Voltage oscillation at the bipolar base is important for the generation of noise.
Here there are some equation about the behaviour of the circuit:

$$V_{tank,+}(\phi) = A_{tank}\sin(\phi) \tag{1.20}$$

where $\phi = \omega_0 t$.

$$A_{tank} \approx \frac{2}{\pi}(2I_B)R_p \tag{1.21}$$

The last equation, given from [9] said that current is directly proportional to voltage amplitude, then to increase amplitude, the first thing to do is to increase bias current. In the analysis of [6] the noise generated from collector current shot noise and base resistance noise is included. At the end, the formula of phase noise neglecting the component relative at the base resistance is:

$$\mathcal{L}_{i_c+R_p}(f_m) = 10\log\Big[\frac{1}{2}\frac{kT}{A_{tank}^2}\frac{1}{R_p(C\Delta\omega)^2}\Big(1+\frac{1}{2n}\Big)\Big] \tag{1.22}$$

The value n is very important, looking at the equation 1.22, in order to have the lowest phase noise is convenient that n should be closed to 1 but as we said before is important to pay attention at the base-collector junction to avoid saturation of transistors, therefore the choise of n and V_B should be optimized to have minimum phase noise.

Tail current-shaping and class-C biasing Looking at the figure 1.17 we can see the main contributors to the phase noise of the cross differential couple VCO, that are the switching transistors M1 and M2, tail current sources and the thermal noise associated with the loss in the resonator. Now we are studying the transistors contribution. As it is said before, the sensitivity of the VCO's phase to current pulses referred to as impulse sensitivity function (ISF) [3]. ISF is typically large when the output voltage is close to the zero-crossing instants and typically small when the output voltage is close to maximum or minimum value. Hence the energy that sustains oscillation in the tank should be injected by current pulses in the right moment, when the ISF is minimum.
As is described in [12] if the conduction angle of each transistors of the differential cross couple is 2Φ, the formula for the amplitude of the first harmonic in the tank is:

$$A = I_{bias}R_p sinc\frac{\Phi}{\pi} \tag{1.23}$$

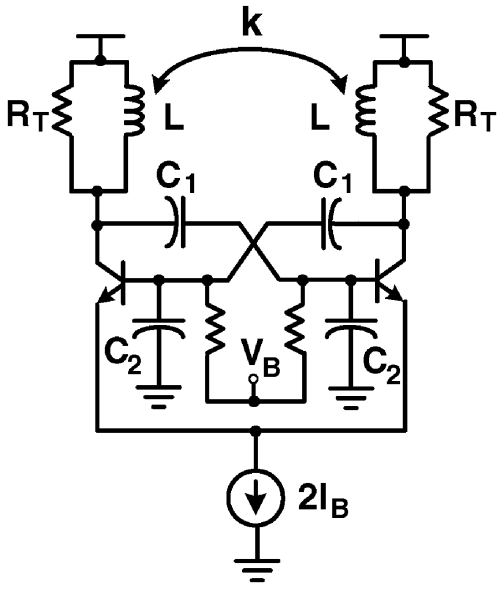


Fig. 1.16: Simplified schematic of differential cross couple oscillator

We can see that with low conduction angle, $sinc(\frac{\Phi}{\pi}) \approx 1$, the tank amplitude becomes:

$$A = I_{bias} R_p \tag{1.24}$$

with the consequence of phase noise reduction. [12] explain that the reduction of noise is due to also to smaller cross-coupled device noise up-conversion, and less tail current noise up-conversion. Also the flicker noise conversion is less, therefore the phase noise in the region $\frac{1}{f^3}$ will be lower with narrow pulses of current in the cross coupled transistors. The solution for the generation of this narrow pulses (class-C biasing) is to put a capacitor C_p in parallel to the tail current generator, [9]; the voltage at the tail node is then approximately a sinusoid with frequency $2\omega_0$.
The current on C_p is a sinusoid with frequency $2\omega_0$ too, and then the total tail current is $I_{tail} = I_{bias} + I_c$. Using this tail waveform, the voltage amplitude on tank become larger because the maximum tail current appear when the output voltage is maximum and therefore zero cross instant corresponds to minimum value of tail current, that is when the (ISF) is maximum. It is shown in [9] that if $n = 1$ the class-C operation does not afford any advantage in terms of effective transistors or tank noise contrary to what has been believed to date [12].
Nevertheless, the class-C operation results in an increase of the maximum voltage amplitude on thank due to a much more efficient generation of the fundamental current harmonic. This is true if the transistor remains in active region, but if it enter in satura-

tion this effect disappear. The use of tail capacitance is discussed a lot, many designers avoid the use of C_p as a major source of phase noise deterioration, but at the same time C_p become the key component generation impulse-like current waveforms in the class-C oscillator, provided the transistors are always in active region. In Figure 1.18 there is a schematic that represent the differential cross-coupled class-C oscillator with a capacitance between tank and base of transistors to decouple DC and to obtain more voltage swing, Figure 1.18.

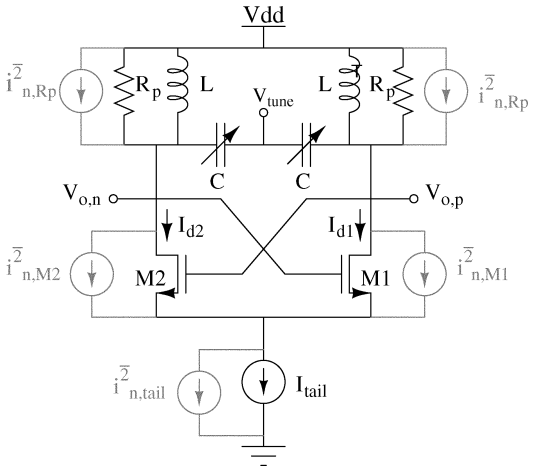


Fig. 1.17: Noise contributions

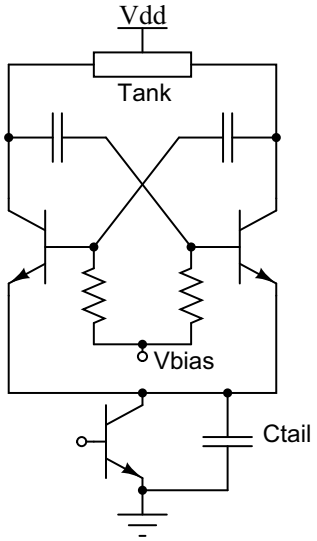


Fig. 1.18: Class C oscillator

1.3.3 Quality factor and inductor

As explained in the previous section, Q (quality factor) is a fundamental parameter for phase noise and is necessary to understand the definition of Q in order to be able to improve the phase noise of the oscillator. Q of a resonant system is considered to be high if the system loses little energy over time comparing to the energy circulating to the system. A definition of the quality factor is the ratio of the total energy in a system to the energy lost per cycle, [34].

$$Q \equiv \omega \frac{Stored\ energy}{Energy\ loss\ in\ one\ oscillation\ cycle} \tag{1.25}$$

An example of resonan network is depicted in Figure 1.19. R_p represent the losses of

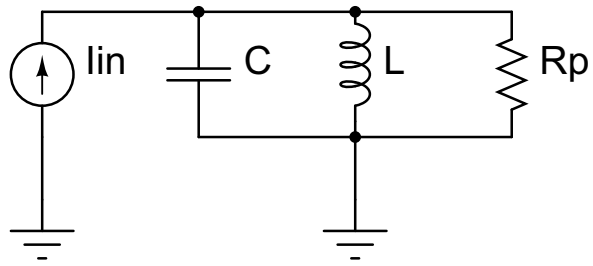


Fig. 1.19: Resonant network

the system; is easy to understand that if R_p is very big, the system resonates with low losses but if R_p is very small, a lot of current flow trough the resistance and more current must be injected by the generator; this is a practical explanation useful to understand the quality factor of a network.
The quality factor referred to the resonant system with impedance $Z(j\omega)$ is in equation 1.26:

$$Q \equiv \frac{Re(Z(j\omega))}{Im(Z(j\omega))} \tag{1.26}$$

Looking at the formula, the Q is inversely proportional to the series resistance of the equivalent impedance and from this consideration it is easy to realize that in a inductor modelled as an inductance with a resistance in series that represent electrical losses of the material, if this resistance is small, the coil is near to the ideality and the quality factor is very high. Using the Figure 1.19 we can extract the formula of the Q form the general definition; the energy stored in the system is:

$$E_{tot} = \frac{1}{2} C (I_{pk} R_p) \tag{1.27}$$

where $I_{pk}R_p$ is the maximum voltage across the capacitor. The energy loses in one cycle or the average power dissipated in the resistance is:

$$P_{avg} = \frac{1}{2} R_p (I_{pk}^2) \tag{1.28}$$

At the end, replacing in 1.25, the result is:

$$Q \equiv \frac{R_p}{\sqrt{L/C}} \tag{1.29}$$

The resonant network presents in this design is made essentially by an inductor and a varactor, this last component come from the technology available, thus is impossible to modify his quality factor.
The work is thus focus on the inductive element studying all the possible ways to make an element with high Q. For this reason, coil can be represented with a resistance R_s and an inductance in series L and obviously some parasitic capacitances. As in [34], the quality factor of the series RLC element is:

$$Q = \frac{\sqrt{L/C}}{R_s} \tag{1.30}$$

If the series resistance is small the quality factor increase, thus the goal of the coil design is to reduce at the minimum the series resistance. There is a relationship between the formula of the quality factor of the coil and the quality factor of a parallel RLC network, and the conversion between the series resistance and the parallel resistance is:

$$R_p \approx R_s Q^2 \tag{1.31}$$

where R_p is the equivalent parallel resistance of the coil as reported in [34]. Therefore, reduction at the minimum the series resistance result in an increase of the equivalent parallel resistance and obviously a reduction of the phase noise looking at the formula 1.19.
Another general definition of the quality factor at the value of the resonance is [34]

$$Q = \frac{f_0}{BW} \tag{1.32}$$

where f_0 is the frequency of resonance of the resonant element and BW is the bandwidth at -3dB of the impedance or admittance, depending of the tank representation is parallel or series.

Chapter 2

Design

2.1 Introduction to the design

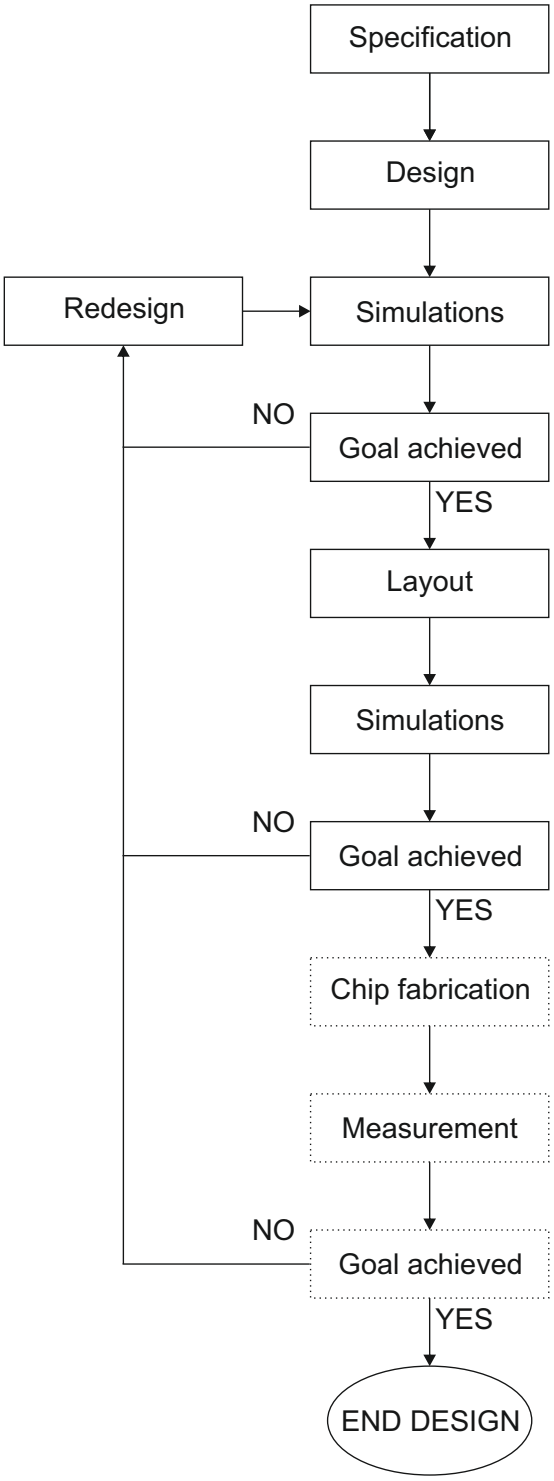
Before to start the real design we have to plan how to proceed; first off all we focus on the block diagram in Figure 2.1. Before the design there is the theory part, the study of the system and all the things that are connected to this. Then there is the study of the technology, like performance of components, components that are available, and then starts the real design.
After a theoretical study of specification resulting in a choose of topology circuit solution and in a focus on over we have to work to reach certain specification, we start to write the first calculation about the circuit. The initial tests are made with the simulator on ideal components with the help of the software "Cadence" and "ADS" in order to see if the system work correctly at least with all ideal stuffs.
The next operation is to add real component and looking at the result of the circuit and focusing on the study and improvement of the part of the circuit that can cause majority degradation of performance. After this, if it is impossible to reach certain performance or to satisfy certain specification should be useful to study another topology of the circuit. An important things is to study the differences between ideal components and real components, and try to improve the performance of real one in order to get closer to the ideals. For this reason in this design we focus at the begin on the tank, mainly on the inductive part because the varactor is available from the library.
At the end of the simulation, when the results have exceeded the specific or at least they are closer to them, layout operation will start, that is the placement of the real component into the silicon respecting technology rules by the help of the software. The connections between components have obviously a resistive and inductive behaviour and present a capacitance with the substrate and with other connections or components near there. The results considering parasitic resulting from the layout operation will degrade performance and should be possible a redesign of the circuit.
When good result comes from the design the real chip will be fabricated and than will be done measurement on this to see if the simulator results are true or not; after mea-

surement is possible to redesign the system if something is not comparable with expected results. This part of the design there isn't in this document.
Initial choose is to use differential cross-coupled LC-VCO, as is mentioned in theory chapter LC VCO present good performance in phase noise that is the most important specification to obtain; in addition, using differential system other forms of noise such as supply noise, are deleted.
After this we will focus on the design of a resonator with high quality factor Q that is an important things looking at the formula in the chapter 1.3.2. Then the coil is inserted into the first version of the circuit and the first simulation starts.
Is not easy to choose the right combination between coil size , varactor size and transistors size, because at the frequency of 20 GHz, transistors present an important capacitive value that add capacitance at the varactor changing the value of the resonance frequency and reducing the tuning range. After first results is possible to increase performance changing a little bit topology of the circuit or try to made resonator with better Q.
In addition to phase noise we can use another way to tests performance of oscillators, FOM (figure of merit):

$$FOM = \mathcal{L}(f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \tag{2.1}$$

$$FOM_T = \mathcal{L}(f_m) - 20\log\left(\frac{f_0}{f_m}\frac{FTR}{10}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \tag{2.2}$$

where $\mathcal{L}(f_m)$ is the phase noise at the offset frequency of f_m, f_0 is the resonance frequency, FTR is the percentage of tuning range and P_{diss} is the power consumption in mW. Second equation present a figure of merit considering also the tuning range, the first one consider only phase noise and power consumption.
In the following part of the chapter, we explain initially the design of a good LC resonator, after that there are the simulations of LC-VCO with comments and possible changes to make at the circuit; then we explain a second version of VCO with a transformer instead of the coil to decouple the varactor from DC supply voltage.
At the end we'll do some comments about various versions of VCOs.


Specification
Design
Redesign
Simulations
NO
Goal achieved
YES
Layout
Simulations
NO
Goal achieved
YES
Chip fabrication
Measurement
NO
Goal achieved
YES
END DESIGN

2.2 Coil design

As it is explained in the chapter 1.3.2, the two most important things to have low phase noise in oscillators are high resonator Q and high output voltage swing. We focus on this two components to try to get best phase noise performance from the circuit. First of all, we work on resonator design trying to have maximum quality factor of the system. It is known that the resistive part of varactor and inductor deteriorate this value, in fact:

$$Q = \frac{Im(Z(j\omega))}{Re(Z(j\omega))} \tag{2.3}$$

where $Z(j\omega)$ is the equivalent impedance of the component in analysis. Real part represent the series resistance, thus the objective is to made a resonator with low resistive part.
At the resonance frequency it is convenient to use this equation that is explained in the section 1.3.3:

$$Q = \frac{f_0}{BW} \tag{2.4}$$

Initial simulations are about an inductive part made by a transmission line; results were not good, therefore the second option is to realize coil on the less conductive layer available in the technology.
Before design a coil with high performance it is necessary to study the effects of high frequency in the structure that we'll design, like skin effect and eddy current effect and currents in the substrate [24], [33], [28], [29],[4]. The main objective is to maintain the lowest possible resistance of the coil following these rules:

- *Limit the width of the metal conductors:* at low frequencies, if the conductor is larger than less resistive part it presents. At high frequencies, skin effect and current crowing effect dominate [26],[5], [28] in the center of wide conductor the current doesn't flow, for this reason, very wide metal conductors are not efficient.

- *Do not fill inductor up to the center:* due to generation off eddy current at high frequencies, the inner most turn suffer of high resistance and minimal inductive contribute, this result in a reduction of quality factor.

- *Limit the area occupied by the coil:* at high frequencies, the magnetic field induces current in the substrate that causes more resistive losses and a decrease in inductance. The magnetic field of small coil penetrates less deep into the substrate.

Design a good coil is not very simple, in addition to the above considerations, it is important to choose a good combination between coil and varactor, in order to ensure the right tuning range and to pay attention that the varactor has an equivalent series resistance too. Another important things is the layout, at high frequencies the connections

between components have high resistance, in addition the values of inductance of the coil are very small and comparable with inductive part of connection; for this reason it is important to make as short as possible connection, this will be better explained in the chapter 3. If the varactor is too huge, the connections between coil and him have an important inductive part that should change the value of resonance frequency predicted with calculations. A good coil design includes all these rules in order to obtain the best performance.

The frequency of resonance is $\omega_0 = \frac{1}{\sqrt{LC_{tot}}}$ where C_{tot} is the global capacitance seen by coil and it includes varactor, parasitic capacitance of bipolar devices and all parasitic capacitive element in parallel at the tank. In order to ensure a good frequency, to consider all these effect is very important in the design. Our working frequency is around 20 GHz, the inductance value in order to have a coil not very large and a compact form of the tank , it is around 100-200 pH and the values of varactors to ensure a good tuning value is around 500-600 fF. After these considerations and calculations, the design of the coil and electromagnetic simulation will start.

The first inductors were made by a rectangular shape and it had low quality factor, around 10 at 20 Ghz, then other test were made on octagonal shape with very good results, Q of 25-30. To avoid intricacies in the project and to avoid the effect of eddy current in the inner turn, we choose to realize only one turn. Another advantage of this is to profit by the space in the middle of the coil for active area that is far from the metal layer so doesn't affect significantly magnetic field.

In addition, in order to avoid losses due to the skin effect we chose to realize a turn with two stripe in parallel [1], like in Figure 2.2, with this solution the Q reached is around 37 at the frequency of 20 GHz. Looking at the curve of Q in Figure 2.3, it is important that the peak of the Q is at higher frequencies because that is the resonance of the coil, not the resonance of the entire tank, we have still to add capacitive part. Another important thing is that the value of inductance of the coil should be extract at low frequency where the parasitic capacitance of the layer does not affect significantly this value.

We can see in the Figure 2.2 the final shape of the coil used in the design, this is a result of a series of redesigns in order to adjust the parasitic effects after layout.

In the Figure 2.4 is depicted the equivalent resistance of the designed coil, is possible to see the physical effects seen above, resulting in an increase of resistance at high frequencies. The value of series resistance is around $R_s = 0.35\Omega$ and using the approximation $R_p \cong \frac{\omega^2 L^2}{R_s} \cong 950\Omega$ we see the value of the resistance parallel to the tank due to the coil. The parallel resistance of the vractor will be added.

Inserting the varactor, obviously the quality factor of the tank decrease, we can see in the Figure 2.7, the quality factor of the entire tank decrease, arriving at the value of 10-15. Another important things is the variation of the vractor quality factor due to the voltage applied at its cathode. We can see in Figure 2.7 that at the frequency of 20 GHz the

quality factor of the tank decrease a lot with low voltage applied at the junction.
In the Figure 2.5 is depicted a representation of varactor that is made by a couple of diode with common cathode.
Biasing inversely the junction, is possible to vary capacitance of the system varying voltage in the common node using the characteristic V-C of the p-n junction. In the model there are also two capacitor in parallel to the varactor that is used to fix the precise resonance frequency after the insertion of bjt that can cause displacements of tuning range.
In the Picture 2.6 there is an example of varactor layout: external stripes are the common cathodes, and internal part represent the junctions (A1-A2) are the 2 diodes for the differential use.

Tab. 2.1: Coil parameters

L	145 pH
Internal radius	41 μm
External radius	72,4 μm
R at 20 GHz	0.4 Ω
Q at 20 GHz	37

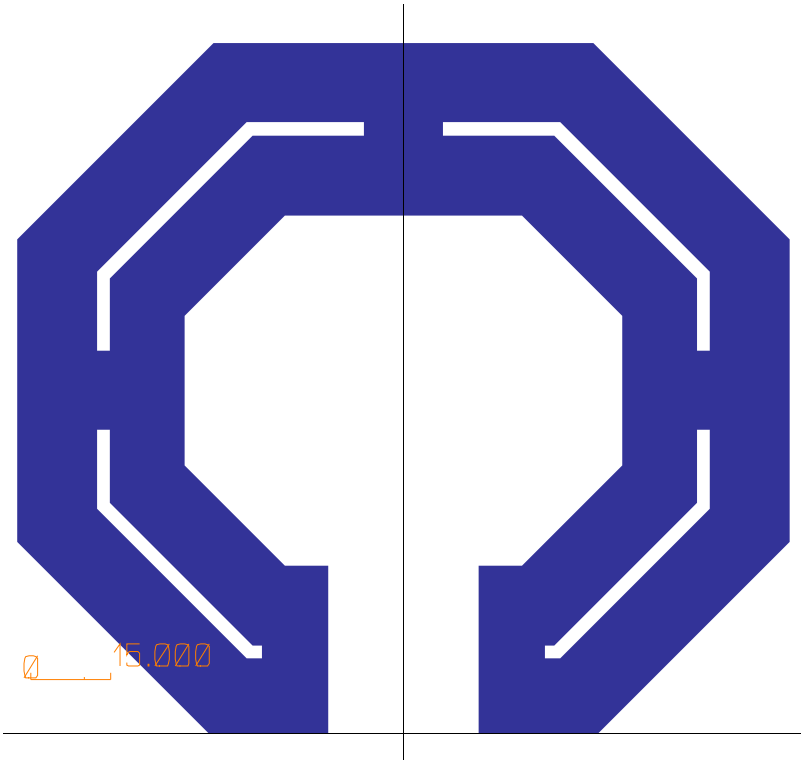


Fig. 2.2: Coil used in the design

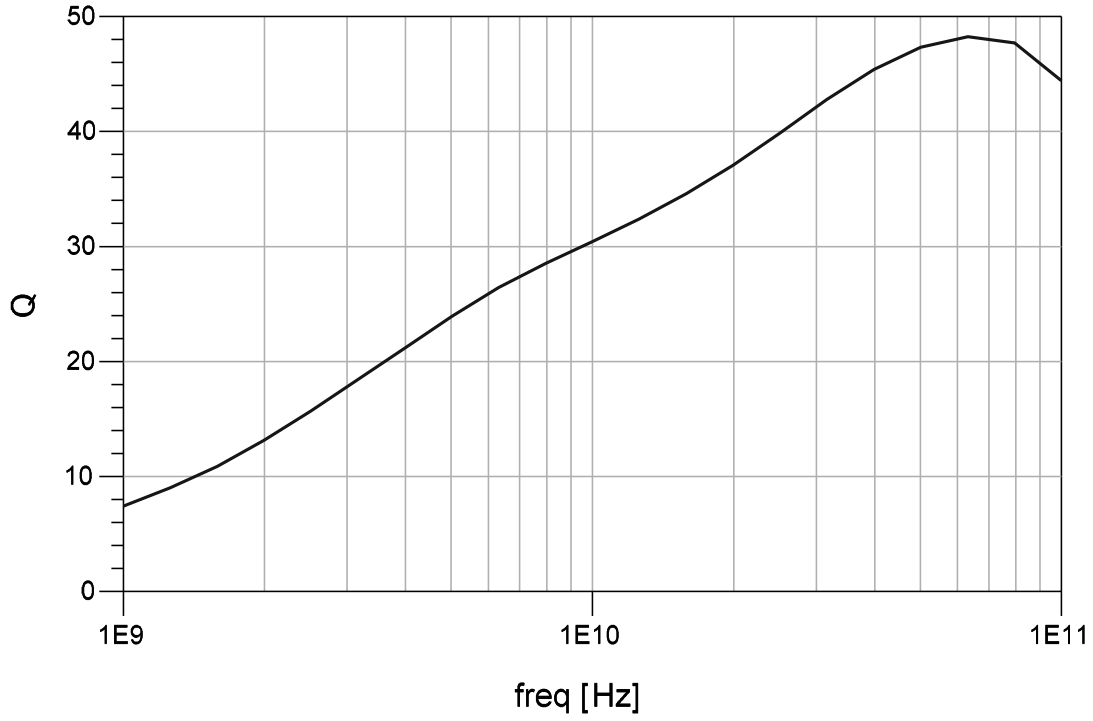


Fig. 2.3: Quality factor of the coil at various frequencies, $Q = \frac{Im[Z(j\omega)]}{Re[Z(j\omega)]}$

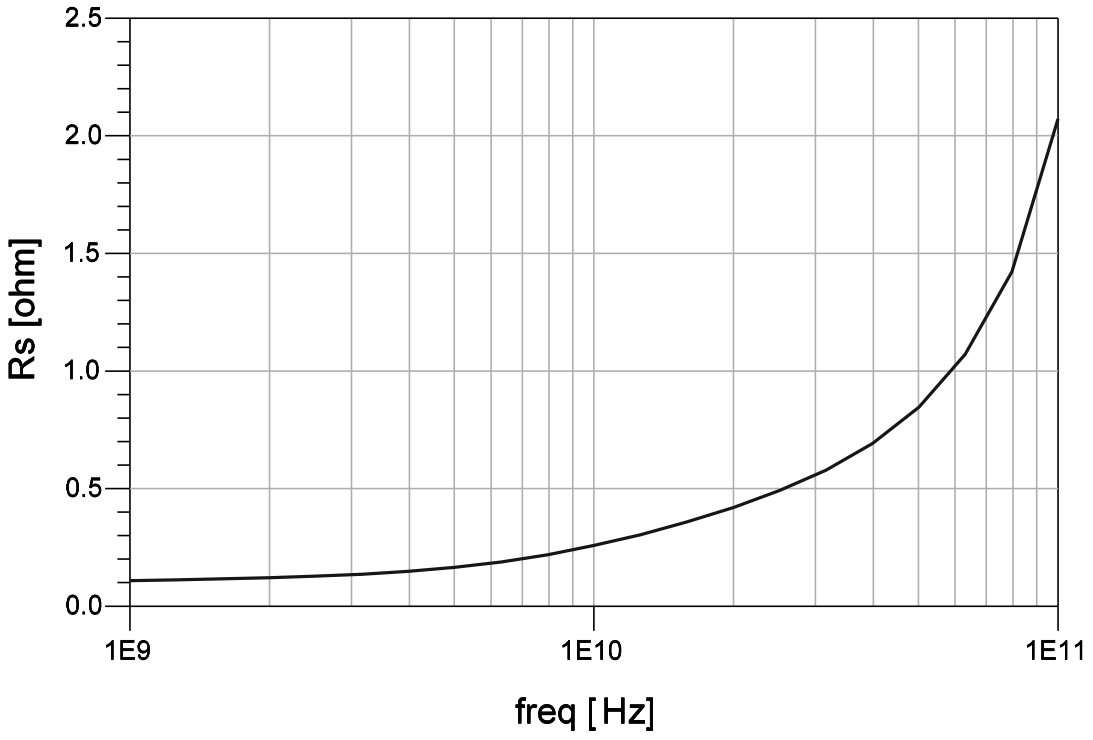


Fig. 2.4: Series resistance of coil at various frequencies $Rcoil = Re[Z(j\omega)]$

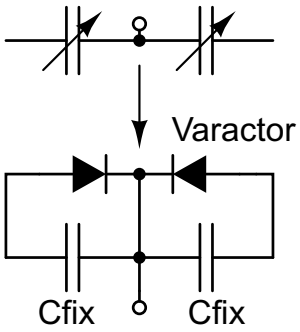


Fig. 2.5: Electric representation of vractor

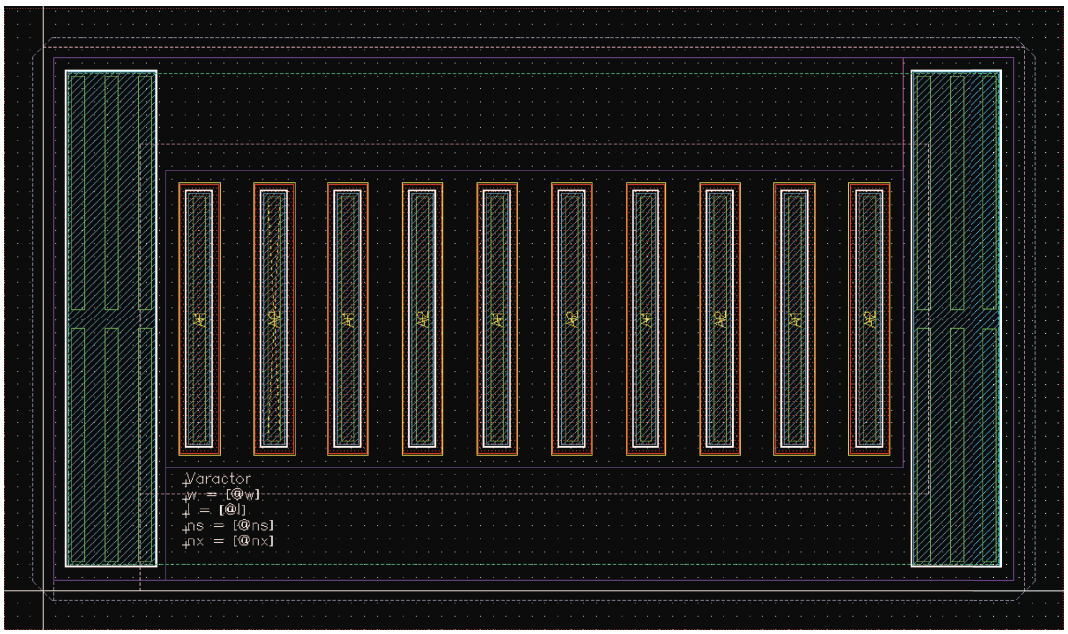


Fig. 2.6: Varactor layout

The problem explained above refers to this, in fact if the voltage across the junction in absolute value become small, the diode is nearer to the conduction zone, thus its equivalent parallel resistance becomes smaller resulting in a degradation of the Q.
The result of the graph in Figure 2.7 is referred to a biasing of 3.3 volt at the anode of varactor and a various voltage amplitude (V_{tune}) at the cathode.
If the Vtune (voltage applied at cathode of varactor) is 3.3 V, the junction has 0 V and actually it is not inversely biased, the resulting quality factor is low, seeing at the solid-line in the Figure 2.7, at 20 GHz his value is 13. Instead, with Vtune=8 volt (dot-line), the junction is inversely biased with a voltage of -4.7 V, we see that now the tank quality factor is higher, $Q_{20GHz} = 27$. This thing is very important because limit the possibility range of voltage Vtune and for this reason we have to find other topology solution to limit the value at 3.3 V if possible. Another delicate things regards the

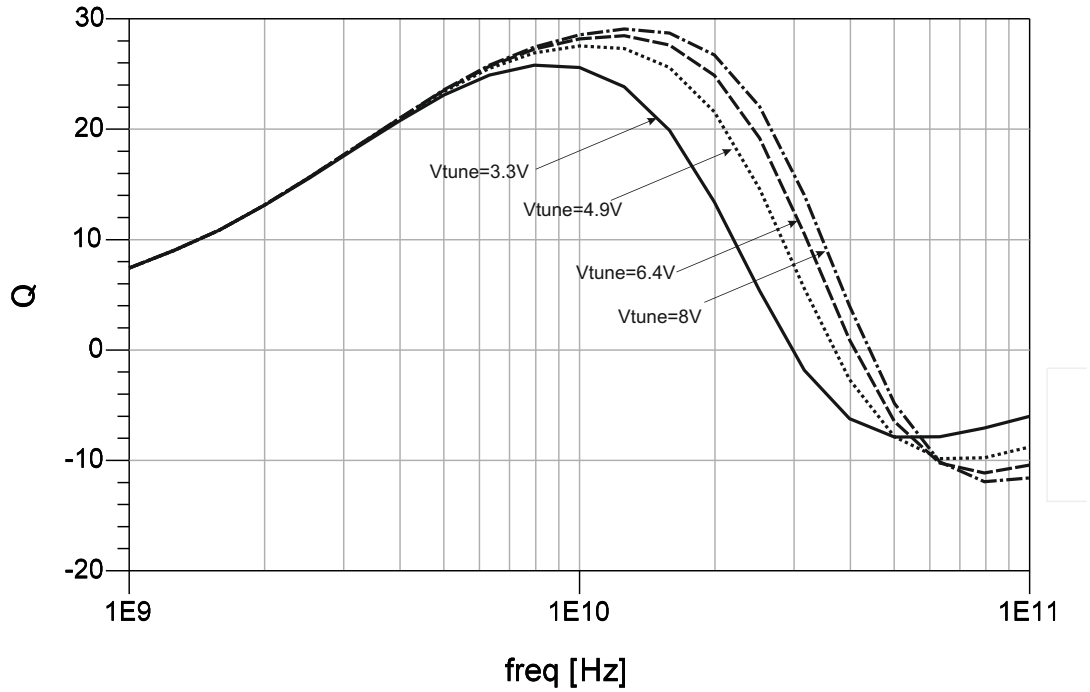


Fig. 2.7: Quality factor of the tank, $Q = \frac{Im[Z(j\omega)]}{Re[Z(j\omega)]}$

voltage amplitude swing across the varactor; we can simulate the signal across it varying the amplitude of the ac current and varying the tuning voltage Vtune. In the first graph, 2.8 is depicted the various value of the amplitude voltage of a sinusoidal signal across the tank. Each different line-style represent a constant value of current; for low value of Vtune the equivalent voltage increase a bit and this effect is more evident with high value of currents. The consequence is that the equivalent resistive part of the impedance becomes bigger resulting in a degradation of the quality factor. This is show in Figure

2.9, where the various lines are referred to the same ones of the precedent graph. Looking at the curve representing an amplitude of approximately 3 V, if Vtune is low, for example 3.5 V, in a part of a signal period, the diode conducts and his parallel resistance is very low, for this reason the Q will be destroyed. If the tuning voltage goes down 4 V, Q becomes very critical and phase noise will be deteriorated.
Remembering at the formula of Phase noise in the section 1.3.2, the quality factor of the tank inversely proportional to the phase noise, then a degradation of Q of factor 2 produce an increment of PN of 3 dBc/HZ. Therefore is very determinant to have an high Q on the tank and avoid the conduction of the diode in the range of frequencies used.

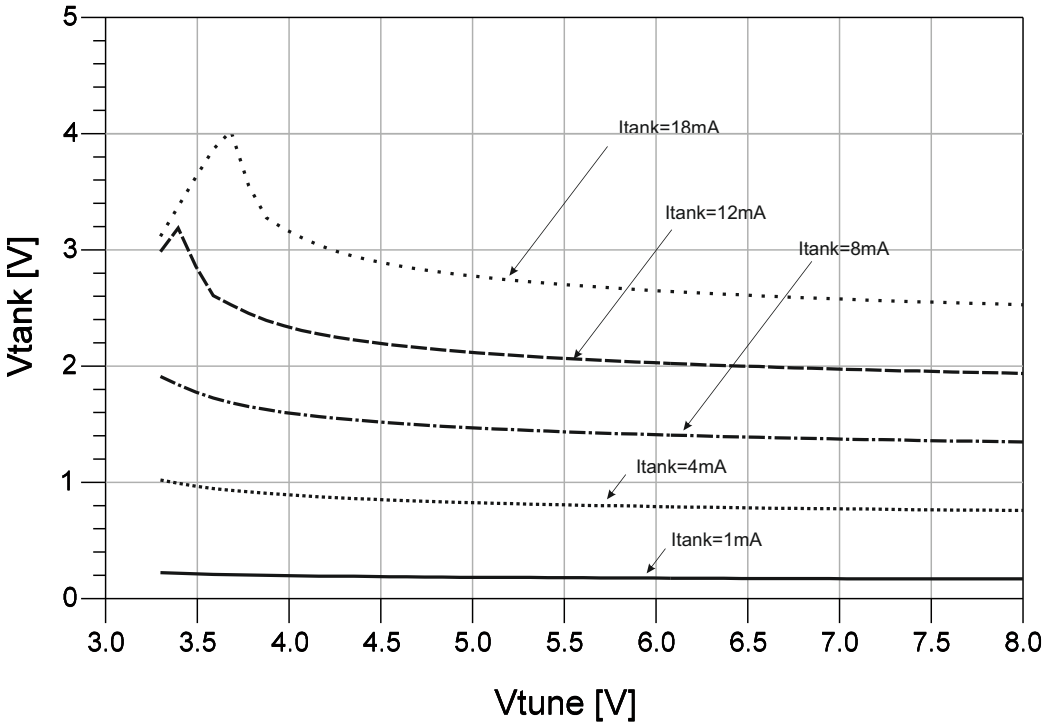


Fig. 2.8: Amplitude on the tank

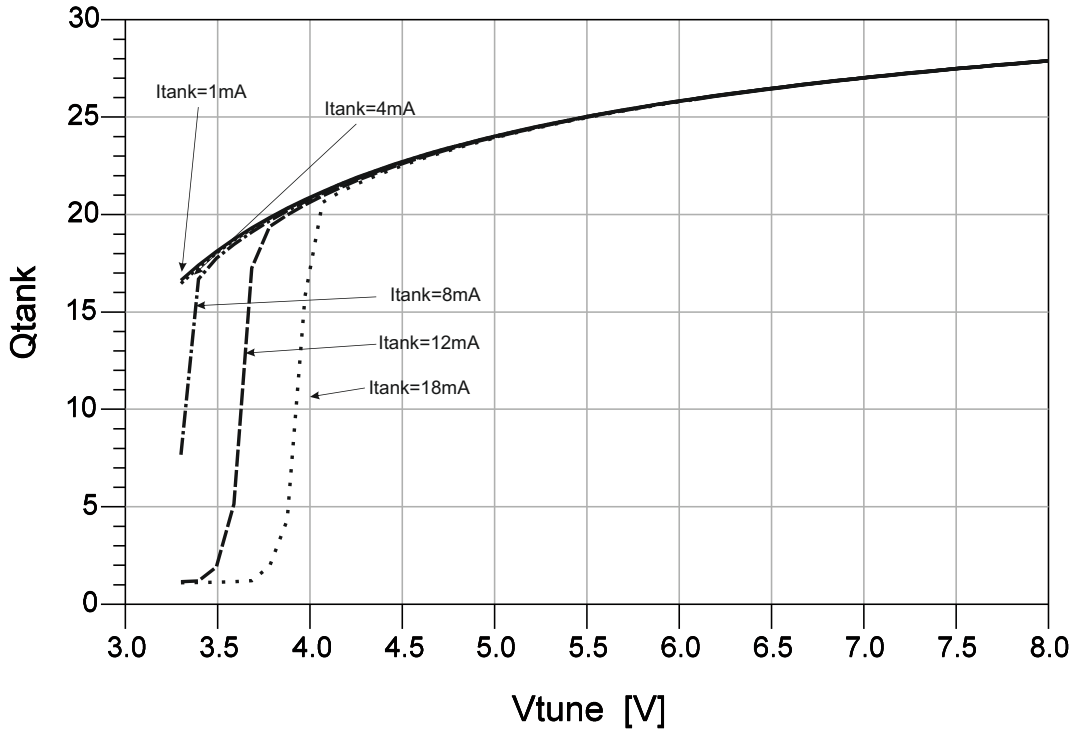


Fig. 2.9: Quality factor of the tank changing amplitude swing, $Q = \frac{Im[Z(j\omega)]}{Re[Z(j\omega)]}$

It is seen that find a good combination for the coil design is not very simple, a lot of factors combine together and the correct way is to focus on the things related to the performance required in the project. For example in this design is not so important the power consumption, therefore is possible to take advantage from this, knowing that the power is proportional to the square of the capacitance in the tank, then reducing dimension of coil, having the same frequency of resonance, will be bigger capacitor resulting in an increase of power consumption.
In the section 2.3 there is the first version of VCO designed.

2.3 VCO with coil

First version of VCO is made by a differential cross-coupled using the coil described in the previous section. At the begin, the first tests are made with a system close to the ideality. The only real components are varactors and bipolar transistors of the differential couple. An ideal current generator is used for the biasing of the transistors and the coil is made by an ideal inductor.

The work is now concentrated on the value of current biasing, evaluating the maximum current that can pass into the active devices and considering equation in section 1.3.2. In fact the value of biasing current is directly proportional to the voltage amplitude across the tank. Since there are no specification about the power consumption, a good choice is to bias devices with high value of current in order to have high swing.

Theory said that the swing is the most important thing in order to decrease the phase noise, for this reason, we'll search to use the highest swing possible, paying attention at the conduction in the varactor, see section 2.2.

The first simulations are with the simple configuration, shorting the base of one transistor

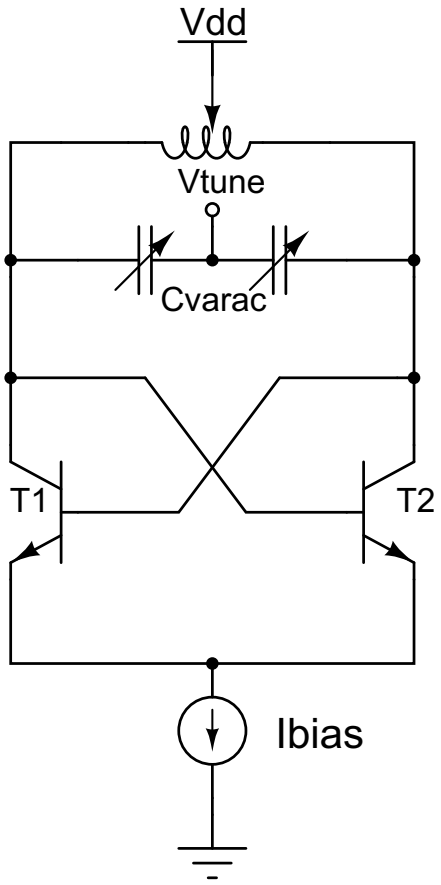


Fig. 2.10: LC differential cross couple VCO

with the collector of the second transistors of the differential pair. It is easy to understand that the bases of the transistors are biased at the same voltage of the collector, therefore

the swing across the junction b-c will be limited from the saturation region of the active device.
The test with this configuration give a minimum phase noise around -105 dBc/Hz in the best case even with ideal inductor instead of the real coil. A possible solution is to decouple the base from the collector with a capacitor and biasing the base of transistors with an external voltage Vbias. With this solution we can extend the swing across the tank biasing the devices of the differential couple near to the class C. Before starting other simulation with this topology, it is necessary to check the datasheet of active device to see if the features are sufficient for the limit of currents and the voltage across the junction.

2.3.1 Choice of bipolar transistor

Technology gives some transistors for this IC-application, the active devices are bipolar transistors for high frequency, maximum frequency of bjt is 200 GHz and the materials of the junctions are Si-Ge. As we said in the Chapter 1.3.2, the two main sources of noise are the losses on the resonator and the noise injected by active devices of the differential pair. For this reason, the choice of the typology of device is quite important.
The first simulation were made with **high-speed** devices, they have a very high transient frequency, around 200 GHz, and they have a good capacity of maximum current. The voltage break-down is a big problem of this typology of bipolar devices [23], therefore we have to pay attention at the amplitude of the swing and this gives some limits.
The other model used in the simulation is **high-voltage** devices, they have lower tran-

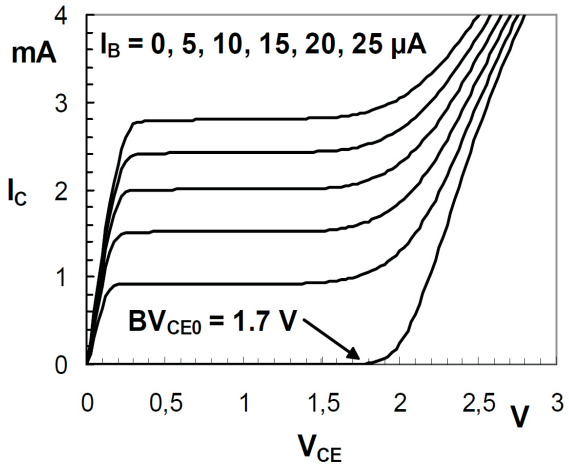


Fig. 2.11: Characteristic IC-VCE of high speed transistors

sient frequency, around 40 GHz, high voltage break-down and they can support less current, for this reason the size will increase. Considering low amplitude voltage swing, result with high-speed transistor give better result than high-voltage about phase-noise, this indicate that they have less noise contribution, furthermore with the same current

consumption, high-speed are smaller than high-voltage, resulting in a less parasitic contribution. In conclusion, first devices should give a better value of figure of merit but the most important specification in this design is the low phase noise, so we have to concentrate on this.
Increasing the voltage swing in order to reduce phase noise, we will see that the low value of break-down of high-speed model compromise the results and using high-voltage model this problem does not appear. For this reason we will use high-voltage model, even if they inject more noise, but the possibility to have an high swing results to be more important.

2.3.2 Biasing

After these initial consideration about certain choice to take in order to decrease the phase noise, the first thing to do in a common design is the biasing of the circuit.
Obviously the dimension of the bipolar devices has to satisfy the relation $g_m > \frac{2}{R}$, the transconductance must be big enough to compensate the global losses of the tank, and we know that it is linked to the biasing current of the transistors, $g_m = I_C/V_t$, the ratio between the biasing collector current in the bjt and the thermal voltage. Increasing current, we have to increase the dimension of the emitters, that cause certainly an increment of the parasitic capacitance.
There is an interesting graph to see before to choice the value of the bias current, Figure 2.12. In the picture 2.12, we see that the best value of Ibias is near to the knee of the curve $I - V_{out}$, this means that the best value of phase noise corresponds at the minimum value of Ibias to ensure the maximum output voltage; there is an equation to find this value of current, "Abidi model" [25]. This model, Equation 2.5 is useful to find the noise factor F for the Leeson model of phase noise.

$$I_{bias} = \frac{\pi V_{dd}}{2R_p} \tag{2.5}$$

Where R_p is the total parallel loss resistance of the tank. This equation is extracted using the maximum ideal voltage that is the supply voltage.
In addition to this, it is important to say that is not very good to have huge transistors:

- more parasitic capacitance resulting in a reduction of tuning range;
- difficult placement of devices in the layout operations that implies longer connections;

We have to choose a good compromise between all this elements, it is necessary to change component, biasing current, dimensions of devices a lot of times but the important things is to have a good starting point.

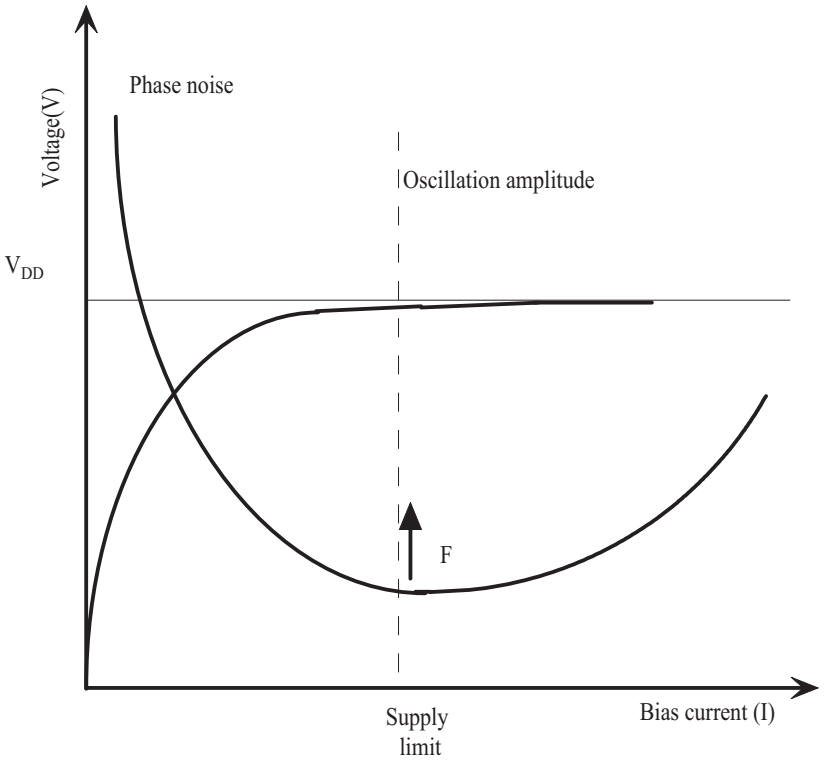


Fig. 2.12: Ibias versus voltage and phase noise

2.3.3 Improvement of Phase noise

When the Ibias has been chosen, we start to focus on the improvement of phase noise looking at the theory and trying to find the limits of the design. Focusing on the formula 1.19 and analysing only the noise of the tank, it is possible to extract the following equation:

$$\mathcal{L}(f_m) = 10\log\Big[\frac{1}{2}\frac{kT}{V_{max}^2}\frac{L^2\omega_0^2}{R_p}\Big(\frac{\omega_0}{\Delta\omega}\Big)^2\Big] \tag{2.6}$$

This represents a strong simplification, from here we can calculate approximately the minimum theoretical value of phase noise that is possible to reach with an LC oscillator. If we consider all ideal things, the unique contribution come from R_P that is the parallel resistance of the tank model. With the tank described in the previous section 2.2, and with the maximum possible voltage swing, the minimum theoretical value of phase noise is -139 dBc/Hz.

This is the physical limit considering the effective noise figure F of the feedback system equal to one. This is impossible in the real systems $F > 1$, normally this factor is extracted from the simulations, and it depend from a lot of things , topology, devices, etc, but an example of calculation is made in [35].

A minimum value for the factor F could be 3. With this, the minimum phase noise due too the R_p become $\mathcal{L}(f_m) = -134dBc/Hz$. Now we can add the component of phase noise considering the collector current of the transistor like in 1.22, and the result is

$\mathcal{L}(f_m)$ = **-133 dBc/Hz** at a frequency offset of 1 MHz.
This result is obtained considering the highest voltage swing possible, that is two times the supply, if we consider the maximum voltage possible using high-speed the limit became **-123 dBc/Hz**, the difference is very huge. Obviously this limit is impossible to reach with real component:

- Is impossible to have a differential output voltage exactly two times the supply voltage because transistors have a $V_{CES} > 0$, which is voltage collector-emitter saturation of transistors.
- The tail bias current is not ideal and it injects noise in to the system [14], in addition it is made by a current mirror that have also an emitter resistance, therefore it causes ulterior loss in the output amplitude.
- Another source of noise is the base resistance of bipolar devices, [6].
- The model used for the initial estimates of phase noise presents a lot of simplification, [6] and could be not very near to the real systems.

At this point of the design, we can start to add at the simulation the real component. As we said before the transistor used are the high-voltage to ensure high voltage at the output without overcome the limits of break-down, the dimension of this transistors depends from the bias current that has been chosen to ensure a wide amplitude output swing, as explained above. If the dimension of the transistor are too big, a lot of parasitic capacitance is added to the varactor and this can cause shifting in the center frequency and also reduction of tuning range, it is convenient to lower a bit the sizes of transistors and therefore lower the bias current too. Another things to do in order to have more tuning range is to change the dimension of varactor but this comport a redesign of the coil and probably a degradation of the quality factor reached before in the analysis of tank. Therefore this second option is discarded if possible.
In order to increase the output voltage, the first operation to do is to put a RC filter between the base of one transistor and the collector of the opposite transistor and biasing the base with a voltage lower than the supply voltage. The schematic is in figure 2.13.
At this point, we can see looking also at the Figure 1.16 in the phase noise section, that there is a capacitor divider in the bjt base. If $C_1 = C_c$ is the capacitor of the filter and C_2 is che sum of the capacitance in the base of bipolars, the value of voltage at the base to collector is: $V_b/V_c = V_c n$ and $n = \frac{C_1}{C_1+C_2}$,hence we have to pay attention at the value of the cross capacitor C_c.
Considering the biasing resistance R_b, the transfer function between base and the opposite collector is:

$$\frac{V_b(s)}{V_c(s)} = \frac{sR_bC_1}{1 + sR_b(C_1 + C_2)} \tag{2.7}$$

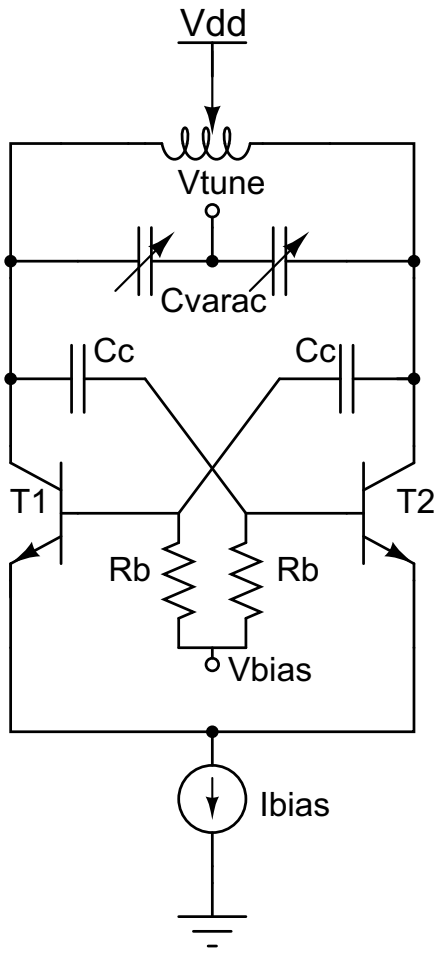


Fig. 2.13: LC differential cross couple VCO

that is an high pass filter, thus the frequency of the pole should be very low, therefore the value of the R_b has to be sufficiently high to do not influence the value of n. Regarding the phase noise of this circuit, the derivation of the model is in the section 1.3.2 and the equation is 1.22. The value of n is important in this design due to the characteristics of transistors. In fact, from the equation 1.22, n should be near to one in order to have less contribution of noise by the bipolar; the problem is the junction base-collector: if the amplitude at the base is too high, there is a forward biasing between base and collector, this degrade the formation of the first harmonic [9], resulting in a worse phase-noise. The choice of a precise value for n is not so easy, thus after an initial estimate, we have to rely to some parametric simulation.

Another component to change from ideal to real is the tail generator. This generator is replaced with a current mirror with ratio 1:10 in order to reduce the power consumption, at the emitter of the transistor there is a resistance (emitter degeneration) to increase the output resistance of the mirror and to have more robustness. The simulation results are better with this resistance.

The final schematic after these changes is depicted in Figure 2.14. In the following pic-

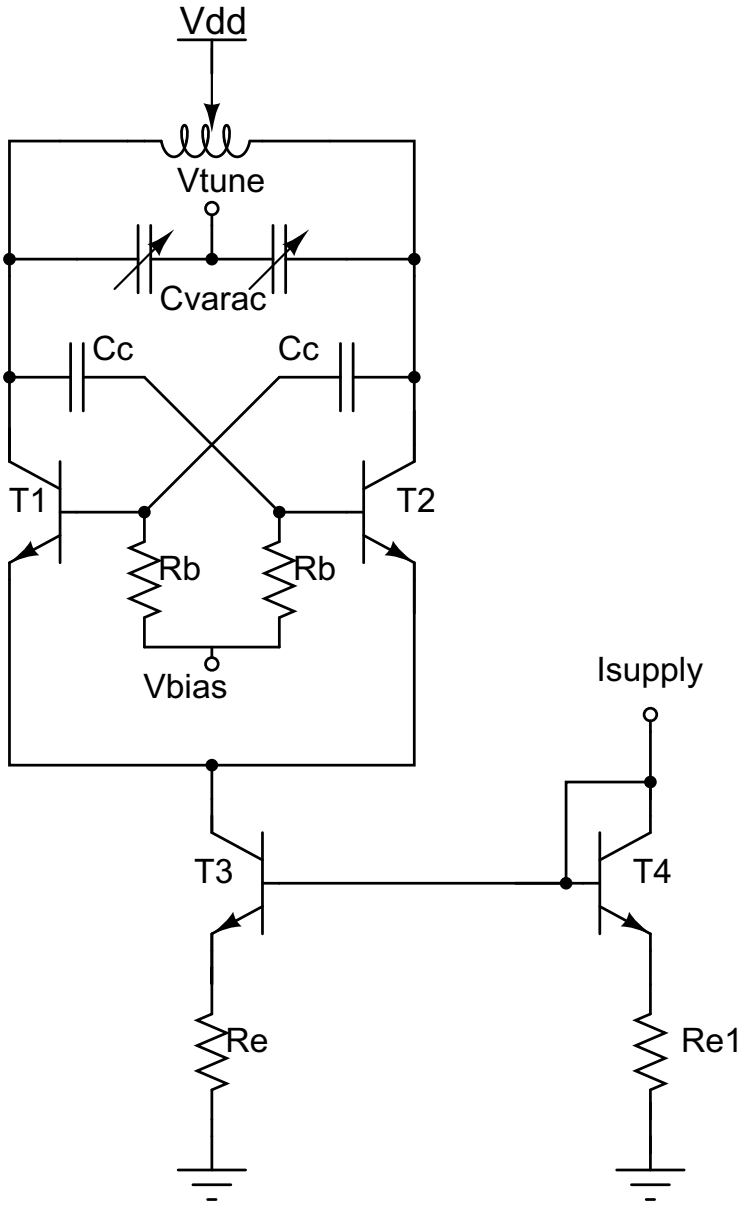


Fig. 2.14: VCO Coil schematic

tures there are the results of the simulation of this circuit considering the coil that is explained in the previous section. All these simulation are made varying temperature from -40 degree to +85 degree.

In the table 2.2 there are some parameters about the design.

In the graph 2.15 is depicted the phase noise at 1 MHz offset frequency versus tuning voltage, in the graph 2.16 there is the output frequency versus tuning voltage, in the graph 2.17 there is the differential output voltage versus tuning voltage and in the graph 2.18 is depicted the Phase Noise at the various offset frequency with $V_{tune} = 8V$ thus the best case of Phase noise. We can see that with low value of tuning voltage V_{tune}, the varactor affects the output differential voltage due to the biasing of the diode, this results in a decrement of the voltage and thus in a phase noise degradation, in addition the

Tab. 2.2: VCO coil parameter

V_{dd}	3.3 V
V_{tune}	3.5-8 V
V_{bias}	2 V
I_{bias}	1 mA
I_{supply}	20mA
P_{DC}	66 mW

quality factor of the varactor is worse at low V_{tune} therefore there is a further degradation of noise.

The frequency covers the range required (1.75GHz-19GHz) even at extreme temperatures, with the worst temperature and the minimum frequency, (worst case), the phase noise at 1 MHz offset is low than -120 dBc/Hz thus the results are good. Looking at the graph 2.18 we can see that the curve decreases with -20 dB/dec thus in order to improve these results, it is important to study the source of noise in the region $1/f^2$ and try to improve the design.

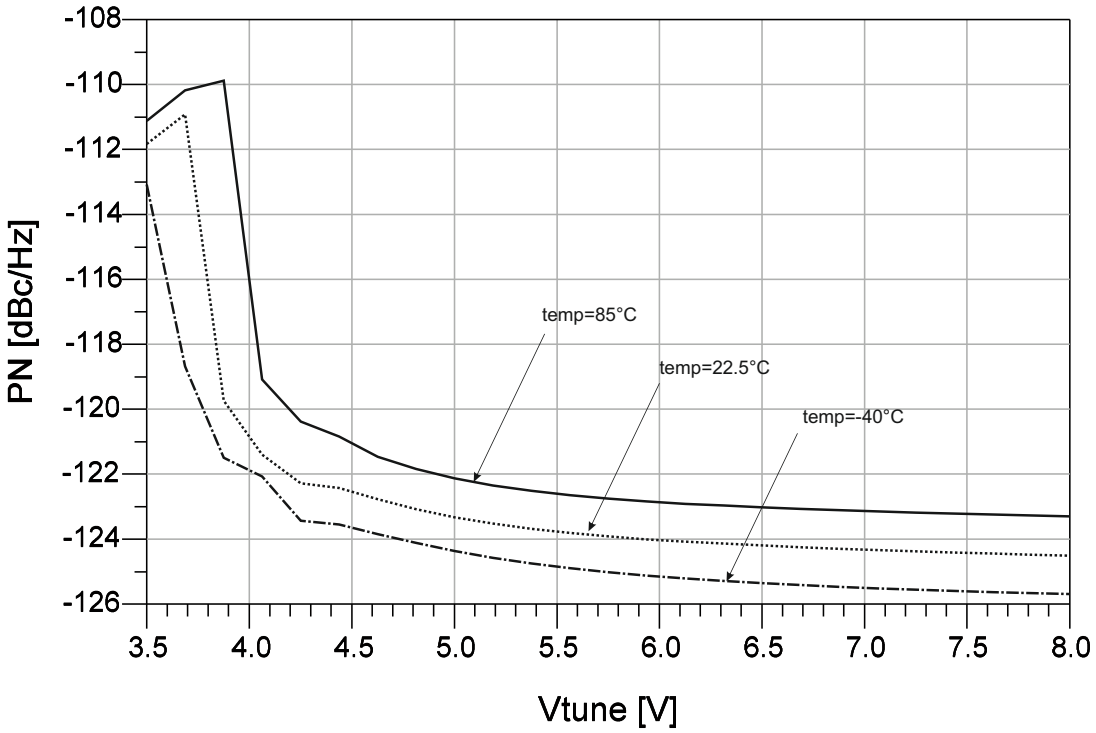


Fig. 2.15: Phase noise at 1 MHz offset versus tuning voltage Vtune varying temperature

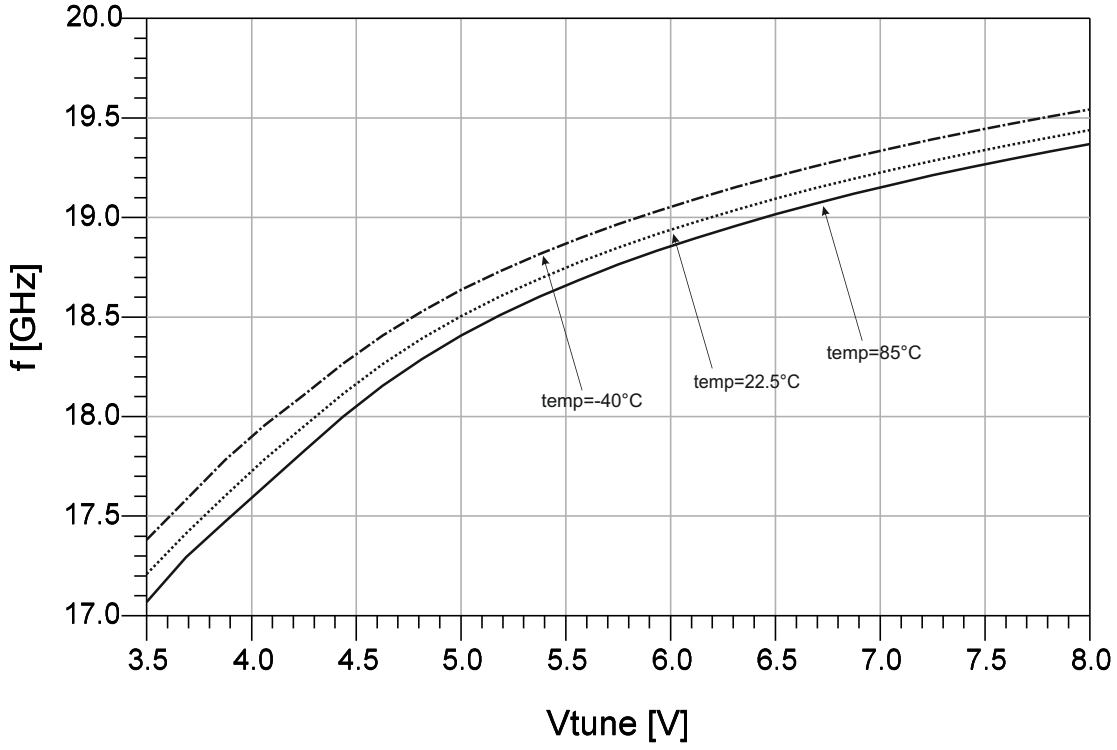


Fig. 2.16: Output frequency versus tuning voltage Vtune varying temperature

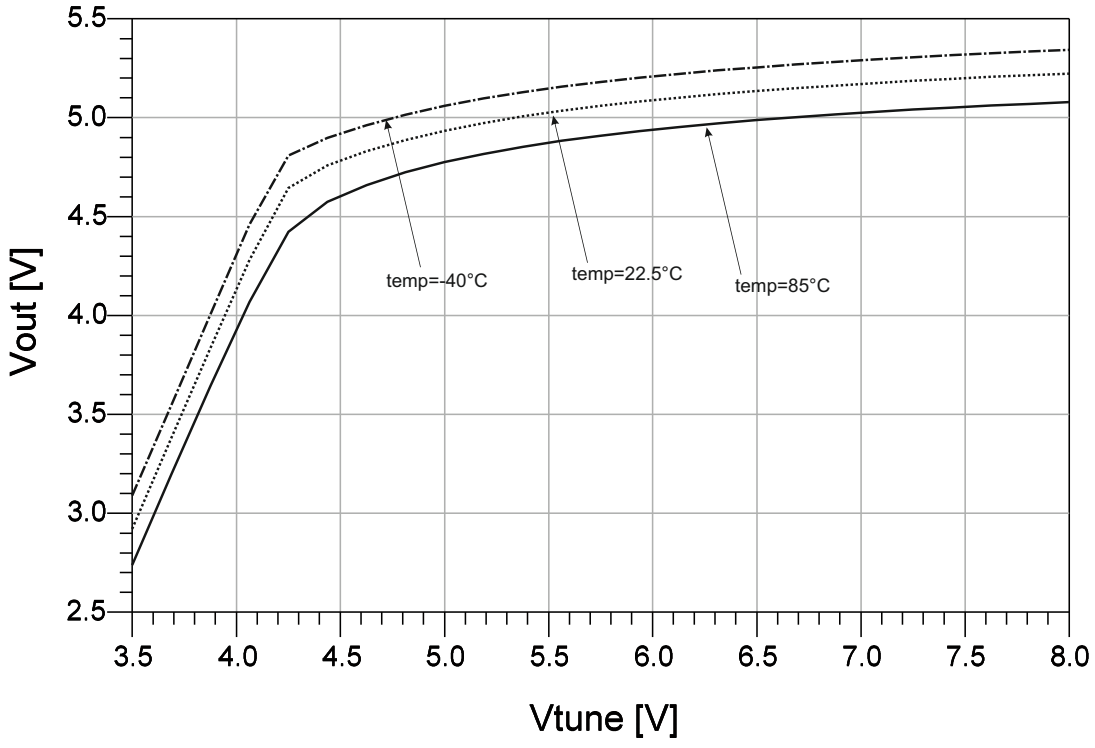


Fig. 2.17: Output voltage versus tuning voltage Vtune varying temperature

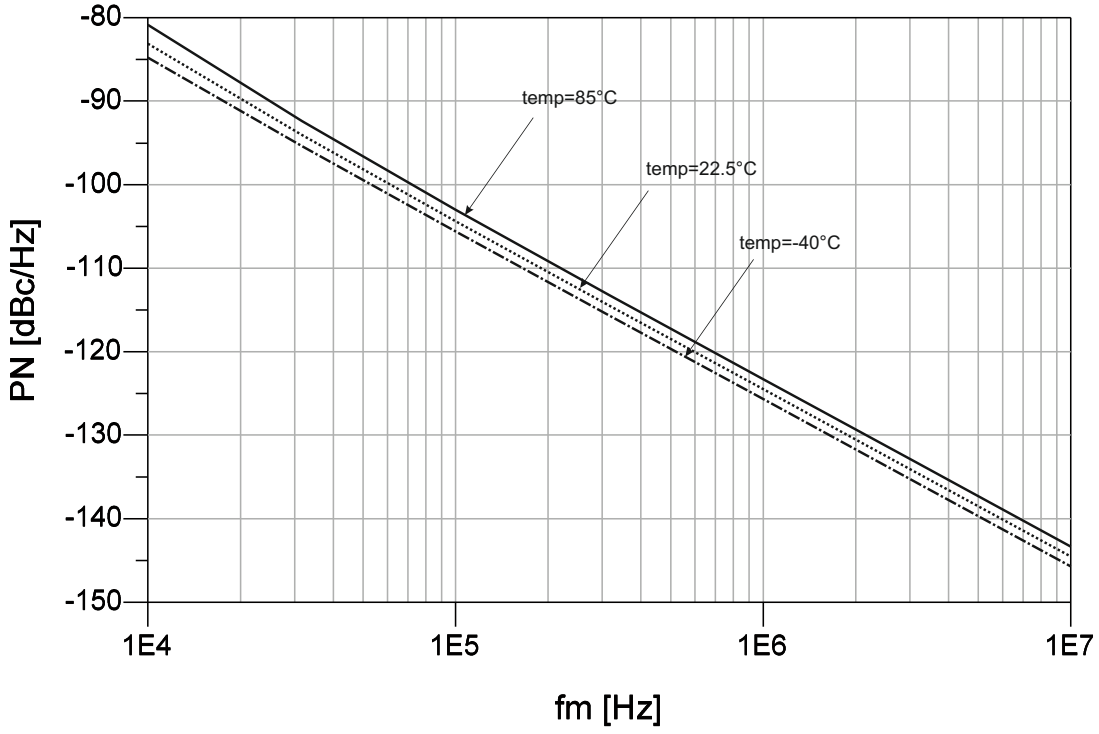


Fig. 2.18: Phase noise versus offset frequency f_m with $Vtune = 8V$

C-tail

At this point, looking at the theory chapter, 1.3.2 we could add a capacitance in parallel to the tail generator for generating an higher voltage output swing with the same current consumption. The choice of the insertion of this tail capacitor is not taken by many designer in order to do not add noise at the system. Simulations must be done before to adopt this method.
Another things to consider is the layout, if this capacitor result to be very huge, it is difficult to fit, resulting in long connections that introduce resistance and parasitic inductance.
In the figure 2.19 is depicted the value of output voltage at various values of tail capacitance.
Contrary to what has been said in the section 1.3.2, the output voltage amplitude is not bigger than the case without capacitor, thus the phase noise should not improve. Looking at the phase noise result 2.20, the result became worse adding capacitance therefore the use of this capacitance is avoided at the moment.
The issue about the tail capacitance is not simple to solve, initially is convenient to observe the amplitude of the first harmonic of current, if this module is near to the value of bias current, the system are working in a class-C, if this value is $I_{\omega_0} = 2/\pi I_{bias}$ the current waves are square and the transistor conduct for half a period. The last possibility is that

transistors enter in saturation, then the formation of the first harmonic should be worse and as consequence, the ratio will be less than the previous. Looking at the simulation, is difficult to understand the value of the first harmonic because the transistors used are very huge and their parasitic capacitance is very big, then the value that we calculate with the simulation includes also the component of the current that flows through this capacitance.

Another method to calculate the module of the first harmonic current is to use the value of the equivalent parallel resistance of the tank and divide the value of the output voltage by this resistance. We use a simulation to extract R_p and the value of this ratio is $I_{\omega_0}/I_{bias} \simeq 0.73$. This ratio is more than $2/\pi$ then we can say that the conduction angle should be less than π for each transistors of the cross couple.

Obviously the theory value is "1" but this is considering very small conduction angle [9]. The reason of this result should be that the parasitic capacitance work like a tail capacitance or that the amplitude of the output is already limited from the varactor conduction and a further increase of current causes a deterioration of the harmonic generation resulting in a worse phase noise.

Doing some simulation with half current consumption and as consequence half transis-

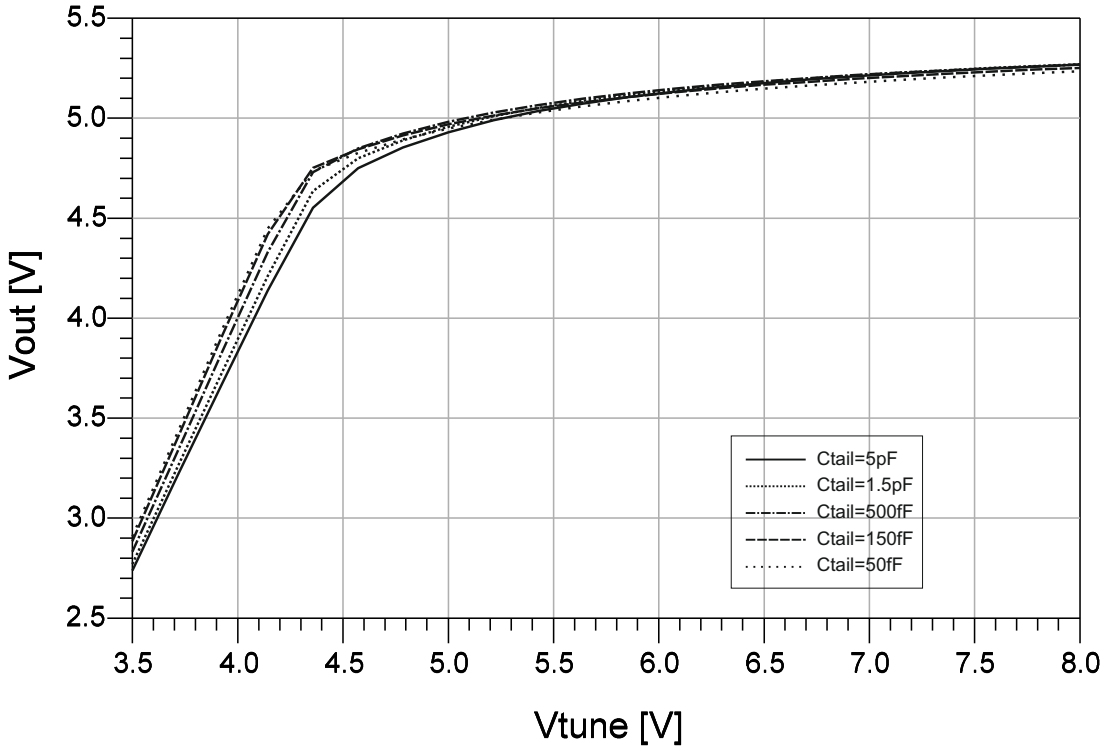


Fig. 2.19: Output voltage at various value of tail capacitance

tors size (less parasitic), we can see that the contribute of the tail capacitance is positive, i.e. less noise, at high tuning voltage, where the varactor does not give problem. In the Figure 2.21,2.22, 2.23 there are the graph of the first harmonic of the current in the

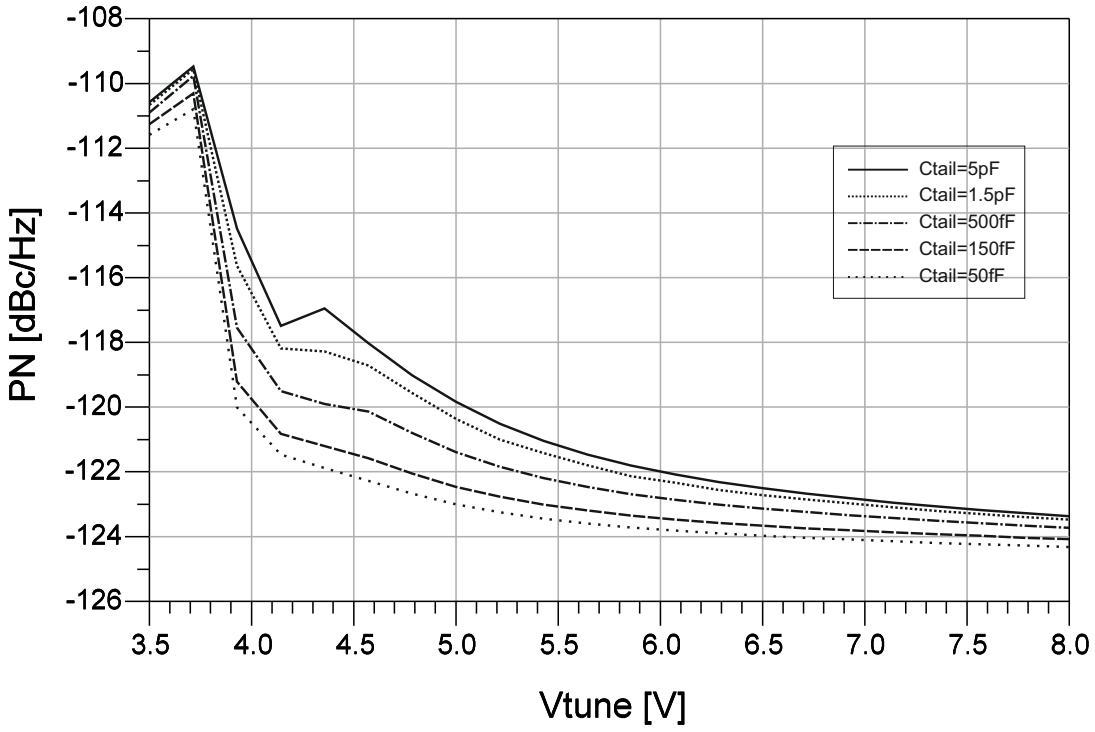


Fig. 2.20: Phase Noise at various value of tail capacitance

transistor, the output voltage of the tank and the phase noise.

In the picture 2.21 the amplitude of the first harmonic of current result higher with the use of tail capacitance and this according to the theory. This results in an increase of the amplitude but this is seen only at high value of tuning voltage, where the varactor does not affect the signal. This result in an improvement of phase noise that is seen only at high V_{tune}, 2.22. At low V_tune the phase noise is degraded and thus the solution is not adopted.

Returning on the right circuit (more bias current and bigger active devices), we can plot the harmonic of current on the transistors, however considering that the parasitic capacitance influences this currents. We can see that with the tail capacitance the value of the first harmonic of bjt current is quite equal to the case without C_{tail} but the second and the third harmonic results larger with the capacitance, therefore the resulting wave should be more degraded, Figure 2.25. We can se this result plotting the transient curves of emitter current in the bjt and looking that the current with the use of capacitance is more distorted, Figure 2.26.

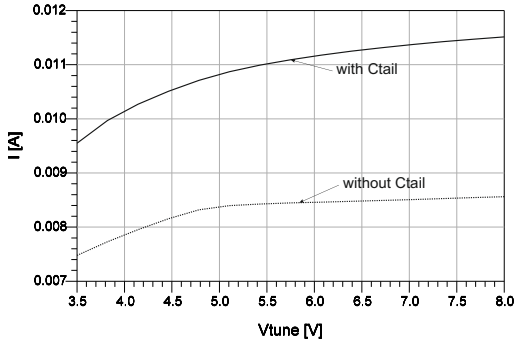


Fig. 2.21: Module first harmonic

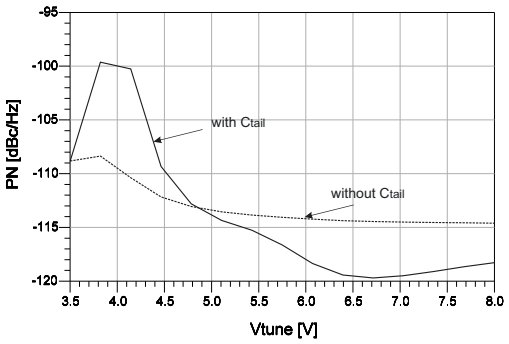


Fig. 2.22: Phase noise

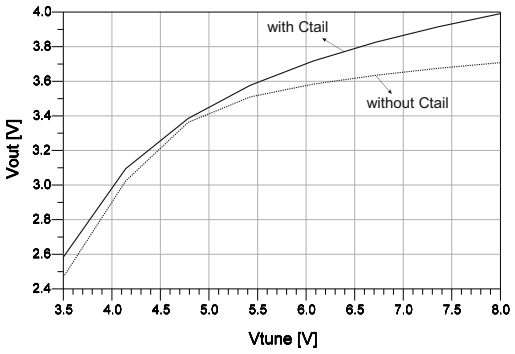


Fig. 2.23: Output voltage

Fig. 2.24: Result on VCO with less tail current and smaller transistors

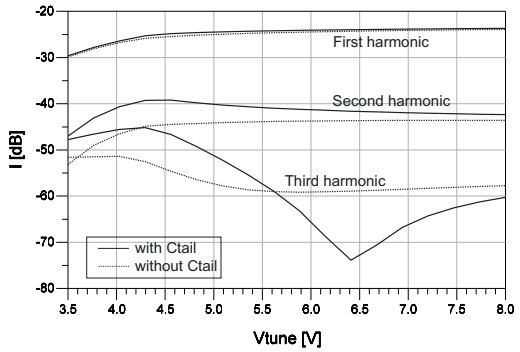


Fig. 2.25: Harmonic current with and without capacitor

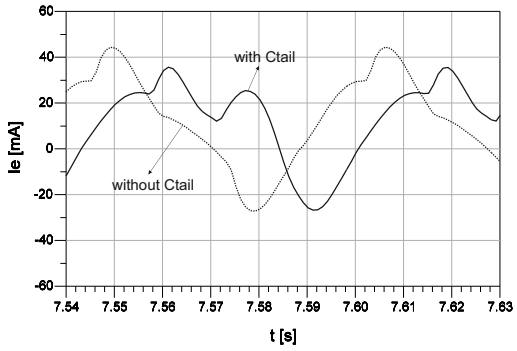


Fig. 2.26: Transient at the emitter of bjt

Output Buffer

The VCO must be linked to another block of the global system, in this case it is necessary to drive a 50 Ω equipment, therefore a buffer is added at the differential output of the oscillator in order to do not add resistance at the tank and to match a possible load with low resistance. The buffer required thus should have high input resistance and an output resistance of 50 or 100 Ω.

The buffer insert into the design is taken from the existing library, thus the document does not spend time on this. It is made by a differential pair with emitter degeneration. Over the collector there is a cascode stage and then the load, a resistor of 50 Ω. The input is ac-coupled by a capacitor.

The schematic of the used buffer is depicted in Figure 2.27.

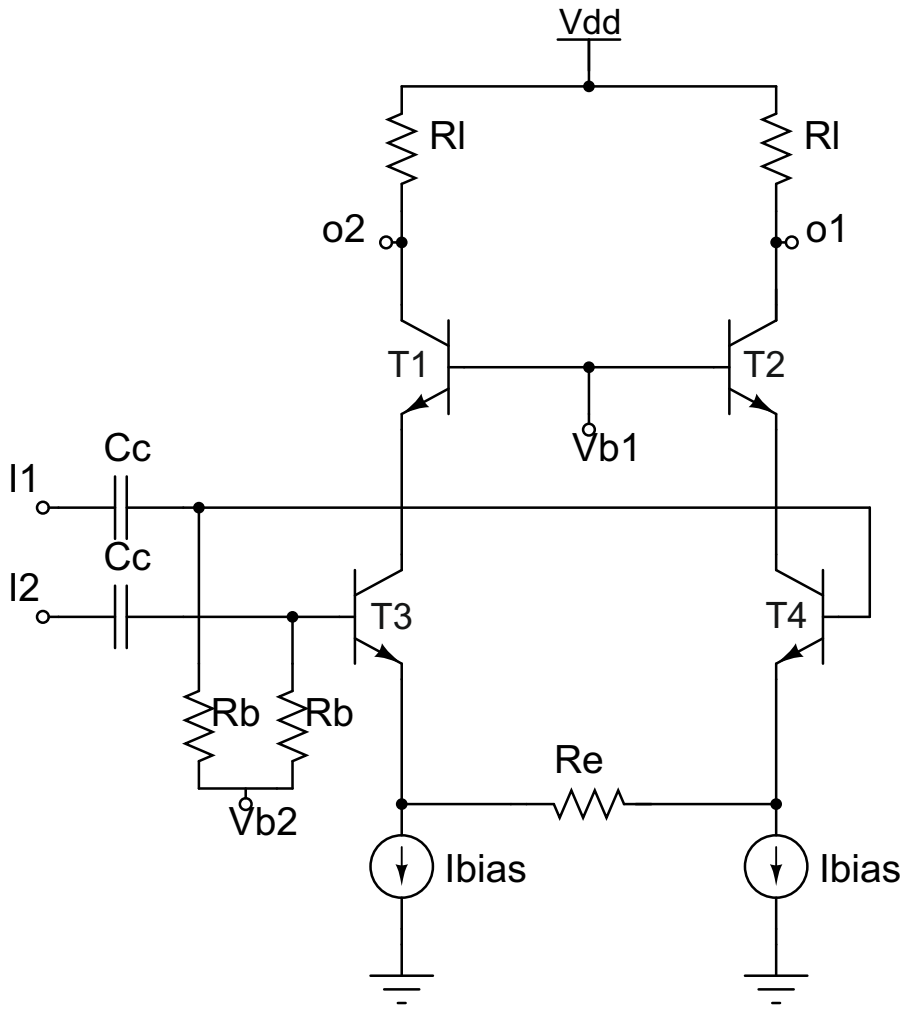


Fig. 2.27: Schematic of the buffer

In the schematic, **Rl** is the load, **Re** is the degeneration resistance, **Rb** is used to bias the transistor **T3**, **T4** of the differential pair; **T1** and **T2** are the transistors of the cascode stage and **Cc** represents the capacitor for the ac-coupling. The voltages **Vb1,Vb2** act as biasing and **Ibias** ensures the right bias current at the bjt.
Certainly the buffer add parasitic to the tank and this causes a little reduction of phase noise, we can see the result in the graphs. Furthermore, the buffer is like a capacitor divider, because his input capacitance, thus the output voltage will be less than before. The input capacitance of the emitter follower load the capacitive part of the tank resulting in a reduction of the tuning range and a lower resonance frequency. Therefore it is necessary to redesign a little bit the resonant circuit. Obviously each piece added to the VCO introduce noise and parasitics, and causes a reduction of performance. Below we can see the results after the insertion of buffer, 2.28, 2.29, 2.30.

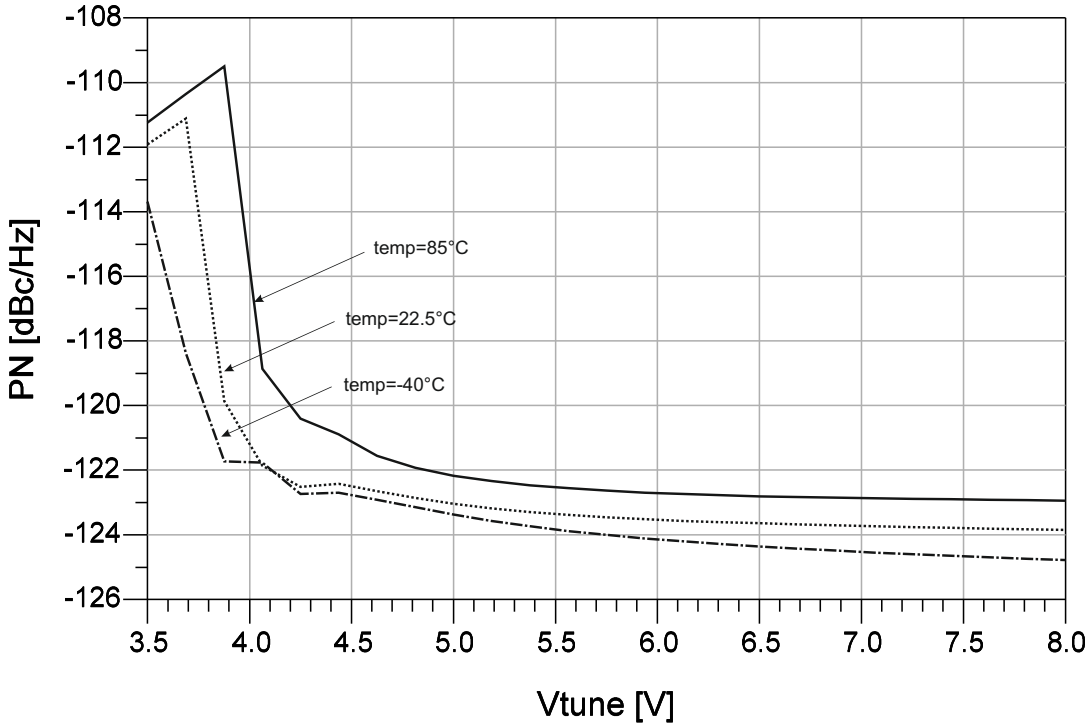


Fig. 2.28: Phase noise at 1 MHz offset versus tuning voltage Vtune varying temperature after buffer

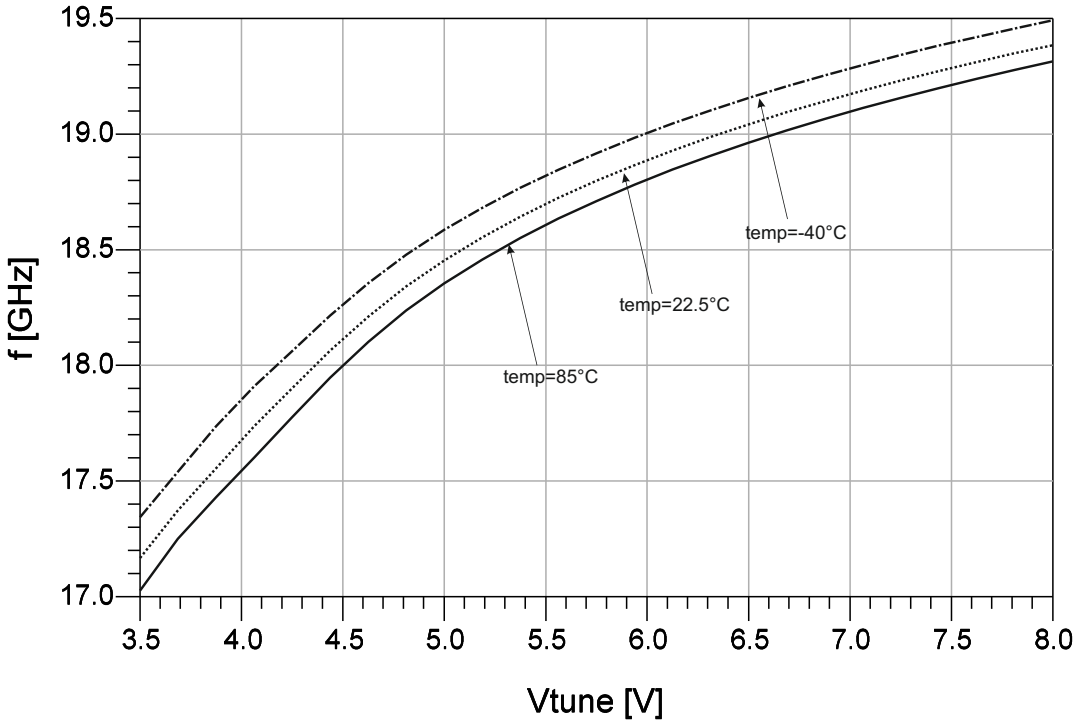


Fig. 2.29: Output frequency versus tuning voltage Vtune varying temperature after buffer

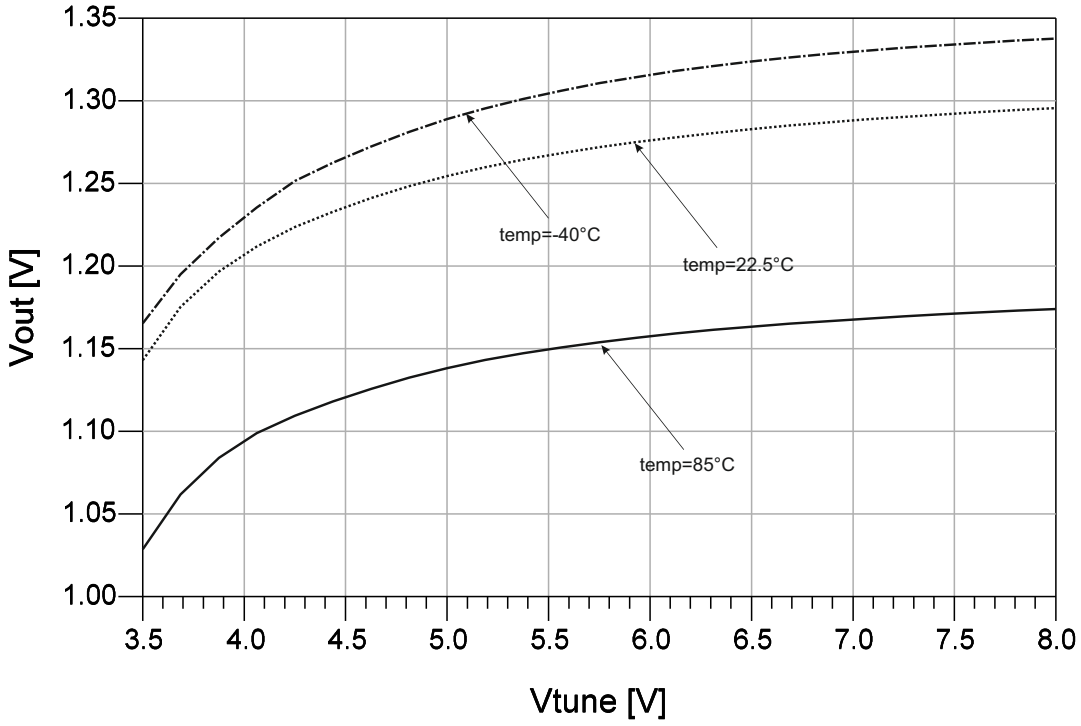


Fig. 2.30: Differential output voltage versus tuning voltage Vtune varying temperature after buffer

2.3.4 Issues and other solution

This circuit, as we can see in the results, present two problems:

- At low tuning voltage the the phase noise results degrade due to the varactor;
- The necessary Vtune is from 3.6 to 8 volt and the voltage for the entire system should be (0-3.3V);

For the first thing is difficult to improve the performance, we should decrease the voltage swing but this affect the phase noise so it is not a solution. In the second case we can have two mainly solution:

- **decoupling the varactor with a RC filter;**
- **using a transformer to decouple the varactor from DC voltage;**

The first solution give good results decoupling the varactor with ideal capacitor, in Figure 2.31 we can see the schematic. The problem appears when the real mimcaps are inserted; looking at the schematic, the capacitive part of the tank is made by the series capacitance of the 3 contributors: C_{varac}, C_{coup}, C_{coup}, and the tuning capacitance is given only by the capacitance of the varactor. For this reason the C_{coup} should be bigger than C_{varac} and this one must have larger value compared to the previous design.
If the mimcaps are too huge, their parasitic capacitance and resistance with substrate influence a lot the quality factor of the tank resulting in a big loss in phase noise. Another disadvantage is the layout: huge capacitors and huge varactor complicate the placements of the components, the consequence is longer connections that vary the inductive component (change the resonance frequency) and introduce more resistance, thus decrement of quality factor. For all these reason this solution is dismissed.
The other solution, that is using a transformer to decoupled the varactor is explained in the section 2.5.
Now we will look at the figure of merit of the described VCO. Using the formula given:

- $FOM = \mathcal{L}(f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right)$
- $FOM_T = \mathcal{L}(f_m) - 20\log\left(\frac{f_0}{f_m}\frac{FTR}{10}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right)$

Here there are the results in FOM, Table 2.3.

Tab. 2.3: Figure of merit results

FOM	**-192.5 dBc/Hz**
FOM_T	**-194.5 dBc/Hz**

The figure of merit represents the best value of phase noise at 1 MHZ offset frequency over

the entire tuning range, and it is calculated without the insertion of the buffer. Certainly after layout operation this value will be reduced.
Hittite VCO2 presented in the introduction, [22], [21], have a figure of merit of $FOM = -181$ dBc/Hz, and $FOM_T = -179$ dBc/Hz for the HMC398QS16G, and $FOM = -172$ dBc/Hz, and $FOM_T = -175$ dBc/Hz for the HMC738LP4. Similar result with the SiGe bipolar technology are presented in [19], where the result on phase noise is -108 dBc/Hz at 100 KHz offset with a center frequency of 5 GHz that correspond approximately at a FOM of -182. Another results with the SiGe bipolar technology is made by IBM [32], the resulting phase noise is approximately -100 dBc/Hz at 17 GHz.
Other results on VCO are in [27]. Sensitivity at voltage supply variation is another important parameter to extract. The simulation give $S = 220MHz/V$ that is a value quite low.

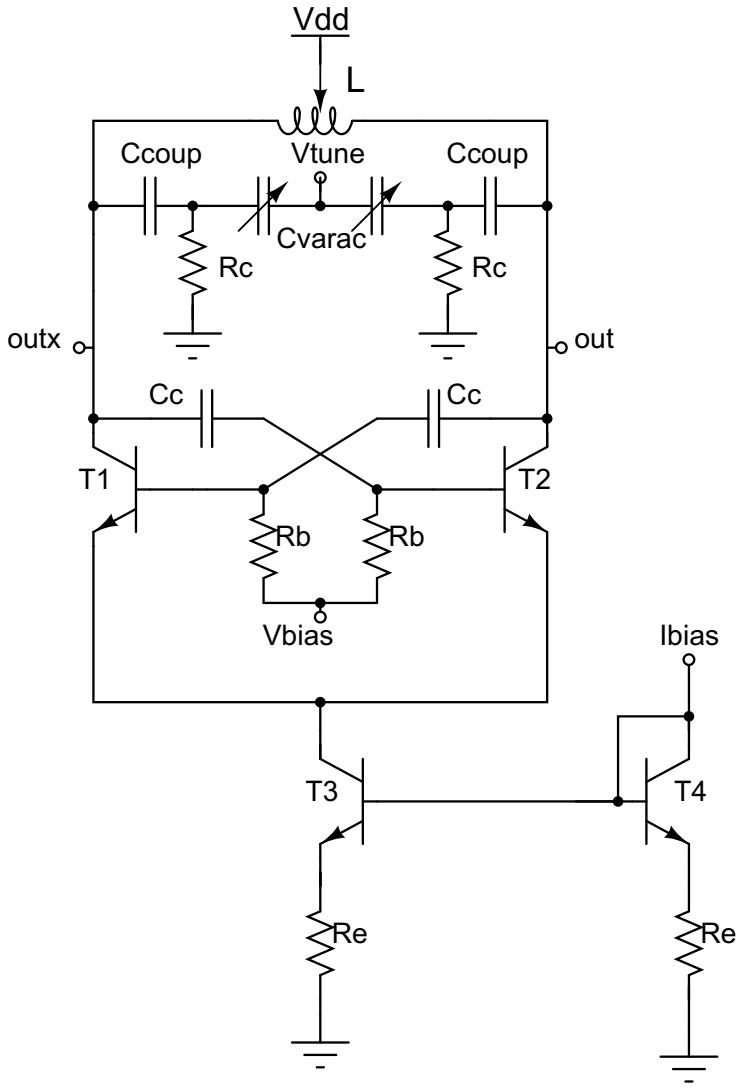


Fig. 2.31: Schematic of VCO with AC coupled varactor

2.4 Tranformer design

After the first consideration on the VCO design with a resonant element made by a coil and a varactor biased at supply voltage that is 3.3 V, we concluded that due to the fact that the varactor should not arrive near conduction zone causing a degradation of the Q, it is necessary to decouple this element from DC supply voltage and we chose to use a transformer to do this.
The primary of the transformer will be connected to the varactor biased at ground and forming the tank element, the secondary will be biased at 3.3 V and connected to the collector of the transistors, this topology will be discussed in the next section.
As in the coil design, the tranformer should have an high quality factor in order to obtain good phase noise result, therefore is necessary to chose a way to make this essential component following these point:

- low resistance of the windings;
- low capacitive contribution in order not to affect the tuning frequency range;
- layout placement;
- right value of inductance;

The resistance of the windings is directly linked to the quality factor, the solution are to use the same tricks as in the coil design, the width of the strips should be large but not so much because the skin effect, furthermore too wide strips generate a lot of parasitic capacitance that reduces the tuning range.
Another fundamental thing is the layout. The varactor must be placed near the primary of the transformer in order not to add inductive components and resistance that affect the Q, furthermore the transistor of the differential pair should be placed near the secondary for the same reason.
Low resistance is obtained making the coil with the least resistive layer of the available technology, the same top layer of the coil used in the previous VCO design. The schematic is depicted in Figure 2.32. The idea is to make the transformer with one winding for the

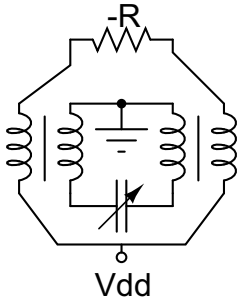


Fig. 2.32: Schematic representation of transformer with tank

primary and one for the secondary (the value of inductance is quite small) and to use the same layer for both, that is the less resistive. In order to place the varactor near the primary and avoid long connection, we use the inner coil for the primary and if possible we connect the varactor into the transformer like depicted in the schematic 2.32. At the secondary is connected the negative resistance or the differential-cross couple. In this manner bridge that causes huge resistive contribute are avoid.
With this solution, the coupling between the windings is less than the case with the vertical placements, overlying strips. We will see that this low coupling factor cause the possibility of the generation of a double resonance in the systems, this happens because there are two resonant elements, tank and the element composed by the secondary of the transformer and the capacitive contribute of the transistors added at the capacitance that is linked between the base of one transistors and the collector of the other transistors like depicted in the Figure 2.14. If the coupling factor between the two circuit is low, they try to be quite independent and the simulation shows the formation of a double resonance, [10], [16], [7], [8].
The first transformer designed and optimized is depicted in Figure 2.33.

In order to avoid the double resonance phenomena, the thing to do is to increase the

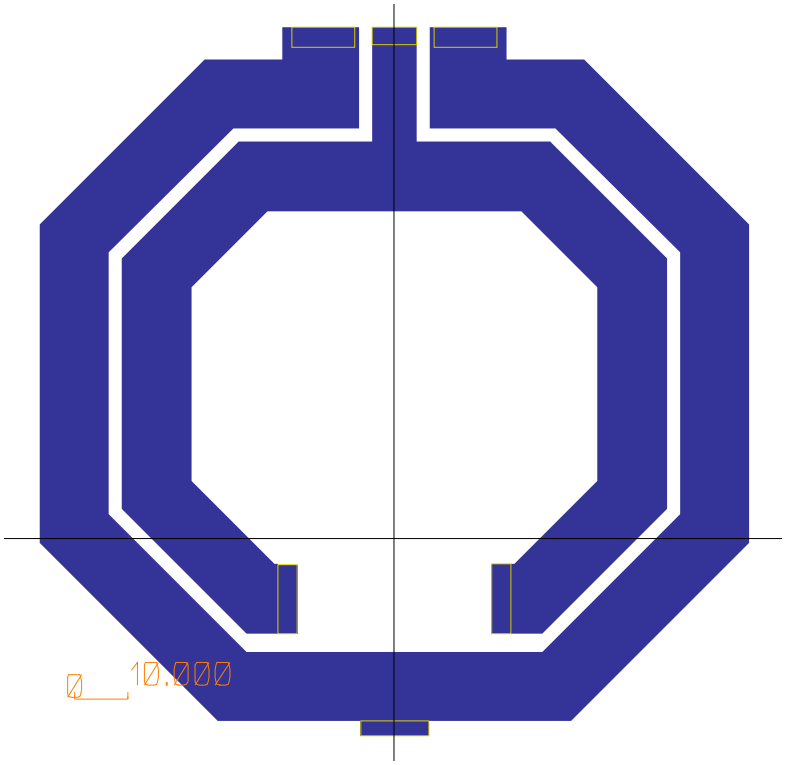


Fig. 2.33: Layout of the transformer

coupling factor of the transformer in order to have more dependence between tank and bjt part of the circuit. The best solution taken without to change dramatically the topology of the transformer is to make a coil in parallel at the primary but make with the layer below. In this case the resistance of the primary is not bigger because the more resistive

path is in parallel with a less resistive path, furthermore the other layer is overlying to the secondary to obtain a better result of the **k**.
In Figure 2.34 is depicted the layout of the final transformer.

In the graph 2.35 there is the coupling factor of the transformer with and without the

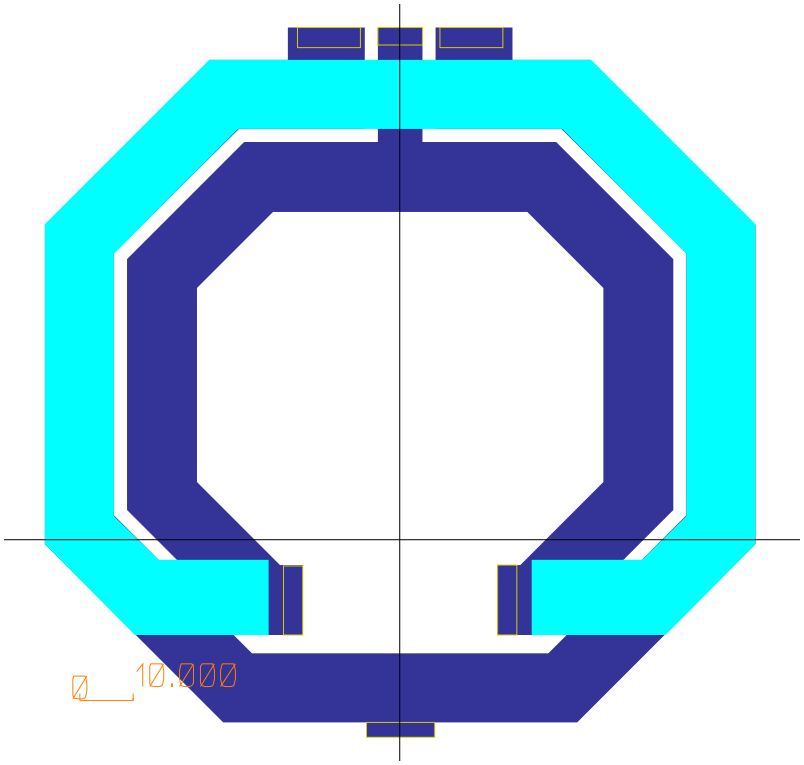


Fig. 2.34: Layout of the final transformer

parallel layer. We can see that with the "vertical coupling" **k** grows of 0.2 and this is very important to avoid the possibility of double resonance. Actually the insertion of the second layer should affect a little bit the quality factor because the resistance decrease but also the inductance decrease, thus we will chose a good compromise between the reduction of the quality factor and the increment of the coupling factor.

The simulation results about the designed transformer are depicted in the Figure 2.36, 2.37, 2.38, 2.39, where are shown respectively the resistance of primary and secondary coil, these values are defined as the real part of the impedance seen by a port with a S-parameter simulation.
In Figure 2.37 there are the values of the inductance, these value should be calculated at low frequencies when the capacitive component doesn't contribute on the imaginary part of the impedance. he quality factor of the primary and secondary coil of the transformer are then extracted using the expression $Q = \frac{Im[Z(j\omega)]}{Re[Z(j\omega)]}$ and the graph depicted in Figure 2.38 represents the two value; obviously the primary must have a better quality factor because added at the varactor represent the resonant element of the systems.
In the Graph 2.39 is represented the quality factor of the network seen by the transistors, that is the quality factor taking from the pin of the S-port at the secondary of the

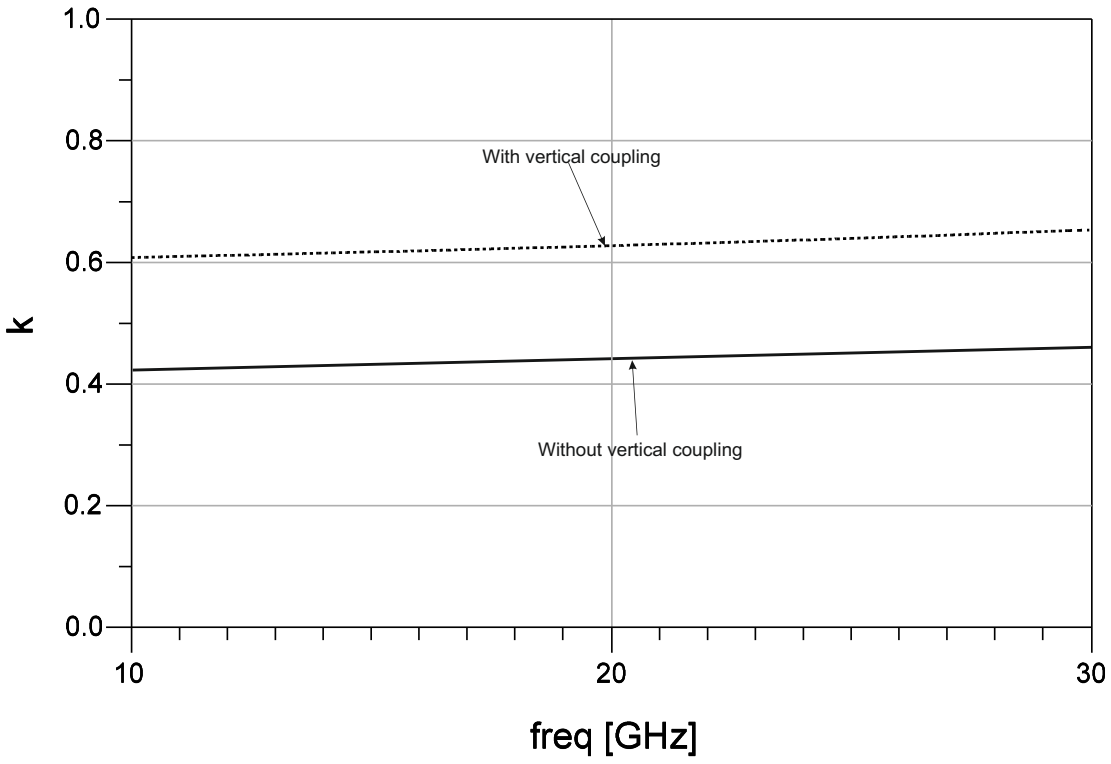


Fig. 2.35: Coupling factor, defined as $k = \sqrt{\frac{Im(Z(1,2))Im(Z(2,1))}{Im(Z(1,1))Im(Z(2,2))}}$

transformer; the value is plotted changing the tuning voltage and it is possible to see the degradation of the quality factor for low V_{tune}.
In he next section the VCO with this transformer forming the resonant network is analysed.

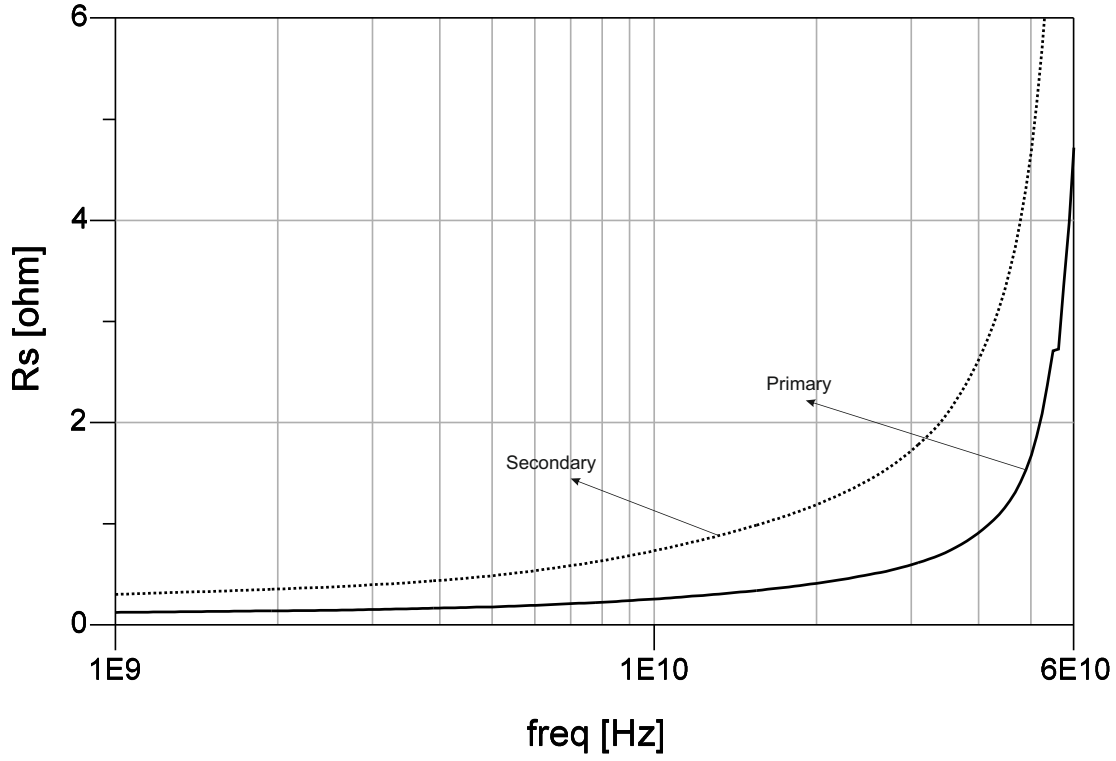


Fig. 2.36: Resistance of the primary and secondary, $R = Re[Z(j\omega)]$

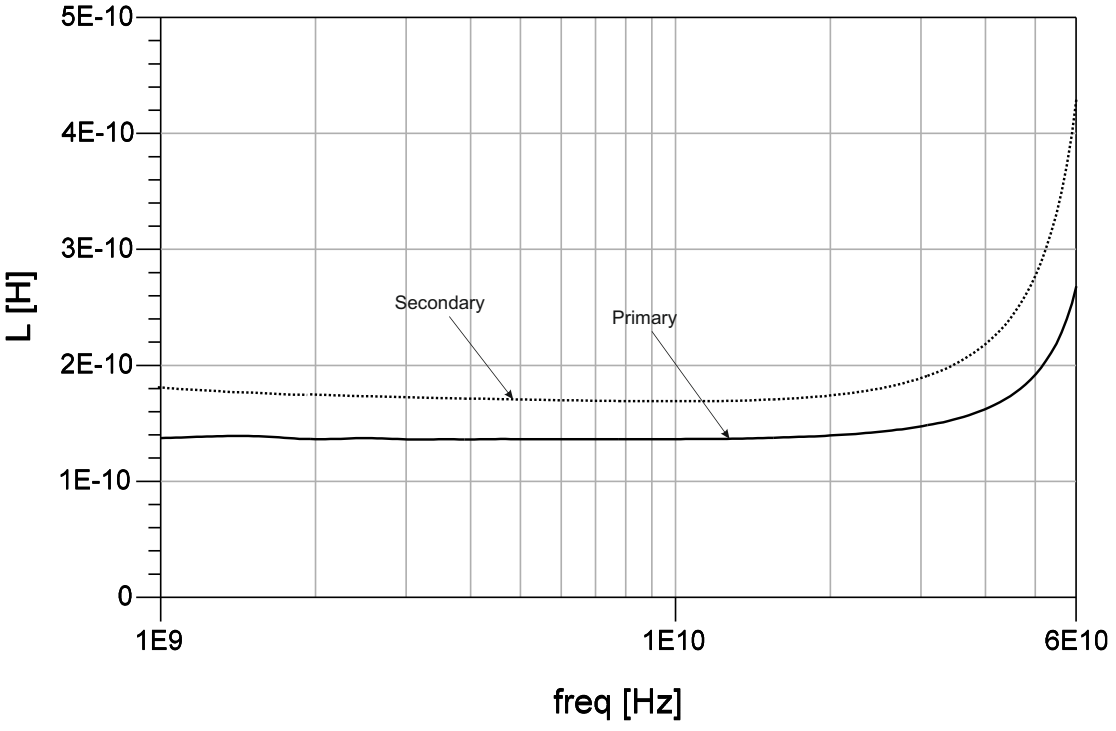


Fig. 2.37: Inductance of the primary and secondary, $L = \frac{Im[Z(j\omega)]}{2\pi\omega}$

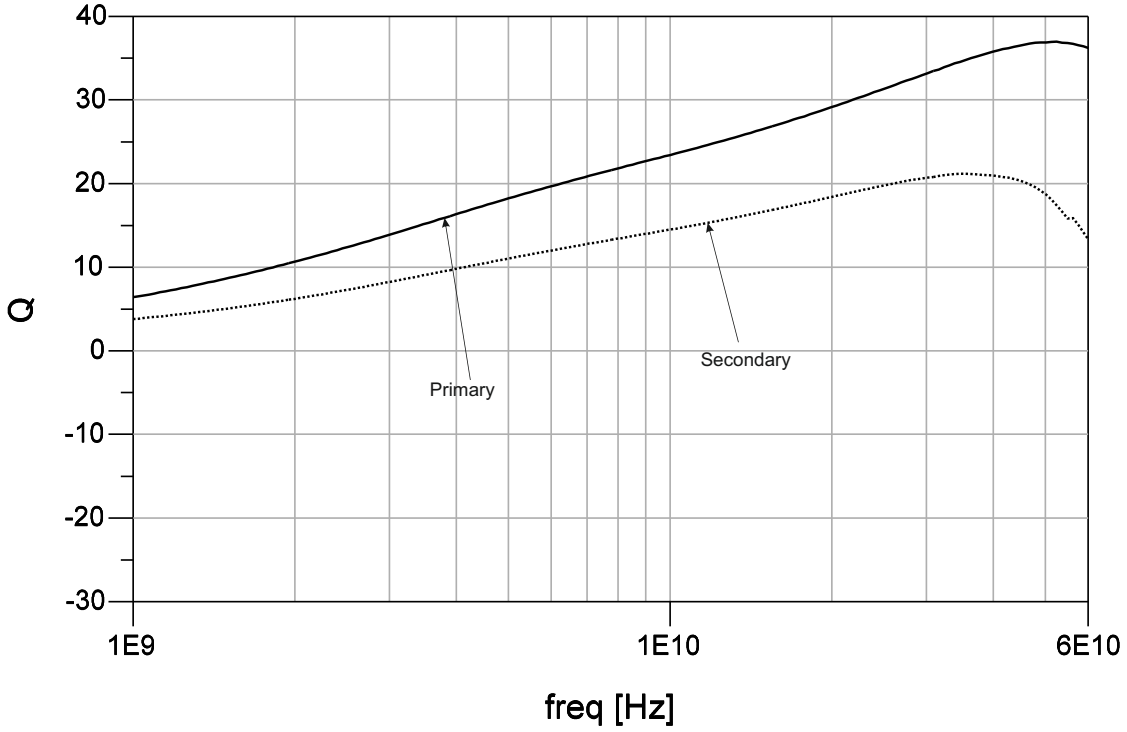


Fig. 2.38: Quality factor of the primary and secondary, $Q = \frac{Im[Z(j\omega)]}{Re[Z(j\omega)]}$

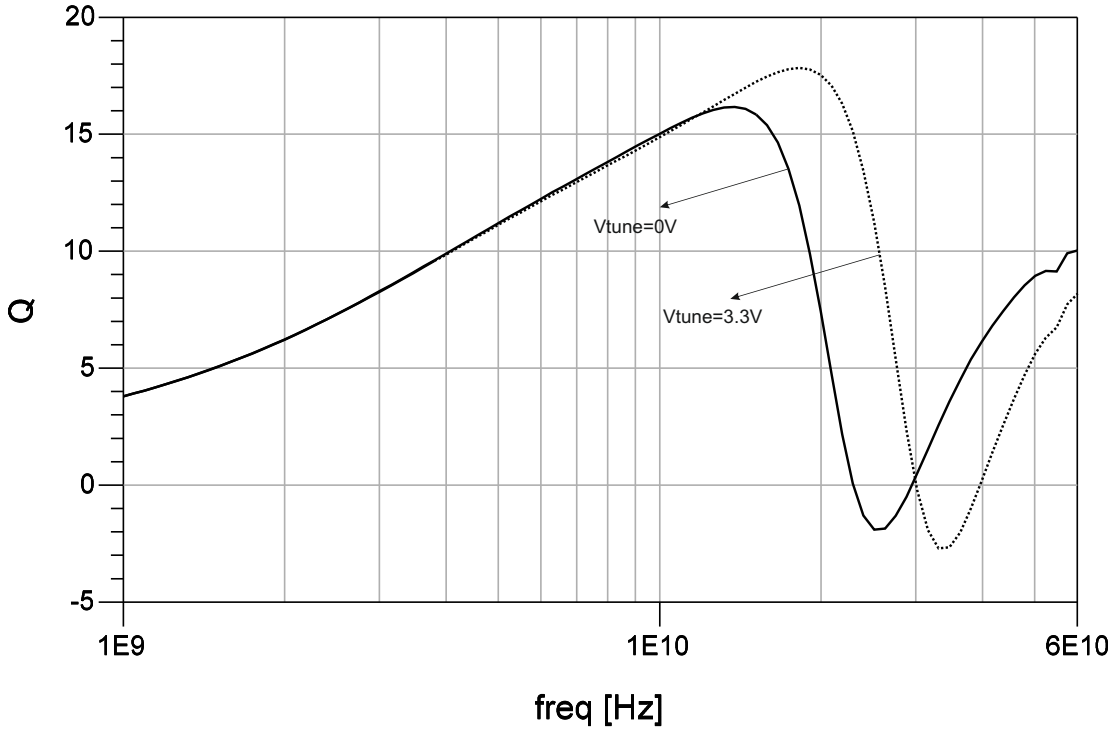


Fig. 2.39: Quality factor of the entire tank, including the varactor, $Q = \frac{Im[Z(j\omega)]}{Re[Z(j\omega)]}$

2.5 VCO with transformer decoupled varactor

In this section there is the presentation of the solution with a transformer decoupling the varactor from the DC component. In the previous design, it has been shown that the varcator limits a lot the phase noise results when he is biased near the conduction zone, even because in this zone the amplitude voltage across the tank is reduced, even because the quality factor of the varactor is low in this zone.
The solution proposed in the previous part, decouple the varactor with a RC filter doesn't present good results, because the mim-capacitor should be big enough to do not affect the tuning range and this cause less possibility of placement in the layout and increment of parasitic components.
Using the transformer described in the previous section and depicted in Figure 2.34, the varactor diode is biased with the anode at 0 Volt and the cathode at the Vtune voltage. **With this configuration it is possible to use a tuning voltage V_{tune} from 0 to 3.3 V instead of from 3.3 to 8 Volt.** This is a big advantage because it is not necessary to add other voltage supply at the circuit unlike the solution proposed by Hittite [20].
The quality factor of the transformer results to be a little bit less than the coil, this is due to more losses in the transformer, like not ideal coupling factor and less quality factor of the single windings. The global results in phase noise are however good, similar at the result presented in the previous VCO design.
The biasing part is the same of the previous circuit design, then the value are reported in the Table 2.4, thus also the power consumption is the same. For the description of the biasing choices the description is reported in the section 2.3.
The schematic of the circuit is depicted in Figure 2.40 where it is possible to see the decouple of the varactor.
The result if phase noise and in tuning range and output voltage swing are depicted in

Tab. 2.4: VCO transformer parameter

V_{dd}	3.3 V
V_{tune}	0-3.3 V
V_{bias}	2.5 V
I_{bias}	1 mA
I_{supply}	20 mA
P_{DC}	66 mW

the Figures 2.41, 2.42, 2.43, 2.44.

The results are similar to the design without the transformer, this signify that the lower quality factor of the primary coil doesn't affect the phase noise. Obviously the advantage is the use of a tuning voltage up to 3.3 V instead of 8 V. The issues of the degrade of phase noise at V_{tune} near to 0 V due to the conduction of the varactor remain but with less effect than before, this is due to the transformer: the coupling factor is obviously less

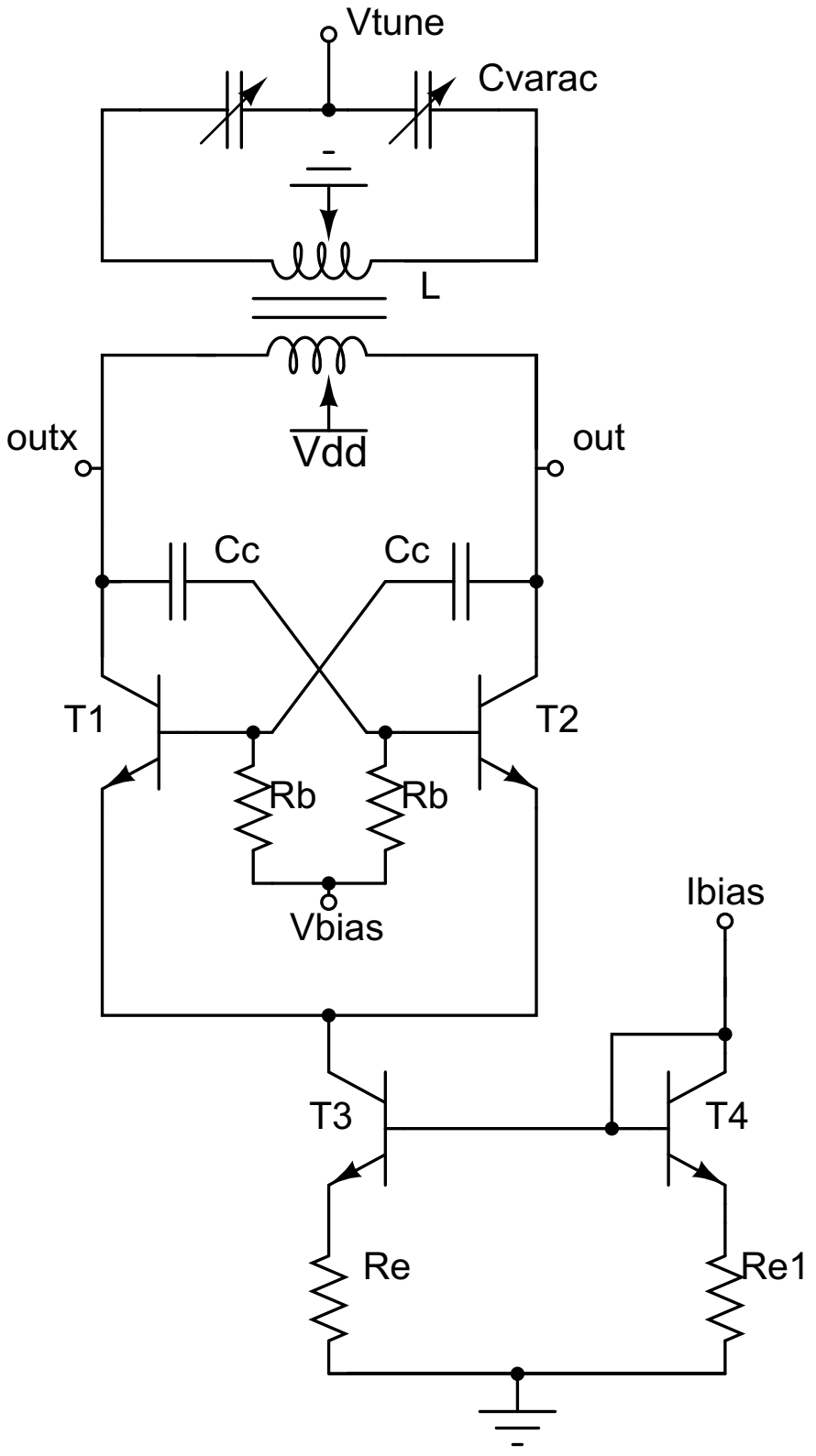


Fig. 2.40: Shematic of VCO with transformer decoupling varactor

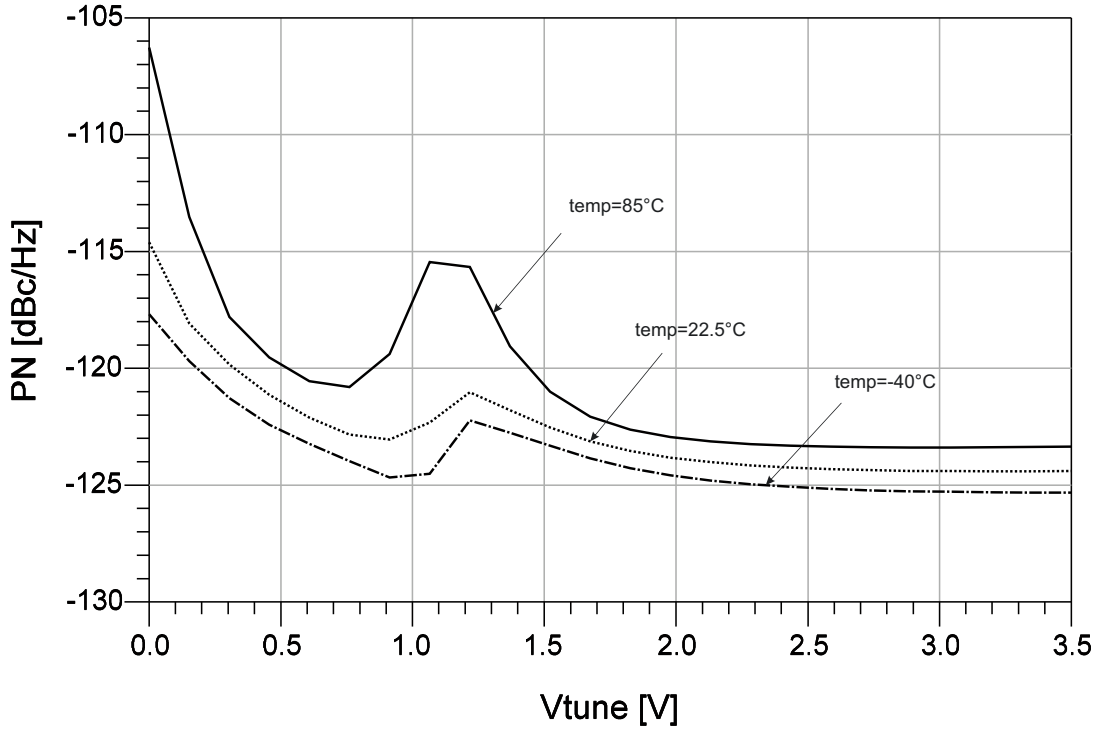


Fig. 2.41: Phase noise at 1 MHz offset versus tuning voltage Vtune varying temperature

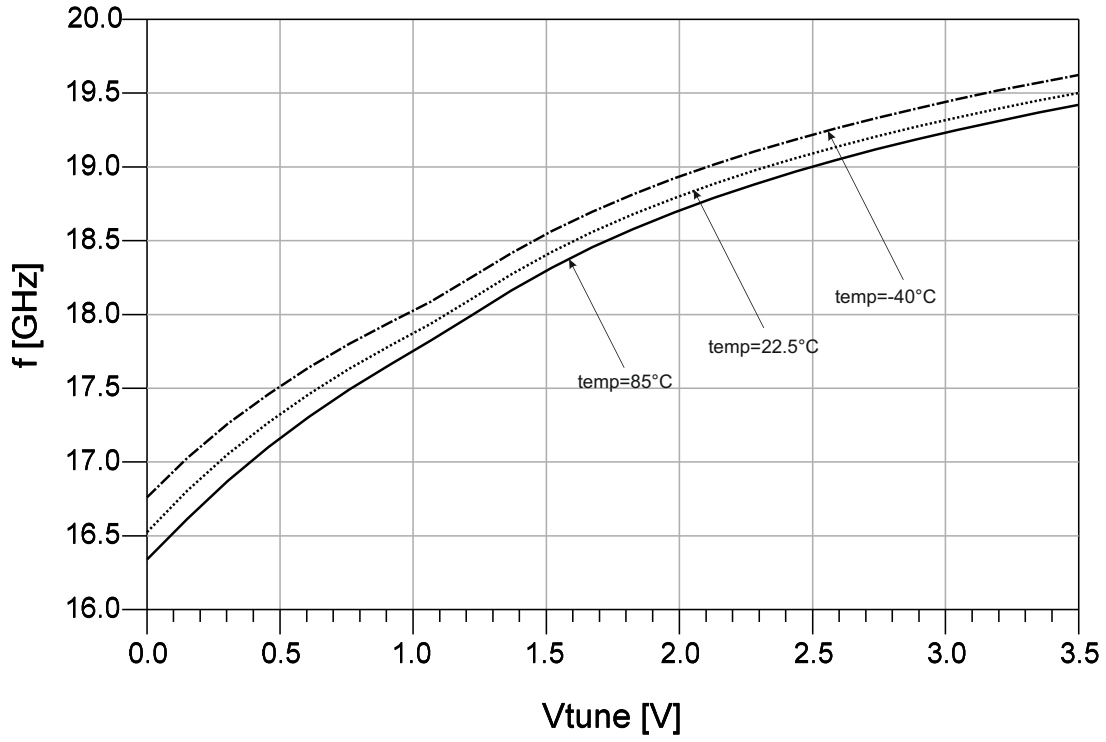


Fig. 2.42: Output frequency versus tuning voltage Vtune varying temperature

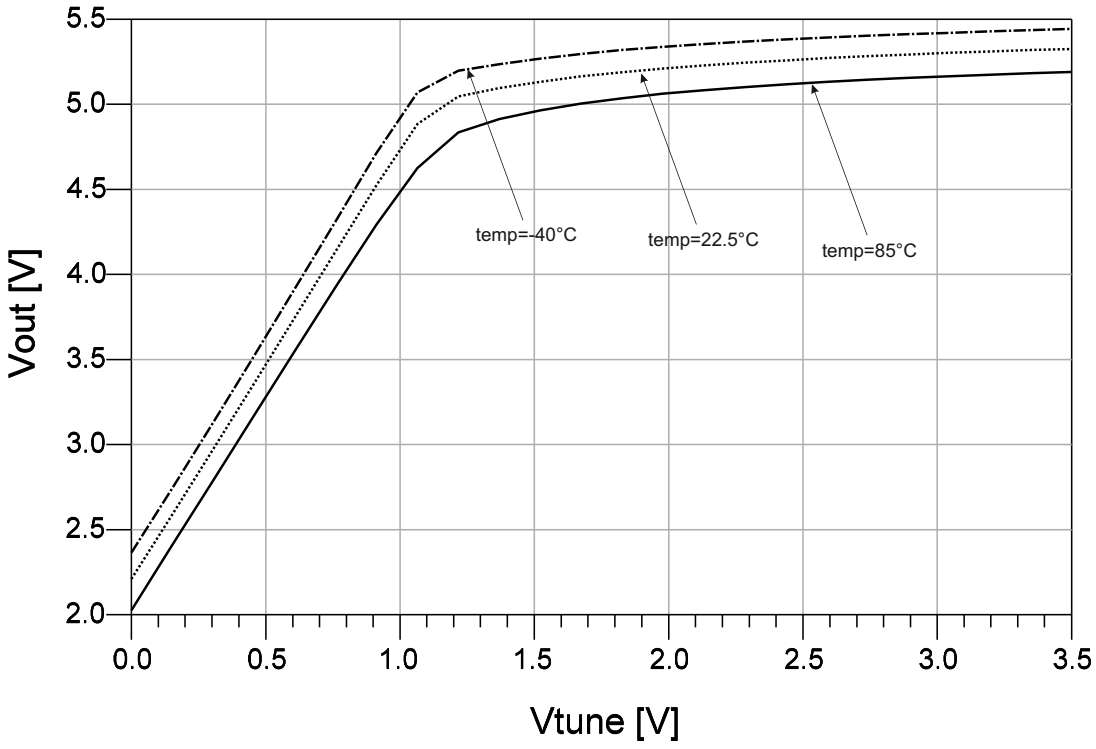


Fig. 2.43: Output voltage versus tuning voltage Vtune varying temperature

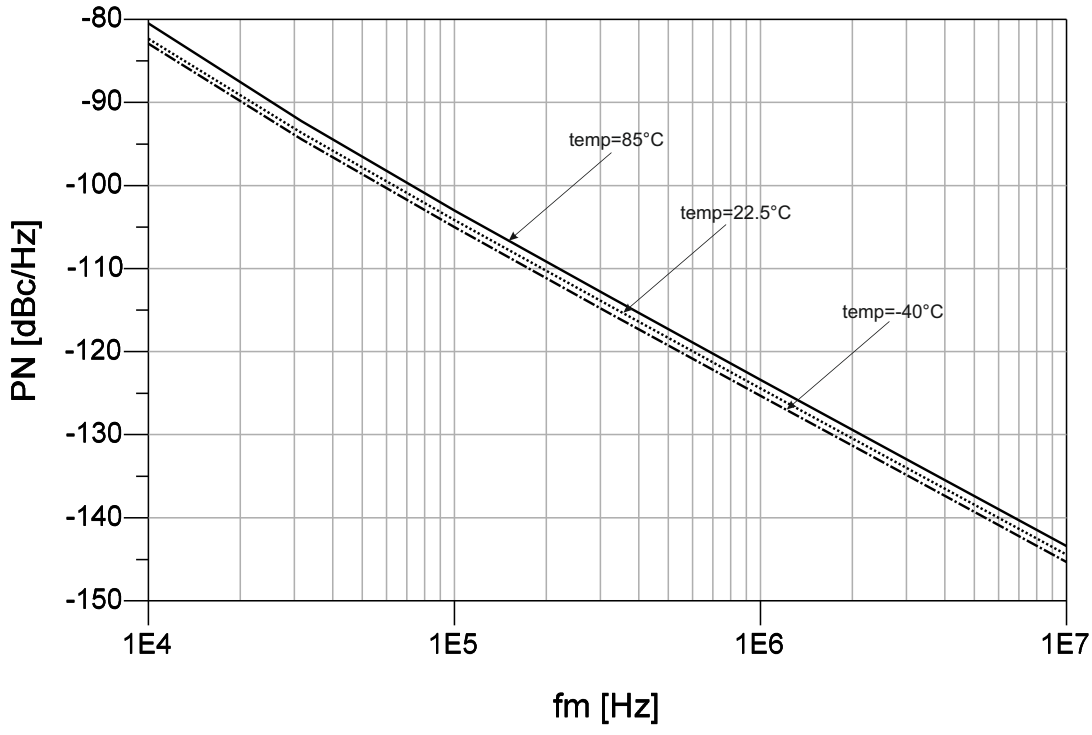


Fig. 2.44: Phase noise versus offset frequency f_m with $Vtune = 3.3V$

than one, hence even if the ratio between the number of windings is 1:1 the ratio between the voltage amplitude resulting from simulation is $\frac{V_2}{V_1} = 1.3$, where V_2 is the magnitude of the voltage at the secondary of the transformer and V_1 is the magnitude of voltage at the primary (tank).
The voltage at the primary is the same that the voltage across the varactor, hence the varactor limits less the voltage amplitude of the tank comparing with the case of the coil where the voltage across the varactor has the same amplitude that the output voltage. This should be an explanation of the reason that even if the quality factor of the entire resonant circuit is less, the phase noise is not worse rather it has been seen a little improvement.

Output Buffer

As in the previous description of the VCO design, in order to couple the output of the VCO with another system, a buffer is insert. The buffer has the same characteristics of the one described in the VCO coil section, thus the features are inserted in the section 2.3.3.
In the Figures 2.45, 2.47, 2.46 there are the results considering also the insertion of this buffer. It has been seen that the output voltage is reduced due to the capacitor divider formed by the AC coupling of the buffer and the capacitance in the input stage of the buffer. The results in phase noise are similar, this means that it doesn't affect significantly the quality factor of the tank. The frequency range results a little bit reduced due to the additive capacitance.
Looking at the figure of merit, it is similar with the one of the previous circuit, Table 2.5. These are the maximum performance results without the consideration of the layout that are in the next chapter.

Tab. 2.5: Figure of merit results

FOM	**-192.3 dBc/Hz**
FOM_T	**-195 dbc/Hz**

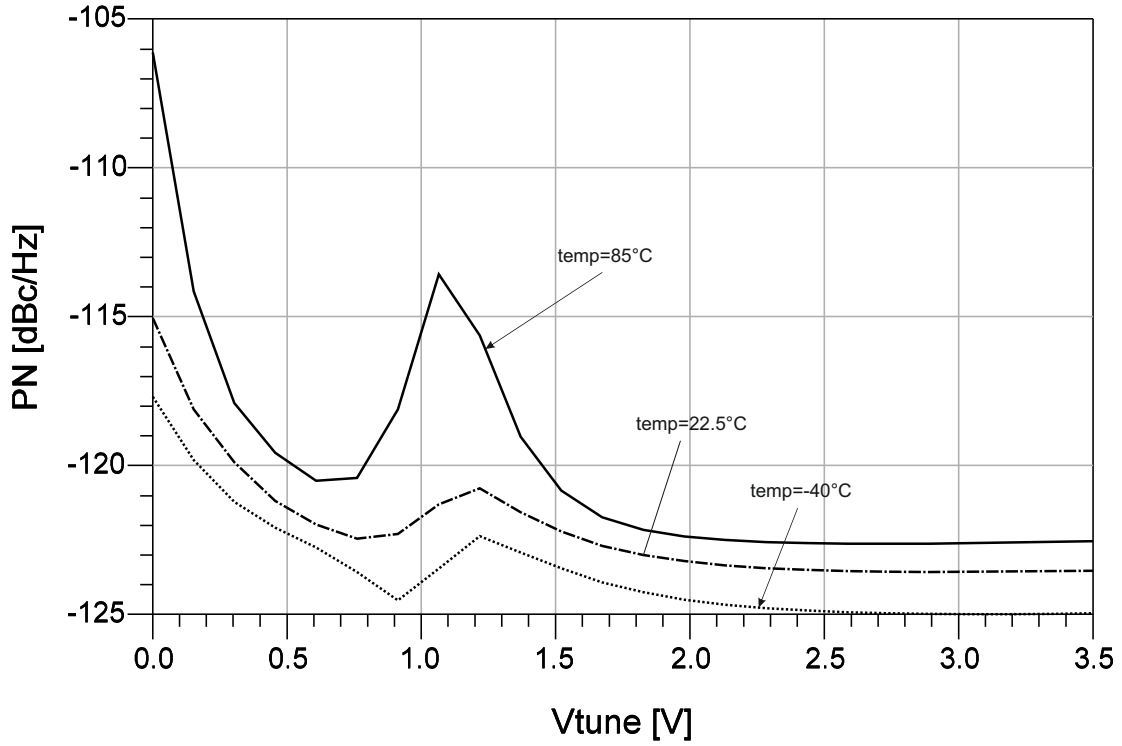


Fig. 2.45: Phase noise at 1 MHz offset versus tuning voltage Vtune varying temperature with the buffer

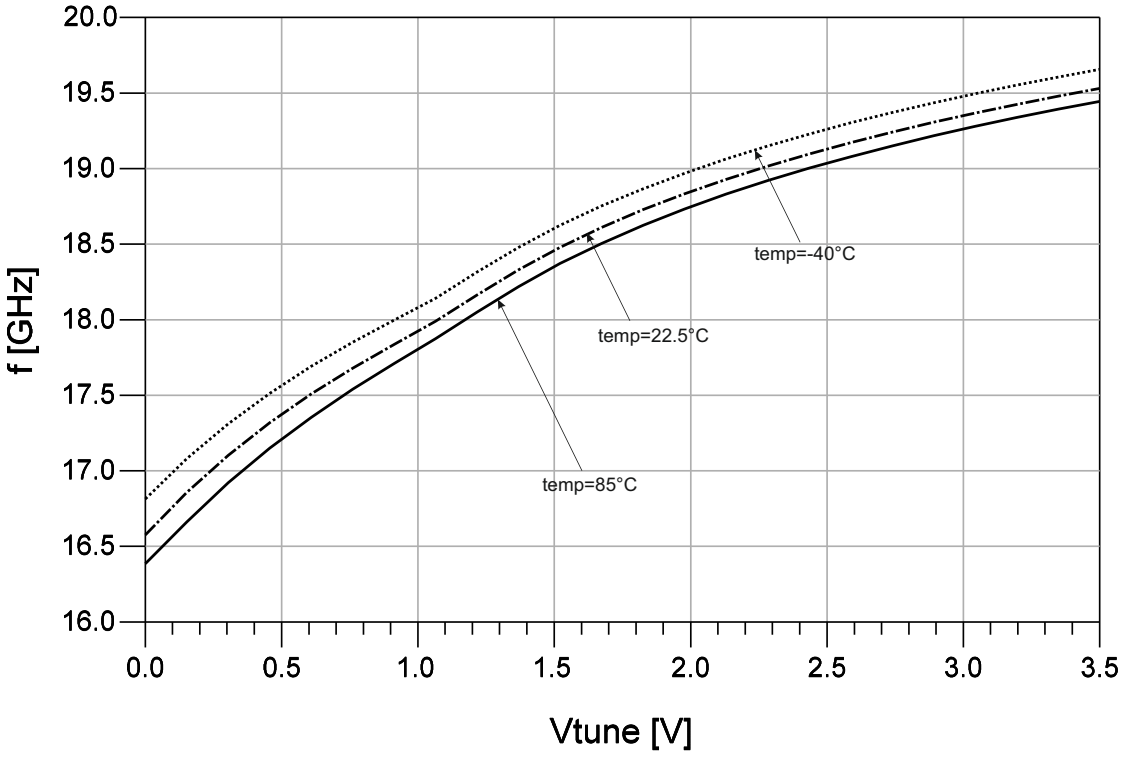


Fig. 2.46: Output frequency versus tuning voltage Vtune varying temperature with the buffer

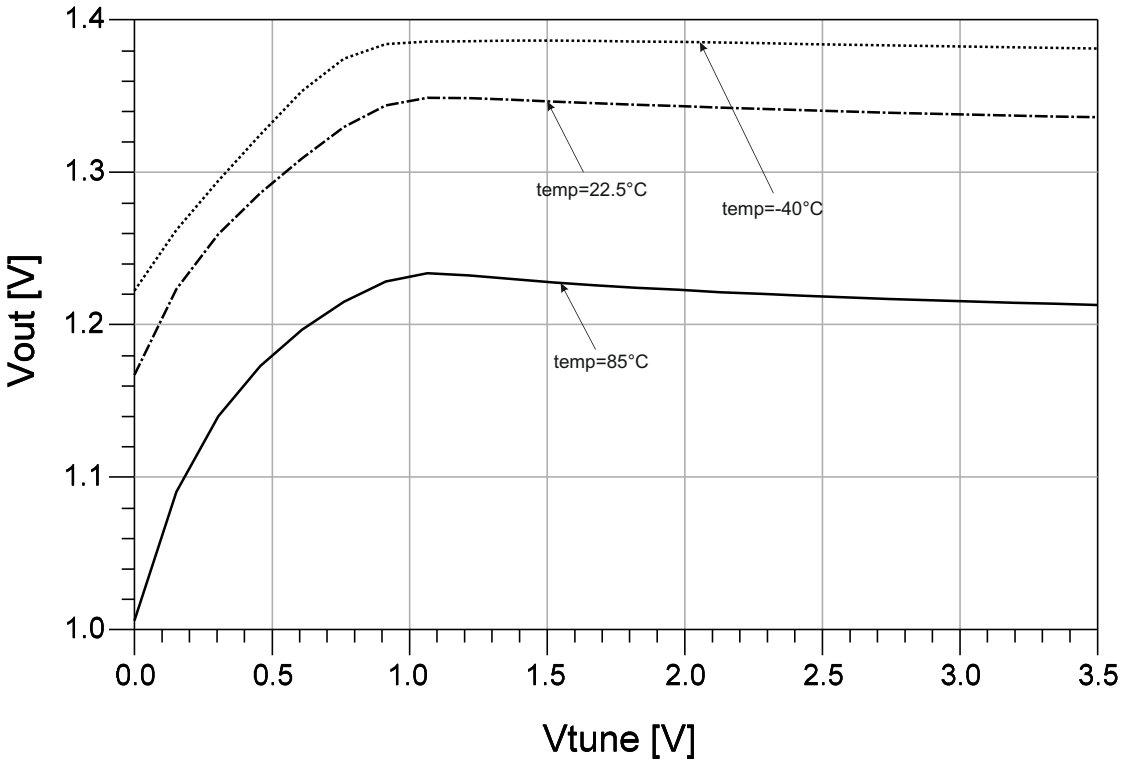


Fig. 2.47: Output voltage versus tuning voltage Vtune varying temperature with the buffer

Chapter 3

Layout

Layout operation is the most important thing of this kind of design, this because at high frequency, the contribute of the parasitics becomes very significant, [28]. There are three different parasitics and loss contributes in the circuits working at high frequencies:

- parasitic capacitance due to the coupling between connections that cause tuning range reduction;
- inductive component of the connection that in this case cause reduction of tuning range and frequency shifting;
- the resistive part of the connection is very high due to the effect at high frequency, this cause degradation of the quality factor;

Therefore the first important thing to do at the begin of the layout is to think about the placement of the devices in order to occupy less place as possible resulting in a compact layout.
In this case, the most important part of the VCO is the tank, or the resonant element, the varactor and the inductor (coil or transformer) should be very near in order to reduce at the minimum the resistances that affect the quality factor and the parasitic inductances of the connections that affect the tuning range. Also the transistors responsible of the current injected in the tank should be near the resonant element because the resistive path between BJT and tank degrade the Q.
If the varactor is too huge, it is difficult to fit it between the coil and the transistor in order to have short connection. On the other hand, reducing the dimension of the varactor cause the reduction of the tuning range, hence the first design should be modify to obtain less as possible parasitic contribution but anyway maintain the sufficient tuning range.
A redesign operation is necessary in order to follow these rule and avoid a substantial degradation of the quality factor of the circuit. Below there is the sequence of the operation done:

1. Choice of the disposition of the components in order to have short connection with low resistance mainly near the tank.

2. Extraction of the parasitics.

3. Simulations of the connections with electromagnetic simulators, extraction of equivalent resistance at the frequency of work and equivalent inductance.

4. Insertion of all the parasitic in the schematic and re−simulation of the performances.

5. Eventually redesign if the parasitics deviate too much the specification of the project.

These operation are repeated several time till the results meet the specifications.
The simulation of the connections are not very easy, for instance the transistor has not only one pin for the emitter, one for the collector and one for the base but it has more contact and there is a certain distance between them.
The more often the distance between the first pin of the transistors "collector−1" and the last pin "collector−n" in n is the number of the collectors in one transistors, is proportional to the distance between the transistor and the component that must be connected with. That's why it is very difficult to understand how to extract the equivalent resistance and inductance of the connections. The Figure 3.1 explain an example of extraction of the parasitics.

If the transistor has 4 collector and the objective is to extract the resistance and in-

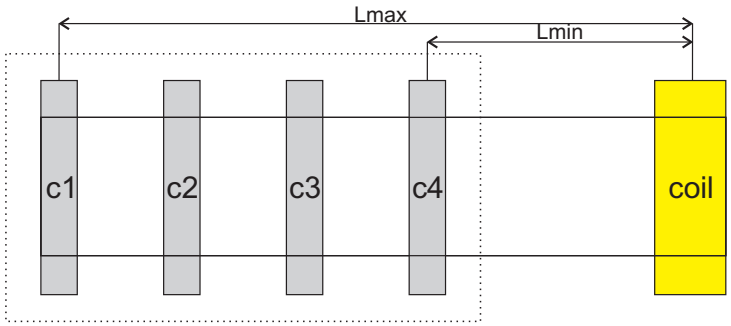


Fig. 3.1: Representation of connection between coil and collector of the transistors

ductance between the pin of the coil and the transistor, there are 4 paths. The first is between the coil and the nearest collector of the transistors, the second is between the coil and the second pin and so on until the last pin. Obviously the resistance between

the coil and the nearest pin of the BJT is much smaller than the resistance between the coil and the most distant one. Furthermore the majority of the current will pass on the nearest pins. Now the difficult thing is to choice the right value of the parasitic.
A pessimistic way is to use the distance that is 2/3 the maximum distance or the medium distance. Since the real flux of current is bigger through the nearest pins and lower in the more distance pin, the real solution should be a value of distance between the medium an the minimum distance.
In this design some times is used the medium distance for the extraction and sometimes 2/3, in order to have a pessimistic analysis.
During these analysis we saw that the most contribute of resistance and inductance that degrade the tank and the tuning range is given by the cross−connection, that is the connection between the base of the transistors and the collector off the other transistors. This connection has a big capacitance C_{couple} in the middle at this comports a quite long path. Moreover it is necessary to use less conductive layers for the point of cross and this point produces a capacitive couple that affect the performance.
For example the value of resistance at 20 GHz and inductance extract from the electromagnetic simulator of the cross connection is $R_{20GHz} = 450m\Omega$ and $L_{equi} = 27pH$. This value is very significant considering that the coil has an inductance of $\approx 140pH$ and an equivalent resistance of $\approx 400m\Omega$. In the Figure below there are the imagines of the layout were it is possible to see the placements of the components.

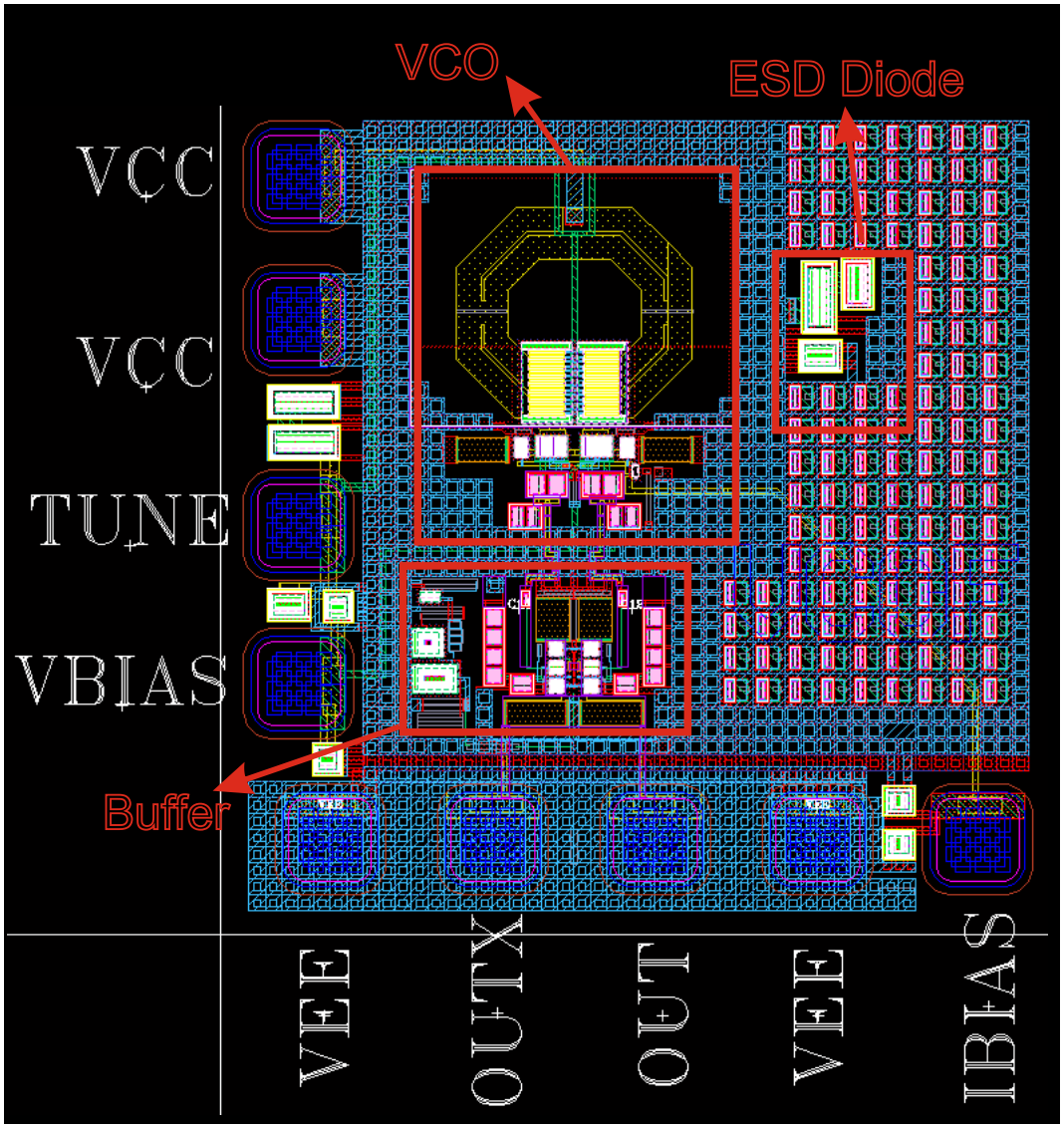


Fig. 3.2: Complete layout of the VCO Coil with the buffer

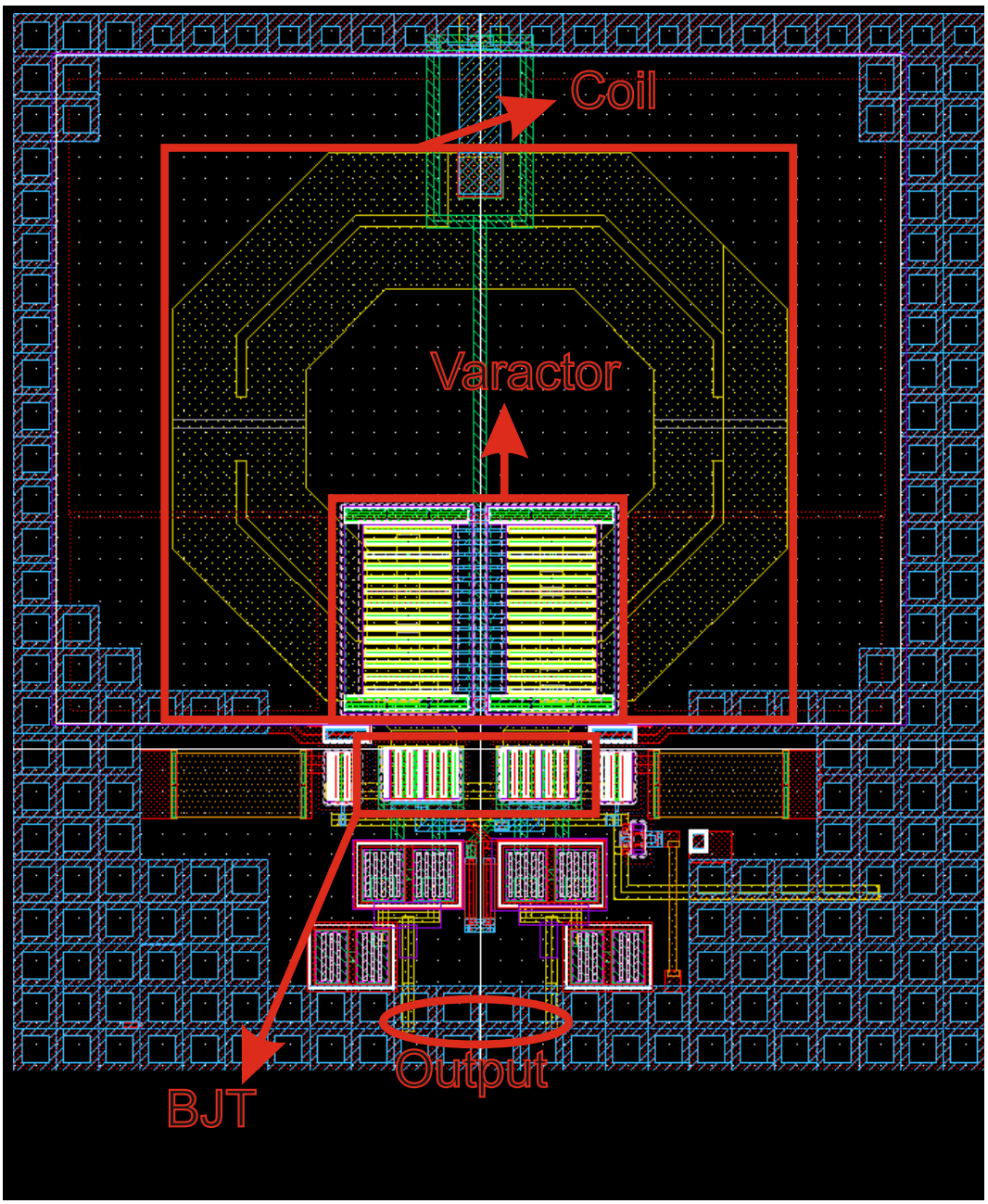


Fig. 3.3: Layout of the VCO Coil

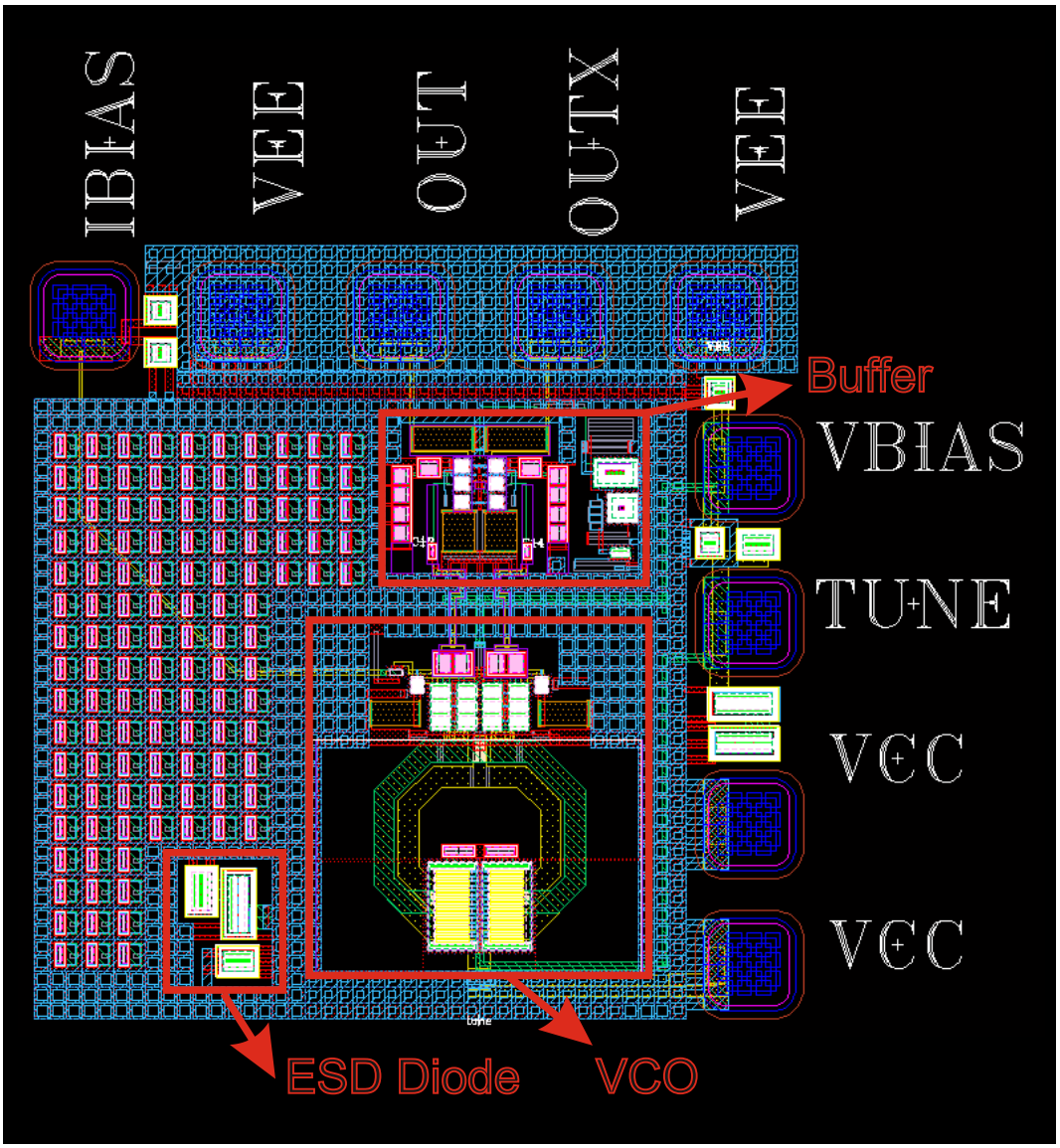


Fig. 3.4: Complete layout of the VCO with the buffer

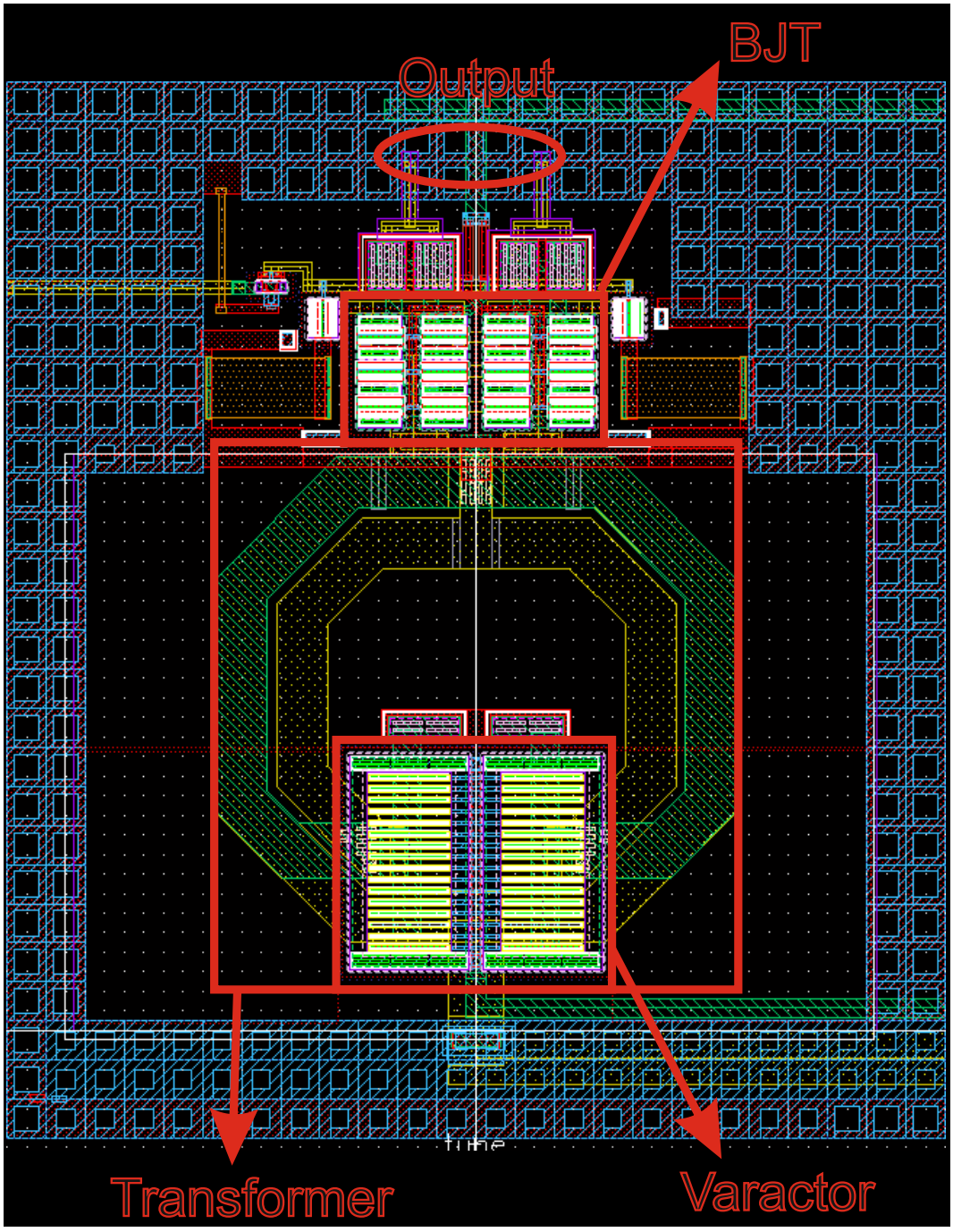


Fig. 3.5: Complete layout of the VCO with the buffer

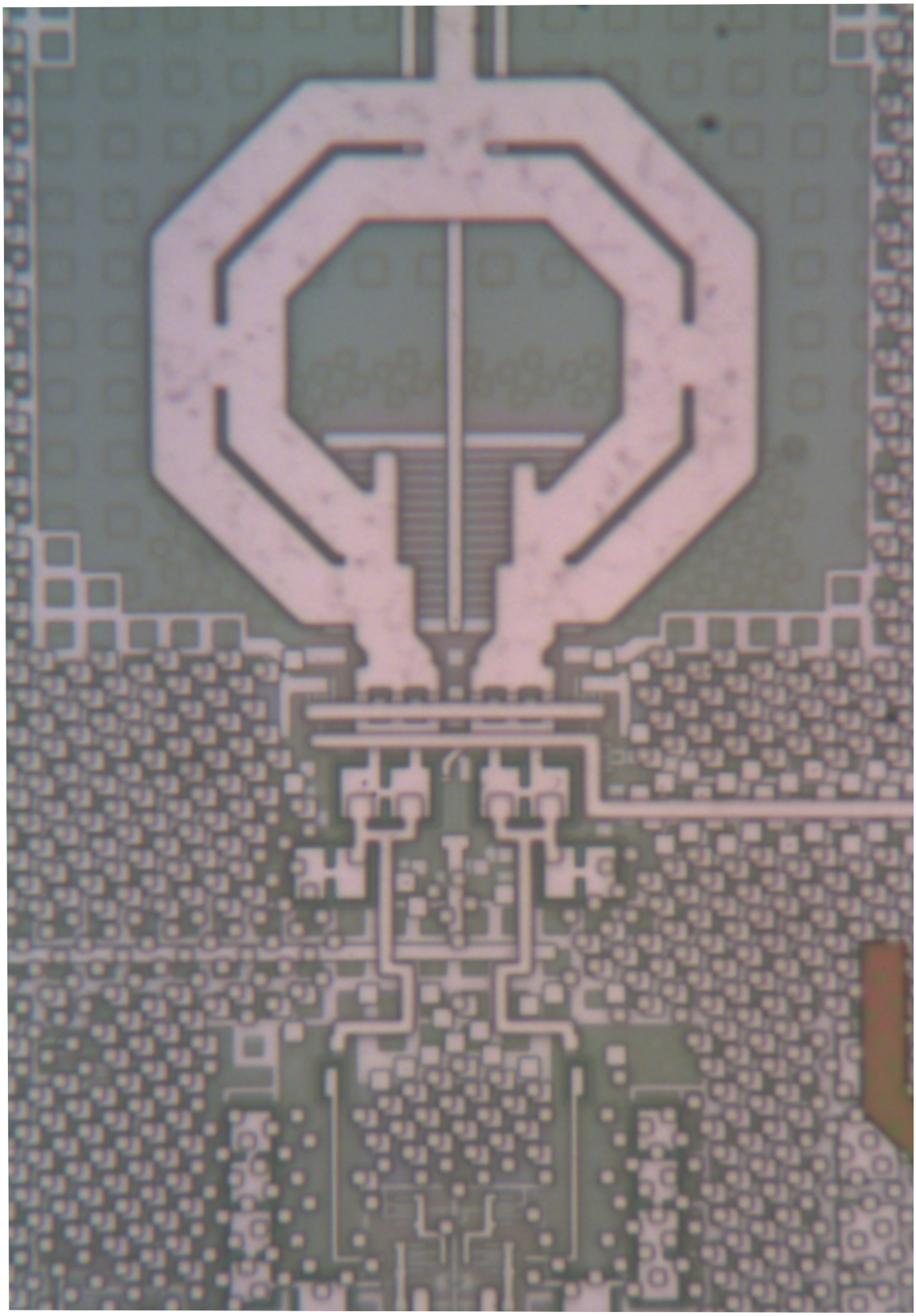


Fig. 3.6: Microscope photo of VCO with coil

Chapter 4

Results

In this chapter there are all the result exposed previously but considering the redesign operations due to the layout. Obviously the results are worse because in the simulation schematics, all the parasitics introduced by the connection are considered. The connections introduce resistive losses that degrade the quality factor of the resonant element and also introduce reactive components that reduce the tuning range and shift a little bit the range down. The graphs 4.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7, 4.8 represent the results. The figures of merits resulting are obviously degraded:

Tab. 4.1: Final results, temperature=25°C

	VCO coil	**VCO transformer**	**COMMENTS**
Vdd	**3.3 V**	**3.3 V**	
Idd	**20 mA**	**20 mA**	
$Vbias$	**2.5 V**	**2.5 V**	
$Vtune$	**3.6-8 V**	**0-3.3 V**	
$Freq$	**17.3-19.2 GHz**	**16.6-19.3 GHz**	
PN @ $1MHz$	**-123 dBc/Hz**	**-122.5 dBc/Hz**	@freq 18.5 GHz
$KVdd$	**200 MHz/V**	**50 MHz/V**	@freq 18.5 GHz
FOM	**-190 dBc/Hz**	**-190 dBc/Hz**	@freq 18.5 GHz
FOM_T	**-189 dBc/Hz**	**-191 dBc/Hz**	@freq 18.5 GHz

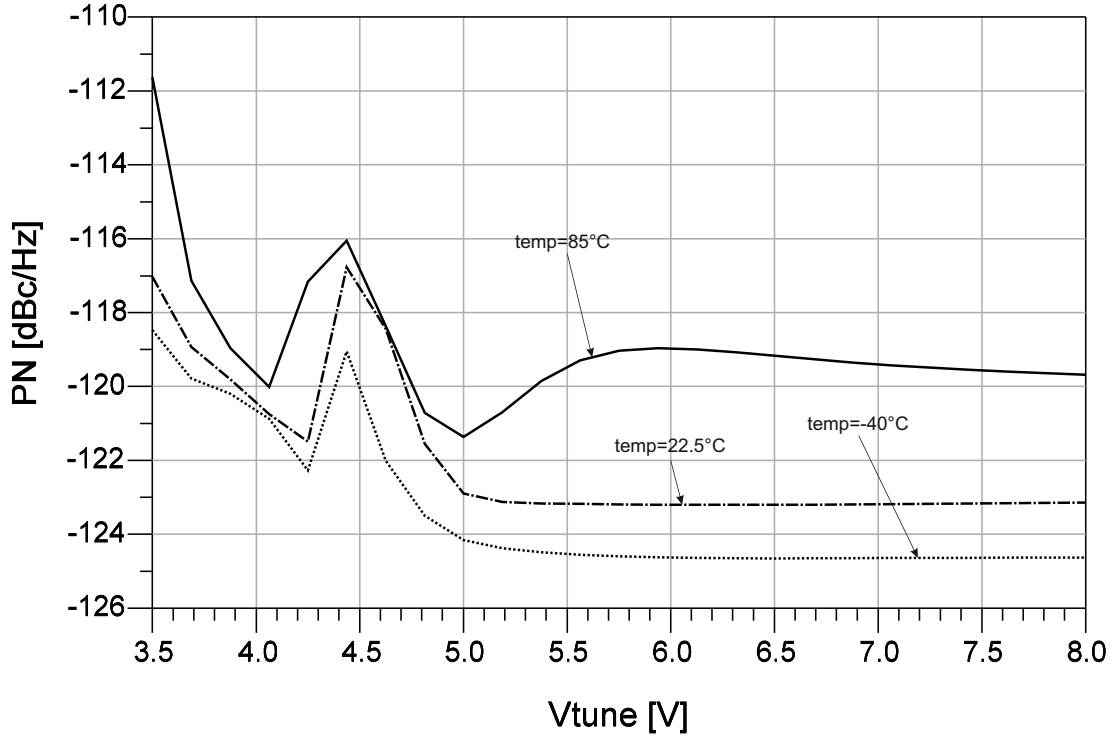


Fig. 4.1: Phase noise at 1 MHz offset versus tuning voltage Vtune varying temperature, after layout in VCO with coil

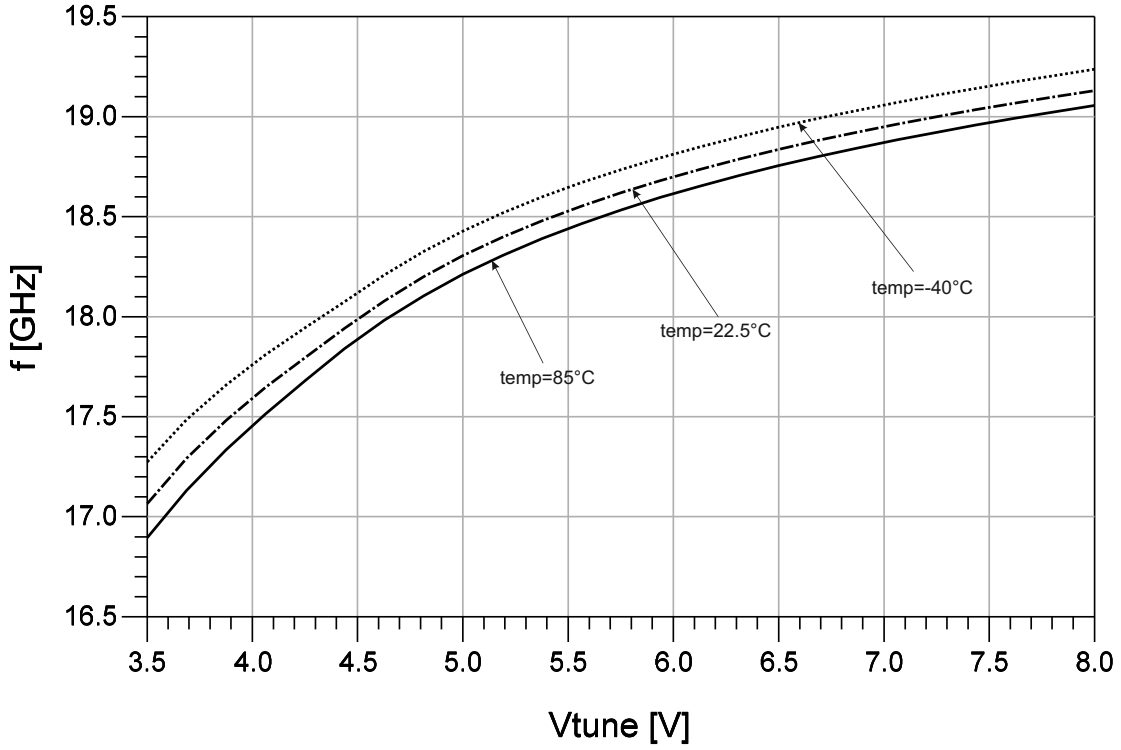


Fig. 4.2: Output frequency versus tuning voltage Vtune varying temperature, after layout in VCO with coil

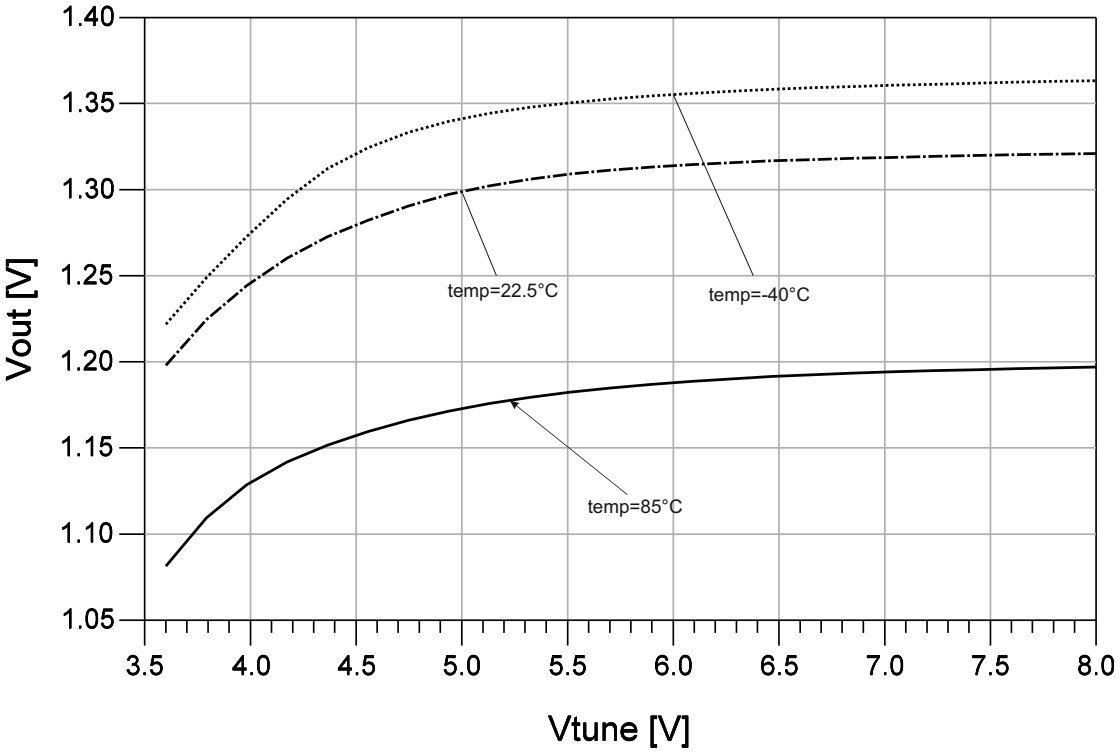


Fig. 4.3: Output voltage versus tuning voltage Vtune varying temperature, after layout in VCO with coil

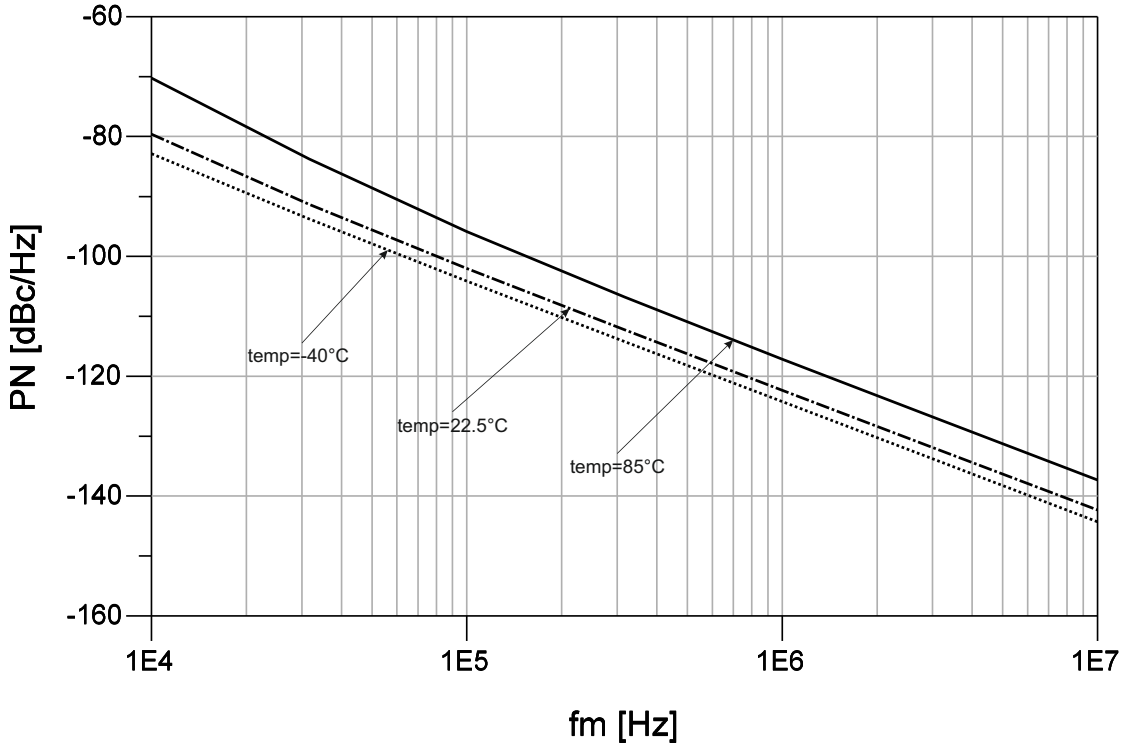


Fig. 4.4: Phase noise versus offset frequency f_m with $Vtune = 8V$, after layout in VCO with coil

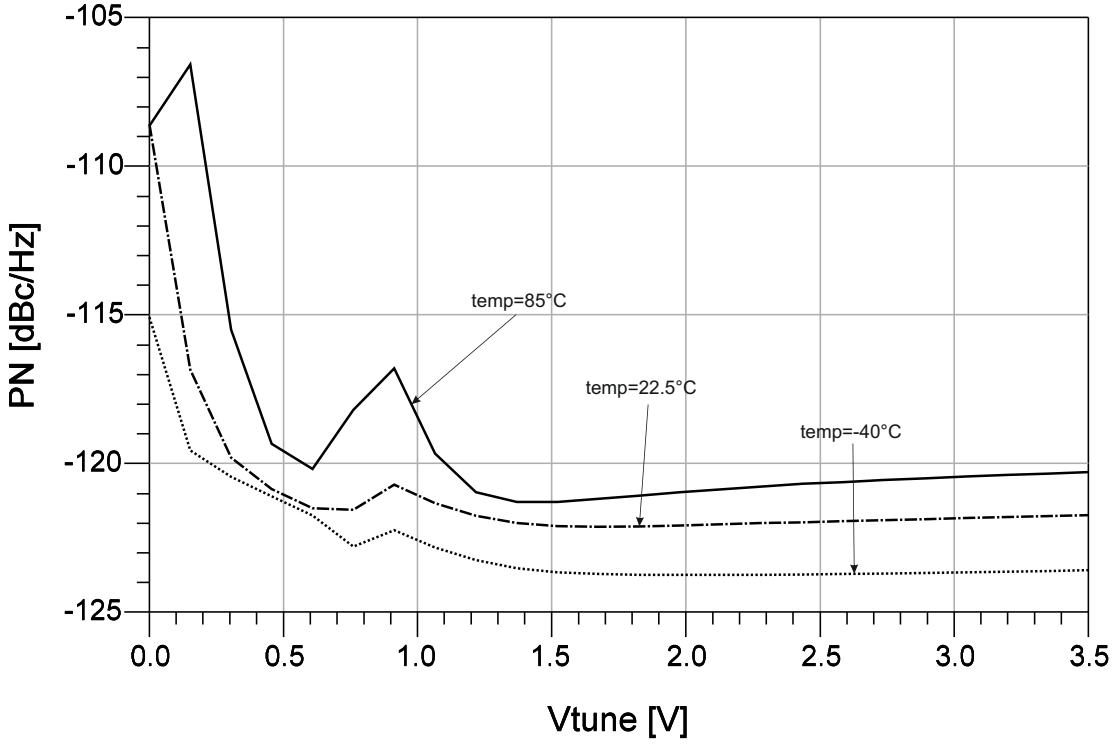


Fig. 4.5: Phase noise at 1 MHz offset versus tuning voltage Vtune varying temperature, after layout in VCO with transformer

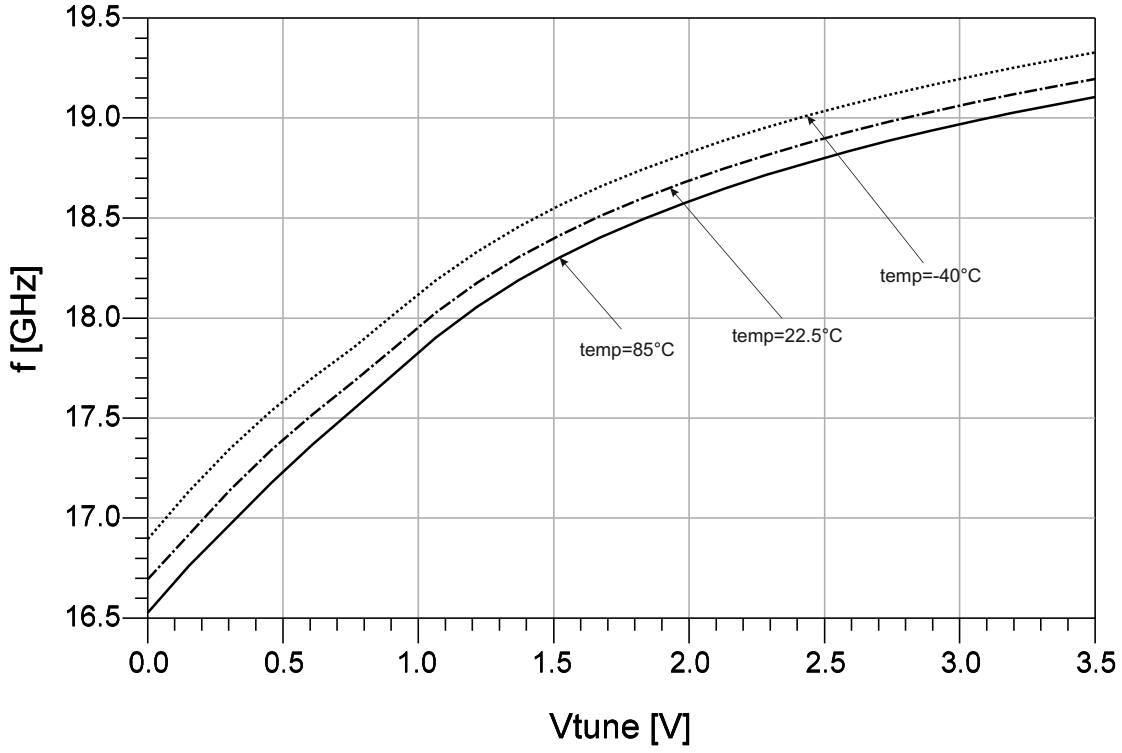


Fig. 4.6: Output frequency versus tuning voltage Vtune varying temperature, after layout in VCO with transformer

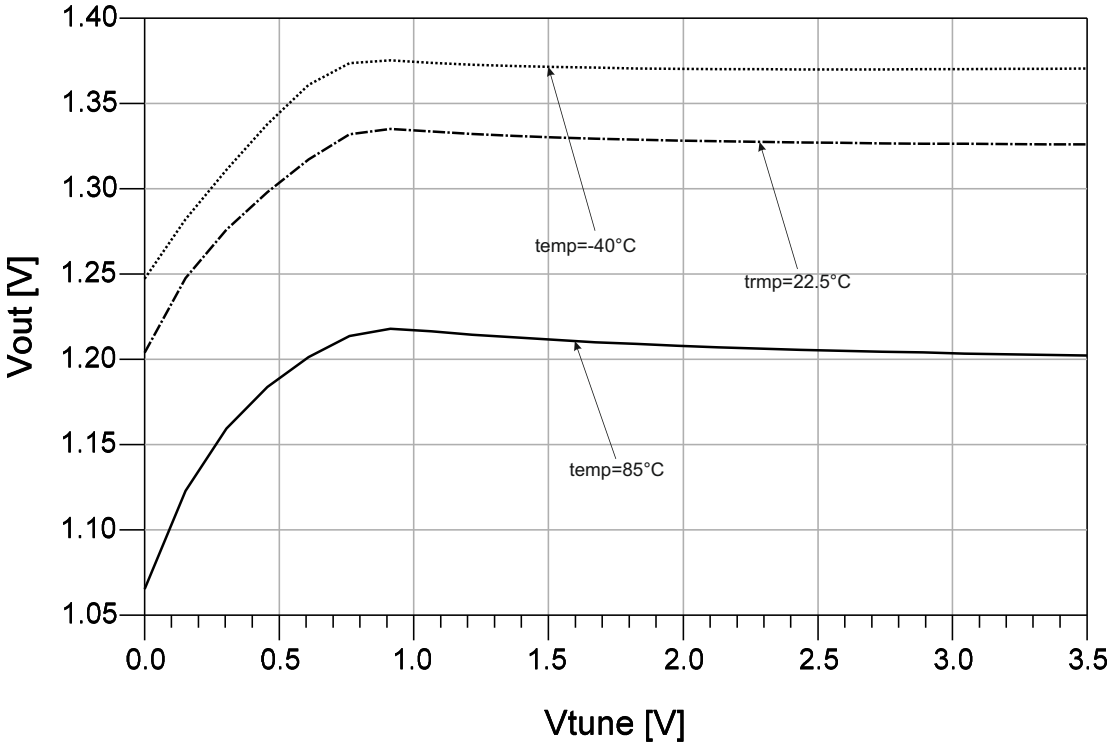


Fig. 4.7: Output voltage versus tuning voltage Vtune varying temperature, after layout in VCO with transformer

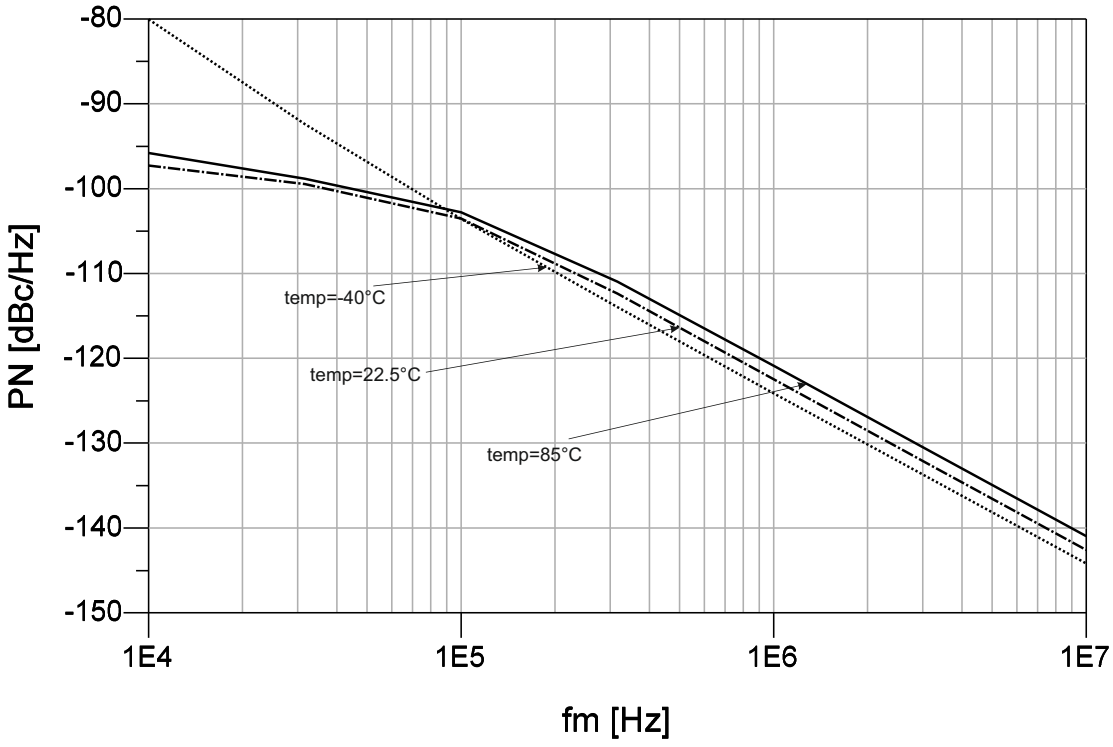


Fig. 4.8: Phase noise versus offset frequency f_m with $Vtune = 3.3V$, after layout in VCO with transformer

Chapter 5

Conclusions

Ultra low phase noise VCO design has been analysed in detail in this work. In the introduction, specifications and requirements for the VCO have been described , i.e. a tuning range from 17.75 GHz to 19 GHz with a phase noise below -120 dBc/Hz at 1 MHz offset. The primary application of the design is LTE backhaul wireless point to point Gbit communication 81-86 GHz which has been mentioned in the section 1.2, but adding a frequency divider by 8 the design will be also of great interest for cellular basestations. A introductory discussion about phase noise theory and literature overview has been presented in section 1.3.2 in order to understand the main sources of phase noise and to focus the design on the reduction of these contributions. Next the VCO has been optimized for low phase noise considering the integrated tank design, choice of transistors, transistor sizing and oscillation amplitude.

Of uppermost importance, a detailed analysis of a highest quality factor coil design has been done in the section 2.2 achieving a simulated quality factor up to 37 at the operating frequency of 19 GHz.

High output voltage swing is the next parameter in order to reach ultra low phase noise, class-C operation of the core design has been introduced and analysed in order to increase the voltage across the tank. Two design variants have been finalized including a full custom layout, both differential VCOs are realized in SiGe bipolar Infineon technology. The first circuit has a high quality factor differential coil implementing the inductive element in the tank. The second design is based on a transformer to decouple the varactor from the DC voltage supply, enabling a tuning voltage between 0 and 3.3 V.

The detailed VCO layout including capacitive, inductive and resistive parasitics at 20 GHz have been discussed in the chapter 3, focusing on the analysis and compensation of the parasitics at high frequency of work.

A phase noise below -120 dBc/Hz has been obtained for both the circuits and the tuning range is around 10%. The power consumption is 66 mW with a supply voltage of 3.3 V for both the designs and the resulting FOM is approximately -190 dBc/Hz. In order to make a comparison with other VCOs realized with the SiGe bipolar technology and used for the same applications, we compare with [32]. The center frequency of the VCO made

by IBM is 17 GHz and a lowest phase noise number of -100 dBc/Hz at 1 MHz offset was reported, that is more or less 20 dB worse than the one presented in this work.
Furthermore this design compares even favourable with respect to commercially available VCOs from HITITE. The presented design achieves a similar phase noise at one third of the power consumption as e.g. HMC398QS16G using InP technology.
Both VCOs were processed and will measured. If the specifications are fulfilled the VCOs will be integrated into the backhaul transceiver design project. Moreover, if the phase noise results are significantly better than [32], the design will be submitted to an international IEEE conference.

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