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Dynamic Rdson Setup and Measurements on Normally-on and Normally-off GaN-HEMT Power Electronic Devices

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Ai miei genitori

Abstract

The increasing demand for high performance devices, in particular in terms of power at high frequencies, has moved the research towards new materials with better properties than the ones of the materials used until now. Si and GaAs technology has by now reached its limits in terms of efficiency and stability at high frequencies. These mid-range bandgap-based electronic devices cannot be used for a wide range of application due to the limit imposed by the size of the bandgap. A solution to these kinds of problems has come from GaN and III-nitrides. The possibility of driving large current densities in GaN and to apply high voltages, together with the possibility of building heterostructures, enables the fabrication of GaN-based High-Electron-Mobility-Transistors (HEMTs) capable of large output power. The main non-ideality of interest in GaN HEMTs is the current collapse. This effect is related to electronic traps in the device structure. GaN based-HEMT's are used for high power and high frequencies applications; this effect is thus really important and considerably limits the performances of this kind of devices. it is possible to evaluate the current collpase by measurements of gate-lag and drain-lag. The term gate lag is used to describe the slow transient response of the drain current, when the gate voltage is pulsed. The gate lag phenomen can also be defined as an increase in the dynamic Rdson value (measured under pulsed conditions), comparing with the static Rdson value (measured in steady state). In this work we will build the GaN DReaM (GaN Dynamic Rdson Measurement): a particular setup capable of measuring the dynamic Rdson of devices both on package level and on wafer level. Then we will compare the measured dynamic value of Rdson with the static Rdson, with the aim of evaluating the level of degradation of the Rdson.

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Contents

Chapter 1

Introduction

1.1 GaN Peculiarities and Applications

The increasing demand for high performance devices, in particular in terms of power at high frequencies, has moved the research towards new materials with better properties than the ones of the materials used until now. Si and GaAs technology has by now reached its limits in terms of efficiency and stability at high frequencies; in the last decades these properties became fundamentals, thanks to the fast development of telecommunication and broadband access systems: there is an increasing demand for much more smaller systems capable of transferring datas very fast. high power and high temperature transistors are needed for automobile engines, future advanced power distribution systems, all electric vehicles and avionics. Many power electronics devices are used for voltage and frequency control for transmitting and converting electric power; reductions in loss and performance improvement of these devices will directly lead to considerable reduction in electric power consumption.

The semiconductors which have been used in electronics until now are Silicon (Si), Gallium Arsenide (GaAs) and all related III-V materials. The energy bandgap of these semiconductors are 1.12 eV for Si and 1.43 eV for GaAs, which are mid-range values. Unfortunately those mid-range bandgap-based electronic devices cannot be used for a wide range of application due

to the limit imposed by the size of the bandgap. A solution to these kinds of problems has come from GaN and III-nitrides. Some possible applications of GaN devices in power electronics are shown in fig. 1.1.

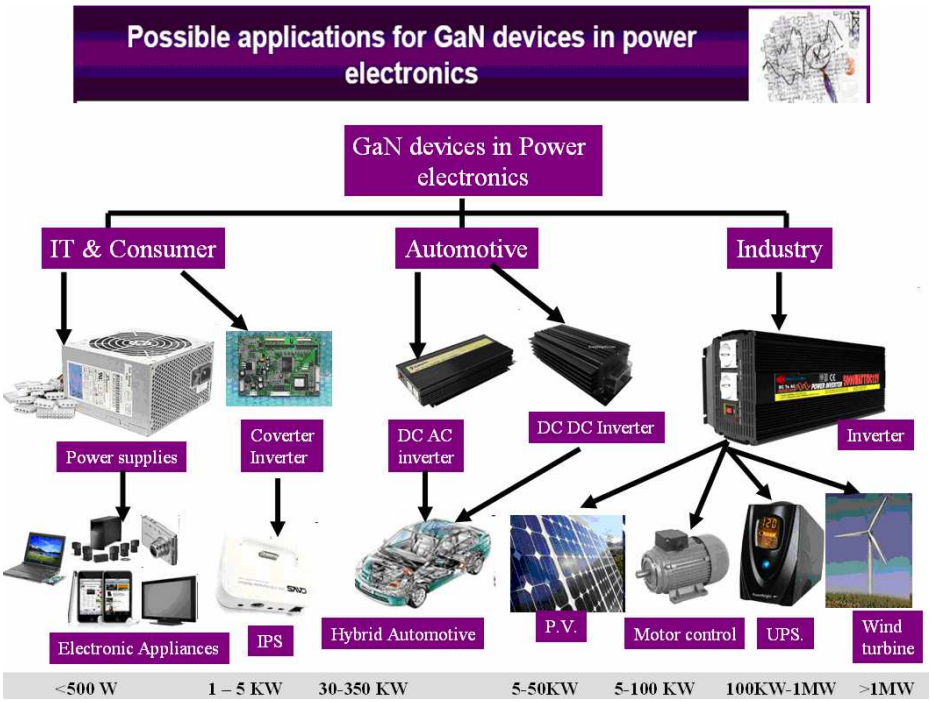

Figure 1.1: Some Applications of GaN Devices in Power Electronics (from a Yole Development study).

The bandgap of III-nitrides are large and direct and vary from 0,7 eV for InN to 6,2 eV for AlN.

The graph 1.2 indicates that semiconductors with small lattice constant exhibit larger bandgap energies; a small lattice constant stands for strong interatomic forces, which are responsible for the strong chemical bonding, thus leading to a large bandgap energy. GaN owns a high energy gap; this is a great advantage is terms of device's performances: the energy gap represents the energy that the electric field must give to a carrier, in order to bring it to the conduction band; thanks to the high energy gap values, GaN can easily support very high breakdown electric fields, so that the size of the devices can be reduced. In particular we usually have high electric field values between

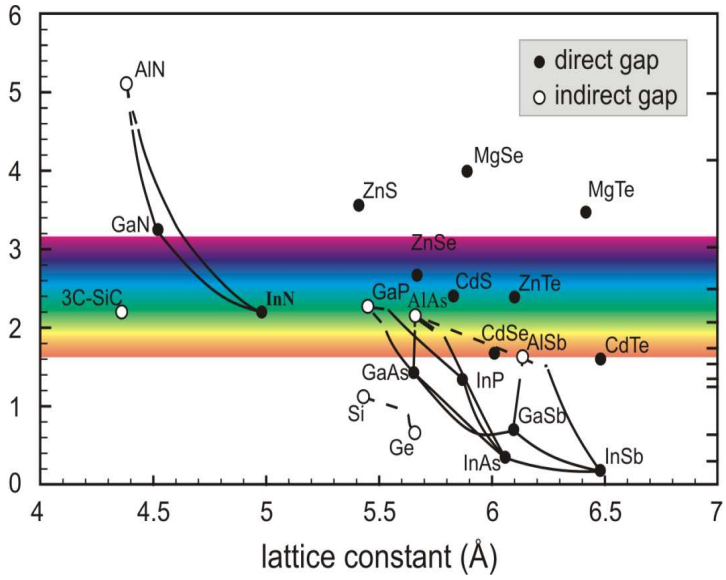

Figure 1.2: Bandgaps of the most important elemental and binary cubic semiconductors versus their lattice constant at 300K. The right-hand scale gives the light wavelength λ, corresponding to the band gap energy.[5][19]

Gate and Drain, thus it is possible reduce this distance. The large Band Gap, moreover, enables GaN to operate at high temperatures: High energy gaps lead to low thermical carrier generation, so that we avoid problems of intrinsical generation wih temperature. The thermal conductivity of Nitrides is about three times that of Si, therefore GaN power electronic devices can operate with less cooling and fewer high cost processing steps associated with complicated structures designed to maximize heat extraction [Pearton 2000].

One of the main features of Nitrides is the possibility of fabricating heterostructures with larger band discontinuity, by using AlGaN, AlInGaN or InAlN. A two dimensional electron gas (2DEG) is formed at the heterostructure's interface due to spontaneous and piezoelectric polarization (more detail will be given in the next section). The presence of a 2DEG leads to a high maximum drift velocity (fig. 1.4) and a relatively high electron mobility (fig 1.3), comparable with the intrinsic semiconductor, thanks to the absence of scattering phaenomenas between carriers or between carriers and doping impurities.

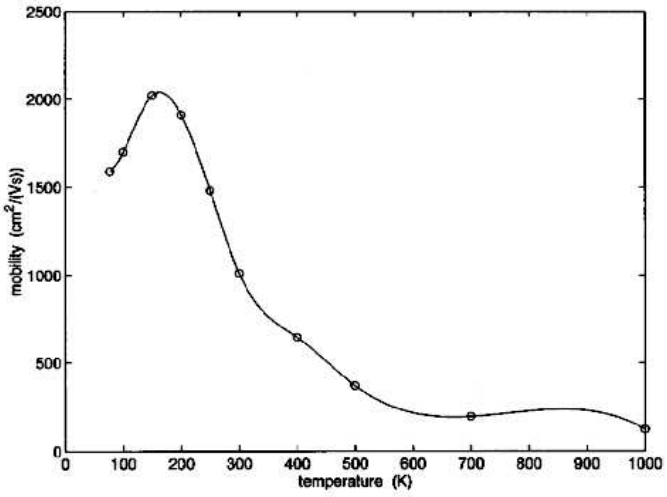

Figure 1.3: GaN Electron Mobility [1].

These peculiarities make GaN-based heterostructures especially promising as high frequency devices.

Electron mobility and drift velocity depend also on the temperature: in the graphs in fig 1.3 [1] we can see that the value of the electron mobility at 300K is about $1000cm^2/Vs$, before going down while the temperature is increasing, due to scattering phaenomenas.

The comparison of GaN with some other important semiconductor materials is shown in fig. 1.5 [Yole 2005]; all semiconductors, which are promising candidates for the RF applications, are schematically indicated in a frequency-power diagram. Current technology is mainly based on Si or GaAs devices. As illustrated in fig. 1.5, GaN covers a fairly large frequency range while maintaining a high output power relative to the others. It is in strong competition with SiC on its low frequency side and with GaAs and InP on its low power/ high frequency side.

To further apprehend the advantages of GaN for future RF market, the material properties and figures of merit (FOM) of GaN, InP, GaAs, SiC and Si are summarized in Table 1.6. The FOM values for GaN are orders of magnitude higher than those for Si or GaAs and slightly higher than those

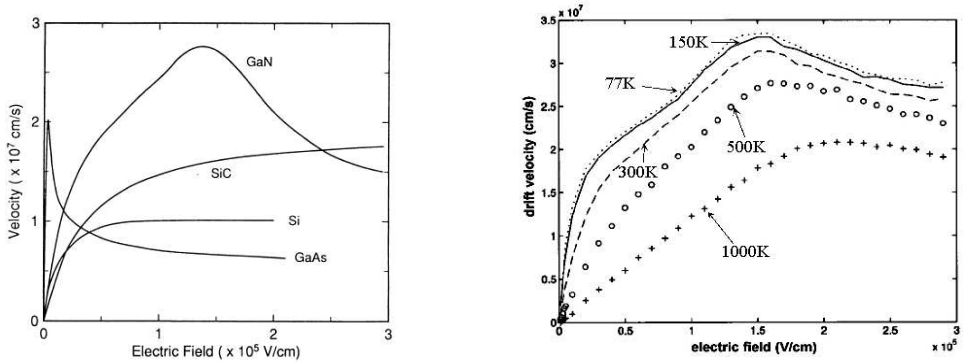

Figure 1.4: Electron Drift Velocity of GaN, SiC, Si and GaAs at 300 K omputed Using the Monte Carlo Technique [Gaska 1998] (on the left) and GaN Drift Velocity vS Temperature (right) [1].

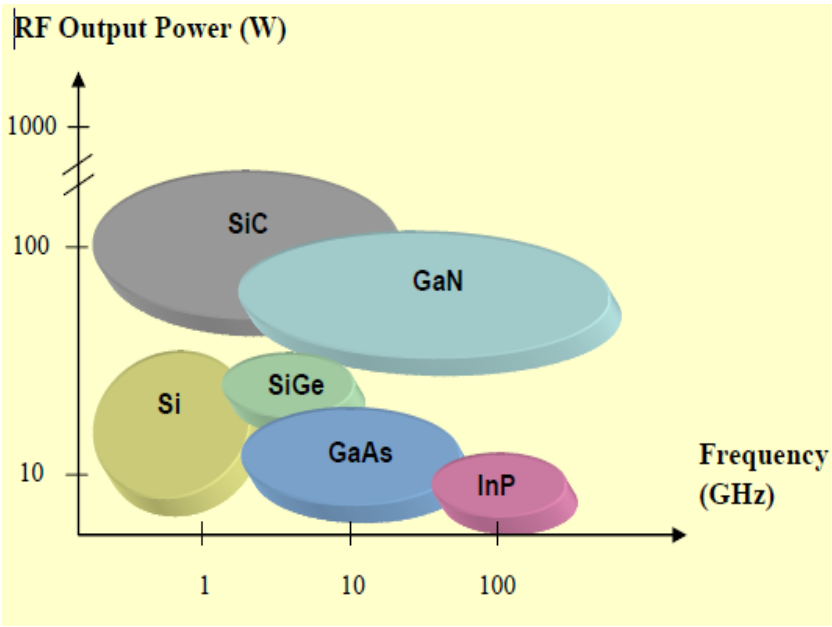

Figure 1.5: Semiconductor Materials for RF Applications. RF Power is Plotted against Frequency [Yole 2005].

of SiC. Thus, it is anticipated that GaN can outperform Si, GaAs, and SiC in the microwave electronic applications.

	GaN	*InP*	*GaAs*	*SiC*	*Si*
Bandgap E_g [eV]	3.39	1.35	1.42	3.26	1.1
Breakdown field E_{br} [MV/cm]	3.3	0.5	0.4	3.0	0.3
e-mobility μ_n [cm^2/Vs]	1200-2000	5400	8500	700	1350
Saturation velocity v_{sat} [10^7cm/s]	2.5	1	1	2	1
Thermal conductivity K_{th} [W/cmK]	1.3	0.7	0.43	4.5	1.5
Relative dielectric constant ε [ε_r]	9.0	12.5	13.1	10.0	11.8

Figure 1.6: Physical Properties of GaN, InP, GaAs, SiC and Si [9].

By using AlGaN, AlInGaN or InAlN, it is relatively easy to produce structure with sheet electron densities of $(1-3)*10^{13}cm^{-2}$; this electron density is 4-5 times larger than in AlGaAs/GaAs heterostructures, moreover the saturation drift velocity of GaN is 2.5 times that of GaAs. The maximum current is proportional to the product of the carrier density and the saturation drift velocity [18]: an approximate calculation shows that the maximum current density for GaN-based (HEMTs) is 10-15 times larger than for AlGaAs/GaAs structures.

As we said before, GaN shows also a high breakdown voltage (Vbr). The critical breakdown field varies roughly with Eg^2 and is estimated to be $> 3MV/cm$ for GaN compared to 0.3 MV/cm for Si and 0.4 MV/cm for GaAs [Bandic 1998], thus GaN-power electronic devices can be made ten times thinner than Si. The large breakdown electric field implies that a large electric field can be applied without damaging the devices. This

means that the possibility of driving large current densities and to apply high voltages, together with the possibility of building heterostructures, enables the fabrication of GaN-based High-Electron-Mobility-Transistors (HEMTs) capable of large output power. The most diffused type of Heterostrusture for HEMT is the AlGaN/GaN junction, capable of having great performances in terms of maximum voltage and current.

1.2 Switching Behaviour and Losses - GaN vs Si

Wide-band-gap semiconductors are expected to be used as materials for new switching devices with low losses and high switching speed, comparing with Silicon. Let us compare GaN HEMTs and Silicon mosfet switching characteristic, in order to understand what are the main differences that make GaN-HEMTs the best as high frequency switching devices. As you can see in figure 1.7, we study the MOSFET switching behaviour thanks to a test circuit that simulates the typical working conditions of the device (in this example, a typical buck converter). We suppose the current I_L, flowing throw the inductance, to be constant. When $i_D < I_L$, a current equal to $I_L - i_D$ flows throw the ideal diode and $v_{DS} = E$. The gate voltage is driven, throw the resistance R_G, by a square wave voltage that goes from 0V up to V_{GG}. In order to fully understand the MOSFET's switching behaviour, we must take into account the capacitances C_{GD},C_{GS} and C_{DS}, shown in fig 1.7.
When we want the transistor to switch on, the gate driver voltage goes up to V_{GG}, while the current i_G charges the capacitances C_{GD} and C_{GS} throw the resistance R_G, then v_{GS} starts to increase. When, after a delay time equal to t_{don} (fig 1.7), v_{GS} reaches the threshold voltage V_{GSth}, the drain-source current i_D starts to increase, until reaching the maximum value I_L, after a delay time equal to t_{ri}. Then the ideal diode inhibits itself and, since the current I_L cannot increment anymore, i_D needs to discharge the capacitances C_{GD} and C_{GS} in order to rise, therefore v_{DS} decreases. In the meantime the gate current i_G charges the capacitance C_{GD}, while v_{GS} remains constant.

Therefore there is a period of time t_{fv} during which the gate voltage is constant: this behaviour is typical of voltage driven devices, such as MOSFET and IGBT. When V_{DS} reaches reaches the limit of the ohmic region, that corresponds to V_{GSth}, v_{DS} stops decreasing, whereas V_{GS} starts again rising up to V_{GG}. The period of time $t_{swon} = t_{ri} + t_{fv}$ is called *switching on time*. The integral of the current i_G gives the total charge Q_G given to the gate, that depends on the gate voltage and that can be divided into Q_{GS} and Q_{GD}, respectively stored in C_{GS} and C_{GD}. These charges have a typical value that is related to the type of device and depends on both v_{GS} and v_{DS}. During the switching off period, the reverse process occurs.

By studying the MOSFET switching characteristic, we can see that during the switching times, the device need a not negligible gate current i_G, in order to charge and discharge the capacitance C_{GS} and most of all C_{GD}. This current represents a power dissipation, that gets worse with the number of commutations, therefore with the working frequency.

Referring to any component operating in switching mode, the power losses (P_l)can be mainly divided in two groups:

- Conduction Losses (P_c) (related to the energy W_{on} and W_{off} in fig 1.8)
- Switching Losses (P_{sw}) (related to the energy W_{cond} in fig 1.8)

Let us see how to calculate the *switching losses* of a silicon MOSFET, in order to compare it with a GaN device [3]:

$$P_{sw} = (E_{swon} + E_{swoff}) * f_{sw} \tag{1.1}$$

As for the switching on time [3]:

$$E_{swon} = \int_0^{t_{swon}} v_{DS}(t) i_D(t) dt = E * I_{Don} * \frac{t_{swon}}{2} + Q_{rr} * E \tag{1.2}$$

where $t_{swon} = t_{ri} + t_{fu}$. t_{ri} depends on the value of the capacitances C_{GS} and

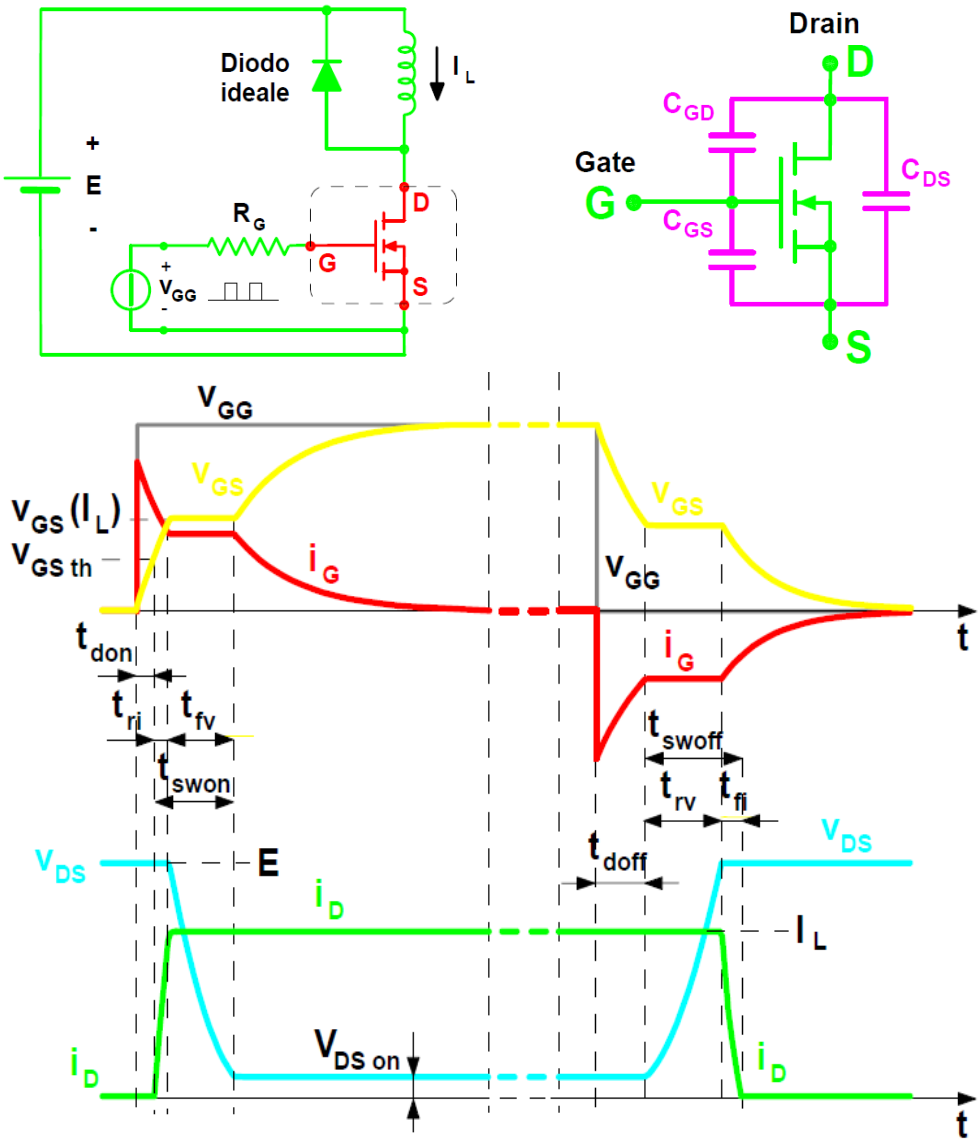

Figure 1.7: Study of the Silicon MOSFET switching behaviour by using a test circuit with inductive load [7]

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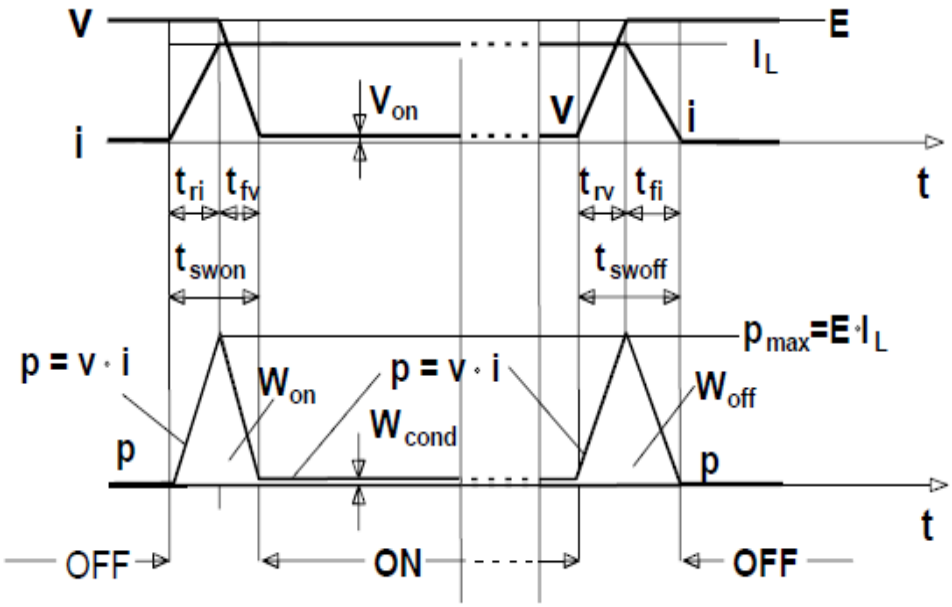

Figure 1.8: Switching and Conduction losses for a silicon MOSFET measured inside a circuit with inductive load [7]

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C_{GD}, whereas t_{fu} is defined as [3]:

$$t_{fu} = (E - R_{DSon} * I_{Don}) \frac{C_{GD}}{I_{Gon}} \tag{1.3}$$

Regarding the switching off time [3]:

$$E_{swoff} = \int_0^{t_{swoff}} v_{DS}(t) i_D(t) dt = E * I_{Doff} * \frac{t_{swoff}}{2} \tag{1.4}$$

where $t_{swoff} = t_{ru} + t_{fi}$. t_{fi} depends on the value of the capacitances C_{GS} and C_{GD}, whereas t_{ru} is defined as [3]:

$$t_{ru} = (E - R_{DSon} * I_{Don}) \frac{C_{GD}}{I_{Goff}} \tag{1.5}$$

Since the MOSFET‘s switching losses are defined by the expression 1.1, we can desume the importance of the capacitances C_{GS} and C_{GD} in the MOSFET‘s switching behaviour. The switching losses are as negligible as the capacitances C_{GS} and C_{GD} are small, where C_{GD} has the main role.

The strength of GaN-HEMTs are the very low values of the capacitances C_{GD}, C_{GS} and C_{DS} in comparison with silicon MOSFETs. In the following an EPC device (fig 1.9) is shown as an example. As you can see in figure 1.9, thanks to the lateral structure, the capacitance C_{GD} comes only from a small corner of the gate: an extremely low C_{GD} leads to a very rapid voltage switching capability. C_{GS} consists of the junction from the gate to the channel summed to the capacitance of the dielectric between the gate and the field plate.C_{GS} is large when compared to C_{GD}, giving GaN transistors excellent dV/dt immunity, but it is still small when compared with Silicon MOSFETs, giving them very short delay times and excellent controllability in low duty cycle applications . The lateral structure of the GaN transistor makes it a very low charge device: it has the capability of switching hundreds of volts in nanoseconds, giving it multiple megahertz capability. This capability will lead to smaller power converters and higher fidelity class D amplifiers [2].

As for the *conduction losses* (P_c), they can be calculated by using a

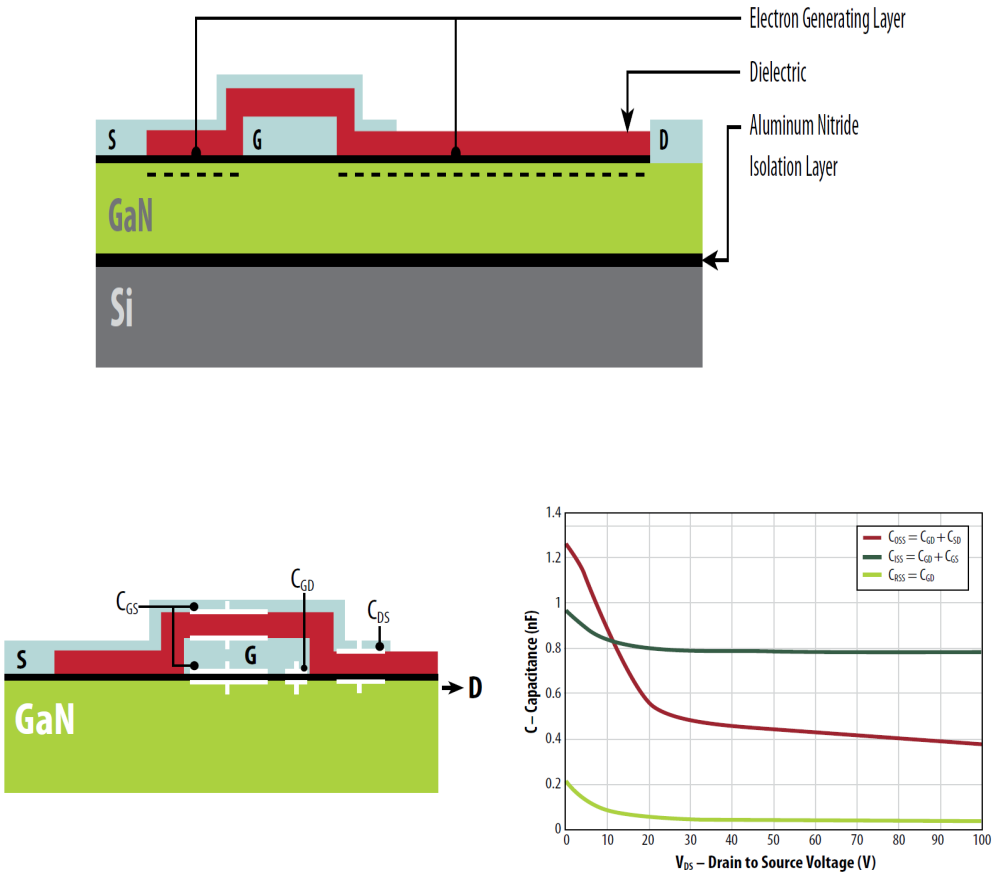

Figure 1.9: Values and locations of physical capacitances inside an EPC device [2]

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MOSFET-approximation with the drain-source on-state resistance (R_{DSon}) [3]:

$$v_{DS}(i_D) = R_{DSon}(i_D) * i_D \tag{1.6}$$

where v_{DS} and i_D are the drain-source voltage and the drain current respectively. Therefore, the instantaneous value of the MOSFET's conduction losses is [3]:

$$p_C(t) = v_{DS}(t) * i_D(t) = R_{DSon} * i_D^2(t) \tag{1.7}$$

The integration of the instantaneous power losses over the switching cycle gives an average value of the MOSFET's conduction losses [3]:

$$P_C(t) = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_C(t)dt = R_{DSon} * i_{Drms}^2 \tag{1.8}$$

where i_{Drms} is the rms value of the MOSFET's on-state current.

As we can see from these formulas, the conductive losses are directly proportional to R_{DSon}.

Therefore, for a switching device, it is very important to have a very low R_{DSon}, in order to minimize the conduction losses. Now the reason why GaN HEMTs particulary fits high frequency applications is clear, but unfortunatelyGaN suffers from current collapse, that is responsible for an increase of the Rdson in dynamic mopde during the switching on, due to trapping effects at the surface or/and in the buffer. The increase in the Rdson means an increase in the conduction losses. In section 3.4.1 we will introduce the method for calculating the Rdson in Gan HEMTs and how to compare the dynamic R_{DSon} value with the static R_{DSon} one, in order to evaluate the presence and, possibly, the level of current collapse.

Chapter 2

GaN-HEMTs - Structure and Operating Principles

2.1 GaN Crystal Structure

In order to better understand the origin for of GaN's benefits, listed in section 1.1, the crystal structure and the band structure will be discussed in the following part.

Gallium Nitride (GaN) is a compound semiconductor, formed by an atom of Gallium (Ga), an element of the III group on the periodic table, and by an atom of nitrogen (N), that belongs to the V group. GaN crystal structure is shown in fig. 2.1.

GaN, as well as other III nitrides-group, can crystallize into wurtzite, zincoblende or rocksalt structure; in ambient conditions the thermo dynamical stable structure is wurtzite for bulk GaN, AlN or InN, therefore the most common used crystal structure in devices is wurtzite, which has a hexagonal unit cell and thus two lattice constants, c and a (fig. 2.1); this crystal structure consists of two interpenetrating hexagonal close-packed lattices, which are shifted with respect to each other.

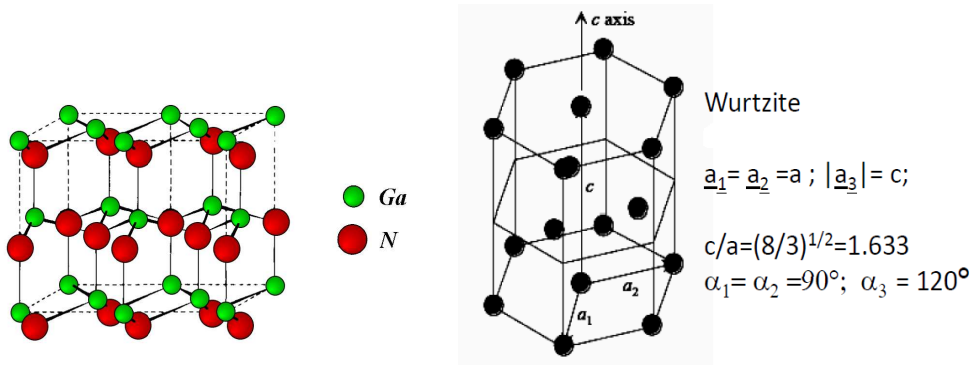

Figure 2.1: GaN Crystal Structure (left) and Wurtzite Unit Cell (right)

2.2 The Concept of Heterostructure

The possibility of building heterostructures enables the fabrication of GaN-based High-Electron-Mobility-Transistors (HEMTs), thus we would like to briefly introduce the concept of heterostructure.
The heterostructures are junctions between materials with different Energy Gap and some other different proprieties. They are obtained by growing a certain type of crystal (epilayer) on another crystal (substrate) with a different lattice constant (fig. 2.2); this type of process is called *heteroepitaxy*. If the lattice constants are similar enough, so that the amount of defects at the iterface between the two materials is negligible, we wil obtain a so called *heterostructure*; vice versa, if the lattice constants are extremely different, so that the amount of defects is prettly big, at the interface we will find defects called *misfit dislocations*, who will act as traps for electrons.

Heterostructures let us obtain particular electrical and optical proprieties, thanks to the electrical and optical confinement. They are used in order to build new devices, such as bipolar transistors, FET, LED, laser, photodetectors etc.

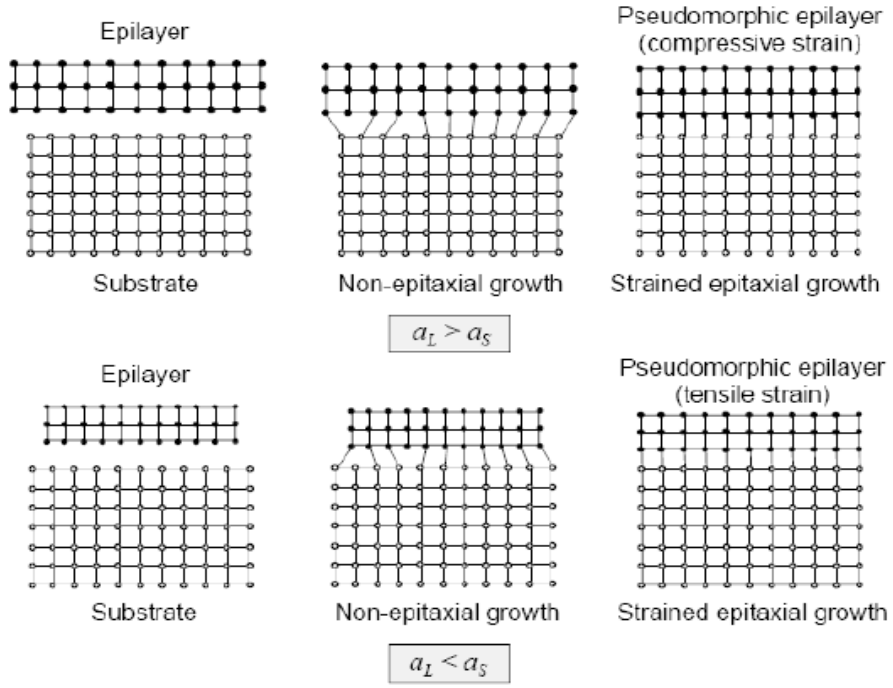

Figure 2.2: Hepitaxy. Compressive and Tensile Strain.

2.3 HEMT's - Structure and Operating Principles

The HEMT, High Electron Mobility Transistor, are transistors with high electron mobility, based on a heterostructure between high band gap semiconductors. The high electron mobility value is related to the way in which the channel is formed: the channel is not formed on a doped semiconductor, but on a intrinsic one: in this way the mobility cannot decrease due to the scattering phaenomena between electrons and doping elements. These kinds of devices are built with a heterostructure that let us take advantage of the high carrier concentration of a doped semiconductor and the high mobility of the not doped one, where the carriers are collected.

The HEMT's fundamental element is the heterostructure, composed by a *buffer layer* (GaAs in fig.2.3), on which we deposit a so called *barrier layer* (AlGaAs in fig.2.3), doped with donors, with the aim of providing carriers. In order to build the heterostructure, we put two materials with different energy gaps closed together: at the interface a conductive channel is formed, thanks to the bands bending (fig. 2.3). The buffer layer conductive band goes down under the Fermi level, so making free a lot of electrons in the conduction band. Now carriers are confined inside the quantum well created by the bending bands. We have formed a channel where carriers can move only along the interface between the two semiconductors; the carriers in the channel are able to move only in two directions, thus the channel is called *Two Dimensional Electron Gas* (2DEG).

By applying voltage to the device, a high quantity of current is passing, thanks to the absence of scattering phaenomena between ions and doping impurities, thus we find mobility values comparable with the ones of the instrinsic material. The heterostructure is usually grown on a substrate, a material suitable for hepitaxial growth, and, in order to reduce the mismatch between buffer and substrate and thus the formation of defects, we can insert a thin layer called *nucleation layer* (fig 2.4). We can find a nucleation layer also between buffer layer and barrier layer, in order to support the carriers confinement and to increase the electron mobility.

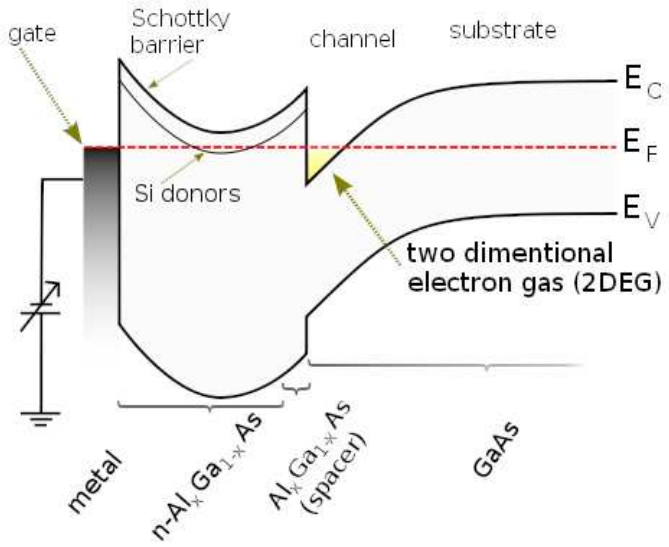

Figure 2.3: Band Diagram of an AlGaAs/GaAs Heterostructure [25].

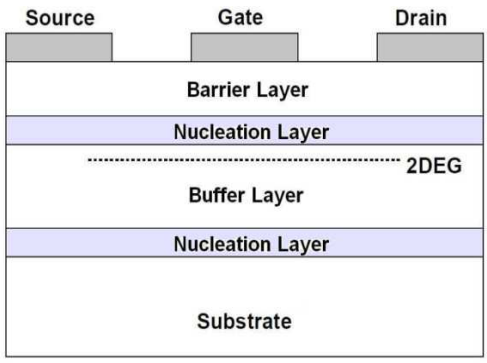

Figure 2.4: HEMT's Typical Structure [25].

Nowadays the most studied heterostructure is the AlGaN/GaN one, that thanks to GaN peculiarities, gives birth to a very high carrier concentration at the interface, even with an undoped barrier layer. GaN based HEMT's way of working is similar to the one described above, but, by comparing with the GaAs-based devices, GaN-HEMT's presents a different channel's formation mechanism.
In order to understand how the 2DEG is formed in GaN-HEMT's, we need to briefly introduce the concept of spontaneous and piezoelectric polarization, without which the channel could not be formed [27].

2.3.1 Polarization

One of the most important properties for wurtzite III-nitrides group, like GaN, is that these materials exhibit an internal field caused by the spontaneous polarization (fig 2.5).

$$E = \frac{P}{\epsilon} \tag{2.1}$$

where P and ϵ stand for the Polarization vector and the dielectric constant respectively [10].

In the III-nitride crystals, for example InN, GaN and AlN, the crystal cell does not correspond to the ideal wurtzite's cell: there is a change in the position of positive and negative ions comparing with the ideal ones, due to the difference in electro negativity between the elements that belong to group-III and group-V; this phaenomena is called **Spontaneous Polarization** and it does not exist in materials with Zincoblenda' structure such as GaAs. Moreover GaN is chatacterized by high piezoelectric constants, so that we can find also a **Piezoelectric Polarization** effect, that, together with the spontaneous one, is fundamental for GaN devices, in order to let them work correctly. Piezoelectric Polarization effects are visible when GaN is put in contact with a material that show different lattice constant: in this way the forces at the interface between the two materials, caused by the lattice mismatch, are transformed into Piezoelectric Polarization, that, depending on the type of strain (compressive or tensile), can be directed in one direction or in the opposite one. In heterostructures such as AlGaN/GaN for example, AlGaN layer is subjected to tensile stress.

Thanks to his polar nature, GaN crystal may have two types of surfaces: one formed by Gallium atoms, Ga-face, and one formed by Nitrogen atoms, N-face. As it is shown in fig. 2.5, if the surface is of the type Ga-face, then the polarization vector is coming out from the surface, vice versa the vector is directed inside the surface.

When the AlGaN barrier layer is deposited on the GaN buffer layer, the piezoelectric polarization appears; this phaenomena is as much considerable as much important is the mechanical strain that the epilayer has to support. The stress between GaN and AlGaN is 5 times more than between AlGaAs

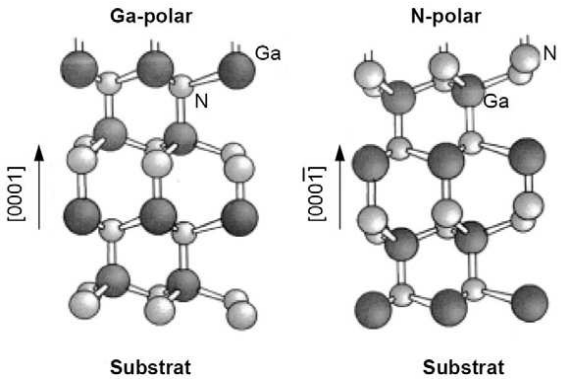

Figure 2.5: GaN Polarization [28].

and GaAs. In case of tensile strain, the vectors spontaneous and piezoelectric polarization are parallel and have the same verso, whereas they are opposed in case of compressive strain. As you can see in fig 2.6, these two types of polarization (only if they both are present) give birth to a quantum well on the low edge of the conduction band.

The different magnitude of the vector polarization in the two materials leads to a high negative charge concentration at the interface; the difference of band gap between the two materials make these electrons be confined in GaN. 2DEG channel is created thus without doping and without applying positive voltage: at the interface the carrier concentration is more or less $10^{13} cm^{-2}$ [**?**], which is more than ten times higher than in the doped AlGaAs/GaAs counterpart, so that GaN polar charge can be considered equivalent to a 2D distribution. In order to have the best carrier confinement, spontaneous and piezoelectric polarization must have the same direction. We can discuss about what are the best conditions for the 2DEG formation, depending on which one is the exposed GaN face: if the Ga-face is exposed, the best situation is when AlGaN is grown on GaN, because AlGaN is suffering from tensile strain, so that piezoelectric and spontaneous polarization vectors are aligned (fig. 2.7).
If the N-face is exposed, vice versa, we could consider the best situation to

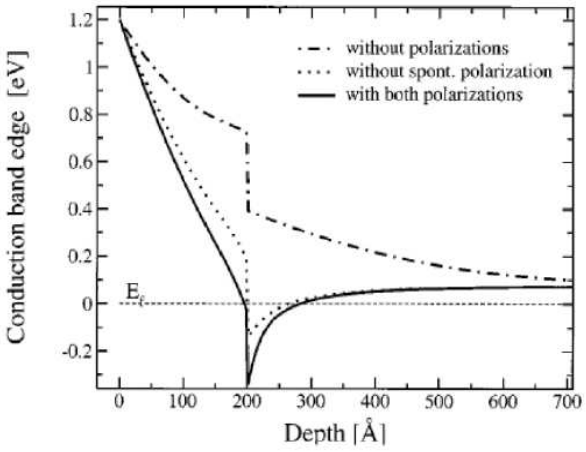

Figure 2.6: Conduction Band Bending for different values of Spontaneous and Piezoelectric Polarization Vectors (After Ambacher et. al. J. Appl. Phys. 1999).

be when GaN is grown on AlGaN, so creating a compressive strain; but in this case the vectors have opposite directions, so that the collected charge is much more smaller. Thus we can say that, by growing AlGaN on GaN (Ga-face), we can have the most populated 2DEG [25].

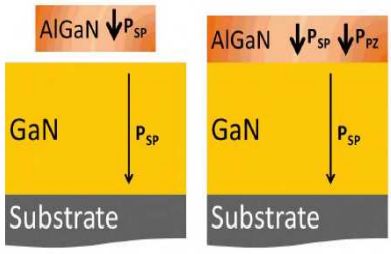

Figure 2.7: Spontaneous and Piezolectric Polarization Vectors in AlGaN before (on the left) and after (on the right) Heteroepitaxy.

2.3.2 The Role of Surface's Holes and Donors in the 2DEG Formation

After have explained the mechanisms that lead to the channel formation, it is necessary to comprehend where this huge amount of carriers comes from.

In fig. 2.8 it is shown how the polarization works in GaN ; inside the material positive and negative polar charges compensate each others, whereas on Ga-face and on N-face the polar charge is clearly present ($-Q_\pi$ on Ga-face and $+Q_\pi$ on N-face) [10].

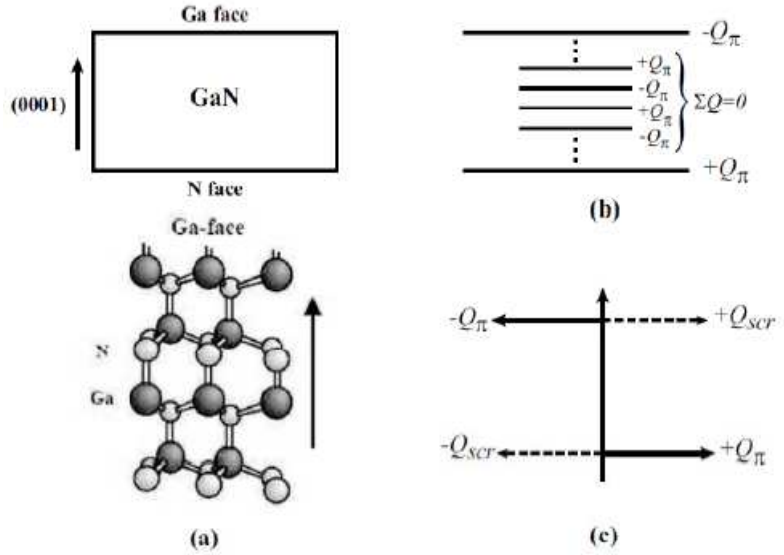

Figure 2.8: GaN Polarization and Polar Charge Compensation [10].

Actually there are some mechanisms tryng to let the system reach an equilibrium status, by compensating the polarization:

1. **Holes generation at the Surface**
2. **Donor States at the Surface**

We believe holes and donor states at the surface to be the source of electrons for the 2DEG formation. According to this theory, the amount of charge in the 2DEG can be modifyied by varying GaN thickness.

1. **Holes Generation at the Surface**

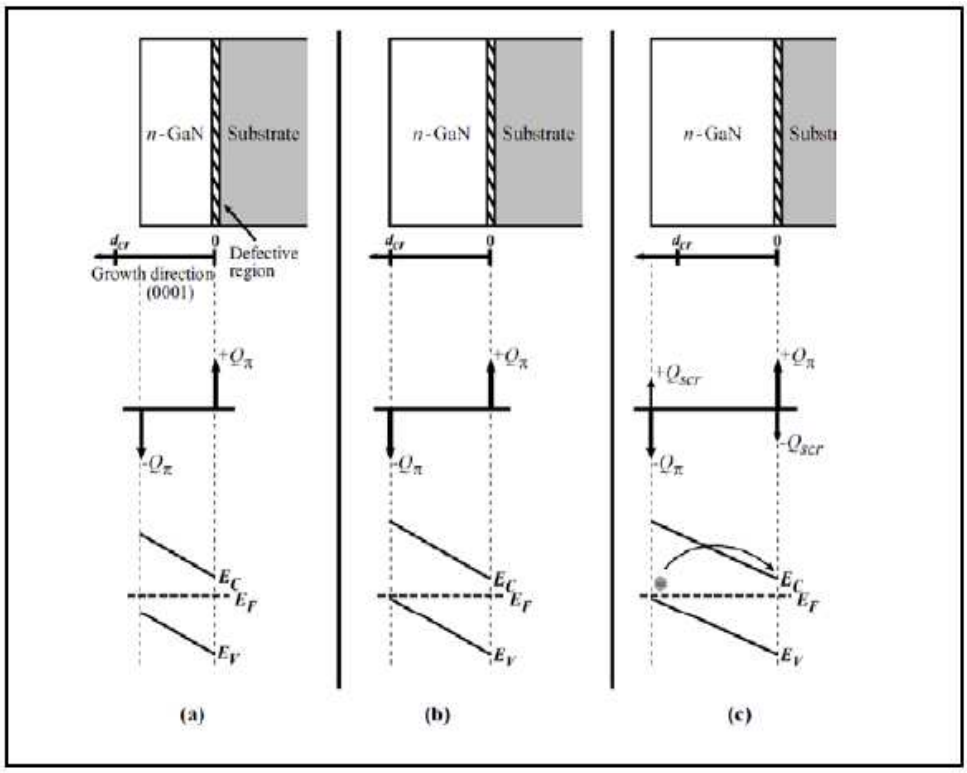

Figure 2.9: Holes Generation at the Surface [10].

When the GaN layer grows over the critical distance d_{cr} (fig. 2.9), the valence band E_v crosses the Fermi level, generating electron-hole pairs; the so generated electrons enter the conduction band, thus creating an additional charge ($+Q_{scr}$ and $-Q_{scr}$) in order to compensate the polarization charge($-Q_\pi$ on Ga-face and $+Q_\pi$ on N-face respectively) [10].

2. **Donor States at the Surface**

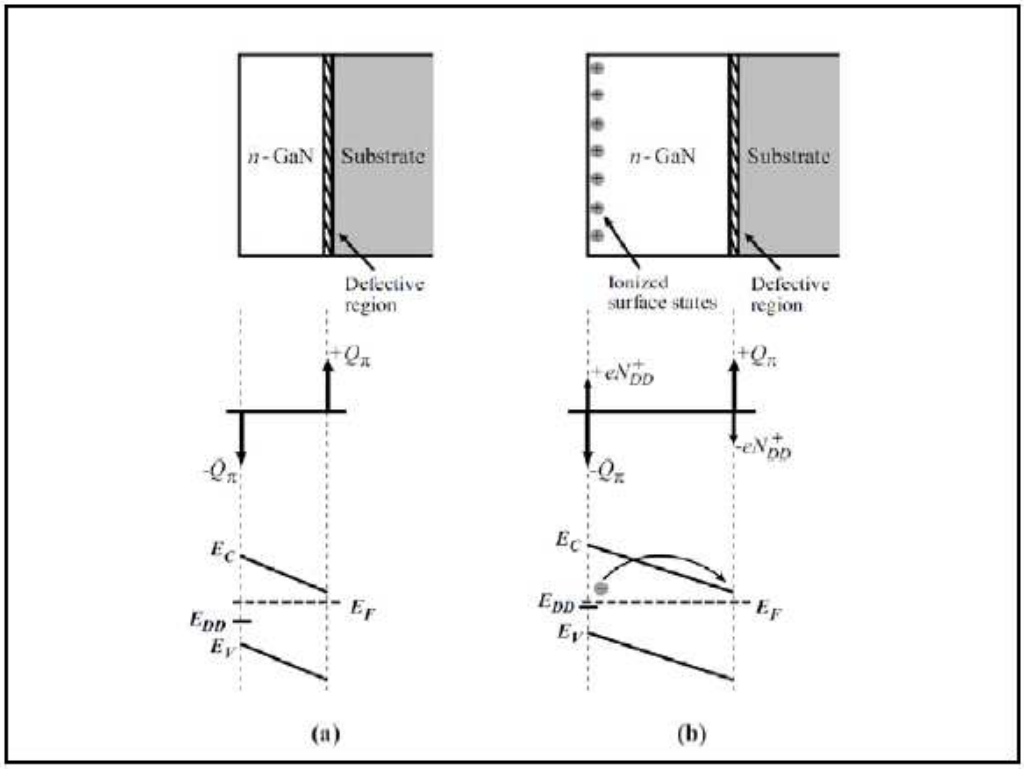

Figure 2.10: Donor States at the Surface [10].

On the GaN surface it is possible to deposit some donors states; they can be represented as allowed states inside the not allowed Energy Gap (fig. 2.10). If the GaN layer is large enough to let the energetic level of the donor states cross the Fermi Level, by letting electrons be free. The so generated electrons enter the conduction band, thus creating an additional charge ($+Q_{scr}$ and $-Q_{scr}$) in order to compensate the polarization charge ($-Q_\pi$ on Ga-face and $+Q_\pi$ on N-face).

While AlGaN thickness is growing, the carrier concentration in the 2DEG (n_s) grows fastly, until the buffer reaches the crytical thickness, then it does not increment anymore, but it even goes a bit down, due to crystal relaxing after mechanical strain [10].

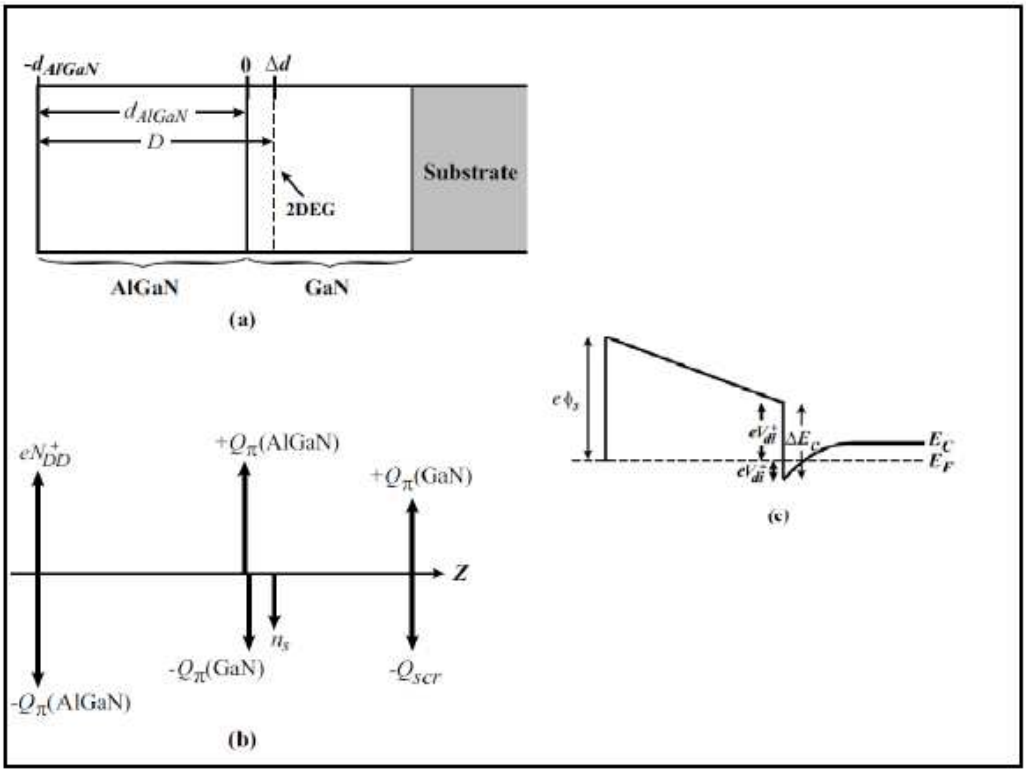

Figure 2.11: GaN HEMT's - 2DEG Formation [10].

In fig. 2.11 the structure, the polar charges and the band diagram of an AlGaN/GaN-HEMT are shown. Both GaN and AlGaN show polar charge at the surfaces (fig.2.11(b)). When the surface states are ionized (eN_{DD}^{+}), their charge is compensated by the generation of an additional charge in AlGaN : n_s and $-Q_{scr}$. Referring to (fig.2.11(b)), we can write the following equation, by using the charge balance principle [10]:

$$qN_{DD}^{+} = +Q_{\pi}(GaN) + n_s \tag{2.2}$$

where n_s represents the conduction channel inside the GaN-HEMT; this channel is actually a quantum-well (fig.2.11(c)) ,where electrons can freely move along two directions; for this reason it is called 2DEG (Two dimensional Elecron Gas). The 2DEG is formed only thanks to polarization mechanisms, thus doping is not needed, whereas in the AlGaAs/GaAs system the charge

in the channel is given by the doping.

As we said in section 1.1, the presence of a 2DEG in GaN-HEMT leads to a high maximum drift velocity ($fig.1.4$) and a relatively high electron mobility (fig. 1.3) ,thanks to the absence of scattering phaenomena between carriers.

Chapter 3

Current Collapse

One of the major effects that continues to limit the performance of GaN-based devices is the presence of electronic traps in the device structure. It has been proven that in AlGaN/GaN HEMTs the 2DEG in the channel is affected by the parasitic charge moving in and out of the traps on the surface and/or in the bulk of the heterostructure. GaN based-HEMT's are used for high power and high frequencies applications; this effect is thus really important and considerably limits the performances of this kind of devices: it is important to understand the origin of the traps in GaN-based transistors, their location, and the physical mechanisms involved, in order to optimize the device's performances.

3.1 Traps

Traps can be caused by defects in the material, that can be related to crystal defects, polluting agents and the mismatch between the different layers. At the interfaces between different materials and at the materials surfaces the periodicity of the crystal lattice ends and creates unbonded bonds. As for the band diagram, these defects are represented by allowed states inside the not allowed band gap: the so called *traps*. HEMT are built throw layers with different lattice constant and they are hepitaxially grown one on the other one, so that the trapping phenomenon is really significant. Traps create

a quasi-static charge distribution both on the wafer surface and inside the buffer below the channel : this leads to a reduction in the drain current and therefore to a limitation in the maximum output power at high frequencies. Moreover these states bring a delay in the device's performances, thanks to the trapping-detrapping effects, therefore limiting the maximum operating frequency. HEMT are widely used for microwave power amplifiers, for this reason the development of these devices has been strongly limited by this phenomenon.
In AlGaN/GaN HEMTS's traps can be set at the surface, inside the AlGaN, at the AlGaN/GaN interface or inside the buffer layer (fig.3.1). Depending

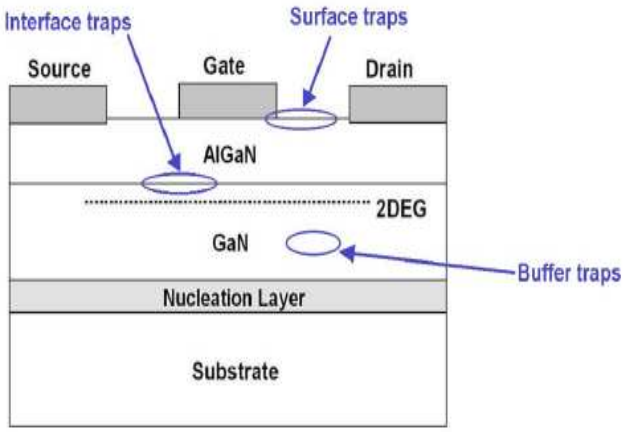

Figure 3.1: HEMT's Typical Traps Setting [25].

on the traps' location inside the device, they show different effects. Even if a considerable research effort has been directed towards the identification and elimination of traps in AlGaN/GaN HEMTs, the trapping processes in GaN are still not completely understood [21] [29].

3.2 Current Collapse

The main non-ideality of interest in GaN HEMTs has been variously referred to as current collapse, transconductance frequency dispersion and current slump. This is the most important problem that impacts GaN FET technology for high power applications. Current collapse is essentially the observation that the measured output power of the device at the frequencies of interest such as 4-18 GHz, is considerably smaller than that expected based on the equation

$$P = 1/8 * IDS_{MAX} * (V_{BREAKDOWN}) \tag{3.1}$$

where the values of IDS_{MAX} and V_{KNEE} are based on the values measured at DC. In fig 3.2 we show the measured DC and pulsed I-V characteristics, typical of a GaN HEMT that exhibits current collapse. The DC curves are measured using a Tektronix curve tracer. The pulsed measurements are made using the pulsed mode of the Tektronix curve tracer where the sequence of drain and gate biases is shown in figure 3.3 [Veturi 2000]. As can be seen from figure 3.2, there is a considerable reduction in the drain current, together with an increase in knee voltage, when measured under pulsed conditions. Current collapse is caused by the presence of deep levels or traps located in the device structure [28].

This phenomenon can be explained by considering that, when the transistor in normally operating and the channel is formed, the surface states behave as donors and their electron moves to the channel. In this way a positive charge distribution is formed on the AlGaN surface, in order to compensate the 2DEG's charge. If on the external surface there are electrons, this charge will be partially neutralized, so that we will see an electron's number reduction in the channel and an enlargement of the depletion region. When the channel is closed, infact, due to the high electrical field between gate and drain, the surface states are filled with negative charges coming from the gate. When the channel is opened again, the surface states are not able to come immediately back to the channel, because the trapping-detrapping

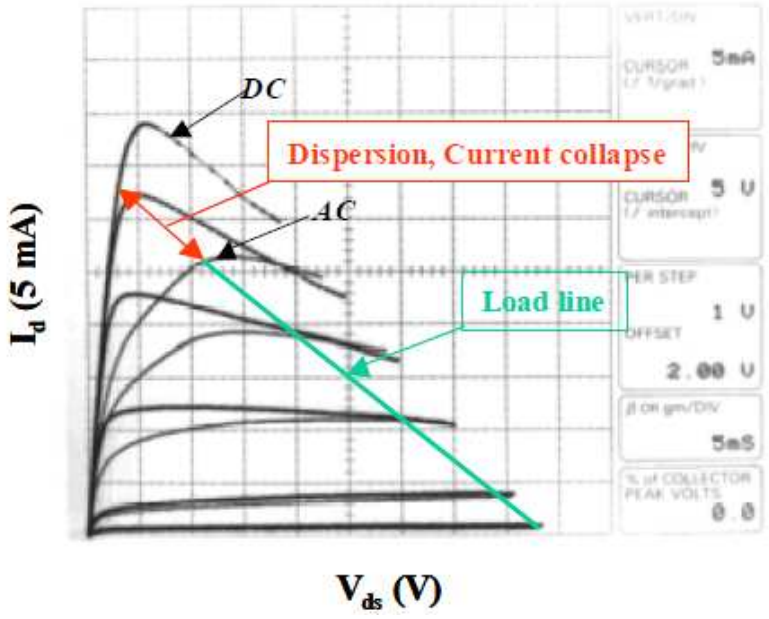

Figure 3.2: Typical DC and Pulsed I-V Characteristic of a GaN HEMT [28].

speed is much more smaller than the channel's formation speed (fig 3.4). This phenomenon brings an accumulation of negative charges, that keep the channel partially off, so that we can see a reduction in the drain current comparing to DC (fig.3.5). The current collapse effect is now explained by using the concept of **virtual gate** [28]: as for this model, a second gate electrode is inserted in series with the real one; the real gate is driven by the applied voltage, whereas the virtual one is driven by the quantity of charge trapped at the surface (fig. 3.6). The drain current is related to both the real gate's voltage and the mechanisms regulating the virtual gate's charge's movement. If we want the current to reach the nominal value, we can use a light source that, thanks to photons wiht energy higher than the GaN energy gap, gives birth to hole-electron pairs in the buffer layer. Holes are therefore moved by the electric field towards the surface, in order to make it positive biased and to eliminate the virtual gate. Nowadays some technics are used in order to eliminate the current collapse: the most common is the **surface passivation**, that is the deposition of a passivation film on AlGaN(fig.3.7),

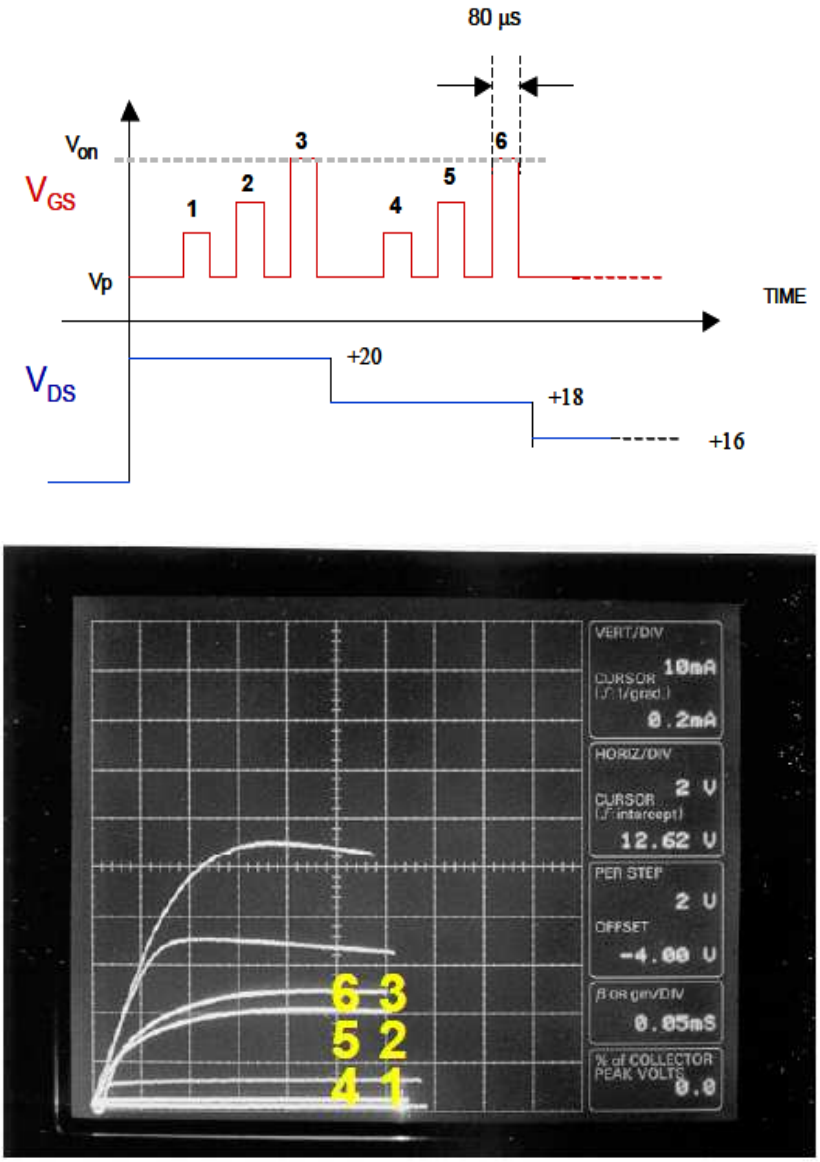

Figure 3.3: Sequence of Pulses used to obtain the Pulsed I-V Curves [28].

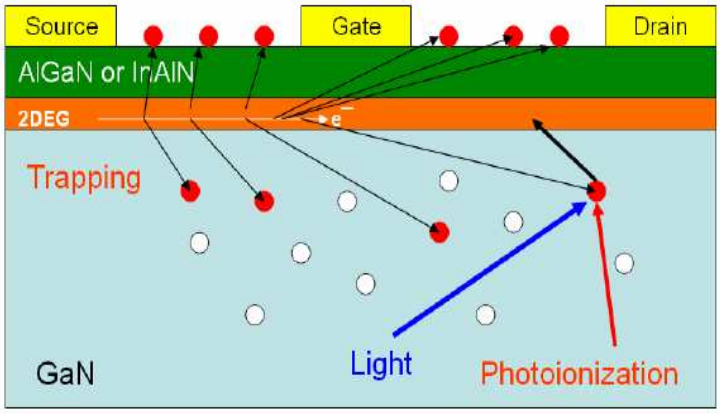

Figure 3.4: Schematic charge movement in and out of the traps on the surface and/or in the bulk of the heterostructure [18].

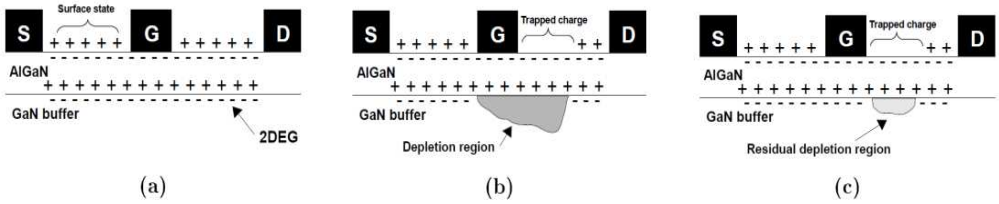

Figure 3.5: The Transconductance Frequency Dispersion Phaenomen in GaN HEMTs [11].

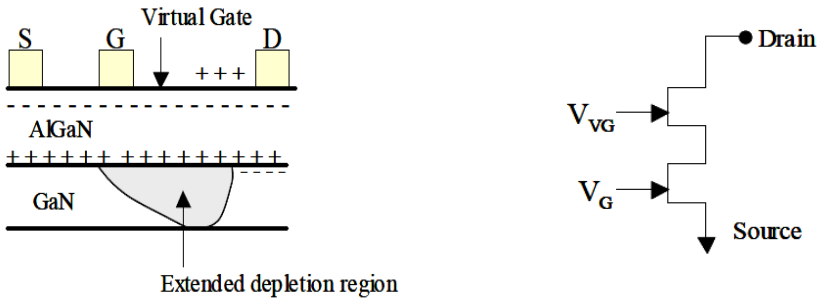

Figure 3.6: Model of device showing the Location of the Virtual Gate [28].

used in order to make superficial defects inert. The most common passivation

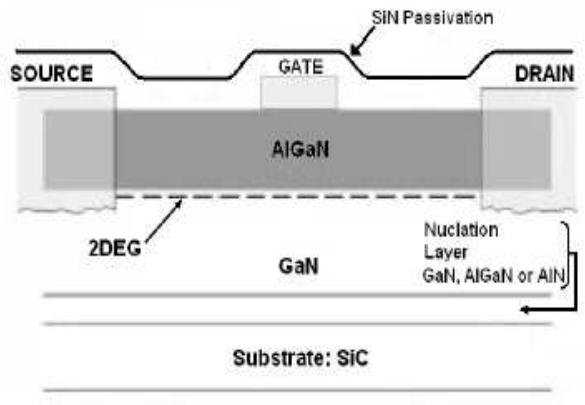

Figure 3.7: Surface Passivation on AlGaN/GaN HEMT [27].

material is Silicon Nitride (Si_3N_4). We build an almost perfect insulating material-semiconductor interface, in order to neutralize the superficial charge caused by unbonded bonds, defects, residual charges and to prevent electrons from reaching the surface. The final result depends on elements such as the surface, the quality of the material and the deposition process. In figure 3.8, it is shown the effect of SiN passivation on the DC characteristic: you can see how the passivation makes the current value increase, but without eliminating the current collapse effect. Another strongly diffused method, in order to reduce the current collapse, is the adoption of a **field plate**. This technique modifyies the gate's layout: in particular the gate has a T or Γ shape, in order to partly cover the gate-drain area (fig.3.9). The field plate gives us the possibility of reducing the maximum electric field between gate and drain, that is the main reason for charges to move from the gate towards the surface. The field plate infact limits the electric field peak and by makes it more homogeneous along all the field plate's length. We can find a huge benefit also in terms of device's degradation after stress: infact the electric field gets lower and the electrons are less sped up, so that all the degradation processes, linked to the presence of hot electrons, decrease. The field plate's design depends on elements such as length, thickness and type of material.

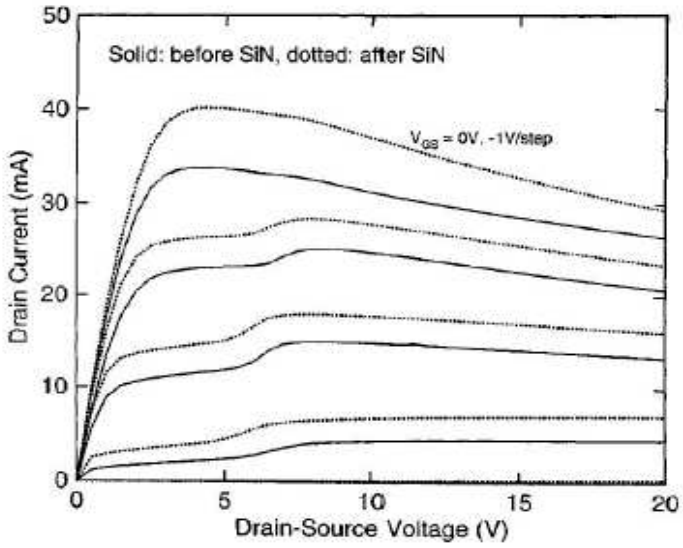

Figure 3.8: Drain Current before (solid line) and after (dotted line) Passivation [**?**].

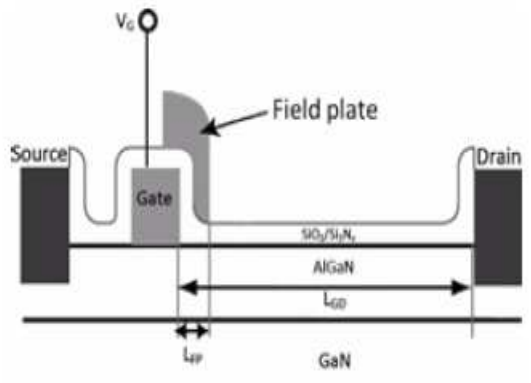

Figure 3.9: Field Plate in AlGaN/GaN HEMT.

Another Technique, called **Gate Recess**, is shown in figure 3.10 and it lets

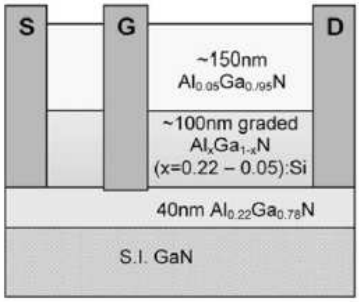

Figure 3.10: Gate Recess Structure [**?**].

us limit the superficial traps effects. The barrier layer is moved more deeply: in this way it is set under the AlGaN and Gan layers, in order to push the surface away from the channel, therefore limiting the current collapse effects, even without passivation.

In order to make the current come back to the nominal value, we can highlight the device: the light source must have an energy level closed to GaN energy gap or closed to the trap's activation energy. If it is possible to use light sources with different wavelength, we can find out the energy of every trap, by understanding which wavelengths are related to current recovery phenomena; moreover the time necessary to the current recovery gives us information about the traps' nature.

I will give an overview of the two electrical characterization techniques used to investigate the various trapping effects in GaN-based HEMTs. These techniques are commonly known as drain lag and gate lag experiments and allow us to discriminate between lateral and vertical trapping phenomena.

3.3 Drain Lag

A significant reduction in the drain current resulting from the application of a high drain-source bias voltage is known as drain lag (fig 3.11).The term drain lag is used to describe the transient in the drain current when the drain voltage is pulsed, while the gate voltage is held constant (fig 3.12) [28]. The

drain lag effect is supposed to be associated with traps located in the buffer layer and in the substrate. GaAs devices are usually fabricated on semi-

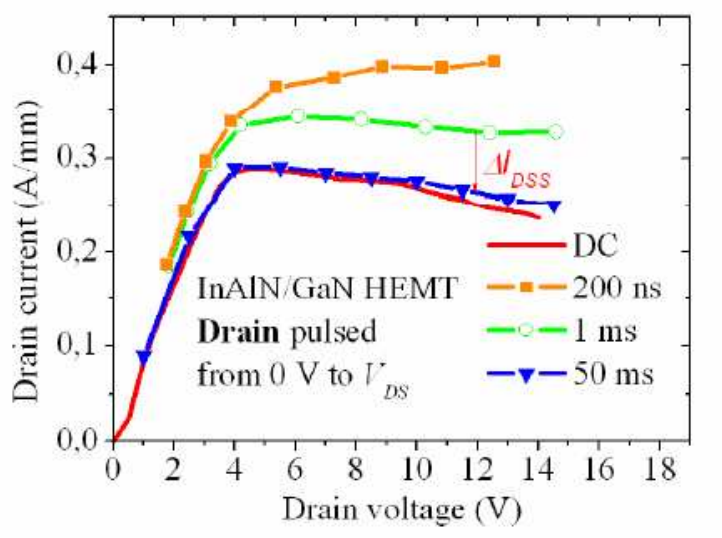

Figure 3.11: Drain-lag output characteristics of an InAlN/GaN HEMT with different pulses (1 ms 50 ms and 200 ns) and in DC. The drain is pulsed from 0 to VDS and the gate is grounded [18].

insulating substrates, which provide good isolation between devices in ICs and minimize parasitic capacitances. However, the semi-insulating nature of the substrate is achieved by impurity compensation by deep levels, which can give rise to transient effects. Although the surface trapping effects cause transient effects in drain currents, even devices with single and double gate recesses and passivated surfaces have exhibited drain current transients. For this reason, drain lag effects are commonly attributed to the substrate trapping effects too [28]. Binari et al. [22] were the first to correlate drain current collapse in GaN-based MESFETs with hot electron trapping by deep traps in the highly resistive GaN buffer layer. Further studies by Binari et al.[24] [23] suggested that the degree of the drain lag is related to the conductivity of the GaN buffer, which can be strongly influenced by the growth pressure. By studying the wavelength dependence of the drain current recovery in more details, no enhancement of the optically induced drain current recovery was

observed for photon energies at or below the AlGaN bandgap. It seems to be obvious that the drain lag in AlGaN/GaN HEMTs is caused by the same traps in the highly resistive GaN buffer layer that also is responsible for the drain lag in the GaN MESFETs [15] [14].

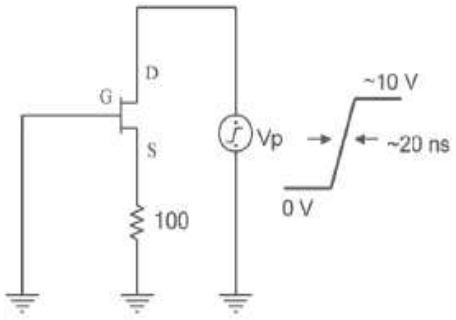

Figure 3.12: Drain-lag measurement schematic [6].

3.4 Gate Lag

The term gate lag is used to describe the slow transient response of the drain current when the gate voltage is pulsed [Veturi 2000] (fig 3.13). Figure

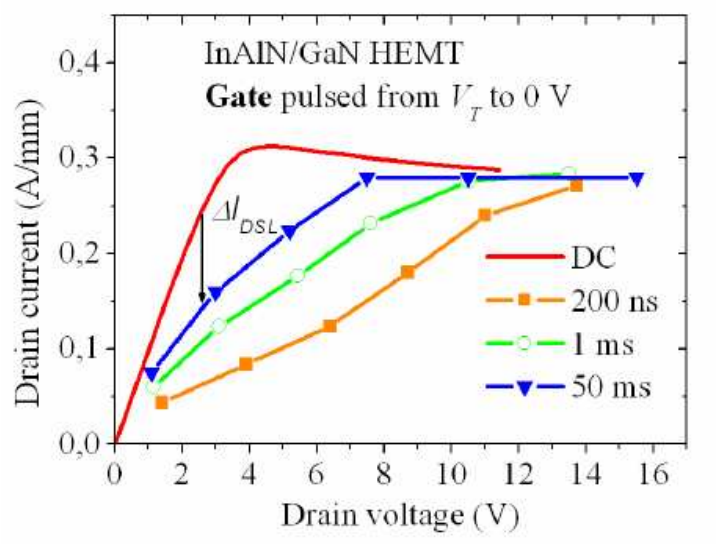

Figure 3.13: Gate-lag output characteristics of an InAlN/GaN HEMT with different pulses duration (1 ms 50 ms and 200 ns) and in DC. The gate is pulsed from VT (off-state) to VGS (on-state) and the drain is DC biased. Gate-Source voltage is VGS=0 [18].

3.14(a) shows the measurement schematic used to quantify gate lag. Fig 3.14(b) shows the movement of the device on the I-V plane. The FET is biased in common source mode and the gate voltage is pulsed from the pinch-off (or a negative value) to a varying final values. A low value of the drain load resistor is usually chosen to keep the drain voltage variation small and to avoid any effects caused by variation in substrate trap densities due to drain voltage variation. Fig 3.14(d) shows the sequence of input pulses and output responses. We refer to as *lag* if, when the gate is pulsed ON, the drain current is larger than its steady state and the drain current slowly reaches its steady state value. This phenomenon is attributed to both surface state as well as substrate deep trap effects. Various research groups have confirmed that drain current reduction during large signal operation at microwave fre-

quencies is mainly caused by electrons trapping phenomena at the unpassivated barrier surface. The effect of the surface states was explained for the first time by Ventury, where they used floating gates as potential probes to directly measure the surface potential along the gate-drain access region suggesting the presence of negative charges on the surface. This negative charges are responsible for a more negative surface potential which leads to a rapid extension of the gate depletion region [28].

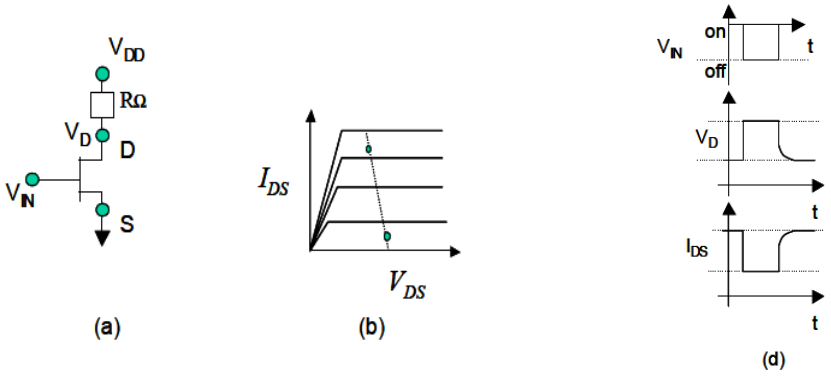

Figure 3.14: Schematic of Gate Lag Measurement [28].

3.4.1 Dynamic Rdson Measurement

As we said in section 3.4, the term gate lag is used to describe the slow transient response of the drain current, when the gate voltage is pulsed. As we can see in fig 3.13, the gate lag phenomen can also be defined as an increase in the dynamic Rdson value (measured under pulsed conditions), comparing to the static Rdson value (measured in steady state). According to this point, we can quantify the current collapse in the following way: we fix the value of the drain-source current to an arbitrary value, belonging to the linear region of the I-V characteristic; we monitor the v_{DS} drop between drain and source, under pulsed conditions, and we compare that with the v_{DS} drop measured in steady state. If $Vds_{DYNAMIC} > Vds_{STATIC}$, we will

have current collapse: according to the following expressions,

$$Rdson_{DYNAMIC} = \frac{Vds_{DYNAMIC}}{IDS} Rdson_{STATIC} = \frac{Vds_{STATIC}}{IDS} \tag{3.2}$$

in case of current collapse, since the drain-source current is constant, it will be $Vds_{DYNAMIC} > Vds_{STATIC}$, because $Rdson_{DYNAMIC} > Rdson_{STATIC}$. Therefore, when the gate voltage is pulsed, we can quantify the current collapse by monitoring the transient response of the v_{DS} drop between drain and source in on-state. As we said in sec 3.2, when the voltage applied to the drain of the device gives birth to an electric field between drain and gate big enough to let some electrons escape from the channel and be captured inside traps, then we will have current collapse: it will be $Rdson_{DYNAMIC} > Rdson_{STATIC}$ and so, thanks to our measurement setup, we will measure in increment in the vds value directly proportional to the degree of current collapse.

In fig 3.15, on the top, is shown the basic schematic we used for the Dynamic Rdson Measurements.

The gate is driven by a pulse generator, whereas the drain potential is held to a fixed voltage, given by the battery in parallel with the capacitance. The capacitance contributes to maintain the drain-source voltage at the value imposed by the battery, by avoiding any voltage over-undershoot coming from the battery. The drain resistance RD is used to fix the current that the device has to support. In fig 3.15 you can see the I-V characteristic of the device and the load line related to the drain resistance RD.
While the gate voltage is pulsed, the device continously switches from on to off-state. When the device is on, it works in the linear part of the I-V characteristic; in particular, the working point is represented by the intersection between the load line and the vertical axis. The drain-source current is fixed throw the drain resistance RD and is equal to $IDS = \frac{VDD}{RD}$, where VDD is the voltage applied by the battery to the drain of the device. The drain-source voltage drop, on the other side, is very small in this working point. When the device is in off-state, it works in the point in which the load line intersects the horizontal axis: $ID = 0$ and $VDS = VDD$.

Fig 3.16 shows how the Scope Screen appears during a Dynamic Rdson

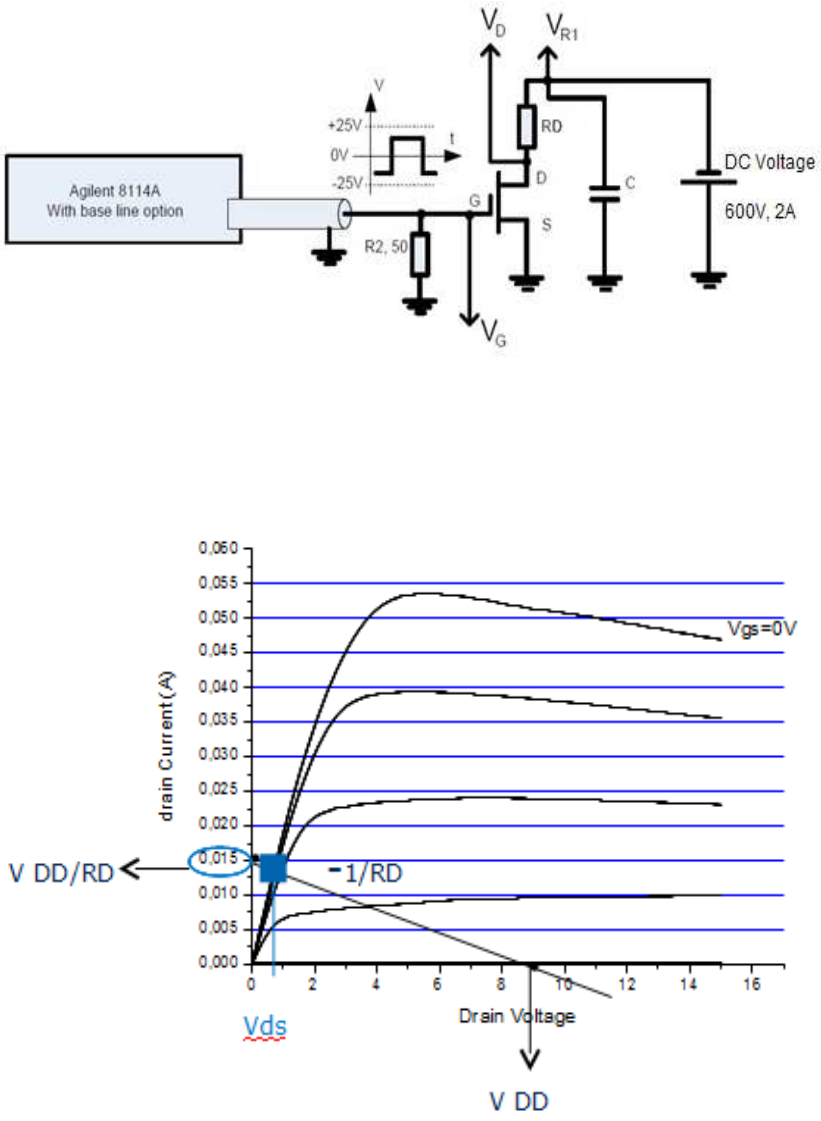

Figure 3.15: Dynamic Rdson Measurement Basic Schematic (on the top); output characteristic (on the bottom) with the load line related to the drain resistance RD.

Measurement. The gate voltage (yellow line) is pulsed from 0V to 5V, in order to keep the transistor switched on for a period of time equal to (i.e. $ton = 5\mu s$). The ton time chosen for the measurement depends on the application, therefore it is connected to the range of frequencies at which the device is supposed to operate.
When the device turns on, the drain-source current (purple line) goes up to the drain-source current value fixed throw the drain resistance RD, (in the example it is $IDS = 900mA$). The drain voltage (blue line) is equal to the voltage on the battery (VDD=450V) when the transistor is off , whereas it is very small when the device is turned on.
When the device is in off-state, the v_{DS} drop between drain and source is big, therefore we have an high electric field between drain and source, that let some electrons come out from the channel and be captured inside traps, mostly on the surface of the device (sec 3.2), even if a trapping effect in the buffer cannot be excluded. The toff time is therefore also referred to as *stress time* . The longer is the stress time, the bigger is the number of electrons trapped and the more it takes, when the device is switched on, to detrap them and let them free to come back to the channel.

When the gate voltage pulse opens the channel again, the electrons need some time to be detrapped: the current does not immediately reach the final value, but it takes a bit longer. This delay time is called *recovery time*. In our type of measurement the current is fixed, so that, by monitoring the drain-source voltage in on-state, we will see that it does not immediately rise to the final value, but it slowly decrements until reaching that. The period of time the drain-source voltage takes to reach the final value representes a limitation for the device: it stands for the maximum frequency at which the device can operate.

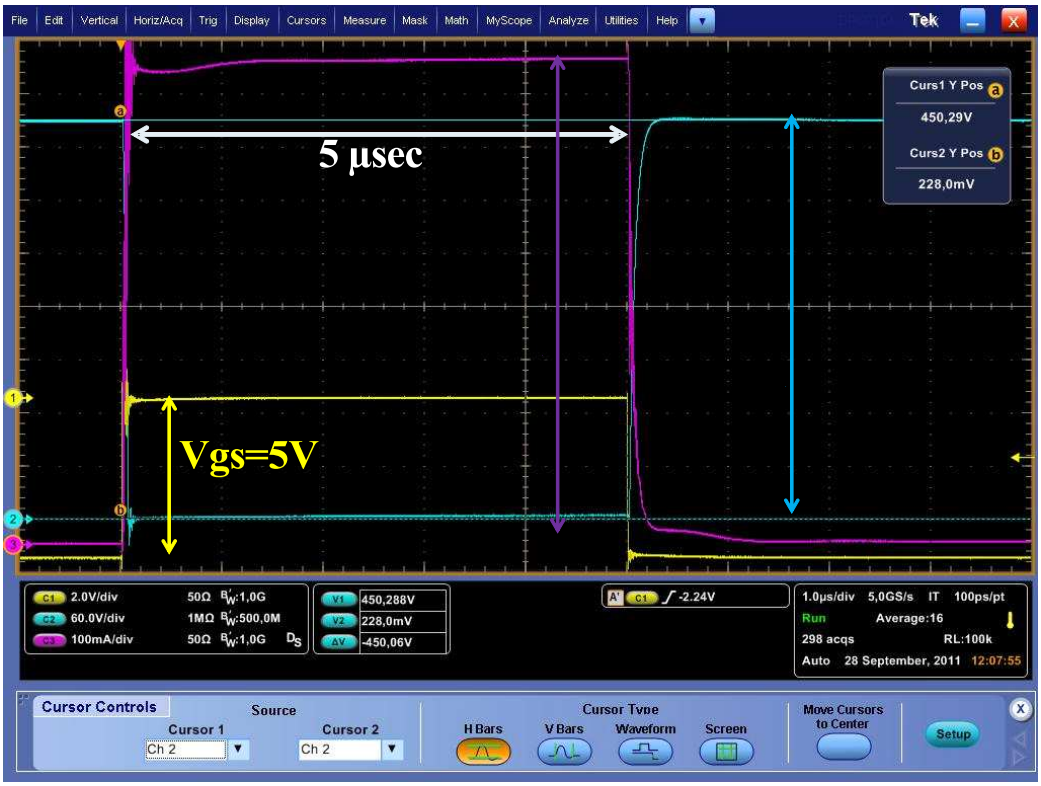

Figure 3.16: Scope Screen. Example of Dynamic Rdson Measurement. Vgs (yellow line), Vds (blue line), Id (purple line)

Chapter 4

Clamping Circuit

4.1 Problems Related with the Scope‘s Resolution

The resolution of an instrument is defined as the minimum value that the instrument is able to evaluate. In order to obtain an accurate measurement, it is important to have as much resolution as possible.newline Referring to the scope, both vertical and horizontal resolution are defined; they are related to the vertical and horizontal number of divisions of the scope, respectively.

The scopes vertical resolution is related to the number of quantization levels of the ADC converter inside the scope; it is defined as follows:

$$VerticalResolution = R = \frac{VBUS}{2^b} = \frac{VBUS}{2^8} = \frac{VBUS}{256} \qquad (4.1)$$

where VBUS indicates the maximum voltage value of the signal to be measured, whereas “b” stands for the number of bit of the ADC converter, usually equal to 8 in digital scopes; this means that the read signal is quantized on $2^8 = 256$ levels.

In fig 4.1, 4.2 and 4.3 you can see the drain-source voltage signal of a silicon MOSFET, measured under pulsed conditions and stressed with different values of drain-source voltage in off-state(VBUS) [4]. The yellow waveforms

on the top indicate the typical and correct signals we should see on the scope's screen, whereas, in the graph on the bottom, the blue waveforms indicate the signals we actually measured. We want to evaluate the value of the drain-source voltage drop in on-state in corrispondence with the end of the v_{GS} pulse (fig 3.16); for example, referring to fig 3.16, if the vgs pulse lasts $5\mu sec$, we will evaluate the degree of current collapse at $f = \frac{1}{5\mu sec} = 200KHz$.

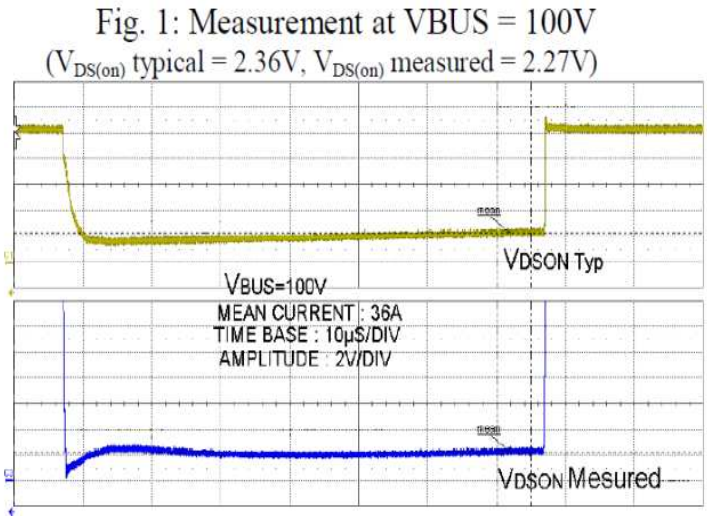

Figure 4.1: Problems with the vertical resolution of the scope. $R = \frac{VBUS}{256} = \frac{100V}{256} = 390mV$: at VBUS=100V the v_{DS} measured is correct [4].

As for fig 4.1, the right v_{DS} value we should measure is $v_{DS} \approx 2.36V$. As you can see in fig 4.1, when the v_{DS} voltage in off state is equal to 100V, we actually measure $v_{DS} = 2.27V$ in on-state, therefore we can consider the measurement to be correct. In this case, if we calculate the vertical resolution of the scope, it is $\frac{VBUS}{256} = \frac{100V}{256} = 390mV$. 390mV infact represents a good resolution to measure 2.27V. This is the reason why the measurement is correct.

Now let us give a look to fig 4.2, where the v_{DS} voltage in off state is equal to $VDD = 200V$. In this case, if we calculate the vertical resolution of the scope, it is $R = \frac{VBUS}{256} = \frac{200V}{256} = 780mV$. 780mV does not represent anymore a perfect resolution to measure 2.27V, therefore the v_{DS} measured

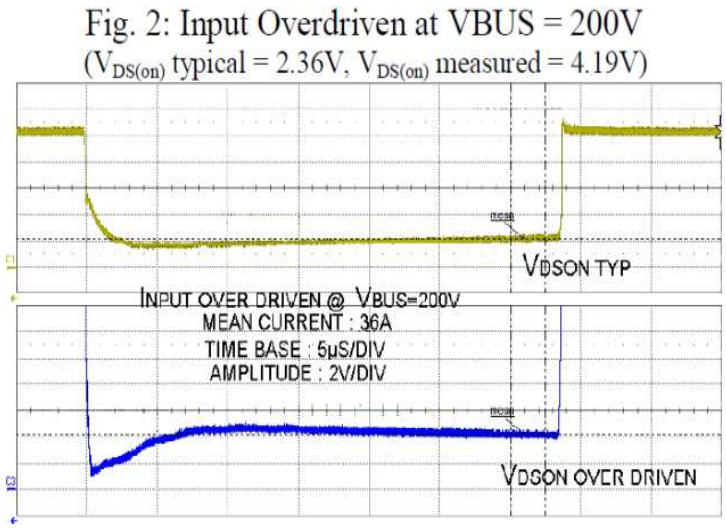

Figure 4.2: Problems with the vertical resolution of the scope. $R = \frac{VBUS}{256} = \frac{200V}{256} = 780mV$: at VBUS=200V the v_{DS} measured is 1.9V too high [4].

is too high, comparing with the typical value.

In the end, regarding fig 4.3, where the v_{DS} voltage in off state is $VDD = 400V$, we actually measure $v_{DS} = 11.03V$, therefore the measurement is completely wrong. In this case, infact, if we calculate the vertical resolution of the scope, it is $R = \frac{VBUS}{256} = \frac{400V}{256} = 1.6V$, that is too small in order to measure 2.27V, therefore the evaluated v_{DS} is completely wrong.

According to this observations, we can say that the larger is the range of values of the signal on the scope, the worse will be the measurement's accuracy. Reagarding the the v_{DS} signal, there is a huge step between the small value of v_{DS} in on state we want to evaluate (in the order of mV or few volts) and the value of v_{DS} in off state, VBUS, during the stress period. Actually we want to measure the value of v_{DS} in on state, regardless to the value of v_{DS} in off state: we would like somehow to cut the upper part of the v_{DS} signal, in order to have a higher accuracy on the value of v_{DS} in on state we are interested in. The solution to use is the so called *clamping circuit*,

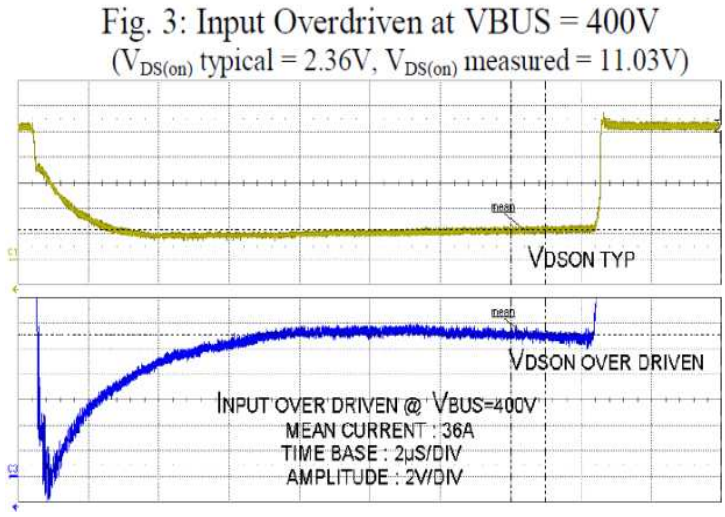

Figure 4.3: Problems with the vertical resolution of the scope. $R = \frac{VBUS}{256} = \frac{400V}{256} = 1.6V$: Between 200V and 400V the scope input amplifier is substantially overdriven and the results are definitely wrong [4].

that gives us the possibility of measuring a clamped value of the drain-source voltage: v_{DS}clamped, instead of v_{DS}. The schematic of the clamping circuit will be shown in a more detailed way in section 4.2.

4.2 Clamping Circuit - Schematic

The schematic of the clamping circuit we used is shown in fig 4.4 [8]. The GaN device under measurement (DUT) is put in parallel with an NMOS. In series with the NMOS there are a zener diode and a small reistance R1. The DUTs v_{DS}clamped is the voltage drop measured across the series composed by the zener diode and the resistance R1, present for safety reasons, as it is indicated in fig 4.4. The gate potential of the NMOS is driven by a power supply (V_{gate} in fig 4.4), that gives about 7V DC , in order to have $V_{GS_{NMOS}} \approx V_{th} \approx 2V$ continously, therefore a small drain-source current is flowing throw the NMOS device, when it is in on-state. The gate driver's power supply is followed by a low pass filter.

The I-V characteristics of the NMOS and of the zener diode, shown in fig 4.5, can help us to better understand how the circuit works. Let us study separately what happens when the GaN DUT is in on or in off-state.
When the DUT is switched off, the voltage drop between drain and source is equal to the voltage VBUS, provided by the drain battery shown in fig 3.15; therefore the NMOS is switched off and supports quite all the drain-source voltage drop across the GaN DUT. For this reason we chose an NMOS with a very high breakdown voltage, equal to 800V. The NMOS's drain-source current is flowing also throw the zener diode, therefore the zener diode is working in the breakdown region with $V_{zener} \approx 5.1V$ (in case of a 5.1V zener diode). The GaN DUT drain-source voltage drop is then shared by the NMOS and the zener diode (the voltage drop on the resistance R1 can be considered negligible, since the current flowing throw the NMOS is very small).
On the other hand, when the GaN DUT is in on-state, the drain-source voltage drop on it is very small; therefore the NMOS is switched on and both the drain-source current flowing throw it and the drain-source voltage are very small (NMOS I-V characteristic in fig 4.5). As for the zener diode's I-V characteristic, the voltage measured on the zener diode is exactly equal to the v_{DS} drop on the GaN DUT.
In this way, when the GaN device is switched on, v_{DS}clamped gives exactly the v_{DS} drop across the GaN DUT, whereas, when the GaN device is off, v_{DS}clamped is limited to the breakdown voltage of the zener diode we are using; in this case Vz= 5.1V.

In fig 4.6 and 4.7 are shown the v_{DS} measurements made on a silicon $90m\Omega$ coolMOS device without clamping circuit (waveforms on the left in fig 4.6 and then with clamping circuit (waveforms on the right in fig 4.6. In fig 4.6 the waveforms at the first sight seem to have the same level of accuracy . In fig 4.7 you can see the same waveforms shown in fig 4.6, respectively, but zoomed: here you can notice the huge difference between the measurements with and without clamping circuit. In the measurement without clamping circuit, infact, due to the low vertical resolution, the scope is not able to distinguish between different quantized values; when the clamping circuit is

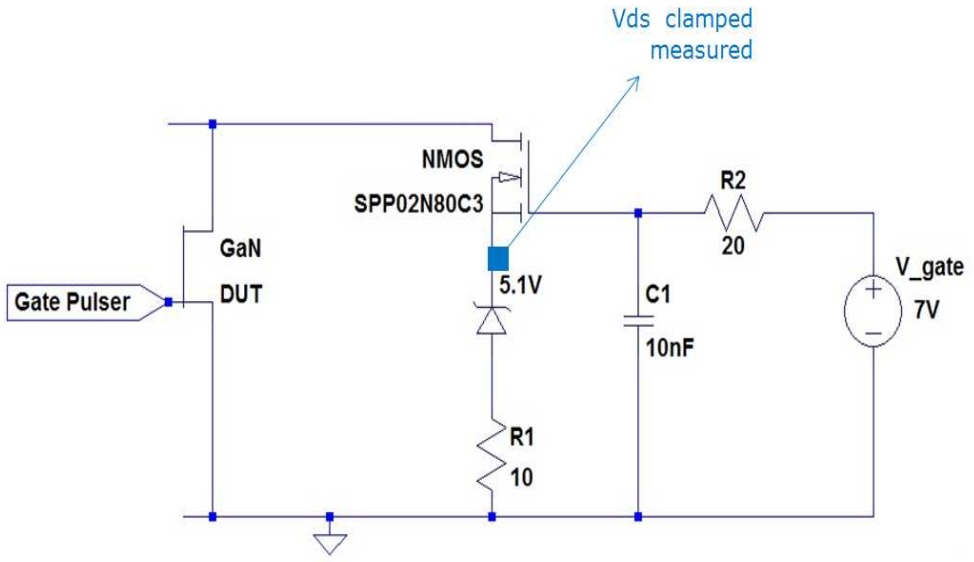

Figure 4.4: Clamping Circuit's Schematic.

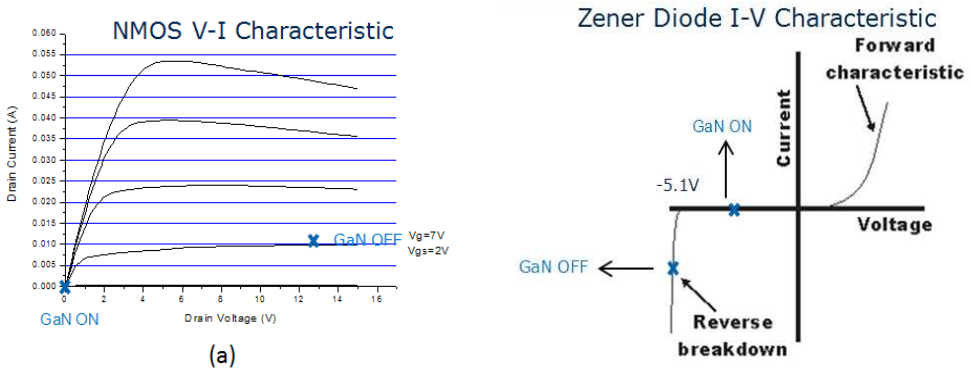

Figure 4.5: I-V Characteristic of the NMOS (a) and I-V characteristic of the Zener diode (b) used in the clamping circuit in fig 4.4.

used, vice versa, the signal's value is very clear.

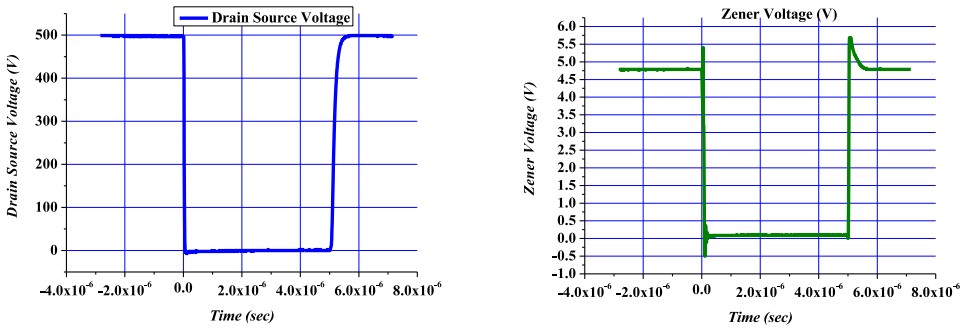

Figure 4.6: Drain-source voltage drop v_{DS} measured under pulsed conditions in a silicon coolMOS device, without using the clamping circuit (on the left) and with the clamping circuit (on the right).

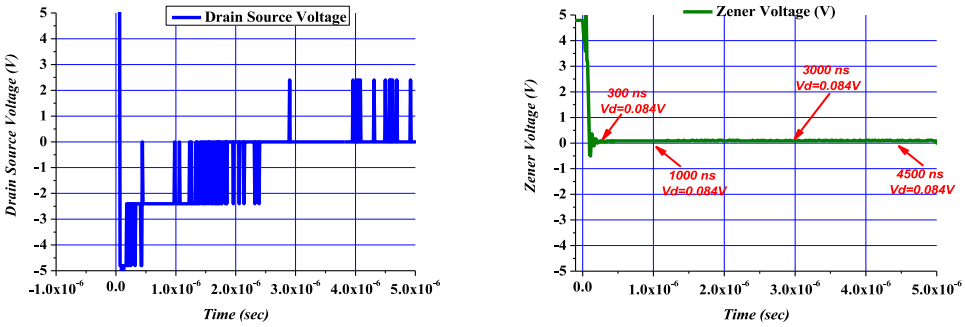

Figure 4.7: Zoomed drain-source voltage drop v_{DS} measured under pulsed conditions in a silicon coolMOS device, without using the clamping circuit (on the left) and with the clamping circuit (on the right). The CollMOS static Rdson measured at VGS=10V and IDS=1A is $StaticRdson = 87.73m\Omega$

The graph in fig 4.8, moreover, shows a comparison between the Rdson values of a silicon and of a GaN device, calculated with and without using the clamping circuit. We can see the high accuracy of the measurement that we obtain thanks to the the clamping circuit, comparing to the measurement of v_{DS} without that. The signal evaluated without clamping circuit, infact,

is completely wrong.

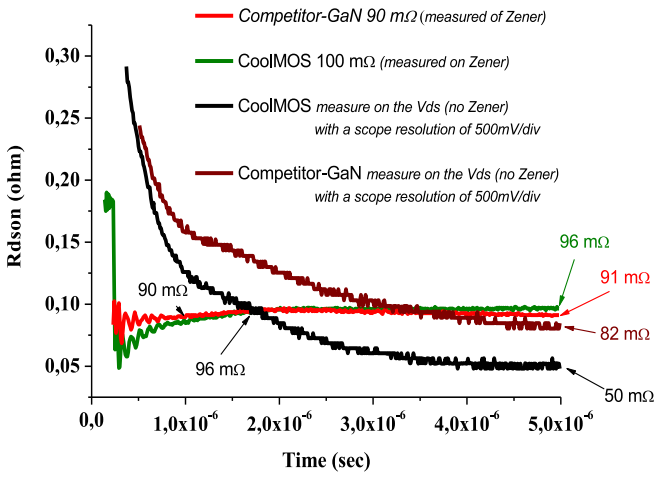

Figure 4.8: Comparison between the drain-source voltage of two different devices (a silicon device and a Gan device) measured under pulsed conditions with and without clamping circuit.

In order to understand how much our measurement is accurate, we have measured the static Rdson of a $90m\Omega$ silicon coolMOS device for different values of the drain-source current; then we have compared that with the dynamic Rdson, measured with our dynamic rdson setup in quasi-static conditions, by using the clamping circuit. We measured the static Rdson value thanks to a particular machine capable of a very high accuracy (fig 4.9). By applying 10V between gate and source and by using different values of drain-source current we obtained:

- $IDS = 10A \rightarrow Rdson = 88.53m\Omega$
- $IDS = 7.5A \rightarrow Rdson = 87.71m\Omega$
- $IDS = 5A \rightarrow Rdson = 86.82m\Omega$
- $IDS = 1A \rightarrow Rdson = 83.75m\Omega$

Figure 4.9: Static Tester M3020 used for measuring the static Rdson.

In fig 4.10, on the left, you can see the comparison between the static Rdson, measured with our static tester, and the one measured with our setup in quasi-static conditions for $I_{DS} = 10A$. The scopes vertical resolution is $R = \frac{VBUS}{256} \approx \ frac6V256 = 23V$. Since the current is equal to 10A, the device has $R_{DSon_STATIC} = 88.53m\Omega$, therefore the drain-source voltage drop I want to measure is $v_{DS} = 885.3mV$; then the error mistake is negligible and equal to $e = \frac{89.4-88.53}{88.53} = 0.97\%$.

Referring to the same type of measurement in fig 4.11, since the current is 7.5A, and the device has $R_{DSon_STATIC} = 87.71m\Omega$, the drain-source voltage drop I want to measure is $v_{DS} = 657.8mV$; then the error mistake is very small, as in the previous case, and equal to $e = \frac{86.47-87.71}{87.71} = 1.73\%$.

Again, referring to fig 4.12, since the current is 5A, and the device has $R_{DSon_STATIC} = 86.82m\Omega$, the drain-source voltage drop I want to measure is $v_{DS} = 433.1V$; the error mistake I make is therefore quite small and equal to $e = \frac{87.71-86.82}{86.82} = 2\%$. As for a general agreement, a measurement is supposed to be correct until the error is $e < 2\%$.

In the end, in fig 4.13, you can see the R_{DSon_STATIC} measured for $IDS = 1A$. Since the current is 1A and the device has $R_{DSon_STATIC} = 83.75m\Omega$, the drain-source voltage drop I want to measure is $v_{DS} = 83.75V$; the error mistake is therefore very big and equal to $e = \frac{97.21-83.75}{83.75} = 13.8\%$.

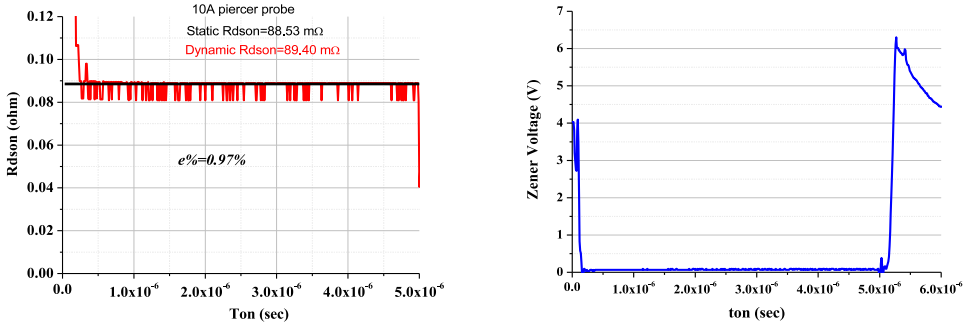

Figure 4.10: Comparison between the static Rdson measured with the machine (black line) and the dynamic rdson measured with our setup and with the clamping circuit in quasi-static conditions (red line) with $I_{DS} = 10A$ (on the left); v_{DS}clamped (on the right).

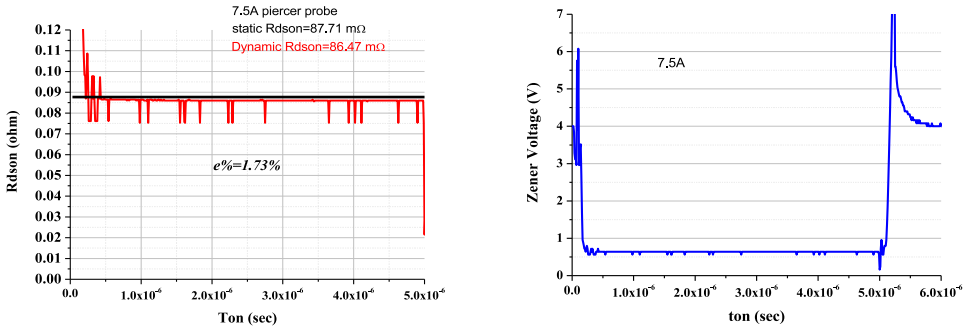

Figure 4.11: Comparison between the static Rdson measured with the machine (black line) and the dynamic rdson measured with our setup and with the clamping circuit in quasi-static conditions (red line) with $I_{DS} = 7.5A$ (on the left); v_{DS}clamped (on the right).

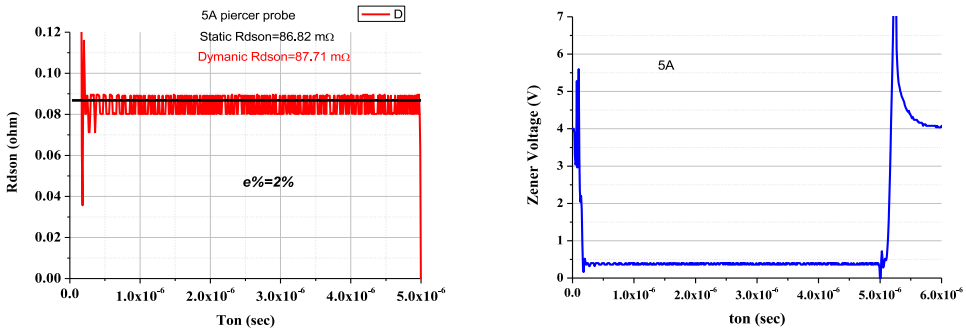

Figure 4.12: Comparison between the static Rdson measured with the machine (black line) and the dynamic rdson measured with our setup and with the clamping circuit in quasi-static conditions (red line) with $I_{DS} = 5A$ (on the left); v_{DS}clamped (on the right).

As we can see from these datas, the bigger is the drain-source current, the bigger is the error I make by measuring v_{DS}clamped and, therefore, Rdson. This error is clearly related to the limitation of the scopes vertical resolution: if the resolution is equal to $R = 23mV$, when the value I have to evaluate is in the range of 600-400mV, the result is accurate and the error I make is as maximum equal to $e = 2\%$; whereas, for smaller values of the drain-source current, the v_{DS}clamped to be measured is smaller than 100mV, therefore my measurement is for sure less accurate, because the value I am evaluating is comparable with the vertical resolution.

Even though the clamping circuit is a very strong ally, errors and imperfections unfortunately belong to every measurement, we can only try to cut them down, but we will never manage to remove them completely. Until now we have used a 5.1V zener diode for our clamping circuit. What we can do, in order to improve our accuracy, also in case of low drain-source currents, is using a zener diode with a smaller brakdown voltage.

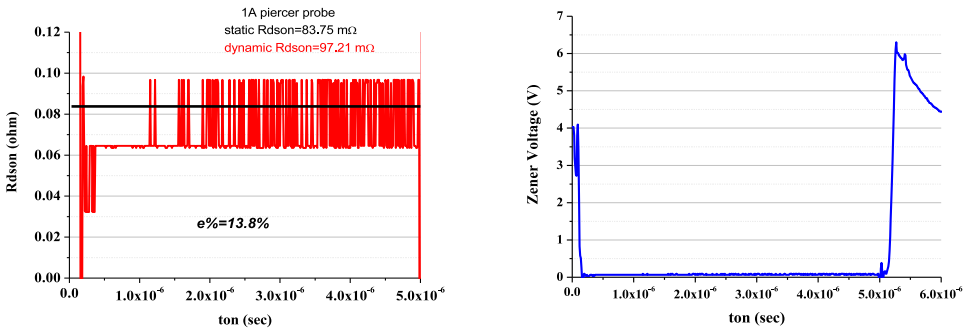

Figure 4.13: Comparison between the static Rdson measured with the machine (black line) and the dynamic rdson measured with our setup and with the clamping circuit in quasi-static conditions (red line) with $I_{DS} = 1A$ (on the left); v_{DS}clamped (on the right).

Chapter 5

GaN DReaM - GaN Dynamic Rdson Measurement Setup

5.1 The Old Dynamic Rdson Measurement Setup

In this chapter we want to better understand how our dynamic Rdson measurement setup is build and how it works.

In fig 3.15 is shown a very simple schematic of the dynamic Rdson measurement circuit we used. Referring to fig 3.15, the drain potential of the device under test (DUT) is continously connected to the main power supply, so that, when the device is in off-state, it is continously stressed with a drain voltage value that can go up to 600V (maximum output voltage for our power supply Agilent N5752A); in the real circuit we inserted a switch between the power supply and the DUT, so that the DUT is connected to the main power supply only for a short period of time, that is equal to the sum of the stressing time(t_{off}) and the on-time t_{on} of the DUT (fig 5.1); after this time period the coolMOS is switched off, so that the device can have a rest before that the next stress time starts. Let us give a look to fig 5.1: here we can see the same circuit shown in fig 3.15, but with a new part circled in red: we introduced infact a high breakdown voltage coolMOS silicon device

(Q1), put in series with the main power supply, with the aim of limiting the stress time of the DUT. The coolMOS Q1, infact, behaves as a switch: it lets the current flow from the power supply to the DUT while Q1 is in on-state, whereas, while Q1 is switched off, the drain of the DUT is disconnected from the power supply and the coolMOS Q1, thanks to its high breakdown voltage, can support up to 650V. As for the on-state drain-source voltage drop on the coolMOS Q1, it is negligible, infact $Rdson\_coolMOS = 37m\Omega$; let us make a fast calculation in the worst case, by considering $IDS_{max} = 20A$ we obtain:

$$VDS\_CoolMOS\_max = IDS_{max} * Rdson = 20A * 37m\Omega = 0.74V \quad (5.1)$$

value that, in comparison with the output voltages we set on the main power supply (from 25V up to 600V), can be considered negligible.

A much more detailed schematic of the circuit in fig 5.1 is shown in fig 5.2. The gate of the coolMOS Q1 is driven by the output of a gate drive optocoupler. The optocoupler is driven by the channel A of the BNC 575 Pulse Delay Generator, shown in fig 5.3(a), that therefore gives the switch-on and switch-off times of the coolMOS Q1.
Now let us understand how the BNC instrument works: the BNC 575 Pulse Delay Generator is an instrument with different output channels; on every channel it can deliver a square wave signal; the square wave period, that is the same for every channel, can be set by the user. The instrument, moreover, gives the possibility of synchronizing each channel with another channel of the instrument or with an external signal. In every channel, furthemore, you can insert a delay with respect to the synchronization source. This instrument owns a very high precision, infact it is possible to define the width of the pulse or the delay of every channel, with respect to the synchronization source, by using up to 15 decimal digits.
After have understood how the BNC instrument works, let us come back to the description of the dynamic Rdson measurement circuit in fig 5.2: the gate drive optocoupler is supplied throw a 15V DC/DC converter, connected to an auxiliary 12V power supply. The 15V DC/DC converter, shown on the

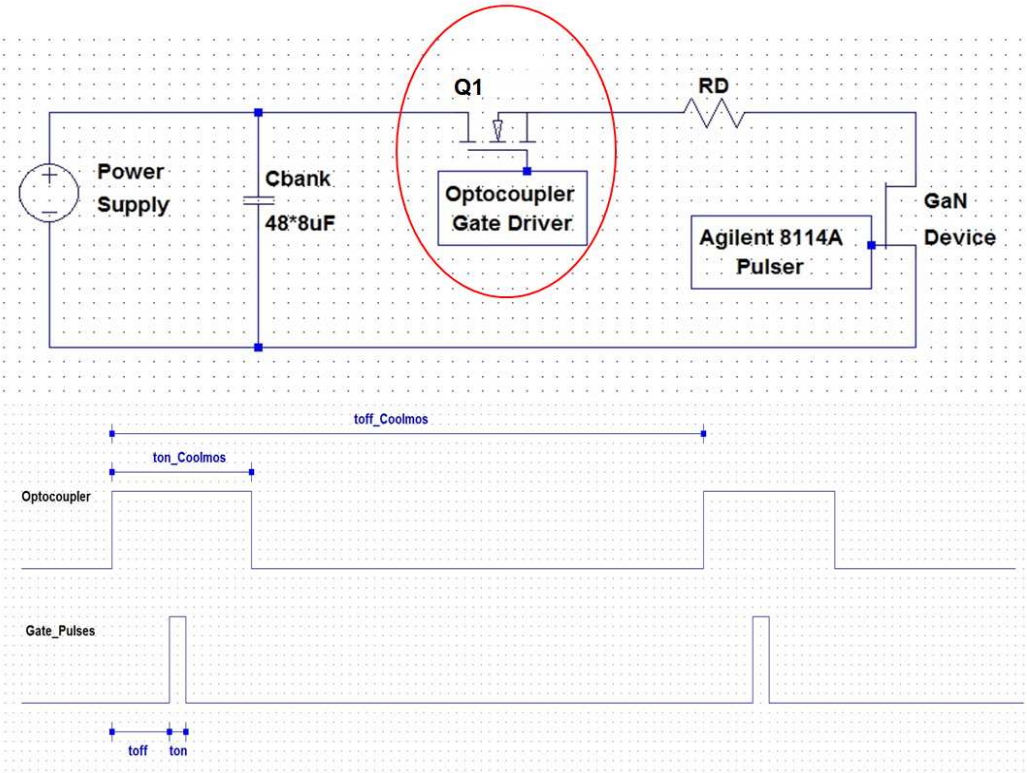

Figure 5.1: Dynamic Rdson Measurement Circuit Schematic. The switch Q1 has the aim of avoiding to stress too much the GaN DUT with the continous voltage coming from the main power supply.

bottom part in fig 5.1, gives us the possibility of galvanic isolation of the 12V auxiliary power supply. The two capacitances connected to the optocoupler‘s 15V supply terminal have the aim of mantaining the optocoupler‘s voltage constant, with the aim of avoiding voltage overshoot, that could damage the optocoupler itself.
Now we would like to understand how the gate signal of the DUT is driven: we would like the gate signal to come directly from the BNC 575 Pulse Delay Generator, in order to synchronize the gate signal with the coolMOS Q1 and to minimize the number of instruments used. Unfortunately the BNC instrument is not capable of delivering pulses with negative amplitude, so that we cannot directly drive normally-on devices by using one channel of the BNC instrument. Since that, the DUT‘s gate potential comes from the output of the Agilent 8114A Pulser (fig 5.3(b)), capable of delivering both positive and negative voltages. The output signal of the Agilent Pulser is triggered with the channel C of the BNC 575, that gives the delay time (t_{off_VGS}) and the width (t_{on_VGS}) of the gate signal. The on-time and off-time of the coolMOS signal are given by the channel A of the BNC instrument: this in order to have the possibility of synchronizing the gate signal with the Q1 signal, by syncronizing channel C with channel A. On the bottom part in fig **??** you can see an example of the gate signal and of the signal associated with the on and off-time of the coolMOS Q1: when the coolMOS signal pulse is up, it means that the device is in on-state and, vice versa, when the signal pulse is down, it means that the device is in off-state. As you can see in fig 5.1, Q1 is in on-state only during the time necessary to cover the delay time(t_{off_VGS}) and the width(t_{on_VGS}) of the gate signal, in order to avoid stressing too much the DUT.

In fig 5.4 is shown the top view and the side view of the first Dynamic Rdson Measurement setup we used. In pink you can see the block of capacitance, in parallel with the main power supply. The capacitance is composed by eight capacitors of $8\mu F$ eachone. They are mounted in parallel on two copper bars, therefore the total capacitance value is:

$$C_{bank} = 8 * 8\mu F = 64\mu F \tag{5.2}$$

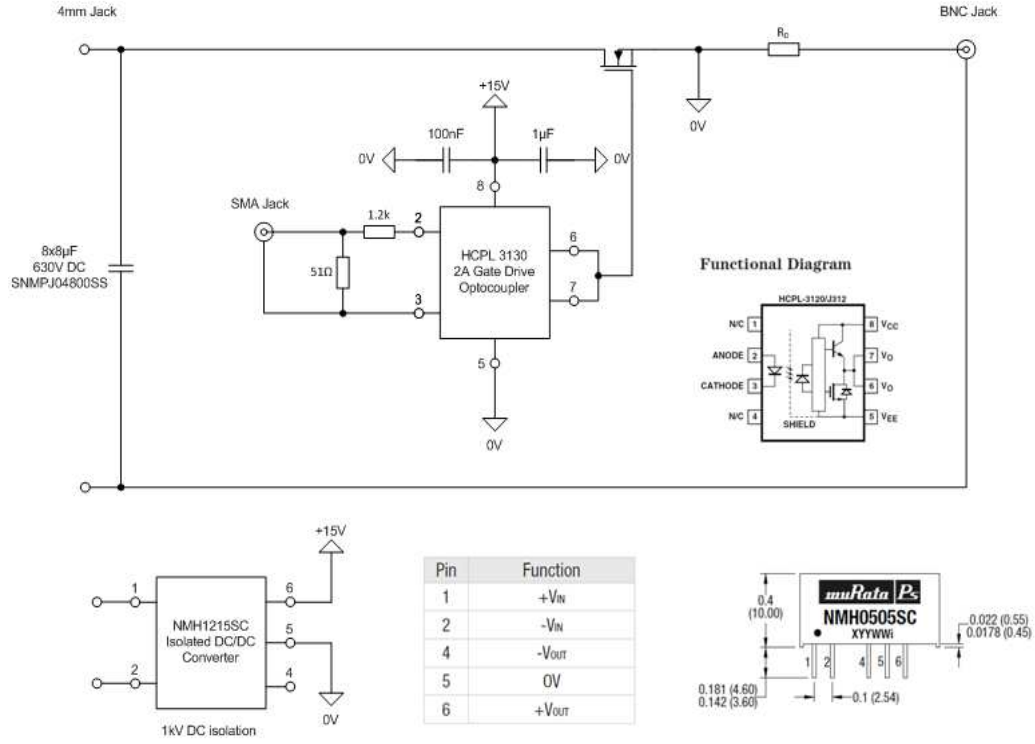

Figure 5.2: Dynamic Rdson Measurement Circuit Schematic. Here you can see how the gate driver of Q1 works (on the top). Then (on the bottom) the schematic of the DC/DC converter is shown.

Figure 5.3: Some instrument we use in the setup are shown here: BNC 575 Pulse Delay Generator(a) and Agilent 8114A Pulser(b).

On the pcb in fig 5.4 the other components of the circuit in fig 5.2 are mounted: here infact we can find the coolMOS Q1, the optocoupler, the DC/DC converter and the drain resistance RD.
According to eq 5.3, every time we set a new value for the drain-source current flowing throw the DUT or for the voltage delivered by the main power supply, the resistance RD has to be manually changed :

$$RD = \frac{VDD}{IDS} \tag{5.3}$$

where VDD is the voltage delivered by the main power supply and applied on the drain of the DUT.
Regarding to fig 5.4 the main power supply is connected across the two copper bars, throw the two connectors shown on the right side in fig 5.4(a).

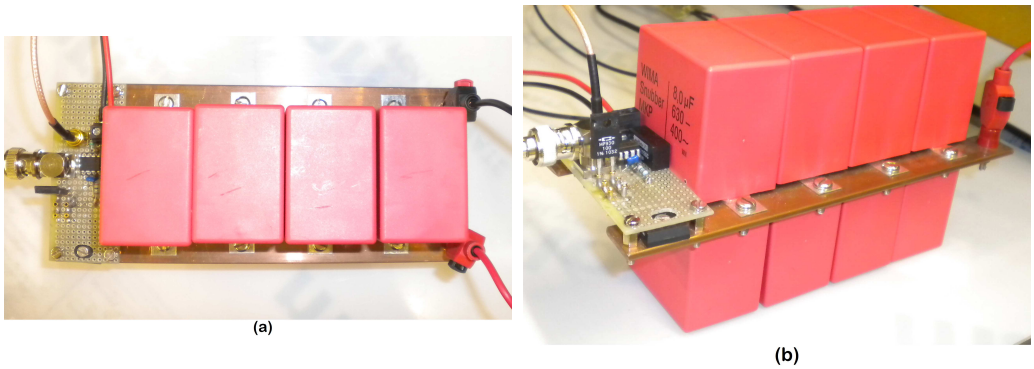

Figure 5.4: Old Dynamic Rdson Measurement Circuit: top view(a), side view(b).

In the following we will exlplain how the capacitances C_{bank} value is chosen. In fig 5.5 you can see a schematic of the circuit in which our capacitance is inserted; the load *Rload* schematically represents the DUT. We would like to comprehend how the voltage ripple, related to the capacitances, is connected with the size of the capacitors bank, in order to understand how far we can go with the t_{on} time of the DUT, without loosing too much in the the amplitude of the voltage delivered by the main power supply. It is relatively simple to approximate the voltage ripple as long as a few circuit parameters

are known.

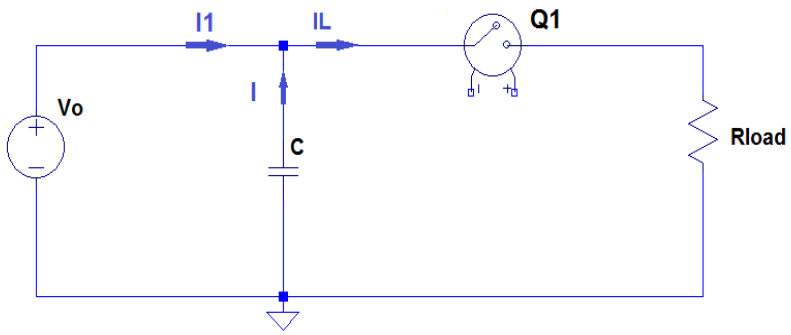

Figure 5.5: Simplified schematic of the circuit in which the bank of capacitors C_{bank} (simply represented by the symbol C) is inserted.

Let us introduce the symbols we will use in the following:

- **To** : Period of the switch Q1 in seconds
- **ton** : On-time of the DUT: period of time in which the drain current is flowing throw the DUT in seconds
- **toff** : Period of time in which the drain current is not flowing throw the DUT ($toff = To - ton$) in seconds
- **f** : Frequency of the switch Q1 in Herz

By assuming the load current IL constant during the time ton, the following expression is valid:

$$\Delta Q = C * \Delta V = I * \Delta t \tag{5.4}$$

and in particular, during the ton and toff time, we have:

$$ton : \Delta Q_{on} = C * \Delta V = I * ton, I + I1 - IL = 0 \tag{5.5}$$

$$toff : \Delta Q_{off} = C * \Delta V = I1 * toff, IL = 0, I1 = -I \tag{5.6}$$

The voltage on the capacitor C must be stationary, so that it has to be:

$$\Delta Q_{C\_discharge} = \Delta Q_{C\_charge} \Rightarrow \Delta Q_{on} = \Delta Q_{off} \tag{5.7}$$

Let us solve eq 5.7 by using eq 5.5 and eq 5.6:

$$\Delta Q_{on} = \Delta Q_{off}$$

$$I * ton = I1 * toff$$

$$(IL - I1) * ton = I1 * toff$$

$$IL * ton - I1(ton + toff) = 0$$

$$I1 = IL\frac{ton}{ton + toff} = IL * \delta \tag{5.8}$$

where δ stands for the duty cycle. If we substitute the result of eq 5.8 in eq 5.5, we obtain:

$$C * \Delta V = (IL - I1) * ton = IL * ton - IL * \delta * ton = IL * ton * (1 - \delta) \tag{5.9}$$

we can finally write:

$$C*\Delta V = IL*ton*(1-\delta) = IL*To*\frac{ton}{To}*(1-\delta) = IL*To*\delta*(1-\delta) \tag{5.10}$$

in the end we can find the value of the voltage ripple, expressed in function of some parameters:

$$\Delta V = IL * \frac{\delta * (1 - \delta)}{C * f} \tag{5.11}$$

Regarding the type of measurements we are interested into, it is $ton << To$,

so that we can approximate eq 5.11 as follows:

$$\Delta V = IL * \frac{\delta}{C * f}$$

$$\Delta V = IL * \frac{tonTo}{C * To}$$

$$\Delta V = IL * \frac{ton}{C} \tag{5.12}$$

As we can see from eq 5.12, the voltage ripple ΔV is directly proportional to:

- **IL** : the drain current in Ampere
- **ton** : the on-time of the DUT in seconds

whreas it is inversely proportional to:

- **C** : the value of the capacitors bank in Farad

Let us make a brief calculation of the worst case in our situation: we want to calculate how long the maximum ton time of the DUT can be in the following conditions:

- $IDS = 5A$ constant
- $\Delta V = 20V$ (a voltage drop of $\Delta V = 20V$ is considered to be negligile as far as we do this type of measurement with a drain-source voltage at least equal to $VDS = 400V$)

the maximum ton time of the DUT we can have in these conditions is given by the following expression:

$$ton_{max} = \frac{\Delta V_{max} * C}{IDS} = \frac{20V * 64\mu F}{5A} \approx 250\mu s \tag{5.13}$$

where C comes from eq 5.2. As we can see in eq 5.13, the circuit we are currently using, shown in fig 5.4 and made up by a capacitor $C_{bank} = 8 * 8\mu F = 64\mu F$, gives us the possibility to let our DUT stay in on-time for $250\mu s$ as maximum, by giving $IDS = 5A$ and with a voltage drop on the VDS equal to $\Delta V = 20V$.

5.2 GaN DReaM: the New Dynamic Rdson Measurement Setup

We would like to overcome the limitation on the t_{on} time , that is connected with the voltage ripple on the Cbank, in order to make our setup suitable for a wider range of measurements.
The circuit in fig 5.4 shows also another limitation: as we said on page 64, according to eq 5.3, the drain resistance RD must be manually chosen and changed every measurement; we would like this step to be automatized, in oder to drastically reduce the time needed for every measurement. We decided thus to build a new dynamic Rdson measurement setup (fig **??**), due to the following reasons:

- Making the setup suitable for a wider range of applications, by comparing with the previous setup (ton_{DUT} as long as possible: overcome Cbank's size limitation)
- Automatization (Introduction of labVIEW software, with the aim of driving all the instruments by software; Introduction of an automatized choice of the drain resistance RD, according to eq 5.3)
- Introduction of safety issues (Interlock), with the aim of letting the user work in safe conditions

In fig 5.6 you can see the schematic of the new setup: the so called *GaN DReaM* setup, acronym that stands for *GaN Dynamic Rdson Measurement*. In the bottom part you can notice the bank of $48 * 8\mu F$ capacitors, put in in parallel with the main power supply. They give us the possibility to extend the maximum gate on-time up to $t_{on} = 1.5ms$ in the worst case (67). Infact, by using the expression 5.13:

$$ton_{max} = \frac{C * \Delta V_{max}}{I_{load}} = \frac{48 * 8\mu F * 20V}{5A} \approx 1.5ms \tag{5.14}$$

The new part of circuitry, related to automation and safety issues, can be found in the upper part of the board-schematic shown in fig 5.6.

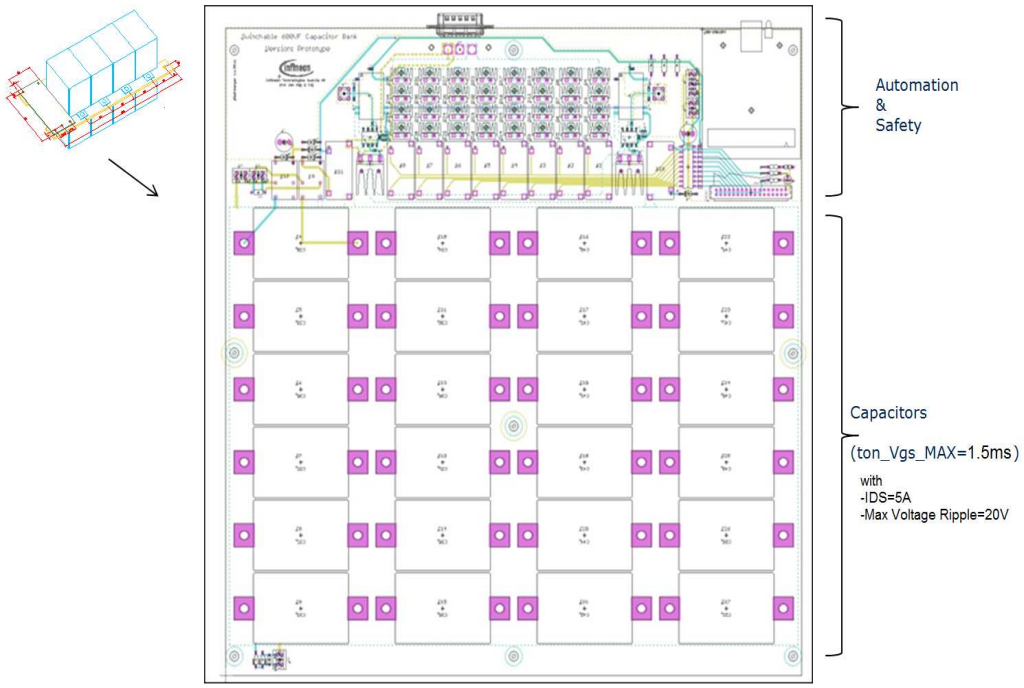

Figure 5.6: GaN DReaM Setup: Circuitry of the new Dynamic Rdson Measurement Setup.

5.2.1 Automatic Selection of the Drain Resistance RD

The way of operating of the new setup is basically the same of the previous one (the schematic in fig. 5.2 is still valid), but there has been the introduction of some new features.
First of all there has been the introduction of a labview software that gives us the opportunity of driving all the instruments used inside the setup. Moreover via labVIEW software it is possible to select the desired drain resistance RD, according to eq 5.3 and to insert it inside the circuit.
Let us see how the drain resistance RD can be automatically selected: in fig 5.7 you can see the same schematic shown in fig 5.1, but now the resistance RD is replaced by a set of eight resistances. Every resistance is connected in parallel with the others throw a switch; the switches are represented by relays, driven by the user via software. Every switch can be opened or closed, indipendently from the state of the other switches. Thanks to the block of resistances, we have $2^N = 2^8 = 256$ possible resistances combinations, thus 256 resistance values I can choose between, in order to set the desired drain resistence value, according to eq 5.3.

Let us see how I can select which resistances to insert inside the resistances bank, in order to have the desired drain resistance value (fig 5.8). In order to have the possibility of selecting via software which resistances to insert in the circuit and so which switches to close, we use a NI USB 6501 device: this device is produced by National Instrument; it is a digital I/O device, connected to the pc via usb. It has 24 digital channels, divided in 3 ports and each port is composed by 8 channels; on every channel I can read or write a digital value via software. The eight resistances are connected to one port of the USB 6501 device. Via software I can choose which digital channels to activate and therefore which resistances to insert in the circuit, in order to obtain the desired value of drain resistence RD. As we can see in fig 5.8, between the USB 6501 device and the eight relays is inserted a driver, with the aim of incrementing the current delivered by the usb device, so that the relays get enough current to switch.
It is important for the relays we use, to have a negligible contact resistance,

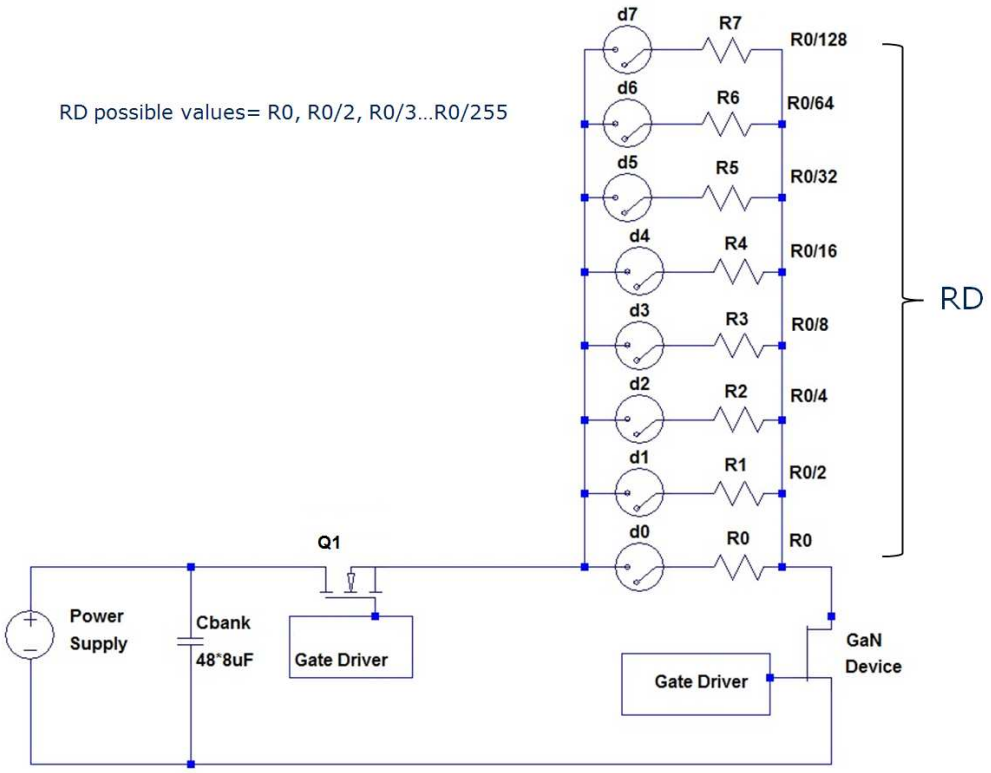

Figure 5.7: Simple schematic that shows how the drain resistance RD can be selected and inserted inside the measurement circuit.

in order not to influence the value or drain resistance we set. The maximum contact resistance for the relays we use is typically $1m\Omega$, value that is absolutely negligible even by comparing with the smallest resistance used to build up RD: $R_{min} = 82\Omega$.

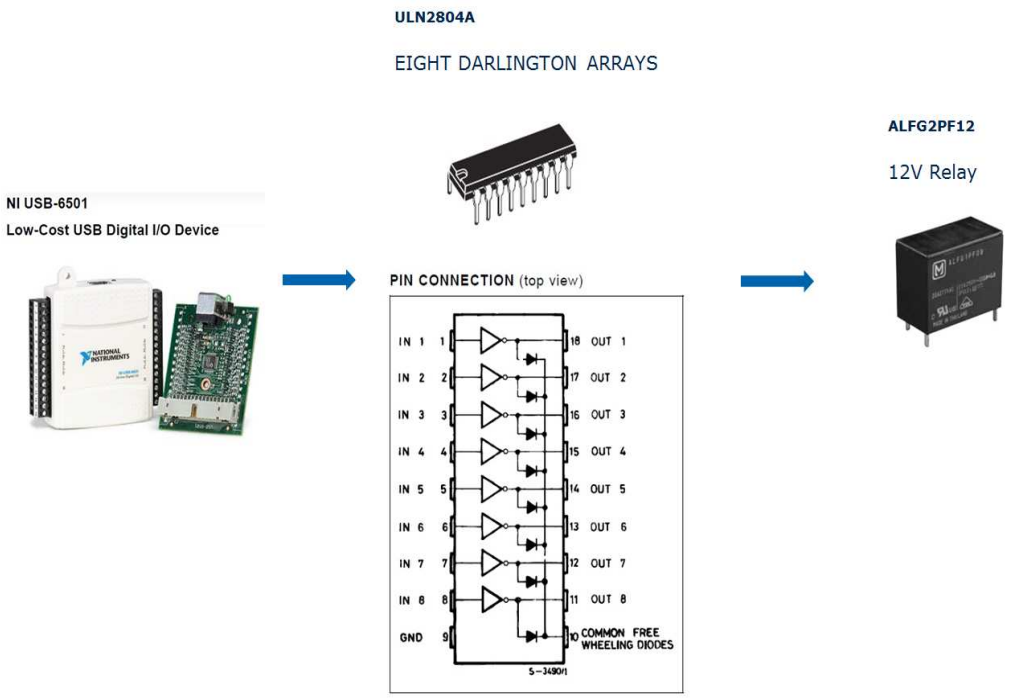

Figure 5.8: How I can choose which resistances to insert in the circuit, in order to have the desired value of the drain resistance RD.

In fig 5.9 the schematic of the circuit relative to the automatic selection of the drain resistance is shown. As for the USB 6501 device, we can see that, from the eight channels of port 0, eight wires depart and, after have passed throw the driver, they reach the eight relays (K1..K8), associated with the drain resistances bank.

In fig 5.10 the labview window related to the selection of the drain resistance is shown. In the left part of the window, circled in red, I can insert the voltage I want to apply on the main power supply(*VDD (V)*) and the

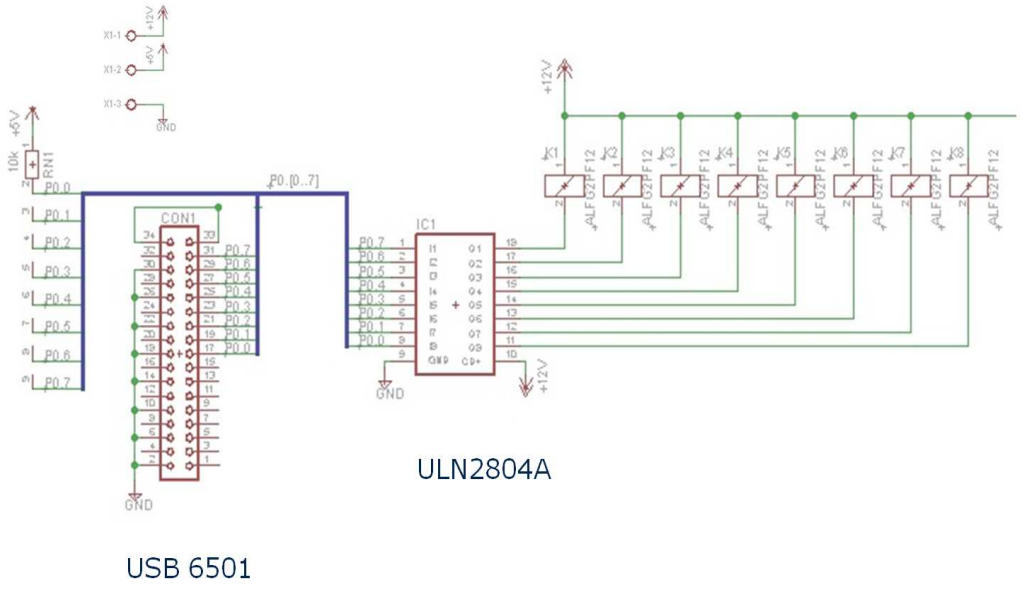

Figure 5.9: GaN DReaM Setup; Schematic of the circuit relative to the resistance bank forming the drain resistance RD.

desired drain current(*ID (A)*).Thanks to the introduction of these values, the software automatically calculates the value of the drain resistance that should be inserted in the circuit (eq 5.3), then it selects and inserts in the circuit the resistences that, put in parallel, best approximate RD. On the right side of the window, in fig 5.10, it is shown the so called *R calculated*, given by eq 5.3, whereas in the box called *R_real_selected*, you can see the real value of the drain resistance inserted in the circuit, that is the value that best approximates the desired RD value, choosen between the 255 possible resistance combinations.

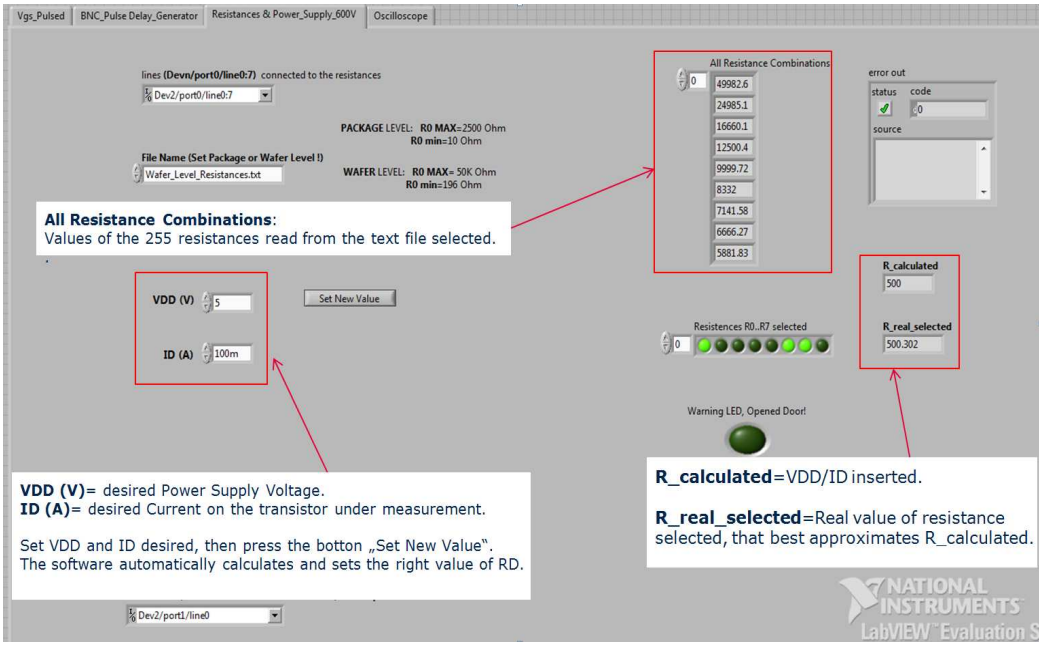

Figure 5.10: GaN DReaM Setup; Labview window related to the selection of the drain resistance RD.

Now let us see how the eight resistances forming the capactors bank are chosen. As you can see in fig 5.11, the eight resistances respect the following

relation:

$$R_{i+1} = 2R_i, i = [0, 6] \tag{5.15}$$

We can write the following expressions:

$$\frac{1}{\frac{R0}{2^0} \parallel \frac{R0}{2^1} \parallel \frac{R0}{2^2} \parallel ... \parallel \frac{R0}{2^N}} = \frac{2^0}{R0} + \frac{2^1}{R0} + \frac{2^2}{R0} + ... + \frac{2^N}{R0} \tag{5.16}$$

since that, we can write:

$$\frac{1}{R \parallel} = \frac{d0 * 2^0 + d1 * 2^1 + d2 * 2^2 + ... + dN * 2^N}{R0} = \frac{D}{R0}, di = [0, 1] \tag{5.17}$$

where the symbol $R \parallel$ stands for the parallel of resistances, while the symbol di represents the switch i: if di=1, the switch i is closed; if di=0, the switch i is opened. In the end we can write the following expression:

$$R \parallel = \frac{R0}{D} \tag{5.18}$$

The table in fig 5.11 represents the way in which the 255 combinations of resistances are made; referring for example to the third line of the table, the resistances R0 and R1 are inserted in the block (the switches d0 and d1 are closed); let us apply eq 5.18 to this case:

$$R \parallel = \frac{R0}{D} = \frac{R0}{1 * 2^0 + 1 * 2^1} = \frac{R0}{3} \tag{5.19}$$

As we have previously said, the GaN DReaM Setup is used to measure devices both on package level and on wafer level. As we know, the devices on package level have much more drain current capability than the ones on wafer level. Due to the fact that we are using the same range of drain-source voltage (10V-600V) both on package and on wafer level, we need a different range of drain resistances RD: one on package level and on wafer level.
As for the resistances block on wafer level, for example, we want to evaluate the miminum and the maximum drain resistance RD we need, in order to understand which range of values we should use; for this reason we have to consider the following datas, valid on wafer level:

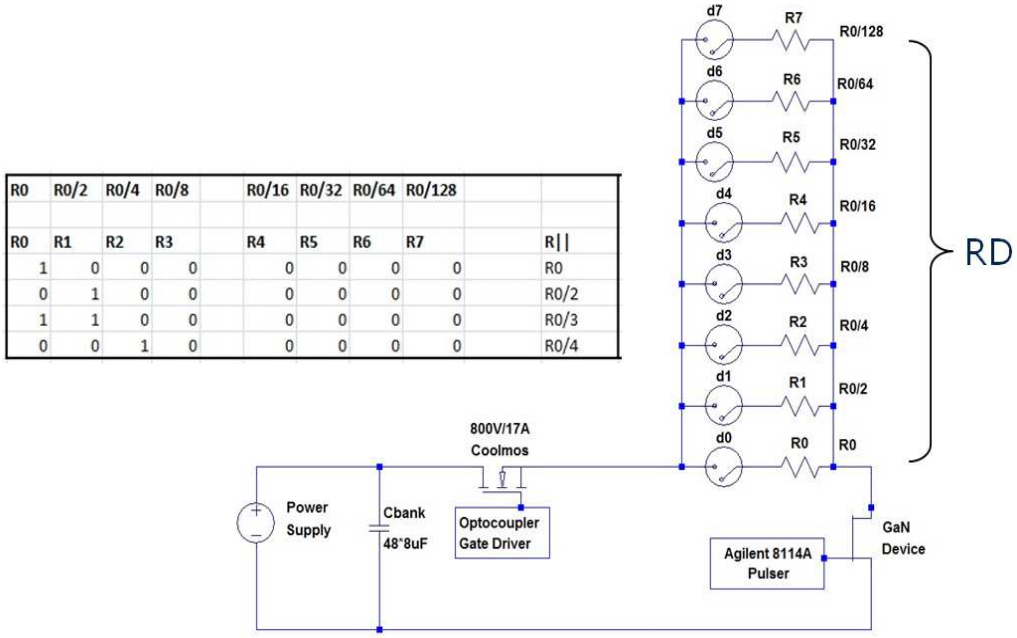

Figure 5.11: GaN DReaM Setup; Simple schematic that shows how the drain resistance RD can be selected and inserted inside the measurement circuit.

- $VDS = 50V \rightarrow 600V$
- $IDS_{min} = 12mA$
- $IDS_{MAX} = 250mA$

Thanks to these datas we can find the upper and lower limitations of the resistance's values forming the block:

$$RD_{min} = \frac{VDS_{min}}{IDS_{MAX}} = \frac{50V}{250mA} = 200\Omega \tag{5.20}$$

$$RD_{MAX} = \frac{VDS_{MAX}}{IDS_{min}} = \frac{600V}{12mA} = 50k\Omega \tag{5.21}$$

It is quite difficult to find eight resistance that exactly respect eq 5.15, 5.20 and 5.21 among the power resistors we use. Since that, if we want to make the best choice, the following criteria have to be used:

- the eight resistances forming the block must respect as much as possible the relation 5.15
- the best resistances combination will be the one that minimize the error, regarding to the 255 possible resistances combinations

After have chosen the eigth resistances, by following these criteria, we want to see how the software can choose the resistance RD, that best approximate the desired value, among the 255 possible combinations (eq 5.3). All the possible combinations are calculated by a digital multimeter, connected to the GaN DReaM Circuit: we make the switch d1-d7 perform every possible combinations; the digital multimiter evaluates all the possible combinations and saves all them by labVIEW software into a text file. In the end we have one text file containing all the possible resistance combinations on wafer level and one on package level. In fig 5.10 is shown the labview window related to the selection of the drain resistance; on the right side of the figure you can see the window **File Name (Set Package or Wafer Level)**, used to select the text file from which we want to read the saved combinations. Afterwards the user can insert the value of the voltage applied on the drain of

the DUT **VDD (V)** and the desired drain current **ID (A)**; thanks to these dats the software evaluates the desired RD (eq 5.3). In the end the software calculates the difference between the desired resistance and all the possible 255 resistances combinations, read by the text file, in order to select the resistance that best approximate the desired RD, so that the error is minimized.

In fig 5.12, on the right side,it is shown the schematic of the circuit comprehensive of the drain resistances block, connected to the switches K1..K8. As you can notice, each of the eight resistances is actually formed by a block of four resistances in parallel: in this way the power can be shared between many resistances. Every single resistance, moreover, is fixed on a heatsink, in order to avoid the resistances to be damaged by overpower. On the left side in fig 5.12 is shown the upper part of the board circuit illustrated in fig 5.6; you can notice, circled in red, the block of resistances that form the drain-resistance RD, divided in columns of four resistances. On the lower part of every column of four resistance, is shown the relay connected with that resistances column. On the right part of the board you can see how the eight relays, associated with the resistances, are connected to the current driver and then to the USB 6501 device (set on the top right corner of the board). in fig 5.13 a picture of the GaN DReaM‘s circuitry is shown.

5.2.2 Gate Driver

In the new GaN DReaM setup the gate driver has been improved, by comparing with one used in the old circuit (60).
In fig 5.14 the schematic of the new gate driver circuit is shown. The gate-source signal is made thanks to a gate driver, the BNC 575 Pulse Delay Generator and an auxiliary double output power supply (Agilent E3649A, in fig 5.15(a)). The voltages V1 and Voffset in fig 5.14 are given by the two output voltages of the auxiliary double output power supply. The gate driver is connected to one of the channels of the BNC instrument, that gives the t_{on} and t_{off} times of the gate-source pulse. The gate driver circuit, mounted on PCB on the gate manipulator inside the wafer station, is shown in fig

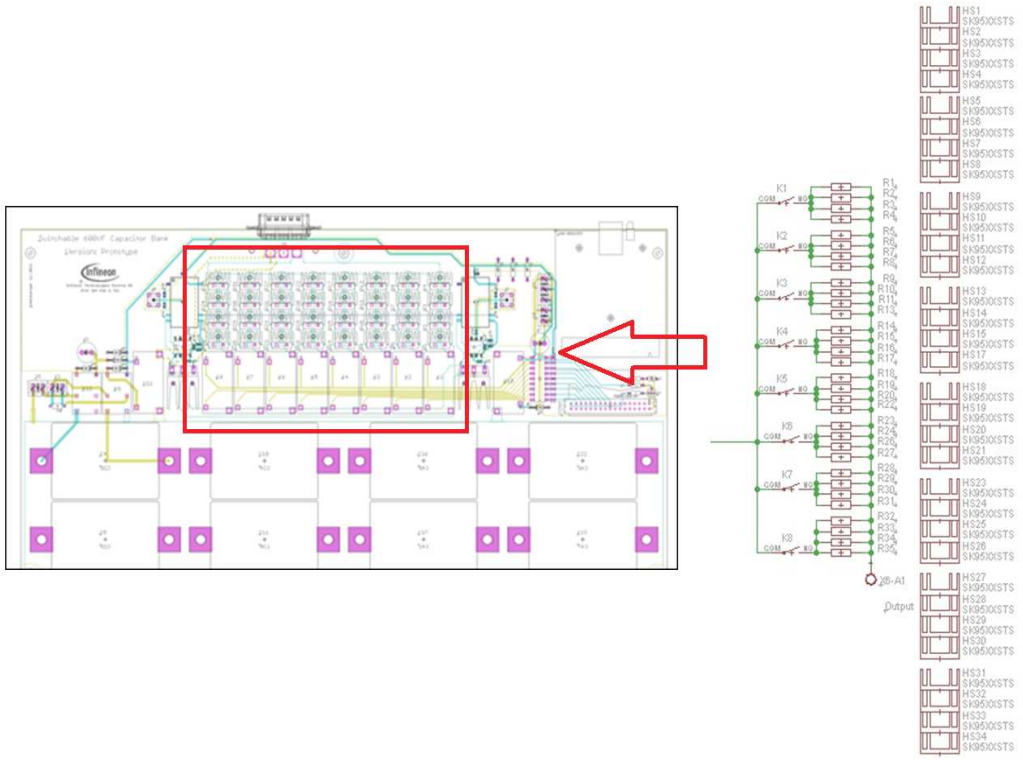

Figure 5.12: GaN DReaM Setup; Upper part of the circuit board shown in fig 5.6 (on the left side) and detailed schematic of the drain-resistance circuit section (on the right side).

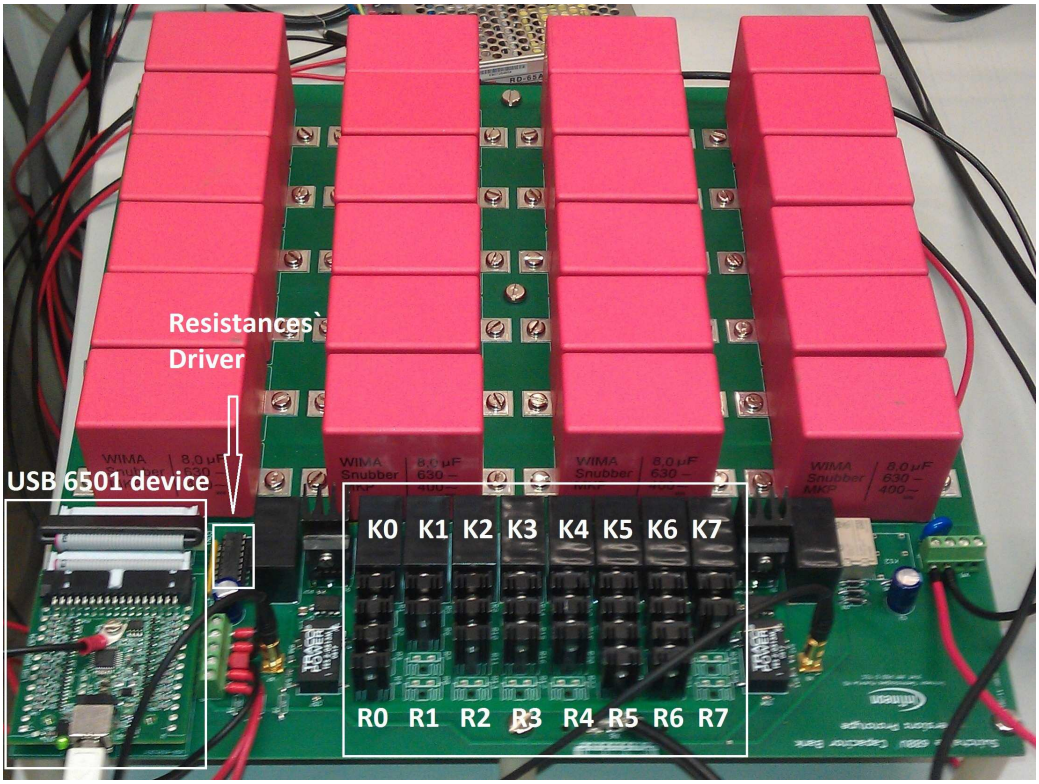

Figure 5.13: GaN DReaM Setup; USB 6501 device, current driver and drain resistances bank are highlighted. In pink you can see the bank of capacitors.

5.15(b).

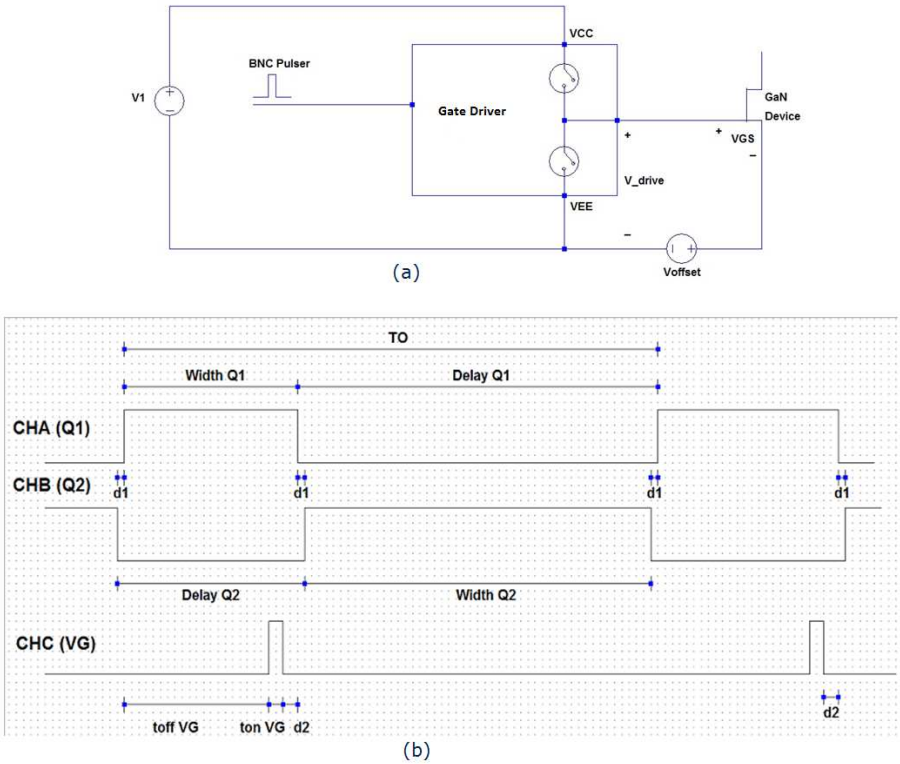

Figure 5.14: GaN DReaM Setup; Gate Driver Circuit Schematic.

By applying the Kirchhoff voltage law on the loop where the gate-source voltage is set, we can extract the expression that describes the gate-source voltage of the DUT:

$$V_{GS} + V_{offset} - V_{drive} = 0$$

$$V_{GS} = V_{drive} - V_{offset} \tag{5.22}$$

Then, if I call V_{GS_HIGH} and V_{GS_low} the high and the low value of the V_{GS} pulse, I can write the following expressions:

$$V_{GS\_HIGH} = V1 - V_{offset}$$

$$V_{GS\_low} = -V_{offset} \tag{5.23}$$

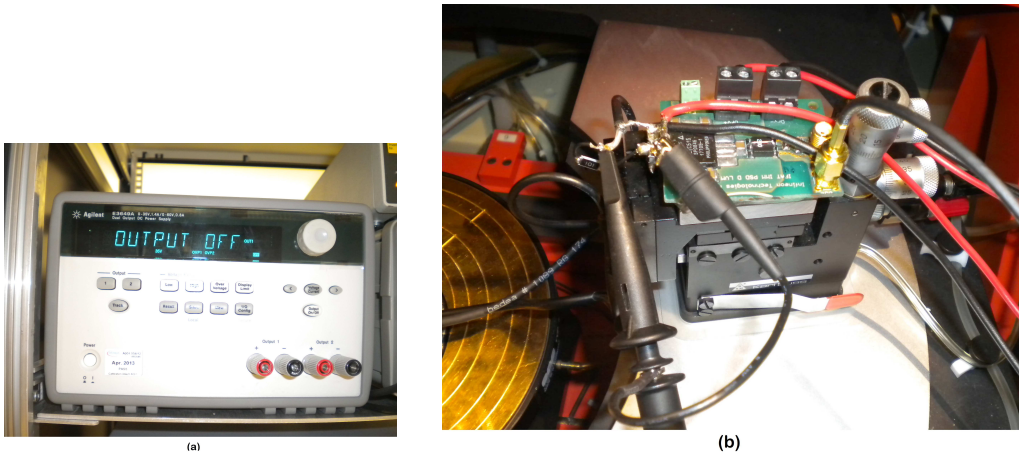

Figure 5.15: GaN DReaM Setup; Agilent E3649A auxiliary Power Supply, used in the gate driving of the DUT (a), Gate Driver mounted on PCB on the gate manipulator inside the wafer station (b).

Thanks to eq 5.23, we can set the values of the two output channels V1 and V2 (where V2 that stands for Voffset) of the auxiliary power supply (fig 5.15(a)).
In fig 5.16 you can see the labview window that we use to drive the double output power supply. On the left side of the window it is possible to insert the high and the low value of the DUT's gate pulse (V_{GS_HIGH} and V_{GS_low}); thanks to the insertion of these values, the software, throw the eq 5.23, automatically calculates the voltage values V1 and V2, shown on the right side of the labview window, and it drives the auxiliary power supply in order to have the desired V_{GS_HIGH} and V_{GS_low}.

After having explained how the gate driver works, we can understand the meaning of the signals in fig 5.14(b). In fig 5.14(b), the signal related to the coolMOS Q1 *CHA (Q1)* and the gate signal *CHC (VG)* are shown. The switch Q1 is driven by the channel A of the BNC 575 instrument, whereas the gate driver is connected to the channel C. Channel A (CHA) is synchronized with the internal clock of the BNC instrument. Channel C (CHC) is synchronized with channel A. On channel C, it has been inserted a delay

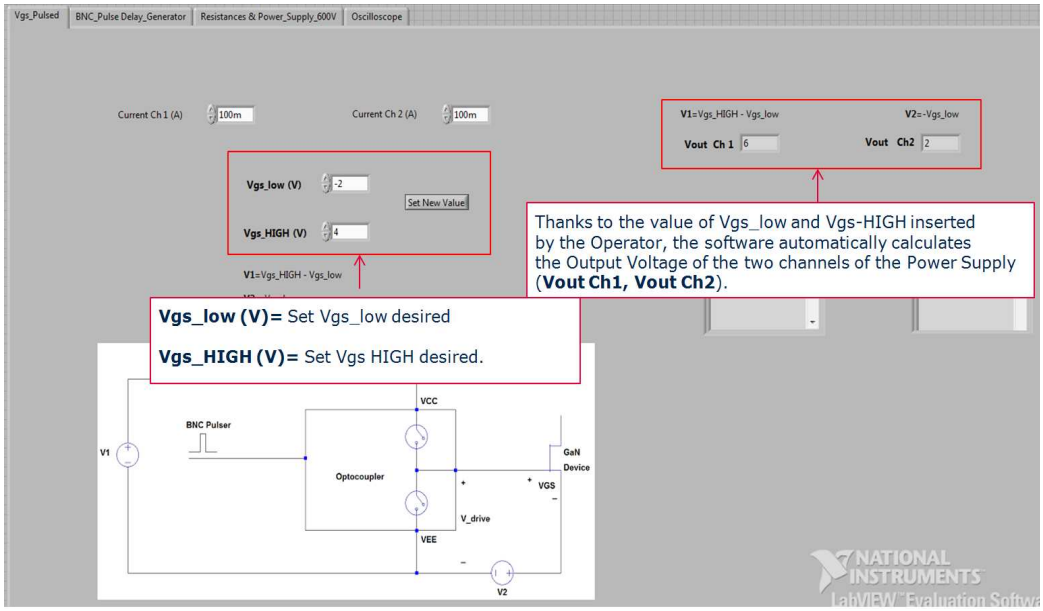

Figure 5.16: GaN DReaM Setup; Labview window used to set the on-time and off-time values of the DUT‘s gate pulse.

time with respect to the synchronization source; this delay represents the t_{off} time (or stress time) of the gate-source pulse; on the other side the width of the gate signal on channel C represents the t_{on} time of the gate-source pulse. The width of the signal Q1 is set by software, according to the following expression:

$$width_{CHA} = toff_{VG} + ton_{VG} + d2 \tag{5.24}$$

where d2 is a small delay, just due to safety reasons inserted between the end of the gate pulse and the end of the signalQ1. As you can see in fig 5.14(b), the channel B of the BNC instrument is used too: we will see why in the following. Referring to fig 5.1, we can notice that the source of the coolMOS Q1 and the source of the DUT have obviously different potentials, so that when the coolMOS Q1 switches off, there is a parasitic capacitance between these two points, that needs some time to discharge; for this reason, when the coolMOS Q1 switches off, the drain voltage of the DUT needs some time to reach the zero level. This phenomenon causes an undesired overstress on the DUT, that we would like to avoid. For this reason we have inserted a second coolMOS device Q2 (fig 5.17(a)): while Q1 is in on-state, Q2 is switched off and vice versa, so that the switching off time of the DUT is much faster than before. The gate potential of Q2 is connected to the channel B of the BNC instrument. In fig 5.17(b) the gate signal of Q1 and Q2 are shown in function of the time.

Channel B is synchronized with channel A, with a delay given by the following expression:

$$delay_{CHB} = width_{CHA} + d1 \tag{5.25}$$

where d1 is a small delay, inserted between the end(beginning) of the Q1 pulse and the beginning(end) of the Q2 signal due to safety reasons: if Q1 and Q2 were in on-state at the same time, the main power supply will be shorted. In the end, in fig 5.14(b) you can see the signals of the three channels. In fig 5.18 the GaN DReaM circuitry is shown, in particular the coolMOS Q1 and Q2, mounted on heatsink, are indicated.

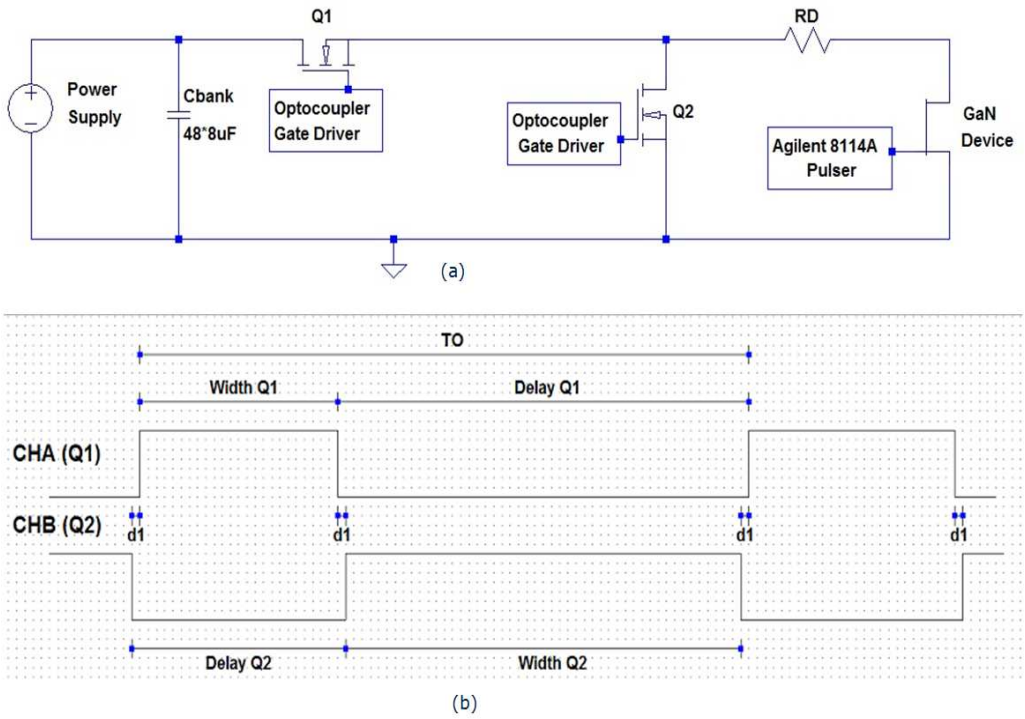

Figure 5.17: GaN DReaM Setup; The auxiliary coolMOS Q2 makes the switching off time of the DUT faster.

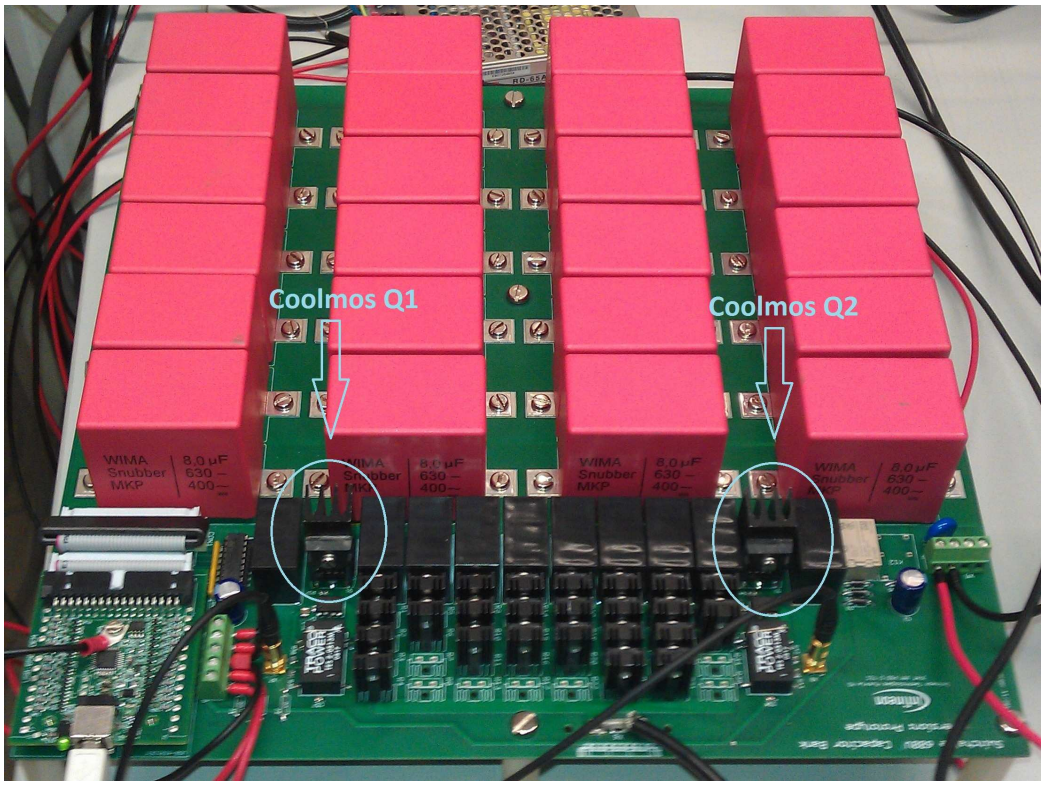

Figure 5.18: GaN DReaM Setup; CoolMOS Q1 and Q2 are highlighted.

The BNC instrument is driven via software; in fig 5.19 the labVIEW window used to drive the Pulse Delay Generator BNC 575 is shown. The box in which the data can be inserted are circled in red. In the *Channel On/Off* window you can decide which channel to switch on or off; in the *Sync/Source* window it is possible to set the synchronization source for each channel. Moreover you can insert the Period of the signals *Period (TO)*, the t_{on} and t_{off} time of the gate pulse and the safety delays d1 and d2 (fig 5.14).

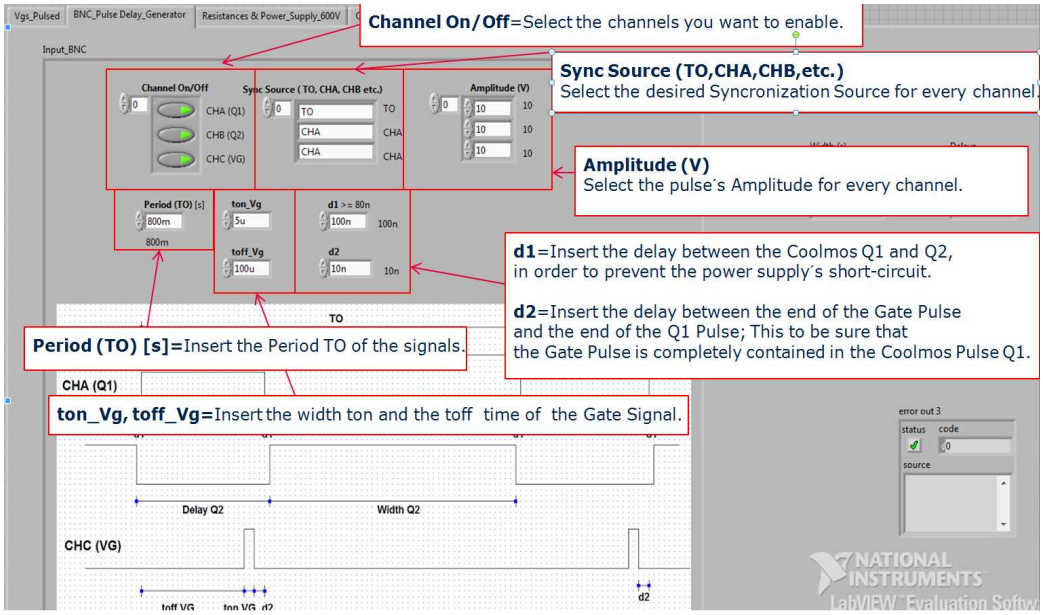

Figure 5.19: GaN DReaM Setup; LabVIEW window used to drive the BNC 575 Instrument.

Referring to fig 5.20, on the right side of the window, you can see the parameters automatically calculated via software, according to eq 5.24 and eq5.25.

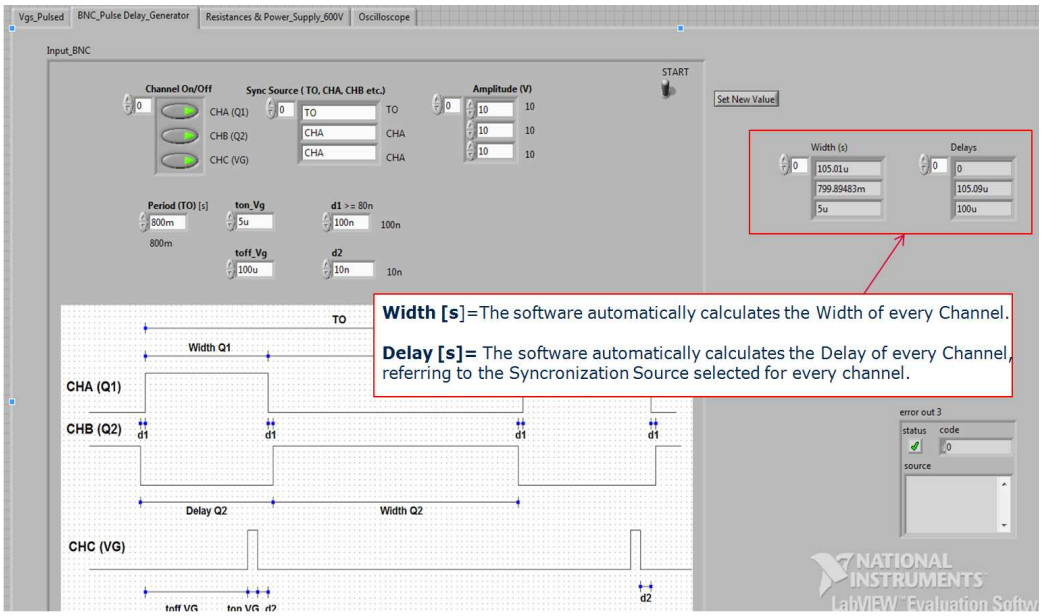

Figure 5.20: GaN DReaM Setup; LabVIEW window used to drive the BNC 575 Instrument.

5.2.3 Oscilloscope

The datas read from the oscilloscope are saved via labVIEW software into text file. The oscilloscope used is a 1GHz Lecroy LC564A (fig 5.21). In fig 5.22 the labVIEW window used to save the datas read from the oscilloscope is shown. In the red square indicated with the number one, you can see a graph, reproducing the waveforms read from the oscilloscope. On the left side of the window, highlighted with the number two, you can select which oscilloscope's channels to read, the name of the waveform read and its unity of measurement. When the user wants to save the datas from the oscilloscope, he can just press the save bottom (indicated with number three in fig 5.22). In fig 5.23 the sections in which you can insert the file path and the file name you want the datas to be saved with are highlighted, moreover it is possible to add the operator's name and a comment, that will appear in the first row of the text file containing the saved datas. In fig 5.24 two more bottons are highlighted: if these buttons are active, the software automatically adds two columns in the data file, containing the calculation of Rdson, by using the VDS signal (by pressing the bottom on the left side) or the Clamped-VDS signal (by pressing the bottom on the right side).

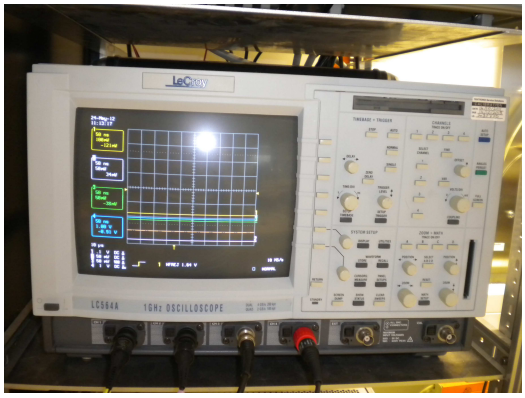

Figure 5.21: GaN DReaM Setup; 1GHz Lecroy LC564A Oscilloscope.

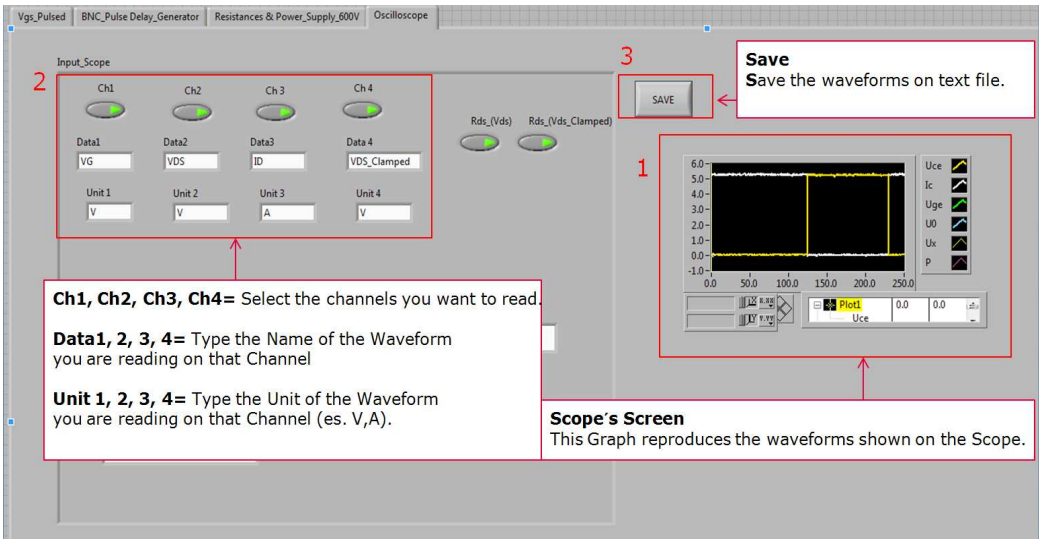

Figure 5.22: GaN DReaM Station: labVIEW window used to save the datas read from the oscilloscope.

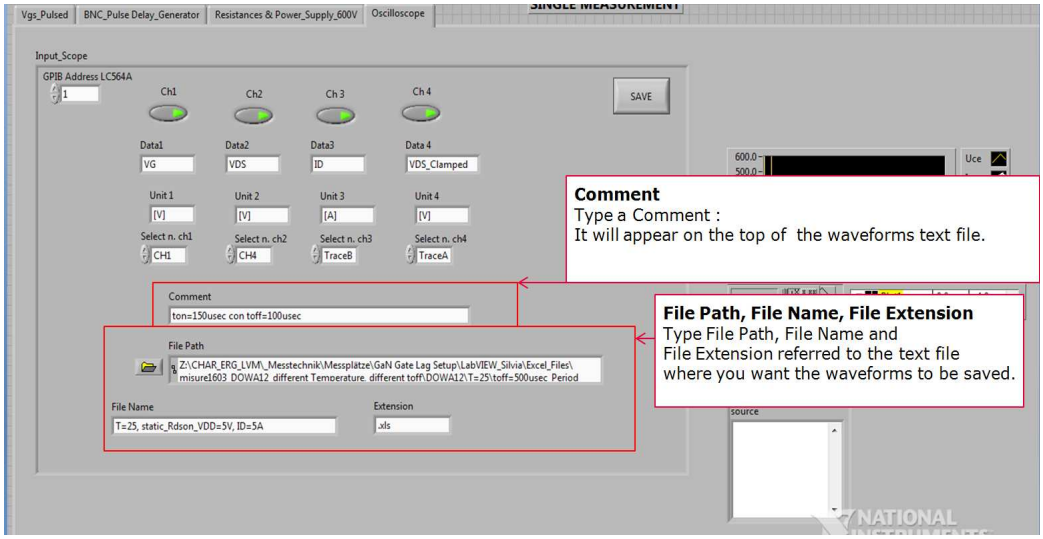

Figure 5.23: GaN DReaM Station: labVIEW window used to save the datas read from the oscilloscope.

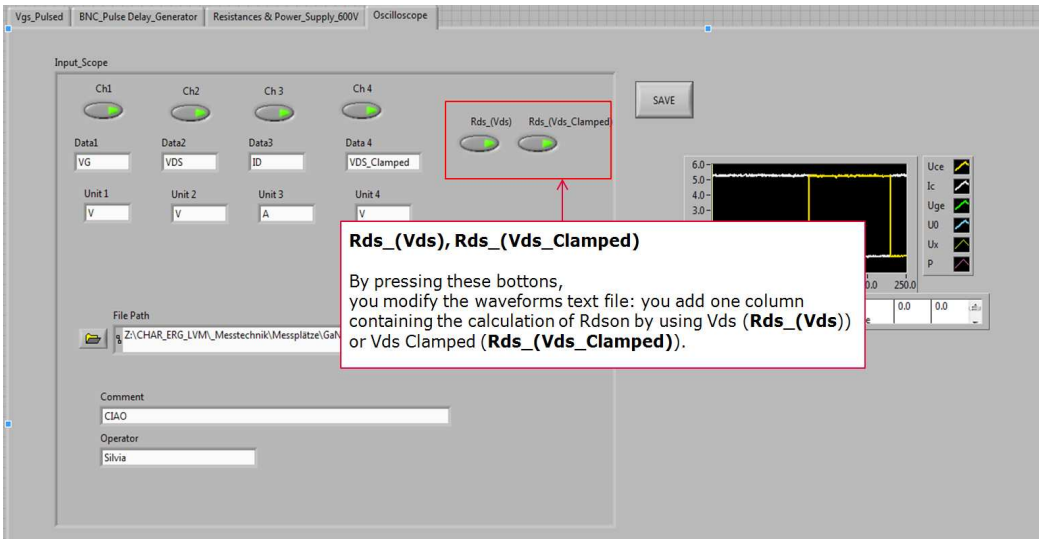

Figure 5.24: GaN DReaM Station: labVIEW window used to save the datas read from the oscilloscope.

5.2.4 Interlock Safety System.

On the top part in fig 5.25 you can see the complete GaN DReaM Station and the black box used for the measurements. The GaN DReaM setup can be used both on package level and on wafer level;in both the cases the device to be measured are located inside the black box: this in order to have the possibility to introduct safety features for the user both on package level and on wafer level. As we said at page 68, infact, some safety issues have been introduced in the GaN DReaM Setup: the main power supply infact, connected to the drain potential of the DUT, is capable of delivering up to 600V/1.3A, so that it is, so that it is important for the new setup to provide some safety features, in order to let the user operate in safe conditions. We want to avoid that, while the measurement is running, the operator has the possibility to enter in contact with the hazardous volatages applied on the DUT. For this reason we use an interlock system (fig 5.25 connected with the black box: if someone accidentally opens the doors of the box, while the voltage on the main power supply is not null, the main power supply is automatically disconnected from the rest of the circuit. As it is shown in fig 5.25, we use some relays that act as switches inside the circuit. While the doors of the black box are closed, the switches K9, K10 and K11 are closed, while the switch K12 is opened. If someone opens the doors, the interlock system is activated, so that the switches K9, K10 and K11 are opened, while K12 is closed: in this way both the power supply and the capacitances bank are disconnected from the rest of the circuit, while the capacitors bank (Cbank) is discharged throw the bleeding resistor R2.

The bleeding resistor value is calculated in the following way: by considering the power supply to deliver 600V, we would like the voltage on Cbank to reach approximately 50V in two seconds. The complete calculation is shown in the following:

$$V = V_0 e^{-\frac{t}{\tau}}$$

$$50V = 600V e^{-\frac{t}{\tau}}$$

$$12 = e^{\frac{t}{\tau}}$$

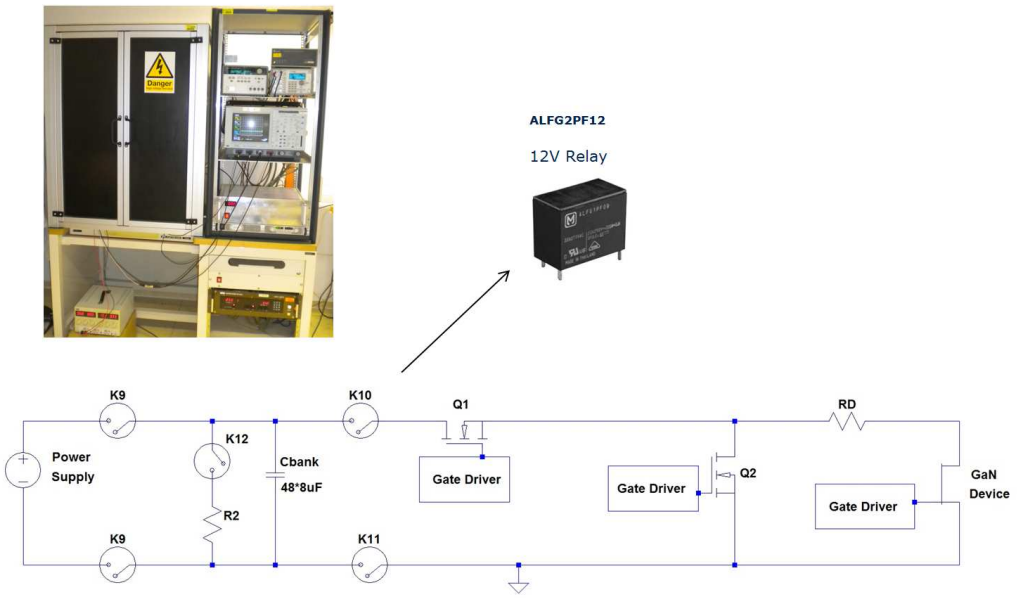

Figure 5.25: Interlock Simplified Schematic.

$$\tau = \frac{t}{ln(12)} = \frac{2}{ln(12)} = 0.805s$$

$$R2 = \frac{\tau}{C} \approx 2k\Omega \tag{5.26}$$

Due to the calculation just shown, we chose $R2 = 2k\Omega$ bleeding resistor to discharge Cbank.
In fig 5.26 you can see the precise schematic of the interlock circuit. The interlock is located on the junction between the two doors of the black box. While the doors are closed, the interlock is closed; while they are opened, the interlock is opened. One side of the interlock is connected to an auxiliary 12V power supply; the other side of the interlock is connected to the pin one of the 12V relay K9, K10 and K11. The diode D1 connects the interlock with the relay K12. The interlock is moreover connected to the base of a BC337 BJT, throw a resistive divider, made up by the resistances R21 and R25. The collector of the BJT is connected to Port 1 line 0 (P1.0) of the USB 6501 device and, throw a resistance, to the pins number 33 and 34 of the USB 6501 device; pins 33 and 34 have a fixed voltage value, equal to 5V. When the doors of the black box are closed, the interlock is closed too, so that the switches K9, K10 and K11 are closed, while the switch K12 is opened. On the other side, when the interlock is opened, the switches K9, K10 and K11 are opened, while the switch K12 is closed: the diode D1 is OFF, so that the capacitor C3 (fig 5.26) discharges throw the relay K12.
The diodes D2, D3, and D5 act as freewheeling diodes: when the relay‘s coil is energized with direct current, a diode is often placed across the coil, in order to dissipate the energy from the collapsing magnetic field at deactivation, which would otherwise generate a voltage spike dangerous for the other components of the circuit.

We would like the interlock‘s state to be checked by software too. In fig 5.27 you can see the labVIEW interlock window. The number 9 indicated the window in which you can insert the port and line of the USB device used to read the state of the interlock (in our case it is port 1 line 0). The number 10 in the window shows the warning light: if someone opens the doors, the main power supply is automatically turned back to 0V by software and the

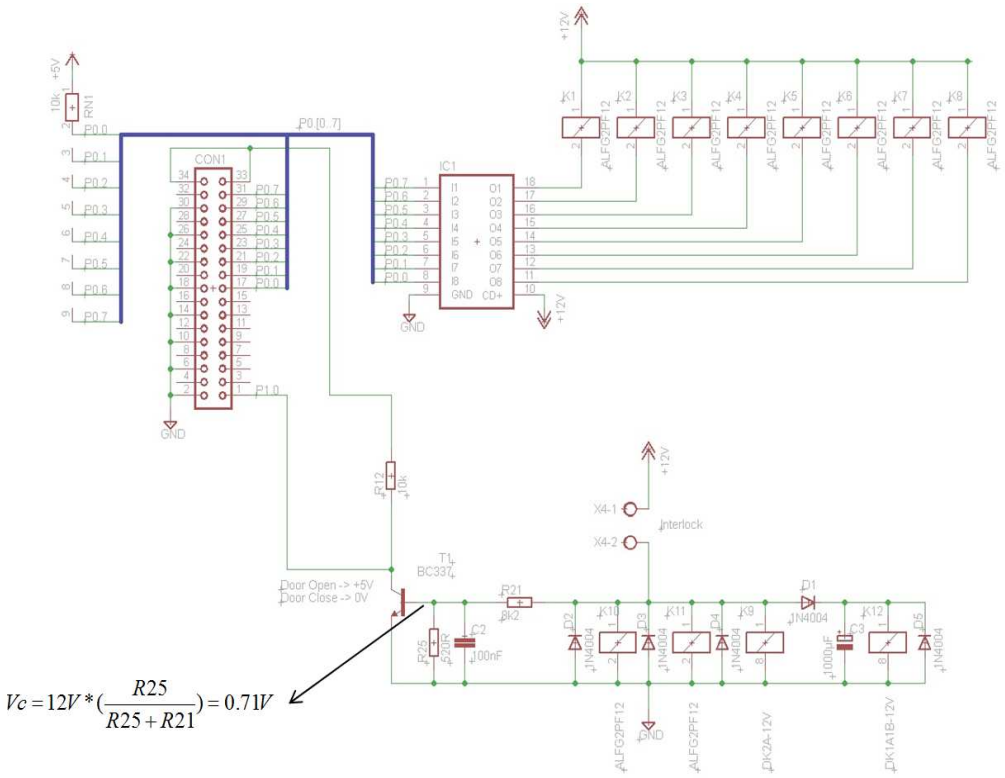

Figure 5.26: Schematic of the Interlock Circuit.

warning light turns on.
Now we would like to understand how the interlock‘s state can be checked by software: In order to have a warning message coming from the software, we take advantage of the USB 6501 device, already used for driving the resistances bank that forms the drain resistance RD. As you can see in fig 5.26, we can use the port 1 line 0 (port 1.0) of the USB device, whose digital value we can read via software. The following expression is valid:

$$Door\_opened \Rightarrow P1.0 = 5V$$

$$Door\_closed \Rightarrow P1.0 = 0V$$

If we want to understand how the interlock‘state can be checked by software, we need to comprehend what is the function of the BJT BC337 inside the circuit. When the interlock is closed, the BJT is switched on, because, thanks to the resistive divider made up by R21 and R25, the following expression is valid:

$$V_{BE} = 12V * \left(\frac{R25}{R21 + R25}\right) = 12V * \left(\frac{520\Omega}{8k\Omega + 520\Omega}\right) = 0.71V \qquad (5.27)$$

So that the port 1.0 of the USB 6501 device is directly connected to 0V potential: $P1.0 = 0V \Rightarrow Door\_closed$. If, on the opposite, the doors are opened, then port 1.0 is connected to lines 33 and 34 throw the resistance R12, so that $P1.0 = 5V \Rightarrow Door\_opened$.

The software, anyway, is not as reliable as the hardware system, so that we can say the interlock system to be hardware based, then the software control is just a subsidiary mean of checking.

In fig 5.28(a) you can see the entire GaN DReaM Setup working; the circled and numbered components in the picture are described as follows:

1. Agilent E3649A: auxiliary power supply used by the gate driver to set the high and low voltage value of the gate pulse

2. BNC 575 Pulse Delay Generator: pulse generator used to set the on

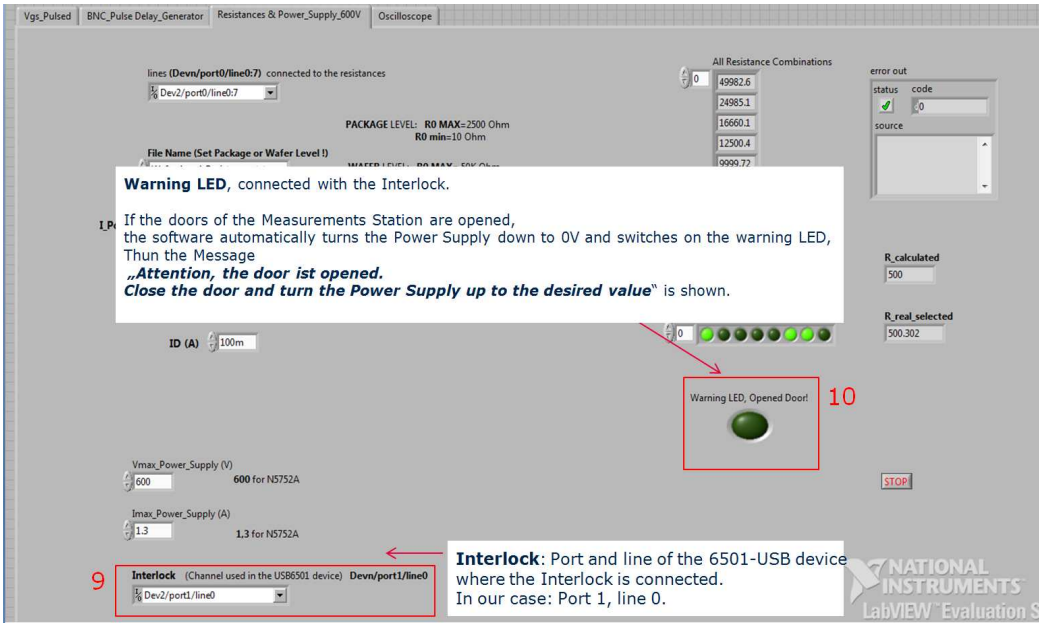

Figure 5.27: LabVIEW interlock window.The Interlock warning led is highlighted.

and off-time of the coolMOS Q1 and Q2 and of the DUT's gate pulse

3. Lecroy LC564A 1GHz Oscilloscope
4. GaN DReaM Circuit; in fig 5.28(b), the front view of the GaN DReaM circuit is zoomed; circled in red you can notice the display used to monitor the voltage on the capacitors bank: the user before entering in contact with the DUT, can check that the voltage applied on the Cbank is null
5. N5752A: 600V main power supply

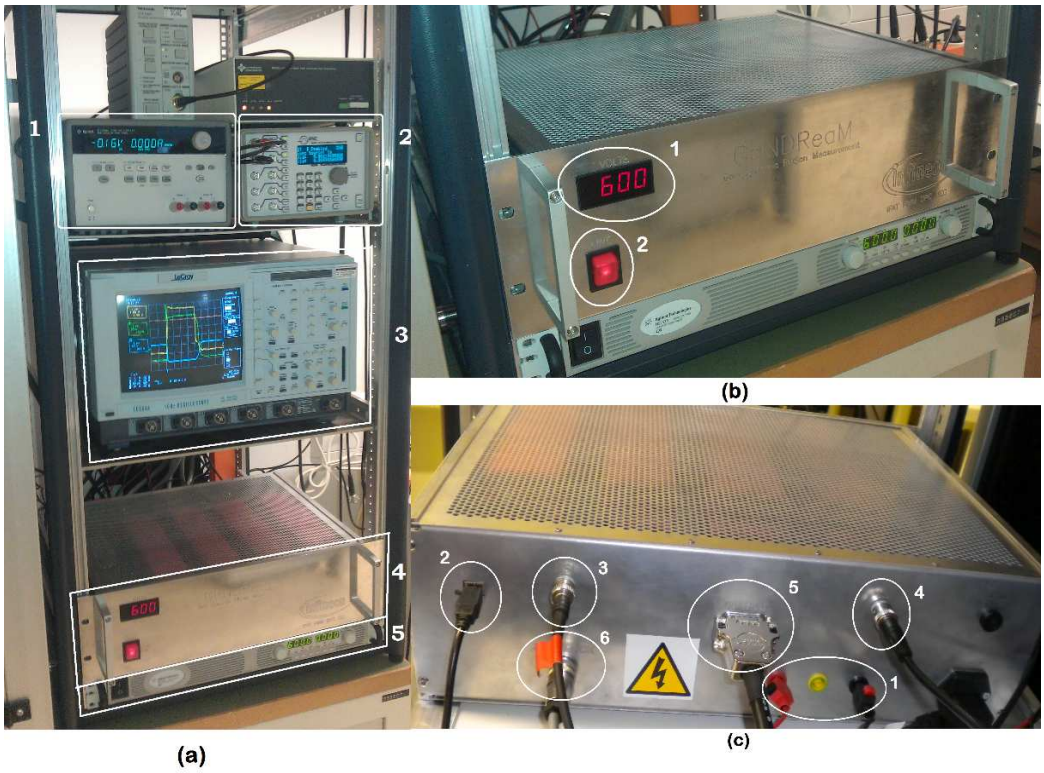

Figure 5.28: GaN DReaM Setup(a), Front(b) and Back(c) View of the GaN DReaM Circuit.

In fig 5.28(c) the connections on the back side of the GaN DReaM circuit are shown; the circled and numbered components in the picture are described as follows:

1. Connectors for the 600V main power supply(Agilent N5752A)
2. Connection for the NI USB 6501 device
3. The CHA of the BNC 575 Pulse Generator is connected to the coolMOS Q1 throw this point
4. The CHB of the BNC 575 Pulse Generator is connected to the coolMOS Q2 throw this point
5. This connector takes the voltage on the capacitors bank and brings that to the DUT inside the wafer station
6. Interlock connector

In fig 5.29 you can see the station on wafer level.

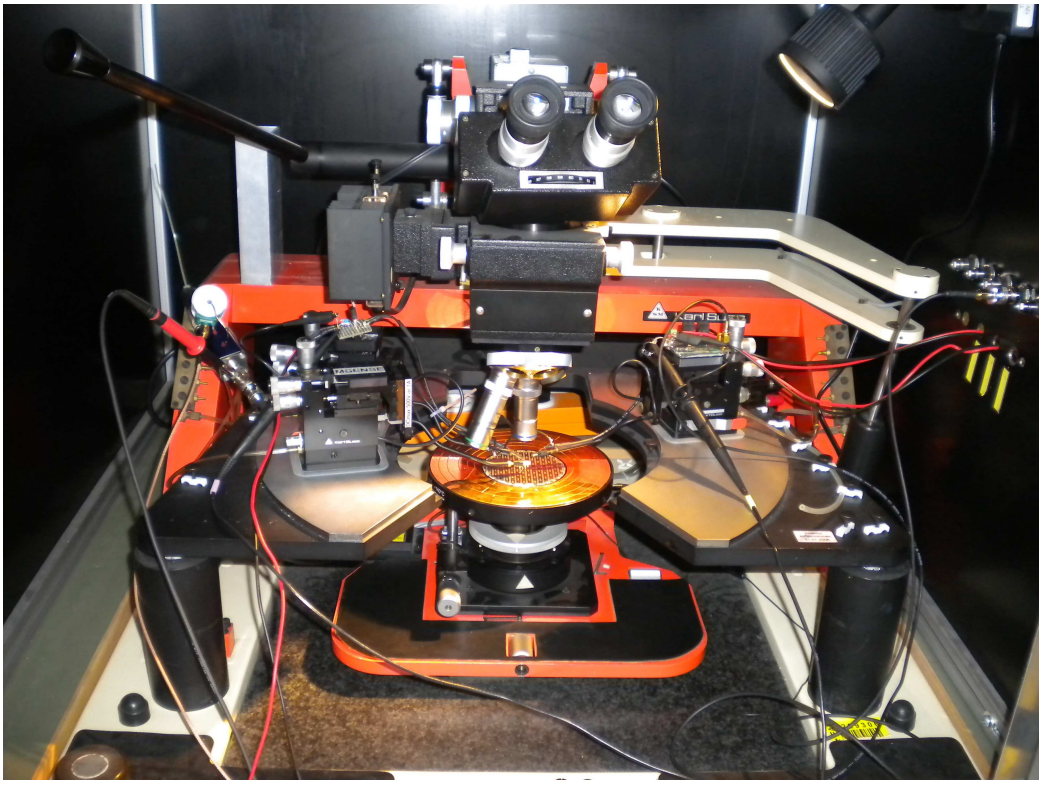

Figure 5.29: GaN DReaM Setup; Probe Station.

Chapter 6

Dynamic Rdson Measurements

This chapter includes the measurements on normally-on and normally-off GaN power HEMTs. Thanks to the GaN DReaM Setup (chapter 5), we are able to measure the dynamic Rdson of the devices, which is compared to the static Rdson, in order to evaluate the Rdson degradation. The measurements are done on devices both on package and on wafer level.

6.1 Measurements on Package Level

This section includes the measurements on GaN-based HEMTs on package level, in order to understand the influence of different parameters on the degradation of the dynamic Rdson.

6.1.1 Reference Point : Silicon CoolMOS

Before doing measurements on GaN-based HEMTs, we want to verify the degree of reliability of our GaN DReaM Setup. Since that, we take a silicon coolMOS as reference point for all the next measurements on GaN-based HEMTs. Silicon transistors, thanks to their structure, do not show any trapping effect. For this reason the dynamic rdson value of silicon transistors is equal to the static one under every condition, such as different t_{on} or t_{off} time of the device and different temperatures. The silicon coolMOS that we take as reference point has a breakdown voltage equal to 600V. First of all

we measure the static Rdson throw the Tektronix Curve Tracer (fig 6.1):

$$StaticRdsonCoolMOS = 94m\Omega \tag{6.1}$$

Figure 6.1: Tektronix Curve Tracer.

next step is to evaluate the dynamic Rdson of the silicon coolMOS and to compare that with the static one. As for the dynamic measurement, done with the GaN DReaM Setup, the gate-source signal applied to the silicon coolMOS can be describe in the following way:

$$ton_{VGS} = 5\mu sec$$

$$toff_{VGS} = 100\mu sec$$

$$VGS_{OFF} = 0V$$

$$VGS_{ON} = +10V$$

The gate signal, read from the oscilloscope, is shown in fig 6.2. The value of ton_{VGS} and $toff_{VGS}$ are chosen so that ton_{VGS} is quite short: ton_{VGS} cannot be smaller than $300-500nsec$, beacause of the overshoot of the signals during the commutation (as you can notice in fig 4.7); this value is not fixed and it depends on how fast the device is able to switch on. $toff_{VGS}$ is long enough so that the Rdson degradation is visible (pag 44). We measured the dynamic Rdson of the silicon coolMOS, thanks to the GaN DReaM Setup,

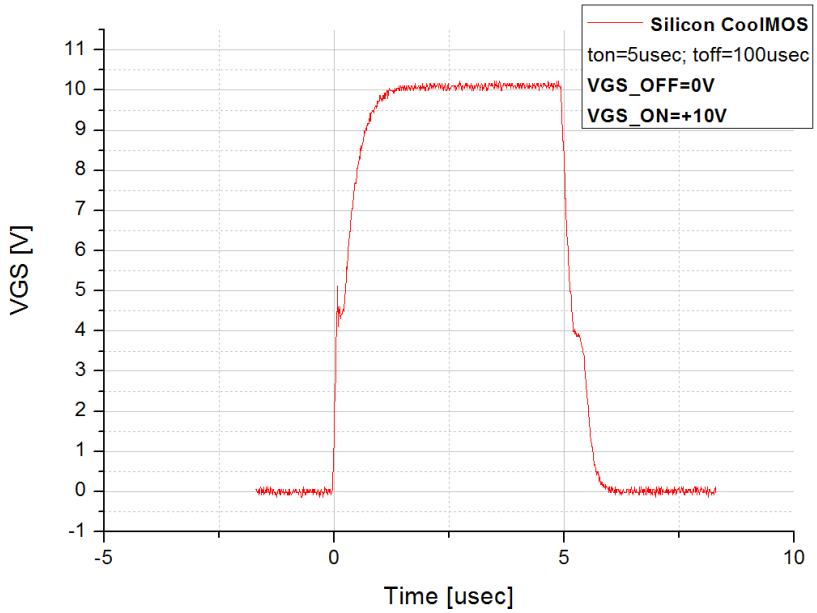

Figure 6.2: Gate Signal applied on the silicon coolMOS; the Miller plateau is well visible.

by applying:

- $IDS = 5A$ (we measure all the devices with the same current ($IDS = 5A$), in order to have the possibility of comparing the results)
- $VDS = 50V - 500V$ with $step = 50V$

The value of dynamic Rdson is read approximately in correspondence of the end of the gate pulse (approximately $5\mu sec$ after the switching-on) and it is calculated as follows:

$$DynamicRdson = \frac{VDS_{Clamped}}{IDS} \tag{6.2}$$

In the graphs in fig 6.3, 6.4, 6.5, 6.6 and 6.7 you can see the waveforms of VDS, VDS Clamped and IDS read from the oscilloscope; the value of dynamic Rdson is calculated for different values of the applied drain-source voltage.

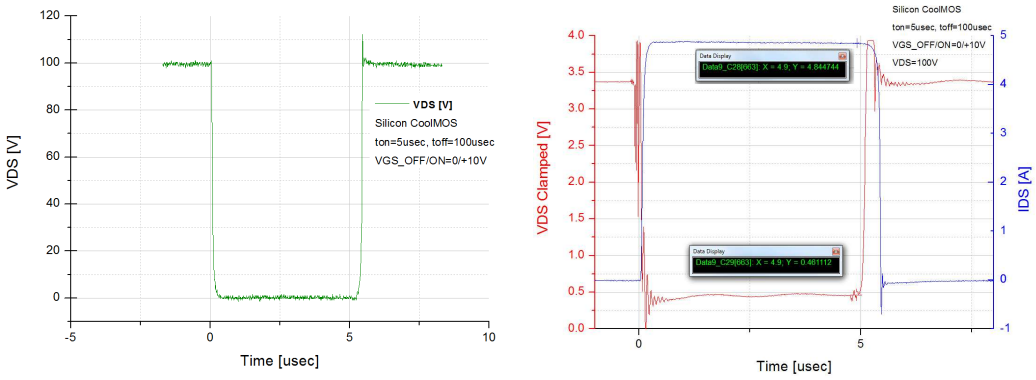

Figure 6.3: Silicon CoolMOS (reference point): VDS=100V (on the left); VDS Clamped and IDS signals (on the right). $DynamicRdson = \frac{VDS_{Clamped}}{IDS} = \frac{0.46V}{4.84A} = 95m\Omega$ at VDS=100V.

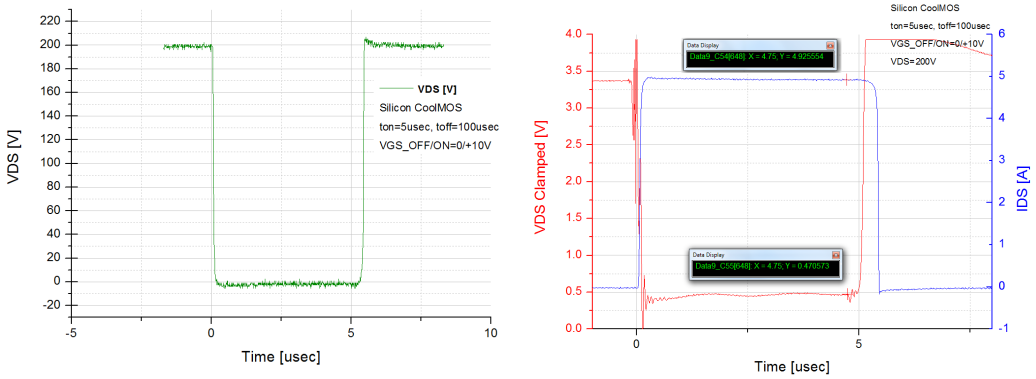

Figure 6.4: Silicon CoolMOS (reference point): VDS=200V (on the left); VDS Clamped and IDS (on the right). $DynamicRdson = \frac{VDS_{Clamped}}{IDS} = \frac{0.47V}{4.92A} = 95.5m\Omega$ at VDS=200V.

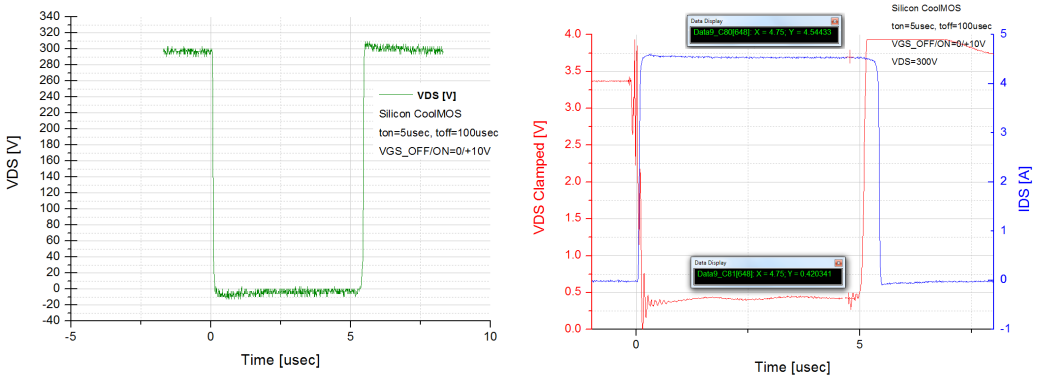

Figure 6.5: Silicon CoolMOS (reference point): VDS=300V (on the left); VDS Clamped and IDS (on the right). $DynamicRdson = \frac{VDS_{Clamped}}{IDS} = \frac{0.42V}{4.54A} = 92.5m\Omega$ at VDS=300V.

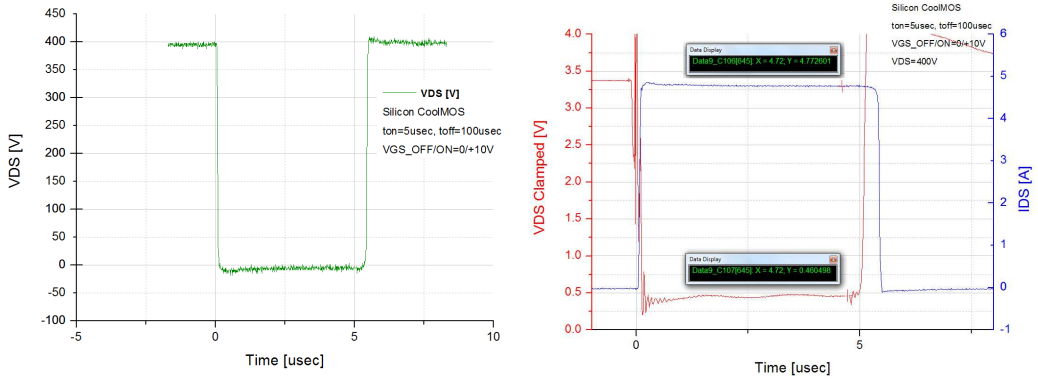

Figure 6.6: Silicon CoolMOS (reference point): VDS=400V (on the left); VDS Clamped and IDS (on the right). $DynamicRdson = \frac{VDS_{Clamped}}{IDS} = \frac{0.46V}{4.77A} = 96.4m\Omega$ at VDS=400V.

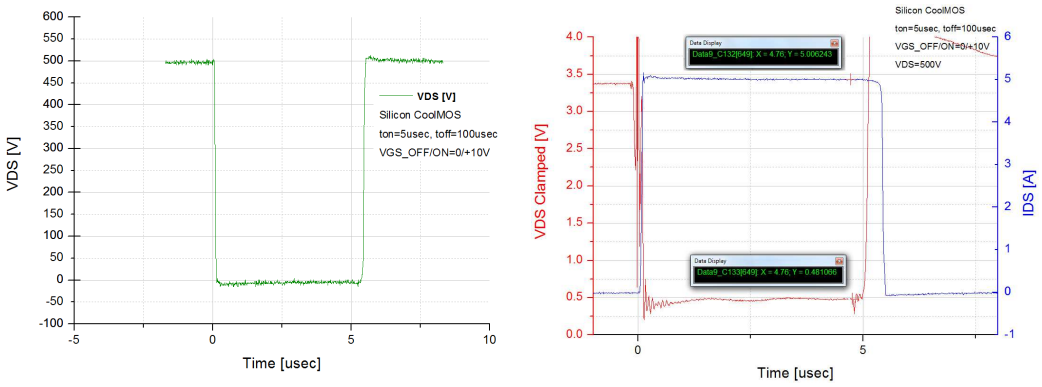

Figure 6.7: Silicon CoolMOS (reference point): VDS=500V (on the left); VDS Clamped and IDS (on the right). $DynamicRdson = \frac{VDS_{Clamped}}{IDS} = \frac{0.48V}{5A} = 96m\Omega$ at VDS=500V.

In fig 6.8 you can see the percentage increase of the dynamic Rdson in the silicon coolMOS, comparing with the static one, shown in function of the drain-source voltage: as you can notice, there is no Rdson degradation under dynamic conditions: the dynamic rdson is constant up to $VDS = 500V$ and it coincides with the static value (pag 101). Thanks to this measurement, we are able to benchmark the dynamic Rdson set-up, since the dynamic Rdson and static Rdson values are equal.

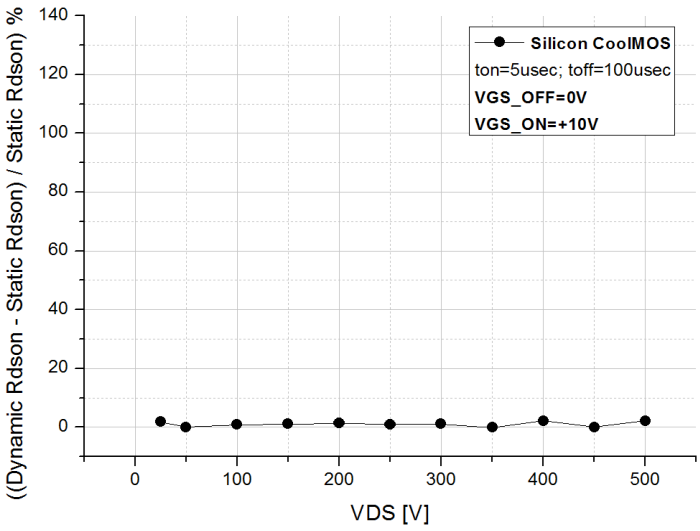

Figure 6.8: Silicon CoolMOS : Percentage Increase of the Dynamic Rdson, comparing with the static one, versus the drain-source voltage.

6.1.2 Influence of the Drain-Source Voltage on the Degradation of the Dynamic Rdson

In this subsection we will see the behaviour of some GaN-based HEMTs in terms of degradation of the Rdson for different drain-source voltages.
In all the dynamic measurements, done with the GaN DReaM Setup and shown in this chapter, we force the same drain-source current:

$$IDS = 5A$$

in order to have the possibility to compare all the results.
First of all it is important to have a static characterization of the devices, in order to understand their peculiarities, before doing dynamic measurements. In fig 6.9 you can see the output and transfer characteristics of the sample C, measured with the Parameter Analyzer (fig 6.10 (a)).

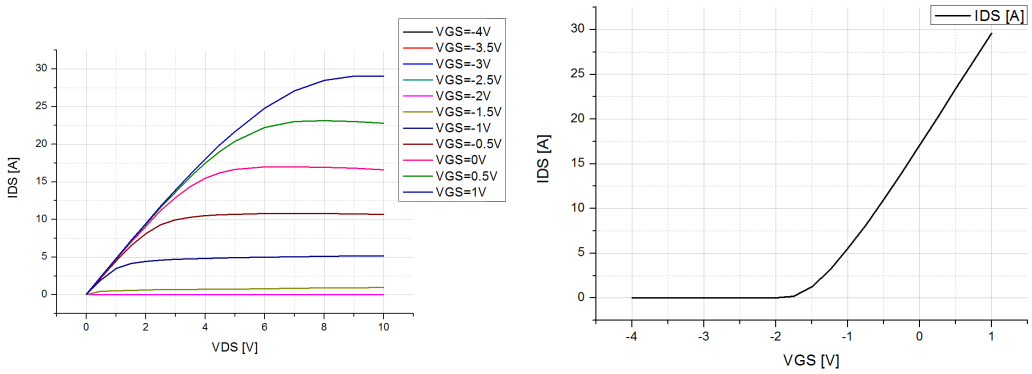

Figure 6.9: Sample C: Output (on the left) and Transfer Characterisctic (on the right).

The graph on the left side in fig 6.11 shows the static Rdson of the sample C, expressed in function of IDS, for different values of VGS; this graph gives us the possibility to directly read the value of static Rdson of the device, simply depending on the value of VGS and IDS we are using. As for the sample C, we are interested in calculating the static Rdson in the same conditions we set in the GaN DReaM Setup, with the aim of being able,

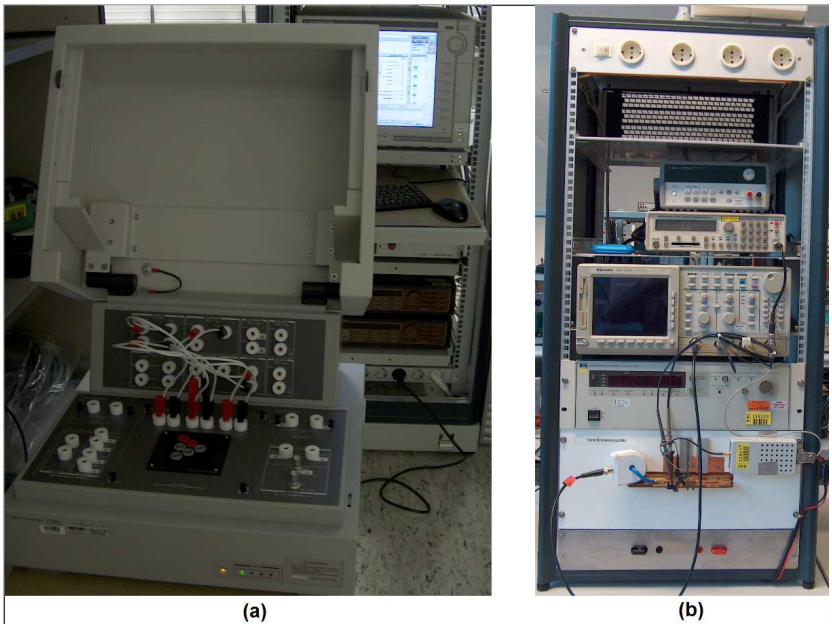

Figure 6.10: Parameter Analyzer (a) and Output Transfer Station (b) used for the DC measurements.

later, to compare dynamic and static Rdson value:

- $VGS_{ON} = 1V$
- $IDS = 5A$

Sample C is a normally-on device with a V_{th} in the range of -1.7V. As you can see from the graph on the right side in fig 6.11, we obtain:

$$StaticRdsonSampleC = 187.7m\Omega \tag{6.3}$$

After have evaluated the static features of the device, we use the GaN DReaM Setup, in order to measure the dynamic Rdson for different values of VDS. The measurements is done in the following conditions:

- $IDS = 5A$
- $VGS_{OFF} = -4V$; $VGS_{ON} = +1V$

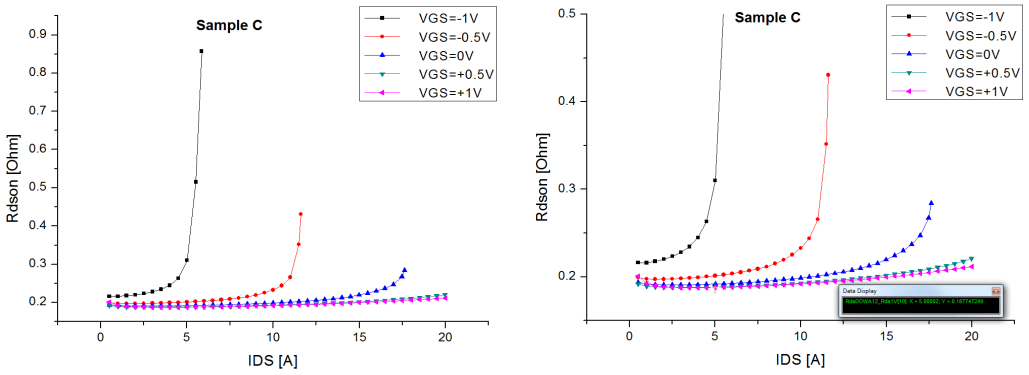

Figure 6.11: Sample C: Rdson vs Ids characterisctics, measured for different value of VGS (on the left); the same graph is then zoomed (on the right), in order to better calculate the static Rdson of the device at $IDS = 5A$.

The result of the dynamic measurement is shown in fig 6.12. While the drain-source voltage applied in off-state is increasing, the electric field between gate and drain increments too, so that the trapping effect is more pronounced and thus the current collapse increases. As you can see in fig 6.12, the sample C shows a high level of degradation of the dynamic Rdson while the drain-source voltage is increasing, infact the dynamic Rdson shows a gradual increment, comparing with the static value, that reaches the 155% at VDS=525V.

Fig 6.13 shows the waveforms read from the oscilloscope at VDS=525V. The value of dynamic Rdson at VDS=525V is read approximately in correspondence of the end of the gate pulse (approximately $5\mu s$ after the switching-on) and it is calculated as follows:

$$DynamicRdson = \frac{VDS_{Clamped}}{IDS} = \frac{2.47V}{5.19A} \approx 480m\Omega \tag{6.4}$$

Referring to the graph in fig 6.12, at VDS=525 the percentage increment of the dynamic Rdson, comparing with the static value, is given by the following equation:

$$\frac{DynamicRdson - StaticRdson}{StaticRdson}\% = \frac{480m\Omega - 187.7m\Omega}{187.7m\Omega}\% = \approx 155\% \tag{6.5}$$

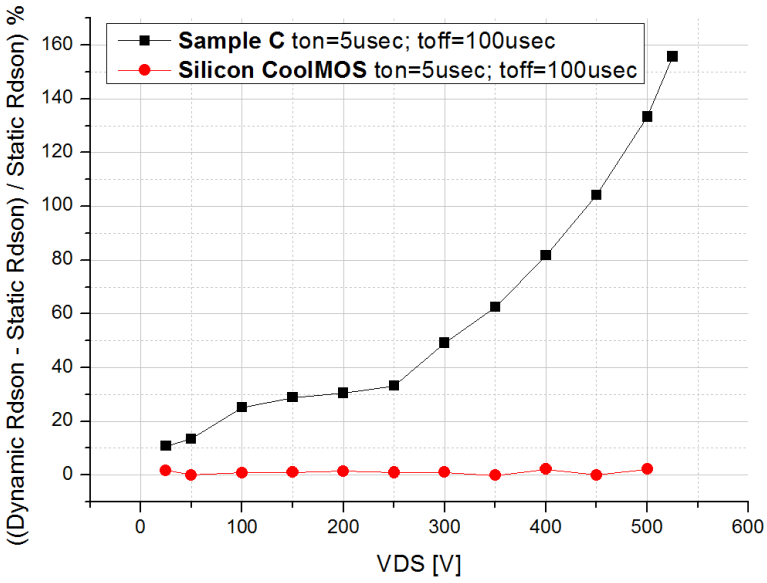

Figure 6.12: Sample C, Influence of the Drain-Source Voltage on the Degradation of the Dynamic Rdson: The percentage increment of the dynamic Rdson, comparing with the static one, is evaluated throw the GaN DReaM Setup and expressed versus VDS.

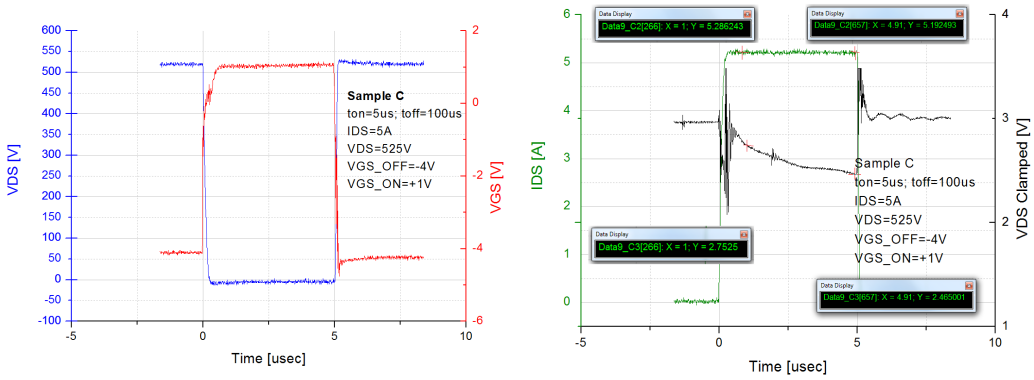

Figure 6.13: Sample C, Influence of the Drain-Source Voltage on the Degradation of the Dynamic Rdson: VGS and VDS (on the left) and IDS and VDS Clamped (on the right) registered from the oscilloscope at VDS=525V.

Clearly, it is also possible to read the Rdson at, for example, $t_{on} = 1usec.$ In that case $DynamicRdson \approx 520m\Omega$ which corresponds to a percentage increment of the dynamic Rdson equal to $\approx 180\%$ The reason is that the shorter is the t_{on}, the smaller is the number of electrons detrapped. We have just analyzed the bahaviour of the sample C in function of the drain-source voltage. Now let us see the behaviour of the sample D, always maintaining the same value of the drain-source current: $IDS = 5A$. In fig 6.14 you can see the output characteristic of the sample D, measured with the Parameter Analyzer (fig 6.10 (a)). Fig 6.15 shows the static Rdson of the sample D, expressed in function of IDS, for different value of VGS. As for the sample D, we are interested in calculating the static Rdson in the same conditions we set for the dynamic measurement, with the aim of being able, later, to compare dynamic and static Rdson value:

- $VGS_{OFF} = 0V$; $VGS_{ON} = 4V$
- $IDS = 5A$

Sample D is a normally-off device. As you can see from the graph on the right in fig 6.15, we obtain:

$$StaticRdsonSampleD = 82.3m\Omega \tag{6.6}$$

After have evaluated the static features of the device, we use the GaN DReaM Setup, in order to measure the dynamic Rdson for different values of VDS; the result of the measurement is shown in fig 6.16. While the drain-source voltage is increasing, the electric field between gate and drain increments too, so that the current collapse increases. As you can see in fig 6.16, the sample D shows a low and constant level of degradation of the dynamic Rdson (23%) while the drain-source voltage is increasing. It is clear that the current collapse effect is already present at $VDS = 50V$, that corresponds to a dynamic Rdson increase of 20%. After that no further increase is observed anymore. Most probably, all the traps are already filled just applying $VDS = 50V$. A better understanding is needed in order to comprehend

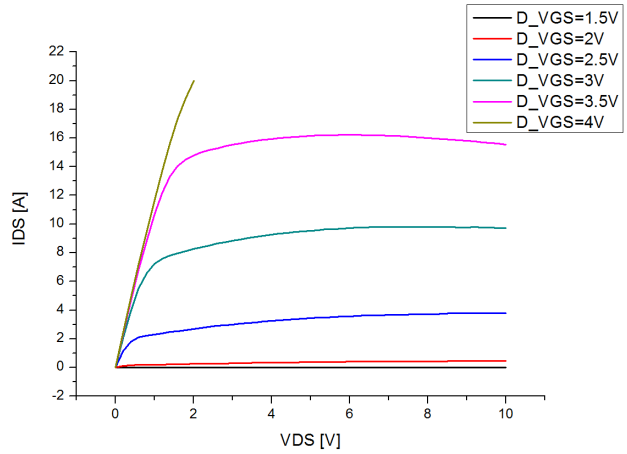

Figure 6.14: Sample D: Output Characteristic.

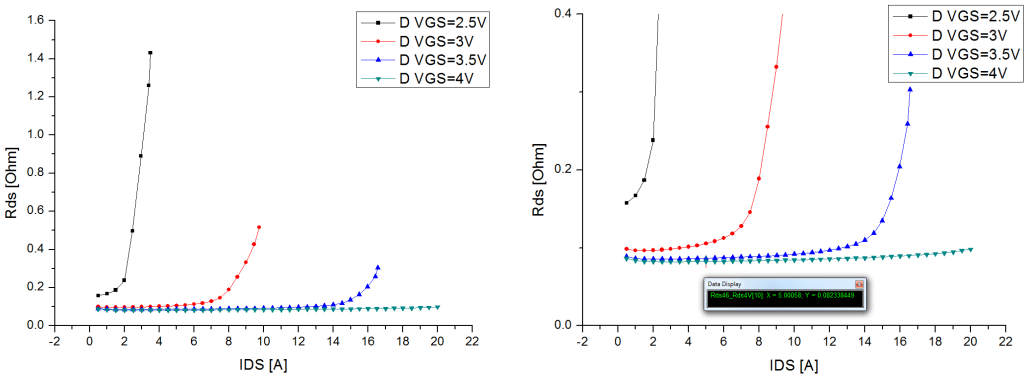

Figure 6.15: Sample D: Rdson vs Ids characterisctic measured for different VGS (on the left); the same graph is then zoomed (on the right), in order to have a better resolution to calculate the static Rdson of the device at $IDS = 5A$.

the trapping behaviour, but for that Diva-Like set-up (double set-up) would be needed.

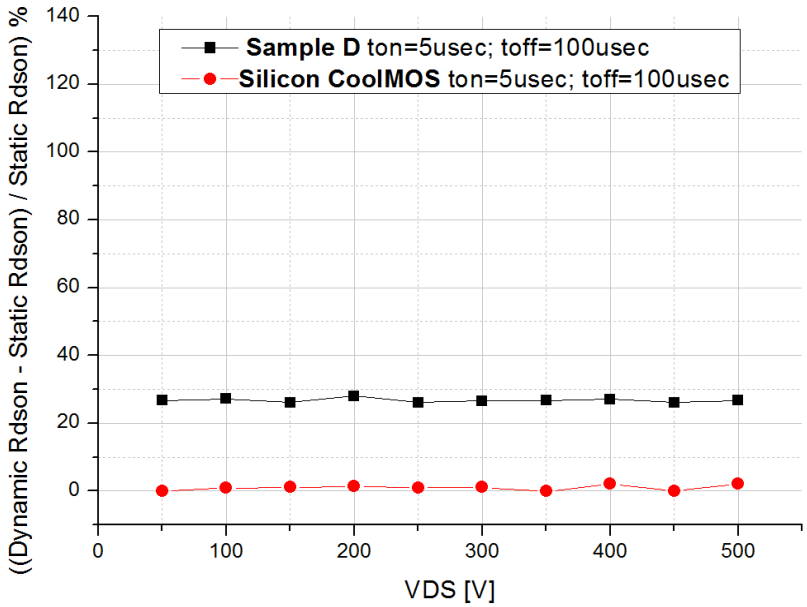

Figure 6.16: Sample D, Influence of the Drain-Source Voltage on the Degradation of the Dynamic Rdson: The Dynamic Rdson, evaluated with the GaN DReaM Setup, is expressed versus VDS.

Fig 6.17 shows the waveforms read from the oscilloscope at VDS=250V. The value of dynamic Rdson is read approximately in correspondence of the end of the gate pulse (approximately $5\mu s$ after the switching-on) and it is calculated as follows:

$$DynamicRdson = \frac{VDS_{Clamped}}{IDS} = \frac{0.5V}{4.95A} \approx 101m\Omega \tag{6.7}$$

Referring to the graph in fig 6.16, at VDS=250 the percentage increment of the dynamic Rdson, comparing with the static value, is given by the following equation:

$$\frac{DynamicRdson - StaticRdson}{StaticRdson}\% = \frac{101m\Omega - 82.3m\Omega}{82.3m\Omega}\% = \approx 23\% \tag{6.8}$$

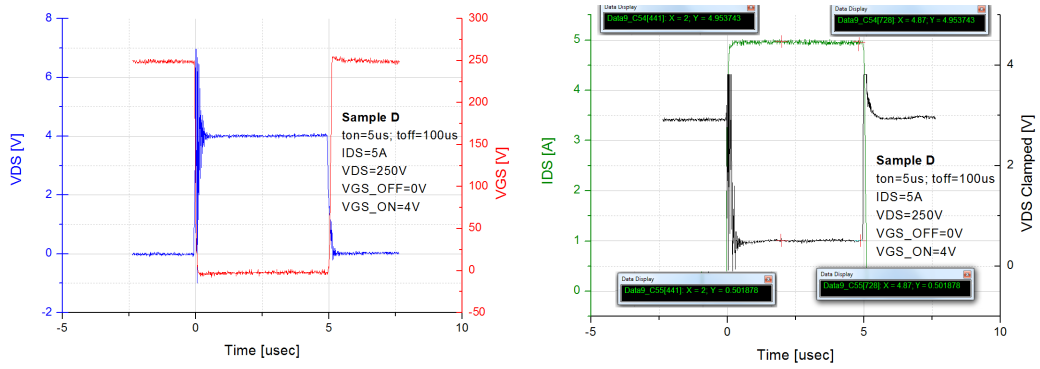

Figure 6.17: Sample D: VGS and VDS (on the left) and IDS and VDS Clamped (on the right) registered from the oscilloscope at VDS=250V.

Clearly, it is also possible to read the Rdson at, for example, $t_{on} = 2usec$. In that case $DynamicRdson \approx 101m\Omega$, that is exactly the same value we measured at $t_{on} = 5usec$. Until now we have seen some examples of devices in which the current collapse is well visible (fig 6.12) and others in which it is small and constant with VDS (fig 6.16). In the following we will see some examples of devices showing severe current collapse effect. In fig 6.18, 6.19, 6.20 and 6.21 you can see the output and transfer characteristics of the samples F1, F2, F3 and F4, measured with the Output Transfer Tester (fig 6.10 (b)).

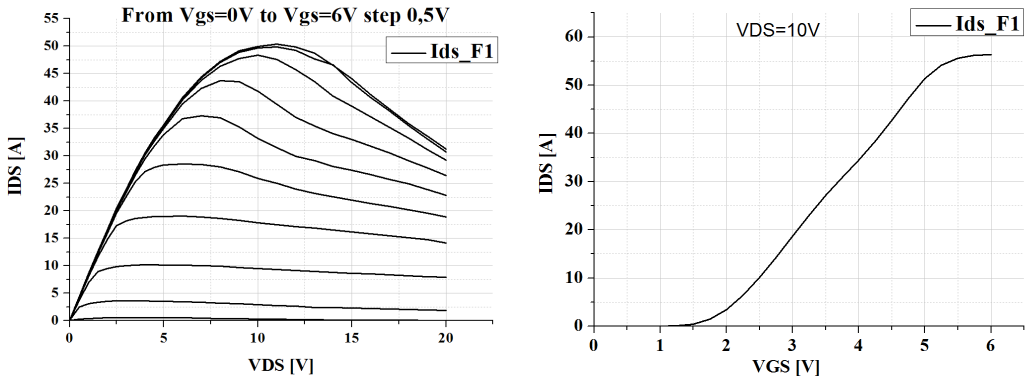

Figure 6.18: Sample F: Output (on the left) and Transfer Characteristic (on the right).

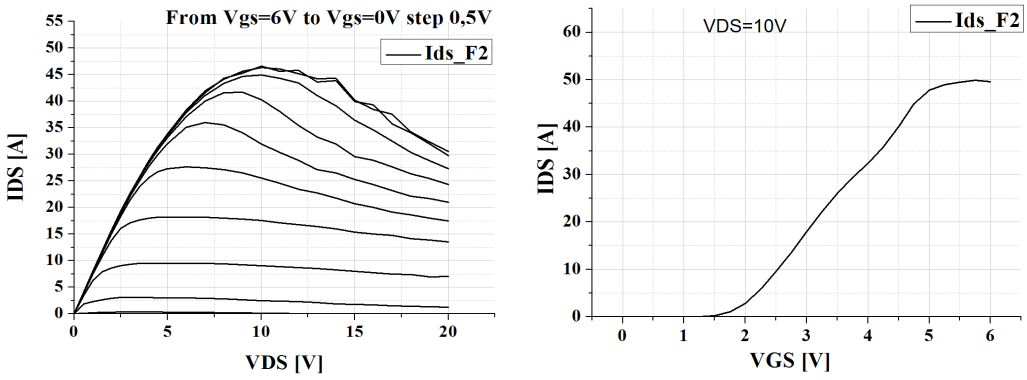

Figure 6.19: Sample F: Output (on the left) and Transfer Characteristic (on the right).

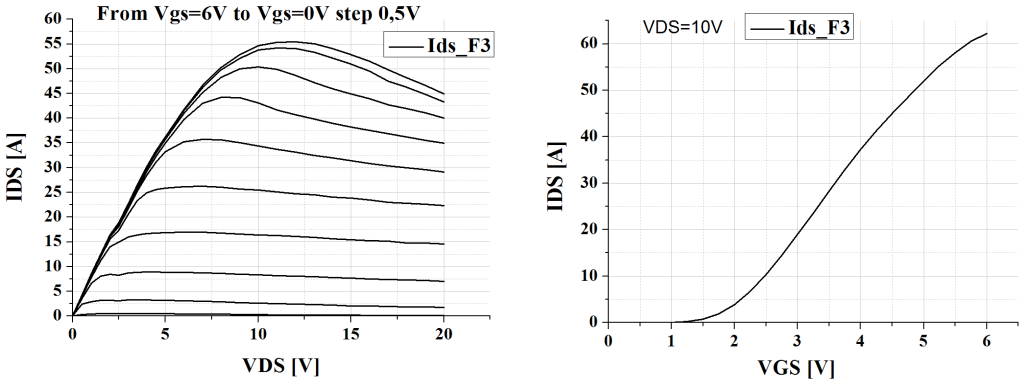

Figure 6.20: Sample F: Output (on the left) and Transfer Characteristic (on the right).

F1, F2, F3, F4 are normally-off devices. After have evaluated the static features of the devices, we use the GaN DReaM Setup, in order to measure the dynamic Rdson for different values of the drain-source voltage: the result of the measurements are shown in fig 6.22 and then zoomed in fig 6.23. As you can see in fig 6.22 and 6.23, the samples of type F show a huge degradation of the dynamic Rdson, while the drain-source voltage is increasing: at VDS=200V the dynamic Rdson corresponds to three times the static Rdson value, in the best case, where as, in the worst case, it corresponds to 850 times the static Rdson value. This huge Rdson collapse is related to the C-doping

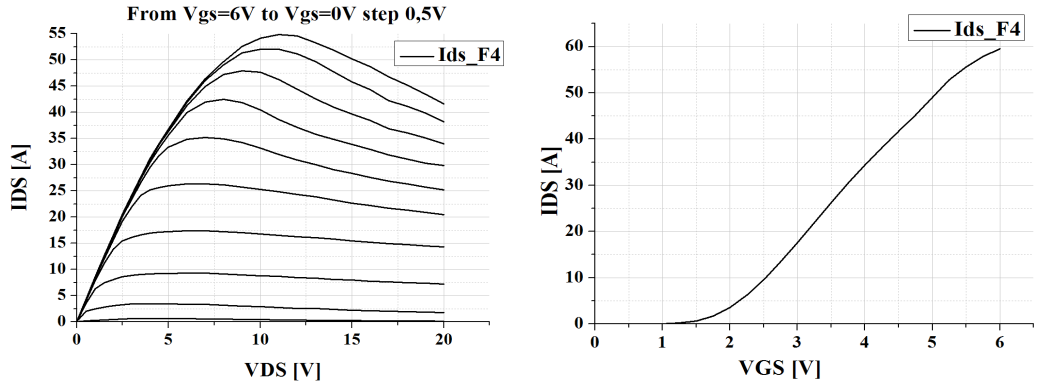

Figure 6.21: Sample F: Output (on the left) and Transfer Characteristic (on the right).

of the buffer. Deep buffer acceptors help to increase the breakdown strength of AlGaN/GaN HFETs, but act as dominating source for increased dynamic Rdson. The reason of such a huge spread in values could be attributed to a not-uniform doping level in the buffer.

Fig 6.24 shows the waveforms of the sample F1_#14 read from the oscilloscope at VDS=200V. The value of dynamic Rdson at VDS=200V is read approximately in correspondence of the end of the gate pulse (approximately $5\mu sec$ after the switching-on) and it is calculated as follows:

$$DynamicRdson = \frac{VDS}{IDS} = \frac{129.75V}{1.68A} \approx 76\Omega \tag{6.9}$$

At VDS=200 the rate between dynamic and static Rdson is given by the following equation:

$$\frac{DynamicRdson}{StaticRdson} = \frac{76\Omega}{89.44m\Omega} = \approx 850 \tag{6.10}$$

Where the static Rdson is evaluated throw the Static Tester M3020, shown in fig 4.9.

The graphs in fig 6.25 are referred to the sample F1_#14 too; they show the sequence of VDS (on the left) and IDS waveforms (on the right) registered from the oscilloscope at $VDS = 50V, 100V, 150V, 250V$. As you can see,

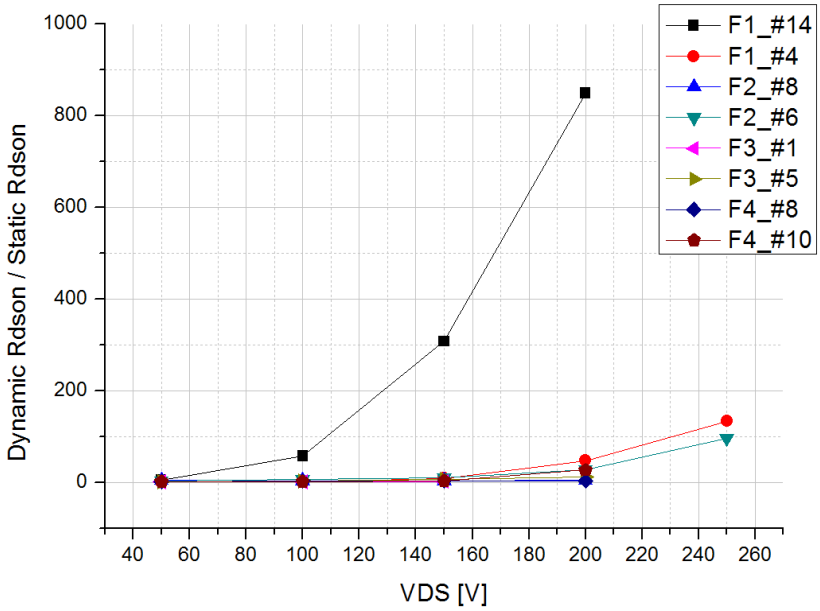

Figure 6.22: Samples of type F, Influence of the Drain-Source Voltage on the Degradation of the Dynamic Rdson: The Dynamic Rdson, evaluated with the GaN DReaM Setup, is expressed versus VDS.

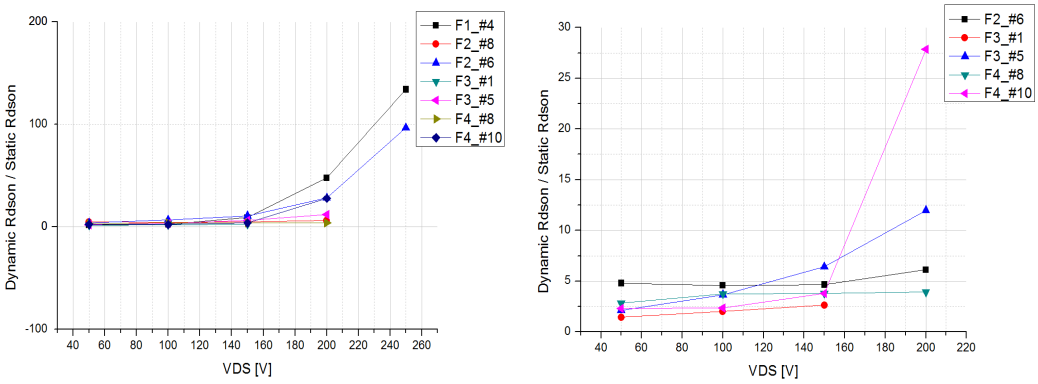

Figure 6.23: Samples of type F, Influence of the Drain-Source Voltage on the Degra- dation of the Dynamic Rdson : The Dynamic Rdson, evaluated with the GaN DReaM Setup, is expressed versus VDS (on the left); the same graph is then zoomed (on the right).

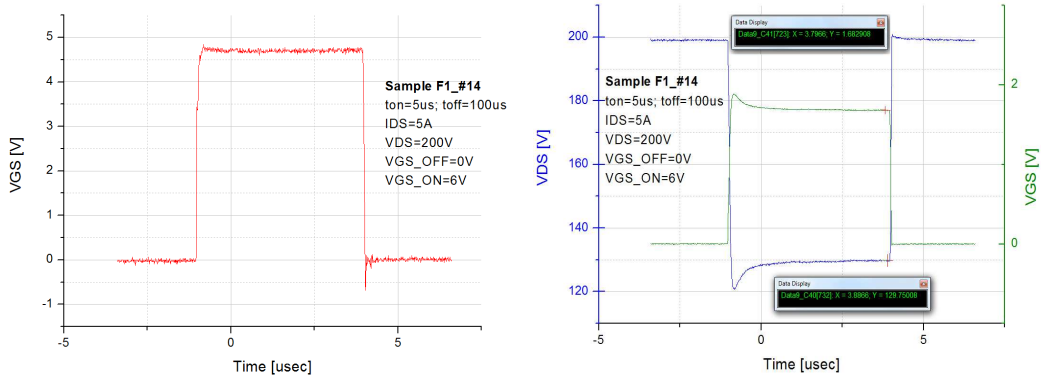

Figure 6.24: Sample F1_#14: VGS and VDS (on the left) and IDS and VDS Clamped (on the right) registered from the oscilloscope at VDS=250V.

the Rdson collapse is really huge: VDS_{on} increases really fast: it passes from $VDS_{on} = 2.5V$, at $VDS_{off} = 50V$, to $VDS_{on} = 130V$, at $VDS_{off} = 200V$. In the meanwhile IDS decreases really fast, by passing from $IDS = 4.5A$, at $VDS_{off} = 50V$, to $IDS = 1.68A$, at $VDS_{off} = 200V$. For this measurement we used a 15V Zener Diode for the clamping circuit. As you can see from the VDS_{on} values read, the VDS read on the clamping circuit is already saturated after have switched from $VDS_{off} = 50V$ to $VDS_{off} = 100V$, infact VDS_{on} passes from $VDS_{on} = 2.5V$ to $VDS_{on} = 20V$; For this reason the values of VDS between $VDS_{off} = 100V$ and $VDS_{off} = 200V$ have been read without clamping circuit, directly from the VDS signal. The graphs in fig 6.26 are referred to the sample F1_#4. The graph on the left in fig 6.26 shows a sequence of pictures, representing VDS Clamped, registered from the oscilloscope every 10s and at VDS=200V; it gives an idea of how fast at VDS=200V the VDS measured on the 15V Zener diode reaches the saturation. In the graph on the right side in fig 6.26 are shown the waveforms of IDS and VDS of the sample F1_#4 read from the oscilloscope at VDS=200V. The graphs in fig 6.27 are referred to the sample F1_#4 too. The graph on the left in fig 6.27 shows a sequence of pictures, representing VDS and registered from the oscilloscope every 10s and at VDS=250V; it gives an idea of how fast at VDS=250V the VDS increases, when the VDS read on the zener diode is already saturated. In the graph on the right in

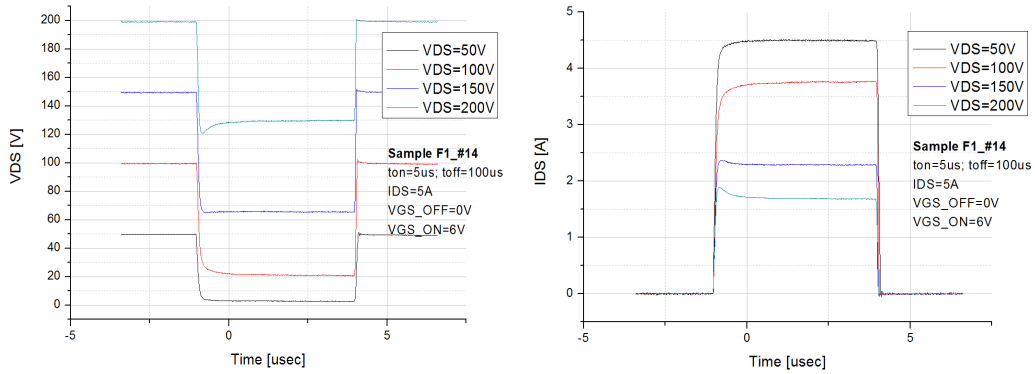

Figure 6.25: Sample F1_#14 : sequence of VDS (on the left) and IDS waveforms (on the right) registered from the oscilloscope at $VDS = 50V, 100V, 150V, 250V$.

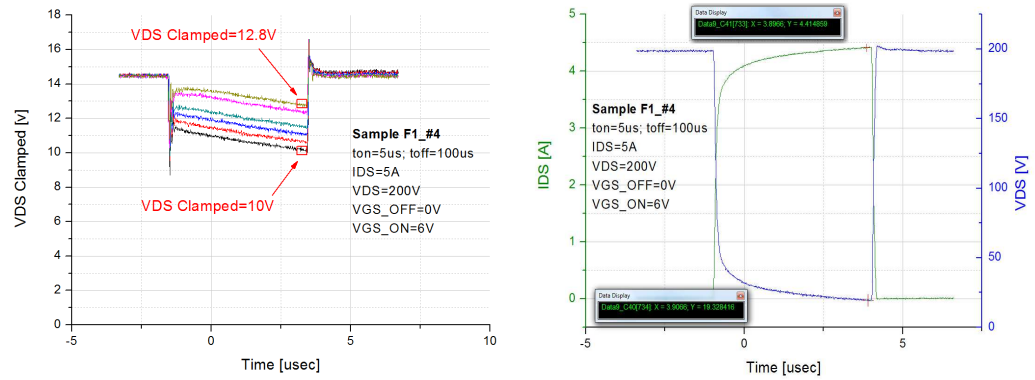

Figure 6.26: Sample F1_#4 : pictures of VDS Clamped registered from the oscilloscope every 10s at VDS=200V (on the left); IDS and VDS Clamped at VDS=200V (on the right).

fig 6.27 are shown the waveforms of IDS and VDS of the sample F1_#4 read from the oscilloscope at VDS=250V. Now let us see the behaviour of the

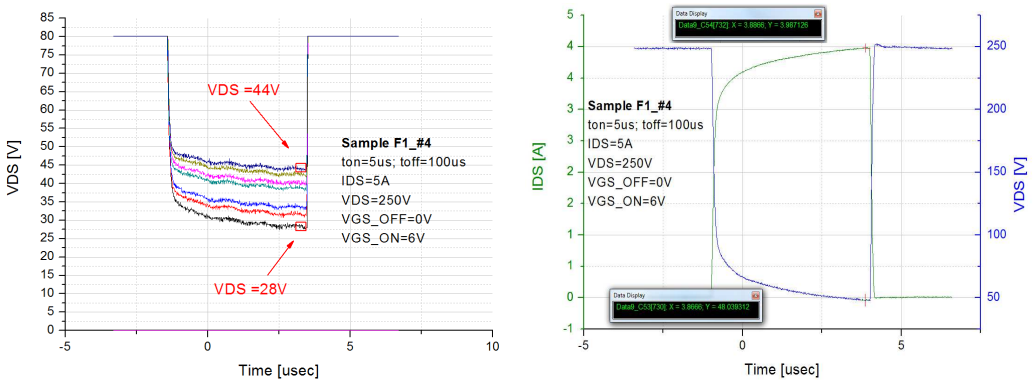

Figure 6.27: Sample F1_#4 : pictures of VDS registered from the oscilloscope every 10s at VDS=250V (on the left); IDS and VDS at VDS=250V (on the right).

the samples E_Source Down and E_Drain Down. These two samples have no difference on wafer level, the only difference can be found on package level. Fig 6.28 shows a simplified schematic of the connections of the devices on package level. In fig 6.28(a) you can se the connections of the sample E_Source Down on package level: the drain is connected to the package: this type of connection makes the package behave like a second source-fieldplate (fig 6.29 (a)).
Regarding to the sample E_Drain Down, the connections on package level are shown in fig 6.28 (b): this type of connection makes the package behave like an extension of the drain contact (fig 6.29 (b)). This difference in the connections on package level brings the following effects:

- The source-down connection, behaving like a double source-fieldplate, brings less current collapse effect, comparing with the drain-down connection, that, on the opposite, makes the electrical field between gate and drain increase.

- The source-down connection brings a decrease in the gate-drain capacitance CGD and an increase in the output capacitance CDS (and

Coss=CDS+CGD), comparing with the drain-down connection.

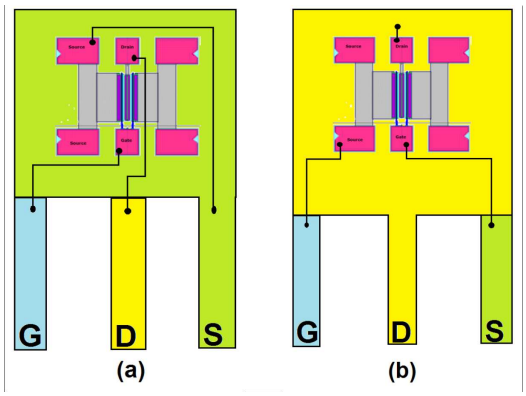

Figure 6.28: Samples E_Source Down, E_Drain Down : Simplified Schematic of the Connections on Package Level: Source Down (a), Drain Down (b).

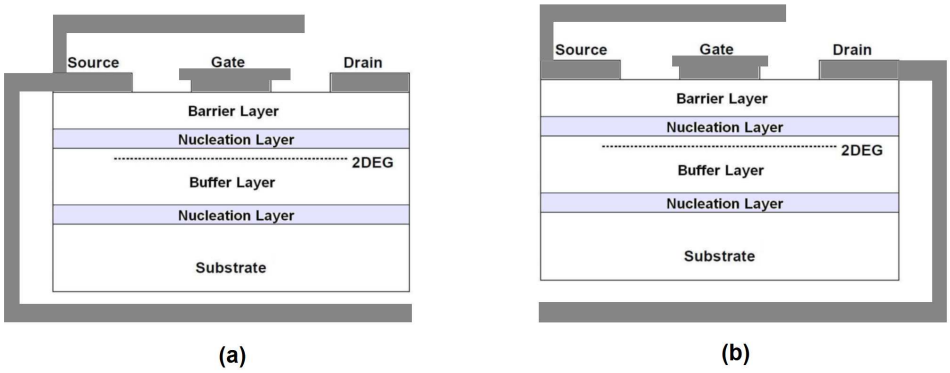

Figure 6.29: Samples E_Source Down, E_Drain Down : Simplified Schematic describing the effects of the Connections on Package Level: Source Down (a), Drain Down (b).

The capacitance Ciss, Coss and Crss (or CGD) of the samples E_Source Down and E_Drain Down are shown in the graph in fig 6.30. We can conclude:

- $Coss\_E\_DrainDown < Coss\_E\_SourceDown$
- $CGD\_E\_DrainDown > CGD\_E\_SourceDown$

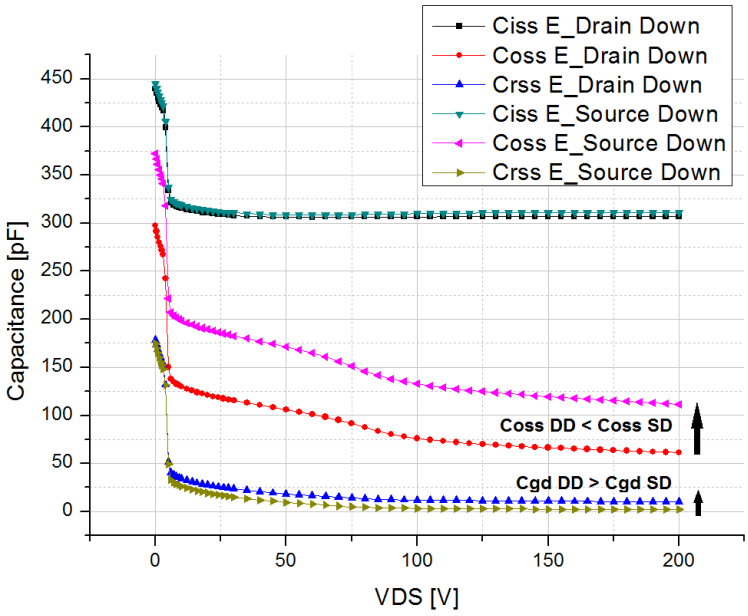

Figure 6.30: Samples E_Source Down, E_Drain Down : Comparison between the capacitances Ciss, Coss, Crss.

As for the current collapse effect, the graph in fig 6.31 shows the percentage increase of the dynamic Rdson of the samples E_Source Down and E_Drain Down, comparing with the static Rdson; as you can see, in E_Drain Down the degradation of Rdson is well visible, whereas E_Source Down shows low and constant level of Rdson degradation (20%). The behaviour of E_Source Down, already seen in the sample D (fig 6.16) means that, already at $VDS = 50V$ all the traps of the device are already filled.

Fig 6.32 shows the waveforms read from the oscilloscope for the samples E_Drain Down at VDS=500V. Referring to the graph in fig 6.31, at VDS=500 the percentage increase of the dynamic Rdson of the sample E_Drain Down, comparing with the static value, is given by the following equation:

$$\frac{DynamicRdson - StaticRdson}{StaticRdson}\% = \frac{173m\Omega - 82m\Omega}{82m\Omega}\% = \approx 110\% \quad (6.11)$$

Where the static Rdson is evaluated throw the Static Tester M3020, shown in fig 4.9.

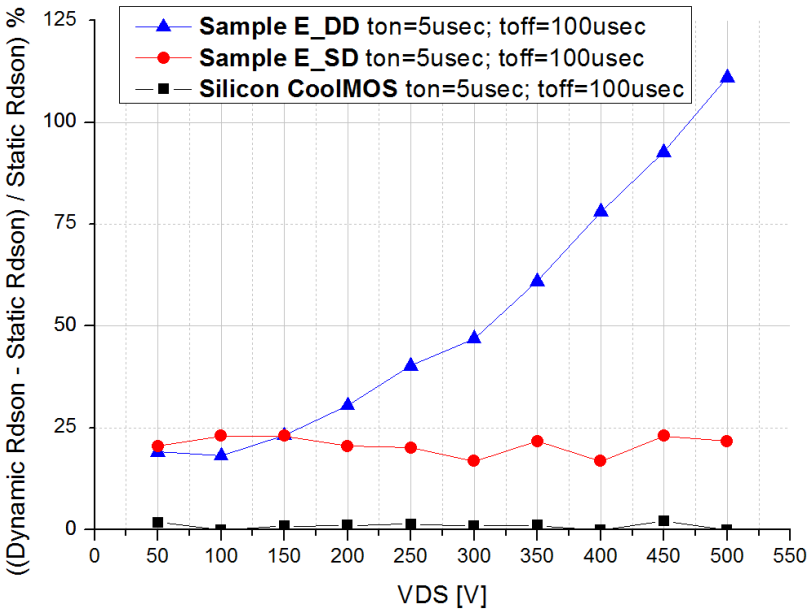

Figure 6.31: Samples E_Source Down, E_Drain Down, Influence of the Drain-Source Voltage on the Degradation of the Dynamic Rdson : The Dynamic Rdson, evaluated with the GaN DReaM Setup, is expressed versus VDS.

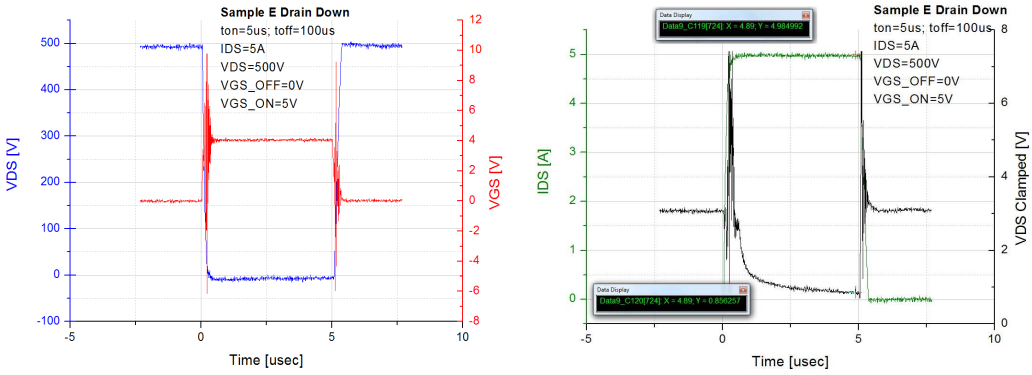

Figure 6.32: Sample E_Drain Down : VGS and VDS (on the left) and IDS and VDS Clamped (on the right) registered from the oscilloscope at VDS=500V.

The graph in fig 6.33 shows the waveforms of the VDS Clamped signal (on the left) and IDS waveforms (on the right) registered from the oscilloscope for the sample E_Drain Down at different VDS values. You can see how the on-state part of VDS Clamped signal goes up with VDS, while IDS shows small variations, that are negligible in the calculation of the dynamic Rdson.

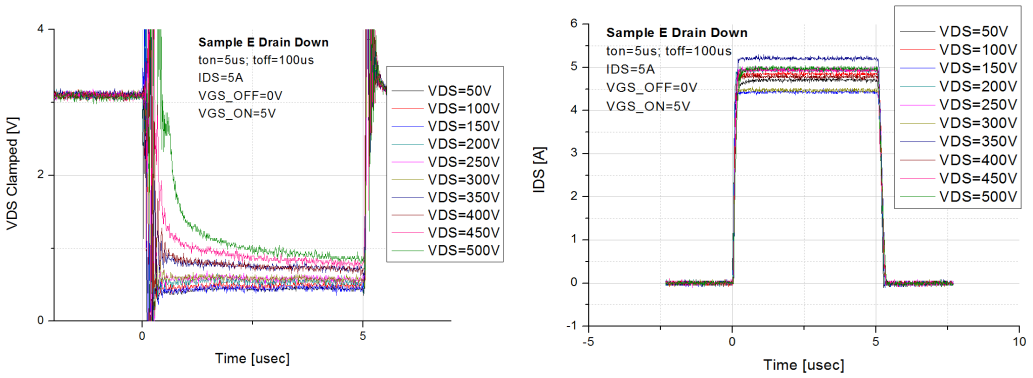

Figure 6.33: Sample E_Drain Down : sequence of VDS Clamped (on the left) and IDS waveforms (on the right) registered from the oscilloscope at different VDS values.

In the graph in fig 6.34 are shown the waveforms of the VDS Clamped signal (on the left) and IDS waveforms (on the right) registered from the oscilloscope for the sample E_Source Down at different VDS values. You can see how the on-state part of VDS Clamped signal is constant, while IDS shows small variations, that are negligible in the calculation of the dynamic Rdson. The current is determined by the drain resisatnce RD. and from the applied VDS. Sometimes it is difficult to find the right RD value, this is the reason why IDS is not constant.

In fig 6.35 are shown the waveforms of the sample E_Source Down read from the oscilloscope at VDS=500V. Referring to the graph in fig 6.31, at VDS=500 the percentage increase of the dynamic Rdson of the sample E_Source Down, comparing with the static value, is given by the following equation:

$$\frac{DynamicRdson - StaticRdson}{StaticRdson}\% = \frac{98m\Omega - 80.5m\Omega}{80.5m\Omega}\% = \approx 21.7\% \quad (6.12)$$

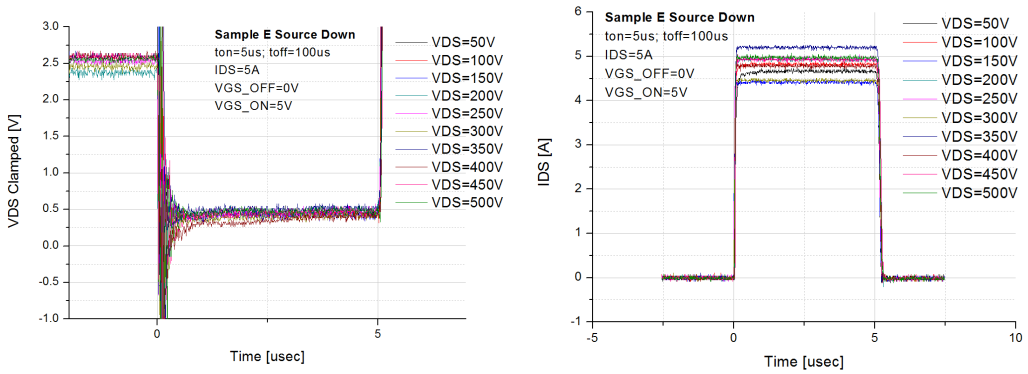

Figure 6.34: Sample E_Source Down : sequence of VDS Clamped (on the left) and IDS waveforms (on the right) registered from the oscilloscope at different VDS values.

Where the static Rdson is evaluated throw the Static Tester M3020, shown in fig 4.9.

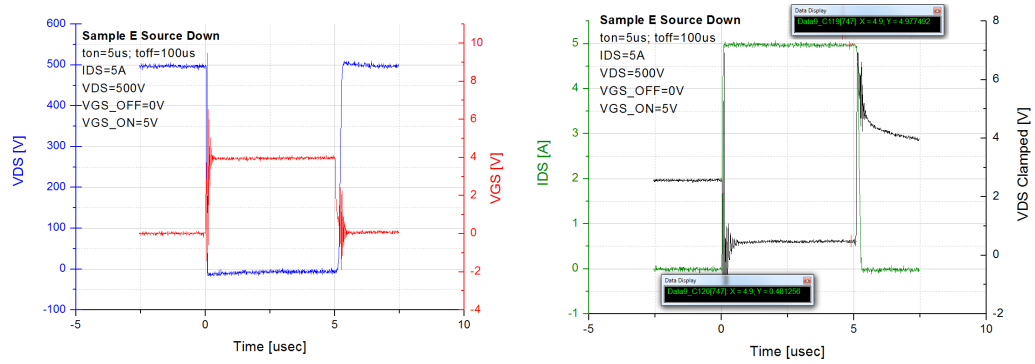

Figure 6.35: Sample E_Source Down : VGS and VDS (on the left) and IDS and VDS Clamped (on the right) registered from the oscilloscope at VDS=500V.

It is important to statistically confirm the trend of the graphs shown in fig 6.31, in order to have the possibility to make a general conclusion. For this reason we measured five samples of the type E_Source Down (fig 6.36 (a)) and five samples of the type E_Drain Down (fig 6.36 (b)). The devices shown in fig 6.36 confirm the trend shown in fig 6.31.

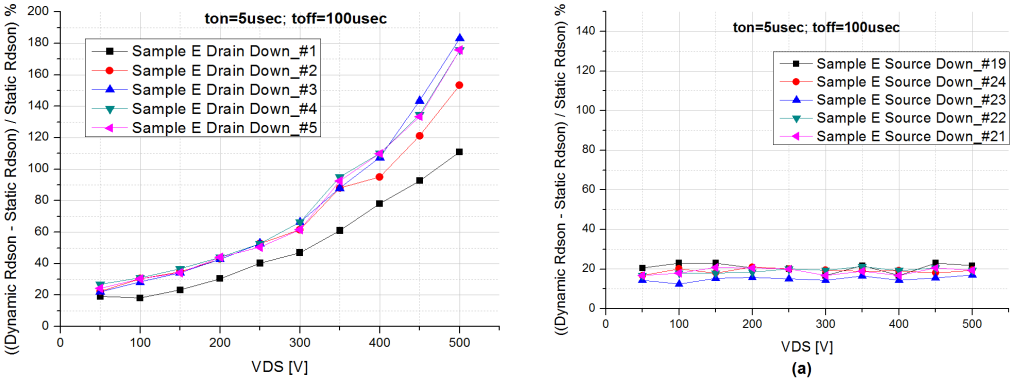

Figure 6.36: Samples E_Source Down, E_Drain Down, Influence of the Drain-Source Voltage on the Degradation of the Dynamic Rdson : The Dynamic Rdson, evaluated with the GaN DReaM Setup, is expressed versus VDS: E_Source Down (a), E_Drain Down (b).

6.1.3 Influence of the Stress Time t_{off} on the Degradation of the Dynamic Rdson

In this section we will discuss the influence of the stress time t_{off} on the degradation of the dynamic Rdson. The measurements shown in sec 6.1.1 have the following settings:

- $ton_{VGS} = 5usec$
- $toff_{VGS} = 100usec$

We want to understand if and how our results change by varying the $toff_{VGS}$ time, while maintaining $ton_{VGS} = 5us$ constant.
At first we will verify how the dynamic Rdson of our devices varies with the following values of the stress time $toff_{VGS}$:

- $toff_{VGS} = 5usec$
- $toff_{VGS} = 100usec$
- $toff_{VGS} = 500usec$

An increase in the time $toff_{VGS}$ corresponds to an increase in the stress time of the device, so that the electric field between gate and drain lasts longer: this means that, in GaN-based HEMTs, the time during which the electrons are kicked out of the channel by the gate-drain electric field increases.
First of all we experiment these measurements on the $94m\Omega$ Silicon CoolMOS used in sec 6.1.1, in order to have a reference for the next measurements. The graph in fig 6.37 shows the rate between dynamic and static Rdson for the Silicon CoolMOS, expressed in function of the drain-source voltage and for different values of the stress time $toff_{VGS}$. As we said at pag 101, the silicon transistors, thanks to their structure, do not show trapping effects or, as we can better say, the trapping effect is so small that anyway it is not found. For this reason in the silicon transistors the dynamic Rdson is equal to the static one under every condition; as the graph in fig 6.37 shows, infact, the Rdson of the Silicon device does not show any change for different value of the stress time $toff_{VGS}$.

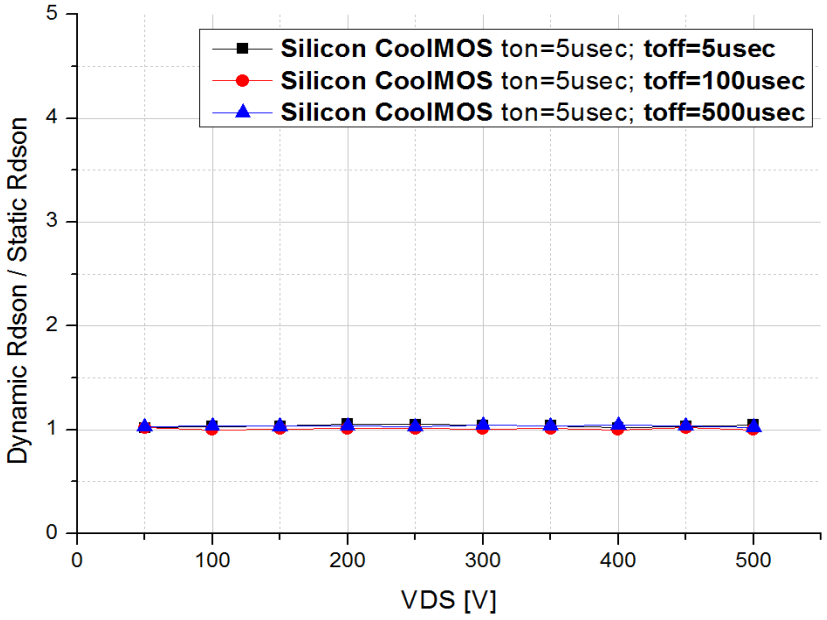

Figure 6.37: Silicon CoolMOS Device : Influence of the Stress Time $toff_{VGS}$ on the Degradation of the Dynamic Rdson.

Now let us see the behaviour of some GaN-based HEMTs for different values of the stress times $toff_{VGS}$. Figure 6.38 shows the influence of the stress time t_{off} on the degradation of the dynamic Rdson for the sample C. As we saw in fig 6.12, the sample C, for $toff_{VGS} = 100usec$, shows a high level of degradation of the dynamic Rdson, while the drain-source voltage is increasing. As we can see in fig 6.38, while the stress time $toff_{VGS}$ increases, the degradation of the dynamic Rdson slightly increases too, expecially for higher drain-source voltages.

Figure 6.39 shows the influence of the stress time t_{off} on the degradation of the dynamic Rdson for the sample D. As we saw in fig 6.16, the sample D shows a very low and constant level of degradation of the dynamic Rdson, while the drain-source voltage is increasing. As we can see in fig 6.39, while the stress time $toff_{VGS}$ increases, the level of Rdson degradation does not change. This graph confirms the fatc that, already at $VDS = 50V$ all the traps of the device are filled, as we already said at page **??**.

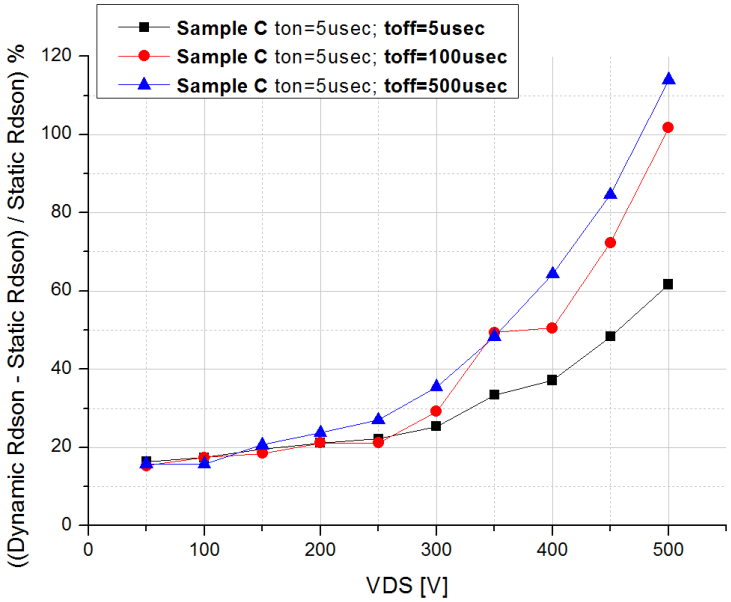

Figure 6.38: Sample C : Influence of the Stress Time t_{off} on the Degradation of the Dynamic Rdson.

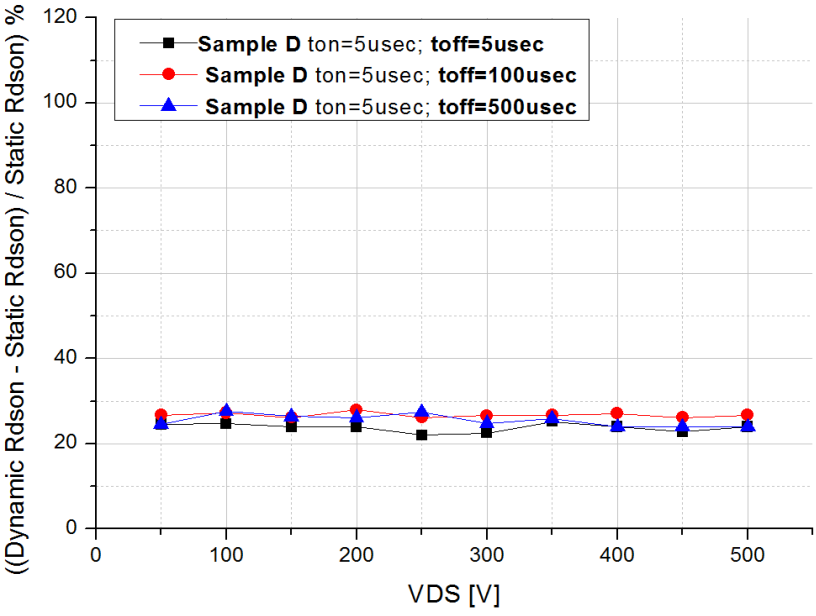

Figure 6.39: Sample D : Influence of the Stress Time t_{off} on the Degradation of the Dynamic Rdson.

Figure 6.40 shows the influence of the stress time t_{off} on the degradation of the dynamic Rdson for the samples E_Source Down and E_Drain Down. As we saw in fig 6.31, the Rdson degradation for the sample E_Drain Down is well visible, while E_Source Down shows no dynamic Rdson degradation. As we can see in fig 6.39, while the stress time $toff_{VGS}$ increases, the dynamic Rdson degradation increases for the sample E_Drain Down, whereas E_Source Down shows no change with the increase of the stress time $toff_{VGS}$.

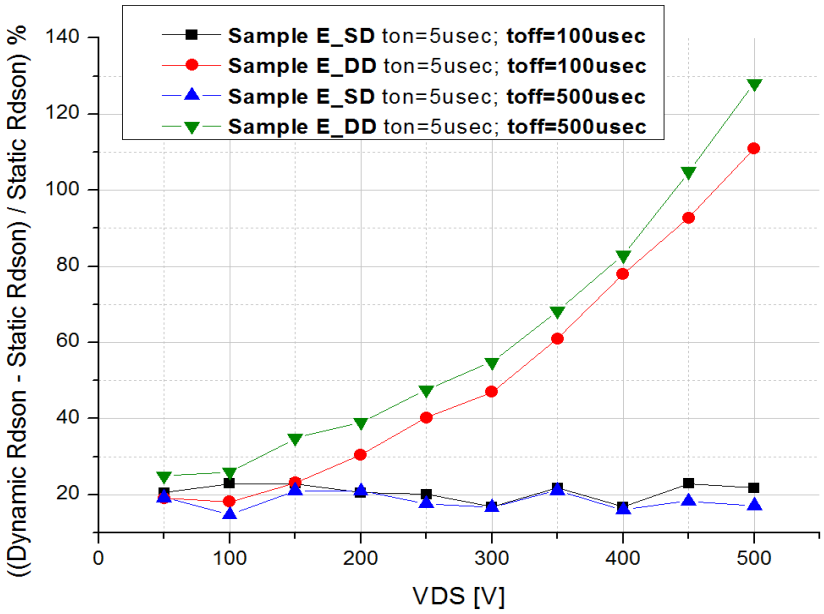

Figure 6.40: Sample E_Source Down, E_Drain Down : Influence of the Stress Time t_{off} on the Degradation of the Dynamic Rdson.

Until now we have seen the influence of the stress time t_{off} on the degradation of the Dynamic Rdson only for $toff_{VGS} = 5usec$, $toff_{VGS} = 100usec$ and $toff_{VGS} = 500usec$. Now we want to see what happens if the device is stressed for a much longer time. The graph in fig 6.41 shows the rate between dynamic and static Rdson in function of the stress time $toff_{VGS}$, for values of $toff_{VGS}$ that go up to $toff_{VGS} = 10sec$. In fig 6.41 the samples D and E_Source Down have been compared; the measured devices show the same trend: the dynamic Rdson degradation increases in the ranges $toff_{VGS} = 100us - 1ms$ and $toff_{VGS} = 100ms - 10s$, whereas Rdson looks constant

for stress time belonging to the middle range: between $toff_{VGS} = 1ms$ and $toff_{VGS} = 100ms$. By considering these datas, we can guess that the charges in the channel are sensitive to relatively short or very long stress time, while a change of the stress time inside the middle range ($toff_{VGS} = 1ms - 100ms$) has no importan teffect on the degradation of the dynamic Rdson.

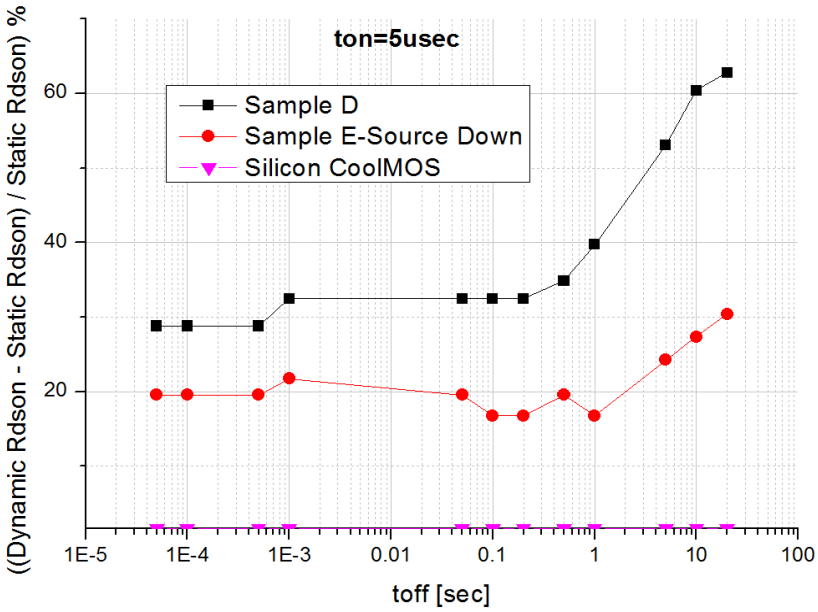

Figure 6.41: Influence of the Stress Time t_{off} on the Degradation of the Dynamic Rdson : Comparison between the Silicon CoolMOS and the samples D and E_Source Down.

The graph in fig 6.42 shows the dynamic Rdson of the sample E_Source Down evaluated at $VDS = 500V$, $toff_{VGS} = 10s$ and expressed versus the time. The percentage increase of the dynamic Rdson, comparing with the static value, is given by the following equation:

$$\frac{DynamicRdson - StaticRdson}{StaticRdson}\% = \frac{101.8m\Omega - 80.5m\Omega}{80.5m\Omega}\% = \approx 27\% \tag{6.13}$$

Where the static Rdson is evaluated throw the Static Tester M3020, shown in fig 4.9.

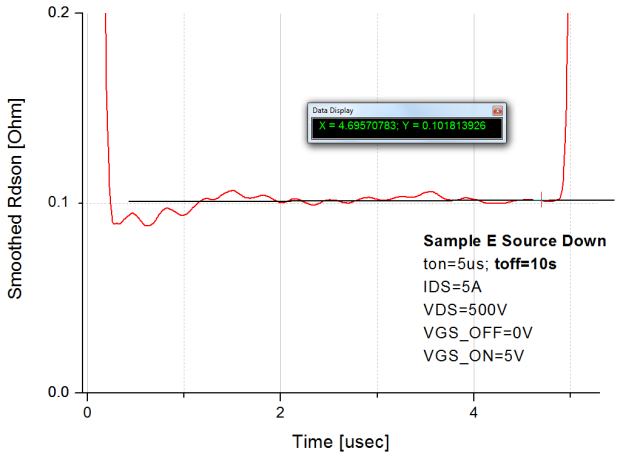

Figure 6.42: Sample E_Source Down : The Dynamic Rdson, evaluated with the GaN DReaM Setup with $ton = 5us$ and $toff = 10s$, is smoothed and expressed versus the time at VDS=500V.

6.1.4 Recovery of the Dynamic Rdson with the On-Time t_{on}

In this section we will see some examples of recovery of the dynamic Rdson with the on-time t_{on}. Referring to GaN-based HEMTs, during the on-time t_{on} the charges, trapped inside the traps of the device during the stress time t_{off}, can be detrapped and come back to the channel; so that the drain-source current recoveries and the dynamic Rdson tends to come back to the static value. We evaluated the Dynamic Rdson of some devices for values of the on-time that go up to $t_{on} = 1ms$. First of all we tested this type of measurement with the Silicon CoolMOS, already seen in sec 6.1.1, in order to have a reference for the next measurements. The graphs in fig 6.43 show the percentage increase of the dynamic Rdson of the Silicon CoolMOS, comparing with the static one. As you can see in fig 6.43, the dynamic Rdson shows an initial increment in the range $t_{on} = 5us - 50usec$, before starting to decrease and almost reaching a constant value. The trend of the graph in fig 6.43 can be directly related to the shape of the drain-source voltage measured with the clamping circuit and shown in fig 6.44. The trend of the clamped drain-source voltage shown in fig 6.44 is not logically explicable. We consider this trend to be wrong and we think it to be caused by a systematic error (in the range of 20%) set inside our setup, probably related to parasitic components. The graphs in fig 6.44 show the waveforms read from the oscilloscope at $t_{on} = 1ms$. The measurements of recovery have been done with the old setup (pag 59). In section 5.1 we talked about the limitations of the old setup; one of the most important limitations is connected with the size of the capacitors bank in parallel with the main power supply (eq 5.13). In the recovery measurement we overcome the limitation given by eq 5.13, by accepting the drain-source current to be not exactly constant during the time t_{on}: it passes from 4.78A at the beginning of the gate pulse, to 4.5A at $t_{on} = 1ms$ (graph on the right side in fig 6.44). In the graph on the right side in fig 6.44 you can see the drain-source current signal, that is not constant during the on-time t_{on}, because, due to the small size of the capacitors bank ($C_{bank} = 64\mu F$), the voltage drop across the capacitors cannot be constant for so long time: as

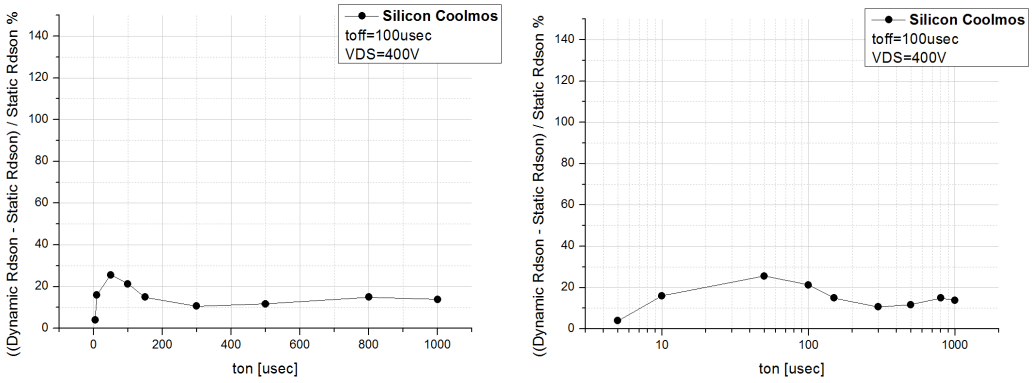

Figure 6.43: Silicon CoolMOS; Recovery of the Dynamic Rdson with the on-time t_{on} ; the horizontal axis is expressed in linear scale (on the left) and in logarithmic scale (on the right).

you can notice, infact, the drain-source voltage, set at $VDS = 400V$ throw the main power supply, reaches only approximately $VDS = 385V$ at the end of the on-time of the DUT.

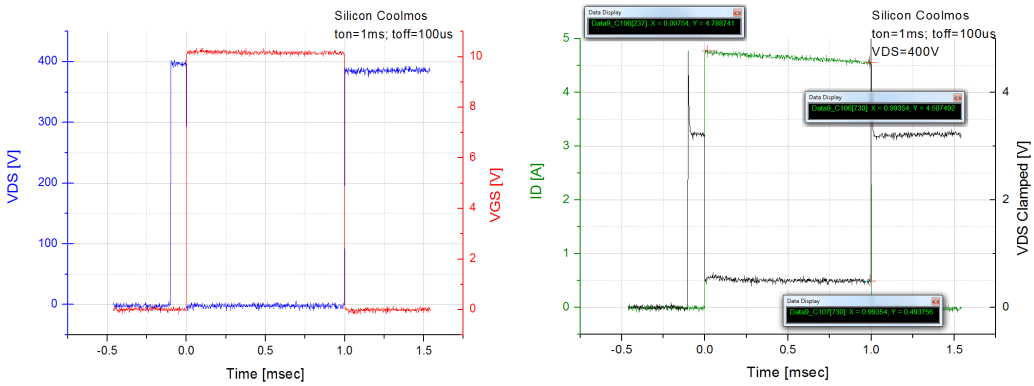

Figure 6.44: Silicon CoolMOS, Recovery of the Dynamic Rdson with the on-time t_{on} : VGS and VDS (on the left); IDS and VDS Clamped (on the right).

When we look at the signal on the oscilloscope, we have always to wander if what we see is real. Sometimes the signal can be unreal due to uncalibrated probes or simply due to probes factors that must be taken into account. As for the current probe, it is important to consider the *droop rate*. Every current

probe is defined by a certain droop rate: the droop rate is the downward slope of the top of the output voltage pulse resulting from a flattop current input pulse [16]. Because the current monitor cannot pass DC, whenever the output voltage is non-zero and the current is constant, as during the flat top of the pulse, the voltage decays toward zero exponentially [16]. This is illustrated in the upper trace in fig 6.45. The lower trace represents the applied current pulse. For our measurements we used a current probe with droop rate=$0.9\%/ms$. Let us consider the following conditions:

- $IDS = 5A$
- $t_{on} = 1ms$
- $drooprate = 0.9\%/ms$

On the oscilloscope, after $t_{on} = 1ms$, we will measure: $IDS = 5A - 0.9\% * 5A = 5A - 45mA = 4.955A$. We have verified that after $1ms$ and with $IDS = 5A$ the droop rate is negligible for our measurement, so that the waveforms shown in fig 6.44 and the results shown in fig 6.43 can be considered real. The trend of the graph in fig 6.43 can be directly related to the shape of the drain-source voltage measured with the clamping circuit and shown in fig 6.44. The trend of the clamped drain-source voltage shown in fig 6.44 is not logically explicable. We consider this trend to be wrong and we think it to be caused by a systematic error set inside our setup, probably related to parasitic components. The graphs in fig 6.46 show the comparison between the percentage decrease of the dynamic Rdson of the Silicon CoolMOS, the sample D and the sample E_Source Down, comparing with the static Rdson value. These devices have been already measured (fig 6.16, 6.31), therefore we know that they show low and constant value of dynamic Rdson degradation. As you can see in fig 6.46, the dynamic Rdson of the different devices has the same trend: it shows an initial increment in the range $t_{on} = 5us - 50usec$, before starting to decrease and reaching almost a constant value. The graphs in fig 6.47 show the percentage increase of the dynamic Rdson of the sample E_Drain Down, comparing with the static one, for $t_{on} = 1ms$ and $t_{off} = 100us$. This sample has been already measured (fig

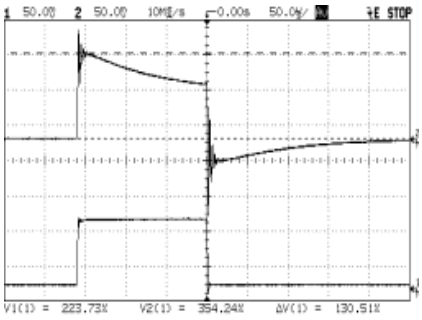

Figure 6.45: Droop Rate on the waveforom seen on the oscilloscope screen(on the top); Real applied current pulse (on the bottom) [16].

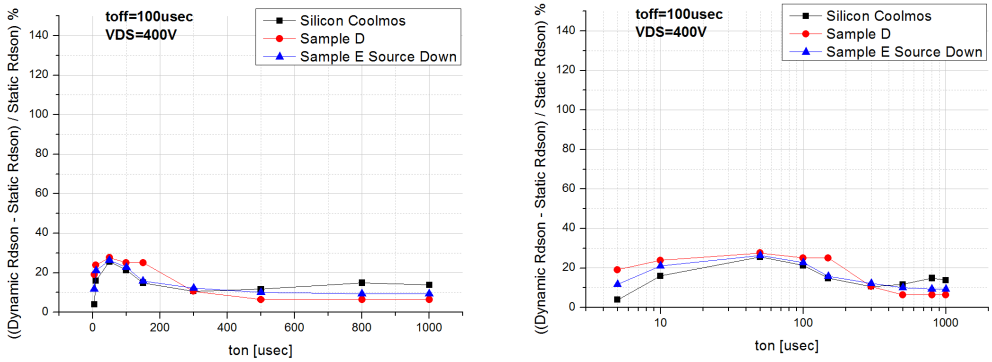

Figure 6.46: Sample E_Source Down, Recovery of the Dynamic Rdson with the on-time t_{on} ; the horizontal axis is expressed in linear scale (on the left) and in logarithmic scale (on the right).

6.31), therefore we know that it shows dynamic Rdson degradation. Fig 6.48

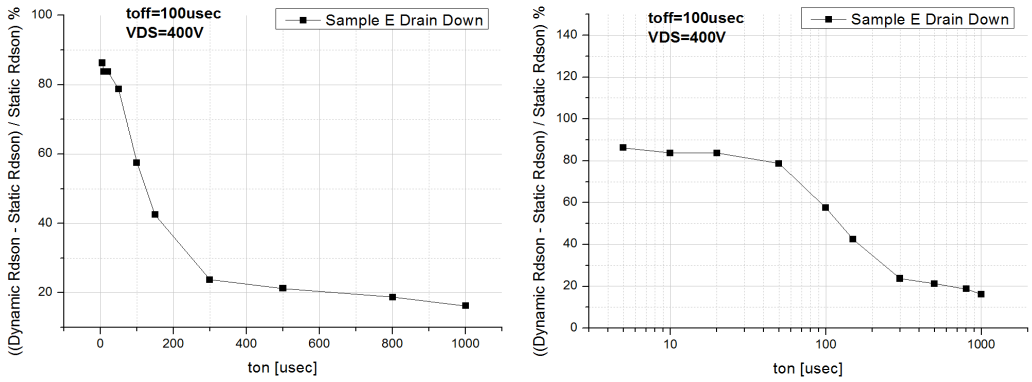

Figure 6.47: Sample E_Drain Down, Recovery of the Dynamic Rdson with the on-time t_{on} ; the horizontal axis is expressed in linear scale (on the left) and in logarithmic scale (on the right).

shows the waveforms referred to the sample E_Drain Down and read from the oscilloscope at VDS=400V. As you can see in fig 6.47, the dynamic Rdson

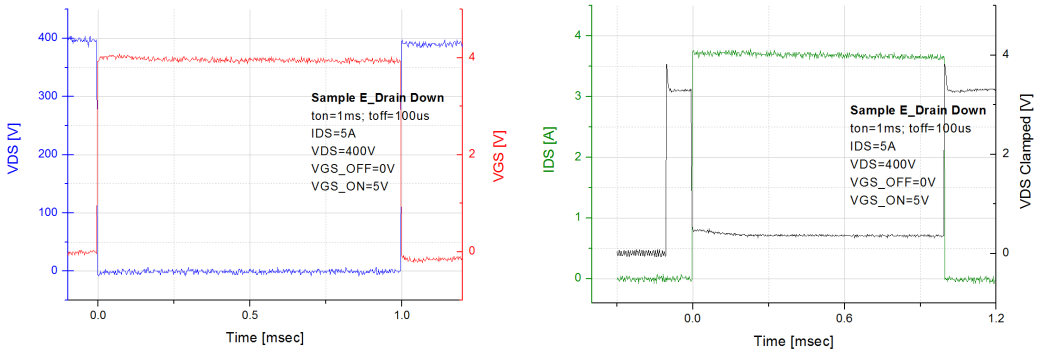

Figure 6.48: Sample E_Drain Down, Recovery of the Dynamic Rdson with the On-Time t_{on} : VGS and VDS (on the left) and IDS and VDS Clamped (on the right) registered from the oscilloscope at VDS=400V.

recovery of the sample E_Drain Down is well visible. In this case we do not see the trend seen in fig 6.46 anymore. We can say that, due to the setup we are using, we are able to evaluate the dynamic Rdson recovery when it

is remarkable, while, when it is very small, the systematical error set in our setup do not give us the possibility to correctly evaluate that. This hypothesis is confirmed by the graphs in fig 6.49; we evaluate the recovery of the dynamic Rdson for the sample C at VDS=525V for values of the on-time t_{on} that go up to $t_{on} = 150us$. The dynamic Rdson recovery is remarkable, so that the systematical error made by our setup is not visible. In fig 6.50 are

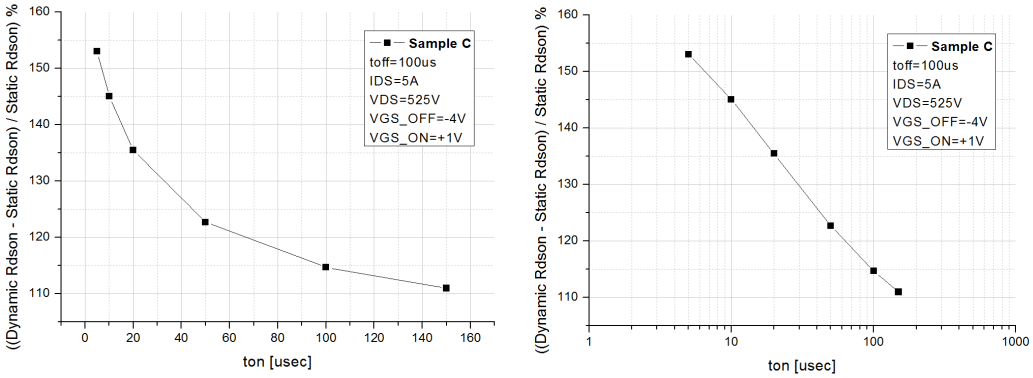

Figure 6.49: Sample C : Recovery of the Dynamic Rdson with the on-time t_{on} ; VGS and VDS (on the left) and IDS and VDS Clamped (on the right) registered from the oscilloscope at VDS=525V.

shown the waveforms read from the oscilloscope at VDS=525V. The recovery of the clamped VDS is well visible. Referring to the graph in fig 6.49, at VDS=525 the percentage increase of the dynamic Rdson comparing with the static value is given by the following equation:

$$\frac{DynamicRdson - StaticRdson}{StaticRdson}\% = \frac{396m\Omega - 187.7m\Omega}{187.7m\Omega}\% = \approx 113\% \tag{6.14}$$

The graph in fig 6.51 shows the comparison between the level of Rdson collpase of all the samples seen until now.

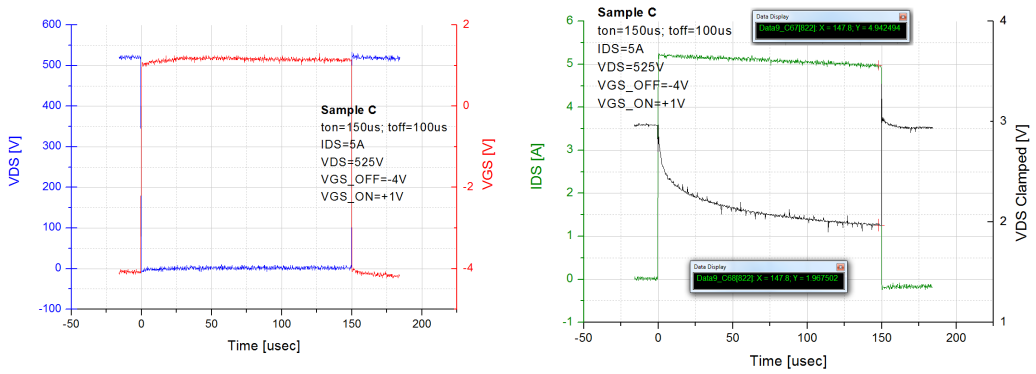

Figure 6.50: Sample C, Recovery of the Dynamic Rdson with the On-Time t_{on} : VGS and VDS (on the left) and IDS and VDS Clamped (on the right) registered from the oscilloscope at VDS=525V.

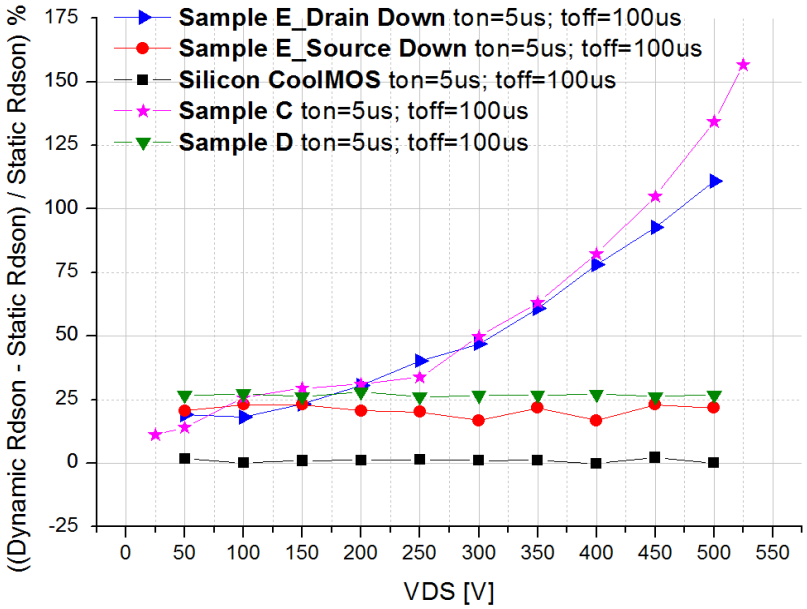

Figure 6.51: Comparison between the level of Rdson collpase of all the samples seen until now.

6.2 Measurements on Wafer level

6.2.1 Influence of the Temperature on the Degradation of the Dynamic Rdson

This section includes the measurements on GaN-based HEMTs on wafer level, in order to understand the influence of the temperature on the degradation of the dynamic Rdson. We take advantage of the WaferTherm (fig 6.52), instrument used to warm up or cool down the chuck inside the probe station. First of all we want to test the measurement on the silicon coolMOS. Power-

Figure 6.52: Wafertherm, used to warm up or cool down the chuck inside the probe station. It is able to warm the wafer up to 140.

MOS transistors all exhibit an increase in Rdson with temperature. Usually this is given in the form of a curve of Rdson vs temperature on the datasheet. In fig 6.53 you can see how the output characteristic of the Silicon CoolMOS changes with temperature. As you can see in the graph on the left side in fig 6.54, the Rdson of the silicon device increases with temperature. The graph on the right side in fig 6.54 shows the percentage increase of the dynamic Rdson, comparing with the static one: the static Rdson of the silicon device increases with temperature, but the dynamic Rdson always conincides with the static one (pag 101). In the following we will see the influence of the temperature on the degradation of the Rdson for some GaN-based HEMTs. The graph in fig 6.55 shows the percentage increase of the dynamic Rdson,

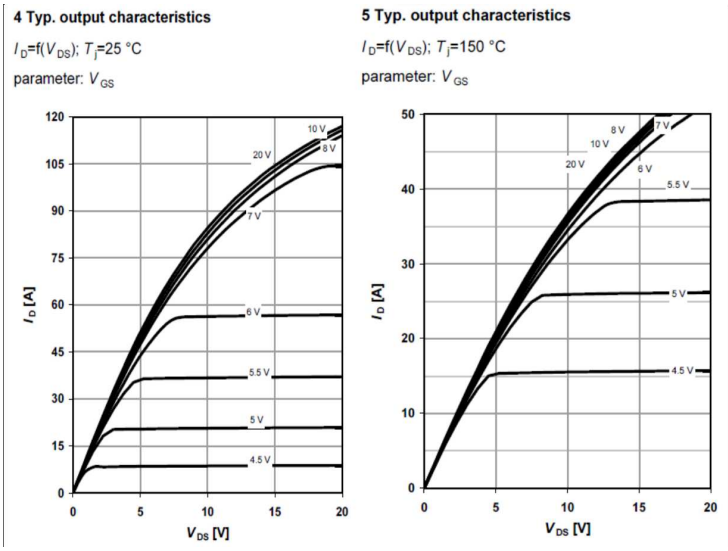

Figure 6.53: Silicon CoolMOS : Influence of the temperature on the Rdson.

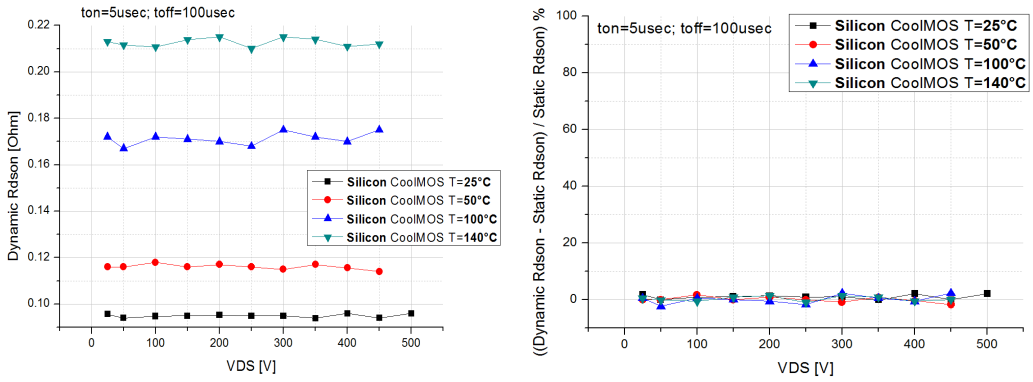

Figure 6.54: Silicon CoolMOS, Influence of the Temperature on the Degradation of the Dynamic Rdson : dynamic Rdson at different temperatures (on the left), percentage increase of the dynamic Rdson comparing with the static one at different temperatures (on the right).

comparing with the static one, for the sample F at different temperatures. As you can see in fig 6.55, even if the static Rdson increments with temperature, as it happens in Silicon devices, the rate between dynamic and static Rdson decreases with temperature; infact, referring to GaN-based HEMTs, drain current and drain current collapse reduce with an increase in temperature, which results from the reduction of the electron mobility (or saturation velocity) and the contemporaneous thermal activation of the trapped electrons [12]. As the temperature increases from room temperature (RT) to 200C, the

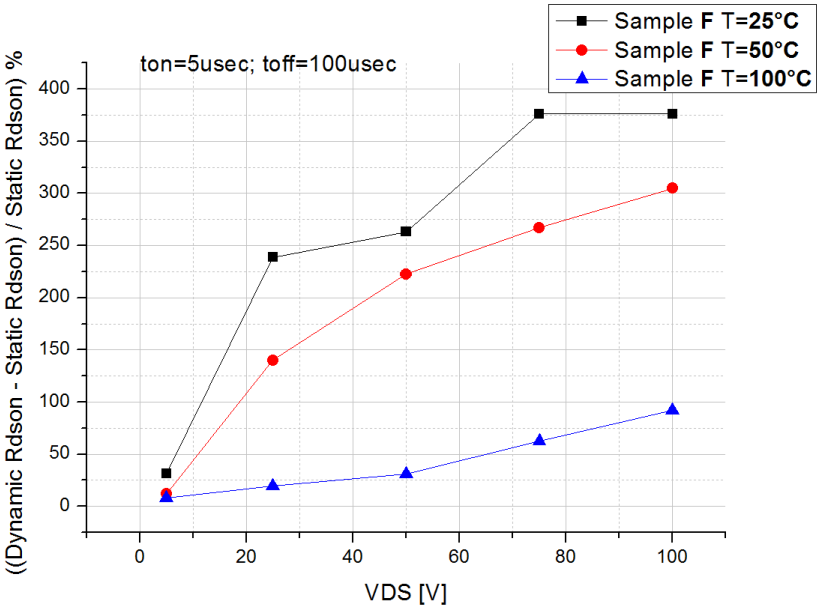

Figure 6.55: Sample F, Influence of the Temperature on the Degradation of the Dynamic Rdson : percentage increase of the dynamic Rdson, comparing with the static one, at different temperatures.

saturation drain current I_{Dsat} decreases [12], as you can see in fig 6.56. The traps in the barrier layer become active as the temperature increases, which is conducive to the electron tunneling between the gate and the channel [12]. The enhancement of the tunneling results in the weakening of the current collapse effects, as the electrons trapped by the barrier traps can escape more easily at the higher temperature [12]. The uniform increase in the thermally activated electron current with the increase of temperature is indicative of a

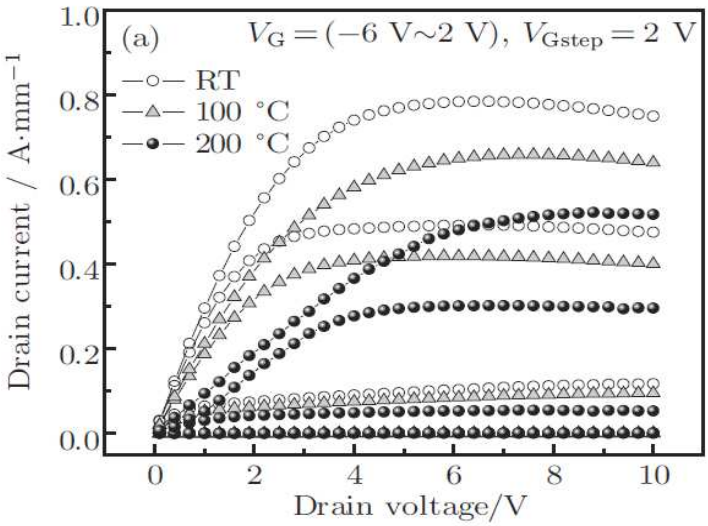

Figure 6.56: Typical Output Characteristics of a GaN-based HEMT device at RT, 100C and 200C [12].

continuous distribution of traps energy levels [12] rather than a single trap with a well defined level, as previous reports [20], [26], [17]. As shown in fig 6.57, the current collapse is thus weakened at higher temperature, for which there are two reasons:

1. The activity of the traps in the AlGaN barrier is increased

2. The electrons obtain higher energy, as the temperature rises.

Both reasons make it easier for electrons to escape from traps into the barrier layer. Thus, the depletion effect of the trapped electrons in the channel is suppressed, eventually leading to the weakening of the current collapse [12]. The study on the conductance frequency and the gate lag characteristics, made in [20], reveals that no new trap is generated in the AlGaN/GaN HEMT, while the activity of the original trap in the AlGaN barrier is enhanced as the temperature increases, which contributes to the electron escaping from the traps in the barrier layer, thus suppresses the depletion effect of the trapped electrons in the channel and eventually leads to the weakening of the current collapse. The graph on the left side in fig 6.58 shows the influence of

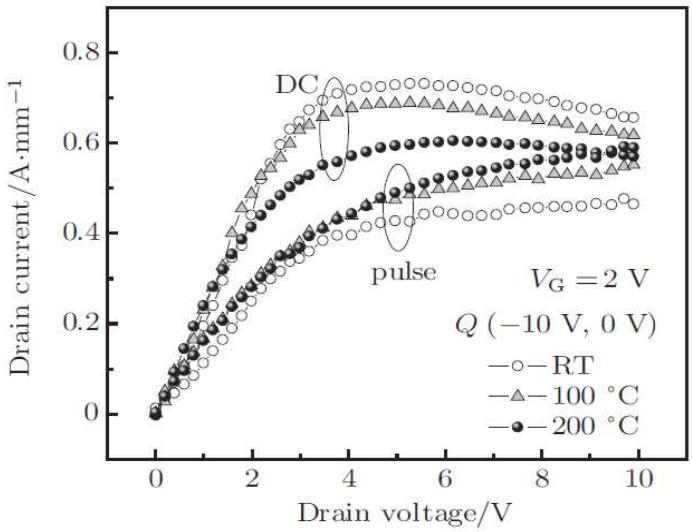

Figure 6.57: Drain-Source Current of AlGaN/GaN HEMTs versus drain-source voltage at RT, 100C and 200C [12].

the temperature on the degradation of the dynamic Rdson for the sample A. The dynamic Rdson is represented at different temperatures versus the drain-source voltage. The value of Rdson increases with temperature, which results from the reduction of the electron mobility (or saturation velocity), but the rate between dynamic and static Rdson is almost constant for different temperatures; this can be related to the fact that this device shows low and constant value of degradation of the dynamic Rdson with the drain-source voltage.

Let us give a look to the graph on the right side in fig 6.58: here the dynamic Rdson at different temperatures is expressed versus the drain-source voltage. As you can see, in this case we register a phenomenon that is the opposite of the one shown in the sample A (graph on the left side in fig 6.58: the Rdson-collapse is increasing with the temperature. This phenomenon is not logically explicable; we can guess that at high temperatures the detrapping phenomenon can be promoted too, so that, even if the detrapping phenomenon is faster, due to the fact that more charge has been trapped during the stress time t_{off}, the Rdson-collapse increases. The double pulse

setup would be necessary in order to better understand this phenomenon. The graphs in fig 6.59 and 6.60 show the overlap of the waveforms of VDS

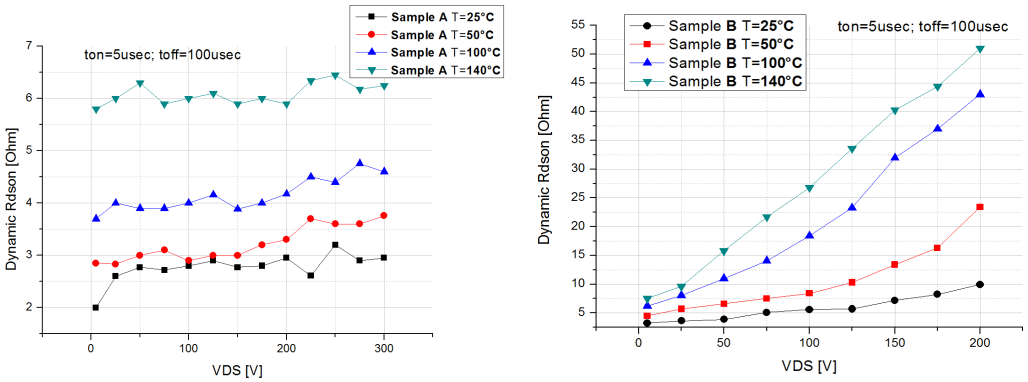

Figure 6.58: Influence of the Temperature on the Degradation of the Dynamic Rdson : Sample A (on the left), sample B (on the right).

Clamped and IDS of the samples A and B, read from the oscilloscope for different value of VDS_{off} at $T = 25C$(on the left) and at $T = 140C$ (on the right). As you can see, IDS is keeped constant in both the cases, while VDS Clamped shows a remarkable increase with VDS_{off} only at $T = 140C$. These graphs confirm the phenomenon shown in the graph on the right side in fig 6.58. The high drain-source current peak, shown at the switching-on of the device (fig 6.60), is increasing with the applied drain-source voltage. We guess that to be connected with the discharge of a high drain-source capacitance. Many other measurements have been done on wafer level, but we decided not to insert all them, due to reasons connected with the lenghth of the thesis.

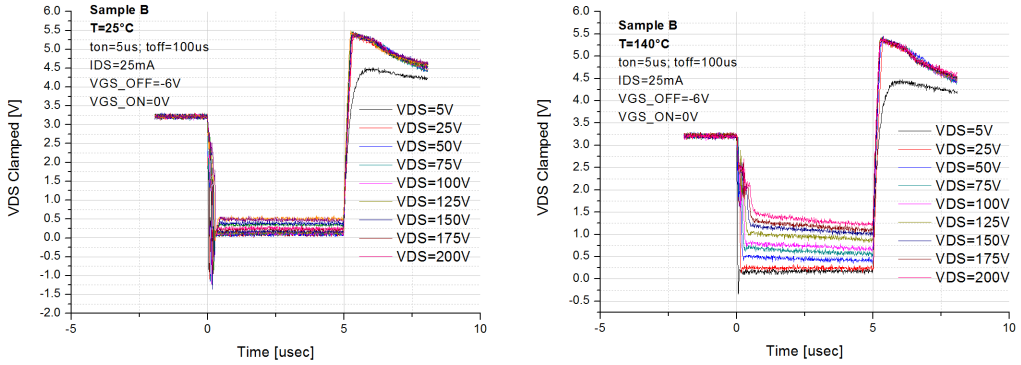

Figure 6.59: Sample A, sample B; Influence of the Temperature on the Degradation of the Dynamic Rdson : Overlap of the waveforms of VDS Clamped read from the oscilloscope at different value of VDS_{off} at $T = 25C$(on the left) adn at $T = 140C$ (on the right).

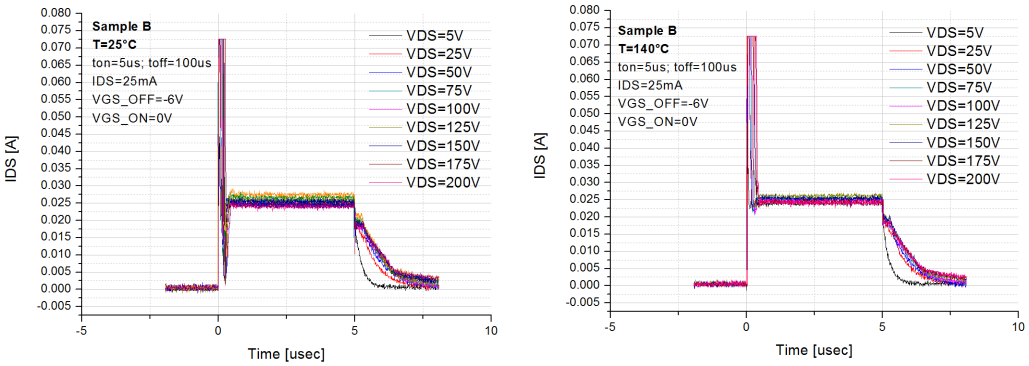

Figure 6.60: Sample A, sample B; Influence of the Temperature on the Degradation of the Dynamic Rdson : Overlap of the waveforms of IDS read from the oscilloscope at different value of VDS_{off} at $T = 25C$(on the left) adn at $T = 140C$ (on the right).

Conclusions

As already mentioned, the increasing demand for high performance devices, in particular in terms of power at high frequencies, has moved the research towards new materials with better properties than the ones of the materials used until now. The semiconductors which have been used in electronics until now are Silicon (Si), Gallium Arsenide (GaAs) and all related III-V materials. The energy bandgap of these semiconductors are 1.12 eV for Si and 1.43 eV for GaAs, which are mid-range values. Unfortunately those mid-range bandgap based electronic devices cannot be used for a wide range of application due to the limit imposed by the size of the bandgap. A solution to these kinds of problems has come from GaN and III-nitrides. The bandgap of III-nitrides are large and direct. Wide-band-gap semiconductors are expected to be used as materials for new switching devices with low losses and high switching speed, comparing with Silicon. The main non-ideality of interest in GaN HEMTs has been variously referred to as current collapse. This is the most important problem that impacts GaN FET technology for high power applications. Current collapse is essentially the observation that the measured output power of the device at the frequencies of interest, such as 4-18 GHz, is considerably smaller than that expected. Current collapse is caused by the presence of deep levels or traps located in the device structure [28]. The term gate lag is used to describe the slow transient response of the drain current when the gate voltage is pulsed [Veturi 2000]. We refer to as lag if, when the gate is pulsed ON, the drain current is larger than its steady state and the drain current slowly reaches its steady state value. This phenomenon is attributed to both surface state as well as substrate deep trap effects. Various research groups have confirmed that drain current

reduction during large signal operation at microwave frequencies is mainly caused by electrons trapping phenomena at the unpassivated barrier surface. the gate lag phenomen can also be defined as an increase in the dynamic Rdson value (measured under pulsed conditions), comparing to the static Rdson value (measured in steady state). In this work we evaluated the dynamic Rdson thanks to the new GaN DReaM Setup (sec 5.2, where many issues concerning automation and safety issues have been inserted, comparing with the previous setup (sec 5.1). We measured the dynamic Rdson of normally-on and normally-off GaN-based HEMTs, then we compared that with the static Rdson, in order to evaluate the Rdson collapse (chap. 6). We evaluated the Rdson degradation under different conditions, in order to understand the influence of different parameters, such as the on and off-time t_{on} and t_{off} and the temperature. We stepped into devices with almost null, well visible and eventually huge Rdson collapse and we tried to understand the reasons behind each kind of behaviour. By considering the behaviour of the devices seen in this chapter, we can say that still a lot of work has to be done in matter of Rdson collapse, in order to have the opportunity to fully take advantage of GaN‘s potential. Some devices, anyway, must be highlighted for their good response in terms of Rdson collapse (sample D in fig 6.16 and sample E_Source Down in fig 6.31).

Talking about projects for the future, in the next months we are going to build the GaN DReaM Setup also on package level. Moreover, regarding the setup on wafer level, we are going to use new needles, in order to have the possibility to go up to $IDS = 10A$. Giving a look to the future, we can expect to find ourselves working with always better devices, having a better behaviour also in terms of Rdson collapse. For this reason it will be important for our GaN DReaM Setup to increase its accuracy. We can do that by optimizing some features. It is not possible, anyway, to completely remove the influence of the parasitic elements that introduce an error; every element of the set-up (the connections, the instruments, etc..) brings an error. We can only try to minimize the error, in order to make it as closed as possible to zero. Nothing is perfect [Harald Thurner].

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