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Tesi di Laurea

Characterization of the mechanisms of charge Trapping in GaN Vertical devices.

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Abstract

Ad oggi, il bisogno di raggiungere elevati livelli di potenza per dispositivi come veicoli elettrici , inverter per impianti fotovoltaici e motori industriali ha spinto verso un rinnovamento dei sistemi di conversione di potenza che sta avvenendo grazie all'uso di semiconduttori ad elevato energy-gap (E_{GAP}). In particolare il Nitruro di Gallio (GaN) possiede caratteristiche eccellenti per l'elettronica di potenza: ha una elevata tensione di breakdown un' elevata mobilità elettronica e velocità di saturazione degli elettroni, inoltre, raggiunge elevate temperature prima di degradarsi.
HEMTs in GaN sono già disponibili sul mercato per applicazioni che operano fino a 650V. Sono dispositivi laterali basati su un'eterostruttura AlGaN/GaN e la formazione di un canale conduttivo bidimensionale sull'interfaccia AlGaN/GaN.
In questa tesi sarà esaminata una nuova tipologia di dispositivi in GaN: i transistor verticali. Questo dispositivi sono promettenti per la futura elettronica di potenza: è infatti possibile aumentare la tensione di breakdown aumentando la distanza tra Gate e Drain senza aumentare l'area del dispositivo. Hanno una resistenza di canale (R_{ON}) inferiore rispetto ai dispositivi laterali e inoltre la corrente scorre in direzione verticale, eliminando il trapping superficiale.
In particolare in questa tesi sono stati esaminati i Fin FET Transistors. In questi transistor non è presente l'eterostruttura AlGaN/GaN, la corrente scorre lungo un canale nanometrico verticale di GaN (Fin) che presenta una struttura MOS ai suoi lati.

Il lavoro di tesi si è sviluppato in due fasi: nella prima sono state svolte diverse misure mettendo in relazione la variazione dei parametri fondamentali del transistor (V_{th} ,R_{ON}) con la larghezza del canale e la variazione di parametri esterni come temperatura ed esposizione a luce UV. Nella seconda sono state svolte delle simulazioni per testare in maniera approfondita i risultati delle misure e dare una spiegazione dei fenomeni di trapping per i diversi potenziali di gate applicati.

Nel primo capitolo della tesi sono state descritte le caratteristiche del Nitruro di Gallio (Polarizzazione Spontanea e Piezoelettrica) e le motivazioni per le quali è un eccellente semiconduttore per la costruzione di dispositivi per elettronica di potenze.
Nel secondo capitolo sono stati introdotti i dispositivi laterali in GaN, il loro funzionamento e i loro limiti come dispositivi per la potenza elevata.
Nel terzo capitolo vengono descritte alcune tipologie di transistor verticali.
Nel quarto capitolo vengono analizzati i Fin FET Transistors presenti in letteratura. Sono state effettuate misure in DC anche a temperature crescenti su

dispositivi con larghezze di canale diverse. Il risultato di queste misure è una V_{th} più elevata per il dispositivo a larghezza di canale inferiore (70nm) rispetto ai dispositivi a larghezza di canale più elevata. L'effetto della temperatura (aumento della R_{ON} e della V_{th}) è lo stesso per tutti i dispositivi indipendentemente dalla larghezza di canale.
Nel quinto capitolo viene studiato l'intrappolamento nell'ossido imponendo al Gate un potenziale di bias positivo crescente $V_{GS,Q}$. Il risultato di queste misure è uno shift negativo della V_{th} per bassi valori di $V_{GS,Q}$ (1,2V) e uno shift positivo per $V_{GS,Q}$ più elevati (3,4,5V).
Nel sesto capitolo si sono studiati gli stessi fenomeni applicando un potenziale di bias positivo al Gate ($V_{GS,BIAS}$) per tempi crescenti e si è inoltre studiato il *recovery* (ritorno della tensione di soglia al valore iniziale). Anche in questo caso si è visto uno shift negativo della V_{th} per bassi valori di $V_{GS,BIAS}$ e uno shift positivo per $V_{GS,BIAS}$ più elevati. Il *recovery* del dispositivo è immediato e completo per bassi valori di $V_{GS,BIAS}$, non avviene invece per i valori di $V_{GS,BIAS}$ più elevati. Le stesse misure sono state effettuate a temperature crescenti ed esponendo il dispositivo a luce UV.
Nel settimo capitolo viene utilizzato un simulatore di dispositivi elettronici per simulare il comportamento dei dispositivi durante le misure e cercare un modello fisico che lo descriva.
In conclusione, con questo lavoro di tesi, si è fatta un' analisi completa dei meccanismi di intrappolamento quando una nuova tipologia di transistor verticale (GaN Fin FET) è sottoposta ad una tensione positiva al Gate, dimostrando con misure elettriche e simulazioni i fenomeni fisici responsabili del comportamento del transistor.

Introduction

Nowadays high power levels required for applications such as electric vehicles, photovoltaic inverters and industrial motors has brought to the renovation of power conversion systems by using wide bandgap semiconductors. Gallium Nitride (GaN) is a promising semiconductor for high power switching applications due to its high critical electric field, high carrier mobility and high maximum temperature reached before degrading. Lateral GaN Transistors are already available on the market for applications in 650V operating range and are based on a GaN/AlGaN heterostructure.
My master thesis will deal with a new type of GaN devices: the Vertical Transistors. These devices constitute an improvement in comparison to lateral devices in fact current flows vertically and breakdown voltage can be increased increasing the distance between gate and drain without increasing the size of the device. They have lower channel resistance and unlike lateral devices, they are not affected by surface trapping.
In particular in my thesis, Vertical Fin FET Transistors will be analyzed. This kind of transistors are not based on the GaN/AlGaN heterostructure but on a fin-architecture, where current flows through nanometer-sized channel having a MOS stack on the sides.

In the first part of my thesis different measurements have been made to see the variation of the parameters of transistors varying the dimension of the fin of the devices and external parameters (temperature and UV light). The results of the measurements are an higher threshold voltage (V_{th}) for the device with lower GaN channel width (70nm) and a negative shift of V_{th} for low positive bias potentials applied to gate and a positive shift of V_{th} for higher positive bias potentials applied to gate.

In the second part simulations through a microelectronics simulator have been performed in order to further analyze the results and give an extensive explanation of the charge trapping behaviour in different bias conditions.

In chapter 1 properties of GaN are described and chapter 2 deals with Lateral Transistors which are the state of art of power electronics.
In the third chapter vertical transistors are introduced and different topologies are described.
In chapter 4 Fin FET transistors are described and analyzed through Direct Current measurements.
In chapter 5 measurements applying a positive bias gate potential have been performed in order to study trapping mechanisms and hypotheses of devices

behaviour are made.
In chapter 6 the same trapping mechanisms are analyzed varying the periods of time in which positive bias gate potentials are applied, varying the temperature and exposing the device to UV-light.
In chapter 7 the results of the simulations of the behaviour of the device during the experimental tests are reported. The physical mechanism responsible of the behaviour is analyzed.

1. Gallium Nitride

Wide bandgap semiconductors show superior properties useful for new power electronics devices. Devices based on these semiconductors are enabled to work at higher voltages and temperatures than those on Silicon.
One of the most promising wide bandgap semiconductor is Gallium Nitride.

1.1 GaN and III-N materials crystal structure

Gallium Nitride is a binary semiconductor composed by a V (N) element and a III (Ga) element.
Every atom of Ga binds with four surrounding atoms of N forming a tetrahedral structure. The bond angles Θ are of 109.5 degrees.
III-N materials such as GaN AlN and InN can have two possible structures, zincblende and wurtzite.
But the most commonly GaN structure used in electronic devices is the hexagonal crystal structure called wurtzite fig. (1).
In wurtzite crystal the perpendicular axis to the hexagonal face is called c-axis, oriented in the direction [0001] The three parameters defining the wurtzite lattice are the edge length of the basal hexagon a_0, the height of the hexagonal lattice cell c_0, and the cation-anion bond length ratio u_0 along the [0001] direction, in units of c_0 Table (1).

1.2 Spontaneous polarization

Nitrogen has an electronegativity of 3.04 and Gallium of 1.81. This high difference of electronegativity causes strong ionicity in the gallium-nitrogen covalent bond. The ionicity is a microscopic polarization which results in macroscopic polarization $\vec{P}$ if the crystal lacks of inversion symmetry as wurzite crystal along

Lattice length	AlN	GaN	InN
$a_0(\mathring{A})$	3.112	3.189	3.54
$c_0(\mathring{A})$	4.982	5.185	5.705
u_0	0.380	0.376	0.377

Table 1: Lattice constants[1]

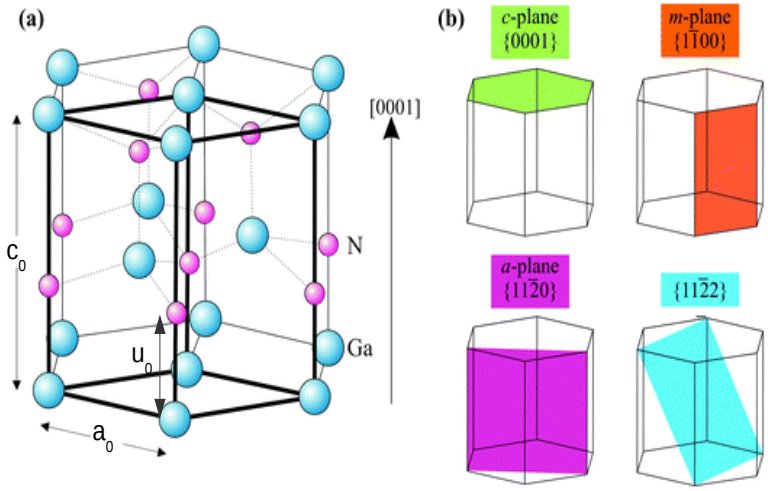


Figure 1: a)Wurtzite structure of crystal GaN b) Wurzite planes[2]

c-axis.
In the freestanding tetrahedral structure the sum of the polarization vectors of the four chemical bonds, is zero[3]:

$$\vec{P_1} + \vec{P_2} + \vec{P_3} + \vec{P_4} = 0$$

Although the polarization is zero inside the crystal, if a perpendicular cut to [0001] direction is made, the total polarization vector is not null along the c-axis. That is called *spontaneous polarization.*
Spontaneous polarization is a characteristics of all the III-N compounds and alloys such as AlGaN.
The orientation of polarization is defined assuming that the positive direction goes from the metal (Ga, Al, In) to the nearest neighbor nitrogen atom along the c axis (that is [0001] direction). In the opposite direction [000$\bar{1}$] (from nitrogen to metal) the polarization is negative fig. (2).
The sign of spontaneous polarization of III-N compounds is found to be negative.

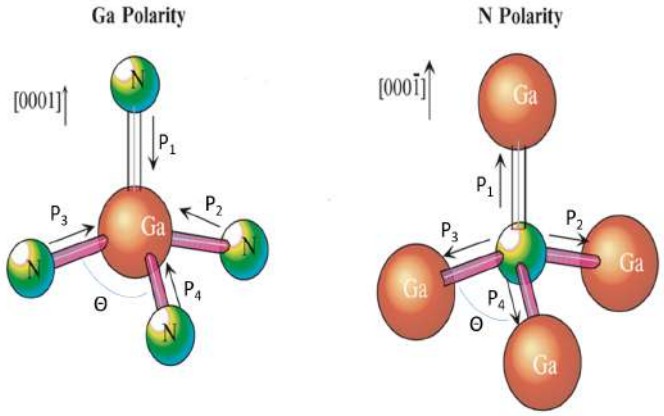


Figure 2: Tetrahedral structure of GaN[4]

The calculated spontaneous polarization for GaN is -0.029 C/m^2 [5] and it is more negative for InN, AlN, and AlGaN.

1.3 Piezoelectric polarization

If the GaN crystal is subject to strain on the c-plane, a_0 and c_0 do not assume their ideal values and the Θ angle is widened.
Also the parameter u_0 changes in fact the strain produces an internal displacement of the metal sublattice with respect to the nitrogen sublattice.
The consequence is a variation of the distribution of electronic charge that causes an internal electric field and a not null polarization vector appears. That is called *piezoelectric polarization.*

The piezoelectric polarization vector $\vec{P}_{PE}$ is related to the crystal strain through the following relation[1][4]:

$$\vec{P}_{PEi} = \sum_{jk} e_{ijk}\epsilon_{jk} \tag{1}$$

where P_{PEi} is the component of polarization vector along i-cartesian direction, ϵ_{jk} is the component of lattice strain direction and e_{ijk} is the component of the piezoelectric tensor.
In the hexagonal symmetry equation using Voigt notation (1) becomes:

$$\begin{pmatrix} P_x \\ P_y \\ P_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{xy} \\ \epsilon_{xz} \\ \epsilon_{zy} \end{pmatrix}$$

(2)

Two of the three independent components measure the piezoelectric polarization along the c axis which turns out to be:

$$P_c = e_{33}\epsilon_{zz} + e_{31}(\epsilon_{xx} + \epsilon_{yy}) \tag{3}$$

$\epsilon_{zz} = \frac{(c-c_0)}{c_0}$ is the strain along the c-axes and $\epsilon_{xx} = \epsilon_{yy} = \frac{(a-a_0)}{a_0}$ assumed to be isotropic is the in-plain strain.

There is a relationship between the strain of the two lattice constants in the hexagonal structure of GaN and it is given by the coefficients of the strain tensor. The strain tensor relates the internal stresses σ_{ij} with the deformation ϵ_{kl} :

$$\sigma_{ij} = \sum_{kl} C_{ijkl}\epsilon_{kl} \tag{4}$$

using the hexagonal symmetry and the Voigt notation tensor C_{ijkl} can be semplified in a 6×6 matrix:

$$\begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{xy} \\ \sigma_{yz} \\ \sigma_{zz} \end{pmatrix} = \begin{pmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0 \\ C_{12} & C_{22} & C_{13} & 0 & 0 & 0 \\ C_{13} & C_{13} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{33} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{66} \end{pmatrix} \begin{pmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{xy} \\ \epsilon_{xz} \\ \epsilon_{zy} \end{pmatrix} \tag{5}$$

If the strain is along c-plane then $\sigma_{zz} = \sigma_{xy} = \sigma_{yz} = \sigma_{zx} = 0$ and $\sigma_{xx} \neq 0$ and $\sigma_{yy} \neq 0$ and the strain tensor has only three non-vanishing components ϵ_{xx} ϵ_{yy} ϵ_{zz} which are related by equation:

$$\frac{(c-c_0)}{c_0} = -2\frac{C_{13}}{C_{33}}\frac{(a-a_0)}{a_0} \tag{6}$$

where C_{13} and C_{33} are elastic constant.

Using equation (6) the polarization along the c-axis can be expressed as:

$$P_c = 2\frac{a-a_0}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \tag{7}$$

As it can be seen in equation (7) P_c increases with strain.

	AlN	GaN	InN
$e_{33}(C/m^2)$	1.46	0.73	0.97
$e_{31}(C/m^2)$	-0.60	-0.49	-0.57
$e_{15}(C/m^2)$	-0.48	0.376	0.377
ϵ_{11}	9.0	9.5	
ϵ_{33}	10.7	10.4	14.6

Table 2: Strain constants and piezoelectric coefficients of III-N compounds[1]

Piezoelectric polarization is typical of III-N materials and under the same strain, it increases from GaN to InN and AlN.

Polarity and piezoelectricity are fundamental characteristics for GaN based devices.

1.4 Why Gallium Nitride for power electronics devices

Traditional power devices are made on Silicon (Si) and Germanium (Ge).
Latest electronic devices are also composed by heterostructures of GaS and AlGaS.
Nowadays new wide band-gap semiconductors are used such as Silicon Carbide (SiC) and Gallium Nitride (GaN).
Gallium Nitride has several features which makes it more useful than the other semiconductors for power electronics and high frequency applications (Table (3)[6]):

- high bandgap is empirically linked to high critical electric field and this means that GaN becomes conductive at high electric field E_c,
- high carrier mobility μ,
- high saturation velocity (maximum velocity of an electron under high electric field) v_{sat},
- high maximum temperature T_{max} before degrading

Gallium nitride finds wide application in devices which require high power and high frequency. It is therefore important to define parameters which describe the performances according to both power and frequency requirements.
In order to evaluate the features of a semiconductor used for fabrication of power devices, Johnson and Baliga derived different figures of merit[7].
Johnson Figure of Merit[8] (JFOM) accounts for the fact that there is a tradeoff between the cut-off frequency (f_T) and the breakdown voltage (BV) that the device can reach.
The BV is defined as:

$$BV = \vec{E}_c \cdot \vec{l} \tag{8}$$

where $\vec{E_c}$ is the critical field and l is the region in which the electric field acts, the cut-off frequency f_T is:

$$f_T = \frac{1}{2\pi\tau} \tag{9}$$

and τ is the time in which the carrier travels the distance l at the saturation velocity (v_{sat}) under $\vec{E_c}$:

$$\tau = \frac{v_{sat}}{2\pi l} \tag{10}$$

the product between BV and f_T is:

$$JFOM = \frac{\vec{E_c} \cdot \vec{v}_{sat}}{2\pi} \tag{11}$$

The parameter to minimize the power loss in on-state is the Baliga Figure of Merit (BFOM) and it is evaluated as:

$$BFM = \epsilon\mu E_g^3 \tag{12}$$

It derives from the fact that the on-resistance[9] is given by:

$$R_D = \frac{4V_B^2}{\mu\epsilon E_c^3} \tag{13}$$

BFOM is dominant for low-frequencies devices where the power loss is mainly in on-state. (ϵ is the dielectric constant).
The power losses in high frequencies devices must take account also of switching losses due to charging and discharging. The power loss is in this case:

$$P = I_{rms}^2 R_{ON} + C_{in} V_G^2 f \tag{14}$$

where I_{rms} is the effective current, C_{in} is the device capacitance, V_G is the gate potential and f the working frequency. The figure of merit for devices operation at high frequency is[10][11]:

$$BHFFOM = \frac{1}{(R_{ON,sp} C_{in,sp})} = f_B \tag{15}$$

$R_{ON,sp}$ and $C_{in,sp}$ are R_{ON} and C_{in} are normalized on the area of device.
BHFFOM has the dimensions of a frequency and evaluates the switching capability of the device.

As it can be seen in Table (4), GaN has the best figure of merits: the highest tradeoff between BV and f_T (JFOM), the minimum power loss in ON-state and the higher switching frequency.

	$\mu(cm^2/Vs)$	$E_g(eV)$	$T_{max}(°C)$	$v_{sat}(X10^7 cm/s)$	$E_c(MV/cm)$
Si	1500	1.1	300	1.0	0.3
GaS	8500	1.4	300	1.3	0.4
SiC	700	2.9	600	2.0	4.5
GaN	1000-2000	3.4	700	2.5	3.3

Table 3: Properties of Si, Gas, SiC, GaN

	JFM	BFOM	BHFFOM
Si	1	1	1
GaAs	11	28	16
SiC	410	290	34
GaN	790	910	100

Table 4: Figure of merit of different semiconductors normalized on Si values

2. Lateral Gallium Nitride high mobility transistors

High electron mobility transistors (HEMT) are field-effect transistors mainly used for power switching applications.
HEMTs are characterized by a junction (called *heterojunction*) between two materials with different bandgaps and lattice constants.
These devices are based on the formation of a two dimensional (2DEG) electron gas conductive channel on the surface between the two layers of the heterostructure and they exploit the high mobility and high density of electrons in the 2DEG channel.
A commonly used materials combination is GaAs with AlGaAs or AlGaAs with InGaAs.
In these devices the element with wider bandgap is kept n-doped while the element with smaller bandgap is kept undoped.
Electrons move from the element with wider bandgap to the element with lower bandgap and form the 2DEG conductive channel.

In these years the effort to implement higher power switching devices has led to the use of new semiconductors, characterized by wider bandgaps and new high electron mobility transistors have been developed.
One of the most promising wide band-gap semiconductor is Gallium Nitride (GaN).

Lateral Gallium Nitride high mobility transistors are composed by a GaN/AlGaN heterostructure.
Aluminum gallium nitride is an alloy of Aluminum nitride and gallium nitride.

The heterostructure is grown on a foreign substrate. A substrate is the mechanical support of the GaN layers but it also acts as a seed crystal necessary for the growth of bulk GaN.
The epitaxial growth of GaN can be physical if the atoms are deposited through physical methods or chemical if the growth takes place through chemical reactions.
The commonly used materials for substrates are Sapphire, Silicon Carbide and Silicon.
Sapphire (Al_2O_3) is the most commonly used substrate but the large mismatch between lattice constants of GaN and Al_2O_3 (15%) leads to high dislocation density (10^{10} cm^{-3}) in the GaN epitaxial film[12]. Silicon Carbide (SiC) have

several advantages over sapphire for GaN epitaxy, including a smaller lattice constant mismatch (3.1 %) for [0001] oriented films, and a much higher thermal conductivity $3.8\frac{W}{cmK}$ but the cost of Silicon Carbide is high. Silicon (Si) has favorable physical properties, high quality and low cost, in fact silicon wafer are available at low price and in very large size due to its mature development and the large-scale production. But the quality of GaN epitaxial layers on silicon is much poorer than that on sapphire or silicon carbide, due to large mismatch and the tendency of silicon to form an amorphous silicon nitride layer when exposed to reactive nitrogen sources.
Recently GaN devices are grown on GaN substrates. Gallium Nitride itself is the best choice as a substrate for GaN epitaxy, as it eliminates all problems associated with the use of a foreign substrate (heteroepitaxy), but the cost of GaN substrates is still quite high.

Gallium nitride is an ideal material for the fabrication of high-power microwave devices for several features[13]:

- the high energy gap of GaN is reflected into an high breakdown field 3500 kV/cm,
- the high energy gap of GaN results in a low thermal electron and holes generation and this makes GaN HEMTs suitable for high temperature applications,
- the 2DEG channel has an electron density of $10^{13}\ cm^{-2}$ five times higher than for GaAs-based HEMTs,
- the formation of the 2DEG channel is due to the polar and pizoelectric characteristics of GaN and there is no need of dopant,
- it is characterized by an high overshoot and saturation velocity (3 10^7 cm/s) and a good mobility (1200 $\frac{cm^2}{Vs}$)

2.1 Structure of GaN based HEMT

The simplest structure of GaN based HEMTs (shown in fig. 3) is composed by an heterostructure formed by a GaN layer and an AlGaN barrier (fig. 4).
This is a type I heterostructure in fact $E_C^{AlGaN} > E_C^{GaN}$ and $E_V^{AlGaN} < E_V^{GaN}$. Both electrons and holes passes from AlGaN to GaN.
The heterostructure can be Ga-face when the bonds parallel to the c-axis go from the cation (Ga or Al) to the anion (N) or N-face when the bonds go from the anion (N) to the cation (Ga or Al). In the former case if a cut along the c-plane is made the heterostructure would end-up with a Ga/Al-surface and in the latter with N-surface. This different configuration will give the material an opposite sign of the polarization charge.
Currently the majority of GaN materials used in power switching industry are grown in Ga-face direction.

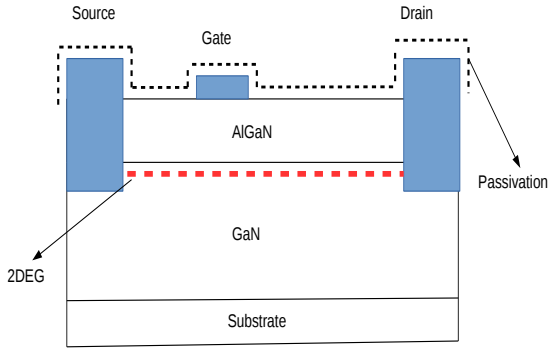


Figure 3: GaN High electron mobility Ga-face

The substrate is generally made of sapphire (Al_2O_3) or silicon (Si) or silicon carbide (SiC).
In GaN lateral transistors substrate has the function of suppressing leakage currents from drain to ground, and to sustain strong voltages (difference of voltage between drain and ground).

The metal junctions are implanted on the AlGaN barrier.
The gate is generally a Schottky junction. A Schottky junction has rectifying characteristics: in the specific case the work function Φ_M of gate metal is higher than the work function of the GaN semiconductor Φ_S and when a positive bias is applied electrons can move from semiconductor to the metal. When a negative bias is applied electrons are not able to overcome the junction. The metals used for gate contact are for example Nichel (Φ_M =5.15eV), Platinum (Φ_M =5.65eV) and Palladium (Φ_M =5.12eV).
The gate voltage bias is applied to create and modulate the 2DEG conductive channel.

The source and the drain are ohmic junctions. In this case electrons can move in both direction from metal to semiconductor. For a n-type semiconductor, in order to obtain an ohmic junction, the metal chosen should have a metal work function lower than the semiconductor work function. Typical materials are: Silver (Φ_M =5.10eV), Titanium (Φ_M =4.10eV) and Tungsten (Φ_M =4.55eV).
The current of the channel flows from source (generally ground connected) to drain (at high voltage).

The surface of the device is subjected to passivation. Passivation is the deposition above the device of a layer of a particular material generally Silicon Nitride (SiN) to create a shield against corrosion.

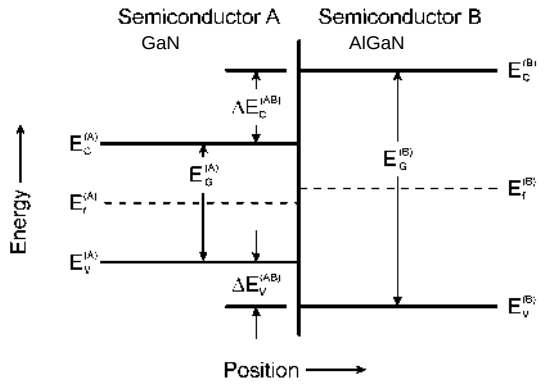


Figure 4: Heterostructure GaN/AlGaN

Another layer can be present: the lattice match layer (called *buffer layer* or *nucleation layer*) which have a big lattice mismatch with substrate crystal but has close lattice parameter to GaN. So there is the formation of many growth defects in the side of the lattice match layer in contact with the substrate, but few defects in the side of the lattice match layer in contact with the heterostructure.

2.2 Formation of two dimensional channel in GaN/AlGaN heterostructure

In order to explain the formation of 2DEG channel[1] we will reference to equation (7) of chapter 1.
For AlGaN the piezoelectric polarization is negative since the equation

$$(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) < 0$$

is valid over the whole range of compositions.
As a consequence, the orientation of piezoelectric and spontaneous polarization of AlGaN is parallel to the c-axis in case of tensile strain and anti-parallel to the c-axis in case of compressive strain of crystal layers.
Since AlGaN barriers are grown on GaN buffer layers AlGaN is therefore under tensile strain. So the spontaneous ($\vec{P}_{PSAlGaN}$) and piezoelectric ($\vec{P}_{PEAlGaN}$) polarization have the same sign and the total polarization is the sum: $\vec{P} = \vec{P}_{SPAlGaN} + \vec{P}_{PEAlGaN}$.
Also the GaN layer has a negative spontaneous polarization $\vec{P}_{SPGaN}$. The total polarization is therefore towards the $c - Al_2O_3$ substrate for Ga-face and toward the surface for N-face polarity crystal.

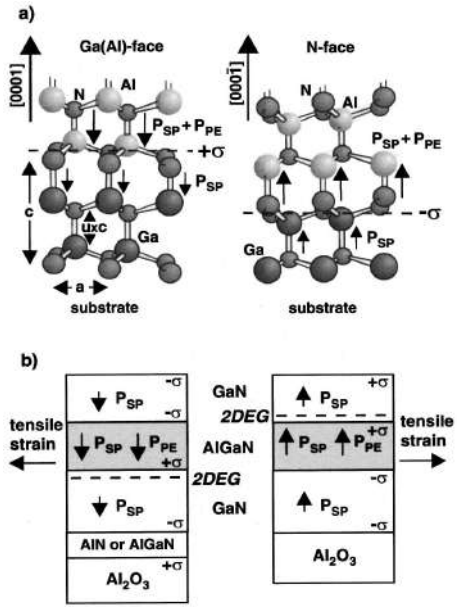


Figure 5: a) Ga-face and N-face at GaN/AlGaN interface and b) heterostructure

At the polarization vector $\vec{P}$ (P_c is the component along c-axis), is associated a density charge $\rho = -\vec{\nabla} \cdot \vec{P}$ and a superficial charge $\sigma = \vec{P} \cdot \hat{n}$ ($\hat{n}$ is the versor perpendicular to the surface).
At an abrupt interface of a top/bottom layer heterostructure (AlGaN/GaN or GaN/AlGaN) the superficial polarization charge is given by the sum of spontaneous and piezoelectric superficial charge:

$$\sigma(P_{SP} + P_{PE}) = P(bottom)_c - P(top)_c = \tag{16}$$
$$(P_{SP}(bottom)_c + P_{PE}(bottom)_c) - (P_{SP}(top)_c + P_{PE}(top)_c) =$$
$$(P_{SP}(top)_c + P_{SP}(bottom)_c) - (P_{PE}(top)_c + P_{PE}(bottom)_c) =$$
$$\sigma(P_{PE}) + \sigma(P_{SP})$$

If the total charge induced by the sum of piezoelectric polarization and spontaneous polarization is positive, a layer of free electrons is formed to compensate the charge at the interface. The result is a 2DEG channel if the conduction band drops below the Fermi level (fig. 6). In analogy if the total induced charge is negative this causes an accumulation of holes at the interface and the valence band crosses the Fermi level.
The positive induced charge is found to be (fig. 5):

- on top of GaN for Ga-face polarity and the formation of the 2DEG channel at lower AlGaN/GaN interface
- on top of AlGaN for N-face polarity and the formation of the 2DEG channel at upper GaN/AlGaN interface

Most of HEMTs are Ga-faces and they can be normally-ON if the channel is already formed without the application of a gate voltage or normally-OFF if a gate voltage is necessary for the formation of the conductive channel.

The charge concentration in the 2DEG channel is the same for Ga-face polarity and N-face polarity and it is given by:

$$n_s(x) = \frac{\sigma(x)}{e} - (\frac{\epsilon_0 \epsilon(x)}{d_{AlGaN} e^2})(e\Phi_b(x) + E_F(x) - \Delta E_C(x)) \tag{17}$$

where:

- $\epsilon(x)$ is the relative dielectric constant of AlGaN
- d_{AlGaN} and d_{GaN} are the thicknesses of the barriers
- e$\Phi_b(x)$ Schottky barriers of the gate contact
- $E_F(x)$ is the Fermi level with respect to the GaN conduction-band-energy
- ΔE_C is the conduction band offset at the AlGaN/GaN interface

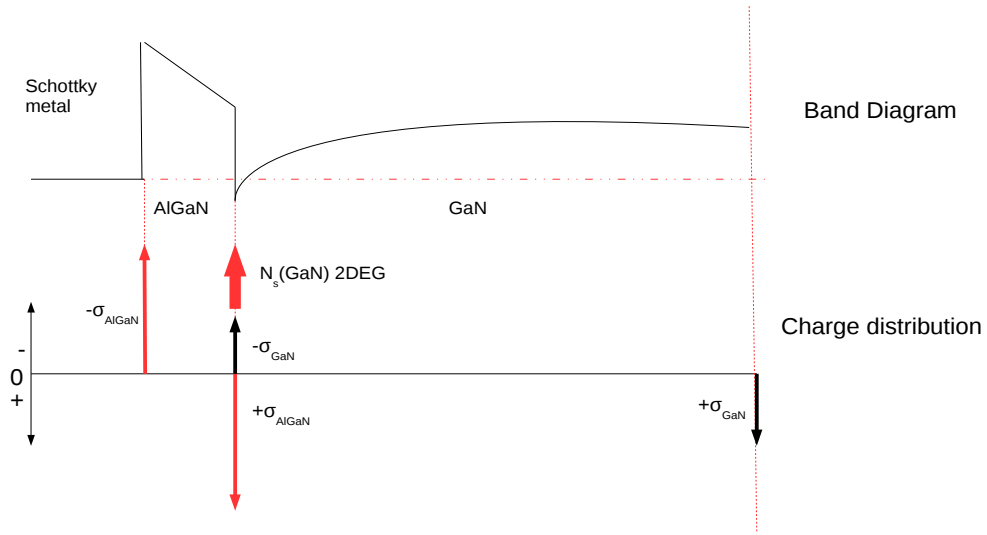


Figure 6: Band diagram of Ga-face hemt

Fundamental parameters in the characterization of the transistors are:

- the resistance of the channel $R_{ON} = \frac{dI_D}{dV_D}$,
- the threshold voltage V_{th} is the minimum gate voltage necessary to create the conductive channel.

2.3 Efficiency and reliability issues related to lateral devices

Lateral GaN HEMTs suffer from efficiency issues mainly due to trapping effects. Defects in reticular structure due to atoms vacancies, undesired atoms and lattice mismatch between different epitaxial layers create trap states for electrons or holes.

The phenomena which affect efficiency and reliability of HEMTs are various. An important issue is current collapse[14] which is significant drop of current when a high voltage is applied to the drain.
The current collapse is the main issue related to the efficiency of the device an it has been explained by the phenomenon of the virtual gate by Vetury et al.[15] (fig. 7 a).
This model argues that the surface AlGaN/GaN of a grown heterostructure has a net positive building charge. A negative screening charge is formed and a consequent negative surface potential arises which behaves as a negatively biased gate metal.
The virtual gate causes an increase of the depletion region, a consequence decrease in the electric field in gate edge and a lowering of the current.
The virtual gate potential V_{VG} is in series with the real gate potential V_G (fig. 7 b).
The current collapse phenomenon can be reduced by introducing a specific passivation to neutralize the superficial trap states[16]. Also the presence of field-plate can decrease current collapse by reducing the peak of electric field at the gate corner[17][18].
Another technique used is gate recess[19]. In this configuration the active area is moved away from the surface, reducing trapping mechanisms.

Another common phenomenon is Gate leakage current which is a current loss through the gate. There are several gate leakage mechanisms:

- Thermoionic emission[20][21]: thanks to thermal energy carriers overcome the Schottky potential barrier,
- trap assisted tunneling[22][23]: the traps inside the oxide splits the energy barrier into two parts thus allowing the the consecutive tunnel through thinner energy barrier and increase the probability of the tunneling process,
- Frenkel-Poole emission[24]: the electron overcome the metal-semiconductor barrier if subjected to high electric field.

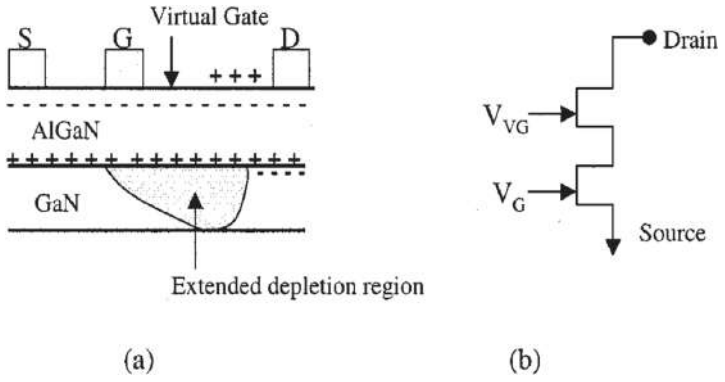


Figure 7: a) Increase of depletion region do to virtual gate,
b) Schematization of the virtual gate

Enhanced lateral devices have been developed in order to overcome the current leakage issues for example P-type HEMTs[25][26] with a layer of p-type doped GaN below the gate and MIS-HEMTs[27], with a superficial layer of dielectric to reduce gate leakage current.

There are other mechanisms which affect the reliability of these devices such as surface contamination through electrochemical reactions and the generation of defects or percolation inside the AlGaN layer when the device is applied a high drain voltage. The AlGaN layer is also subjected to cracks and pits following the application of a reverse bias voltage at gate-drain[14].

2.4 Limits of Lateral devices

Lateral power transistors have excellent electrical characteristics but their power handling is limited to few kWatt; this is an enhancement with respect to previous devices but it is not enough for future power applications.
The electronic devices used for power application should be able to manage high breakdown but BV scales with the distance between gate and drain (L_{GD}).

$$BV = E_c L_{GD} \tag{18}$$

Increasing L_{GD} implies an increase of the area of the transistor, an inefficient

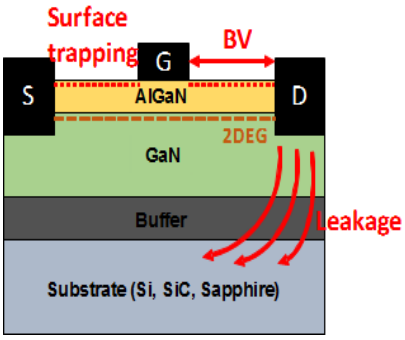


Figure 8: Issues and limitations of lateral HEMT

utilization of the material, difficult current extraction and poor reliability.

In lateral structure, the 2DEG channel (characterized by an high density and mobility) can be affected by superficial trapping.
Finally lateral HEMTs can suffer from substrate leakage current even if recent enhanced devices minimize this issue[28].

In order to overcome these limitation (fig. 8) and to improve the device performances for power applications, GaN based devices with new topologies have been developed, for example implementing vertical structures devices.

3. Vertical devices

Lateral devices show low conduction and switching losses that make them suitable as switch in power applications in the range of 650 V, moreover they do not require doping for the AlGaN/GaN heterostructure and they can be easily grown on silicon substrate. Nowadays, GaN HEMTs are commercially available with relatively low cost processing and good performance.
However, they do not handle high power levels required for applications such as electric vehicles, photovoltaic inverters, and industrial motors. In order to meet this request, a new topology has been developed for GaN transistors: the Vertical topology.
In vertical transistor current flows vertically through the device, unlike lateral structures in which current flows near the surface.

Vertical GaN devices for power electronics have the following advantages making them very suitable for power applications[29]:

1. the breakdown voltage in vertical GaN devices can be increased by increasing the thickness of the drift region while keeping the device size constant. Vertical devices are expected to reach higher breakdown voltage and power density then lateral devices,

2. the maximum electric field in vertical devices is far from surface and this reduces dynamic on-resistance and the trapping effects,

3. in vertical devices the current flows vertically and this allows to avoid the phenomenon of surface trapping and current collapse.

Vertical GaN Transistors are promising for future power electronics but few studies have still been developed concerning their stability and reliability. The aim of this work is to fill the gap and give an extensive analysis on the performance stability and trapping phenomena of a particular structure of GaN Vertical Transistor: the Vertical GaN based field effect transistors (VFET).

3.1 Elementary structure of Vertical GaN Transistor

The elementary and most general structure of a Vertical GaN Transistor is formed by the following layers (from top to bottom) as shown in fig. 9 a)[30]:

- GaN channel with Source and Gate implanted junctions,

- n^- doped GaN drift layer,
- GaN substrate,
- ohmic metal contact for drain.

From electrostatic the breakdown voltage BV (9 b)) can be calculated as[31]:

$$BV = E_c W - \frac{qN_D W^2}{2\epsilon_s} \tag{19}$$

where E_C is the critical field, W is the thickness of the n^- GaN drift layer, q is the electron charge, ϵ_s is the permittivity of GaN, N_D is the net carrier density of the n^- GaN layer.

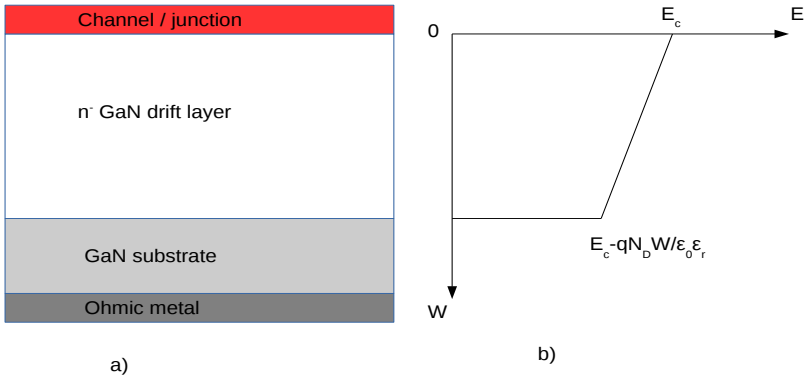
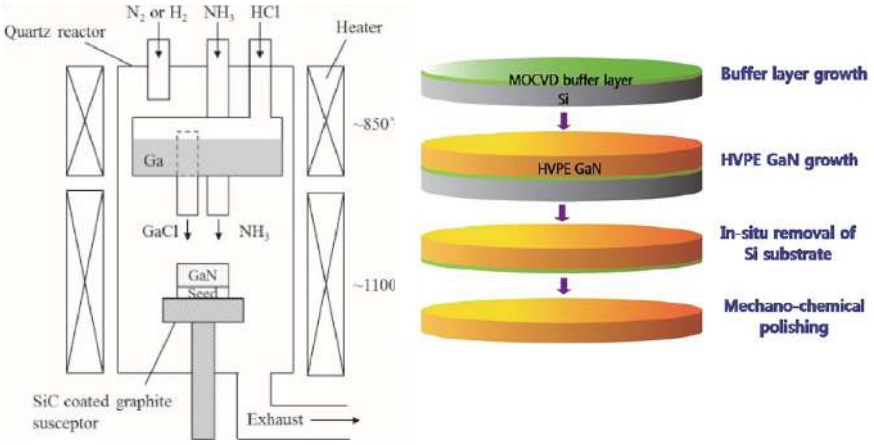


Figure 9: a) Elementary Vertical Structure on GaN Transistor b) Electric field in n^- layer

3.2 Growing and doping a Vertical GaN transistor

Vertical GaN transistors are not simple to be produced. The GaN substrate and GaN drift layer are grown through different techniques.

The Czochralski crystal growth process commonly used for silicon and GaAs cannot be used for GaN, due to its extreme melting condition.
The most common approach for manufacturing GaN substrate is
Hydride Vapor Phase Epitaxy (HVPE) (fig. 10).
In this process GaN films are grown in vertical reactor on a foreign substrate. The first step of the process is the production of gallium mono-chloride (GaCl)



a) b)

Figure 10: a) Vertical reactor for Hydride Vapor Phase Epitaxy b) Phases of Hydride Vapor Phase Epitaxy

in the reactor by reacting HCl gas with liquid Ga metal at $800 - 900°C$.
The GaCl is transported to the substrate where it is reacted with NH_3 at 1000-1100° C to form GaN, via the reaction:

$$GaCl + NH_3 \leftrightarrow GaN + HCl + H_2$$

The foreign substrate is then etched away.
The first foreign substrate used was sapphire but the large mismatch in thermal expansion coefficients creates cracking in GaN layer. A common foreign substrate is GaAs which have a lower lattice mismatch and can be easily etched away.

GaN n^--doped layer is produced through
Metalorganic Chemical Vapour Deposition (MOCVD) (fig. 11). The MOCVD process is extremely complex and involves a series of gas phases and surface reactions. In MOCVD ultra-pure gases are injected into a reactor and finely dosed to deposit a very thin layer of atoms onto a semiconductor wafer. Surface reaction of organic compounds or metalorganics and hydrides containing the required chemical elements creates conditions for crystalline growth epitaxy.

MOCVD has several steps which can be summarized as follow:

- evaporation and transport of reagents or precursors,

- pyrolysis of precursors leading to deposition of the semiconductor materials,
- removal of the remaining fragments of the decomposition reactions from the reactor zone.

The hydride source is NH_3 gas which can be stored in pressurized cylinders and conveniently dispensed through regulators and flow controllers. The gas handling of a MOCVD system regulates the delivery of amount of precursors into the reactor growth chamber. Typically it consists of a network of gaslines, with many gas switching valves.
Precursors which are in liquid or solid forms are kept in sealed containers called "bubblers" or "sublimers".
The growth chamber is where the reactions take place and can be "vertical" or "horizontal". In the vertical configuration, the gases are introduced from the inlet at top, and flow downward perpendicularly onto the surface of the substrate in the reactor. In the horizontal configuration the gases are introduced horizontally from the inlet and flow tangentially to the growth front. A fundamental requirement for the effective control of the MOCVD deposition process is to have laminar flow in the growth chamber where the carrier gases approach the substrate surface.
In the chamber there is a rotating disk reactor consisting of a disk which holds the wafer and spins at a high speed against the steady stream of gases flowing toward it at a normal angle.
In accordance with the boundary layer concept, it can be assumed that the gas in contact with the surface of the disk are stationary relative to it and moves at the same speed as the spin rate. Hence as the gas flows vertically toward the rotating disk, it is dragged by the disk to spiral down. The drag of the disk in essence acts as a pumping force to the gas. This pumping force can be used to counteract the convection effect of a heated disk surface.

The GaN layer is n^--doped. However as it can be seen in formula (19) and in fig. (12) in order to have high breakdown voltage n-doping should be kept low under $10^{16} cm^{-3}$.
Oxygen and in particular Carbon impurities are incorporated in GaN-layers during MOCVD process and they behave as donors or acceptors. MOCVD should therefore be optimized at high temperature and pressure to reduce the inclusion of these kind of impurities.

Many vertical transistors architectures such as CAVET are provided by *Current Blocking Layer* (CBL). CBL are p-doped layers used to force current flowing from source to drain.
The activation of implanted p-type doping (for example Mg) requires annealing temperatures over 1300°C, which causes the decomposition of GaN at atmospheric pressure. The decomposition brings loss of nitrogen, surface damage and nitrogen vacancies.
In order to prevent the loss of nitrogen at GaN surface a Aluminum Nitride (AlN) capping layer is deposit above the device. The AlN cap is deposited by chemical vapor deposition.
The technique used to enable the activation of Mg is Symmetric Multicycle

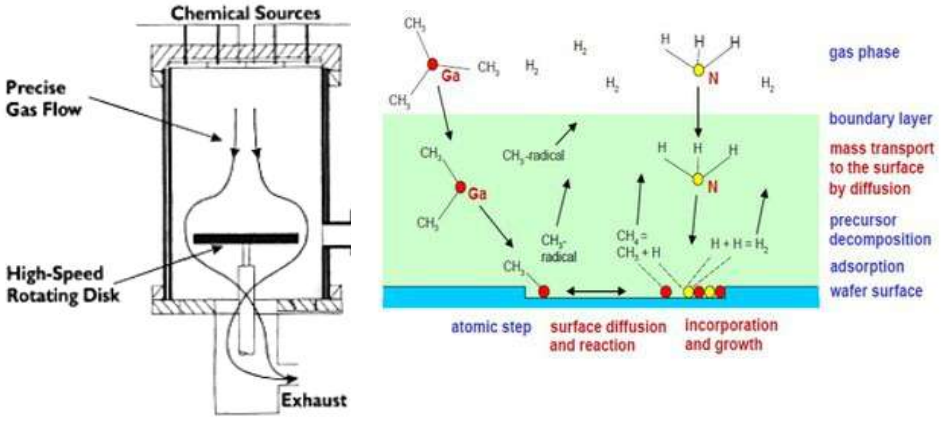


Figure 11: Metalorganic Chemical Vapor Deposition apparatus

Rapid Thermal Annealing (SMRTA). The process consists of 1000°C anneal for 30 minutes, followed by 40 pulses of 20s up to 1350°C at each cycle and another 1000°C for 30 minutes.

3.3 Different structures of Vertical Transistors

Several vertical device architectures have been proposed.

CAVET: Ben Yaacov et al. in 2004 proposed[32] a Current Aperture Vertical Electron Transistor structure (fig. 13).
The device is based on the formation in the source region, of the 2DEG channel of the AlGaN/GaN heterojunction and the current flows from the source contacts along the 2DEG but then through the aperture into the n-type GaN and it is collected at the drain.
The leakage current in vertical direction is suppressed through Mg Current Blocking Layer.
The aperture region required a dry-etching of the Mg-doped GaN and a regrowth of the n-GaN channel.
The etching of the aperture region exposed non-c planes and regrowth resulted in non-planar layers.
This increased gate leakage current and n-impurities tended to incorporate in

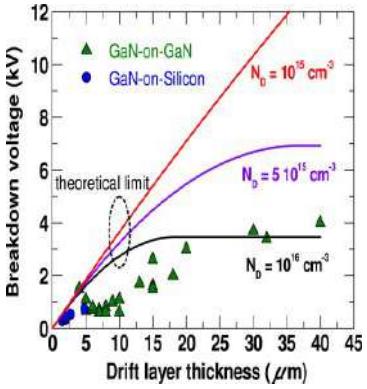


Figure 12: Breakdown Voltage versus drift layer for vertical diodes at different doping values

the aperture region and leads to a reduction of device breakdown voltage.
In order to overcome this issue new techniques without the regrowth of GaN on the aperture region were used.
AlGaN/GaN layers are grown through Molecular Beam Epitaxy technique over CBL.
However, the CAVET shows normally-on operations and poor pinch-off capability, requirements necessary for power applications.
The big enhancement of this type of device is that the peak of the electric field is buried in the bulk region below the gate metal. The consequence is that there is not an electric field on the surface and charge does not accumulate at the gate edge.
Main problems of CAVET are is intrinsic normally-on operation and poor pinch-off capability.

Trench CAVET: in order to overcome CAVET limitations Shibata et al.[33] proposed a new structure (fig. 14 d)).
This new architecture is characterized by a V-groove on which a GaN/AlGaN heterostructure and a p-type gate are grown.
The trench CAVET design places the channel at the sidewall of the etched trench, which enables the normally OFF operation.
Another big advantage of this configuration is that by using the slanted channel a higher V_{th} is achieved as it can be seen in fig. 14 a) b) c).
Due to activation inefficiency of Mg-doped p-type layer the conventional CAVET shows a leakage current in CBL. The current loss is reduced in the trench CAVET with hybrid blocking layer with carbon-doped GaN and p-type layer.
This improves breakdown voltage from 580V up to 1.7kV.

Trench MOSFET: the main characteristic of this kind of vertical transistor is

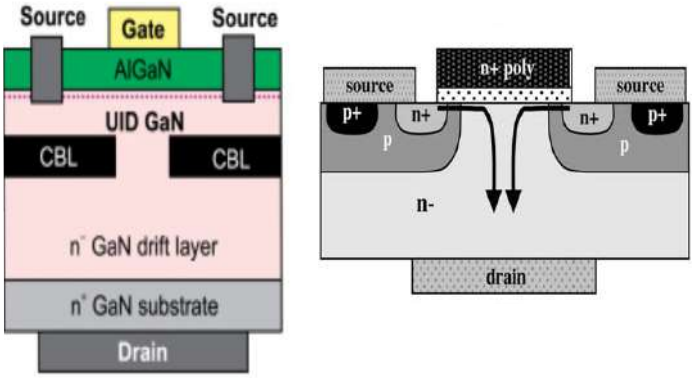


Figure 13: a)Current Aperture Vertical Electron Transistor b)Current in CAVET

the absence JFET region of the AlGaN/GaN heterostructure[34][35] (fig. 15 a)). In the first trench MOSFET architectures the channel was on the [0001] plane where spontaneous and piezoelectric effects are present. Therefore an enhanced stucture has been developed etching on [0001] plane GaN: the channel along the gate vertical surfaces.
Vertical structure has a channel on $[1\bar{1}00]$ plane produced through wet-etching, reported by Itoh et al.[36]
By optimizing the etching techniques different etched shapes have been obtained: in particular the U-shape trench with rounded corner and smooth sidewalls is optimal to achieve high voltage due to suppression of the electric field which is stronger at the corners[37] (fig. 15 b)).

The CAVET, Trench CAVET and trench MOSFET structures are very promising for power applications but they still have issues concerning the epitaxial growth and the working performance. For example in the GaN CAVET and trench MOSFET structures, epitaxial regrowth or p-GaN layer for CBL is required and it increases the production process complexity and the poor transport properties of p-GaN channel results in high on-resistance[38][39].

Vertical Fin FET Transistors is a new normally-off MOSFET with a submicron

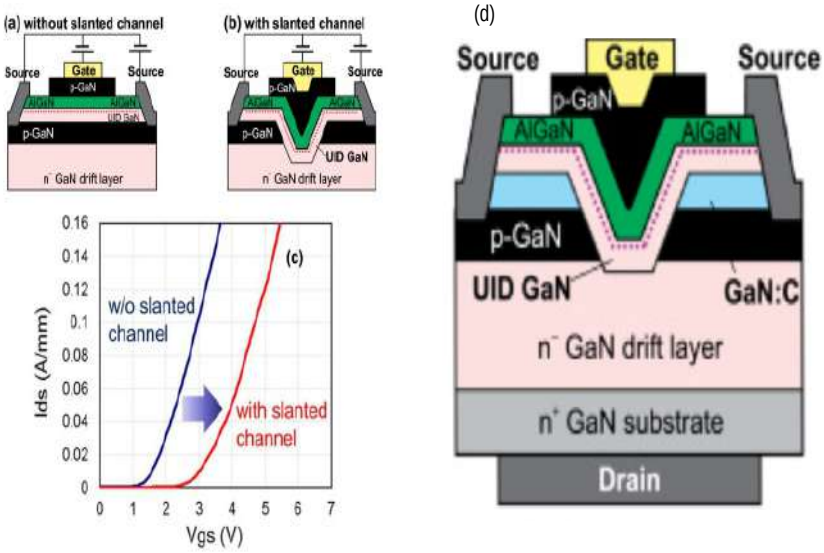


Figure 14: a) Transistor without slanted channel b)Transistor with slanted channel c)Comparison $I_D - V_G$ curves of two transistors d)Current Aperture Vertical Electron Transistor

vertical fin[40] (fig. 16 a)).
In Fin FET there is no need of p-GaN doped layer, with only n-type GaN epilayers and this reduces the production complexity.
This devices are based on a Fin-architecture where current flows through nanometer-sized channels having a MOS stack on the sides.

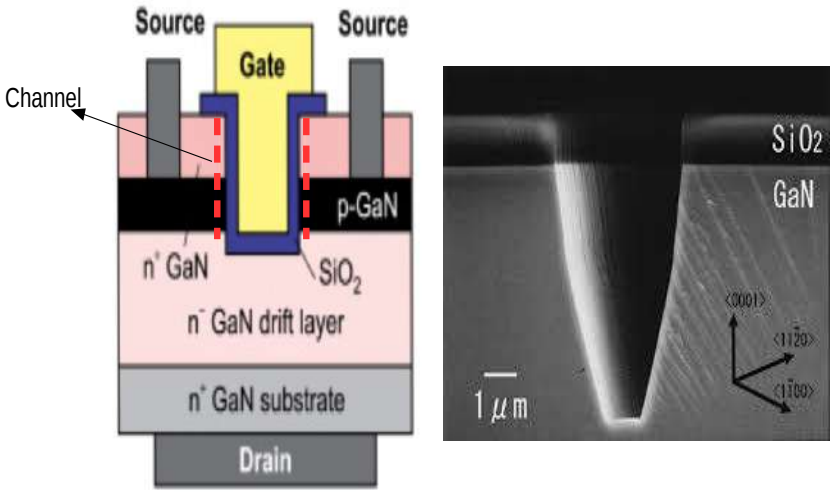


Figure 15: a) Trench MOSFET Transistor b)U-shaped trench

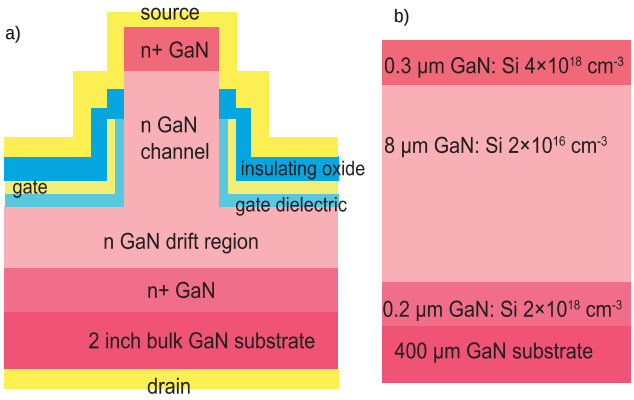


Figure 16: a) Vertical Fin FET b)Doping distribution

4. Fin FET transistors

4.1 Structure of tested devices

The aim of my work of thesis is to analyze the GaN Vertical fin FETs provided by Massachusetts Institute of Technology (MIT) measuring variations of performance in relationship to channel width, variation of external parameters such as temperature, exposure to UV-light, application of gate positive voltage for different channel widths. By means of simulations, we demonstrate a physical model of the behaviour of the transistor and the mechanisms of charge trapping in the oxide.
In fig. 17 is pictured the wafer on which transistors are grown.
The wafer is composed of cells pictured in fig. 18 a). Each cell is formed by two types of devices (fig. 18 b), c)). In my master thesis the devices of type in fig. 18 c) are examined.

The cross section of tested devices is shown in fig. 19 a). The epitaxial-structure is grown by metal-organic chemical vapor deposition (MOCVD) on 2 inch bulk GaN substrates.
These devices are based on a fin-architecture, where current flows through nanometer-sized channel having a MOS stack on the sides.
The fin-shape vertical channel is surrounded by gate metal electrodes. The source contact is on the fin channel.
At $V_{GS} = 0V$ the channel is depleted due to difference between the work function of gate metal and GaN channel.
Increasing V_{GS}, electrons accumulate at fin interface and channel is formed.
The device is made of layers of different n-doping (fig. 16 b)):

- 400μm GaN substrate,
- 0.2μm Si doped 2x10^{18} cm^{-3} GaN layer
- 8μm lightly Si doped 2x10^{16} cm^{-3} GaN drift layer
- 0.3μm heavily doped 4x10^{18} cm^{-3} GaN cap layer

A layer of 15nm Al_2O_3 is placed as a gate dielectric and a molybdenum layer as gate metal.

The device is built by using several different constructive techniques. The epitaxial-structure is grown by MOCVD on the GaN substrate. The channel fins are made by a top-down fabrication technology. Sub-micrometer width is

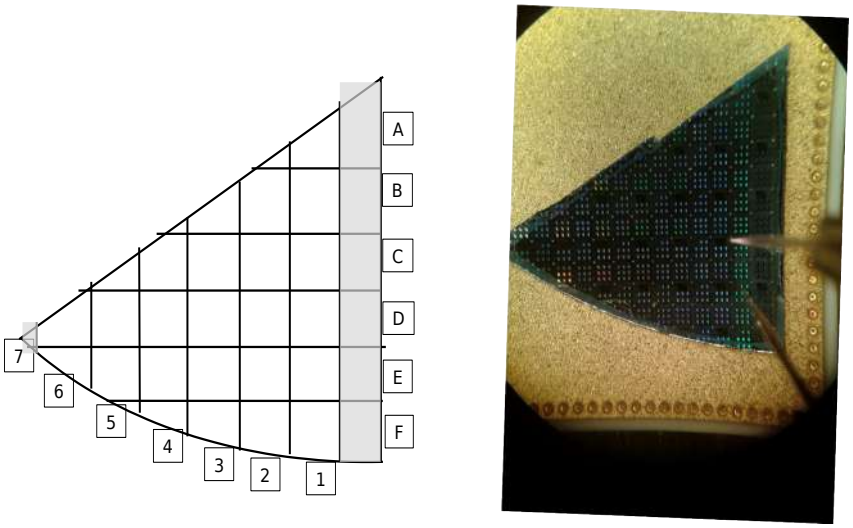


Figure 17: MIT Fin FET Wafer

necessary to achieve normally off operations. The fins are defined by electron beam lithography consisting in the following steps:

- dry etching: the masked pattern of the fins is removed by the exposition to a bombardment of ions,
- the sample is dipped in hot Tetramethylammonium hydroxide solution.

The oxide is deposited by Atomic Layer Deposition: the deposition of thin layers through the reactions of precursors in atomic phases.
A layer of dielectric is sputtered on the device and a layer of photoresist is deposited on the surface.

The fins looked from above form the ribbons (fig. 19 b)) forming the active area of the transistor.

Source metal contact is placed over the n^+ GaN cap and the gate metal is on both the left and right side of the fin. The sources and the gates of every ribbon

are short-circuited together fig. 18 a).
Also the drains are short-circuited together and they can be contacted through a copper plate (conductive side in contact with the device) bonded to a ceramic substrate (insulation side) (curamik).

Between the gate metal and the GaN channel there is a 15nm wide layer of oxide (Al_2O_3).

56 GaN channel layers operate in parallel. Current control is obtained thanks to a MOS structure (metal=molybdenum, insulator Al_2O_3) on the sidewall of each fin. For $V_{GS} > 1V$, a channel is formed through accumulation) at GaN/Oxide interface, and current can flow vertically. These devices are an example of Vertical Device with promising performance: the presence of a vertical channel of nanometric dimension allows to eliminate the current blocking layer of p-doped GaN which was previously necessary to force current flowing from source to drain and was responsible of growing of R_{ON}.

As can be seen in fig. transistors have been produced with different channel widths from 70nm to 280nm.

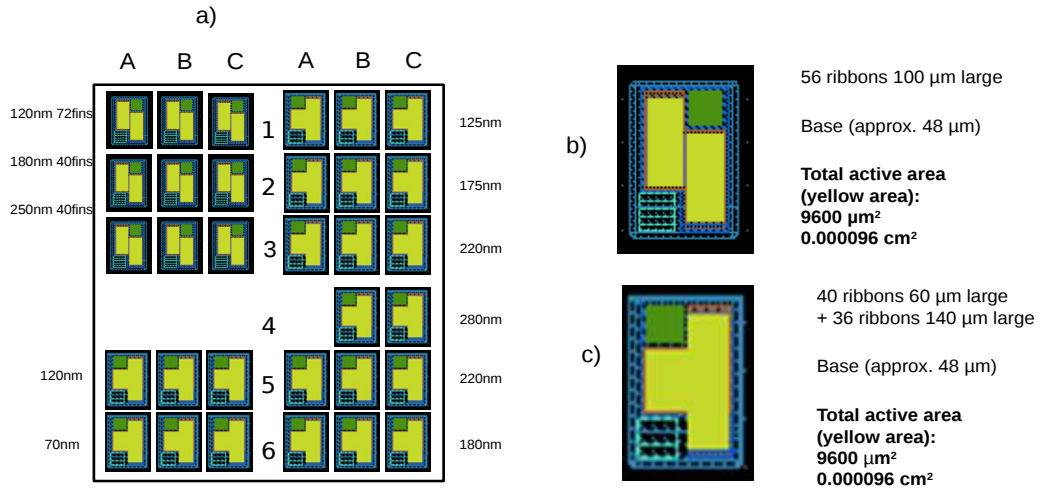


Figure 18: a) A cell of MIT Wafer, b) and c) Two typologies of Fin FET devices

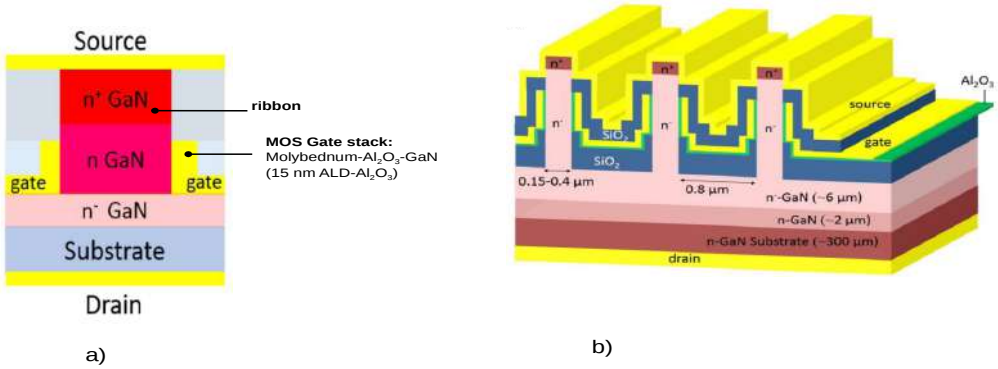


Figure 19: a) Fin FET Transistor, b) Ribbons of the Fin FET transistors

4.2 Device performance and behaviour

Measurements start with Direct Current characterization of devices at room temperature.
This measurements are necessary for an overview of the threshold voltage V_{th} and the on-resistance R_{ON} of this kind of transistors and their variation with channel width.

Gate and source zoomed under an optical microscopy, are contacted by the use of probes. A third probe contacts the curamik and thus the drain.
The measurements are performed through Agilent E5260/E5270 an electronic instrument for the semiconductor DC parametric measurements. The parameter analyzer consists of a source/monitor unit (SMU) which is able to furnish voltage and current and measure voltage and current.
SMU has triaxial connectors to the probes.
Source is usually grounded (o connected to zero bias), gate and drain are biased to a defined voltage (V_{GS}, V_D).

Through DC-measurements the following plots are obtained:

- I_D-V_{GS} plots varying V_{GS} from -1V to 4V with fixed value of V_{DS} (0.1V, 0.5V, 1V, 2V, 4V),
- I_D-V_{DS} plots varying V_{DS} from 0V to 4V with fixed values of V_{GS} (-1V, 0V, 1V, 2V, 3V, 4V),
- transconductance: $g_m = \frac{dI_D}{dV_{GS}}$
- the leakage current of source and gate diode.

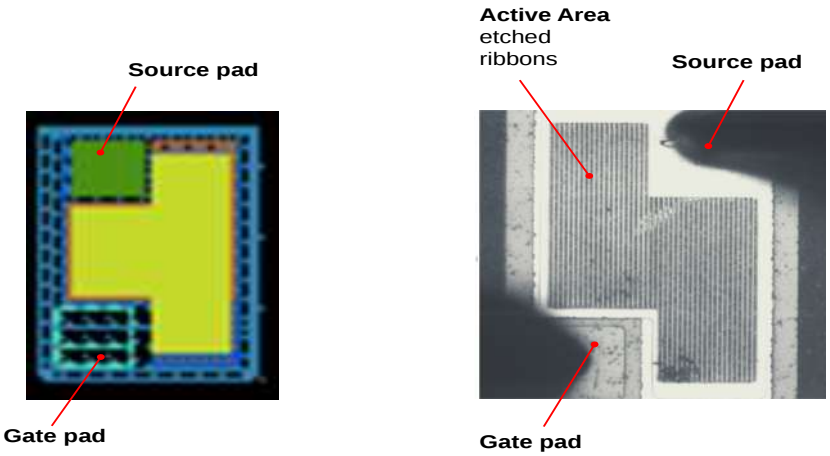


Figure 20: a) Source and gate contacts obtained short-circuiting source and gate of each ribbon, b) Photo of the ribbons of the Fin FET transistors

Here is an example of DC-analysis plots (fig. 22 and fig. 23) of the device 220nm channel width , of cell D5 row 5 column C and of the device 120nm channel width , of cell D5 row 5 column B (fig. 24 and fig. 25).
The calculated parameters for each examined device are (Table 5 and Table 6):

- R_{ON}: the channel resistance between drain and source. It is calculated as the reciprocal of angular coefficient of I_D-V_{DS} graph, in the linear region of I_D-V_{DS} plot in ON condition,

- V_{th}: minimum voltage applied at the gate necessary for the formation of the conductive channel. Two methods are used for V_{th} calculation:

  1. in the first method a linear fit is made in the linear behaviour zone of I_D-V_{GS} graph. V_{th} is the opposite of the ratio between intercept and slope of the linear fit: I_D = m V_{GS} + q where m is the slope and q the intercept. V_{th} is:

$$V_{th} = V_{GS}(I_D = 0V) = -q/m \tag{20}$$

  2. In the second method V_{th} is the value of the gate potential at which the current reaches the value of 10^{-7}A.

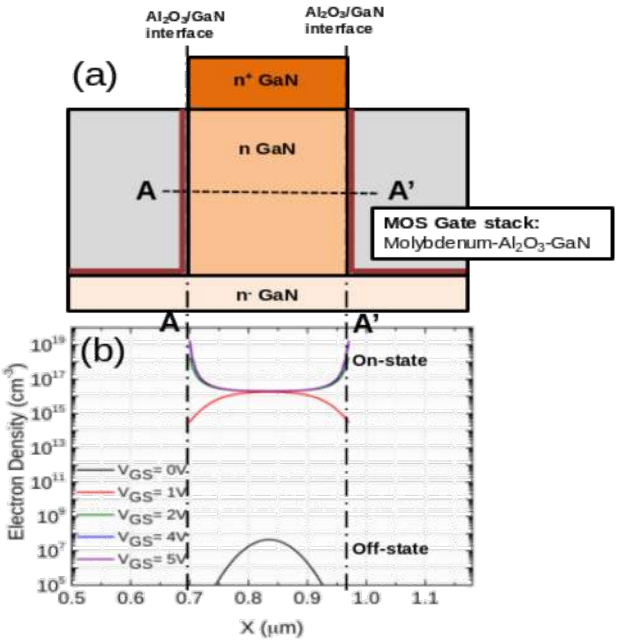


Figure 21: a) Channel of Fin FET transistor, b) Simulation of electron density: for V_{GS}=0,1V the electron density peak is in the center of the channel, for V_{GS}=2,4,5V the electron density peak is on the surface of the channel

4.3 Direct current measurements: summary of the results

In performing this kind of measurement we pointed out the relation between parameters R_{ON} and V_{th} and channel width.

In fig. 26 V_{th} and R_{ON} at different channel widths in two cells (D1,D5) at V_{DS}=1,2,4V are plotted.
And in fig. 27 there is a summary of V_{th} and R_{ON} at different channel widths, of devices belonging to different cells.

R_{ON} [Ω] @ 4V	11.260 ± 0.007	
	V_{th} [V] first method	V_{th} [V] second method
@ 1V	0.47 ± 0.02	0.10 ± 0.05
@ 2V	0.51 ± 0.02	0.08 ± 0.02
@ 4V	0.49 ± 0.02	0.06 ± 0.04

Table 5: Calculated R_{ON} and calculated V_{th} with two methods for device of 220nm channel width

R_{ON} [Ω] @ 4V	29.601 ± 0.003	
	V_{th} [V] first method	V_{th} [V] second method
@ 1V	0.77 ± 0.05	0.41 ± 0.04
@ 2V	0.80 ± 0.07	0.41 ± 0.06
@ 4V	0.85 ± 0.03	0.41 ± 0.03

Table 6: Calculated R_{ON} and calculated V_{th} with two methods for device of 120nm channel width

As conclusions we can say that there is a huge variability of the parameters between the same type devices too.
But despite the variability, the general tendencies observed are:

- R_{ON} seems have no dependence on channel width,
- V_{th} is higher for devices of 70nm channel width, then for more than 120nm it seems to have no dependence on channel width.

Even if we do not have enough devices with different channel widths, we can imagine that V_{th} is in general higher for devices with thinner fin and decrease increasing the channel dimension until an asymptotic value.
This means that devices with higher channel widths start to conduct current at lower gate potential.

4.4 Direct current measurements: hypothesis

Preliminarly simulations[41] has been performed to explain the behaviour of this type of transistors (fig. 28).

Simulations were made for a fixed channel width (270nm) and they have shown that in this device for low values of gate potential (V_{GS}) the electron density rises at the center of the channel, for higher values of V_{GS} the electron density peak is on the Al_2O_3/GaN surface of the fin and a vertical nanometer-size conductive channel is formed.

The devices with lower channel width have higher threshold voltage in respect to devices with higher channel width, this can be related to the creation of a parasitic current (peak of electron density at the center of the channel width) that shifts the threshold voltage towards lower values for channel widths higher than 70nm.
We can assume that the parasitic current occurs in the devices with higher channel width (for example 220nm) but not in those with lower channel widths (for example 70nm) (fig. 28).

4.5 Direct current measurements: variation of threshold voltage with temperature

In order to study the variation of threshold voltage with temperature, DC measurements at different temperatures were made on devices with 220nm and 120nm channel widths. Temperature is varied from 30°C to 110°C.
In conclusion by increasing the temperature the observed tendencies are:

- a positive shift of threshold voltage is observed for both devices of 120nm and 220nm. The increasing of V_{th} seems not depending on channel width (fig. 29 a),b)). This tendency can be explained by activation of trapping phenomena.
- a light increase of R_{ON}. As for V_{th} the increasing seems not linked to the channel width and can be due to a decrease of mobility.

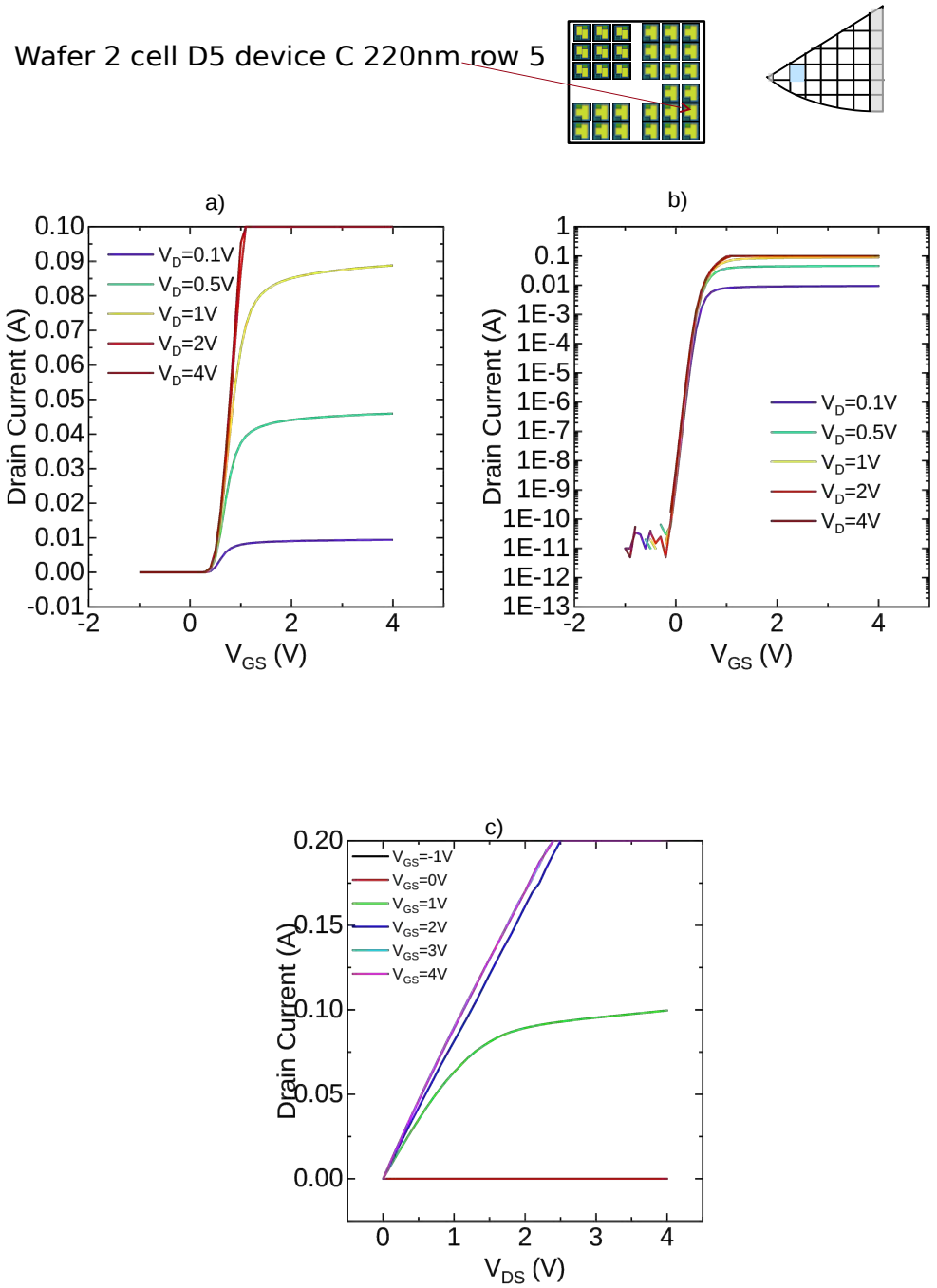


Figure 22: a) Drain current-Gate voltage plot of 220nm channel width device , b)Drain current-Gate voltage plot in logarithmic scale of 220nm channel width device, c) Drain current-Drain voltage plot of 220nm channel width device

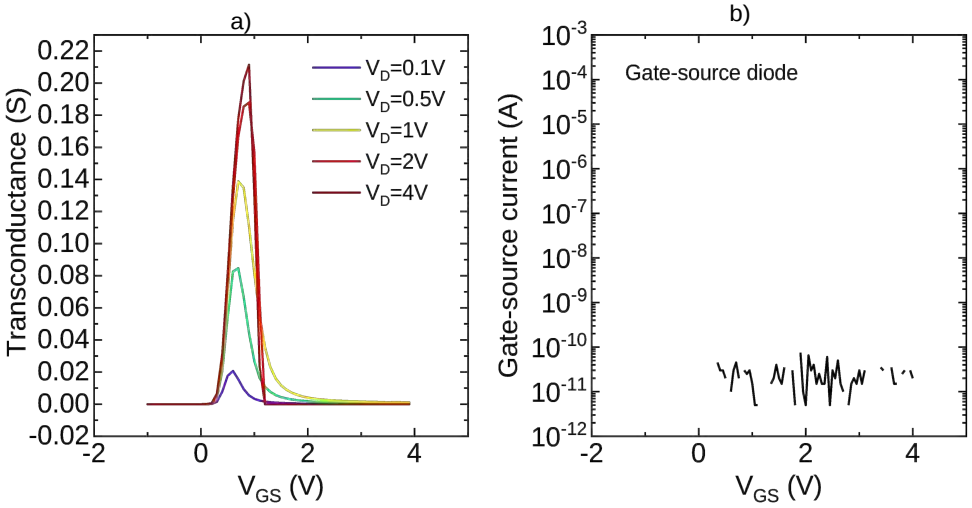


Figure 23: a) Leakage current gate-source diode of 220nm channel width device
b) Transconductance of 220nm channel width device

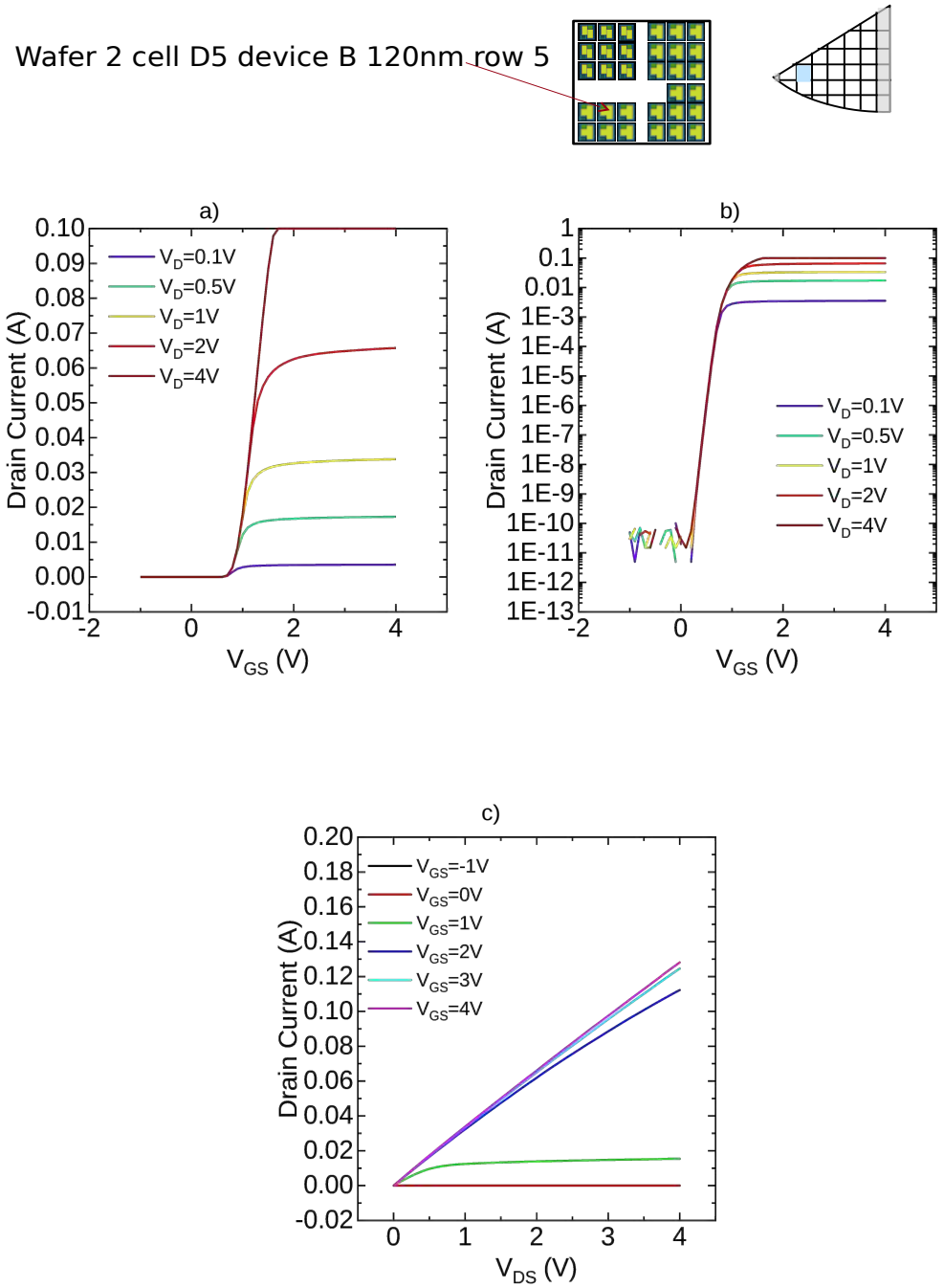


Figure 24: a) Drain current-Gate voltage plot of 120nm channel width device , b)Drain current-Gate voltage plot in logarithmic scale of 120nm channel width device, c) Drain current-Drain voltage plot of 120nm channel width device

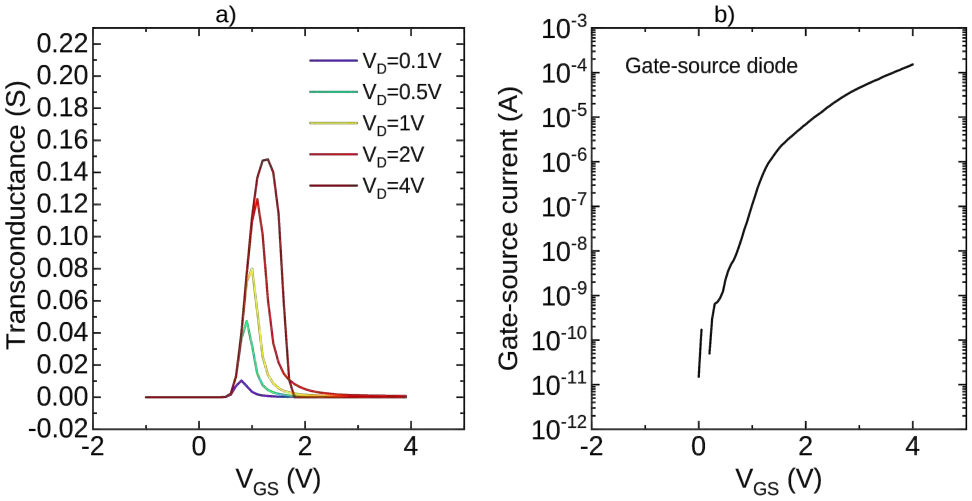


Figure 25: a) Leakage current gate-source diode of 120nm channel width device
b) Transconductance of 120nm channel width device

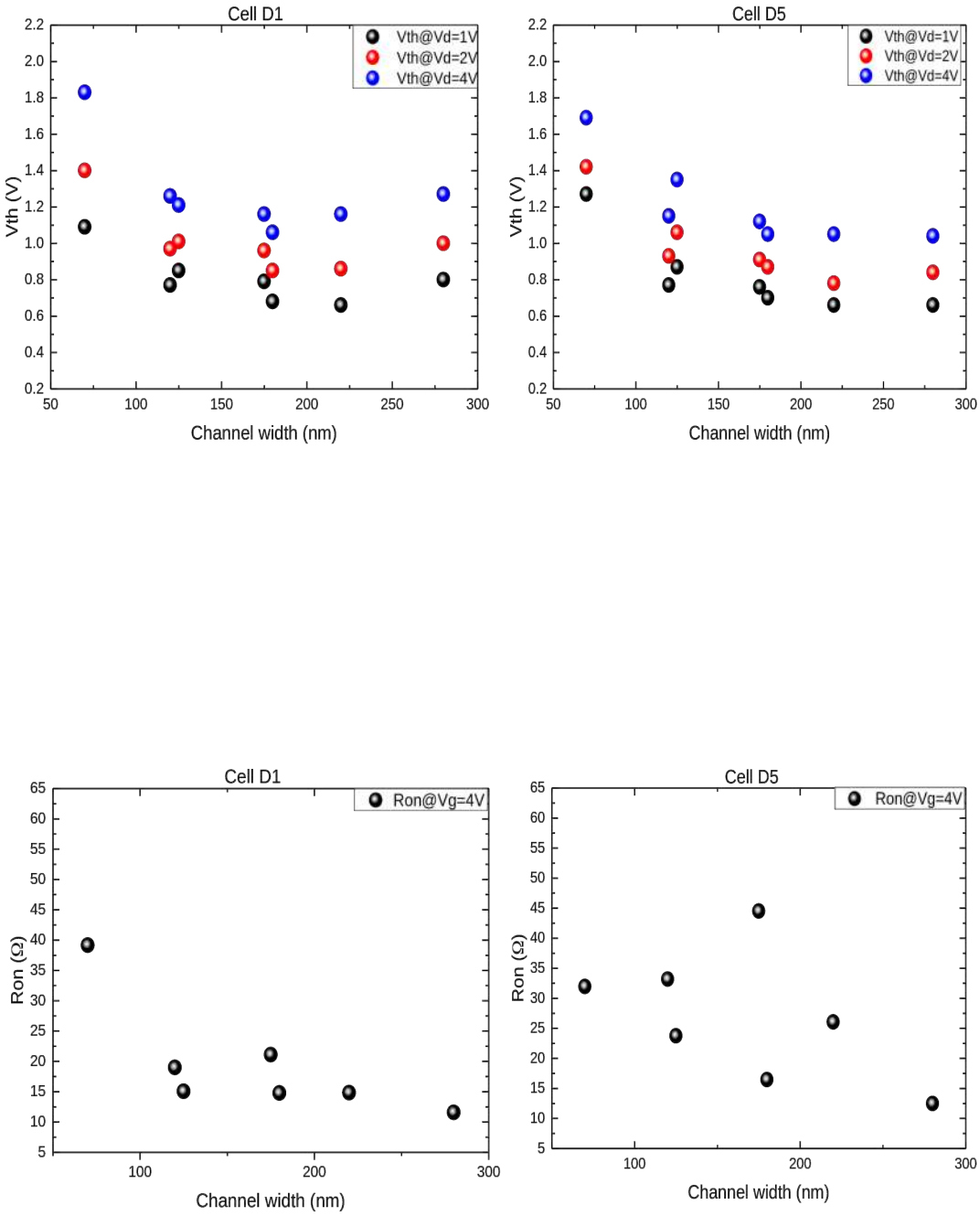


Figure 26: V_{th} and Ron for different channel widths in cell D1 and D5

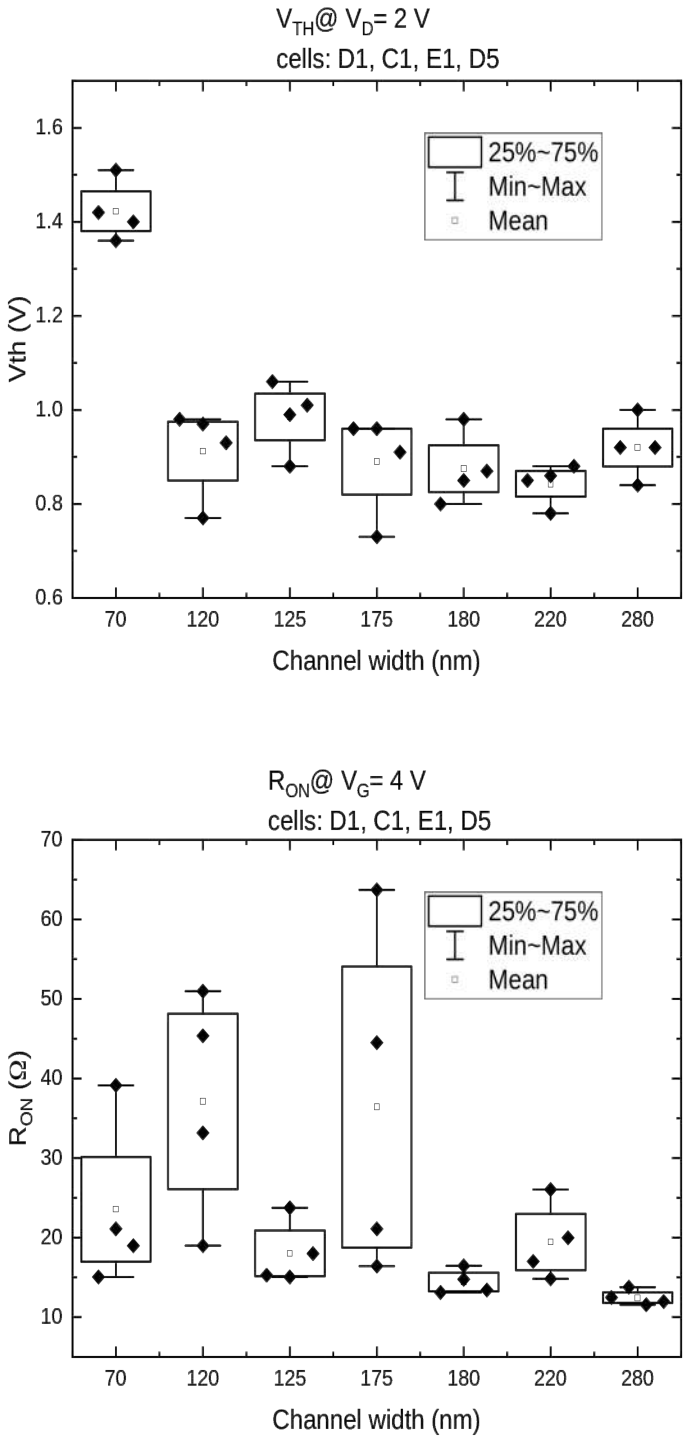


Figure 27: Summary of V_{th} and Ron for different channel widths. V_{th} is higher for 70nm channel width. R_{ON} seems to have no dependence on channel width

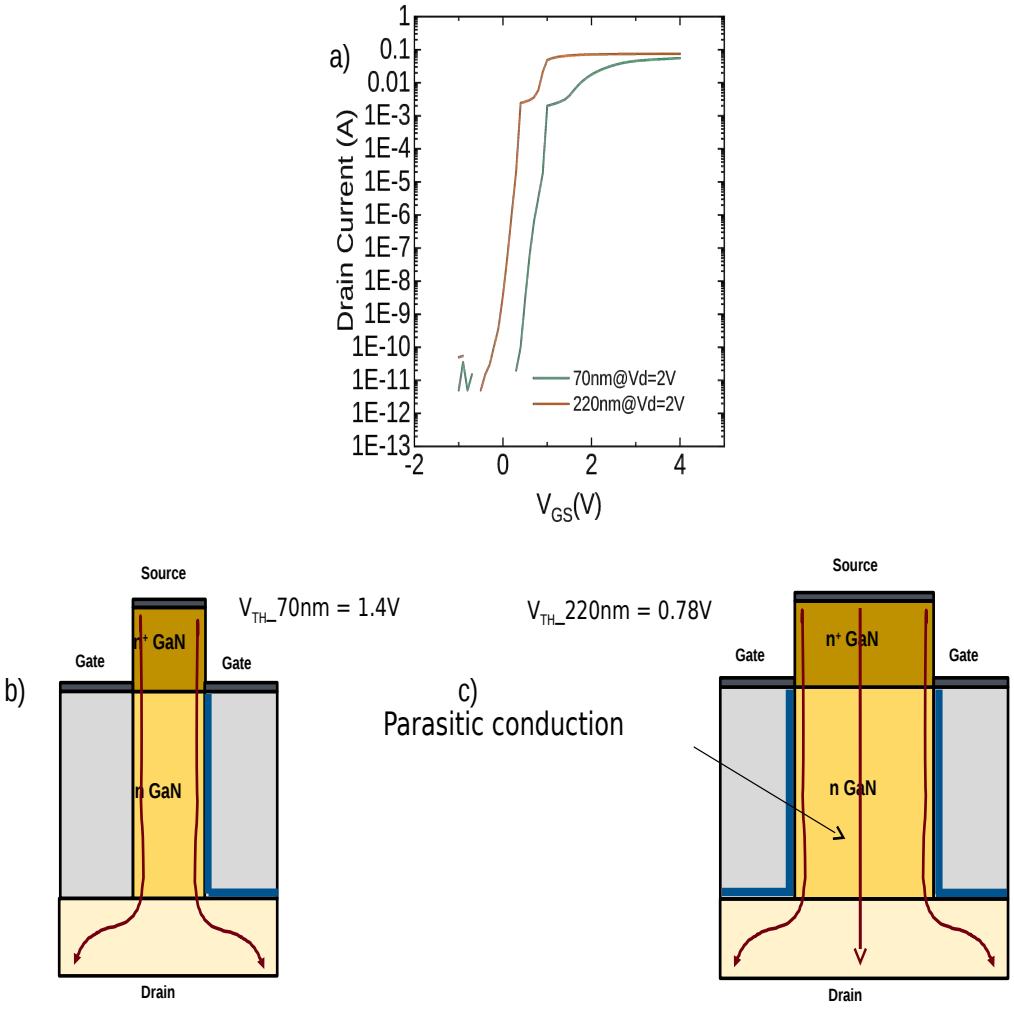


Figure 28: a) I_D-V_{GS} of devices of 70nm and 220nm channel widths, b) Picture of 70nm Fin FET transistor without parasitic conduction, c) Picture of 220nm Fin FET transistor with parasitic conduction

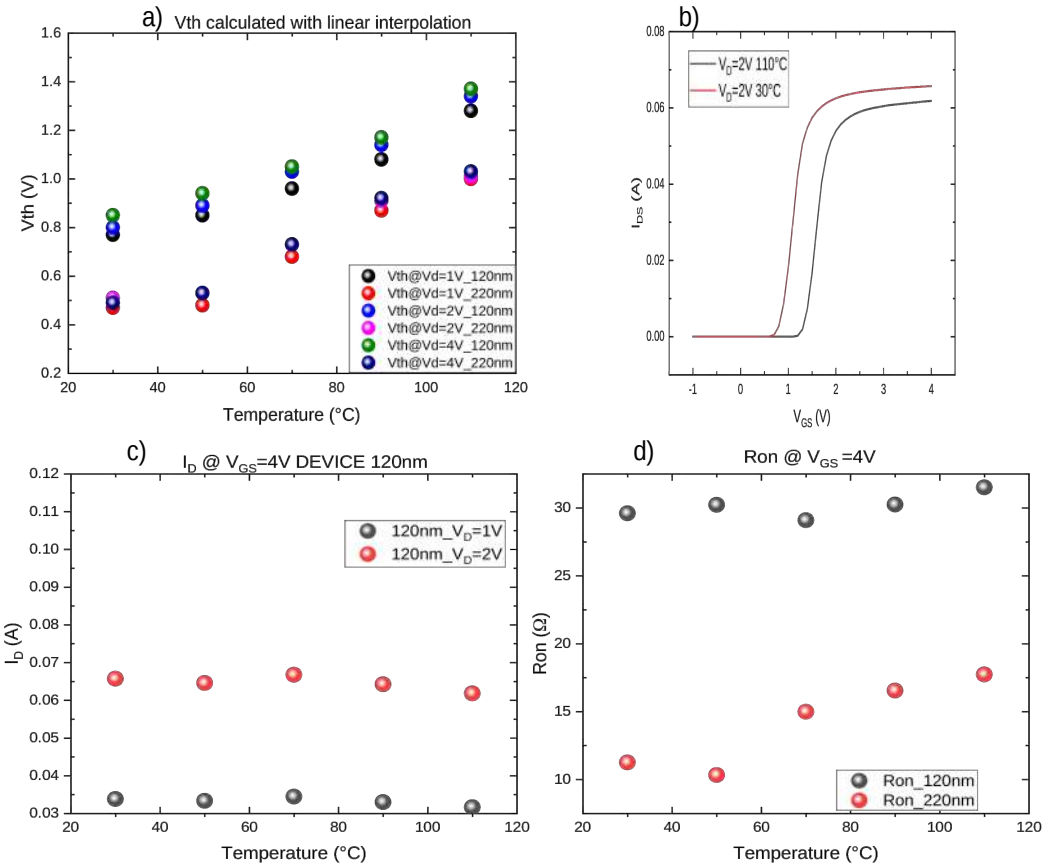


Figure 29: a) V_{th} of 120nm and 220nm channel widths at different temperatures for V_D=1,2,4V, b) I_D-V_{GS} of device 220nm channel width at 30°C and 110°C for V_D=2V, c)light decrease of current in 120nm channel width device for V_D=1,2V and V_{GS}=4V d)light increase of R_{ON} for devices 120nm and 220nm channel widths for V_{GS}=4V

5. Analysis of trapping

In the analysis of the variations of transistors parameters for example during the application of different gate voltages or the variation of external parameters such as temperature, a crucial role is played by trapping phenomena.

In particular the main trapping effect is the oxide trapping, activated by the application of a voltage at the gate.

In order to study trapping phenomena the device should be kept under *trapping condition*.
Which means that a gradually increasing positive potential should be applied to the gate, to improve trapping and measurements should be made under this condition.

Charge-trapping effects were investigated by Double Pulsed measurements.
In these measurements the device is exposed to different quiescent (stress) conditions increasing the gate bias voltage and through double pulse measurements I_D-V_{DS} and I_D-V_{GS} curves at different stress conditions are obtained.

5.1 Double Pulse measurements: setup

In Double Pulsed measurements both gate and drain contacts are synchronously pulsed from a quiescent bias-point ($V_{GS,Q}$;$V_{DS,Q}$) to a measurement bias-point ($V_{GS,M}$;$V_{DS,M}$); during the measurement phase, the drain-current (I_D) is acquired thanks to the presence of a current-sensing resistor (50Ω). For this study the quiescent bias points were selected at different positive gate voltages (while quiescent drain voltage is kept zero $V_{DS,Q}$=0V) and the sweep of I_D-V_{DS} and I_D-V_{GS} was performed from 0V to 5V at V_{GS}=4V and V_{DS}=2V, respectively.
The device is subject to $V_{GS,Q}$ for 5ms (this is the trapping phase), the measurement phase lasts 5μs (fig. 30).

The double pulse setup is composed by (fig. 31):

- 2 waveform generators (Agilent 33250A),
- 2 amplifiers (20x) (FLC A400),
- current sensing resistor (50Ω) ,
- a differential probe (10x attenuation),

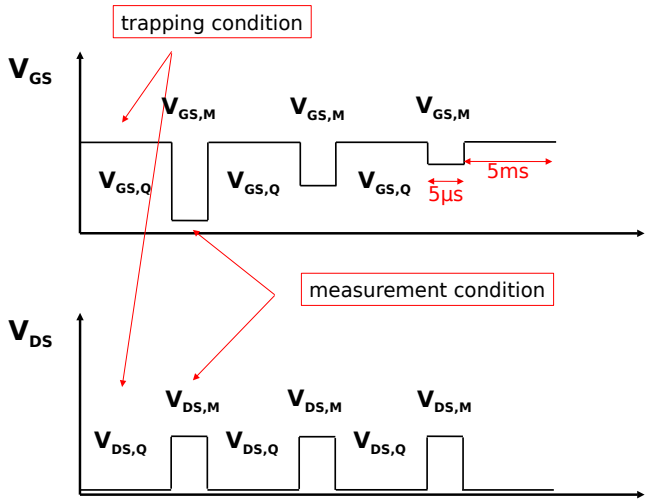


Figure 30: Double Pulse waveform

- oscilloscope (Tektronic TD654C),
- 50Ω input impedance gate amplifier.

5.2 Double Pulse measurements: results

As shown in plot of fig. 32 double pulse measurements were performed for $V_{GS,Q}$=0,1,2,3,4,5V and, after the measurements, a $V_{GS,Q}$=0V double pulse is made in order evaluate the recovery of a possible change of parameters V_{th} and R_{ON}.

All devices examined have the same behaviour which is independent from the channel width.

A negligible variation in RON is detected under positive gate bias.

For V_{th} calculated from I_D-V_{GS} obtained increasing $V_{GS,Q}$, two opposite tendencies have been observed (fig. 33):

1. at low $V_{GS,Q}$ ($\leq$2V or $\leq$3V) there is a negative shift of V_{th},
2. at higher $V_{GS,Q}$ there is a change of tendency: V_{th} increases reaching the initial value and for $V_{GS,Q}$=4,5V exceeding it.

I_D-V_{GS} of the last double pulse at $V_{GS,Q}$=0V made after measurements shows that there is no recovery and V_{th} assumes the value of the double pulse made at $V_{GS,Q}$=5V.

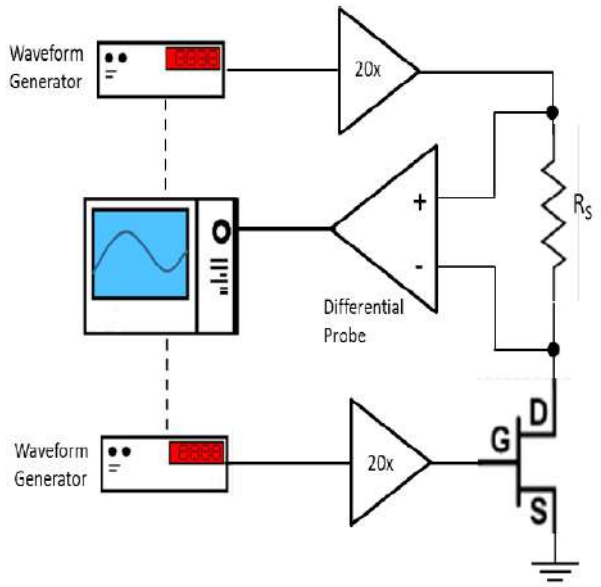


Figure 31: Double Pulse setup

5.3 Double Pulse measurements: hypothesis

This behaviour can be explained by the action of two different phenomena:

1. when a (moderate $V_{GS,Q}$=1,2V) positive gate bias is applied, electrons trapped in the oxide are detrapped towards the gate metal. It results in a net positive charge in the oxide charge tending to attract electrons from the channel at the turn on (fig. 34). Thus, the threshold voltage moves towards lower values (negative shift).

2. Increasing $V_{GS,Q}$ electrons are injected inside the oxide and accumulate on the interface between oxide and GaN rejecting other electrons and causing the increase of V_{th} (fig. 35).

The injection of electrons in the oxide could be favored to the presence of positive charge at the oxide/GaN interface. This charge is originated from defects and trap states generated during the growth process.

Electrons remain trapped in oxide for long times, in fact Double Pulsed at measurements at $V_{GS,Q} = 0V$, performed after hours showed no recovery.

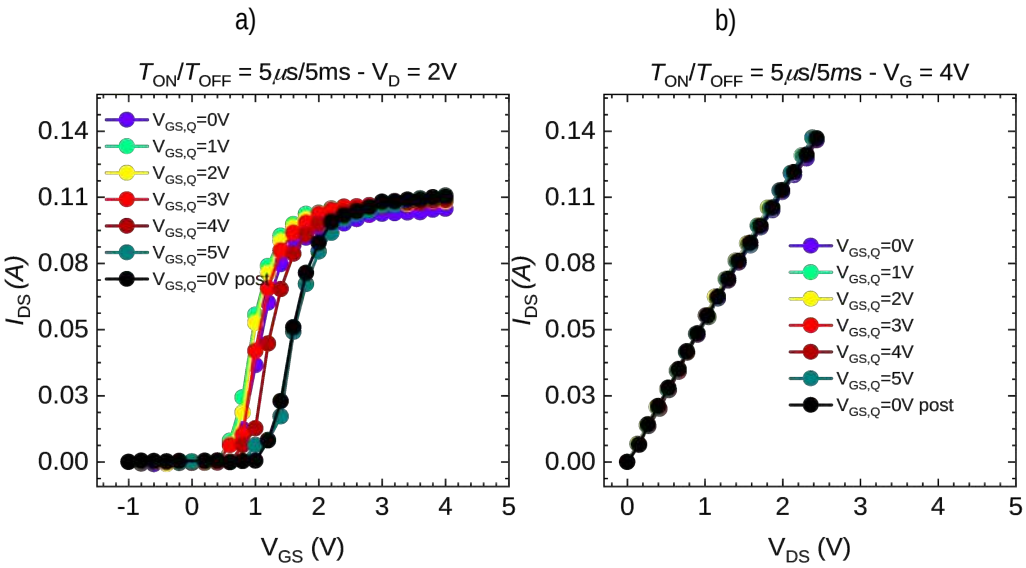


Figure 32: a) I_D-V_{GS} at V_{DS}=2V from double pulse measurements and b) I_{DS}-V_{DS} performed for $V_{GS,Q}$=0,1,2,3,4,5V

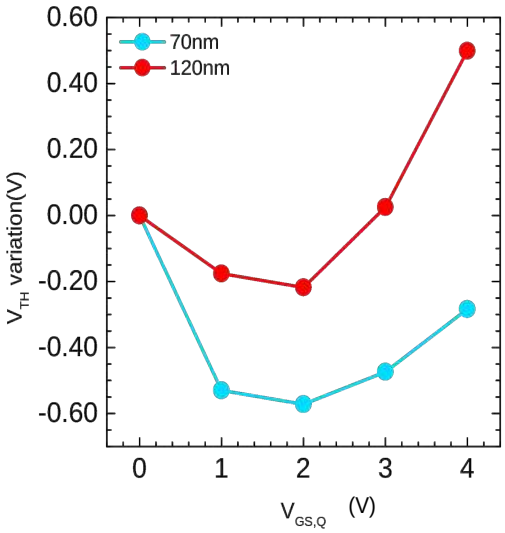


Figure 33: V_{th} variations in double pulse measurements of device 120nm and 70nm channel width

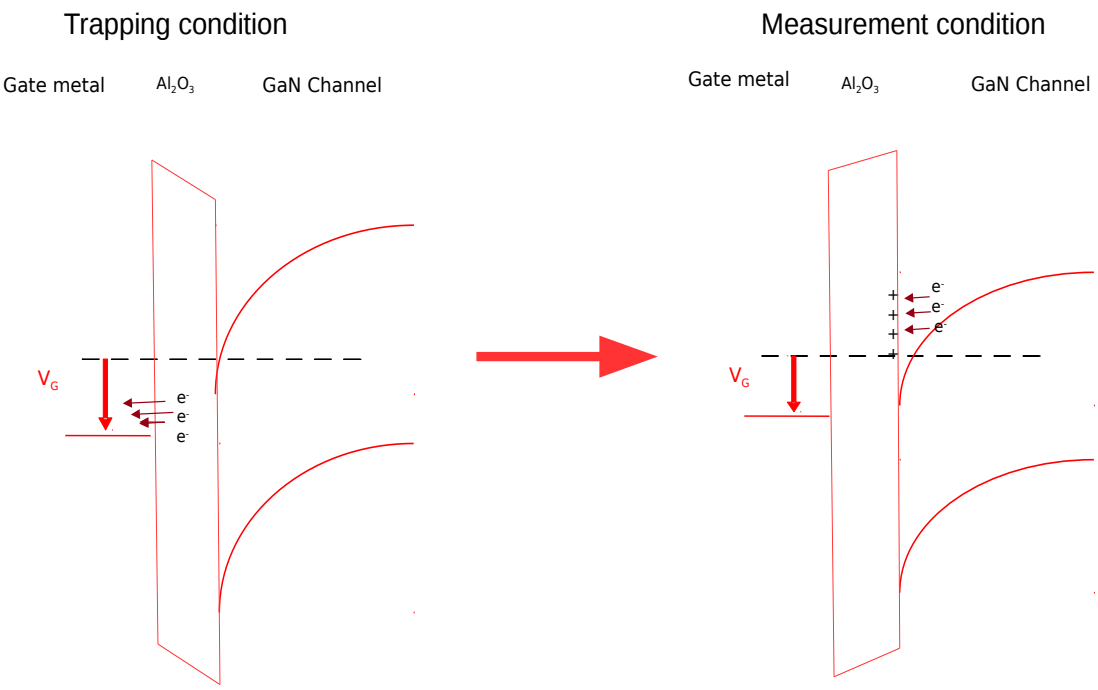


Figure 34: Electrons trapped in oxide are detrapped for positive V_G and pass in gate metal. The resulting positive charge attracts electrons from channel

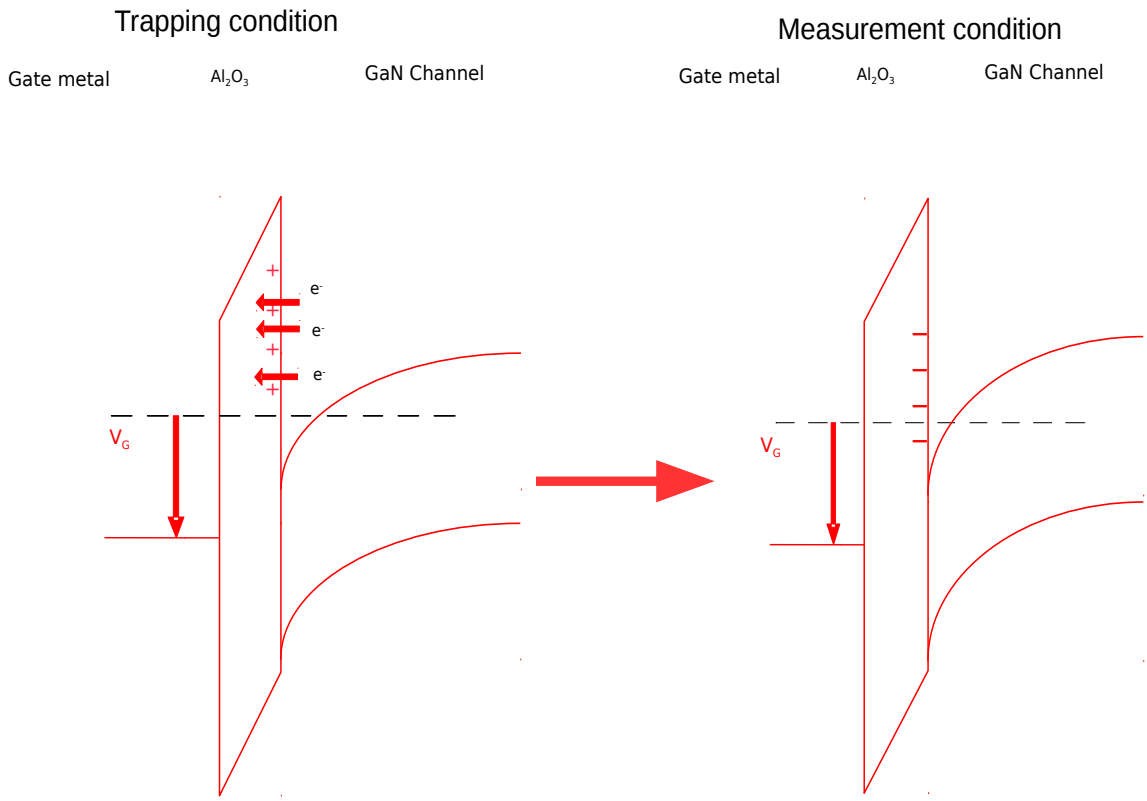


Figure 35: Electrons are injected in the oxide for more positive V_G bias. Oxide has a net negative charge.

6. Analysis of the time-dependence of the trapping processes

In order to evaluate the insulator-related trapping processes responsible of the threshold voltage instability in vertical GaN fin FETs we tested the devices at different gate bias, monitoring the threshold voltage transients. The standard stress-recovery experiments to evaluate the impact of gate bias in the transfer characteristics consist in constant voltage stress with fast $I_D V_{GS}$ performed at defined steps during the stress/recovery phase. With this kind of measurements we are able to monitor the changes in V_{th} which occur for t>1s.
One approach that has been recently developed within the microelectronic research group at the university of Padova consists in monitoring the threshold voltage drifts under gate bias stress by applying consecutive stress and varying the period of stress from 10 μs to 100 s. At the end of every stress period, the device under test is biased at a specific bias point ($V_{G,MEAS}$, $V_{D,MEAS}$) in the linear region of the transfer characteristic in order to evaluate thresholds voltage shift. The threshold voltage transient could be measured after a bias condition ($V_{G,BIAS}$, $V_{D,BIAS}$) that can induce trapping or in order to evaluate the recovery (with $V_{G,BIAS}$, $V_{D,BIAS}$ at 0 V).

With this new technique we were able to study the characteristic times of trapping and detrapping under positive gate bias.

6.1 Measurement setup

In V_{th} transients measurements the gate is kept under positive voltage bias ($V_{G,BIAS}$) for a period Δt and I_D-V_{GS} measurements are made in 10 μs at the end of each period by sweeping the gate from -1 to 5 V with drain voltage at 2V. The test is repeated consecutively at different $V_{G,BIAS}$ by increasing the period of stress from 10μs to 100s. For each value of $V_{G,BIAS}$ a recovery phase is made with $V_{G,BIAS} = 0$V.
In this setup it is also possible to apply a constant voltage ($V_{G,FILL}$) and evaluate only the V_{th} variations in the recovery phase.
As shown in fig. 37 the set-up is made of:

- an oscilloscope (Tektronic TD654C),

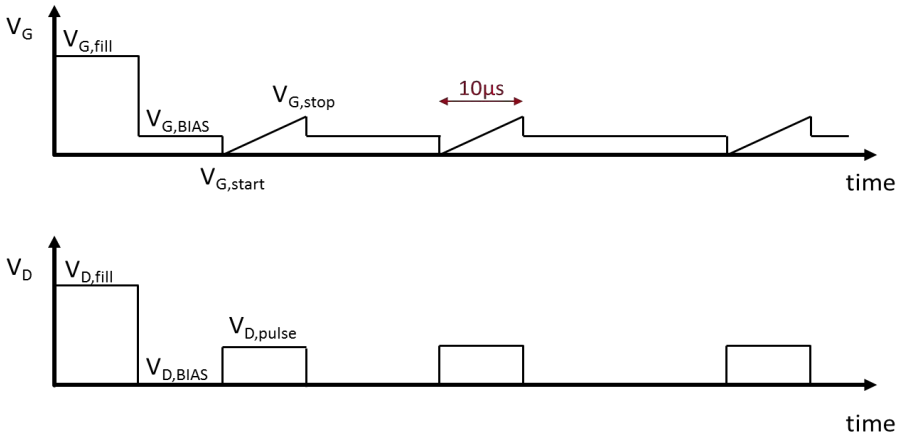


Figure 36: Waveform of V_{th} transients

- a waveform generator (AWG) (Agilent 33250A),
- a current probe.

In order to evaluate the timings related to the mechanisms responsible of the threshold voltage shift and to further study the phenomena we tested devices with different channel widths at different gate voltages. We carried out a first characterization considering a phase of stress and a phase of recovery (with $V_{G,FILL}$ $V_{D,FILL}$ equal to 0 V) at different temperatures. Then, we evaluated the recovery phase at room temperature (using $V_{G,FILL}$ as trapping condition) in dark and under UV-light.

6.2 Results and conclusions

V_{th} transients were performed for devices of 220nm and 120nm channel widths (fig. 38 and fig. 39).

The measurements consist of two consecutive phases:

1. *stress phase*: is the first phase, the $V_{G,BIAS}$ is applied as in the depicted scheme fig. 36,
2. *recovery phase*: is the second phase, $V_{G,BIAS}$ is kept zero and it is possible to study a possible recovery of parameters and its characteristic times.

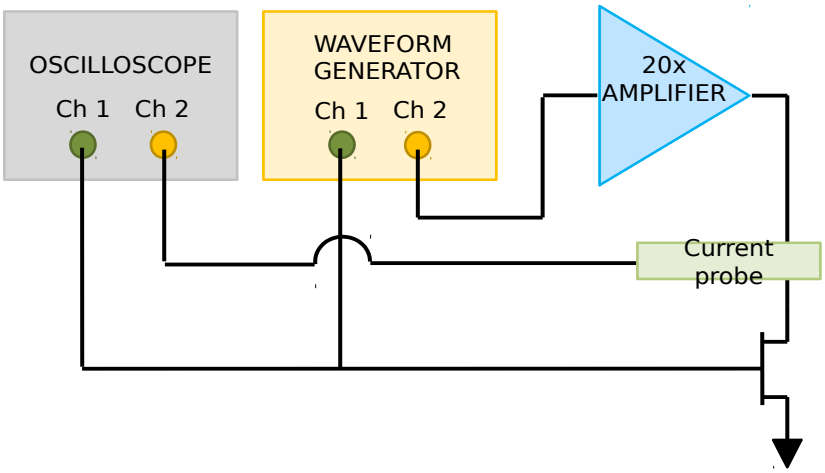


Figure 37: Set-up of V_{th} transients measurements

The fig. 38 and fig. 39 reports the V_{th} variation performed at 30°C for $V_{G,BIAS}$= 0V,1V,2V,3V,4V and the recovery phase for devices 120nm and 220nm channel widths.
In conclusions V_{th} measurements confirm DC and double pulse results and hypothesis.
In particular in the stress phase:

1. in the measurement performed at $V_{G,BIAS}$=0V, the initial threshold voltage for the device with 120 nm of channel width is more positive than that of the device of 220nm channel width as seen in DC measurements,

2. once $V_{G,BIAS}$=1,2V of gate voltage is applied, a negative shift of the threshold voltage is observed. The shift is higher for 120 nm device.
   This is a consequence of the net positive charge at oxide/GaN interface due to electrons shift in gate metal.

3. For $V_{G,BIAS}\geq$3V a positive shift of the threshold voltage is observed after 0.1 s of stress.
   This is related to the second assumed phenomenon: the injection of electrons inside the oxide.

In the recovery phase:

1. for low gate voltage of stress the recovery is fast and complete. This means that the first assumed phenomenon is reversible. So electrons are attracted toward the oxide/GaN interface but not trapped.

2. For $V_{G,BIAS}$≥3V no recovery is observed in 100s, confirming double pulsed measurements. The trapping inside the oxide (second phenomenon) is not reversible in short periods of time.

The obtained results show that the measurements at $V_{G,BIAS}$=1,2V are characterized by a negative shift of V_{th} but around 10^{-2}s or 10^{-1}s these curves have a change of tendency toward a positive shift. The positive shift for log time of stress is probably related to the measured $I_D V_{GS}$ performed by sweeping the gate from 0 to 5 V. The gate biased at 5V induces electron trapping in the oxide and the consequent positive shift of the threshold voltage for long times of stress.
From $V_{G,BIAS}$=3V, the recovery is not complete. So the following V_{th} transient measurements will begin with higher V_{th} values.

In conclusion we can say that Direct Current measurements and Double Pulsed measurements hypothesis are confirmed by V_{th} transients measurements.

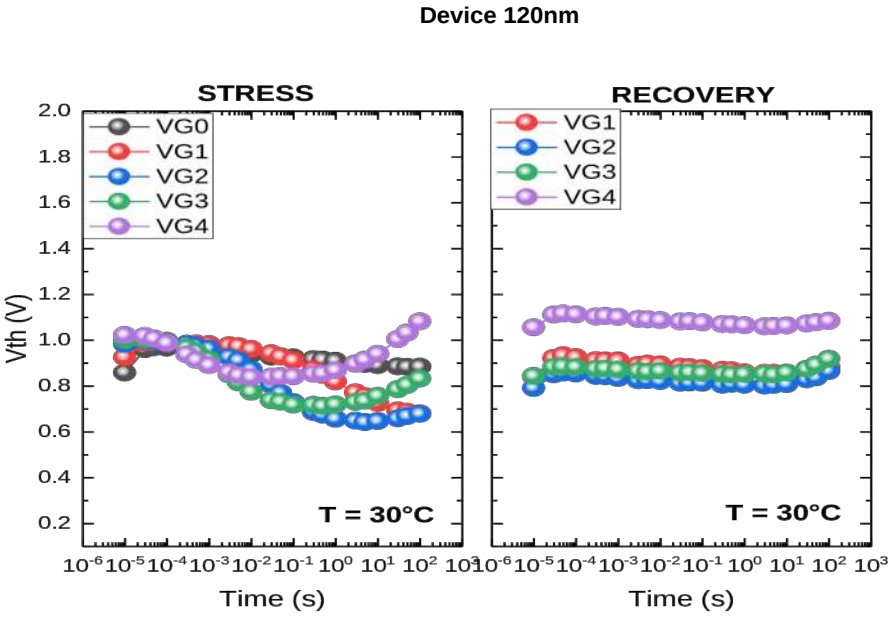


Figure 38: V_{th} transients of 120nm device

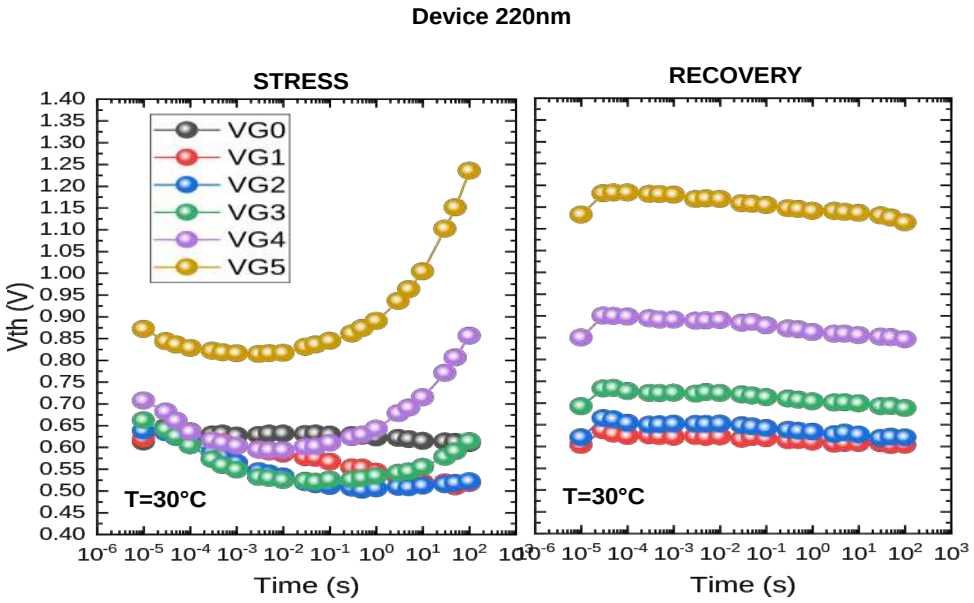


Figure 39: V_{th} transients of 220nm device

6.3 Temperature dependence of the trapping-detrapping processes

Further measurements of V_{th} transients were made at different temperatures 30°C, 50°C, 70°C, 90°C in order to study the effect of the temperature on the degradation/recovery kinetics.

The results (summarized in fig. 40 for 120nm and fig. 41 for 220nm devices) indicate that the temperature does not significantly affect the trapping kinetics. The behaviour is the same of V_{th} transients performed at 30°C: at low ($V_{G,BIAS}$=1,2V) a negative shift is shown but for higher ($V_{G,BIAS}$=3,4V) there is a change of tendency toward an increment of V_{th}.

6.4. V_{th} transients with UV-light

In this section we report the analysis of the recovery phase performed in dark and under UV illumination λ=365nm (E = hc =3.4eV).

The setup is modified in order to have and automatic and immediate recovery after the stress phase.

In these measurements the gate bias voltage is obtained applying $V_{G,FILL}$=1,2,3,4V for 100s and $V_{G,BIAS}$=0V as reported in fig. 42.
Recovery is performed in dark condition and in UV-light condition using a LED (light emitting diode) as light source.

In fig. 43 a) and b) the threshold voltage variation in dark and under UV illumination are reported.
With UV light exposure there is a strong recovery also for $V_{G,BIAS}$ =3V and 4V which was absent in dark V_{th} transients. V_{th} also lowers far below the initial V_{th} value.
We can make this hypothesis: trapping happens at a specific energy level which corresponds to a energy below 3.4 eV when the device is lightened by the LED the energy given from UV-light (3.4 eV) helps electrons to be detrapped. Then electrons can proceed towards the GaN layer through hopping[42][43], thus being collected at the semiconductor side and contribute to the conductive channel and the turn ON.
Another possibility is that when the device is exposed to UV light in OFF-condition (0V at the gate), the UV-light exposure could lead to the creation of electron-hole pairs inside the GaN since the bandgap of GaN is equal to the UV light energy.
Thanks to the slight band bending at 0V the holes can be accumulated at the GaN/Al_2O_3 interface and can compensate part of the negative charge in the oxide due to trapped electrons. In conclusion, the UV-exposure induces a negative shift of the threshold voltage by increasing the conductive electrons either by electron detrapping from oxide, either by generation of carriers fig. (44) in good agreement to previous reports on different MOS structures [44][45] (fig. 44).

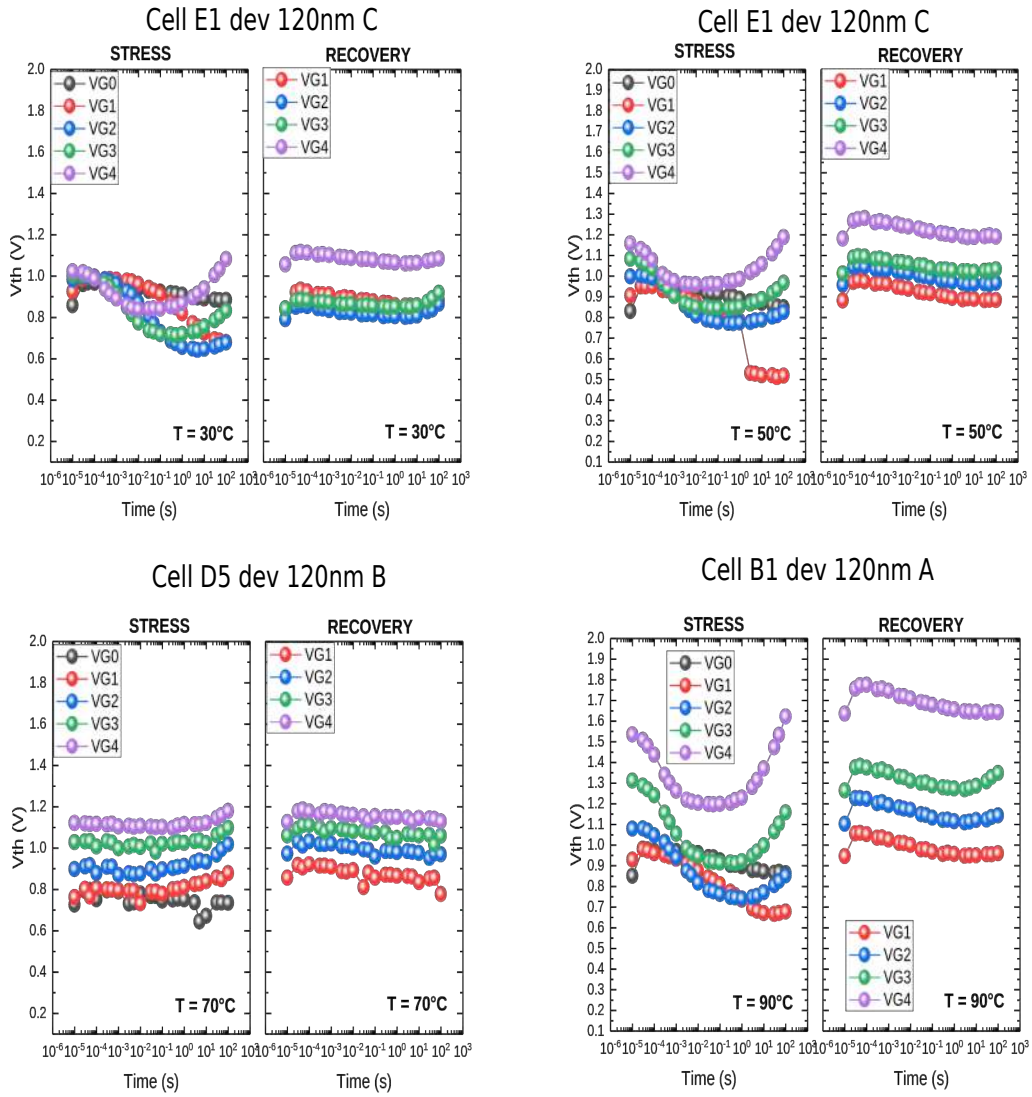


Figure 40: V_{th} transients and recovery phase of 120nm device for $30°C, 50°C, 70°C, 90°C$

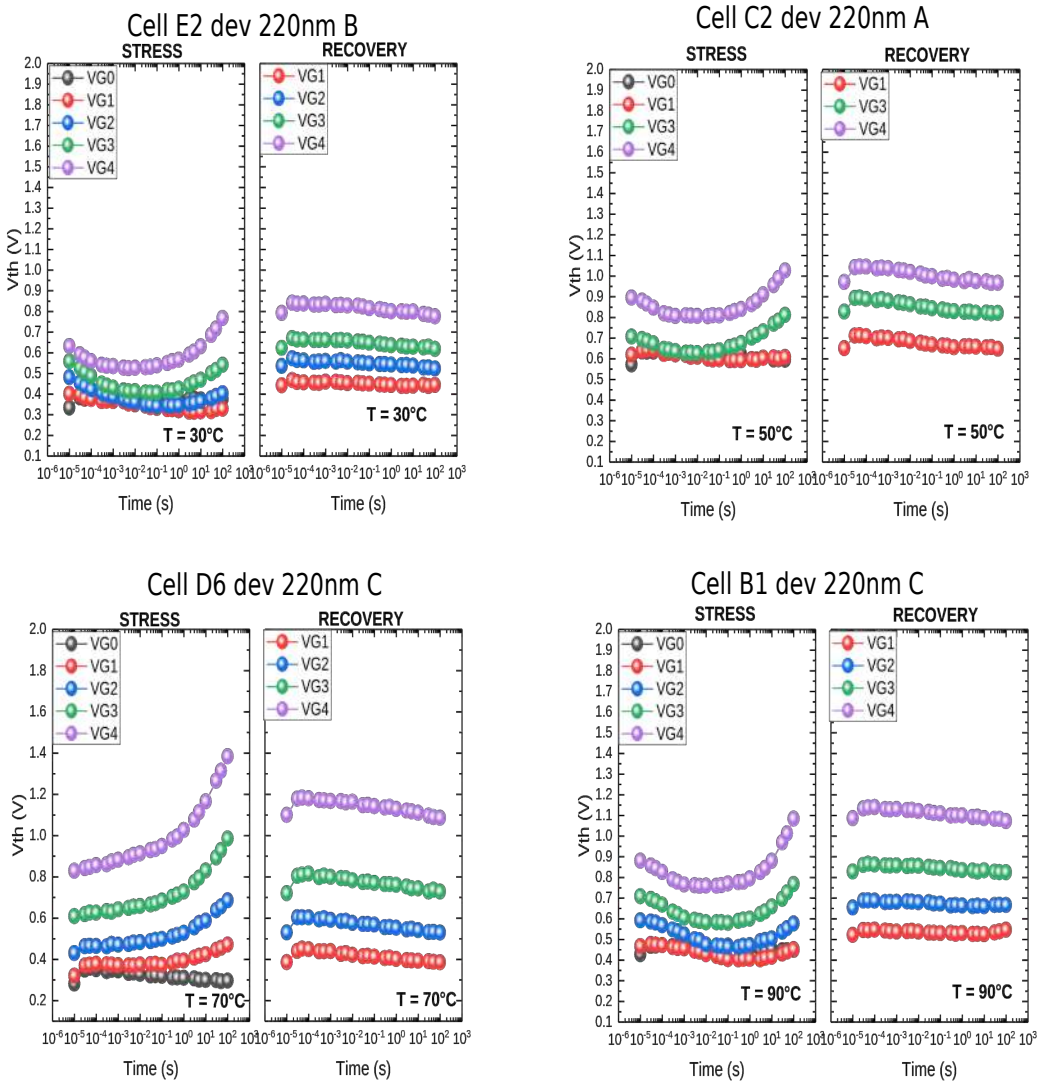


Figure 41: V_{th} transients and recovery phase of 220nm device for 30°C, 50°C, 70°C, 90°C

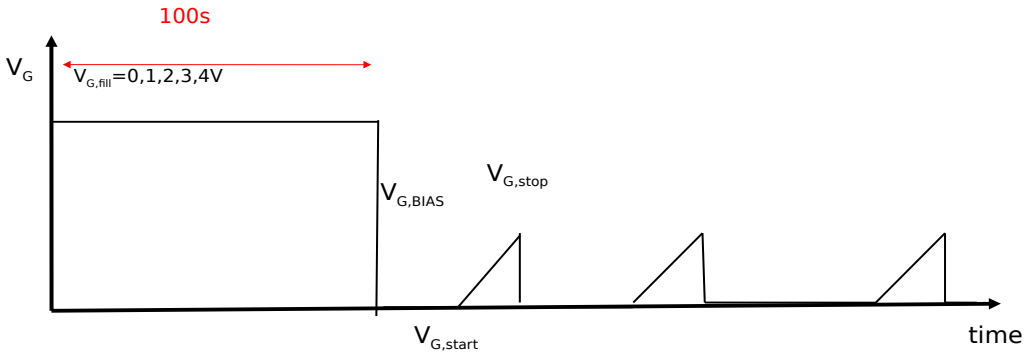


Figure 42: Waveform of V_{th} transients measurements

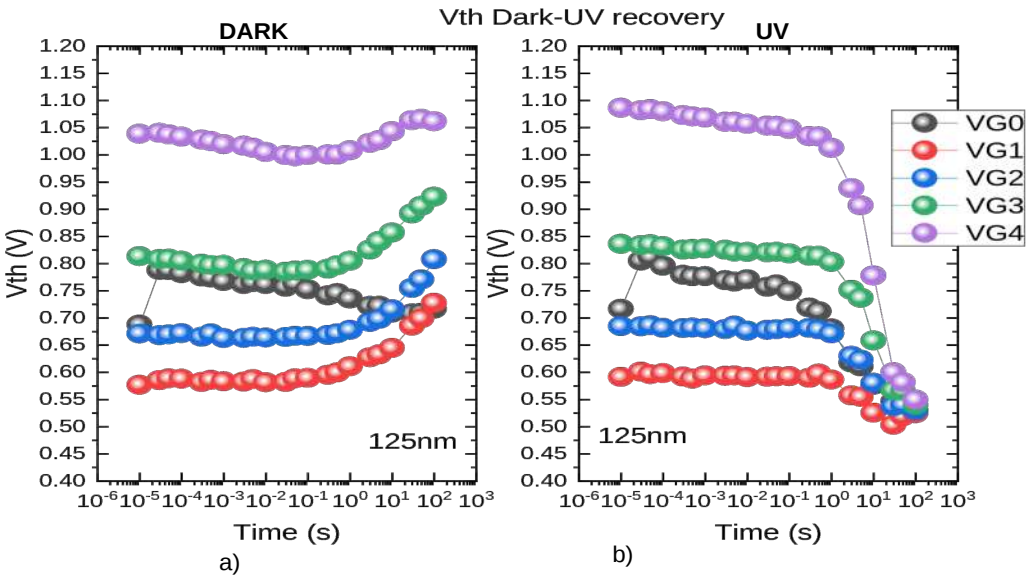


Figure 43: a) Recovery phase of V_{th} transients in dark condition, b) Recovery phase of V_{th} transients in UV-light

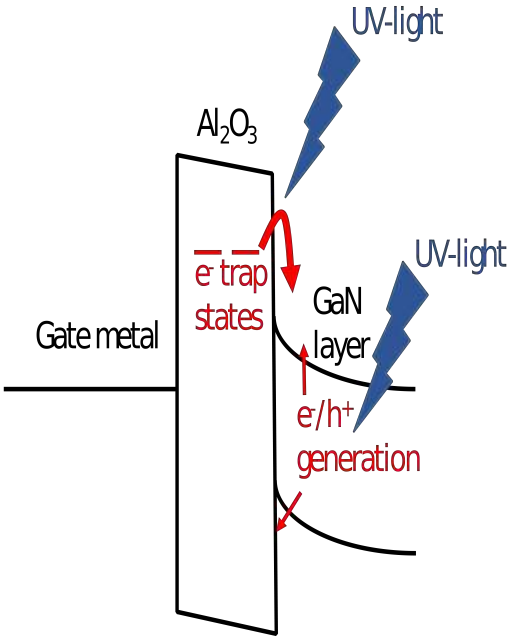


Figure 44: Device exposed to UV light

7. Simulation

Generally, simulation activity can be done in order to reproduce the real behaviour of either a device or a circuit. With simulations, we can understand how the device works, we can reproduce or predict a trend, without using real devices. In the industry and research fields, simulations are used together with device characterization to improve the comprehension of the physical phenomena and reduce the fabrication costs.

In this work, we used a microelectronics simulator Sentaurus TCAD, provided by Synopsys, for simulate the fabrication, operation and reliability of semiconductor devices. Sentaurus simulator is composed by different tools to simulate different steps of the process flow and device operations. In our case we used the Sentaurus structure editor to edit the 2D structure of the GaN based vertical fin FET with different channel widths; the mesh generator to create an array of point in which the device is divided in order to capture as much as possible the variations in physics features using a finer mesh in areas with steep gradient. With Senturus device tool we were able to simulate electrical characteristics of the device. This tool contains a comprehensive set of physics models for different semiconductor materials like GaN.

In order to fit the tested device we introduced trap states in the GaN layer. Depending on the Fermi level, carbon can be incorporated in the GaN during the growth processing either in nitrogen substitutional position (C_N), behaving as acceptor state, in gallium substitute (C_{Ga}), or in interstitial position (C_i), behaving as donor state. In our case, a good fit of experimental data is achieved by introducing a carbon related acceptor state.
We took into account two possible scenarios. In one study of GaN reported by Armstrong et al.[46], a prominent deep level state at E_c-3.28 eV was identified with carbon impurities, ascribed to C_N. Another possibility proposed by Lyons et al.[47] suggests that carbon in nitrogen substitutional position C_N could behave as deep acceptor and not a shallow acceptor with the transition level at E_V+0.9eV.

In order to take into account the two scenarios we simulated with an acceptor state in two different levels:
E_{CN}= 0.2 eV from the Valence Band
E_{CN}= 0.8 eV from the Valence Band

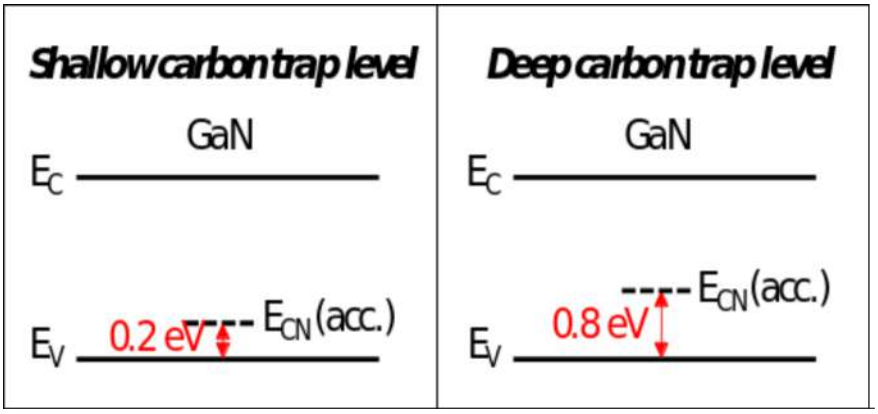


Figure 45: Possible trapping energy level of Carbon

7.1 Sentaurus devices physical models

In all semiconductor devices, mobile charges (electrons and holes) and immobile charges (ionized dopants or traps) play a central role. The charges determine the electrostatic potential and are themselves affected by the electrostatic potential. Therefore, each electrical device simulation at the very least must compute the electrostatic potential.

$$\vec{D} = \epsilon_0 \vec{E} + \vec{P} \tag{21}$$

$\vec{D}$ is the *Displacement field* and its sources are free charges, ϵ is the electrical permittivity, $\vec{P}$ is the ferroelectric polarization and $\vec{E}$ is the total electric field and it is the gradient of electrostatic ϕ potential $\vec{E} = -\vec{\nabla}\phi$. Using Gauss theorem:

$$\vec{\nabla} \cdot (\epsilon \vec{E}) = \rho_{free} \tag{22}$$

$$\vec{\nabla} \cdot \vec{P} = \rho_{polarization} \tag{23}$$

$$\vec{\nabla} \cdot (\epsilon_0 \vec{\nabla} \phi + \vec{P}) = -q(p - n + N_D - N_A) - \rho_{trap} \tag{24}$$

where:

- q is the elementary electronic charge,
- n and p are the electron and hole densities,
- N_D is the concentration of ionized donors,
- N_A is the concentration of ionized acceptors,
- ρ_{trap} is the charge density contributed by traps and fixed charges.

As well as the electrostatic potential the simulator allows to draw the charge density distribution.

Even if electrons and holes are fermions for low densities values it is possible to use Boltzmann statistics.
In Boltzmann statistic the distribution function is:

$$n = N_C exp(\frac{E_{F,n} - E_C}{K_B T}) \tag{25}$$

$$p = N_V exp(\frac{E_V - E_{F,p}}{K_B T}) \tag{26}$$

where:

- N_C and N_V are the density of states,
- $E_{F,n} = -q\Phi_n$, $E_{F,n} = -q\Phi_p$ are the quasi-Fermi energies for electrons and holes,
- Φ_n, Φ_p are electrons and holes quasi-Fermi potentials,
- E_C E_V are conduction and valence band edges, defined as:

$$E_C = -\chi - q(\phi - \phi_{ref}) \tag{27}$$

$$E_V = -\chi - E_{g,eff} - q(\phi - \phi_{ref}) \tag{28}$$

- χ electron affinity,

- $E_{g,eff}$ effective band gap,
- ϕ_{ref} constant reference potential.

But for higher electron densities the Fermi statistic is used:

$$n = N_C F_{1/2} exp(\frac{E_{F,n} - E_C}{K_B T}) \tag{29}$$

$$p = N_V F_{1/2} exp(\frac{E_V - E_{F,p}}{K_B T}) \tag{30}$$

where $F_{1/2}$ is the Fermi integral of order 1/2.

Sentaurus Device supports several carrier transport models for semiconductors. All these models are based on the continuity equations:

$$\vec{\nabla} \cdot \vec{J_n} = qR_{net,n} + q\frac{\partial n}{\partial t} \tag{31}$$

$$\vec{\nabla} \cdot \vec{J_p} = qR_{net,p} + q\frac{\partial p}{\partial t} \tag{32}$$

1. $R_{net,n}$ and $R_{net,p}$ are the electron and hole net recombination rate,
2. n and p are the electron and hole densities,
3. $\vec{J_n}$ is the electron current density,
4. $\vec{J_p}$ is the hole current density.

But the difference between models is the definition of $\vec{J_n}$ and $\vec{J_p}$.

The default carrier transport model is *Drift-Diffusion Model*.
In this model the current electron and hole densities are defined as:

$$\vec{J_n} = \mu_n(\nabla E_C - 1.5K_B T \nabla Ln(m_n^*)) + D_n(\nabla n - n\nabla Ln(\gamma_n)) \tag{33}$$

$$\vec{J_p} = \mu_p(\nabla E_V - 1.5K_B T \nabla Ln(m_p^*)) + D_p(\nabla p - p\nabla Ln(\gamma_p)) \tag{34}$$

where:

- m_p^* and m_n^* are the effective mass of holes and electrons,

- the diffusivities D_n and D_p are given through the mobilities by the Einstein relations, $D_n = K_B T \mu_n$ and $D_p = K_B T \mu_p$,
- $\gamma_n = \gamma_p = 1$ in Boltzmann model and $\gamma_n = \frac{n}{N_C} exp(\frac{E_C - E_{F,n}}{K_B T})$, $\gamma_p = \frac{p}{N_V} exp(\frac{E_{F,p} - E_V}{K_B T})$ in Fermi model.

The first term of equations (33) and (34) takes into account the contribution due to the spatial variations of the electrostatic potential, the other terms account the contribution due to the gradient of concentration, and the spatial variation of the effective masses m_n^* and m_p^*.

Another model takes into account the temperature effects:
ThermodynamicModel
In this model the equations (33) (34) are generalized including gradient of temperature.
The last physical model supported by Sentaurus is the *Hydrodynamic Model*.

$R_{net,n}$ and $R_{net,p}$ is the result of generation-recombination processes. These are processes that exchange carriers between the conduction band and the valence band.
Sentaurus supports different generation-recombination models.
The first is the *Shockley Read Hall Recombination (SRH)*. In this process there is the presence of a deep level E_T in which the electron and the hole recombine.

The SRH rate of recombination is given by:

$$R^{SRH} = \frac{n \cdot p - n_i^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{35}$$

where:

- n_i is the intrinsic carrier concentration at equilibrium (number of holes is equal to number of electrons),
- τ_p and τ_n are the electrons and holes lifetimes. They depend on doping and temperature.
- p_1 and n_1 are defined as:

$$n_1 = n_i exp(\frac{E_{trap}}{K_B T}) \tag{36}$$

$$p_1 = p_i exp(\frac{-E_{trap}}{K_B T}) \tag{37}$$

E_{trap} is the difference between the trap level and the intrinsic level.

Some other supported generation-recombination models are:

- Trap-assisted Auger Recombination,
- Surface SRH Recombination,
- Coupled Defect Level (CDL) Recombination,
- Radiative Recombination.

7.2 Commands describing the structure of the device

The first command file allows to define the structure of the device. The file can be divided in four sections.

In the first section it is possible to create the geometrical forms of the device. The rectangular forms are drawn by defining the coordinates of the lowest left vertex and the highest right vertex. In every rectangle it is possible to define the material of the region. The characteristics of the materials are default parameters.
Six rectangles are defined: the GaN layer, GaN cap, two Oxide rectangles and two Molybdenum rectangles for the gate right e left.
Through the superposition of these six rectangles the structure of thr device is formed.
For example the first device simulated is 220nm channel. The code is reported below and the structure is shown in fig. 46.

```
(sdegeo:create-rectangle (position 0 0 0) (position 1.62 8 0)
"GaN" "GaNLayer")
(sdegeo:create-rectangle (position 0 6.5 0) (position 0.7 8 0)
"Oxide" "OxideLeft")
(sdegeo:create-rectangle (position 0.92 6.5 0) (position 1.62 8 0)
"Oxide" "OxideRight")
(sdegeo:create-rectangle (position 0 6.515 0) (position 0.685 8 0)
"Molybdenum" "GateLeft")
(sdegeo:create-rectangle (position 0.935 6.515 0) (position 1.62 8 0)
"Molybdenum" "GateRight")
(sdegeo:create-rectangle (position 0.7 8 0) (position 0.92 8.3 0)
"GaN" "GaNCap")
```

In the second section it is possible to define the contacts: gate left, gate right, source and drain. The position of the contacts are set as shown in fig. 47.

```
(sdegeo:define-contact-set "Source" 4 (color:rgb 1 0 0 ) "")
(sdegeo:define-contact-set "Drain" 4 (color:rgb 1 0 0 ) "")
(sdegeo:define-contact-set "GateLeft" 4 (color:rgb 1 0 0 ) "")
(sdegeo:define-contact-set "GateRight" 4 (color:rgb 1 0 0 ) "")

(sdegeo:set-current-contact-set "Source")
(sdegeo:set-contact-edges (list (car (find-edge-id (position 0.81 8.3 0)))) "Source")
```

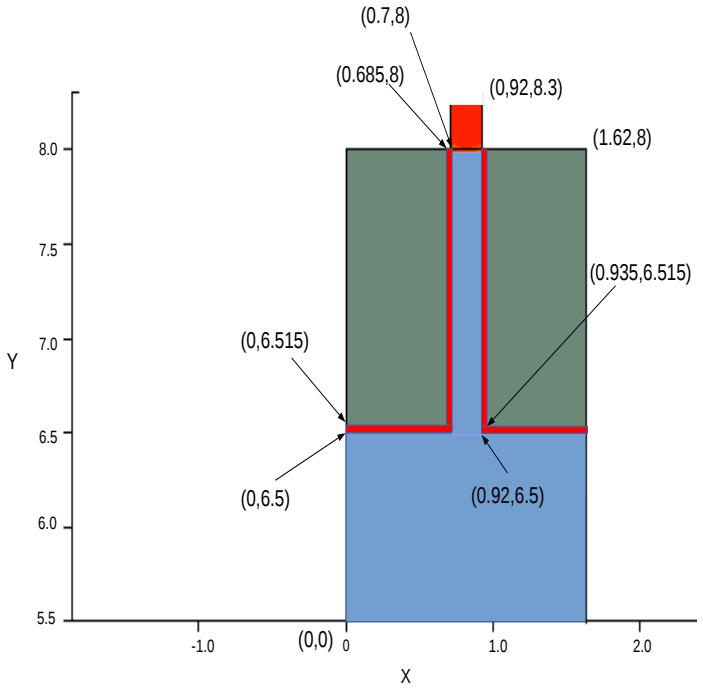


Figure 46: Structure of 220nm device

(sdegeo:set-current-contact-set "Drain")
(sdegeo:set-contact-edges (list (car (find-edge-id (position 0.81 0 0)))) "Drain")

(sdegeo:set-current-contact-set "GateLeft")
(sdegeo:set-contact-edges (list (car (find-edge-id (position 0.3425 6.515 0)))
(car (find-edge-id (position 0.685 7.2575 0)))) "GateLeft")

(sdegeo:set-current-contact-set "GateRight")
(sdegeo:set-contact-edges (list (car (find-edge-id (position 0.935 7.2575 0)))
(car (find-edge-id (position 1.2775 6.515 0)))) "GateRight")

In the third part there is the definition of the doping. Two doping regions have been defined with a constant doping profile. The regions are both n-doped: the GaN Layer $2 \cdot 10^{16}$ cm^{-3} and the GaN Cap $5 \cdot 10^{17}$ cm^{-3} fig. (48).

(sdedr:define-constant-profile "ConstantProfileDefinitionTotal1"
"NDopantConcentration" 2e16)
(sdedr:define-constant-profile-region "ConstantProfilePlacementTotal1"
"ConstantProfileDefinitionTotal1" "GaNLayer" 0 "LocalReplace")
(sdedr:define-constant-profile "ConstantProfileDefinitionTotal2"
"NDopantConcentration" 5e+17)

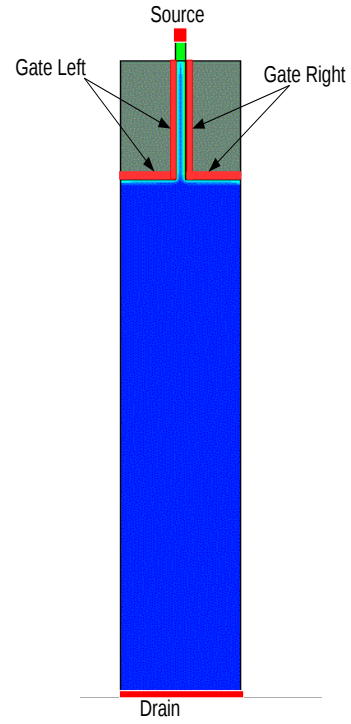


Figure 47: Contacts of device

(sdedr:define-constant-profile-region "ConstantProfilePlacementTotal2" "ConstantProfileDefinitionTotal2" "GaNCap" 0 "LocalReplace")

In the fourth section we define the mesh, which is a lattice formed by the spatial calculation points.
It is possible to define the zone containing the mesh and the size of the mesh. The complete mesh is pictured in fig. 49. There are seven meshes with different sizes:

- the largest mesh is extended all over the device,
- a second mesh is in the center of the channel of the device,
- two meshes symmetrically located along the interfaces Oxide/GaN,
- two meshes symmetrically located at the two angles between the channel and the substrate.

Below it is reported the instructions of the largest mesh which is extended all over the device.

(sdedr:define-refeval-window "RefEvalWinGlobal" "Rectangle" (position 0 0 0) (position 1.62 8.3 0))
(sdedr:define-refinement-size "RefinementDefinitionGlobal" 0.15 0.7 0.015 0.07)

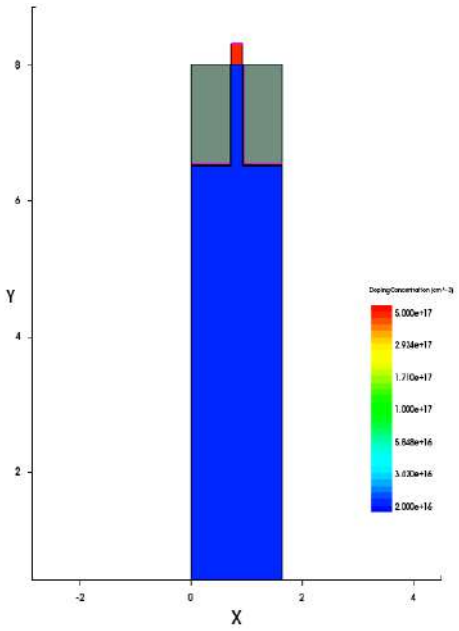


Figure 48: Doping of the device

7.3 Commands for the simulation of the behaviour of the device

In the second command file in the first section it is possible to define the simulation starting voltage of Gate, Source and Drain and the Schottky workfunction of the metal (molybdenum).

Electrode
Name="GateLeft" Voltage= 0 Schottky Workfunction= 4.6
Name="GateRight" Voltage= 0 Schottky Workfunction= 4.6
Name="Source" Voltage= 0
Name="Drain" Voltage= 0

In second section *Physics* there is the choice of the physical model.
The Drift Diffusion Model is the default model, the Thermodynamic Model is activated through the word *Thermodynamic* and the Hydrodynamic Model through the word *Hydrodynamic*.
The model used in these simulations is The Drift Diffusion Model.
Using the word *Fermi* the Fermi model is used otherwise the default model is the Boltzmann model.
In the function *Recombination(SRH)* defins the model used for recombination:

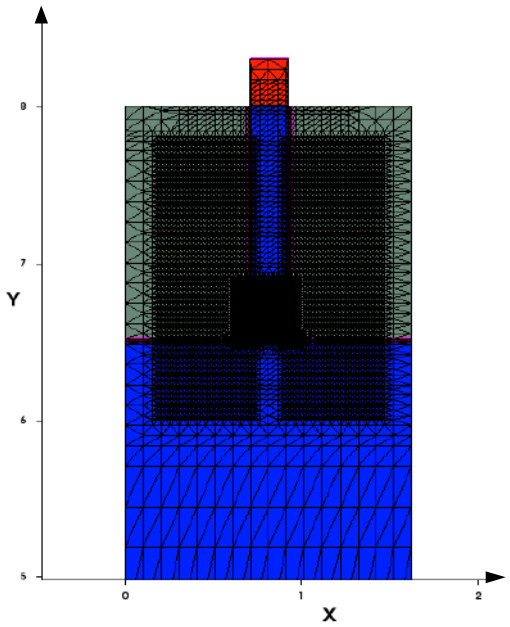


Figure 49: Mesh of the device

the Shockley Read Hall Recombination.
Another parameter present in *Physics* section is *AreaFactor*. The simulated structure is a simplified version of the real one in two dimensions. In the simulations, the current density is taken considering the length in the third dimension as 1μm. In order to fit the real device which is a complex structure in 3D with 40 ribbons of 60μm-length and 36 ribbons of 140μm-length, we selected a AreaFactor of 4000. This parameter is necessary to fit the I_D-V_{GS} of the real device.

Physics
AreaFactor= 4000
Fermi
Recombination(SRH)

Through Sentaurus we could simulate three types of charge and impurities:

1. a superficial charge between oxide and GaN channel defining its density
   Physics (MaterialInterface="GaN/Oxide")
   (conc=0.8e12)

2. a charge in the oxide defining its density.
   Physics (Material="Oxide")
   (conc=0.8e12)

3. traps which can be donors or acceptors. It is possible to define the traps density and their energy level from the GaN valence band:
   Physics (Material= "GaN")
   Traps ((Acceptor Conc=1.2e16 Level EnergyMid=0.8 fromValBand)

7.4 Results of simulations

The first skip in these simulation is the fit of an experimental curve I_D-V_{GS}.

In the first set of simulations the traps considered has and energy (E_{trap}) of 0.2eV from GaN valenceBand (shallow Carbon trap level).
The device chosen is 220nm channel width. The I_D-V_{GS} is fitted through the following parameters:

- *AreaFactor*=4000,
- traps in GaN bulk region: acceptor type with density of $1.2 \cdot 10^{16}$ cm^{-3} and energy from GaN valence band of E_{trap}=0.2eV,
- positive superficial charge in the interface between Oxide/GaN with density of $0.8 \cdot 10^{12}$ cm^{-2},
- no charge in bulk Oxide.

The charge density has been depicted in false colors through Sentaurus function to show the formation of the channel at V_D=1V for the device 220nm channel width.
For a negative V_{GS} the channel is depleted of electrons (fig. 51), for positive increasing potentials electrons are attracted toward the gate and around V_G=0.8eV the channel is formed (fig. 52 and fig. 53).
In fig. 54 is shown the electron density at different V_{GS}. Around V_{GS}=0V the electron density is negligible and peaked far from the Al_2O_3 interface. In this case, the device is in the OFF-state and the channel is depleted. For low voltages (V_{GS}=0.2,0.4V), the electron density rises at the center of the drift region, but it is still relatively low at the interface. At high gate voltages ($V_{GS} > 0.8$V), the channel is fully formed, and the electron density peaks at the Oxide/GaN interfaces.

The fig 55, 56, 57 report the band diagrams for V_G=-1,0,1V and V_D=1V. For negative potentials or sub-threshold potentials the conduction and valence bands have minimum at the center of the GaN channel layer fig. 55 and fig. 56, from 0.8eV (threshold voltage) the conduction and valence bands have maximum in the center of the GaN channel layer and the conduction band drops below the valence band: the conductive channel is formed fig. 57.

We simulated the tested device by changing the GaN channel width. The fig. 58 reports the $I_D V_{GS}$ at different GaN channel widths: the threshold voltage changes from around 1.2 V for 10nm-width to 0.2 for 500nm-width demonstrating the behaviour hypotized in DC-measurements: V_{th} increases decreasing channel width.

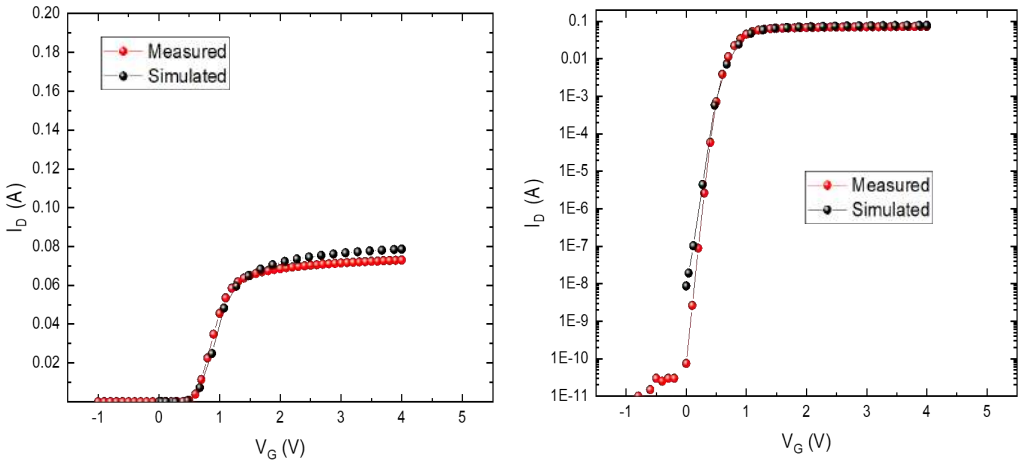


Figure 50: a) Fitted I_D-VGS of 220nm channel width device at V_D=2V in linear scale, b) Fitted I_D-VGS of 220nm channel width device at V_D=2V in logarithmic scale

To explain the differences in threshold voltage for different GaN channel width, we supposed the presence of a parasitic current which is predominant for higher GaN channel width. In order to demonstrate this hypothesis we performed the simulation of the electron density in the GaN channel layer at specific bias condition in different devices that differs for GaN channel width. In Fig. 60 we report the electron density at V_G=0.4V and V_{DS}=1V taken at 6.7μm of the y-axis (Fig. 54), we observe that the device with 280nm GaN channel width shows a maximum electron density of $1.6 \cdot 10^{15}$ cm^{-3} at the center of the GaN channel. This value is at one order of magnitude more than the electron density at the center of the GaN layer of 30nm channel width simulated device at the same conditions. So we demonstrated that the higher channel widths devices have an higher density in the center of the channel which originates the parasitic current.

In the second set of simulations the traps considered has and energy (E_{trap}) of 0.8eV from GaN valenceBand.
The device chosen is 220nm channel width. The I_D-V_{GS} is fitted through the following parameters:

- *AreaFactor*=4000,
- traps in GaN bulk region: acceptor type with density of $1.5 \cdot 10^{16}$ cm^{-3} and energy from GaN valence band of E_{trap}=0.2eV,
- positive superficial charge in the interface between Oxide/GaN with density of $0.8 \cdot 10^{12}$ cm^{-2},
- no charge in bulk Oxide.

In order to further study the trapping behavior observed in the DP measurements, we simulated the $I_D V_{GS}$ with different charge in the oxide investigating the influence of a fixed positive charge at the surface and distributed inside all the oxide region. We demonstrate that the tested device has already a fixed positive charge at GaN/oxide interface probably introduced during the growth processing. When we apply a slight positive gate bias the charge increases (detrapping of electrons towards the gate metal), the effect in the simulation is an increase of the GaN/oxide interface charge (which has a stronger effect to the conductive channel layer than the charge uniformly distributed inside the oxide[48]). The increase of the positive charge at the interface induces a negative shift of the threshold voltage in respect to the simulated initial condition of the real device (which has already a positive oxide charge). This is in good agreement with the experimental data obtained with the DP measurements for low gate voltages. If we lower the interfacial positive charge and we increase the charge uniformly distributed inside the oxide, we observe a positive shift of the threshold voltage: this simulate the condition of trapping when the device is submitted to higher positive gate bias. In this case, electrons are trapped in the GaN/oxide interface and compensate GaN/oxide interface charge. In the Fig. 61 the simulated device without positive charge in the oxide is reported, it has the higher positive threshold voltage demonstrating that the positive oxide charge at the interface moves the threshold voltage toward lower values and it has a stronger effect than the positive charge uniformly distributed inside the oxide.

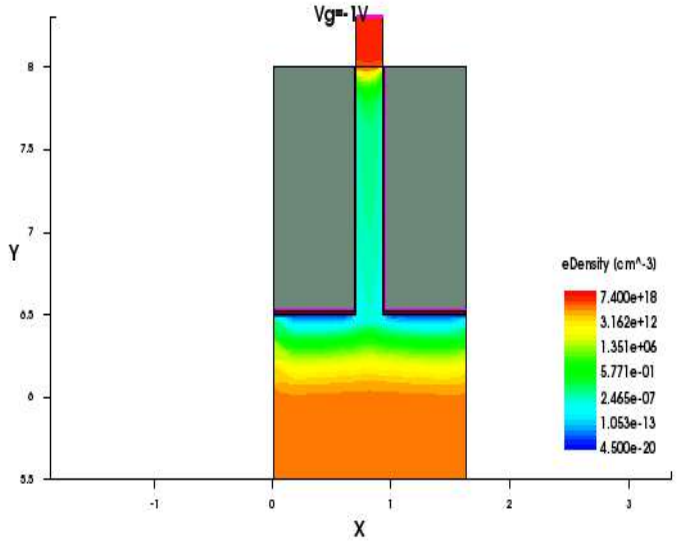


Figure 51: Distribution of electron density at V_{GS}=-1V

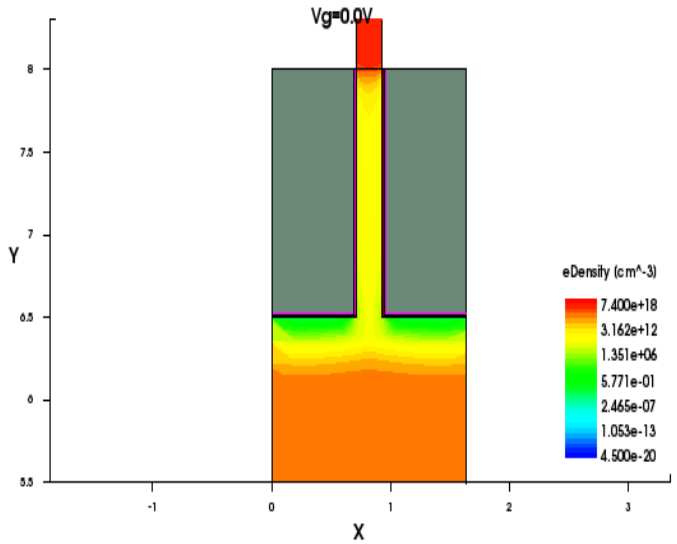


Figure 52: Distribution of electron density at V_{GS}=0V

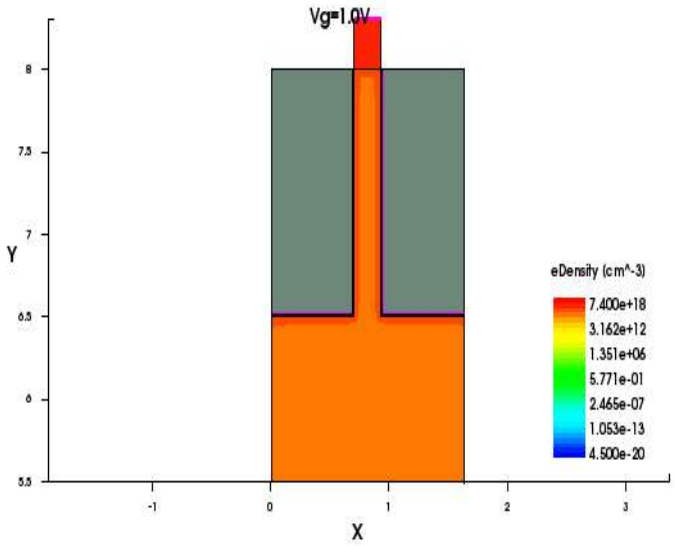


Figure 53: Distribution of electron density at V_{GS}=1V

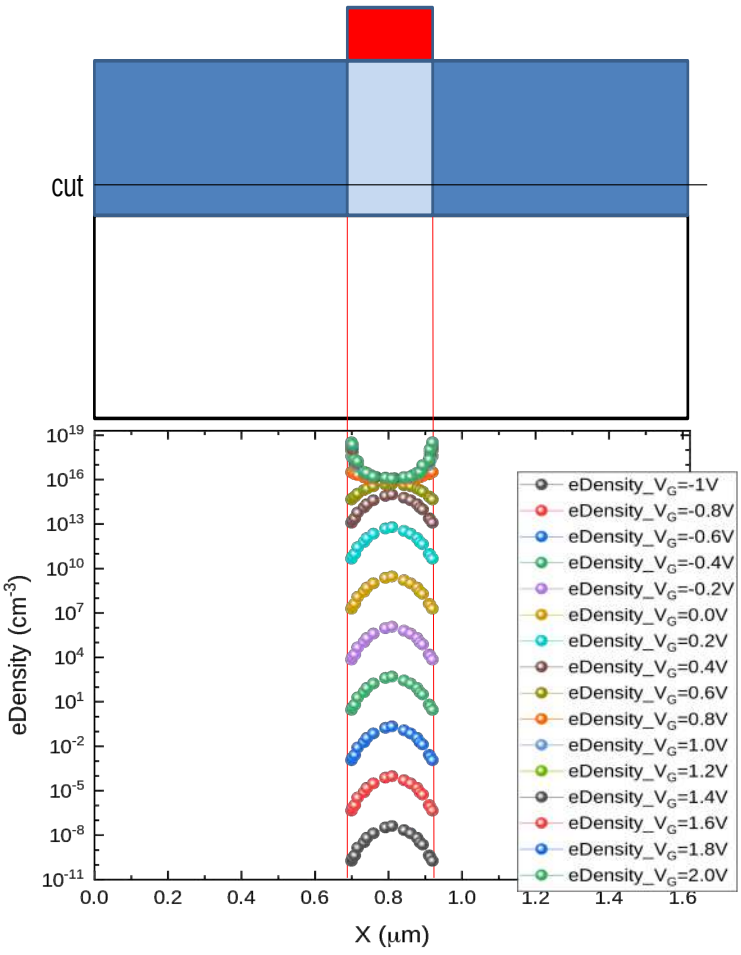


Figure 54: Density of electrons in log scale at different value of V_{GS}

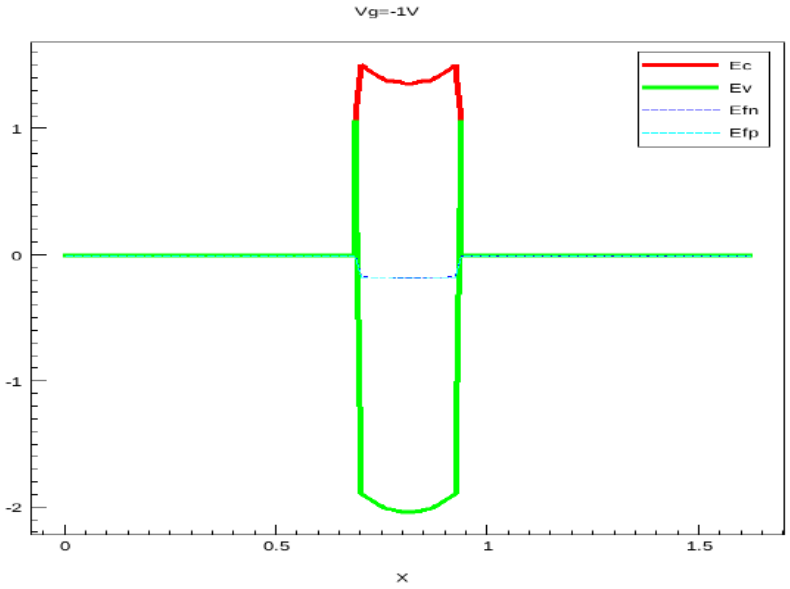


Figure 55: Valence and conduction bands V_{GS}=-1V

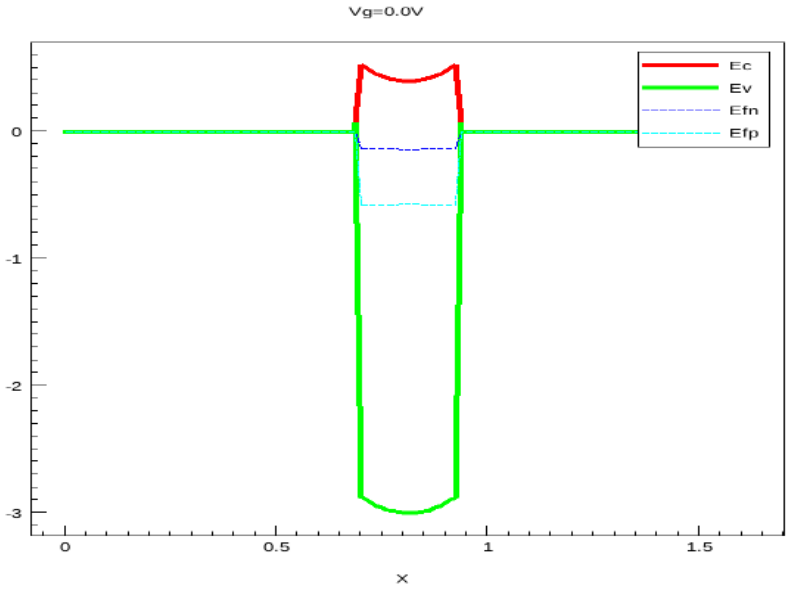


Figure 56: Valence and conduction bands V_{GS}=0V

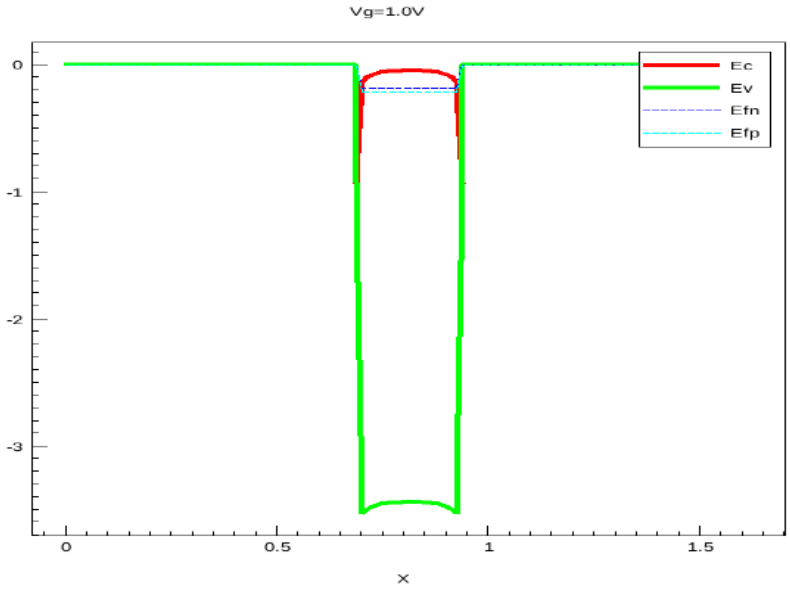


Figure 57: Valence and conduction bands V_{GS}=1V

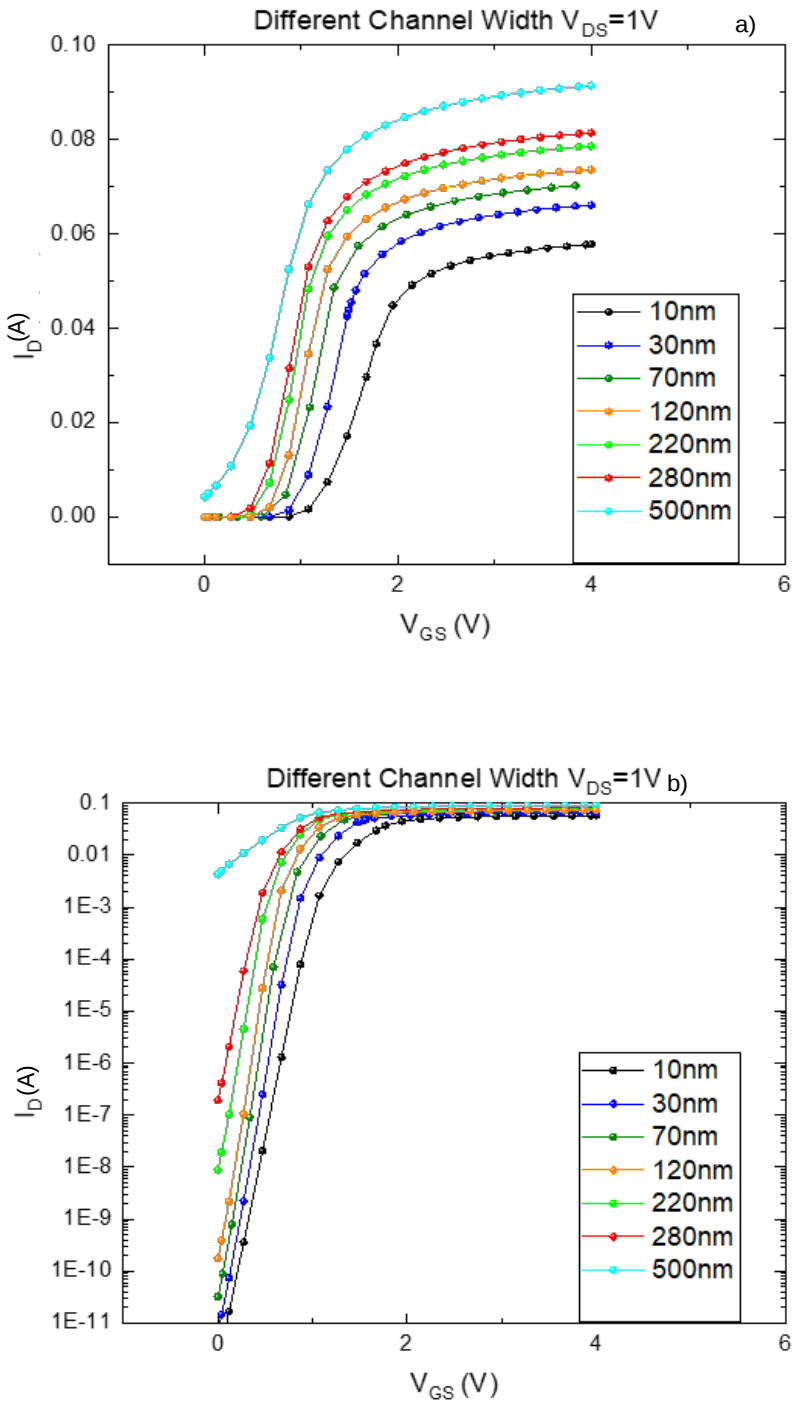


Figure 58: a)Simulated I_D-VGS at different channel widths, b)Simulated I_D-VGS at different channel widths in log-scale

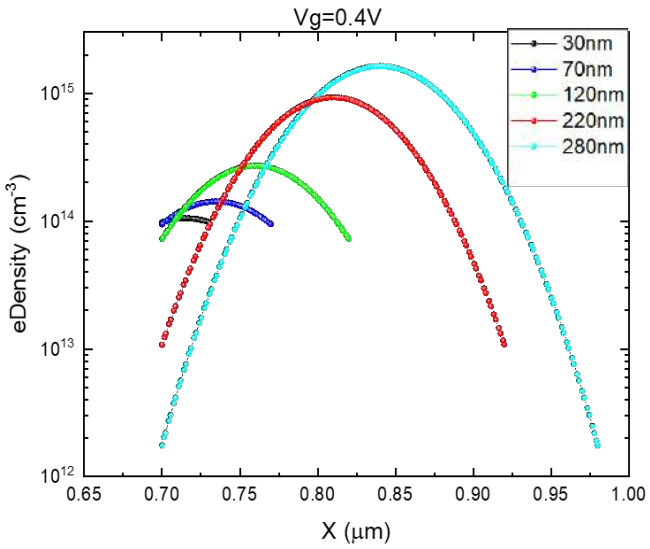


Figure 59: Electron density at V_{GS}=0.4V in the center of the GaN-layer for different channel widths

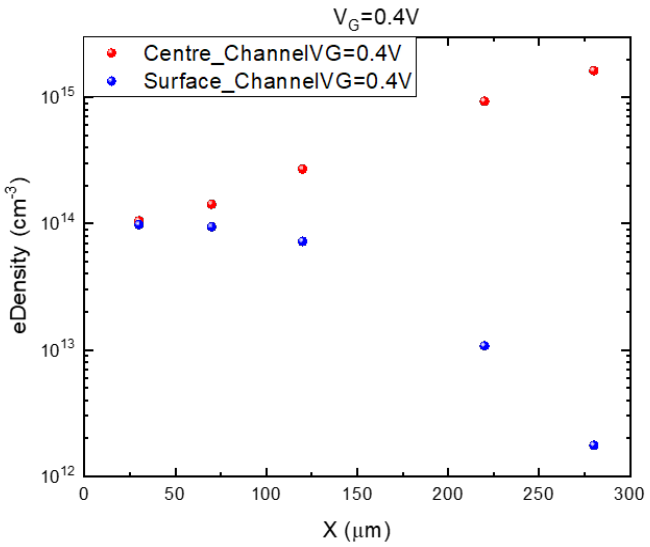


Figure 60: Electron density at V_{GS}=0.4V in the center of the GaN-layer and at the Oxide/GaN interface for different channel widths

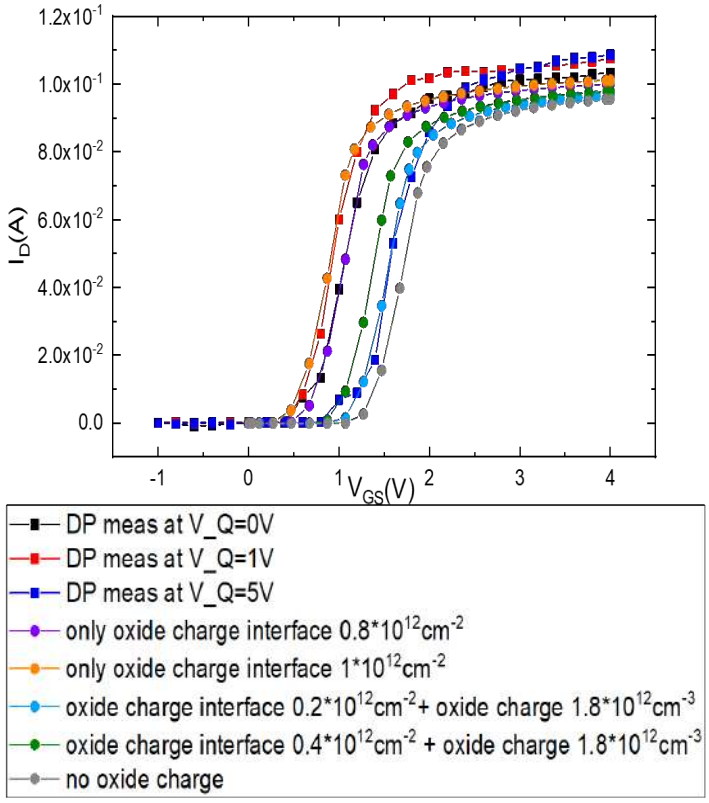


Figure 61: Fit of Double Pulse measurements.

Conclusions

The subject of my master thesis is the analysis of the behaviour and of the reliability of a new topology of transistor: the Fin FET Transistor.
My thesis is divided in two parts: in the first part different kinds of measurements have been performed and hypothesis of physical models of the behaviour of these transistors have been made, in the second part simulations have been performed in order to confirm the hypothesis made in the first part.
The first measurements performed have been the direct current measurements (DC measurements). In these measurements we focused on the variation of V_{th} at different channel widths. The 70nm channel width device had an higher V_{th} compared to the higher channel widths devices. The hypothesis made has been the presence of a parasitic current in devices with higher channel widths which lowers the threshold voltage.
The DC measurements have been performed at different temperatures (50°C, 70°C, 90°C). The behaviour of the devices is the same independently of the channel width: both R_{ON} and V_{th} increase.
The second measurements performed have been the Double Pulse measurements (DP measurements) in order to investigate the oxide trapping by applying a bias gate potential $V_{GS,Q}$. In these measurements V_{th} has a negative shift for low values of $V_{GS,Q}$ ($V_{GS,Q}$=1,2V) and a positive shift for high values of $V_{GS,Q}$ ($V_{GS,Q}$=3,4,5V). The behaviour is the same for every device independently of the channel width.
The last measurements performed have been the V_{th} transients measurements in order to study the times of trapping and detrapping. In these measurements devices have been kept under a positive voltage bias $V_{GS,BIAS}$ for increasing periods of time, and the recovery has been performed too. There is a negative shift of V_{th} for low values of $V_{GS,BIAS}$ and the recovery is complete, for higher $V_{GS,BIAS}$ there is a positive shift of V_{th} and there is no recovery.
In the second part of my thesis we used a microelectronics simulator Sentaurus TCAD to perform simulations.
First, we have fitted the experimental curve $I_D V_{GS}$. The fit is obtained simulating a positive interfacial charge Oxide/GaN and acceptor traps in GaN channel. With the obtained parameters we simulated devices with different channel widths confirming the results of DC measurements: V_{th} increases decreasing channel width. Electron density has been simulated. Electron density for higher channel widths reaches high values in the center of the channel for lower value of V_{GS} and this is the origin of the parasitic current.
In order to simulate the Double Pulse measurements simulations have been performed varying the superficial Oxide/GaN charge and inserting a positive charge within the oxide. The $I_D - V_{GS}$ at $V_{GS,Q}$=1V is simulated increasing

the superficial positive charge, simulating the electrons which pass from Oxide to Gate metal. The $I_D - V_{GS}$ at $V_{GS,Q}$=5V is simulated decreasing the superficial positive charge and inserting a positive charge in the Oxide and it simulates the trapping of electrons in the Oxide surface which reduces the effect of the initial positive charge.
In conclusion we can say that the device has a positive building charge in the Oxide.

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