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BATTERY MANAGEMENT SYSTEM FOR A FORMULA SAE CAR CONCEPT

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ABSTRACT

In this thesis, a Battery Management System prototype has been developed for a formula SAE concept car.
The design is focused on trying to improve the reliability of the system and remove problems that the previous version had. To do this, numerous tests were carried out on the previous version and critical points were analyzed in order to solve them.
The purpose of this report is to explain the entire development phase and how the prototype came about.
The choices of the components that make up the prototype will be analyzed and the programming code written to be able to control the microcontroller and allow the correct exchange of data between the various integrated components in the prototype will be presented.
However, with this elaborate we do not want to propose a finished design of the entire battery monitoring system, but a good starting point for the development of the structure.

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ACRONYMS

SAE	Society of Automotive Engineers
FSG	Formula Student Germany
TS	Tractive System
MCU	Main Control Unit
AIR	Accumulator Insulation Relay
SOC	State Of Charge
SOH	State Of Health
CAN	Controlled Area Network
SPI	Serial Peripheral Interface
GPIO	General Purpose Input/Output
NTC	Negative Temperature Coefficient
AMS	Accumulator Management System
BMS	Battery Management System
IMD	Insulation Monitoring Device
TSAC	Tractive System Accumulator Container
HV	High Voltage
IC	Integrated Circuit
PCB	Printed Circuit Board
EMI	Electromagnetic Interference
LED	Light Emitting Diode
MSB	Most Significant Bit
CS	Chip Select
PEC	Packet Error Code
CRC	Cyclic Redundancy Check
CC	Command Code
DCP	Discharge Permitted
LVS	Low Voltage System
SDC	Shutdown Circuit

1 INTRODUCTION

1.1 FORMULA SAE COMPETITION

The **Formula SAE** is an international University competition in which the students have to build up a single-seater competition car prototype. This competition was initially proposed by the Society of Automotive Engineers (SAE) in 1981 and the main purpose is to give to university students the opportunity to put into practice what they learn during the course of study.
Nowadays, the events are reserved to four types of categories:

- **Combustion vehicle (CV)**: a car powered by a thermal engine.
- **Electric vehicle (EV)**: a car that uses electric motors for propulsion.
- **Driverless vehicle (DV)**:a car that moves without human involvement.
- Reserved to teams that present only the vehicle project.

Every year there are many Formula SAE events in different countries and each competition is characterized by some static and dynamic events.
Every event is divided in 3 parts: Static events, Technical inspections and Dynamic events.

1.1.1 *Static Events*

The static events are:

- Design: which consists of the presentation of the complete project of the car, evaluated by a jury of experts of the automotive sector. Particular attention posed on the engineering aspect of the choices made during the prototype design phase.
- Business Plan: in which the team has to present a project in front of a potential sponsor to capture their attention.
- Cost: in which the team has to demonstrate the expenses incurred to carry out the prototype and explain their make or buy choices.

1.1.2 *Technical inspection*

Before accessing the dynamic events, that evaluate the real performances of the car, it has to pass the technical inspections and the tests in which the students have to demonstrate that their prototype was designed and built according with the rules. These rules may change from competition to competition, but they all refer to the same set of rules that characterizes the competition that takes place in Germany (Formula Student Germany (FSG)).
These inspections are:

- **Pre-Inspection**: in which the driver's equipment, rims and tyres are checked.
- **Accumulator Inspection**: in which the accumulator is analysed in order to verify if it is compliant with the rules. Also the accumulator insulation, the hand cart used to transport the battery and the critical data communication are checked. If the accumulator and the hand cart are comply with the rules, they are sealed.
- **Electrical Inspection**:in which the whole electric component in the car is placed under scrutiny. The isolation of the whole vehicle is checked and if it is electrically safe.
- **Mechanical Inspection**: in which the judges verify all the mechanical components and the used materials. Also the samples of the used materials for the impact attenuator and the chassis are checked.
- **Vehicle weighing**: in which the vehicle is weighted.
- **Tilt Test**: in which the vehicle is posed on a tilt table that is tilted of 60° with the tallest driver on board. The vehicle has to remain in contact with the tilt table and there must be no leakage of liquids.
- **Rain Test**: in which the vehicle is sprayed with water for 120 seconds to verify if it is water insulated. The car must be switch on and must remain on in order to pass the test. The insulation device must not detect humidity for the entire duration of the test.
- **Brake Test**: in which the efficiency of the brake system is verified. The driver must accelerate, switch off the tractive system, and break the car. The test is passed if the car stops on a delineated space and all four wheels stop at the same time.

Once the team has pass all the technical inspections, the students can take part at the dynamic events which have the purpose of verifying

the actual performances of the vehicle under various circumstances. The score system is based on the principle that the fastest vehicle takes the maximum points available for that specific events, while other participants take a score in a scaled way with respect to the best score recorded.

1.1.3 *Dynamic Events*

The dynamic events are reported and described in the list below:

- **Acceleration**: the aim of this event is to test how long the car takes to travel a distance of know length. The track is a straight line with a length of 75 m from starting line to finish line. The track is at least 3 m wide and cones are placed along the track at interval of about 5 m. The vehicle starts the run from a standstill.

- **Skidpad**:the aim of this event is to test the car's lateral grip on a flat surface while making a constant radius turn. The track consist of two pairs of concentric circles in a figure of eight pattern. The centres of the circles are 18.25 m apart and the inner circles are 15.25 m in diameter, the outer circles are 21.25 m instead. The driving path is 3 m wide path between the inner and outer circles. The line that pass through the centre of the circles defines the starting and the finishing line. The car will enter perpendicular to the figure of eight and will take two laps on the right and then two laps on the left circles. The first laps on the right circle and the first lap on the left circle are not timed, they are aimed to take confidence with the track and to prepare the correct vehicle speed. Immediately upon finishing the fourth lap, the vehicle will exit the track perpendicular to the figure of eight and move in the same direction as entered in the track. The run time is the average time between the second and the fourth laps, plus eventual penalties given by the hitting of one or more cones that are positioned around the outside of each outer circle and around the inside of each inner circle. Figure 1.1 shows the skidpad track layout.

- **Autocross**: the aim of this event is to test the dynamic ability of the vehicle. The track is a series of turns, straight and slaloms. The track length is less than 1.5 km, the straights are no longer than 80 m, the constant turns are up to 50 m diameter, and the slaloms cones are posed in a straight line with 7.5 to 12 m spacing.

- **Endurance**: the aim of this event is to test the whole car system efficiency. The track is similar to the autocross one, sometimes is even the same. The drivers have to drive in order to reach a distance of 22 km long. Each driver has to split the 22 km in two

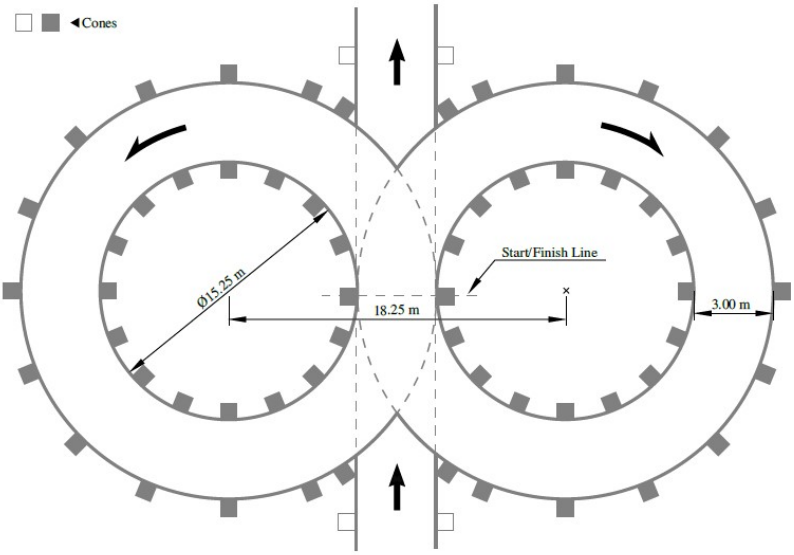


Figure 1.1: Skidpad track layout[1]

equals part up, so there is only one stop period in which the driver change must be made during a three-minute period.

- **Efficiency**: this is part of the endurance event and the aim is to test how efficiently the car has completed the whole endurance. The endurance energy is calculated as the time integrated value of the measured voltage multiplied by the measured current logged by the data logger. The energy regenerated is multiplied by a factor of 0.9 and it is subtract from the used energy.

2

UNIPD FORMULA STUDENT TEAM: RACE UP TEAM

The Formula SAE team of the University of Padua is made up of about 80 members for the two divisions, combustion and electric. Each member is normally part of the team for at least two years, in order to consolidate and pass on the knowledge acquired during their stay within the team to the new members who join the group every year.
The University of Padua has participated in the competition every year with a new combustion car since 2006 further improving their results at events and introducing significant improvements. The current car being designed is the sixteenth: the MG 17-22.
In the 2015 the design phase for the electric machine has begun with which to compete in the specific category. In 2016 the first car, the ORIGIN-E, debuts in FS Germany.
The sixth electric car, SG-e 05, is currently in the planning stage.
Some of the best results are shown below:

- **2010** winners of the Best Newcomer award at the Silverstone event (UK)
- **2013**: third among cars with internal combustion engine and winners of the acceleration test at the Silverstone event (UK)
- **2014**: winners of the Business Plan Presentation in Hockenheim (DE) and in Varano (IT)
- **2015**: 2nd place in the acceleration test in Hockenheim (DE); 1st place in the skidpad test (lateral grip evaluation), 2nd place in the autocross test (qualifying lap) and 4th place in the acceleration test in Varano (IT)
- **2016**: 1st place in Design and Skid Pad, 3rd place in Autocross in Varano (IT)
- **2017**: winners in Class 3 with the ORIGIN-E in Varano (IT)
- **2018**: 2nd place in the Cost Event in Varano (electric). 1st place Cost Event in Varano and 5th place overall (combustion)
- **2019**: 2nd place (combustion) and 6th place (electric) overall in Varano. Finalists at the Cost Event at FSG with SG-e 03 (electric). 4th place overall in Hockenheim (DE) with Mg 14.19 (combustion)
- **2020**: 1st place Design Event and 1st place Business Plan Presentation at Formula Ata (virtual event) (combustion)

Figure 2.1: SG-e 04: The car designed by UniPD team for the FSAE competition of season 2020-2021

- **2021**: 5th place overall (combustion) and 5th place Business Plan (electric) in Spielberg (A); 4th place Business Plan Presentation (electric) in Budapest (HU); 5th place Autocross (combustion) and 4th place Business Plan (electric) in Hockenheim (DE); 3rd place Overall, 3rd place Business Plan Presentation and Endurance and 1st place Skidpad and Autocross (combustion) in Varano (IT).

Figure 2.1 shows the car designed by UniPD team for the FSAE competition of season 2020-2021: the SG-e 04.

2.1 RACE UP ELECTRIC TEAM

The Electric division of the Race Up team is made up of about 40 members and each of them is part of a specific department that, during the season, will take care of very specific works for the design and construction of the racing car.
There are 7 departments in total and they are:

- **Aerodynamics**: this department is responsible for producing an aerodynamic package that guarantees maximum competitiveness in the dynamic tests of events and the right levels of flow to the components dedicated to cooling.

- **Electronics**: : is responsible the management of the low voltage electronics of the vehicle at the hardware level, from the Printed Circuit Board (PCB) development to the entire wiring present in

the car, therefore everything that allows the Main Control Unit to correctly detect the values obtained from the sensors placed in the car.

- **Monocoque and composites**: mainly deals with the design and construction of the monocoque, made entirely with a sandwich structure of composite materials, with the aim of satisfying both the lightness, stiffness requirements linked to performance and to safety.

- **Mechanical Structures**: is responsible for the design and maintenance of the gearboxes, the steering unit and the brakes with the aim of increasing efficiency and reducing weight.

- **Powertrain**: mainly deals with the propulsion system of the car and everything that concerns the high voltage part present in the car.

- **Vehicle Dynamics**: is responsible for the definition of the general specifications of the car, studies on tires, and suspension kinematics

- **Software**: deals with the programming of the numerous microcontrollers present in the car, such as the one present in the Main Control Unit, in the Battery Management System, or in the driver's display.

However, during the season all departments work closely with each other to lead to the design and construction of a high-performance and highly competitive car.
Figure 2.2 shows the Race Up electric team after the Design presentation at FS EAST 2021 which took place at Hungaroring (HU).

Figure 2.2: Race Up Electric Team at FSEast 2021

3

DESIGN OF FSAE ELECTRIC VEHICLE

3.1 MECHANICAL COMPONENTS

The main structure of the car is the chassis which, in our case, is made of a monocoque made from a sandwich of composite materials including carbon fiber. This part is critical since it must weigh as little as possible to allow the car to achieve good performance but at the same time ensure high rigidity, especially as regards the torsional stiffness which establishes the basis for good vehicle dynamics.
Figure 3.1 shows a render of the monocoque used in the season 2020/2021.
The arms that support the wheel groups are fixed to the monocoque, each of which is fitted with one of the four electric motors present in the vehicle's configuration. The suspensions are also fixed to the chassis, which are of the double wishbone type with pushrod thanks to which numerous parameters can be set to influence the dynamic response of the car based on the type of set-up desired and the type of event in which the car must compete.

3.2 AERODYNAMIC PACKAGE

Another element of considerable importance is the aerodynamic package.
This is made up of a set consisting of: a front wing, a rear wing and a large number of components applied to the bottom of the car thanks to which it is possible to exploit the speed of the air to generate downforce in order to ensure better adherence of the car to the asphalt to increase performance on the track.

Figure 3.1: Render of monocoque used in the season 2020/2021

Figure 3.2: Render of aeropack used in the season 2020/2021

Figure 3.2 shows a render of the aerodynamic package used in the season 2020/2021.

3.3 ELECTRIC POWERTRAIN

The electric powertrain refers to the sets of components that generates power required to move the vehicle and deliver it to the wheels. The main components are: the battery, the electric motors and the power inverters. The tractive system accumulator provides powers to feed the inverters, that takes input from the main control unit to power up four independent motors, which ones are mounted before an epicyclic gearbox, with transformation ratio 1:14, inside the upright.
Figure 3.3 shows an overview of electric powertrain system.

3.3.1 *Motors and Inverters*

Currently as motors and inverters they are used the Formula Student Electric (FSE) Racing Kit by AMK. This kit has been specially developed for University teams for this type of competition and includes:

- An AMKASYN KW26-S5-FSE-4Q Inverter
- Four DD5-14-10-POW synchronous servo motors

The DD5-14-10-POW are internal permanent magnet synchronous motors (IPMSM). The choice of an are internal permanent magnet (IPM) was made to take advantage of a higher torque range with the same rpm compared to an surface permanent magnet SPM. It has a number of polar pairs equal to 5, so 10-pole, and can reach 20 k rpm in a weakening regime. The maximum torque at the shaft is 21 Nm and the maximum power is 35 kW. It is equipped with a digital encoder with temperature sensor and base is not cooled. The stator case is made of aluminum.

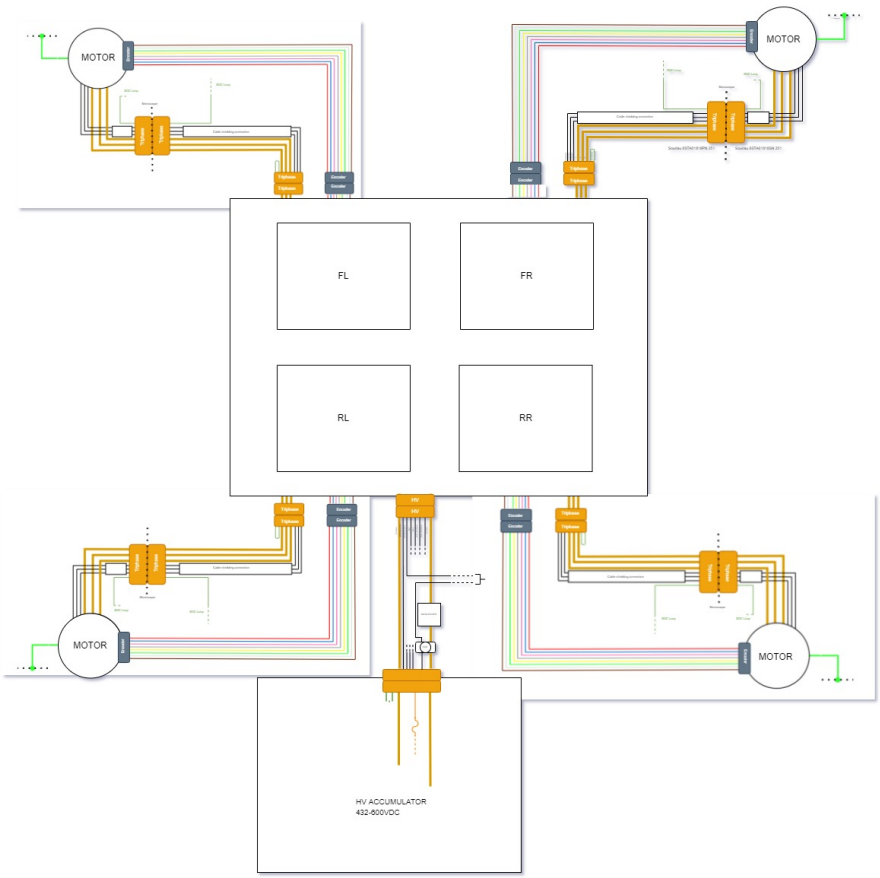


Figure 3.3: Overview of the electric powertrain system

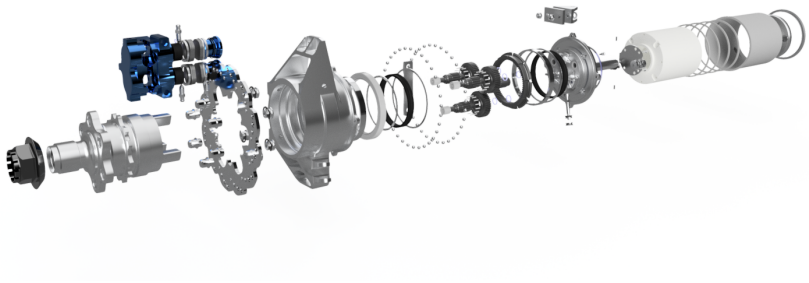


Figure 3.4: Exploded view of motor and upright

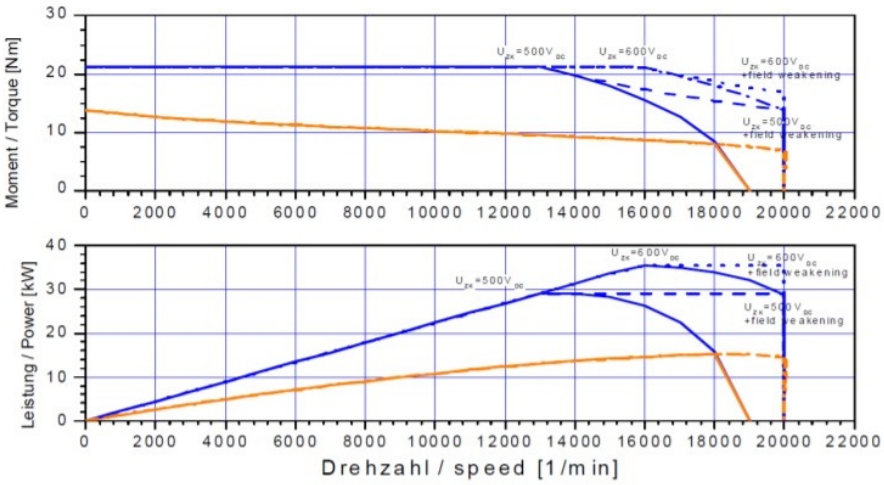


Figure 3.5: DD5-14-10-POW motor characteristic curve [2]

Figure 3.4 shows the motor placed before of the epicyclic gearbox inside the upright.
Figure 3.5 is an abstract from the datasheet of the motor showing its performance curves.
The top graph show the moment/torque as a function of the speed, while the second one represents the power curve as a function of the speed. In those graphs you could see two different curves, the orange one represents continuous torque and rated power, while the blue one represents the maximum peak performance available.
Figure 3.6 shows the AMKASYN KW26-S5-FSE-4Q inverter assembly at the time of purchase.
From this image can be recognise the main parts that are:

- I1, I2, I3 and I4 that represents each one modular inverter that contains the power electronic circuits and the controller board for each motor.
- P1, P2, P3 and P4 that are the Power Electronic of each inverter module

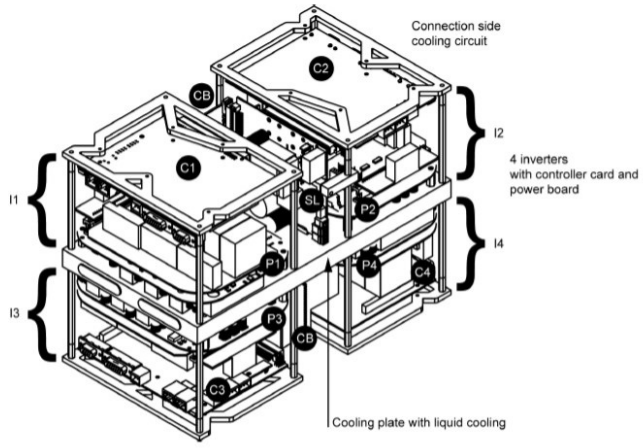


Figure 3.6: AMKASYN KW26-S5-FSE-4Q Initial inverter assembly view [2]

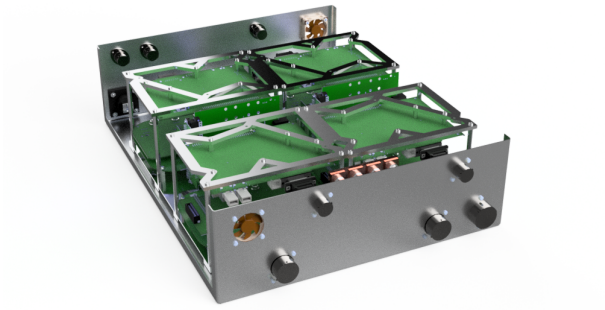


Figure 3.7: AMKASYN KW26-S5-FSE-4Q current Inverter configuration

- C1, C2, C3 and C4 that represents the control board for each inverter and motor. C1, C2 and C3, C4 shares respectively the same low voltage supply network and the same CAN network.

This configuration has been changed to be able to place the inverter under the battery to take up less vertical space.
Figure 3.7 shows the current configuration while figure 3.8 shows how the inverters (green highlighted in the figure) and the battery (red highlighted in the figure) are positioned at the rear of the car.

3.3.2 *Battery*

An electrochemical cell is a device capable of either generating electrical energy from chemical reactions or using electrical energy to cause chemical reactions. A battery is composed of several cells connected in parallel, series or series-and-parallel pattern in order to obtain the desired characteristics.
The operation of the batteries is based on an oxidation-reduction, or redox, reaction in which the oxidation states of atoms are changed. Oxidation is the loss of electrons or an increase in the oxidation state

Figure 3.8: Location of the inverter and the tractive system battery in the car

of an atom, while reduction is the gain of electrons or a decrease in the oxidation state of an atom.
Redox reactions of opposite type occur when connecting the battery to an electric load or to an electric energy source. The battery in this case acts as an energy generator.
In a charged battery, an electromotive force (EMF) of electrochemical type arises due to the different polarities of the reactants, this is called polarization EMF and produces a flow of electrons (current) in the load connected to the battery terminals and is responsible for the conversion of chemical energy into electric energy, this leads to battery discharge. The connection of the load to the battery terminals produces a spontaneous redox reaction.
When an electric energy source is connected to the battery, this acts as a user. The polarization EMF opposes the flow of electrons (current) produced by the external source into the battery and is responsible for the conversion of electric energy into chemical energy, this leads to battery charging.
The anode of the battery is the electrode that loses electrons, which oxidizes, during the redox reaction. These electrons go out from the anode and enter the cathode that is the electrode in which the reduction reaction occurs, so it gains electrons.
The rechargeable battery, also known as a secondary battery, differ from the primary type precisely for the particularity of being able to be recharged once used. This type of batteries are indicated for portable consumer devices, tools, uninterruptible power supplies and vehicles.
For their property, in the secondary batteries, the roles of cathode and anode are depending on the type of operation. When a load is connected to the battery and it works as an energy generator, the

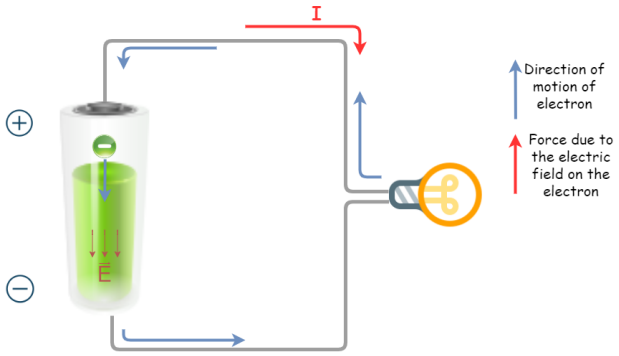


Figure 3.9: Ideal EMF Source

positive pole is the cathode because the current goes out from it (due to the convention) and enters into the negative pole, that is the anode. When the battery operates like an user, so an electric energy source is connected to the battery terminals, the positive pole is the anode while the negative pole is the cathode. When the load is connected to the EMF source, the electron leave the negative terminal, and return to the positive terminal, passing through the load. The EMF source has to maintain the potential difference between the to terminals, so the negative charges (electrons) must be moved from the positive terminal to the negative terminal.

Figure 3.9 show the EMF Source that maintain a potential difference between the two terminals. The force on the electrons from the negative charge is in the opposite direction of the electric field, so, in order to move the electrons towards the negative terminal, work must be done. The energy required to carry out this work comes from the chemical that happens reactions inside the battery.

The electromotive force is defined as the potential difference across the terminals of the battery when no current is flowing through it and depends on the reactants and the state of the charge of the cell.

The emf is also defined to the work done by the cell on the charge per unit charge:

$$\epsilon = \frac{\delta W}{\delta q}$$

The voltage at the battery terminals is a voltage measured across the terminals of the battery when there is no load connected among them. An ideal battery is an electromotive force source that is able to maintain the voltage at the terminal constant, independent of the current between the two terminals. An ideal battery has also no internal resistance, and the voltage at the terminal is equal to the emf of the battery.

There are many types of batteries technology available on the market and they differ in the type of chemistry with which they are made internally such as sodium-sulfur, lithium-ion, and lead-acid batteries. These different technologies offer different characteristics and depend-

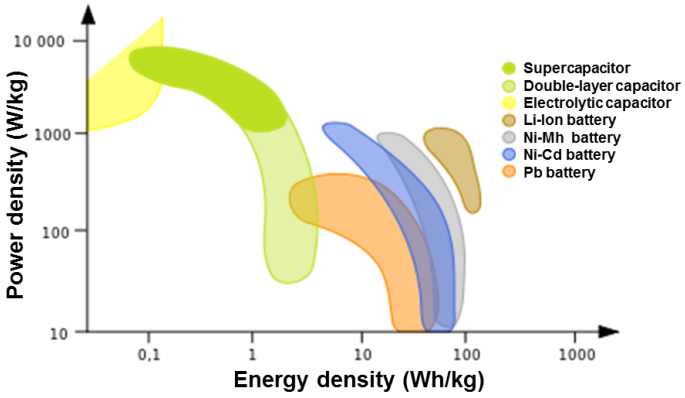


Figure 3.10: Energy and power densities of different batteries technology [3]

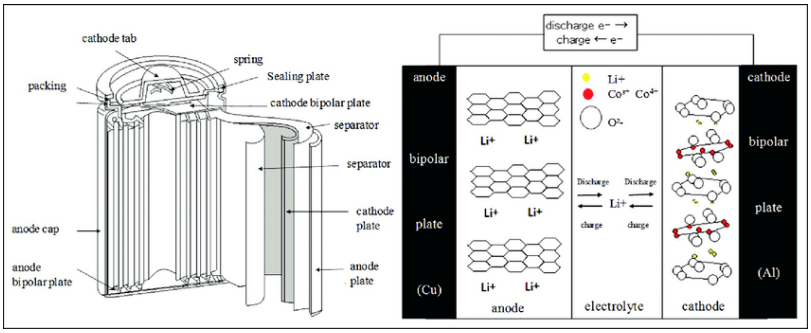


Figure 3.11: Lithium battery internal structure [4]

ing on the type of use, certain chemicals are chosen over others.
Figure 3.10 shows the energy and power densities of different types of batteries.

3.3.2.1 *Lithium-Ion (Li-ion) battery*

The Lithium-ion (Li-ion) battery uses lithium as a chemical element. The internal structure essentially consists of four elements: anode, cathode, electrolyte, and separator.
Based on what type of electrolyte you are using can be spoken of Lithium-ion (Li-ion) battery if the electrolyte used is solid and Lithium polymer (Li-Po) battery if it is used polymer electrolyte.
Figure 3.11 shows the typical internal structure of a lithium battery. Mostly used materials for the cathode are lithium oxides, for example lithium-cobalt oxide $LiCoO_2$ lithium oxides with manganese dioxide $LiMn_2O_4$ or with iron and phosphorus dioxides $LiFePO_4$.
The anode consists of crystallized carbon or graphite or, more recently, of lithium titanate LiTO.
The operating principle of Lithium accumulators is based on a chemical action called "intercalation" which consists in inserting lithium ions into the crystal lattice of the carbon without modifying its crystalline structure.

For li-ion battery, the electrolyte is a lithium salt (for example: lithium hexafluorophosphate $LiPF_6$) dissolved in a non-aqueous organic solvent because lithium reacts violently with water. The electrolyte of Li-ion accumulators does not participate in redox reactions but acts as a conduction medium for lithium ions.
For Li-Po battery, the electrolyte is dissolved in a solid polymer, such as polyacrylonitrile, that unlike the organic solvent used by Li-ion cells, it is not flammable.
The separator prevents an internal short circuit caused by the two electrodes that can come into contact with each other when the electrodes are pressed and a liquid or gelatinous electrolyte is used. The separator must be insulating but permeable to ions.
One particular aspect to keep under observation is the internal temperature of the lithium battery because at elevated temperature $LiCoO_2$ decomposition generates the oxygen that reacts with the organic electrolyte of the cell giving rise to a highly exothermic reaction that, without adequate detection or mitigation can spread to adjacent cells or ignite nearby combustible material. The worst-case consequence is thermal runaway.
As can be seen from figure 3.10, the lithium battery offers high energy density, which can help to reduce the weight and volume of the battery pack. Moreover, they need low maintenance, have very low self-discharge, and a long lifespan but require a protective circuit because they are dangerous.
In order to keep constantly monitor the critical parameters of the lithium cells, specific boards are used and take the name of the Battery Management System (BMS).

3.3.2.2 *SG-e 04 tractive system (TS) accumulator*

There are several parameters that are normally used to characterize a battery, the most important are described below:

- Nominal voltage V_N : is the average battery terminal voltage during the allowed discharge process and it is measured at the mid point between full charged and fully discharged based on a 0.2C discharge (where C is the rated capacity of the cell in mAh).

- Capacity C : is the charge that the battery can delivers during the discharge under specified conditions, it is typically reported in Amp-hr.

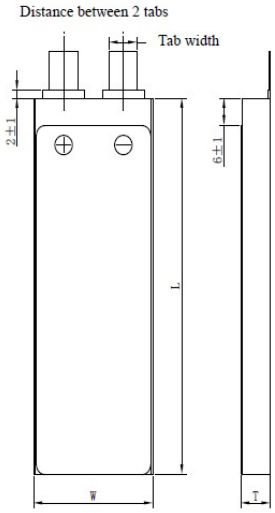
- Theoretic energy E_T : is defined as the product between the nominal voltage V_N and the theoretic capacity.
  C_T
  $$E_T = V_N \cdot C_T$$

2. 型号 MODEL

SLPBA843126 6350mAh 15C 3.7V

3. 产品规格 SPECIFICATION

单颗电池规格 Specifications of single cell



◆标称容量 Typical Capacity①		6.35Ah
◆标称电压 Nominal Voltage		3.7V
◆ 充电条件 Charge Condition	最大电流 Max. Continuous charge Current	12.7A
	峰值充电 Peak charge current	25.4A(≤1sec)
	电压 Voltage	4.2V±0.03V
◆ 放电条件 Discharge Condition	Max Continuous Discharge Current	105A
	Peak Discharge Current	127A(≤2sec)
	Cut-off Voltage	3.0V
◆交流内阻 AC Impedance(mOHM)		<2.0
◆循环寿命【充电:1.0C,放电:15C】 Cycle Life【CHA:1.0C,DCH:15C】		>100cycles
◆使用温度 Operating Temp.	充电 Charge	0℃~45℃
	放电 Discharge	-20℃~60℃
◆ 电芯尺寸 Cell Dimensions	厚度 Thickness(T)	10.5±0.3mm
	宽度 Width(W)	42.7±0.5mm
	长度 Length(L)	127.5±0.5mm
	极耳间距 Distance between 2 tabs	21±1mm
◆ 极耳尺寸 Dimensions of Cell tabs	极耳材料 Tab Material	Pure Aluminum
	极耳宽度 Tab Width	15mm
	极耳厚度 Tab Thickness	0.2mm
	极耳长度 Tab Length	Max 30mm
◆重量 Weight(g)		131±2.0
①标称容量：0.5CmA,4.2V~3.0V@23℃±2℃ Typical Capacity:0.5CmA,4.2V~3.0V@23℃±2℃		

Figure 3.12: MELASTA SLPB A843126 6350 mAh 15C 3.7V characteristic parameters [5]

- Energy efficiency η_e : is defined as the ratio between the energy delivered during the discharge process W_d and the energy absorbed during the preceding charge process.
  W_c

$$\eta_e = \frac{\int_0^{t_d} v_d \cdot i_d \, dt}{\int_0^{t_c} v_c \cdot i_c \, dt} = \frac{W_d}{W_c}$$

In order to compete competitively in the competitions, the electric vehicles must be able to use all the energy stored in the tractive system accumulator. The configuration used in the $SG-e$ 04 is composed of 144 series made of 2 parallels $(144s2p)$ of LiPo cells. The battery cells used are the MELASTA SLPB $A843126$ 6350 mAh 15C $3.7V$.
Figure 3.12 is an abstract from the MELASTA SLPB $A843126$ 6350 mAh 15C $3.7V$ datasheet and shows its characteristic parameters. The battery pack consists of 8 segments of 36 *cells each* $(18s2p)$ and can deliver 3.6 MJ for a maximum voltage of 75.6 V. Each individual segment weighs 5 kg and the whole battery is 48 kg.
The whole battery guarantees 6.7 kWh with withstand continuous

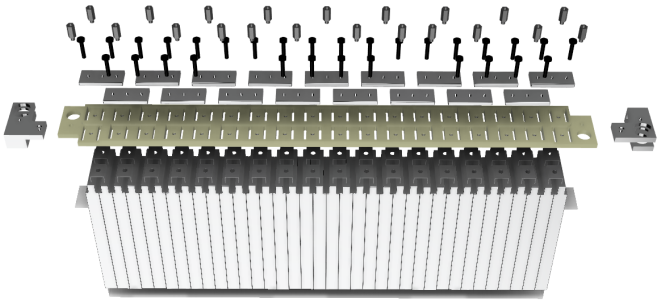


Figure 3.13: exploded view of the SG-e 04 battery segment

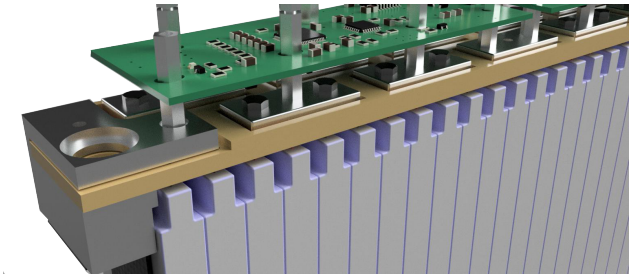


Figure 3.14: Macro of SG-e 04 battery segment

discharge current of 210 A and a peak discharge current for up to 2 *seconds of* 254 A.
The cells are mounted in a milled epoxy-fiberglass support and are connected in series by through aluminium busbars that are designed with a aluminium spacer used to connect to the BMS slave boards both mechanically and electrically.
At the end of each segment there are two end-tabs that allows the connections to the next segments via maintenance plugs.
Figure 3.13 shows an exploded view of the battery segment.
Figure 3.14 shows a macro view of the battery segment.

Figure 3.15 shows a render of the tractive system accumulator of the SG-e 04.

Figure 3.15: Render of the SG-e 04 tractive system accumulator

4 BATTERY MANAGEMENT SYSTEM

The battery management system is an electronic circuit used to monitor the battery cells.
Its main roles are to sense the voltage, the temperature, and the current of the cells in order to keep the battery in its safe operating area during the charging and discharging cycles, to manage the charging and discharging operation, and to provide health state of the battery. All this is to keep at all times the battery in a safe condition and to increase its lifetime. In order to do that, a dedicated cell monitoring controllers are being used which monitor the state of each individual cell according to pre-adjusted voltages and temperatures using high precision ADCs.
To have a better estimate of the State Of Charge (SOC) or State Of Health (SOH), all the cells measurement of the entire battery have to be synchronized.
For the Battery Management System of Formula SAE cars it is required to:

- The battery monitoring system must be remain operative whenever the Low Voltage System (LVS) that powers the vehicle, is active or if it is connected to a charger;
- monitor the voltage of all cells inside the battery pack;
- the temperature of at least 30% of the cells equally distributed within the Tractive System Accumulator Container (TSAC) and cell temperature must be measured at the negative terminal of the respective cell.
  The sensor used must be in direct contact with the negative terminal or less than 10 mm along the high current path;
- Produce a voltage fault if the critical thresholds are exceeded for a time greater than 500 ms;
- Produce a temperature fault if the temperature of 60°C is exceeded for more than 1 s;
- If a fault is detected, it must switch off the Tractive System (TS) via the shut-down circuit.

4.1 OLD VERSION LAYOUT AND RELATED ISSUES

The previous version of the BMS was made with a centralized system where there was a master / host referenced by all the slaves.

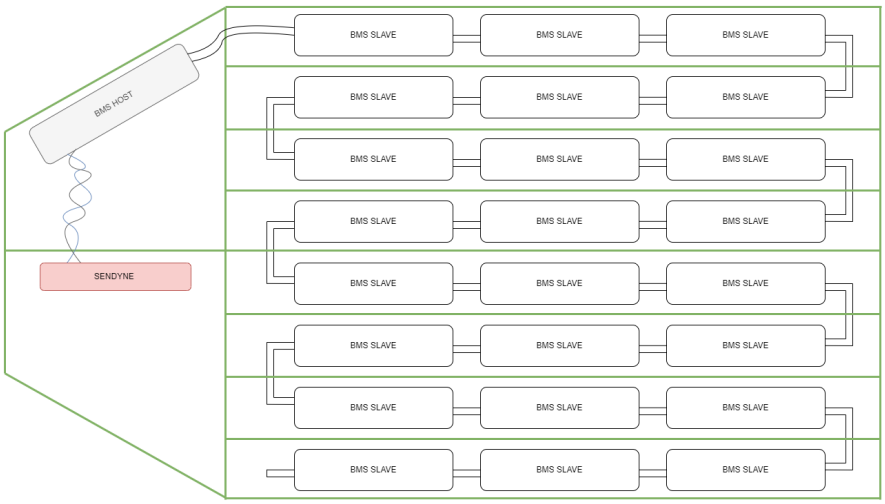


Figure 4.1: BMS with current sensor architecture

The slave had the tasks of reading the voltages and temperatures of the various cells and subsequently sending this information, through a dedicated CAN bus line, to the master to be analysed.
The host, on the other hand, had the task of consulting the slaves and once the data had been analysed, it had to communicate with the Main Control Unit (MCU) of the vehicle via another dedicated CAN bus line to warn of any anomalies and possibly open the Shutdown Circuit (SDC). The SDC is the portion of wiring that connects all the sensitive elements and safety sensors. It is used to control the power supply of the Accumulator Insulation Relay (AIR), which are used to interrupt the electrical circuit of the High Voltage (HV) battery pack in the event of a crash, short circuit, overheating and other emergencies.
A further task of the host was to read the output current values from the battery pack through an additional dedicated CAN bus line coming from a PCB with an integrated shunt, made by Sendyne (Sendyne SPF 200).
Figure 4.1 shows the BMS system with the current sensor architecture scheme. Figure 4.2 show a render of the previous version of the BMS Slave.
However, this version of BMS suffered of some problems that affected its correct functioning. Some of these problems are listed below:

- The bad voltage sensing point of contact, that was made with a pitch in the PCB and that took the voltage references from M3 aluminium spacers.
- The mechanism for mounting the PCBs on the M3 aluminium spacers, which provided both electrical and mechanical contact, was long and difficult because it was necessary to be very careful in placing the boards firmly without moving them to avoid false contacts that could damage the control devices. This contact

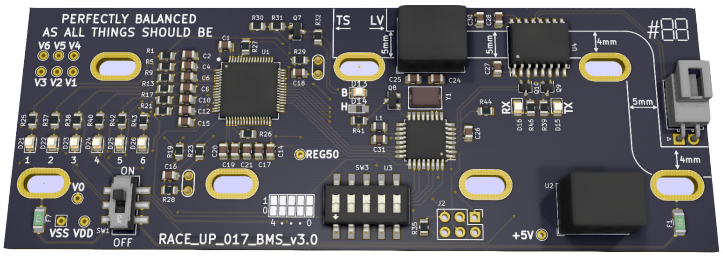


Figure 4.2: Render of the previous version of the BMS Slave

mechanism was very time-consuming during the board debugging phases.
BMS slave mounting mechanism on the battery segment can be seen in figure 3.14.

- The impossibility of completely turning off the microprocessor made it almost mandatory to remove the PCBs from the battery pack during periods of long inactivity in order to prevent the cells from going under their cut-off voltage, thus making them no longer usable.

- the use of CAN as a communication protocol made it necessary to have a microcontroller in each slave board. This implied that every minimum change in the slave program, such as the minimum voltage threshold value, or the registers of the integrated circuit to be sent to the vehicle control unit, resulted in the reprogramming of each of the 24 boards present in the battery pack.

- The presence of two microcontrollers, one in the slave and one in the host meant developing two separate codes. This involved a significant amount of time in the design and debugging phase.

- The problem with the Integrated Circuit (IC) used for monitoring cell voltages and temperatures. It often happened that integrated circuits burned for unknown causes. In particular, it was noted that the device entered thermal protection and heated up in the area near the sensing part of the cells.

- The interferences generated by the inverter switching modules which produce noise on the reading values consequently causing the opening the shut-down circuit because they detected values outside of the pre-selected limits on the cell temperatures and voltages.

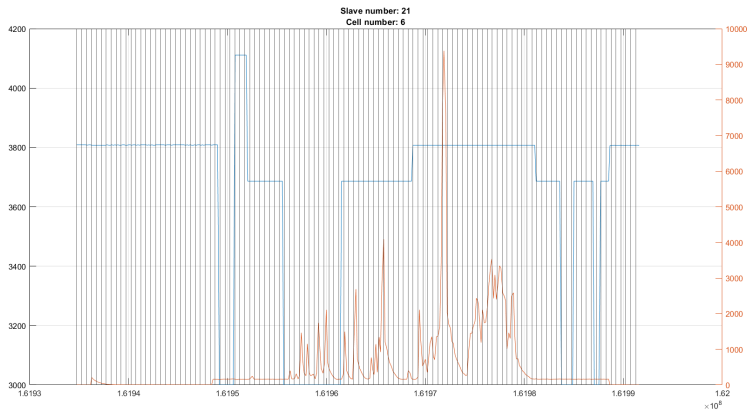


Figure 4.3: BMS Slave Interference plot analysis

- Long cables used to connect all the BMS slaves board.
- Often the pins in the connectors broke due to mechanical stress. This was because the wiring was arranged in a messy manner inside the battery pack.

To go into more detail and to explain in a better way the issues of interferences that significantly influenced the voltage and temperature readings of the BMS Slave, in figure 4.3 can be seen a plot showing the voltage detected by the board during a short period of data acquisition during a track test of the car. As can be seen, the voltage (represented by the blue line in the figure 4.3) is highly disturbed, going under the under voltage threshold of 3000 mV for non-negligible periods.
The black lines in the figure are temporally spaced by 500 ms, the time for which the shut-down circuit must be open if one of the 6 voltages that monitors each board exceeds the under or over voltage limits. The orange line represents the current logged by the current shunt sensor.
Almost certainly these interferences are caused by electromagnetic interference caused by the switching of the power MOSFETs of the inverters which are positioned under the high voltage battery.
In the new design configuration of the inverters, some precautions will be adopted that will reduce interference. In particular, according to the manufacturer AMK, the grounding of the motors and inverters has not been carried out correctly because cables with too large a cross-section have been used unnecessarily as at high frequencies the current tends to be distributed more on the surface of the conductor and less inside (this phenomenon is also known as the skin effect).

4.2 CHANGES AND IMPROVEMENTS

In order to solve these old version problems of the BMS, a study was carried out. In particular, in order to solve the Electromagnetic Inter-

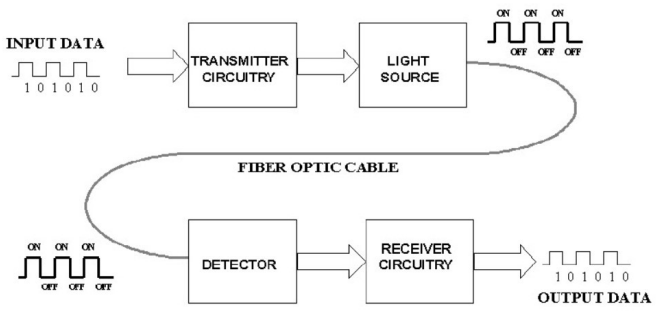


Figure 4.4: Basic fiber optic communication system

ference (EMI), some analysis about different types of communications has been made.
The two communication topologies considered were:

- fiber optic communication,
- wireless communication.

The fiber optic communication involves the transmission of signals in the form of light from one point to the other and the communication system is composed by transmitting and receiving circuitry, a light source, and detector devices.
When the input data available in the form of electrical signals are send to the transmitter circuitry, it converts these signals into a light signal using a light source like a Light Emitting Diode (LED) with characteristics as, frequency, amplitude, and phase that must remain the same for the entire service life in order to have an efficient transmission. The choice of the type of light source to be used depends on the type of applications and some parameters to be take into account could be power, speed, spectral linewidth, cost and noise.
When the optical signal comes to the receiver, it has to convert into an electrical signal again in order to be analysed.
The receiver circuit is composed of a photo detector and an electronic circuit able to measure the magnitude, frequency, and phase of the optic field.
The two mainly used type of photodetectors used for optical receivers in optical communication systems are PN photodiode and avalanche photodiode. A Basic fiber optic communication system is shown in figure 4.4.
This communication system was considered for its main feature of being inherently immune to EMI and radio frequency interference, because, not having a charge that transport the information, it is not affected by magnetism and the presence of an external magnetic field does not affect the integrity of the signal.
A further aspect that led to the consideration of this communication system is the property of electrical insulation that provides. Moreover,

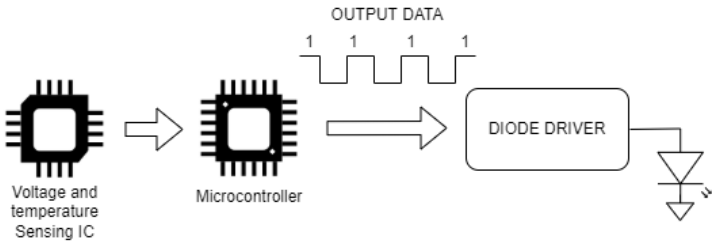


Figure 4.5: basic BMS-slave fiber optic communication system

the fiber cable is very flexible and lightweight.
However, the solution that uses this type of communication would have led to a considerable increase in the complexity of the entire architecture for battery monitoring and, furthermore, each board would be particularly expensive because, in order to develop this architecture, each slave PCB needs to have a microcontroller for management of the LED driver to allow communication.
The basic BMS - slave fiber optic communication system can be seen in figure 4.5.
Another communication method under analysis was the wireless one. This type of communication was considered because it would provide several benefits to the existing system.
In particular, it could offer the potential to guarantee improved reliability, reduce the cost, save space, reduce wiring complexity for connection and eliminate the mechanical wiring failure that is a big source of maintenance problems.
Therefore, due to its intrinsic nature of transmitting information without the use of a cable as a transmission medium, this system would allow reducing costs because there is no longer any need for isolation systems between the various PCBs. Moreover, it would reduce engineering costs due to the time it takes to develop specific communication systems or redesign the wiring diagrams for a new vehicle and reduce the time it would take to make the wiring.
A further behaviour of the wireless connection is the possibility of installing sensors in places previously unsuitable for wiring.
An important aspect that must be taken into consideration in the use of wireless technology is that this system must not interfere with the normal operation of other modules inside the vehicle, so it must ensure good electromagnetic compatibility.
By the way, it is also true that the metal and high EMI environment present in the vehicle could be too harsh to be reliable for a wireless system but the use of a wireless mesh network could be a solution to offer a redundant interconnect system through its use of different paths and frequency diversity to route wireless messages around obstacles and mitigate interference.
A mesh network consists of the network in which devices, which are called nodes, are connected to one another, so the various devices

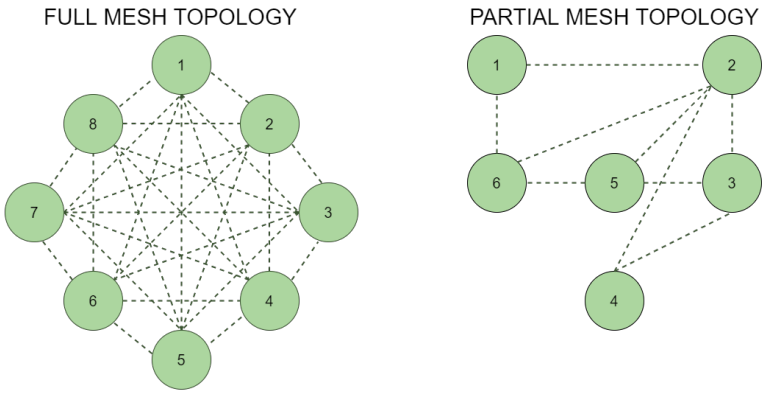


Figure 4.6: Full vs. Partial mesh network topology

in a mesh network have multiple paths through which to exchange information.
There are two typologies of the mesh network, the full and the partial one. The first topology refers to a network in which all nodes are connected directly to all the others, while, the second one refers to a network in which only some nodes are connected to one another.
Figure 4.6 shows a graph depicting these two types of mesh networks.
For this type of communication system, several typologies of protocols can be used, such as ZigBee / ZigBee-Pro, Wi-Fi (IEEE 802.11) / Wi-Fi HaLow (IEEE 802.11ah), Bluetooth Low Energy (BLE 5.0).
Some interesting integrated circuit has been found regarding the wireless communication system. One of great interest is the system developed by *Texas Instrument* (TI) that uses in each sensing board the $CC2642R-Q1$ wireless microcontroller unit for transmitting data. TI, for this project, has developed his own communication protocol based on Bluetooth Low Energy technology operating in the 2.4-GHz frequency band.
This system is a Wireless BMS Development Kit that is called $CC2662RQ1-EVM-WBMS$.
However, this type of data transmission for this project was abandoned because we wanted to bring a working and reliable solution for the BMS for the 2022 season.
The project developed via wireless communication would have taken much longer to build and make the system reliable.
Furthermore, due to the global shortage of chips caused by the COVID-19 virus pandemic, the components for the construction of PCBs with wireless communication (and not only these) were nowhere to be found except with times ranging from 9 to 15 months.
In the end, it was decided to maintain a cable communication method but to change the type of devices for managing the voltages and temperatures of the cells and to change the type of cable communication method.

4.3 NEW BMS CONFIGURATION

Also for this project, as for the one previously carried out, it was decided to use a centralized architecture divided into two parts formed by: host and slaves.
The host's tasks remain that of interrogating the slaves to ensure that they are still operational and of managing any faults originating from the slaves that will take care of acquiring cell voltages and temperatures.
After a careful analysis of the components on the market, it was decided to adapt the configuration using components produced by Analog Devices, to go into detail we are talking about the $LTC6820$ and $LTC6811$.
More precisely, the first integrated circuit, the $LTC6820$, is used in the master/host to be able to interface the microcontroller used to the various slaves by converting the communication from standard SPI to isolated SPI.
On the other side, on the slaves is used the $LTC6811$.
Among the features that make the latter aforementioned integrated circuit suitable to use in the slave board, there are:

- Possibility of measures Up to 12 Battery Cells in Series,
- $16 - Bit$ ADC with Programmable Noise Filter,
- The presence of 5 General Purpose Digital I/O or Analog Inputs, so, with the possibility of being used as Temperature or other Sensor Inputs,
- $1.2\ mV$ Maximum Total Measurement Error,
- Built-in isoSPI Interface,
- Operating temperature range $-40°C$ to $+125°C$ (the $LTC6811H$ version)

Firstly, one of the most important feature for which this integrated circuit was chosen is to be found in the fact that, first of all, it is able to monitor a higher number of cells, and in particular double, compared to the integrated circuit ($BQ76PL536A - Q1$) used in the old version of the BMS Slave that was able to monitor 6 series cells.
This allows having fewer PCBs to monitor the cells of the entire battery pack.
Secondly, with the use of this chip it is possible to create an architecture such that it is no longer necessary to use a microcontroller, such as the $ATMEGA32M1 - AU$ was on previous versions, for each slave.
This configuration therefore offers considerable savings in economic terms for the realization of the entire battery management system.
In addition to an economic saving, with this configuration, it is possible

to save time because it is no longer necessary to reprogram each slave every time if a change is made to the code to be loaded into the microcontroller present in the slave board.
Moreover, one of the features of the *LTC*6811 highlighted above is the presence of a built-in isoSPI interface, this means that this integrated circuit offers the opportunity of using the aforementioned proprietary protocol developed by *Linear Technology*.

4.3.1 *isoSPI communication protocol*

As previously mentioned, isoSPI was developed by *Linear technology* and consists of a simple two-wire adaptation of the Serial Peripheral Interface (SPI) standard, a serial communication protocol between microcontrollers.
The isoSPI then converts a full-duplex SPI signal into a differential signal which is usually transmitted through a pair of twisted cables and a simple transformer. This protocol allows a data transmission speed up to 1 Mb/s.
This type of protocol was created to provide an alternative to much more expensive communication architectures immune to electromagnetic interferences such as the Controlled Area Network (CAN) which, in combination with isolation systems, provide a further solution for applications where it is necessary electrical insulation because there are high working voltages. This type of environment, such as the drivetrain of an electric vehicle, strains the integrity of the information that must be transmitted to the central processor for processing.
The isoSPI gives a solution for this type of application because it provides good resistance to electromagnetic interferences providing low electromagnetic interference susceptibility and emission.
This protocol uses two differential signals of which neither of them is grounded, this allows the differential signal transmitted to remain relatively unaltered as the common mode noise generated by an external electromagnetic interference will be almost identical on both cables.
In addition, this technology uses a transformer to magnetically couple and electrically isolate the signals between the various devices connected to each other, in this way each device is protected from significant variations in the common-mode voltage created by electromagnetic interferences, so, in other words, it allows the rejection of the common-mode interference that can be impressed on the wiring.
As previously mentioned, it is possible to realize a battery management system also with a classic isolated CAN bus in which magnetic, capacitive or optical devices can be used to obtain galvanic isolation for the purposes of safety and integrity of the signals.
The same system can be implemented with the SPI communication protocol, but this would mean having to isolate all 4 signals and this involves considerable costs.

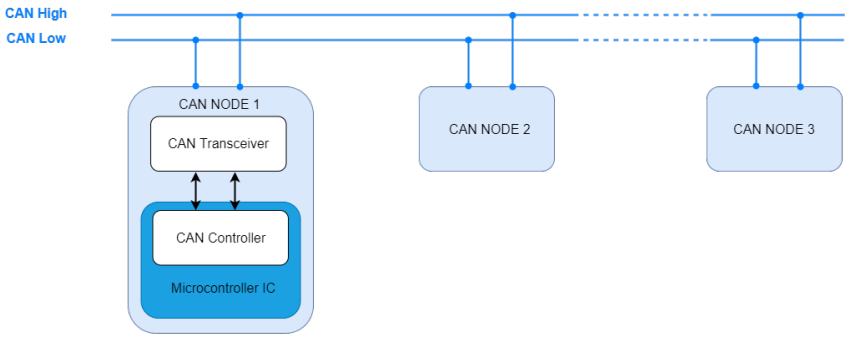


Figure 4.7: CAN Bus communication architecture

As well as the latter system, even the architecture that uses the CAN protocol would be very expensive, it would requires the addition of a CAN transceiver, a controller or microprocessor and an isolator to adapt the signals to the communication bus and the related management, on each PCB such as host and slaves.
This type of communication architecture is shown in the figure 4.7.
The use of the *LTC*6820 and the *LTC*6811 allow respectively to create the isoSPI interface for the master and for the slaves, thus being able to create the communication system significantly reducing costs and space on the board because the first integrated circuit has a package 16-MSOP and the second 48-Lead SSOP.
The primary function of the *LTC*6820 is to provide bidirectional SPI communications between two isolated devices through a single twisted-pair connection.
In order to achieve this, the device must be coupled using a transformer through which the device translates standard SPI signals (CS, SCK, MOSI, and MISO) into differential pulses.
The transmitter is a current regulated differential driver (see 4.8) where the voltage amplitude is determined by the drive current IB ($IBIAS$) and the equivalent resistive load due to the cable and termination impedance. The IP and IM pins delivers a current of $20 \cdot IB$.
The receiver consists of a window comparator with a differential voltage threshold, $VTCMP$, and the comparator detects the following logic values:

- $+1$, when $VIP - VIM$ is greater than $+VTCMP$;
- -1, when $VIP - VIM$ is less than $-VTCMP$.
- a logic 0 indicates that $VIP - VIM$ is between the positive and negative thresholds.

The comparator outputs are sent to filters that discriminate between short and long pulses (see 4.3.1.1). In order to create a configuration that uses communication via isoSPI, it is possible to use several *LTC*6820s properly connected or other devices that convert the signals

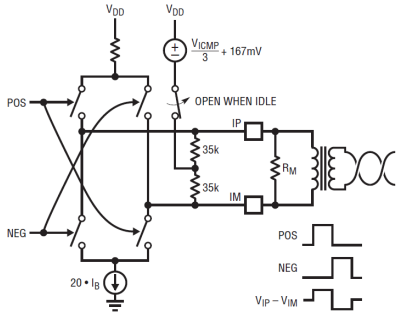


Figure 4.8: LTC6820 current regulated pulse driver [6]

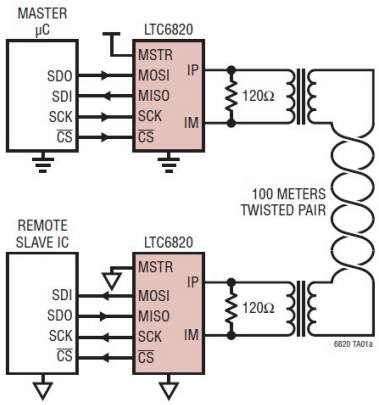


Figure 4.9: typical isoSPI communication architecture [6]

from standard SPI to isolated SPI.
Figure 4.9 shows a typical isoSPI communication architecture using two *LTC*6820, in which the first is paired with a microcontroller or other SPI master where its IP and IM transmitter/receiver pins are connected through a transformer to a second *LTC*6820 that translates the differential SPI signals into standard SPI signals to then be used by one or more slave devices.
Figure 4.10 shows how multiple slaves can be connected to a single master by connecting them in parallel (multidrop configuration) along one cable.
There are two versions of the integrated circuit used on the slaves, namely the *LTC*6811 and the *LTC*6811 − 2, and they differ in that the first allows connections between the various integrated circuits only in a daisy chain, while the version chosen for the realization of this prototype, the *LTC*6811 − 2, allows the connection in an addressed way of the device. In order to set the integrated circuit address, it is necessary to connect the appropriate pins to the positive or negative reference (see 4.3.3.3) and the maximum number of devices that can

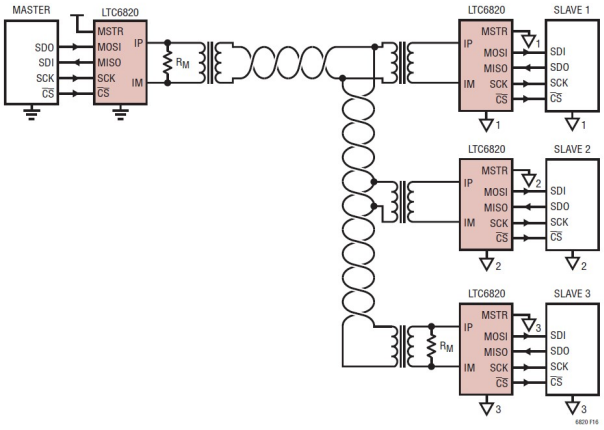


Figure 4.10: typical isoSPI communication architecture with multidropping configuration [6]

be connected in this way is 16 devices.
The choice of the integrated circuit that allows an addressed connection was made because with the parallel addressable bus offers a better fault tollerance due to the fact that the data transmission is directed to the Master without having to go through an electronic component as happens in series connection.
A further advantage is the saving of a connector used for communication for each connected PCB, this is an advantage in economic terms and brings an advantage in terms of space occupied on the board.
Figure 4.11 shows how the isoSPI configuration with the daisy chain method is, and how multiple *LTC*6811 are connected to each other with this type of configuration (figure 4.12).
While figure 4.13 shows how multiple $LTC6811-2$ are connected with multidrop configuration.
As mentioned before, this last type of configuration is the one chosen for this project.

4.3.1.1 *isoSPI Pulse Detail*

Communication consists in the transmission and reception of differential pulses through an isolation barrier. There are three voltage levels: $+VA$, $0\ V$ and $-VA$.
In order to eliminate the DC signal component and to improve the reliability, this protocol uses two different pulse lengths. In this way, there are four types of pulses that can be transmitted.
The $+1$ pulse is transmitted as a positive pulse followed by a negative one.
The -1 pulse is transmitted as a negative pulse followed by a positive one.
The duration of each pulse is defined as t_{PW}, and the total isoSPI pulse duration is $2 \cdot t_{PW}$. Figure 4.14 shows this four pulse types. In order

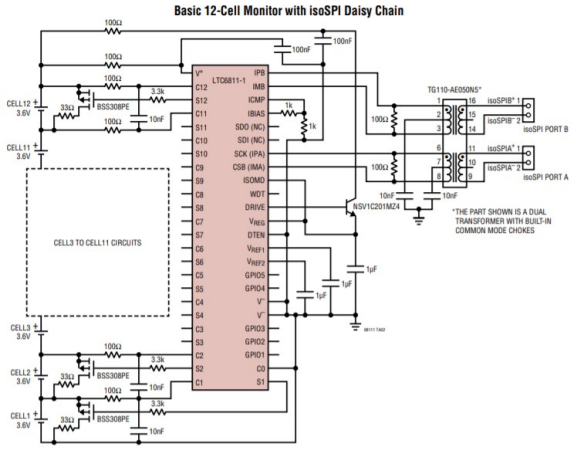


Figure 4.11: LTC6811 connection with daisy chain [7]

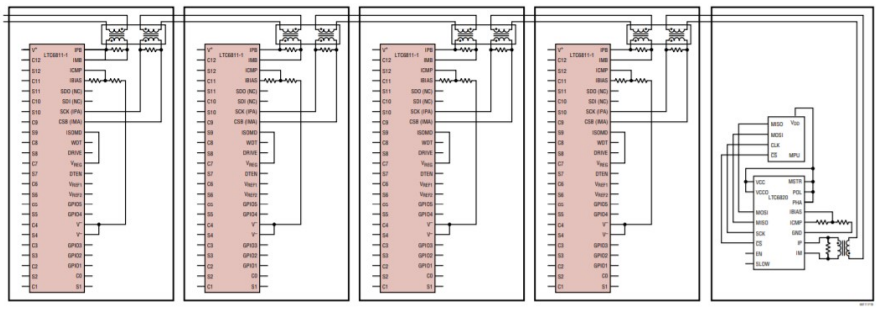


Figure 4.12: Multiple LTC6811 IC in daisy chain configuration [7]

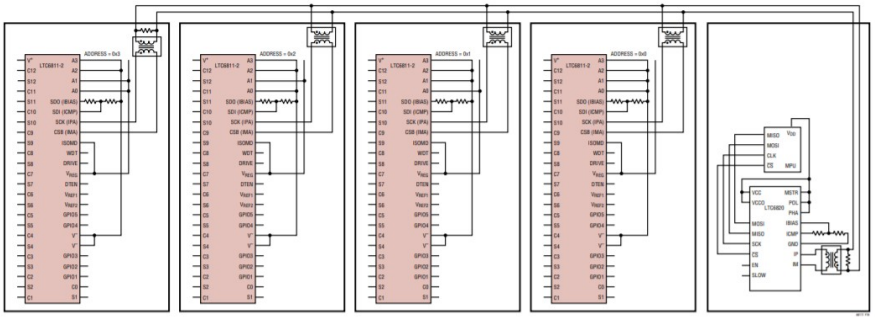


Figure 4.13: Multiple LTC6811-2 IC in multidrop configuration [7]

PULSE TYPE	FIRST LEVEL ($t_{½PW}$)	SECOND LEVEL ($t_{½PW}$)	ENDING LEVEL
Long +1	$+V_A$ (150ns)	$-V_A$ (150ns)	0V
Long –1	$-V_A$ (150ns)	$+V_A$ (150ns)	0V
Short +1	$+V_A$ (50ns)	$-V_A$ (50ns)	0V
Short –1	$-V_A$ (50ns)	$+V_A$ (50ns)	0V

Figure 4.14: isoSPI pulse type [7]

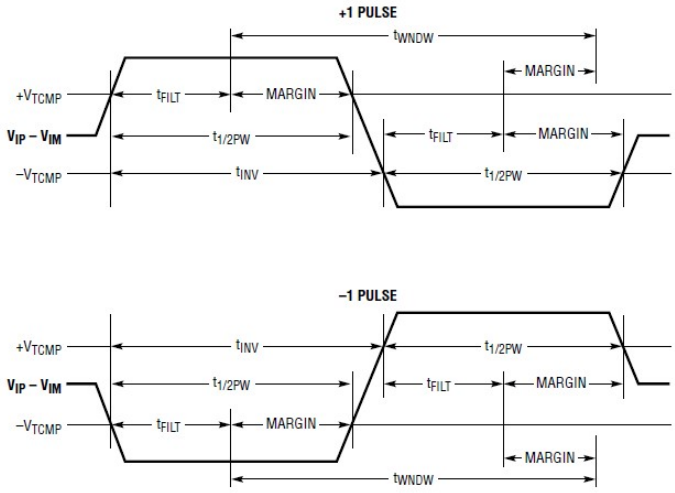


Figure 4.15: isoSPI pulse detail [7]

to allow the communication between the devices, the *LTC*6820 can be used to translate SPI signals into isoSPI pulses, or, if only *LTC*6811 are used, this conversion is done internally because the device has a built-in isoSPI Interface.
Figure 4.15 shows isoSPI pulse details.

4.3.2 *BMS Host*

For this prototype version of the Battery Management System it was chosen to create the BMS Host as a shield for an Arduino due, as it was made in the previous version, so as to be able to verify the correct functioning of the system before integrating a microcontroller into the board.

4.3.2.1 *Schematic analysis*

The schematic of the BMS Host boards has been divided into three worksheets to facilitate reading and speed up the debug. The most significant connections that connect the various worksheets are indicated.
The three parts are called: Arduino Due shield, *LTC*6820 and Auxiliary.
Figure 4.16 shows the part of the schematic where is reported this division into sheets.

4.3.2.2 *Arduino Due shield schematic area*

The Arduino due shield schematic area is very simple because it shows only the symbol of the Arduino Due with all the labels necessary to

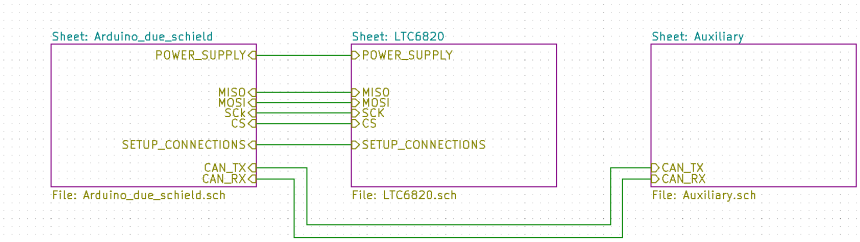


Figure 4.16: BMS Host worksheet schematic

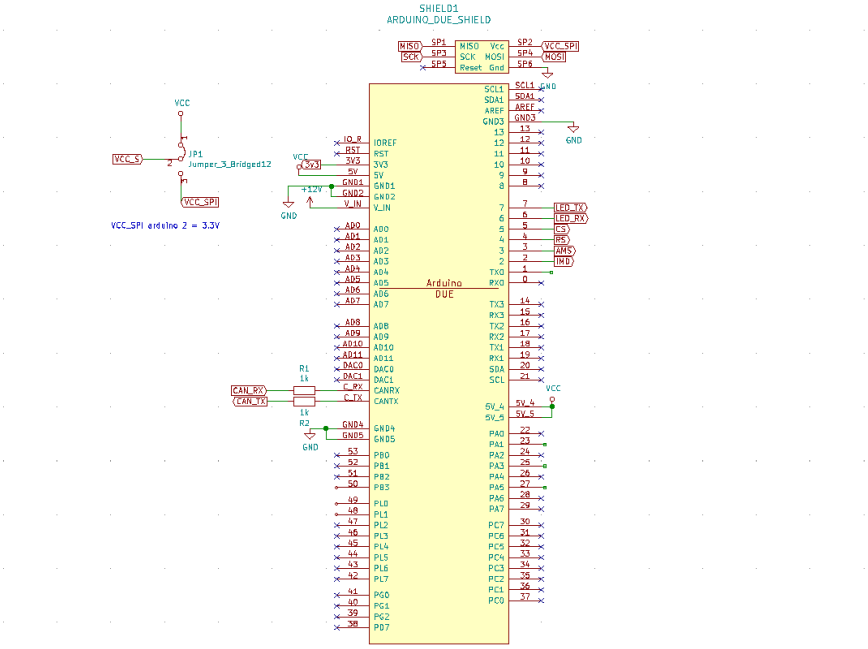


Figure 4.17: BMS Host Arduino due schematic area

make the connections between the ICs and to make the correct setup to use the SPI communication.
This schematic area can be seen in figure 4.17.

4.3.2.3 *LTC6820 schematic area*

The worksheet named with *LTC*6820 has in turn been divided into four macro areas to facilitate reading and understanding during the debug phase.
These four areas are highlighted by labels, namely: LTC6820, COMMUNICATION, SETUP and DEBUG.
The *LTC*6820 worksheet and these four macro areas can be seen in figure 4.18.
The *LTC*6820 schematic part shows the symbol of the IC produced by Analog Devices with all the labels needed to interface it with the Arduino due in order to convert the standard SPI into isolated SPI.

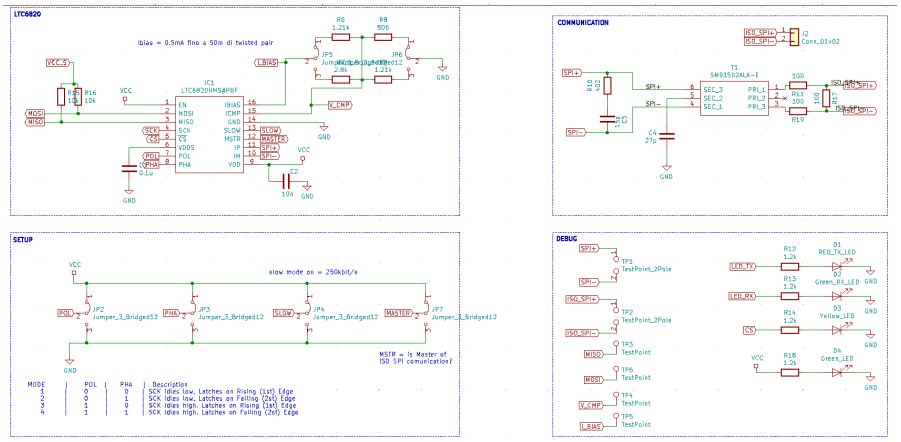


Figure 4.18: LTC6820 schematic area

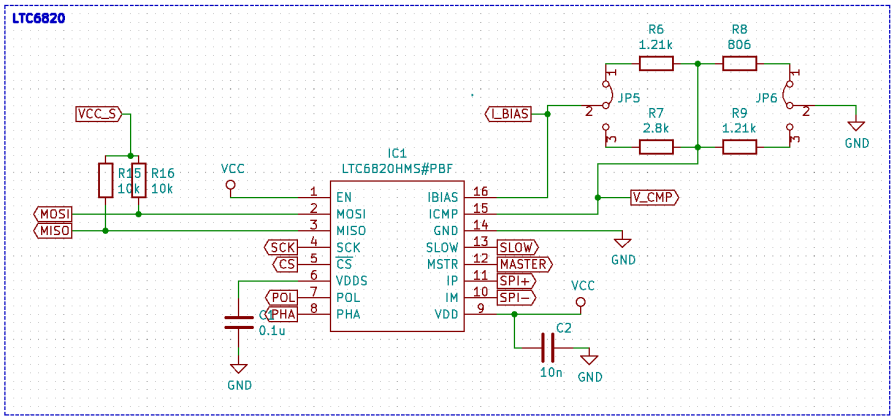


Figure 4.19: LTC6820 schematic part

This schematic part can be seen in figure 4.19.

Can be seen that connected to the IBIAS pin, two branches of resistors have been arranged to create a voltage divider in order to obtain a correct value for the output current level for communication.

The function of the IBIAS pin is explained in details in section 4.3.1.

Pull up resistors have been added on the MISO and MOSI pins for SPI communication because these two outputs of the *LTC*6820 are of the open drain type, therefore they need a resistor to reach the high logic value (indicated with a VCC_S label in the schematic) to avoid having wrong logic values when the internal MOSFET does not go into conduction.

The VDDS pin represents the input threshold voltages of SCK, CS, MOSI, MISO and EN, it can be connected to VDD or to a power supply above or below VDD to shift the SPI I/O level.

It was decided to have a separate SPI level for communication because the Arduino Due logic for this type of communication is 3.3 V, therefore different from $VDD = 5\ V$.

The VDDS pin was therefore bypassed with a capacitor of 0.1 μF as indicated in the datasheet to be able to separate the two references.

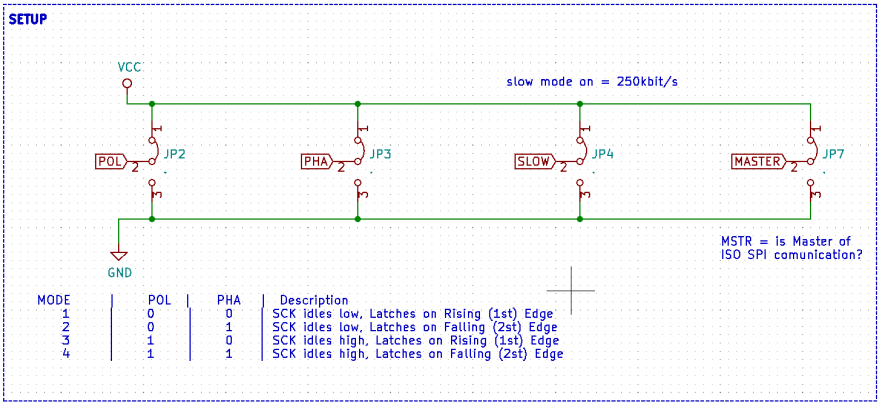


Figure 4.20: Setup schematic part

Table 4.1: SPI Modes based on POL and PHA

MODE	POL	PHA	DESCRIPTION
0	0	0	SCK Idles Low, Latches on Rising (1st) Edge
1	0	1	SCK Idles Low, Latches on Falling (2nd) Edge
2	1	0	SCK Idles High, Latches on Falling (1st) Edge
3	1	1	SCK Idles High, Latches on Rising (2nd) Edge

The schematic part of the SETUP (see 4.20) shows the symbols of the four jumpers necessary for the correct setup of the SPI communication between master and slave.

To go deeply in details, in SPI communication, the master can select the clock polarity and clock phase. This can be set, respectively, using the JP2 and JP3 jumpers shown in 4.20.

The POL pin sets the polarity of the clock signal during the idle state, that is the period when $\overline{CS}$ is high and goes low at the start of the transmission and when $\overline{CS}$ is low and goes high at the end of the transmission.

The PHA pin set the clock phase and determines which edge of the clock, rising or falling, is used to sample the data on the MOSI or MISO lines.

According to how the POL and PHA pins are configured, there are four possible configurations of the SPI communication between master and slave.

These configurations are shown in Table 4.1.

The JP4 jumper, attached to the SLOW label, must be connected to VDD if the clock frequency is less than 200 kHz, while it must be connected to GND if the frequency is higher than 200 kHz.

While, the JP5 jumper that is attached to the MASTER label, must be connected to VDD if the device is on the master side of the isolated interface or to GND if the device is on the slave side of the isolated interface.

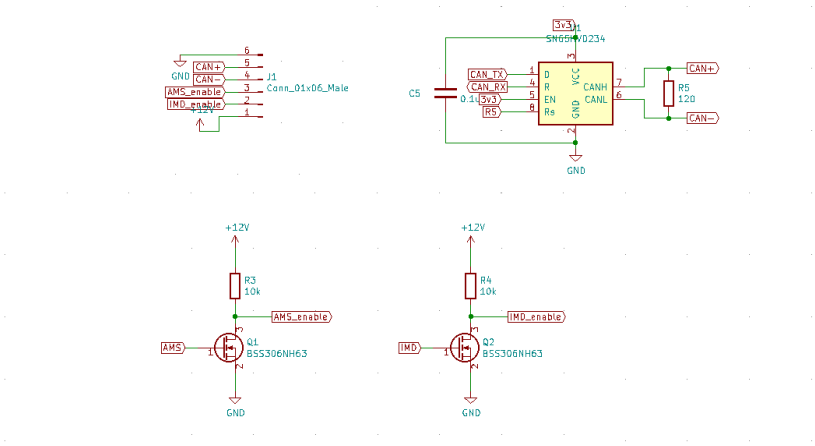


Figure 4.21: Auxiliary schematic part

The COMMUNICATION schematic part shows the symbol of the transformers used to isolate the signals and the symbol of the connector used to connect and allow communication between host and slaves.
R11, R19 and R17 have been set up to possibly correct the impedance on the transmission lines if necessary.
The DEBUG schematic part contains a series of test point and a series of LEDs inserted to make the debug phase more easily and in order to have a visual feedback.

4.3.2.4 *Auxiliary schematic area*

The auxiliary schematic part contains some components that have been installed with the aim of making this BMS Host prototype usable as a partial replacement of the previous Host version and therefore use it in the car to perform tests.
A transceiver $SN65HVD234$ has been used to implement a second CAN line to be used to interface the BMS Host with the car MCU.
While two switches made with an N-MOSFET ($BSS306NH63$) and a resistor have been inserted to check the Accumulator Management System (AMS) and Insulation Monitoring Device (IMD) fault error which in case of anomalies must send a low level signal to the MCU in order to open the SDC.
A connector is used to bring the CAN, IMD and BMS signals to the MCU.
Figure 4.21 shows this part of schematic.

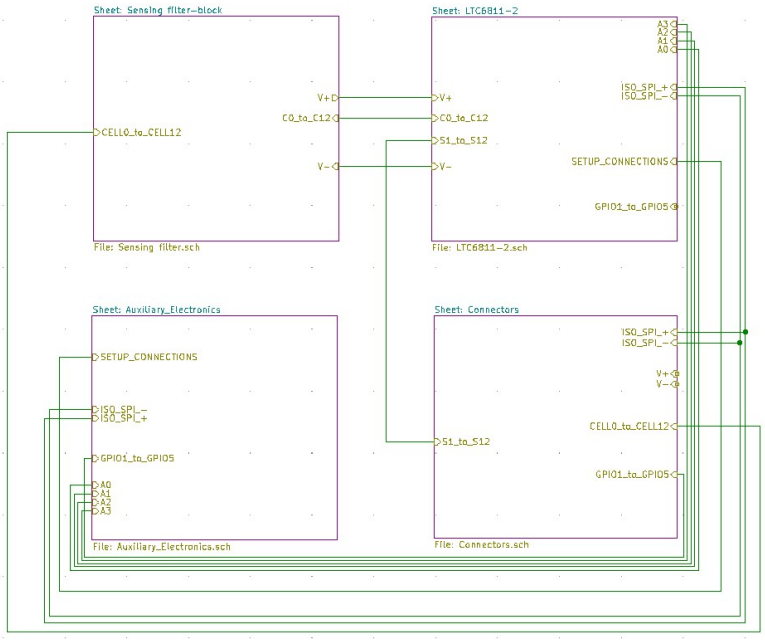


Figure 4.22: BMS slaves worksheet schematic

4.3.3 *BMS Slave*

As previously said, the BMS Slave no longer has any microcontroller on the board.
The main component that characterizes it is the integrated circuit used for the management and monitoring of the voltages and temperatures of the lithium cells that make up the high voltage battery, the $LTC6811-2$.
The schematic describing the operation of the board and the construction of its printed circuit will be analyzed in detail in the following sections.

4.3.3.1 *Schematic analysis*

The schematic of the BMS Slave boards has been divided into four worksheets to facilitate reading and speed up the debug.
These four parts are: Sensing Filters, $LTC6811-2$, Auxiliary Electronics and Connectors.
These four macro-areas and the main connections that link them could be seen in figure 4.22 that shows an overview of the schematic.

4.3.3.2 *Sensing filter schematic area*

To go into the details of each of them, the Sensing filter area, as shown in figure 4.23, contains the labels for the electrical connections of the board and the RC filters composed of a $R = 100\,\Omega$ and $C = 10\,nF$

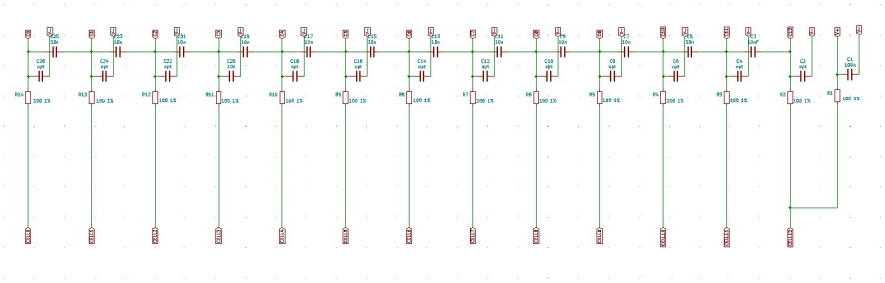


Figure 4.23: BMS Slave Sensing filter schematic area

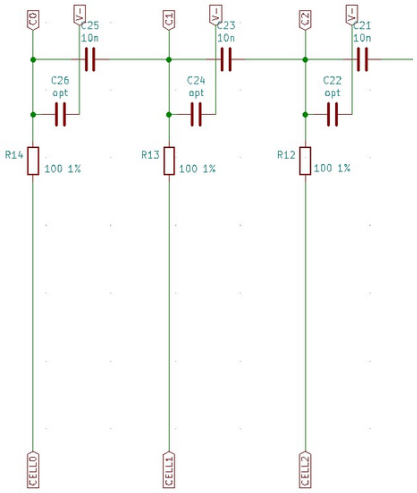


Figure 4.24: Detail of BMS Slave Sensing filter schematic area

that is able to attenuate frequencies higher than its cut off-frequency that is equal to $f_c = \frac{1}{2\pi \cdot R \cdot C} = 159155\ Hz$. They are useful to reduce fast transient noises that could disturb the ADC measurement and could also helps to reject potentially damaging high energy transients. Another optional capacitor is predisposed to each ADC input towards the negative reference if an higher level of battery voltage ripple rejection is required, as recommended by the integrated circuit datasheet. Figure 4.24 shows a macro of the detection filter area for easier viewing of the ADC input RC filters.

The $CELLx$ labels correspond to the voltage detection points while the Cx labels are used to connect the signals to the schematic portion which contains the integrated circuit symbol.

4.3.3.3 *LTC6811-2 schematic area*

In this portion of the schematic there are no particular components, only the symbol of the $LTC6811-2$ in which the various labels are reported in order to make the schematic easier to read.
Figure 4.25 shows the $LTC6811-2$ schematic part. The functions of the related pins of the integrated are described below.

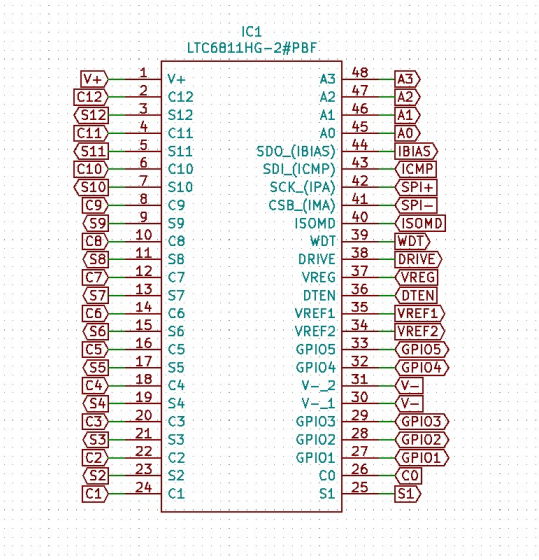


Figure 4.25: LTC6811-2 schematic part

- $V+$ and $V-$ are the positive and negative power pins respectively. These pins are taken from the positive terminal of the higher potential cell of the stack and from the most negative terminal of the lower potential cell. In order to have a correct function of the device, the voltage between these pins must remain between $V+_{min} = 11\ V$ and $V+_{max} = 55\ V$.
  The V+ pin requires voltage greater than or equal to the top cell voltage minus 0.3 V and it provides power to the high voltage elements of the core circuitry.

- $VREG$ is a 5 V input pin. The voltage to this pin must be maintain between $V_{REGmin} = 4.5\ V$ and $VREG_{max} = 5.5\ V$ in order to maintain the accuracy. This input provides power to the core circuitry not powered by V_+ and to the isoSPI circuitry.

- $A3, A2, A1, A0$ are the pins used to address the device. In order to address the device they must be connected to $VREG$ to have an high logical level and to $V-$ to have a low logical level.

- $ISOMD$ is the Serial Interface Mode pin. It is used to choose whether to use the standard 4-wire SPI mode or the 2-wire isolated interface (isoSPI) mode. If this pin is connected to $V-$ set the integrated circuit in 4-wire SPI mode, if it is connected to $VREG$ set the integrated circuit in 2-wire isolated interface mode.

- $SPI+$ and $SPI-$ are the differential input/output pair pins used by the isoSPI communication protocol.

- $IBIAS$ is the pin for the Isolated Interface Current Bias. This pin is 2 V output when the isoSPI interface is enabled. The $SPI+$

and $SPI-$ output current drive is set to 20 times the current I_B sourced from $IBIAS$ pin. Using a resistor divider is possible to set the isoSPI signal amplitude to allow the system to carry out a trade-off between power consumption and noise immunity for communication robustness.

- $ICMP$ this pin is the Isolated Interface Comparator Voltage Threshold Set and connecting this pin to the voltage divider between $IBIAS$ and $V-$ allow to set the threshold voltage of the isoSPI receiver comparator.
- WDT is the watchdog timer output pin and consist of a open drain NMOS digital output. It can be left unconnected or connected with a 1 $M\Omega$ resistor to $VREG$. This watchdog timer circuit is useful because if the $LTC6811$ does not receive a valid command within 2 seconds, it will reset the device and the WDT pin will go high impedance.
- $DRIVE$ this pin is 0 V when the device is in a $SLEEP$ State. This can be useful to drive a $ENABLE$ pin of another integrated circuit in order to drive it in power save mode.
- $VREF1$ is the ADC reference voltage pin.
- $VREF2$ is the second reference voltage pin. This pin is $3V$ nominal.
- $GPIO1, GPIO2, GPIO3, GPIO4$ are general purpose input/output pins. They can be used as digital inputs or digital outputs, or as analog inputs with a measurement range from $V-$ to 5 V. In this they are used as inputs to read the voltage across the Negative Temperature Coefficient Thermistor (Negative Temperature Coefficient (NTC)).
- $C0 - C12$ are the cell voltage input pins and comes from the Sensing filter schematic area.
- $S1 - S12$ are the balance input/output pins. They can be used as inputs for cell discharging because there are 12 internal N-MOSFET connected between $S(n)$ and $C(n-1)$ pins, able to discharge up to 60 mA. Balancing with current larger than 60 mA is not recommended for the internal switches due to excessive die heating. These pins can act as digital outputs suitable for driving the gate of an external MOSFET used for cell discharging.

4.3.3.4 *Auxiliary Electronic schematic area*

In this part of the schematic can be found all the auxiliary electronics used to ensure the correct operation of the $LTC6811-2$ and the desired behaviour of the device.

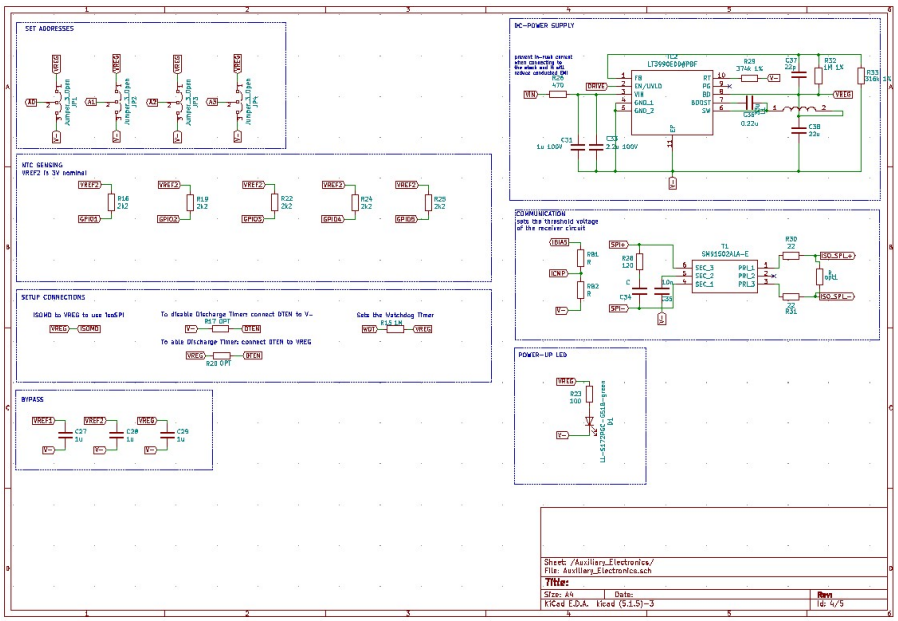


Figure 4.26: Auxiliary-Electronics schematic area

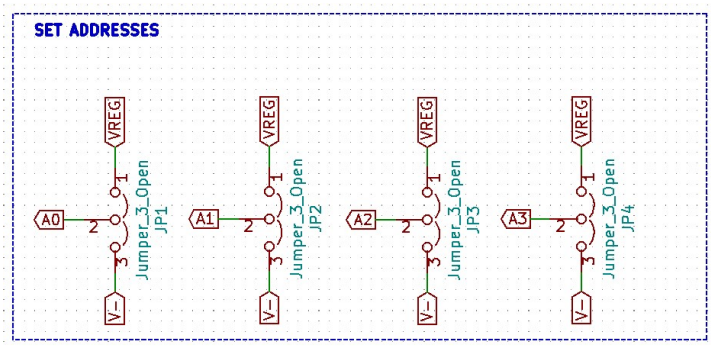


Figure 4.27: SET ADDRESSES schematic part detail

Figure 4.26 shows the Auxiliary-Electronics schematic part. This part of the diagram is divided into seven macro blocks for easier reading. These blocks are: SET ADDRESSES, DC-POWER SUPPLY, NTC SENSING,COMMUNICATION, SETUP CONNECTIONS, BYPASS, POWER-UP LED.
The SET ADDRESSES schematic part is a simple part and is needed in order to connect the addresses pins, $A0, A1, A2, A3$ to $VREG$ which allows having logic 1 level or to $V-$ for a logic 0 level. The addressing of these pins permits to address $4^2 = 16$ different addresses because there are 4 pins with 2 possible combinations each. To allow this type of connection a 3-position SMD Normally Open (NO) jumper symbol was used.
Figure 4.27 shows this schematic part in detail.
The schematic part of DC-POWER SUPPLY describes the circuit part necessary for the correct power supply of the device present in the board.

As previously mentioned, the type of power supply needed by the $LTC6811-2$ is of two types, the first, the one supplied to pin $V+$ supplies power to the high voltage elements of the circuit, while the second, supplied to the $VREG$ pin supplies power to the remaining main circuit and isoSPI circuit. This last type of power supply is the one described in the schematic part $DC-POWER\ SUPPLY$.
In order to deliver the stable 5 V to the $VREG$ pin, multiple options could be used.
The first option recommended in the datasheet is the one shown in figure 4.28, where to provide a stable 5 V power supply to the device, the $DRIVE$ pin is used to make a voltage regulator by means of an NPN transistor. The $DRIVE$ pin, connected at the transistor base, is capable of providing a voltage of 5.7 V with 1 mA of current. When it is buffered with an NPN transistor it is able to provide a stable 5 V. In the schematic representation (see 4.28) can be seen an RC filter, useful to protect the NPN transistor from transients.
The transistor must have good current gain h_{FE} (or $\beta = \frac{I_C}{I_B}$) to provide the supply current required for the $LTC6811-2$ to function properly. Considering that the $VREG$ pin is not used to power additional circuits, the peak current demand is given to the worst-case during isoSPI communication and simultaneous ADC conversions, during which the $LTC6811-2$ requires a peak power supply of about $30mA$.
There are many transistors considered for this use, such as the $NSS1C201LT1G$ produced by $ONSEMI$, the $DXTN07100BP5$ produced by *Diodes Incorporated* or the $PHPT61002NYCLH$ produced by *Nexperia*. All these devices would have the correct ratings regarding voltage, current and power, however the problem of using transistors for this type of use is that of the thermal characteristic. More precisely, the voltage at the collector would be taken at the positive terminal of the cell with a higher potential present in the module, therefore at a maximum voltage that can vary from $4.2\ V \cdot 12 = 50.4\ V$ to $4.45\ V \cdot 12 = 53.4\ V$ based on the type of lithium cells used. This, during normal use, would lead to a significant increase in temperature, leading to possible damage to the component itself and a potential destructive chain reaction for the devices powered or present near this component.
For example, the $DXTN07100BP5$ transistor manufactured by *Diodes Incorporated* has a junction-to-ambient thermal resistance that varies from $39°C/W$ to $169°C/W$ depending on the size and type of dissipation surface used.
Making an approximate calculation, using a thermal resistance ($R_{\theta JA}$) equal to $75°C/W$ which corresponds to that provided in the product datasheet with the device mounted with the exposed collector pad on $25mm \times 25mm$ 1 $oz\ of\ copper$, the device, considering the

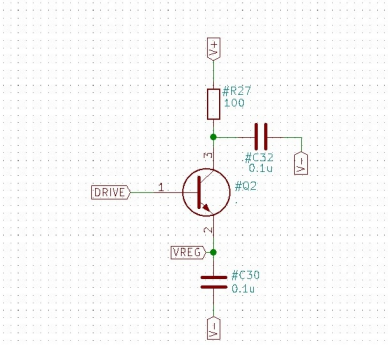


Figure 4.28: DC power supply with BJT

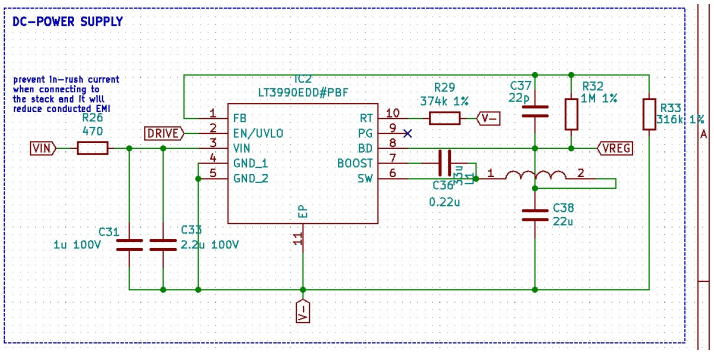


Figure 4.29: DC power supply with LT3990

working environment at a temperature of $R_a = 25°C$, would reach a temperature of:

$$T_d = R_a + R_{\theta JA} \cdot P = 75°\ C/W \cdot (12 \cdot 4.2\ V \cdot 0.03\ A) =$$

$$= 25°C + 113.4°C = 138.4°C$$

Considering that the maximum operating temperature of the component is $150°C$ and that the environment in which it will operate will often be at a temperature above $25°C$, the solution to supply power to the $LTC6811-2$ with this type of solution has been excluded.

The second option recommended in the datasheet is the one shown in figure 4.29 where an integrated circuit, the $LT3990$ that is produced by Analog Devices, is used to supply power to the device. This device is a step-down (buck type) regulator with the possibility to adjust the switching frequency.

The functions of the pins of this device are described below.

- VIN is the positive power pin. This pin supplies current to the internal circuitry and to the internal power switch of the device. To have a correct function of the device, the voltage between this pin and the negative reference must remain between

$VIN_{min} = 4.2\ V$ and $VIN_{max} = 62\ V$. In this project this pin is connected to the positive terminal of the higher potential cell through a resistance $R26 = 470\ \Omega$ to prevent in-rush current when connecting the PCB to the stack and to reduce conducted EMI.
For this project, the minimum applicable input voltage is determined from both the device minimum operating voltage of $4.2\ V$ and by the maximum duty cycle $DC_{max} = 1 - f_{sw} \cdot t_{OFF,min}$ ($t_{OFF,min}$ is the minimum switch-off time, see 4.31).
So, the minimum voltage applicable to the input due to duty cycle for a buck converter is:

$$V_{IN,min} = \frac{V_{OUT} + V_D}{1 - f_{sw} \cdot t_{OFF,min}} - V_D + V_{SW}$$

Where V_{OUT} is the output voltage, V_D is the integrated catch diode drop, typically near to $0.7\ V$, and V_{SW} is the internal switch drop, equal to $0.5\ V$.
The minimum input voltage turns out to be equal to:

$$V_{IN,min} = \frac{5\ V + 0.7\ V}{1 - 400\ kHz \cdot 160\ ns} - 0.7\ V + 0.5\ V = 5.889\ V$$

Also the maximum input voltage during normal operation is due to minimum duty cycle $DC_{min} = f_{sw} \cdot t_{On,min}$ ($t_{ON,min}$ is the minimum switch-on time, see 4.31).
The highest allowed input voltage during normal operation can be calculated as:

$$V_{IN,OP-max} = \frac{V_{OUT} + V_D}{f_{sw} \cdot t_{ON,min}} - V_D + V_{SW}$$

and turns out to be equal to:

$$V_{IN,OP-max} = \frac{5\ V + 0.7\ V}{400\ kHz \cdot 225ns} - 0.7\ V + 0.5\ V = 63.53\ V$$

With the output voltage and switching frequency values chosen for this project, the value of $V_{IN,OP-max}$ obtained is greater than the maximum sustainable voltage VIN, max of the input device, therefore the maximum voltage that can be imposed on the VIN pin of the $LT3990$ is equal to $62\ V$.
However, the device would be able to withstand input voltages higher than the value just calculated up to the declared maximum voltage nominal value (equal to $VIN_{max} = 62\ V$). During transients where VIN is higher than $V_{IN,OP-max}$, the switching frequency is reduced below the programmed frequency to avoid causing damage to the IC.
The ripple of the output voltage and ripple of the inductor cur-

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.2	787
0.3	511
0.4	374
0.5	287
0.6	232
0.8	169
1.0	127
1.2	102
1.4	84.5
1.6	69.8
1.8	59
2.0	51.1
2.2	44.2

Figure 4.30: Switching Frequency vs RT Value [8]

rent may also be higher than in typical operation but the output will still be regulated.

- $GND1$ and $GND2$ are the negative power pins.
- $EN/UVLO$ is the enable pin that allows the device to enter in power save mode when the voltage applied to this pin is lower than 1.19 V. This pin is connected to the $DRIVE$ pin of the $LTC6811-2$ which will put the $LT3990$ into a low power state when the $LTC6811$ is in the $SLEEP$ state.
- RT this pin is used to set the switching frequency of the device. The resistor is tied between this pin and the negative reference. Figure 4.30 shows the resistor value to choose to have the corresponding switching frequency value of the device.
  The choice of the switching frequency is a trade-off between efficiency, component size and maximum input voltage. From datasheet and the buck equation results that the maximum acceptable switching frequency for a certain type of application can be calculated by:

$$f_{SW,max} = \frac{V_{OUT} + V_D}{t_{ON,min} \cdot (V_{IN} - V_{SW} + V_D)}$$

Where V_{OUT} is the output voltage, V_D is the integrated catch diode drop, typically near to 0.7 V, V_{SW} is the internal switch drop, equal to 0.5 V, V_{IN} is the typical input voltage and $t_{ON,min}$ is the minimum switch-on time. In this project the maximum acceptable frequency results equal to:

$$f_{SW,max} = \frac{5\ V + 0.7\ V}{225\ ns \cdot (12 \cdot 4.2\ V - 0.5\ V + 0.7\ V)} = 500.66\ kHz$$

Where, $t_{ON,min}$ has been chosen equal to 225 ns, which corresponds to the value of the switch-on time at the temperature of 150°C, because it corresponds to the worst case, this value is taken from the characteristic curve in the datasheet of the device

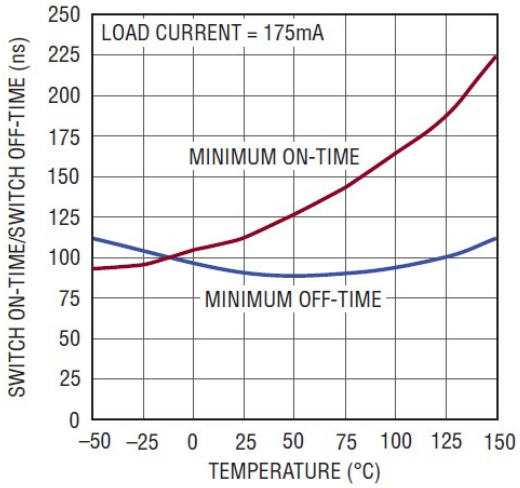


Figure 4.31: Minimum switch-on time and switch-off time vs temperature [8]

which shows how the minimum switch-on and switch-off times vary as the temperature varies.
This curve can be seen in figure 4.31.
Also the power supply voltage V_{IN} value has been choosen equal to $12 \cdot 4.2\ V$ because it is the maximum input voltage reachable from the series of 12 cells.
In the light of these considerations, the R_T resistance value chosen is that equal to 374 $k\Omega$ which corresponds to a switching frequency equal to 400 kHz.

- BD this pin supplies current to the device internal regulator when BD is above $3.2V$ and connects to the anode of the boost diode.

- FB this pin is regulated to 1.21 V by the device and the feedback resistor divider must be connected to this pin. This resistor divider is needed to set the output voltage, and in order to choose the resistor values the following equation for a voltage divider has been used:

$$R_1 = R_2 \cdot (\frac{V_{OUT}}{1.21} - 1)$$

So the $LTC6811-2$ need 5 V input voltage supply and choosing large resistors will decrease the quiescent current of the application circuit. The first resistor value chosen is: $R_2 = 316\ k\Omega$, so:

$$R_2 = 316\ k\Omega \cdot (\frac{5\ V}{1.21\ V} - 1) = 989.78\ k\Omega$$

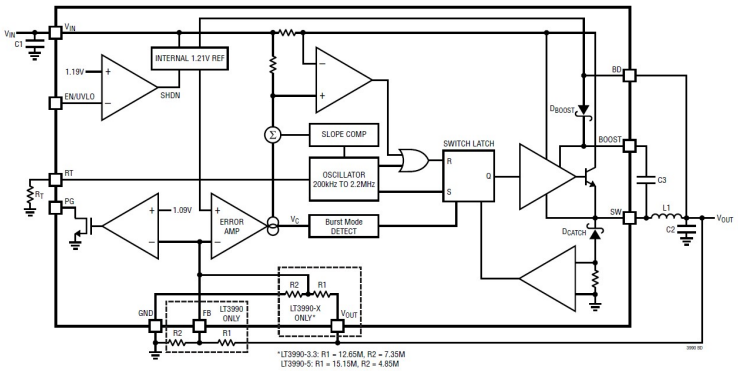


Figure 4.32: LT3990 internal structure representation [8]

so the closest commercial value is $R_1 = 1\ M\Omega$, these resistors values guarantee an output voltage of the device equal to:

$$V_{OUT} = (\frac{R_1}{R_2} + 1) \cdot 1.21\ V = 5.04\ V$$

- PG this is the open-drain output of an internal comparator. This pin is valid when the voltage at the positive power pin , VIN,is above 4.2 V and the pin $EN/UVLO$ is high. Moreover, this pin remain low until FB pin is within 10% of the final regulation voltage.
- $BOOST$ this pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch.
- SW this pin is the output of an internal power switch.

The $LT3990$ internal structure is represented in figure 4.32.
For the correct power supply of the $LTC6811-2$, the must supply a constant output voltage of 5 V with a deviation from this value of a maximum of half volt. It can therefore reach a maximum of $V_{OUT,max} = 5.5\ V$ and a minimum of $V_{OUT,min} = 4.5\ V$.
To ensure this, the choice of components for the $LT3990$ is crucial especially for the inductor and the output capacitance. These two components, in fact, have a fundamental role in determining the ripple on the output voltage.
For the inductor, the higher is its value, the higher is the maximum output current because of the reduced ripple current and, in general, the lower the inductor value, the smaller is the solution size. The device datasheet suggests using a $L = 33\ \mu H$ value for the inductor, therefore it was decided to follow this suggestion and to do a simulation to choose the correct inductor to obtain the best compromise between price, size and performance.
The output capacitor chosen is the 22 μC ceramic type with $X5R$

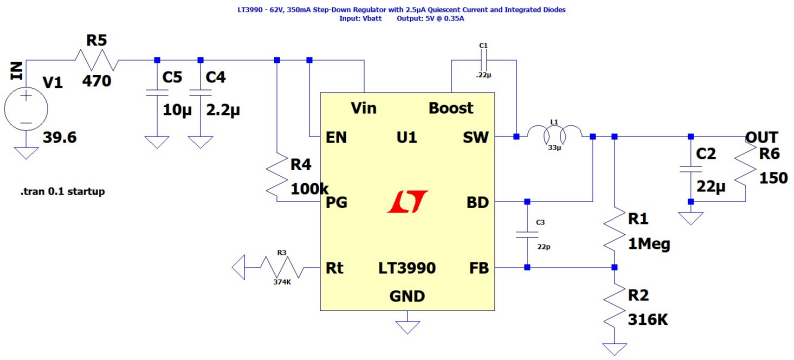


Figure 4.33: LT3990 PSpice simulation schematic

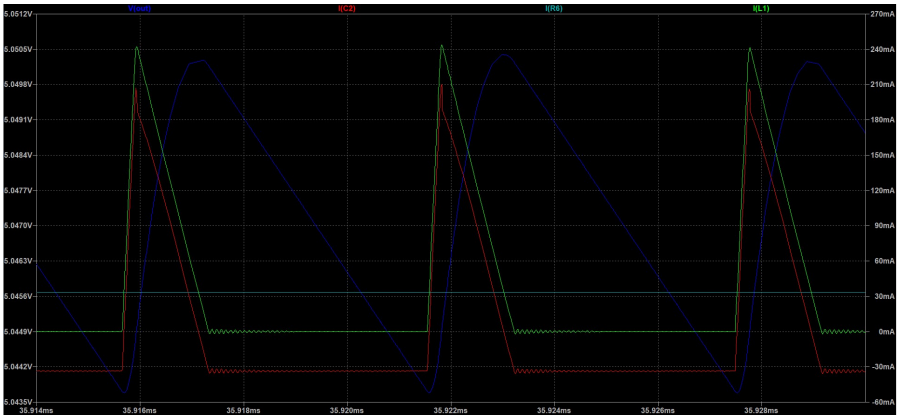


Figure 4.34: LT3990 PSpice simulation results

dielectric material, so it is able to operate from a minimum temperature of $-55°C$ to $+85°C$ and the change of its capacitance over the temperature range is $\pm 15\%$.
Figure 4.34 shows the inductor current ripple (highlited in green) that is $I_{L,peak} = 240\ mA$, the output capacitor current and the output voltage that deviates from mean output value of $\Delta V_{OUT} = 0.05\ V$.The simulations of the power supply circuit created with the $LT3990$ as described in the figure 4.29 are shown below.
The simulations were carried out using the LTSpice software simulator, the simulation circuit is shown in figure 4.33.
This simulation values were obtained with input voltage of $V_{IN} = 36.9\ V$
The values obtained are not taken as truthful but as guidelines for a more targeted design, the graphs obtained during the test phases are also shown below to confirm or not these results.
The input of the $LT3990$ is bypassed with a ceramic capacitors of $X7R$ which, in contrast to $X5R$ type, can withstand a working temperature up to $+125°C$. Two capacitors have been prepared, respectively from 2.2 μF and 10 μF in the case of only one is not able to manage the

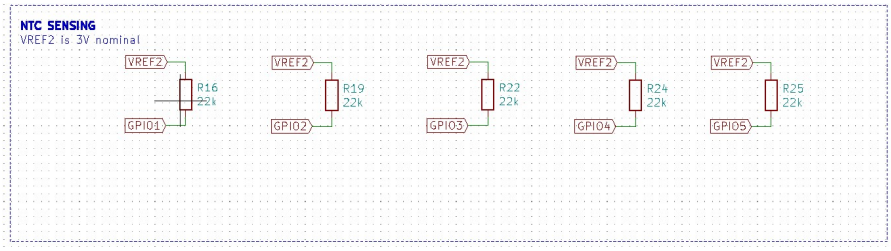


Figure 4.35: Detail of NTC SENSING schematic part

incoming ripple voltage. When the device is powered by an already powered source, the current flowing at the input must be limited in order not to exceed the component ratings, as previously mentioned, a series resistor has been set up to limit this current.
The *NTC SENSING* schematic part represents the circuit part necessary for detecting the cell temperatures.
Figure4.35 shows *NTC SENSING* schematic part in detail.
The *NTC* sensors have a temperature coefficient lower than zero, which means that as the temperature increases, their resistance decreases.
In order to read the cells temperatures, the 5 available General Purpose Input/Output (GPIO)s of the $LTC6811-2$ are used as analog inputs for the detection and reading of the voltages coming from the circuit created with the NTCs. Such a circuit is made from a simple resistor divider where the first terminal of the first resistor is connected to the voltage reference pin, $VREF2$ that provides 3 V, and taking the voltage reference for conversion via the ADCs to the second terminal of this resistor. This last connection point is connected to the NTC sensor connector, depicted in the schematic with the $GPIOx$ label, where is connected one of the two sensor terminals while the other is linked to the system negative voltage reference $V-$.
Since these devices are always powered during normal operation of the device, 100 $k\Omega$ NTCs were chosen instead of the 10 $k\Omega$ ones used more frequently, so as to consume less energy for the power supply and related circuit readings. The resistance to make the voltage divider with the sensor was chosen of $22 \pm 1\%$ $k\Omega$ to have a good compromise between reading and circuit consumption.
It is necessary to use at least 4 GPIOs to read the voltage level of the temperature because the competition rules require the monitoring of the temperature of at least 30% of the cells equally distributed within the TSAC. Since the device used in this project for managing cell temperatures and voltages monitors 12 cells in series, at least 3.6 cells, rounded to 4, must be monitored.
For a safety factor, it was also chosen to use the fifth GPIO as an analog input for reading the voltage relative to the temperature.
By doing this, approximately 40% of the cells for each slave are monitored.

The resistance of this type of sensor changes according to the decreasing exponential law reported below:

$$R_T(T) = R_0 \cdot exp(B \cdot \frac{T_0 - T}{T_0 \cdot T}) = R_0 \cdot exp(B \cdot (\frac{1}{T} - \frac{1}{T_0}))$$

where $R_T(T)$ is the resistance of the thermistor at the generic temperature T, R_0 is the resistance of the thermistor at the temperature of $T_0 = 25°C$, B is a characteristic dimensional constant of the thermistor and is within the interval of $2000 : 5500\ K$ depending on the sensor type and T_0 is the reference temperature given by the manufacturer expressed in K.
The sensor considered for the development of this project is the $NJ28RA0104H$ produced by $Kyocera\ AVX$, it has $AEC - Q200$ based qualification, designed for automotive applications with an high accuracy and a fast thermal response.
The values of the parameters indicated above for this type of sensor are:

- $R_0 = 10\ k\Omega$;
- $T_0 = 25°C$;
- $B25/85 = 4380\ \pm\ 1\%\ K$;

The $B25/85$ parameter is determined by the ceramic material with which the component is made and represents the slope of the R/T curve and it can be expressed by the formula:

$$B25/85 = \frac{T \cdot T_R}{T - T_R} \cdot ln(\frac{R_R}{R_T}) = \frac{25°C \cdot 85°C}{25°C - 85°C} \cdot ln(\frac{R_{(T=25°C)}}{R_{(T=85°C)}})$$

$$B25/85 = 1779.7 \cdot ln(\frac{R_{(T=25°C)}}{R_{(T=85°C)}})$$

For this value of B the datasheet indicates a tolerance of $\pm 1\%$, therefore, the respective values are:

$$B25/85_H = 4380\ K \cdot 1.01 = 4423.8\ K$$

$$B25/85_L = 4380\ K \cdot 0.99 = 4336.2\ K$$

The $LTC6811 - 2$ datasheet indicates a maximum error of $2.2\ mV$ for voltages of $3\ V$ at the input of the $GPIOx$ pins referred to the negative reference $V-$. The reading error at a temperature of $60°C$ is of particular interest because it is the maximum temperature that the cells can reach and the temperature at which the shutdown circuit must be opened if this temperature is exceeded for more than 1 second. From the datasheet of the NTC sensor it results that the values of the resistances at a temperature of $60°C$ are:

$$R_{60,H} = 22.818\ k\Omega$$

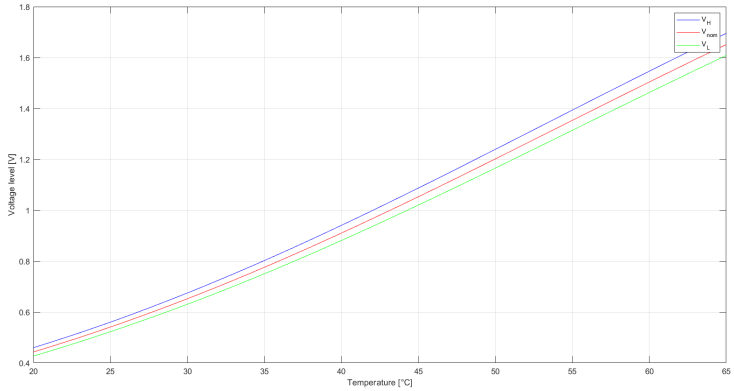


Figure 4.36: GPIO input voltage range for NTC sensors vs Temperature

$$R_{60,L} = 20.955\ k\Omega$$

The voltage read by the $GPIOx$ pins also depends on the voltage supplied at the output by the $VREG2$ pin, which can assume the following variations:

$$VREF2_H = 3.005\ V$$

$$VREF2_L = 2.995\ V$$

The voltage read by the device on the voltage divider may fluctuate from a minimum to a maximum of:

$$V60_H = VREF2_H \cdot \frac{22\ k\Omega \cdot 1.01}{22\ k\Omega \cdot 1.01 + R_{60,L}} =$$

$$= 3.005\ V \cdot \frac{22.22\ k\Omega}{22.22\ k\Omega + 20.955\ k\Omega} = 1.5465\ V$$

$$V60_L = VREF2_L \cdot \frac{22\ k\Omega \cdot 0.99}{22\ k\Omega \cdot 0.99 + R_{60,H}} =$$

$$= 2.995\ V \cdot \frac{21.78\ k\Omega}{21.78\ k\Omega + 22.818\ k\Omega} = 1.4626\ V$$

The GPIO inputs have the $-0.82\ V$ to $+5.73\ V$ resolution range, with the negative readings rounded to $0\ V$. The data input has $16 - bit\ unsigned\ integer$ where the LSB represents $100\ \mu V$.
Therefore the voltage variation due to the voltage divider for reading the temperature of the NTC sensors can vary according to the tolerances of the components used from a maximum to a minimum level. These possible values are observable from the figure 4.36 in which these two levels are shown in a temperature range from $20°C$ to $65°C$. The manufacturing tolerances of the resistances used in the voltage divider were also taken into consideration in this calculation. To ob-

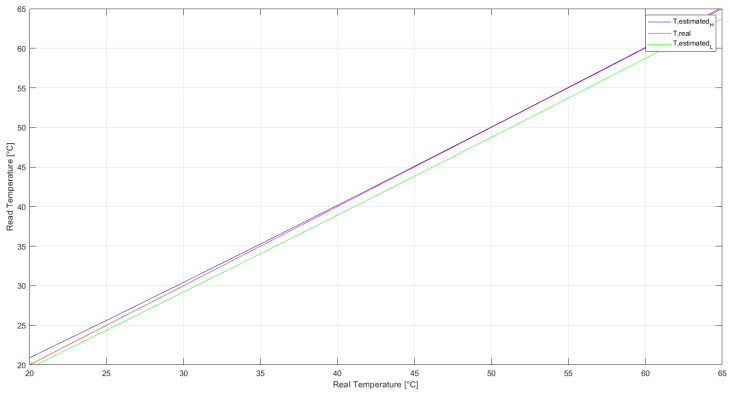


Figure 4.37: NTC Real vs Read temperature

tain the corresponding temperature for these values, it is necessary to invert the exponential formula of the NTC sensor:

$$T_{estimated,H} = \frac{1}{\frac{1}{T_0} + \frac{1}{B25/85_H} \cdot ln(\frac{R_{60,L}}{R_0})}$$

$$T_{estimated,L} = \frac{1}{\frac{1}{T_0} + \frac{1}{B25/85_L} \cdot ln(\frac{R_{60,H}}{R_0})}$$

The difference between the read and the real temperature of the NTC sensor regarding the maximum and the minimum temperatures due to the various tolerances of the components that can be obtained can be seen in the figure 4.37.
The maximum reading error that can be made at a temperature of $60°C$ is about $1.28°C$, it will be necessary to take this error into account during software implementation in order to correct this offset and not allow the cells to reach and exceed the critical temperature.
As mentioned above, this type of configuration offers a good compromise between reading range and consumption which are very low, below there are the calculations that shows this consumptions:

$$I_{min} = \frac{VREF2_L}{22\ k\Omega \cdot 1.01 + R_{-55,H}} = \frac{2.995\ V}{22220\ \Omega + 12359857\ \Omega} = 241.88\ nA$$

$$I_{max} = \frac{VREF2_H}{22\ k\Omega \cdot 0.99 + R_{150,L}} = \frac{3.005\ V}{21780\ \Omega + 1036\ \Omega} = 131.70\ \mu A$$

Considering that the usual temperature range during which track tests or competitions are carried out are usually summer, therefore around an ambient temperature of $T_{amb} = 30°C - 35°C$, it can be considered that the consumption given by the circuits for detecting the temperature of the cells is around 10 nA and therefore can be considered almost negligible.
The *SETUP CONNECTIONS* schematic part (4.38) contains all the

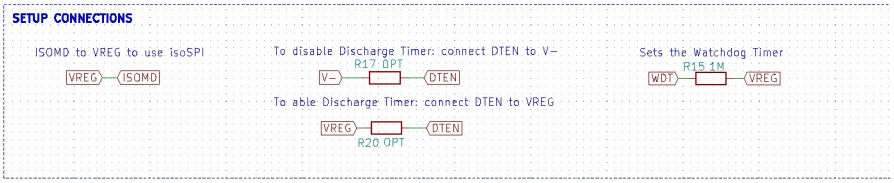


Figure 4.38: SETUP CONNECTIONS schematic part

connections necessary to correctly configure the device for this specific use.
In particular the label indicated with $VREG$ is directly connected with the label indicated with $ISOMD$ in order to configure the use of the isoSPI.
The label indicated with $DTEN$ is connected to $VREG$ with an optional resistor ($R17$) in order to enable the discharge timer, and to $V-$ (with $R20$) to be able to disable it for any future reconsiderations. It will be necessary to be very careful not to solder both resistors to avoid having a short circuit between $VREG$ and $V-$.
The WDT label is connected to $VREG$ with a 1 $M\Omega$ resistor in order to possibly set the watchdog timer, as previously mentioned, if the $LTC6811-2$ does not receive a valid command within two seconds, the watchdog timer will reset the device and the watchdog pin will go into high impedance.
The $COMMUNICATION$ schematic part (4.39) shows how the isoSPI communication circuitry has been implemented.
The schematic shows the isolation provided by the transformer and the two resistors that compose the voltage divider needed to provide the correct value of isoSPI transmitter drive current.
This current value controls the isoSPI signaling currents and must be chosen carefully in order to ensure the right balance between power consumption and noise immunity. It can be choose in a range from 100 μV to 1 mA by carefully choosing the bias resistances named with $RB1$ and $RB2$ in 4.39 and powered by $IBIAS$ pin that provide 2 V when the isoSPI interface is enabled. The voltage divider is connected to the $ICMP$ pin, which sets the comparator threshold V_{TCMP} to 1/2 of this voltage V_{ICMP}. The IP and IM pins drive currents are $20 \cdot IB$.
The datasheets report that for most applications setting $IB = 0.5\ mA$ is a good compromise between power consumption and noise immunity for systems with a transmission cable up to 50 m, as in our case, but considering the type of environment in which the system will work and especially considering the problems due to the electromagnetic interferences generated by the inverters that occurred during the last season, it was decided to use a $IB = 1\ mA$ to promote noise immunity to interferences at the expense of power consumption.
The values chosen for the bias resistors are respectively:

$$RB1 = 1.21\ k\Omega$$

$$RB2 = 806\ \Omega$$

With these resistance values we obtain that the bias current is equal to:

$$IB = \frac{VBIAS}{RB1 + RB2} = \frac{2\ V}{1.21\ k\Omega + 806\ \Omega} = 992\ \mu A \simeq 1\ mA$$

and therefore the drive current is equal to:

$$I_{DRV} = IP = IM = 20 \cdot IB = 20\ mA$$

The comparator threshold V_{TCMP} results equal to:

$$V_{TCMP} = 1/2 \cdot V_{ICMP} = 1/2 \cdot (2\ \cdot \frac{RB2}{RB1 + RB2}) =$$

$$= 0.5 \cdot (2\ V \cdot \frac{806\ \Omega}{806\ \Omega + 1.21\ k\Omega}) = 0.5 \cdot (0.8\ V) = 0.4\ V$$

This means that the pulse drive current I_{DRV} will be 20 mA and the receiver comparators will detect pulses with $VIP - VIM$ amplitudes greater than 400 mV (see figure 4.15).
For the choice of the transformer, the guide proposed by the $LTC6820$ and $LTC6811 - 2$ datasheets were followed. In particular, in order to be able to transmit with the necessary fidelity the signals with pulse amplitudes up to $VA = 1.6\ V_{P-P}$ and pulse widths of 50 ns and 150 ns (as described in 4.3.1.1), the system requires that the transformer have primary inductances above 60 μH, a $1:1$ turn ratio and a leakage inductance less than 2.5 μH.
The value of the primary inductance turns out to be very important as it will mostly affect the pulse droop of the 50 ns and 150 ns pulses. If the primary inductance is too low, the pulse width will begin to decrease and decay during the pulse period, if this decrease is significant, the actual pulse width seen by the receiver will substantially decrease causing a reduction in pulse margin error which can lead to incorrect conversions and propagation of errors.
On the other hand, the leakage inductance mainly affects the rise and fall times of the pulses, in fact, if too slow, they will drastically reduce the pulse amplitude leading, in the worst cases, to not reaching the comparator threshold voltage V_{ICMP} for detection of the correct logic level. For this reason, it is best to keep pulse edges as fast as possible.
For common-mode noise rejection, a center-tapped transformer was chosen where, the center tap has been connected by a 10 nF capacitor to GND (as shown in figure 4.39)
One more important aspect to take into account is the isolation rating for the application. To have a conservative situation, the working voltage that the component must withstand has been matched to the total voltage of the battery pack (maximum of 600 V by regulation). Also by regulation, it is necessary to guarantee galvanic isolation between parts that can potentially become high voltage and low voltage parts,

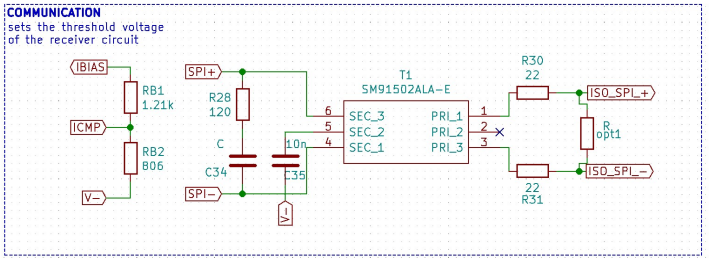


Figure 4.39: COMMUNICATION schematic part

for this specific rule, two components are understood as correctly galvanically isolated if all of the following are true:

- the resistance between both circuits is $\leq 500\frac{\Omega}{V}$, related to the maximum TS voltage of the vehicle, at a test voltage of maximum TS voltage or 250 V, whichever is higher.
- the withstand voltage between both circuits is higher than three times the maximum TS voltage or 750 V, whichever is higher.

Especially for the second constraint mentioned it means that in our case, since the voltage of the battery pack is about 600 V, an insulation of at least 3 times this voltage must be guaranteed for a total therefore of 1800 V.
The transformer chosen is the $SM91502ALA$ produced by $BOURNS$ and offers the following values for the parameters described above:

- $AEC-Q200$ compliant
- primary inductance from 150 μH;
- maximum value of leakage inductance equal to 0.5 μH
- working voltage of 1000 V_{DC}
- correct electrical insulation up to 4300 V_{DC}

The $BYPASS$ schematic part (4.40) contains all byass capacitors from $VREF1$, $VREF2$ and $VREG$ to route AC signals to $V-$.
The $POWER-UP\ LED$ schematic part (4.41) contains a simple LED power circuit, which has the primary purpose of providing visual feedback if power to the $LTC6811-2$ is properly supplied. The chosen LED has a Continuous Forward Current $I_F = 30\ mA$, which corresponds to a drop of about $V_F = 2\ V$. To limit the current flowing in the LED and avoid burning it, has been used a resistor with a value equal to:

$$R_{min} = \frac{(V_{REG,max} - V_F)}{I_F} = \frac{(5.5\ V - 2\ V)}{30\ mA} = 116.7\ \Omega$$

The chosen resistance is $R = 150\ \Omega$ which allows a maximum current of:

$$I_{F,max} = \frac{(V_{REG,max} - V_F)}{R} = \frac{5.5\ V - 2\ V}{150\ \Omega} = 23.3\ mA$$

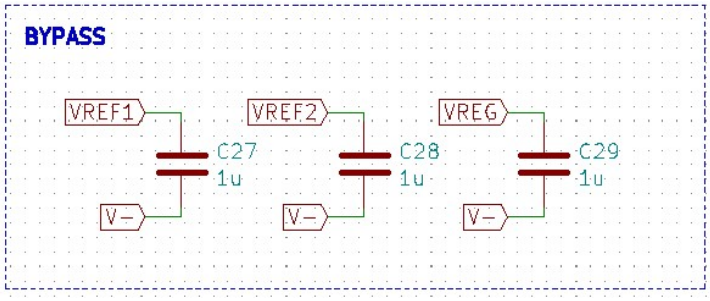


Figure 4.40: BYPASS schematic part

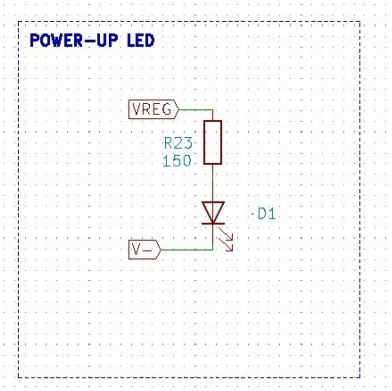


Figure 4.41: Power-on LED schematic

The maximum power that can be dissipated by the LED is $P_{max} = 72\ mW$, while, in these conditions of use, the dissipated power is equal to:

$$P = V_{LED,max} \cdot I_F = 2.4\ V \cdot 23.3\ mA = 55.92\ mW < P_{max} = 72\ mW$$

4.3.3.5 *Connectors schematic area*

In this part of the diagram can be found all the labels that correspond to the various signals that go to the 3 connectors on the board in order to allow you to have input or output signals.
The connector shown on the left in the figure 4.42 is used as a connector for the isoSPI communication signals, named with ISO_SPI+ and ISO_SPI-. While the other two connectors are necessary to detect the voltages coming from the cells, named with Cx, to be able to control the p-MOSFETs used to allow the passive balancing of the cells, named with Sx, and to detect the voltages coming from the NTC thermistors for the detection of cell temperatures, named with $GPIOx$.

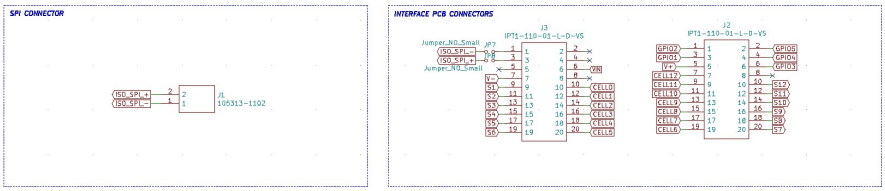


Figure 4.42: Detail of connectors schematic area

4.3.4 *BMS Slave PCB layout*

The geometry for this BMS Slave PCB was chosen to be as small and solid as possible, the result is a rectangle of 45 mm height and 70 mm width.
A render of the BMS Slave PCB can be seen in figure 4.43 The idea was to create the voltage and temperature management system on two levels, the first formed by this board while the second formed by an interface board on which the PCB, which will be analysed in this section, will be plugged.
The interface PCB will be analysed later (see 4.4).
This type of architecture offers the possibility to work on the board that present a greater number of elements during the debug phase without having to assemble and disassemble the entire battery segment each time.
This offers a considerable saving in terms of time and minimizes the possibility of accidental short circuits due to maintenance on the segment because it would only be an unplugging procedure of a PCB from another PCB.
The fastening system between the two boards is done through the use of two connectors with 20 contacts each, arranged in two rows, each with 10 contacts. The connector being referenced is the $IPT1-110-01-L-D-VS$ manufactured by SAMTEC. This offers a standard pitch of 2.54 mm, an insulation voltage between the individual contacts is guaranteed up to 1095 V_{DC} and the contacts are individually shrouded, this minimizes the possibility of accidental short circuits when plugging and unplugging the PCB on the interface one.
The voltages taken from the cells are split between the two connectors, from the first cell to the sixth on the left connector while from the seventh cell to the twelfth in the right connector (see figure 4.44). For the other signals present in the connectors see 4.3.3.5.
In the left connector there are two pins for the isoSPI communication of the $LTC6811-2$, in addition to this, a two pin connector ($Nano-fit$ 1053131102) produced by $MOLEX$ has been inserted.
Both pins of the two connectors can be excluded from communication as SMD jumpers have been set up.
These two solutions have been set up for isoSPI communication between host and slave because, with the first of the two solutions, i.e.

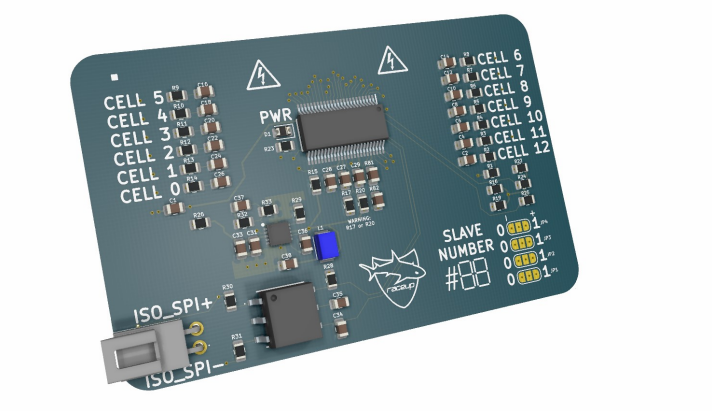


Figure 4.43: Render of the BMS Slave PCB

with the use of the *SAMTEC* connector, the communication signals would arrive from the interface board in which the traces for the differential communication have been drawn. With this configuration, the design of the entire battery pack would be tidier because, with the second solution i.e with the *MOLEX* connector, the standard connection (as well as recommended by the datasheet) would be to connect all the slaves to the host with a cable (CAT 5 is recommended).
However, since the effectiveness of the first solution proposed has not yet been demonstrated and there is currently no finished battery segment to test it in the environment in which it will normally operate, the second two-contact *MOLEX* connector has been set up to bypass the *SAMTEC* connector if the communication that uses this connector will not work properly or if it will be not very reliable.
The first components that were placed on board were the two 20 contacts connectors, as they determine the geometry of the PCB and the complete design of the solution composed of the two PCBs.
Then the main device, the $LTC6811-2$, was placed in the center of the board between the two connectors placed on the opposite side.
It was decided to place it horizontally with respect to the direction of the connectors because this position, together with the choice of positioning on the board, facilitates the routing of the critical signal traces for the detection of voltages, temperatures, and for the management signals for the cell discharge.
The next component that was placed on the board was the transformer ($SM91502ALA$) which ensures isolation in the communication part.
The positioning of this component is of fundamental importance because a positioning too close to the $LTC6811-2$ could create interference in the readings and in the proper operation due to the coupling of the magnetic field.
The manufacturer recommends a placement close to the IC but at least $1-2\ cm$ away to help isolate the integrated from the magnetic field. Moreover, another important aspect to take into account is that

the transformer should be placed as close to the isoSPI connector as possible and this distance should be kept less than 2 cm in order to avoid the occurrence of any interference in the signal.
The output signals from the transformer (board side) are the differential signals that will go into the $LTC6811-2$. These isoSPI signal traces should be as direct as possible and isolated from adjacent circuits by a ground plane or space. Moreover, no trace should cross the isoSPI signal lines unless separated by a ground plane on an inner layer.
A good practice for isolating differential traces is to space them at least of $5 \cdot w$ (where w indicates the thickness of the track) from components, any other traces or layers.
From figure 4.45, which shows these isoSPI signal traces highlighted, can be seen that these traces are isolated by the rest of the components and signal traces as the datasheet suggest.
The thickness of these communication traces has been chosen of 0.254 mm and their distance of 0.254 mm, this allows to have a differential impedance between the traces of approximately $Z_{diff} = 120\ \Omega$ as shown in figure 4.46, where the *KiCad* calculator tool used to set these parameters can be seen.
The parameters chosen for the correct calculation are reported below:

- $E_r = 4.6\ F/m$ is the FR-4 dielectric constant;
- $tanD = 0.02$ is the dielectric loss factor;
- $Rho = 1.72e-8\ \Omega/m$ is the conductor's specific resistance;
- $H = 1.6\ mm$ is the distance between traces and bottom ground plane;
- $H_t = 1e+20\ mm$ is the distance between traces and top ground plane, we want this to be approximate infinity, as we are using an external layer for the differential pair;
- $T = 0.035\ mm = 1\ oz.\ copper$ is the copper thickness;
- $Rough = 0\ mm$ is the roughness of surface (not relevant for this application);
- $me\ Rel\ c = 1$ is the relative permeability of conductor (not relevant for this application).

Figure 4.44 shows the BMS Slave PCB layout and can be recognized: the two $SAMTEC$ connectors highlighted in blue, the $LTC6811-2$ IC highlighted in pink, the $MOLEX$ connector highlighted in red and the $SM91502ALA$ transformer highlighted in orange.

Afterwards, the $LT3990$ IC that provides the low voltage reference for the $LTC6811-2$ has been positioned. Care has been taken during the PCB layout for this component in order to make it work in a proper

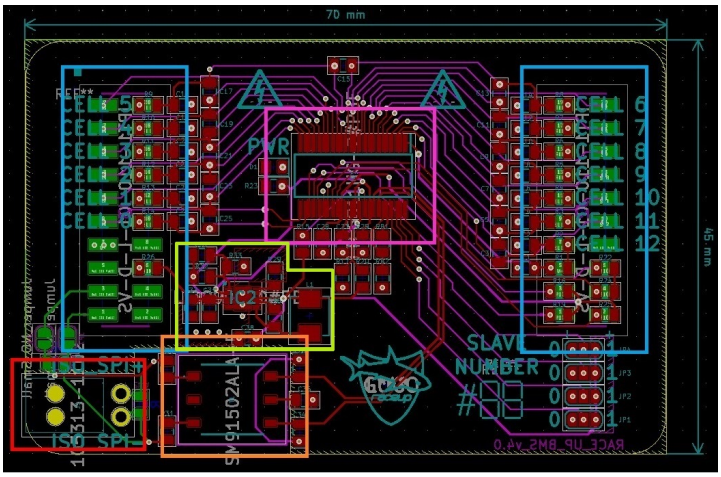


Figure 4.44: BMS Slave PCB layout

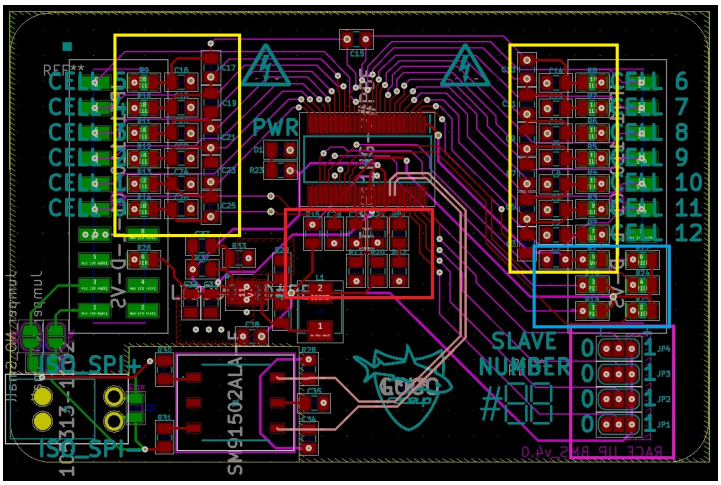


Figure 4.45: BMS Slave PCB layout - isoSPI traces highlighted

way and reduce at minimum the EMI.
Figure 4.47 shows the datasheet guideline for proper power and low EMI operation. The positioning of this component on the board is highlighted in yellow in figure 4.44.

The RC type filters described above (see 4.3.3.1) have been positioned above the *SAMTEC* connectors, highlighted in yellow in figure 4.45. The jumpers for setting the slave address are highlighted in pink in figure 4.45.
On the same figure can be seen the NTC resistors highlighted in red and the bypass and setup connections (see 4.3.3.1).

Even if the board has free space on the external layers, it was decided to make it anyway with 4 layers as they offer good EMC performance and good signal integrity compared to two-layer boards.
This is because with the four-layer layout is possible to realise a board

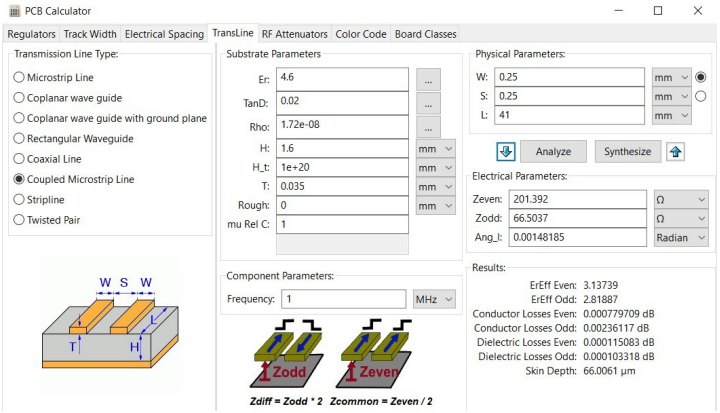


Figure 4.46: KiCad traces impedance calculator for BMS Slave PCB

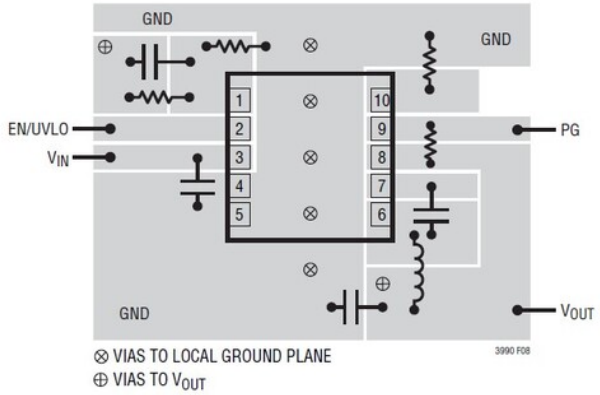


Figure 4.47: LT3990 datasheet layout guideline [8]

containing ground or power planes that results to be better than the boards without planes for the following reasons:

- It is possible to route the signals in a microstrip (or stripline) configuration which allows controlling the impedance transmission lines that produce much less radiation than the random traces used on one- and two-layer boards.
- The current return flow can flow back on the adjacent plane reducing the loop area.
- The presence of a ground plane significantly decrease the ground impedance and hence the ground noise.

As Henry W. Ott.writes in his book [9], during the design of multilayer boars, six design objectives should be kept in mind.
These points are summarized below:

- A signal layer should always be adjacent to a power or ground plane.
- Signal layers should be close to their adjacent power or ground planes.
- Power and ground planes should be closely coupled together.
- High-speed signals should be routed on buried layers located between planes.
  The planes can then act as shields and contain the radiation from the high-speed traces.
- Multiple-ground planes are very advantageous because they will lower the ground impedance of the board and reduce the common-mode radiation.
- When critical signals are routed on more than one layer, they should be confined to two layers adjacent to the same plane.

However, with a four-layer board it is difficult to satisfy all six of these points and some compromises have to be made.
The stack-up designs that are covered in [9] are many, among which can be found similar to the one that was decided to use for the realization of the BMS Slave developed in this project.
One of the most interesting designs is the one proposed in the figure 4.48 where the external layers are used for the power plans, while the internal ones are used to route the signals.
Figure 4.48(A) provides signal shielding in the internal layers thanks to the ground outer layers, but the power supply planes are likely to be very discontinuous in the case of PCBs with high component density.
Figure 4.48(B) still provides signal shielding in the internal layers,

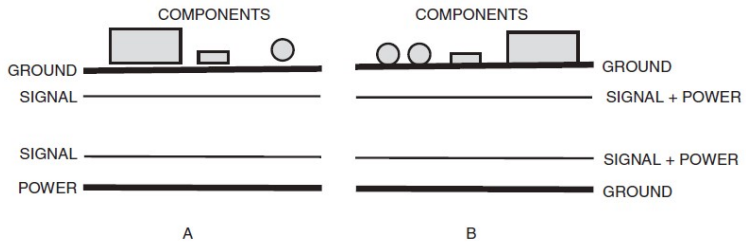


Figure 4.48: PCB stack-up layout design with signal traces on the inside layers and the planes on the outside layers [9]

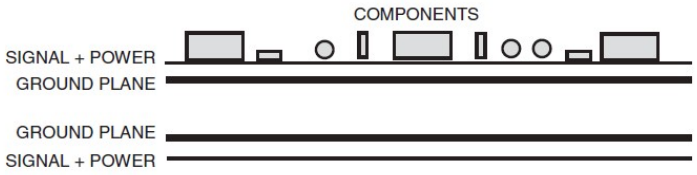


Figure 4.49: PCB stack-up layout design with two internal ground planes and no power plane [9]

without exposing the power plane externally which can thus be continuous.
With this type of configuration it is possible to hit three of the six points discussed above. Precisely, it is possible to place a signal and a ground (or power) planes one close to the other, they can be placed adjacently and the signals could be routed in the inner layers.
Moreover, the two ground planes can be connected on the perimeter of the board, creating a Faraday cage. This can decrease the ground impedance thereby reducing the radiation due to the common mode.
However, one of the disadvantages of this type of configuration lies in the fact that it is difficult to do rework on the signal traces because they are placed in the inner layers of the stack up.
Another design that turns out to be very interesting is the one shown in the figure 4.49. This figure shows the stack-up layout with two internal ground planes and no power plane.
Contrary to what happens in the configuration of figure 4.48, in this configuration the ground planes do not provide any shielding but still provides for the low ground impedance.
With this type of configuration, it is possible to hit three objectives, which are: the possibility to place a signal and a ground (or power) plane one close to the other, they can be adjacent and multi ground planes can be used in order to reduce ground impedance.
The configuration chosen for the BMS Slave developed in this project can be seen in figure 4.50. It is a mix from the stack-up configuration seen in figure 4.48(B) and that seen in figure 4.49.

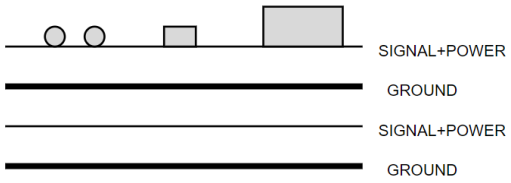


Figure 4.50: BMS Slave stack-up layout design

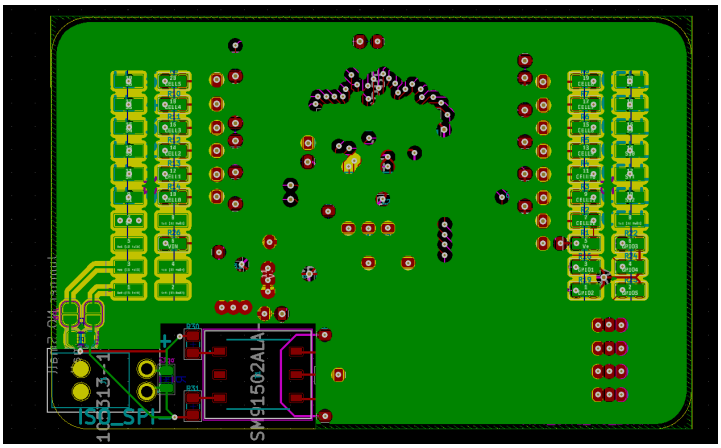


Figure 4.51: BMS Slave ground plane on second PCB layer

With this type of configuration, good signal integrity should be achieved because it is possible to use an internal layer for the transmission of critical signals and to place two ground planes, one above and one below the layer in which the signals are placed.
This should ensure a good shielding of the signals and the presence of two ground planes should decrease the ground impedance thus reducing the noise as well.
It is possible to hit four of the objectives discussed above. In particular it is possible, as the other two previous configurations, to have the signals and ground planes one adjacent to the other and one close to the other. In addiction of the previous configurations, it is possible to route the critical signals in the inner layers with one ground layer up and one above it, this helps to shield them and to realize a low impedance ground path.
Figure 4.51 and figure 4.52 shows the ground planes of the BMS Slave described above.

Furthermore, with this technique is easy to realize a continuous underlying ground reference plane free of cuts that would decrease the impedance of the track, as the datasheet suggests, for the length

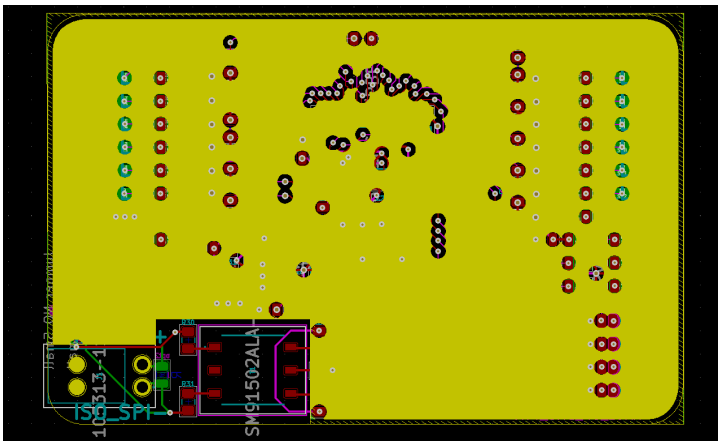


Figure 4.52: BMS Slave ground plane on fourth PCB layer

of the isoSPI traces.
It is noted how the objective of placing the power supply and the ground layer adjacent could be useful to create an intrinsic interplane capacitance used as a bypass for the various integrated circuits.
However with normal PCB construction techniques, there is not enough interplane capacity between adjacent power and ground planes to provide adequate decoupling below approximately 500 MHz so, it was preferred not to focus on achieving this goal because it is easy to overcome this problem by using suitable decoupling capacitors for the various devices.

4.4 INTERFACE PCB

In order to solve the problem of mounting the BMS on the support to ensure electrical contact and mechanical contact which took a long time, it was thought to create a modular system in which there are two boards that act as BMS Slaves. The first board is the one described previously and its function is that of managing signals and the effective detection of voltages and temperatures, as well as communication with the BMS Host.
The second board, named in the project as interface PCB, has the task of interfacing the management board with the segment where the cells are present. In particular, this board takes care of getting the voltages for detecting the temperatures and the state of charge of the individual cells.
The structure created by the two boards is made up of the interface PCB that acts as a support for the monitoring PCB that is fixed through its two $SAMTEC$ connectors.
This configuration allows an easier debugging phase because it will be enough to remove the monitoring board from the interface board

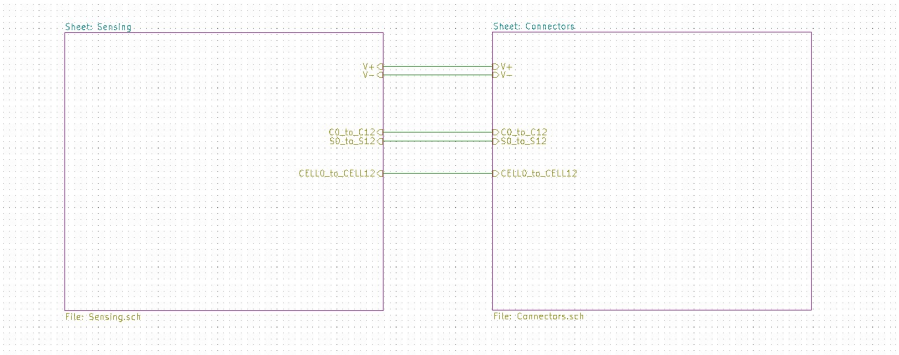


Figure 4.53: Interface PCB worksheets schematic

to be able to work on it in an easier way.

4.4.1 *Schematic Analysis*

The schematic of this interface PCB has been divided into two worksheets, namely Sensing and Connectors.These worksheets and the most significant connections that link them can be seen in the figure 4.53.

The sensing schematic area, shown in figure 4.54, has a series of components necessary for the correct voltage detection and for the controlled discharge of the cells. This type of configuration is recommended in the $LTC6811-2$ datasheet.
The schematic results to be the composition of the same block 12 times, one per cell, so later it will be analyzed only once.
This fundamental block can be seen in the figure 4.55.
The voltages of the single cells are taken from the labels indicated with $CELLx$, these labels start from 0 to 13, where with $CELL0$ refers to the negative reference of the series of the 12 cells.
The VIN label and the one indicated by $V+$ represent the positive reference of the cell with the highest potential of the series made up of 12 cells.
The first of the two corresponds to the power supply voltage of the step-down (buck) regulator, $LT3990$, used to power the low voltage part of the integrated circuit for the management of voltages and temperatures present in the monitoring PCB.
The label $V+$ instead corresponds to the input for the power supply of the high voltage circuitry of the device $LTC6811-2$ present in the monitoring board, this voltage is brought to the input pin of the integrated after an RC type filter with values and function explained in 4.3.3.2. The resistor R62 and the MOSFET Q12 are placed in parallel to the cell, their function is to discharge the cell in a controlled way on the resistor with the aim of balancing the series of 12 cells to bring

them to an almost equal voltage.
The discharge of the cell takes place by bringing the MOSFET into conduction through the driving of the gate connected to the balancing pin ($S(n)$) of the $LTC6811-2$ which allows you to use this pin as a digital output for driving the gate of an external MOSFET used for cell discharging, as previous mentioned in 4.3.3.3.
The R50 resistor is used as a pull up for the P-type MOSFET to prevent undesired conduction events due to fluctuations in the drive signal, especially when the monitoring board will not be mounted on the interface board, because, on this occasion, the gate signal would not be driven but would otherwise be left floating.
The LED diode D12 and the resistor R38 are placed in parallel with the balancing resistor R62 to have visual feedback when a cell enters the discharge phase, this arrangement makes the debug phase easier.
The chosen LED has a Continuous Forward Current $I_F = 30\ mA$, which corresponds to a drop of about $V_F = 2\ V$. To limit the current flowing in the LED and avoid burning it when it turns on, a resistor with a value equal to:

$$R_{min} = \frac{(V_{Max} - V_F)}{I_F} = \frac{(4.2\ V - 2\ V)}{30\ mA} = 73.3\ \Omega$$

The chosen resistance is $R = 100\ \Omega$ which allows a maximum current of:

$$I_{F,max} = \frac{(V_{Max} - V_F)}{R} = \frac{4.2\ V - 2\ V}{100\ \Omega} = 22\ mA$$

The maximum power that can be dissipated by the LED is $P_{max} = 72\ mW$, while, in these conditions of use, the dissipated power is equal to:

$$P = V_{LED,max} \cdot I_F = 2.4\ V \cdot 22\ mA = 52.8\ mW < P_{max} = 72\ mW$$

For the sizing of the balancing resistor, it was taken into consideration that the discharge phase occurs in the final phase of the charge, i.e. when the cell voltage is around $4.2\ V$.
an imbalance of about 5% of the state of charge of the cell was considered, i.e. $3\% \cdot 6.35\ Ah = 0.1905\ Ah$ to be balanced. This value was rarely detectable in the previous configuration, in which often the deviation was about $100\ mAh$, the 3% can therefore be considered a worst-case.
Therefore, in the final charge phase, with a resistance $R_{disch} = 3.9\ \Omega$ there would be a current of approx $I = V/R = 4.2\ V/3.9\ \Omega = 1.07\ A$.
The key aspect to consider is the balancing time necessary to bring the cells to the same voltage.

To balance the 3 % of the total capacity of the cell, with a resistance of $R_{disch} = 3.9\ \Omega$, a time of approximately is required:

$$t = \frac{Q}{I} = \frac{0.1905 Ah \cdot 3600}{1\ A} = \frac{685.8\ C}{1\ A} = 685.8\ s$$

which are equivalent to approx 12 min. However, this time during the discharge phase will be extended to avoid excessive overheating of the electronic components, such as the resistors and MOSFETs.
The resistor has been chosen with a power rating higher than necessary, in fact the $35603R9JT$ produced by $TE\ Connectivity$ offer a dissipating power of $P_{diss} = 6\ W$, while the necessary ones turn out to be approximately equal to $P = R \cdot I^2 = 3.9\ \Omega \cdot 1\ A = 3.9\ W$.
The package of these SMD components is 4527, therefore of considerable size, however this package was chosen as there is enough space on the interface board for proper heat dissipation.
Due to the increase in the temperature of the balancing resistors due to the thermal dissipation caused by the Joule effect, it will probably be necessary to use the PWM control setup for the $S(n)$ pins provided for the $LTC6811-2$.
As regards the MOSFETs, the BSS308PEH6327XT produced by $Infineon\ Technologies$ was chosen, which offers the following parameters:

- DRAIN-SOURCE voltage of $V_{GS,max} = \pm 20\ V$;
- RAIN-SOURCE max current of $I_{DS,max} = 2\ A at T_{amb} = 25°C$;
- DRAIN-SOURCE on max resistance of $R_{DS(on),max} = 130\ m\Omega$ with a $V_{GS} = -4.5\ V$;
- a power dissipation of $P_{tot} = 0.5\ W$.

The power dissipation of BSS308PE is greater than required:

$$P_{diss,MOSFET} = R_{DS(on),max} \cdot I_{DS}^2 = 130\ m\Omega \cdot (1\ A)^2 = 0.13\ W\ <\ P_{tot} = 0.5\ W$$

The pin $S(n)$ of the $LTC6811-2$ that controls the gate of the discharge MOSFET can be brought to a potential equal to $C(n)$, during the unwanted discharge phase, through an internal resistance of the integrated circuit or to a voltage equal to $C(n-1)$, during the discharge phase.
The internal structure to which is referred is shown in the figure 4.56.
The minimum GATE-SOURCE voltage to bring the MOSFET in conduction is $V_{GS,th,min} = -2\ V$, this value guarantees the possibility of balancing for any voltage in the expected operating range of the cell because the voltage between $C(n)$ and $C(n-1)$ can never be less than the minimum $V_{GS,th,min}$ voltage of the MOSFET because it would go under the cell cut-off voltage with potentially serious consequences.

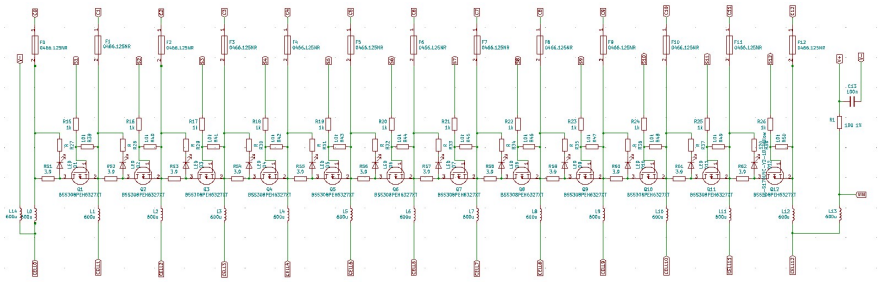


Figure 4.54: Interface PCB sensing schematic area

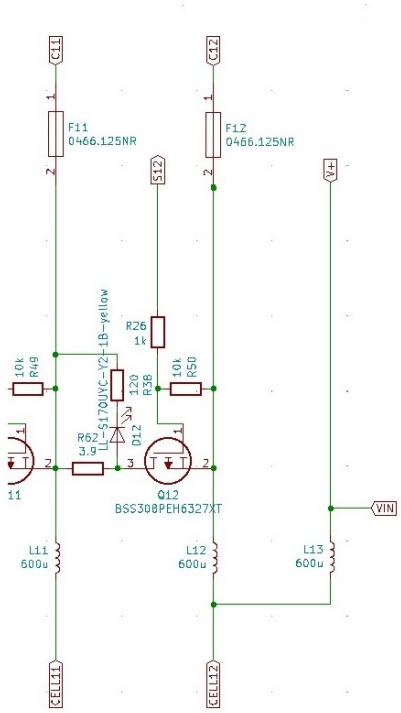


Figure 4.55: Interface PCB sensing and discharge schematic block

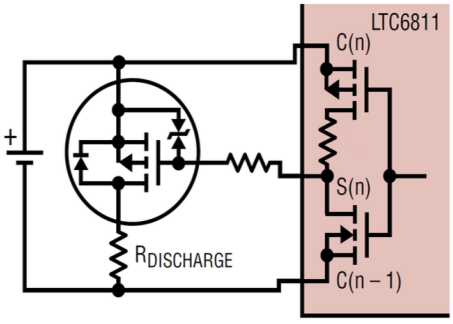


Figure 4.56: LTC6811-2 internal discharge circuit [7]

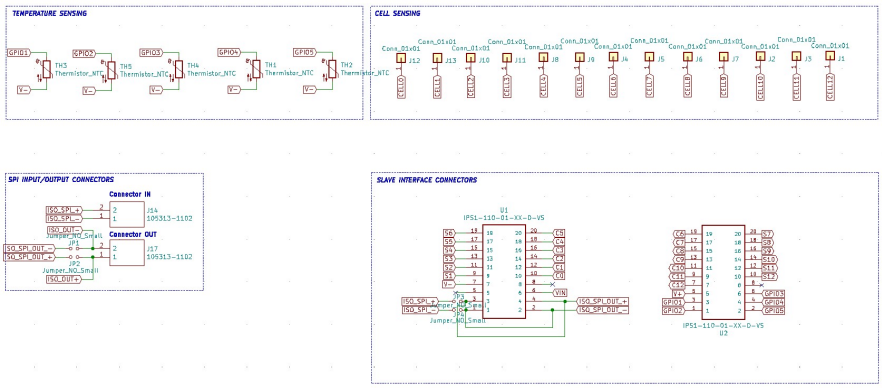


Figure 4.57: Interface PCB Connectors schematic part

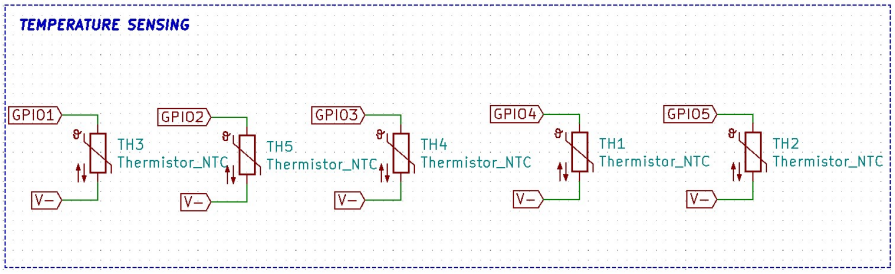


Figure 4.58: Interface PCB TEMPERATURE SENSING schematic part

In addition, it can be noted that 0.125 mA fuses have been set up before the signals go to the monitoring board, in order to protect the integrated circuit that performs the voltage and temperature monitoring function from overcurrents caused by incorrect connections during the debugging phase.

The schematic area of the connectors is divided into four macro areas for easier reading and faster debugging. These four areas are: TEMPERATURE SENSING, CELL SENSING, SPI INPUT / OUTPUT CONNECTORS and SLAVE INTERFACE CONNECTORS, these parts could be seen in figure 4.57.
The TEMPERATURE SENSING area, shown in figure 4.58, simply shows the symbols for the connectors where the five NTC sensors will be soldered to detect the cell temperatures.
The CELL SENSING area, shown in figure 4.59, shows the connectors symbols where the 12 series cells will be connected.
The SPI INPUT / OUTPUT CONNECTORS area, shown in figure 4.60, shows the input and output SPI connectors. These two connectors are necessary in order to put the various interface PCBs in communication and, consequently, the various monitoring boards. It was thought to arrange two connectors in such a way as to reduce the cable wiring because it was messy and there was a risk of accidental breakage as it is of considerable length, the isoSPI communication therefore takes

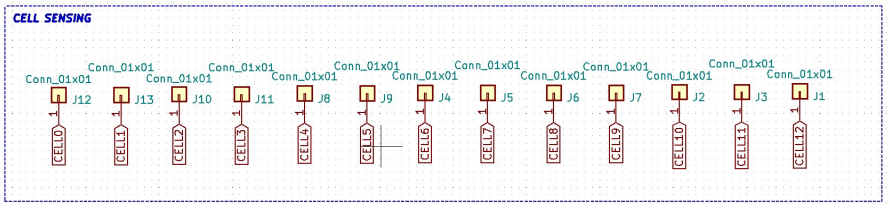


Figure 4.59: Interface PCB CELL SENSING schematic part

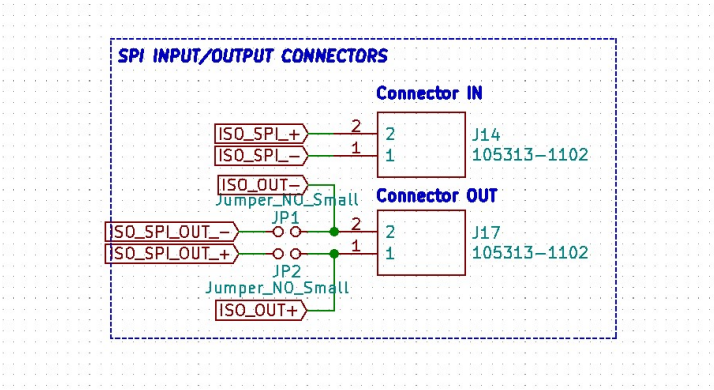


Figure 4.60: Interface PCB SPI INPUT / OUTPUT CONNECTORS schematic part

place through the traces present on the board and then comes out of the connector to be able to interface multiple interface PCBs. This topic will be covered in more detail in 4.4.2.

The SLAVE INTERFACE CONNECTORS area, shown in figure 4.61, contains the symbols of the connectors used with the relative labels in order to correctly interface the interface board with the signal management board.

Through these connectors the voltages are taken for the correct power supply the $LTC6811-2$ integrated circuit (VIN, $V+$, $V-$), the signals necessary for the correct reading of the voltages ($C(n)$) and of the cell temperatures ($GPIOx$), signals for the management and enabling of the MOSFETs that control the discharge of the single cells ($S(n)$) and the isoSPI communication.

4.4.2 *Interface PCB layout*

The geometry of the PCB interface board was initially designed to be able to adapt it to the battery segment of the previous version. This allows starting debugging the system more quickly as, otherwise, we would have had to first create the new battery segment and then create the interface board, then begin the system debugging phase for the system for handling critical signals. Such a procedure would have taken up a considerable part of the time available.

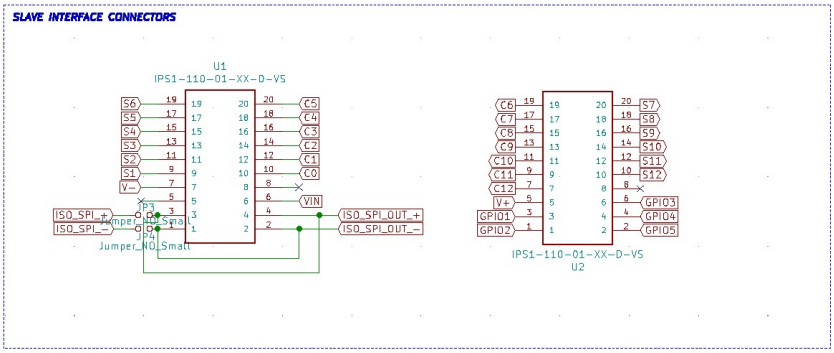


Figure 4.61: Interface PCB SLAVE INTERFACE CONNECTORS schematic part

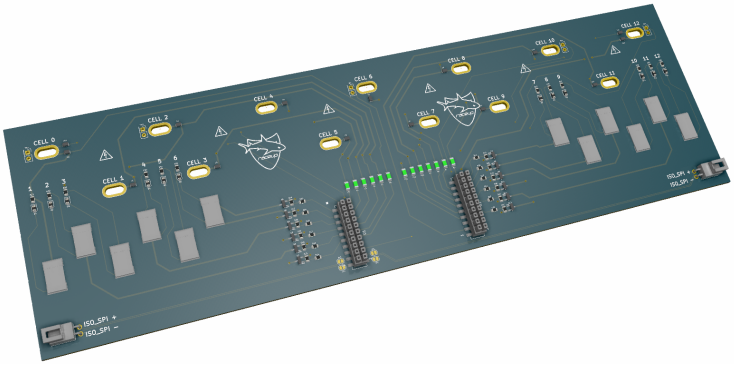


Figure 4.62: Render of the BMS Interface PCB

A render of the interface BMS PCB can be seen in figure 4.62. Once the layout of the battery segment has been completed, the version of the suitable interface PCB will also be created.
This geometry is constrained by the BMS Slave mounting system that was in the old configuration (see 3.14).
In particular, the contact points that guarantee the electrical connection for measuring the voltages of the individual cells are made with M3 aluminum spacers fixed to the busbars. Therefore, the pitches that guarantee the electrical connection in the board must be concentric in shape.
In this interface PCB prototype, also the position of the NTC sensors for detecting the temperature of the cells have a constrained position, this because otherwise they would not be properly in contact with the aluminum busbars.
Figure 4.63 shows the PCB layout of the interface board prototype.
In this figure (4.63) can be seen the concetric pads described above, indicated with the name of *CELLx* and yellow in color, which allow mechanical fixing to the segment spacers and allow the detection of the voltages of the single cells.

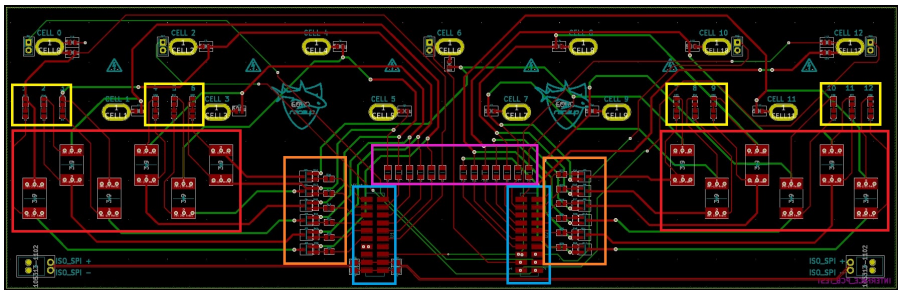


Figure 4.63: Interface PCB layout

The connectors used to house the monitoring board are highlighted in blue (see 4.63).
The connectors used are the counterpart of those used in the board to be connected and are the $SAMTEC\ IPS1-110-01-L-D-VS$.
It was decided to use the male counterpart of this connector in the interface board so as not to have exposed contacts when inserting the card and as they are individually shielded there is no risk of creating accidental short circuits during maintenance.
Moreover, can be seen the fuses (highlighted in pink) designed to protect the IC of the monitoring board from from potentially harmful overcurrents during the debug phase.
The electronic circuitry used to enable or disable the flow of current through the discharge resistors (which are highlighted in red in figure 4.63) which allows the balancing of the single cell is visible in orange. The operation of this circuit has been previously analysed (see 4.4.1).
In addition, in yellow can be seen the balancing LEDs and their resistors used as visual feedback to know when, and which cell, is discharging.
At the bottom left and bottom right of the board can be seen the connectors for isoSPI communication set up for connection between the various devices.
The communication traces have been drawn in a differential manner with a width of $w = 0.254\ mm$ and a distance between the two differential tracks of $d = 0.254\ mm$ (as previously described in 4.3.4).
As previously mentioned (see 4.4.1), the correct functioning of this method will be analysed with the correct setup and in normal use conditions, therefore during bench tests of the car or on the track, to determine the effective possibility of using it instead of using a cable to connect all BMS slaves.
A negative reference potential plane was created in the last layer of the PCB to provide a minimum of shielding to the signals, it can be seen in figure 4.64

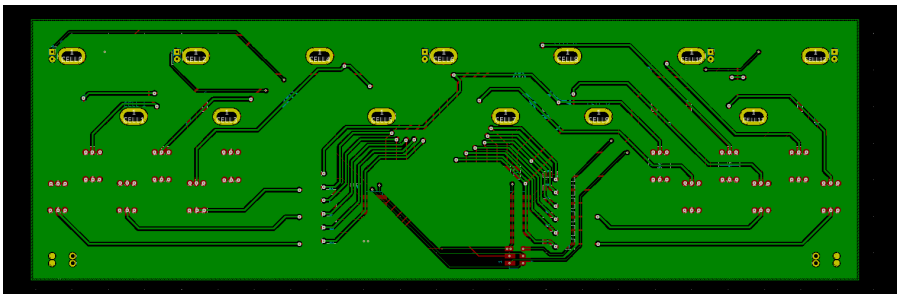


Figure 4.64: Interface PCB negative reference plane

5 BMS HOST PROGRAMMING CODE

The development part of the code for the communication between the BMS Host and the BMS Slave took up most of the time of this project.
The code was written using the C ++ programming language and the Visual Code Studio program as a code editor.
Several existing libraries to write the code has been used.

5.0.1 *BUS protocol*

All the data sent by and to the $LTC6811-2$ are composed in byte groups and they are transferred with the Most Significant Bit (MSB) first.
During the command transfer sequence, the Chip Select (CS) pin must remain low and during the write commands, data are latched on the rising edge of the CS pin.
With the $LTC6811-2$ it is possible to send messages both in broadcast and addressed to individual devices.
If an address command is used to send a message only this device connected to the bus will respond. An addressed device will respond to an address command only if the physical address of the device on its pins (A3 to A0) match the address specified in the address command
A broadcast command is used to send the same message to all devices on the bus and they all will respond, regardless of the device address. It is useful for setting up the same settings for all the devices for example.
However, the polling function can be also used for broadcast commands but not with the parallel isoSPI configurations as the case in this project.
For the first version of the code, the polling function works in such a way that it continues to wait for the same device until it finishes executing the function.
The structure of the broadcast and the address commands are shown respectively in table 5.2 and 5.3.
The broadcast command has a value of 0 for $CMD0[7]$ to $CMD0[3]$ while the address command has a value of 1 for $CMD0[7]$ followed by the 4-bit address of the device (A3, A2, A1, 0) in $CMD0[6]$ to $CMD0[3]$.
The Packet Error Code (PEC) is a 15-bit Cyclic Redundancy Check (CRC) value calculated for all the bits in a register, it must be computed on

Table 5.1: Command description structure [7]

COMMAND DESCRIPTION	NAME	CC[0:10] - COMMAND CODE										
Start Cell Voltage ADC Conversion and Poll Status	ADCV	0	1	MD[1]	MD[0]	1	1	DCP	0	CH[2]	CH[1]	CH[0]
Start GPIOs ADC Conversion and Poll Status	ADAX	1	1	MD[1]	MD[0]	1	1	0	0	CHG[2]	CHG[1]	CHG[0]
Clear Cell Voltage Register Groups	CLRCELL	1	1	1	0	0	0	1	0	0	0	1
Clear Auxiliary Register Groups	CLRAUX	1	1	1	0	0	0	1	0	0	1	0

Table 5.2: Broadcast command structure [7]

NAME	RD/WR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CMD0	WR	0	0	0	0	0	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

the entire 16-bit command (*CMD*0 and *CMD*1).
The Command Code (CC) acronym expresses a unique sequence of bits necessary to use a specific device command.
Some of the most important commands are shown in table 5.1. All the functions described in the datasheet have been implemented in the code, in order to have maximum flexibility in future.

5.0.2 *Code Structure*

First of all, as previously highlighted, the BMS Slave board appears to be devoid of microcontroller, which leads to the advantages described above (see 4.1).
This means that the code that has been written is loaded into the BMS Host microcontroller which, through SPI communication, interfaces with the various BMS slaves boards, configuring and controlling them.
It was decided to write the code in a parametric way, in such a way

Table 5.3: Address command structure [7]

NAME	RD/WR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CMD0	WR	1	a3	a2	a1	a0	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

as to already prepare the basics to be able to use the code even with more than one BMS Slave.
So, the main goal was not to create a code only with the purpose of testing the functioning of a prototype but to make it that can also be used in the future for the entire battery pack monitoring system project.
Therefore, all the possible options for configuring the device have been integrated into the code that are described in the component datasheet, from the choice of the working frequency to the choice of which cells to detect or for how long to discharge them.
The first thing that was done was to create the necessary structures to properly configure the device.
Critical device values such as the undervoltage threshold, overvoltage threshold and other parameters are saved in the configuration register group.
Table 5.4 shows the structure of the configuration register group.
The acronyms used in this table and their function are described below:

- GPIOx: indicates the GPIOx Pin Control and can be: during Write: 0 to set GPIOx Pin Pull-Down ON and 1 to set GPIOx Pin Pull-Down OFF, during Read: 0 to set GPIOx Pin at Logic 0 and equal to 1 to set GPIOx Pin at Logic 1.

- REFON: indicates the References Powered Up and can be: 1 to set References Remain Powered Up Until Watchdog Timeout and equal to 0 to set References Shut Down After Conversions.

- DTEN: indicates the Discharge Timer Enable. It can be Read-only and if it is equal to 1 means that the discharge timer for discharge switches is enabled and if it equal to 0 means that the discharge timer is disabled.

- ADCOPT: indicates the ADC Mode Option Bit. It can be equal to 1 or to 0. If it is equal to 1 means that the ADC frequency can be set to one of the following values with MD[1:0] Bits in ADC Conversion Commands: 27 kHz, 7 kHz, 422 Hz or 26 Hz. If it equal to 1 the ADC frequency can be set equal to 14 kHz, 3 kHz, 1 kHz or 2 kHz.

- VUV[x]: indicates the Undervoltage Comparison Voltage. The desired value can be set using the following formula:

$$Comparison\ Voltage = (VUV + 1) \cdot 16 \cdot 100\ \mu V.$$

- VOV[x]: indicates the Overvoltage Comparison Voltage. The desired value can be set using the following formula:

$$Comparison\ Voltage = VOV \cdot 16 \cdot 100\ \mu V.$$

Table 5.4: Configuration register group structure [7]

REGISTER	RD/WR	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CFGR0	RD/WR	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	REFON	DTEN	ADCOPT
CFGR1	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGR2	RD/WR	VOV[3]	VOV[2]	VOV[1]	VOV[0]	VUV[11]	VUV[10]	VUV[9]	VUV[8]
CFGR3	RD/WR	VOV[11]	VOV[10]	VOV[9]	VOV[8]	VOV[7]	VOV[6]	VOV[5]	VOV[4]
CFGR4	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGR5	RD/WR	DCTO[3]	DCTO[2]	DCTO[1]	DCTO[0]	DCC12	DCC11	DCC10	DCC9

Table 5.5: Configuration register matrix structure [7]

tx_cfg						
COLUMN / ROW	[0]	[1]	[2]	[3]	[4]	[5]
[0]	IC1_CFGR0	IC1_CFGR1	IC1_CFGR2	IC1_CFGR3	IC1_CFGR4	IC1_CFGR5
[1]	IC2_CFGR0	IC2_CFGR1	IC2_CFGR2	IC2_CFGR3	IC2_CFGR4	IC2_CFGR5
[2]	IC3_CFGR0	IC3_CFGR1	IC3_CFGR2	IC3_CFGR3	IC3_CFGR4	IC3_CFGR5
[3]	IC4_CFGR0	IC4_CFGR1	IC4_CFGR2	...	...	...
...	...	...	...	...	...	...

- DCCx: indicates the Discharge Cellx. If it is equal to 1 means that the Cellx shorting switch is turned ON while if it is equal to 0 means that that the Cell x shorting switch is turned OFF.
- DCTO[x]: indicates the Discharge Time Out Value. It can be used to set the discharge time from a minimum of 0.5 *min* setting this pin to 0 to a maximum of 120 *min* setting this pin to hexadecimal value F.

To write this type of register it was decided to use a two-dimensional matrix, which in the code is called tx_cfg, in which the first number indicates the number of the device present in the bus while the second number indicates the value of the configuration register to be written. The $LTC6811-2$ configuration data that will be written should be stored in blocks of 6 bytes and the matrix structure have the format shown in table 5.5.

Also the battery cells variables received from the $LTC6811-2$ integrated circuit are stored in a matrices of the same structure as the one shown in 5.5 waiting to be sent to the IC on the host through the *LTC*6820.
These matrices in the code are called as:

- cell_codes are used to store the cells voltages detected by the IC according to the Cell Voltage Register Group memory map.

- aux_codes are used to store the GPIOx voltages detected by the IC according to the Auxiliary Register Group memory map.
- stat_codes are used to store the GPIOx voltages detected by the IC according to the Status Register Group memory map.

All these register structures are reported in the $LTC6811-2$ datasheet.

First of all, when the code is started, the communication between the devices in the BUS is initialized and opened, as previously mentioned the communication used is of the SPI type.
Once the communication is initialized correctly, the code is structured in such a way as to initialize the $LTC6811-2$ by writing the tx_cfg matrix previously set by the user using the dedicated parameters contained in table 5.4.
This configuration message is sent with the broadcast method because all the slaves must have the same overvoltage and undervoltage thresholds. Initially, the discharge parameters of the cells are all set to OFF for a safety factor.
Once the device has been configured correctly, the actual part of the code begins and is repeated cyclically and consists in sending repeatedly the various messages of interest.
In our case, the commands that are sent are those of ADC conversion start of the voltages read for the analysis of the temperatures and voltages of the cells, respectively, ADAX and ADCV previously described. Based on the data received, an analysis is made and a decision is taken on whether or not to open the SDC.

5.0.3 *Code and system testing*

Due to the difficulty in finding integrated circuits caused by the semiconductor crisis affecting the electronic components market in this period, it was decided to buy the two evaluation boards produced by Analog Devices in order to test the correct functionality of the system and the written control code.
The evaluation board for the $LTC6811-2$ is the $DC2260A$ and is shown in figure 5.1, while the evaluation board for the $LTC6820$ is the $DC1941D$ and shown in figure 5.2.
The first of the two evaluation board represents the BMS Slave in our system while the second one represents the BMS Host.
The setup used to test the system and the written control code is composed of:

- Arduino Due to simulate the Host microcontroller,
- the $DC2260A$ evaluation board necessary to convert the SPI signals into isolated ones,

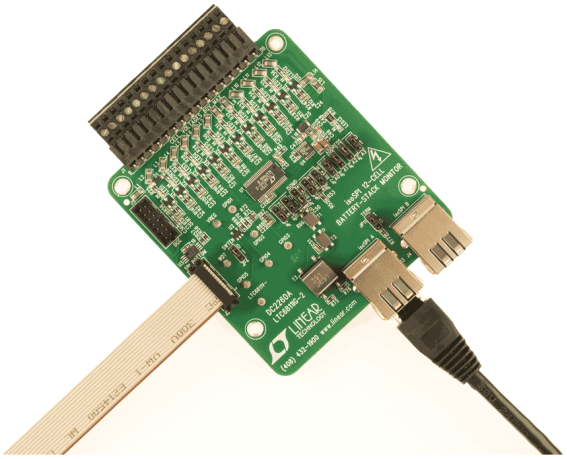


Figure 5.1: DC2260A Evaluation Board [10]

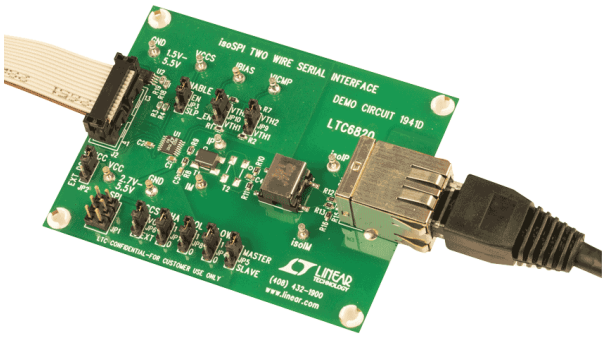


Figure 5.2: DC1941D Evaluation Board [11]

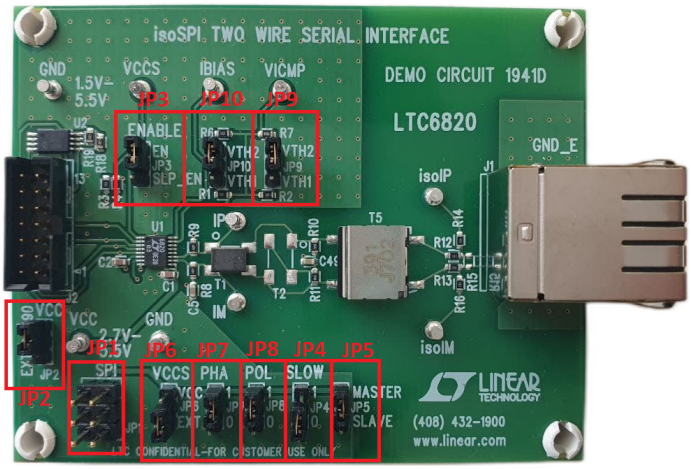


Figure 5.3: DC1941D jumpers highlighted [11]

- the *DC*1941*D* evaluation board to simulate the monitoring IC of the Slave board.

On the board there are several jumpers that can be set in different positions in order to configure the operating mode in the most appropriate way for the test to be carried out.
These jumpers can be seen in figure 5.3.
For our needs, the various jumpers have been set according to the following configuration:

- *JP*2: to *DC*590 in order to power supply the board with the 5 *V* provided by Arduino Due board;
- *JP*3: to EN in order to have the *LTC*6820 always enabled;
- *JP*4: to FAST in order to set the SPI clock frequencies greater than 100 *kHz*.
- *JP*5: to MASTER, in this way, the *LTC*6820 will operate as the isoSPI master and with this configuration, the *J*2 ribbon connector or *JP*1 header connector should be connected to an SPI master. We use the *JP*1 header connector to make the connection between Arduino Due and the evaluation board.
- *JP*6: to EXT, this allows the SPI input/output supply (VCCS) to be connected to a separate voltage from VCC, which allows the logic levels to be set to a different voltage. The external supply can be connected on the turret labeled with VCCS. During the

test, the VCCS voltage has been set to 3.3 V which is the SPI voltage level of Arduino Due.

- $JP7$, $JP8$: respectively to PHA and to POL. This ensure that the SCK idles high ($POL = 1$) and that the data is latched on the rising (second) clock edge ($PHA = 1$). For more details refer to 4.1.

- $JP9$, $JP10$: both to $VTH2$. This sets the $LTC6820$ output drive to 1 V and the receiver input threshold to 600 mV. For more details refer to 4.3.1.

This board is connected to the Arduino Due through seven wires used to communicate between the two boards with SPI communication protocol.
Four of these wires are for SPI communication and are: MISO, MOSI, SCK and CS while the remaining three wires are used to supply the board with VCC at 5 V, GND and VCCS at 3.3 V.
It is then connected to the second evaluation board where the $LTC6811-2$ is housed. This second evaluation board also has several jumpers to set the operation configuration.
These jumpers can be seen in figure 5.4.
The setup chosen for these jumpers are reported below:

- $JP1$, $JP2$, $JP3$, $JP5$, $JP6$ are set to 1 in order to use isoSPI communication mode;

- $JP4$ is set to 0 in order to disable the Discharge Timer Enable (DTEN);

- $JP11$ set to 1 in order to adapt the communication trace impedance.

The first test that was carried out was to test the communication code between the two evaluation boards, to do this on the connector used for connection to the cells of the $DC2260A$ a resistive divider with twelve 100 Ω resistors was created in order to simulate a load and do not leave the IC pins with floating references.
After verifying that the communication was stable and that the code on the Arduino Due really did what it was programmed for, it was decided to proceed with the tests and try the part of the code that balances the cell voltages by downloading them to the discharge resistances.
In order to test this code part, in which the main aim is to make all the cells reach the same voltages to maintain them at the same level of SOC,the $DC2260A$ board has been connected through 13 wires to the 12 cells of the battery segment.
The balancing programming code currently consists of detecting the minimum voltage of the read cells and the consequent discharge of

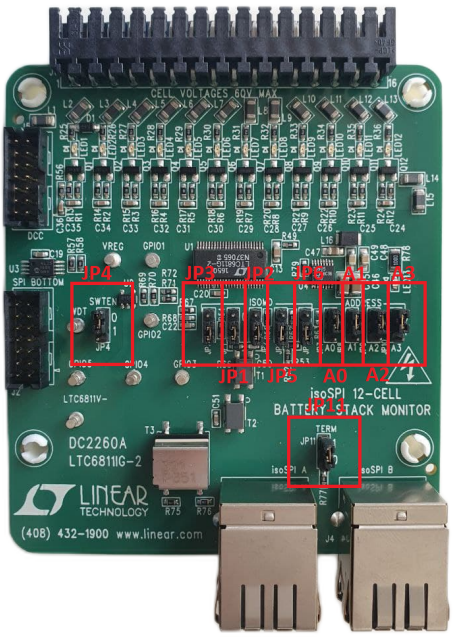


Figure 5.4: DC2260A jumpers highlighted [10]

the cells which have a voltage higher than the minimum one.
Figure 5.5 shows the previously described test. In this figure can be seen the RED discharge LEDs that provides visual feedback on which cells is discharging.
During the discharge process it is possible to continue reading the cell voltages if the Discharge Permitted (DCP) parameter present in the configuration register is correctly set (see figure 5.4).
To go deeply in detail, if the DCP pin is set equal to 1 at the time of cell measurement command, the S pin discharge state does not change during the cell measurement. On the contrary, if this pin is set to low the S pin discharge state will be disabled while the corresponding cell or adjacent cells are being measured.
Obviously the reading that occurs with the DCP pin set high is not very accurate because there is an error due to the voltage drop caused by the current flowing in the discharge branch.
After the tests with the evaluation boards, the test with the BMS Slave was carried out. The first test that was carried out was to verify the correct communication between the $DC1941D$ evaluation board and the BMS Slave.
In figure 5.6 can be seen the setup used to carry out this test.
The BMS Slave is plugged on the BMS Interface board, where between CELL0 and CELL12 are applied 20 V in order to simulate a battery

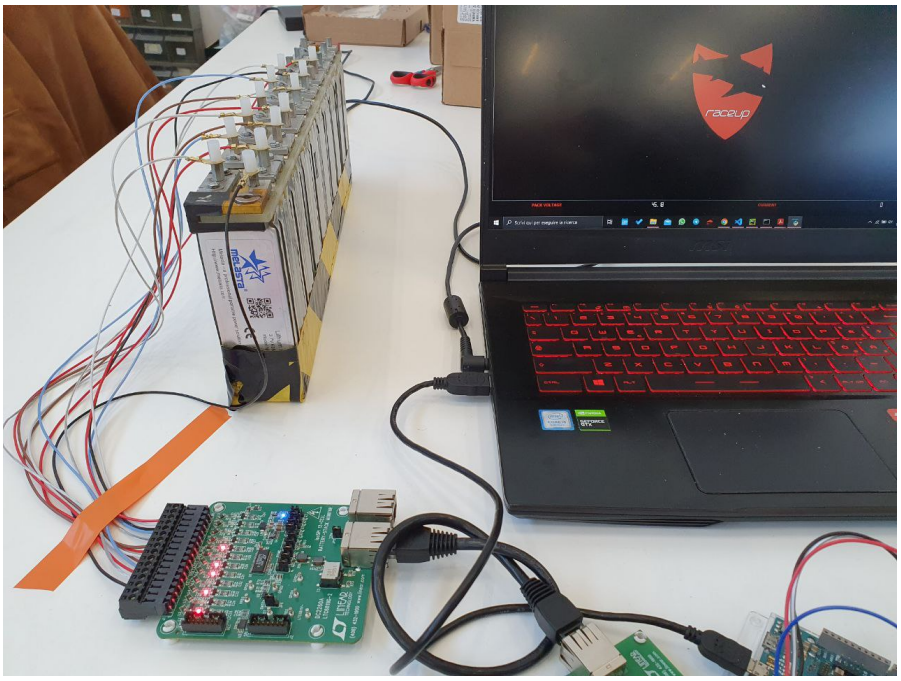


Figure 5.5: DC2260A discharge test

module and to provide the power supply to the BMS Slave board.
As can be seen, the power-on LED remains steady on, this means that the communication between the evaluation board and the BMS Slave is stable. If the communication between the two boards is not established correctly, the power-on LED will turn off after 2 seconds, that is when the $LTC6811-2$ watchdog expires, bringing the device into SLEEP mode. In this state, the DRIVE pin of the $LTC6811-2$ is brought to $0\ V$ and since this is connected to the EN pin of the $LT3990$ this will also enter the IDLE state causing the power-on LED to turn off that is connected in parallel to the power supply branch which powers the $LTC6811-2$. The fact that the communication is established and the two boards are able to correctly communicate is confirmed also by the fact that the total voltage value read corresponded to the voltage imposed by the generator and applied to the interface PCB. The read values of the single cells provided variable values because they were not connected to any reference.
The next step was to test the entire system, so the BMS Host connected to the BMS Slave plugged on the interface PCB.
The setup used to test this configuration can be seen in figure 5.7.
We obtained the same results as the previous carried test. So the communication is correctly established and the system read the values applied from CELL0 to CELL12 with a satisfying precision.
The last test that was carried out was the one with the whole BMS system mounted on the battery segment and verifying that it correctly reads the cell voltages and temperatures.
This test can be seen in figure 5.8.

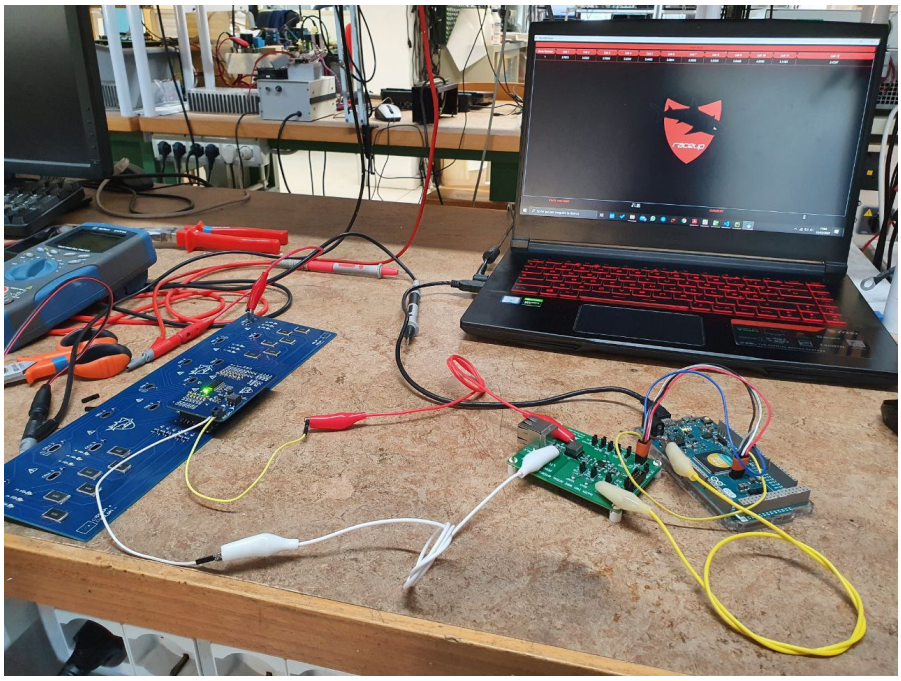


Figure 5.6: BMS Slave communication test

Downstream of the tests carried out, it can be said that the system is stable, in particular, the error on the voltage readings is very low, in the order of 10^{-4} V, as can be seen from figure 5.9.

5.0.4 *BMS User Interface*

According to the FSG rules, during the technical inspection, a device (e.g. a laptop) must be provided in order to display all measured values of the BMS.
In order to satisfy this rule and to make debugging easier, an user interface has been created.
To create this interface, the Python programming language and the PYCharm development environment developed by JetBrains were used.
The program mainly consists in the extrapolation of all the data present in the serial that the BMS Host, in this case made by the Arduino Due, sends and the relative data processing.
A representation of the interface can be seen in figure 5.10
This user interface will display all the cell voltages and temperatures that a single slave can monitor.
All the ICs that make up the battery pack will be shown dynamically, with the relative information.
Furthermore, as can be seen from figure 5.10, the total voltage of the battery pack and the current output from it are shown in the bottom.

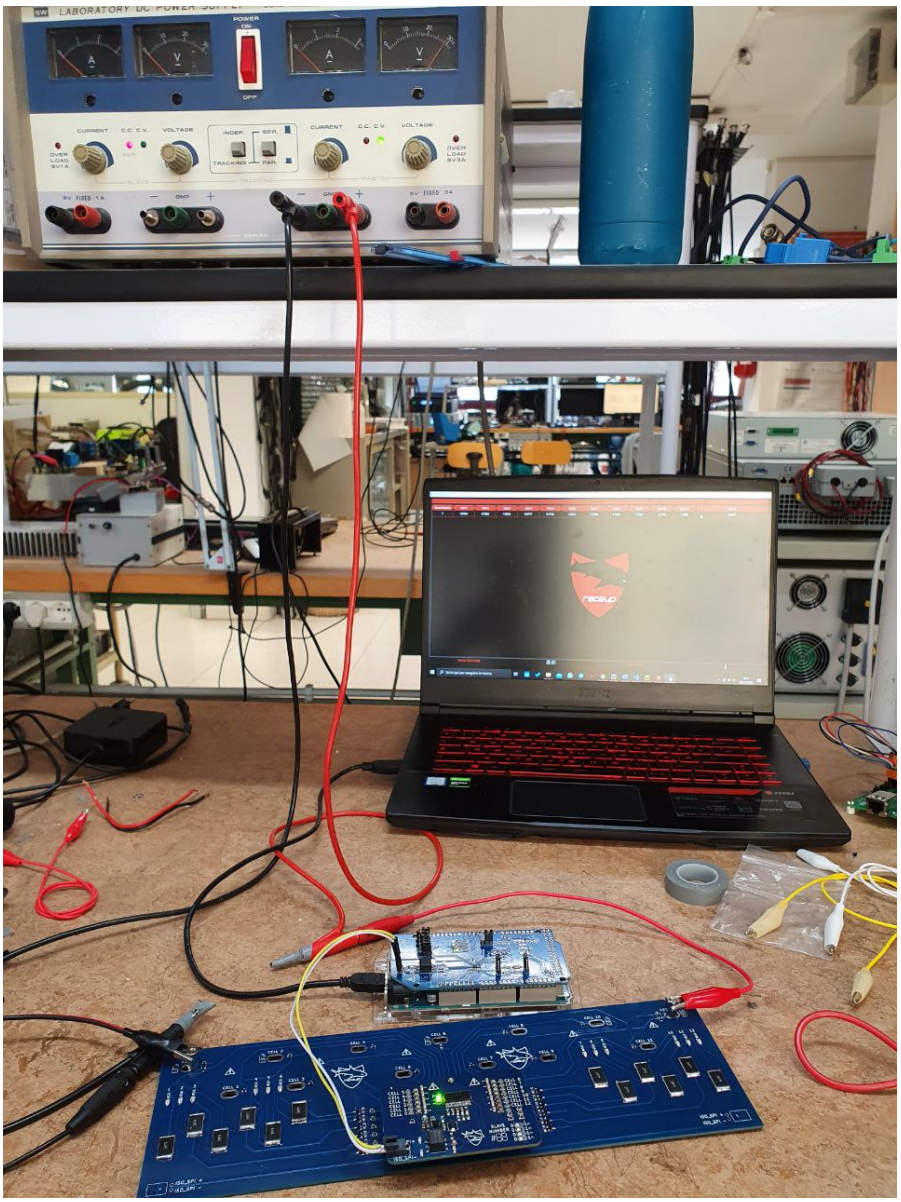


Figure 5.7: BMS System communication test

Figure 5.8: BMS System communication test on battery segment

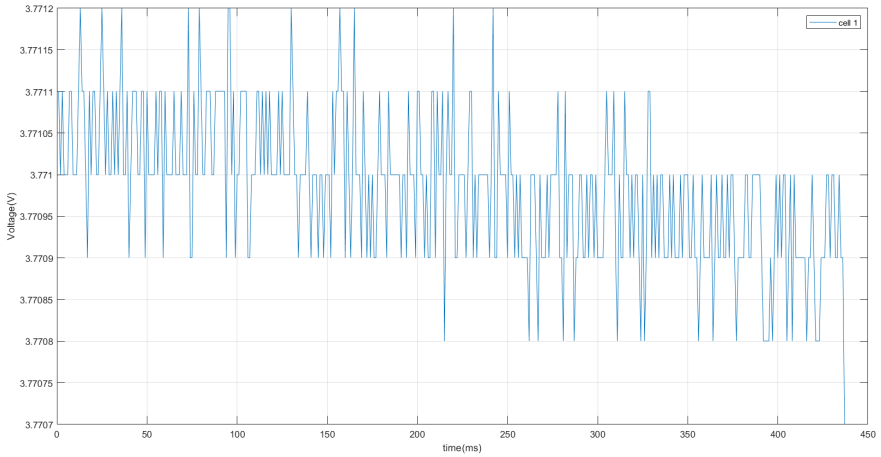


Figure 5.9: Cell reading error of the BMS system

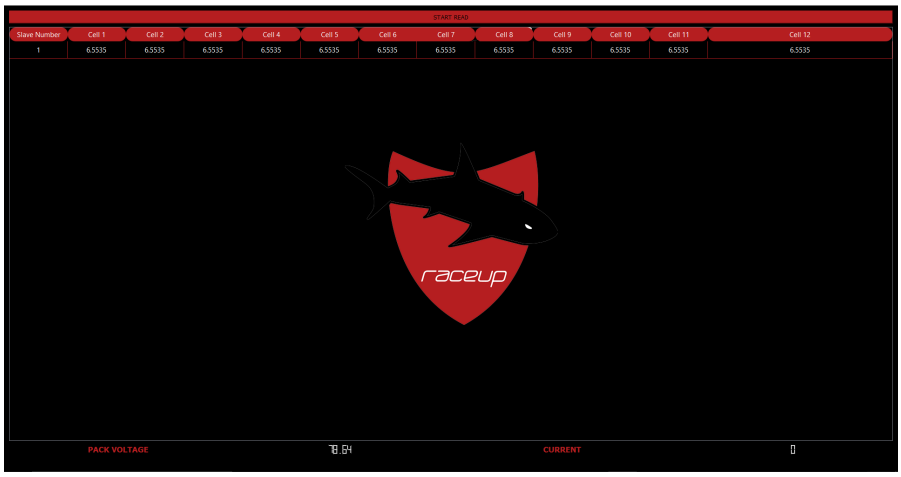


Figure 5.10: BMS User Interface

6 NEW BATTERY SEGMENT STRUCTURE

In this chapter will briefly analyze how the structure of the single segment that makes up the base piece of the entire battery pack was conceived.
First of all, the cells chosen for this battery segment are the $EP9543126VVP$ $6800mAh$ $3.90V$ $15C$ produced by Electric Power.
These cells offer a higher energy density than those previously used, the difference between the old and the new cells used for the HV battery pack is shown in table 6.1.
The datasheet for the $EP9543126VVP$ battery cells is shown in figure 6.1.
With this type of configuration, the set of only the cells that form the battery pack, and which make up most of the bulk of the same, save a considerable amount of kilograms in terms of weight, to be precise with this type of cells we would have a weight of about 27 kg against the 34 kg that occurs when using Melasta $SLPB$ $A843126$ 6350 mAh $15C$ $3.7V$.

With this type of cells, the battery pack will consist of 11 segments made up of a configuration of the $12s2p$ type, for a total of 264 cells.
Since the maximum voltage of a single cell is equal to 4.45 V, this type of configuration is able to supply a maximum voltage of 587.4 V for the entire battery pack with a deliverable direct current of 204 A and a maximum of 340 A for a maximum of 3 s.
The load-bearing structure of the segment is made up of a milled fiberglass plate in such a way as to be able to house the cell tabs and to be able to connect them in series with each other using specially milled aluminium busbars.
A containment structure will be built around the cells which will give structural rigidity to the segment, this will guarantee the cells not to move along the three directions (x, y, z) during the race of the vehicle.
This containment structure can be seen in the render of the segment shown in figure 6.2.

Table 6.1: Cells energy density comparison

BATTERY CELL MODEL	DENSITY OF ENERGY [Wh/Kg]
MELASTA $SLPB$ $A843126$ 6350 mAh $15C$ $3.7V$.	0.179
ELECTRI POWER $EP9543126VVP$ 6800 mAh $15C$ $3.9V$.	0.255

2、主要技术参数
Main Technical Parameter

2.1 电芯和电池组规格参数 Technical Parameter Of Cell and Pack:

项目 Item	电芯 Cell	成品 Pack	备注 Remark
1. 主要化学成分 Cell Chemistry	LiCoO2	N/A	
2. 标称容量 Rated Capacity	6800mAh	N/A	电芯标准充电后 0.2C 放电至 2.75V Fully Discharge to 2.75V @ 0.2C. after the cell standard charger
3. 额定电压 Rated Voltage	3.90V	N/A	平均放电电压 Average Discharge Voltage (discharged at 1CmA)
4. 内阻 Internal Resistance	Max: ≤2.5mΩ	N/A	通过电芯组合后总的正负极耳测试 Measure the resistance with the overall cathode and anode tab
5. 最大连续放电电流 Max. Constant Discharge Current	102A	N/A	15C
6. 最大峰值放电电流 Max. Peak Current	170A	N/A	25C
7. 峰值电流放电时间 Time for peak discharge current	3S	N/A	
8. 放电截止电压 Discharge Cut-off Voltage	2.75V	N/A	2.75V/Cell
9. 最大持续充电电流 Max. Constant Charge Current	27A	N/A	4CmA *
10. 最大峰值充电电流 Max. Peak Charge Current	54A	N/A	8CmA *
11. 最大峰值电流充电时间 Time for peak charge current	3S	N/A	
12. 充电截止电压 Charging Cut-off Voltage	4.45V	N/A	4.45V/Cell
13. 尺寸 Product Size	N/A	N/A	
14. 重量 Weight	104g	N/A	±4g
15. 工作温度范围 Range of Work Temperature	充电 Charge		0~+45℃ *Can be charged at 60℃, but may cause swell.*
	放电 Discharge		-20~+60℃

* The cell can achieve constant charging of 5C and peak charging of 10C for fields with low requirements of cycle life, for KERS systems.

Figure 6.1: *EP*9543126*VVP* battery cell datasheet [12]

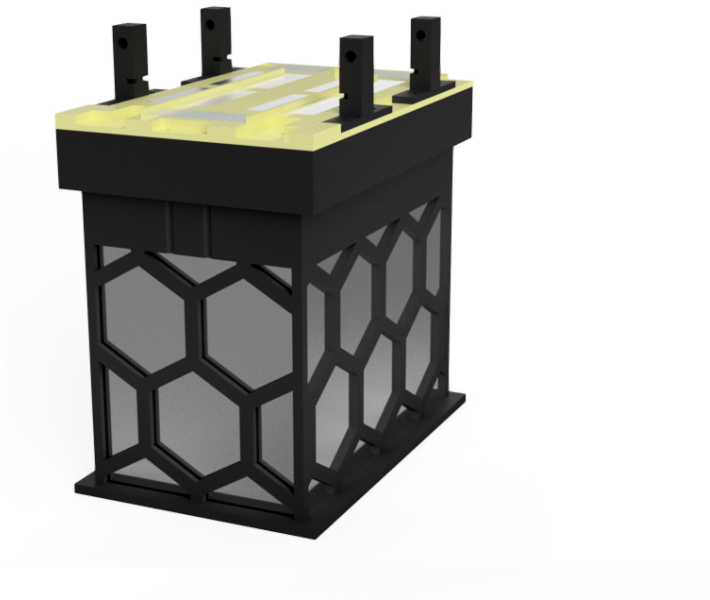


Figure 6.2: render of the new battery segment

The eleven segments will be connected in series through the use of maintenances. We are waiting for the realization of these pieces necessary for the connection between the various segments because the rules concerning these parts of the battery pack could change during the course of the season and at the beginning of the next.
In order to connect the BMS to this segment, supports have been made that will allow the interface PCB to remain in position.
To bring the cell voltages to the connector where the BMS Slaves will be connected, it was thought to use pogo pins on the interface PCB, in order to ensure uniform contact between the interface board and busbars.
The realization of the interface PCB will be carried out once the mechanical supports for housing the cells and for fixing the interface board will be ready.
This is because the creation of the segment is very delicate and changes to the structure could occur during the manufacturing phase.

7 CONCLUSIONS

In this thesis work, a general overview of the main electric components of the HV battery with a particular focus on the Battery Management System were analyzed.
The previous version of BMS has been described and its problems have been analyzed. From these, a study began to be able to reduce them in such a way as to be able to create a reliable prototype.
These studies have led to the manufacturing choices of the prototype that has been described in this paper.
Several improvement ideas have been proposed with technologies different from those used which could further improve the stability and reliability of the system.
In general, the tests that have been carried out with the development boards have reported positive results, both as regards the control code and how the integrated devices behave.
Tests on the new prototype are still being processed because we are waiting to test the system in the proper environment during the car track tests.

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