UNIVERSITÀ
DEGLI STUDI
DI PADOVA

DIPARTIMENTO
DI INGEGNERIA
DELL'INFORMAZIONE

INFORMATION ENGINEERING DEPARTMENT

DEGREE COURSE IN ELECTRONIC ENGINEERING

Design of the tests for the Passive Protection Circuit of the High Voltage Radio Frequency Test Facility

Supervisor: Prof. Paolo Bettini

Graduating: Matteo Faoro

Co-Supervisor: Ing. Marco De Nardi

Prof. Simone Buso

ACADEMIC YEAR 2021 – 2022

Graduation Date 22/9/2022

INDEX

Figure index

Table index

Abstract

ITER ("The Way" in latin) is an ambitious international project aiming to demonstrate the feasibility of fusion as large-scale and carbon-free energy source. ITER is designed to produce around $500\ MW$ of fusion power with $50\ MW$ of input power for heating the plasma. This input power is produced by means of three different Heating and Current Drive (H&CD) systems: Electron Cyclotron Resonance Heating (ECRH), Ion Cyclotron Resonance Heating (ICRH) and Neutral Beam Injector (NBI). In ITER, two NBI are foreseen, each capable of injecting neutral particles beam of $16.5\ MW$ power inside the plasma for an hour, by extracting and accelerating a negative beam of hydrogen and deuterium ions up to $1\ MeV$ of energy and neutralizing it before entering the plasma. These requirements have never been reached experimentally before. For this reason, a dedicated test facility, NBTF (Neutral Beam Test Facility), was developed to test and optimize the ITER NBI by means of two separate experiments: SPIDER (the ITER-scale radio frequency negative ion source) and MITICA (the full-scale prototype of the ITER heating neutral beam injector). In SPIDER, the plasma is generated inside four couples of inductively coupled plasma drivers, each powered by a radio frequency generator rated to provide $200\ kW$ at $1\ MHz$. SPIDER beam source is fully installed in vacuum and thus the RF drivers and the related circuits, on the backside of the beam source, operates at the residual background pressure. Moreover, during SPIDER operation, the drivers and other components of the ion source are subjected to high intensity electric fields in vacuum which can lead to the generation of electric arcs. Consequently, the High Voltage Radio Frequency Test Facility (HVRFTF) was developed as a dedicated test facility to verify the voltage hold off on mock-ups of the radio frequency circuits and special components installed inside the SPIDER ion source. This facility is able to reproduce the operating conditions of the drivers: the high voltage is produced exploiting a resonant circuit with high quality factor, while the components under test components are installed within a vacuum vessel filled with the desired gasses and pressure. Different mock-ups geometries generate different electric fields and are supplied with an increasing RF voltage up to the formation of an electric arc, that is the limit not to exceed with SPIDER to avoid damages. The effects of this arc, however, can lead to damages to the amplifier supplying the resonant circuit. Moreover, the resonant circuit is subjected to insulation failures that can cause damages too.

Both the arc on the device under test and the insulation failures are characterized by fast transients with relatively high voltage and current peaks. A Passive Protection Circuit (PPC) was developed to dissipate the energy stored in the resonant circuit and to limit possible overvoltage at the amplifier output. Nevertheless, before relying on the protection, it is necessary to verify its effectiveness with dedicated tests. The aim of this thesis is to design the procedures to test the passive protection circuit.

In the Chapter 1, a brief introduction to the NBTF and its experiments will be done. In Chapter 2, the HVRFTF role in NBTF and its functioning will be described together with the modelling of its component in MATLAB Simulink. After the identification of the possible type of faults, some simulations will be provided, and the results will be compared with the maximum rating of the main components of HVRFTF to justify the needs and the layout of a protection circuit. In Chapter 3, a more detailed analysis of the PPC modelling and functioning will be provided and its positive effect in limiting the fast transients generated by the faults will be shown. Moreover, its influence in the steady state operation and the effect of series stray inductances on the wiring of the protection will be studied. Chapter 4 will cover an analysis on the power and thermal stresses generated during the intervention of the GDT present in the PPC. In Chapter 5, the layout of the test setup will be shown and described together with the detailed design of the test procedure. Also, some of the test expected waveforms obtained with simulations will be provided. Chapter 6 summarised the most important results of this thesis work.

Sommario

ITER ("La Via" in latino) è un ambizioso progetto internazionale che mira a dimostrare la fattibilità della fusione come fonte di energia su larga scala e senza emissioni di carbonio. ITER è progettato per produrre circa $500\ MW$ di potenza dalla reazione di fusione con $50\ MW$ di potenza in ingresso per il riscaldamento del plasma. La potenza di ingresso è fornita attraverso tre diversi sistemi di riscaldamento (H&CD): riscaldamento a risonanza elettronica ciclotronica (ECRH), riscaldamento a risonanza ionica ciclotronica (ICRH) e riscaldamento tramite l'iniezione di fasci di neutri (NBI). In ITER è prevista la presenza di due NBI, ciascuno in grado di iniettare nel plasma un fascio di particelle neutre con un potenza di $16{,}5\ MW$ per un'ora. Tale fascio viene ottenuto estraendo e accelerando un fascio di ioni negativi di idrogeno e deuterio fino a 1 MeV e neutralizzandolo prima di entrare nel plasma. Tali requisiti non sono mai stati raggiunti sperimentalmente. Per questo motivo, è stata sviluppata una struttura di test dedicata, NBTF (Neutral Beam Test Facility), per testare e ottimizzare il NBI di ITER attraverso due diversi esperimenti: SPIDER (la sorgente di ioni negativi a radiofrequenza a grandezza naturale di ITER) e MITICA (il prototipo a grandezza naturale dell'iniettore di fasci neutri di ITER). InSPIDER, il plasma viene generato all'interno di quattro coppie di driver accoppiate induttivamente con il plasma, ciascuna alimentata da un generatore a radiofrequenza in grado di fornire 200 kW a 1 MHz. Inoltre la sorgente di SPIDER è installata in una camera da vuoto, così i driver RF e i relativi circuiti, montati sul retro della sorgente, si trovano ad operare alla pressione di fondo residua. Tali parti si trovano quindi sottoposte a campi elettrici in vuoto ad alta intensità che possono portare alla generazione di archi elettrici che vanno evitati altrimenti la sorgente si potrebbe danneggiare. Per questo è stata sviluppata l'High Voltage Radio Frequency Test Facility (HVRFTF) con lo scopo di essere un esperimento accessibile, dedicato a verificare la tenuta della tensione di mock-up dei circuiti a radiofrequenza e dei componenti principali installati all'interno di SPIDER. Tale facility è in grado di riprodurre le condizioni operative dei driver di SPIDER: l'alta tensione viene prodotta utilizzando un circuito risonante ad alto fattore di qualità, mentre i componenti in prova sono installati all'interno di un vessel sotto vuoto che può essere riempito con differenti gas e alla pressione voluta.

Differenti geometrie di mock-up generano campi elettrici diversi e vengono alimentati con una tensione RF crescente fino alla formazione di un arco elettrico, che rappresenta il limite da non superare in SPIDER per evitare danni.. Gli effetti di tale arco, tuttavia, possono causare danni all'amplificatore che alimenta il circuito risonante. Inoltre, il circuito risonante può essere soggetto a guasti dell'isolamento che possono anch'essi causare danni. Questo perchè sia l'arco sui mock-up che i guasti relativi all'isolamento sono caratterizzati da transitori veloci con picchi di tensione e corrente particolarmente elevati. Per limitare i danni di tali transitori è stato progettato un circuito di protezione passivo (PPC) in grado di dissipare l'energia immagazzinata nel circuito risonante e limitare eventuali sovratensioni che si dovessereo presentare sullo stadio di uscita dell'amplificatore. Tuttavia, prima di affidarsi alla protezione, è necessario verificarne l'efficacia con test dedicati. Lo scopo di questa tesi è quello di progettare le procedure per testare il circuito di protezione passivo.

Nel Capitolo 1 verrà fatta una breve introduzione a NBTF ed ai suoi esperimenti. Nel Capitolo 2 verrà descritto il ruolo di HVRFTF nel contest di SPIDER ed il suo funzionamento, assieme alla modellazione dei suoi componenti in MATLAB Simulink. Successivamente, dopo aver identificato i possibili tipi di guasto, verranno effettuate delle simulazioni, i cui risultati verranno discussi e confrontati con i massimi valori sopportabili dai componenti principali di HVRFTF con lo scopo di giustificare la necessità di un circuito di protezione. Infine, verrà presentato brevemente il layout della PPC. Nel Capitolo 3 verrà presentata più nel dettaglio la modellazione e il funzionamento della protezione passive. La sua efficacia nel limitare i transitori veloci dovuti ai guasti verrà analizzata con il supporto di simulazioni. Successivamente, verrà valutata la sua influenza nel funzionamento a regime e verranno presentati gli effetti della presenza di induttanze parassite in serie dovute ai collegamenti della protezione. Il Capitolo 4 tratterà lo studio degli stress termici e della potenza dissipata durante gli interventi del GDT presente nella protezione. Nel Capitolo 5 verrà illustrato e descritto il setup di prova, assieme alla progettazione dettagliata delle procedure di test. Verranno inoltre presentate alcune delle forme d'onda, ottenute tramite simulazione, che ci si attenderà di ottenere durante i test. Infine il Capitolo 6 riassumerà i risultati più importanti ottenuti in questo lavoro di tesi.

CHAPTER 1:

Introduction

1.1 ITER and The NBTF project

ITER ("The Way" in Latin) is an ambitious international energy project and a fundamental step within the path that will lead to the development of a future commercial thermonuclear fusion power plant. It will be the world's largest tokamak (with a size of almost two times the fusion machines operating today) and the first fusion device able to produce net energy from thermonuclear fusion reaction between Deuterium and Tritium in a magnetically confined plasma, with the goal to demonstrate the feasibility of thermonuclear fusion as large-scale and carbon-free energy source. The site designated for the installation of the project is Saint Paul-Lez-Durance, southern France. The construction activities have been started in 2010 and the first plasma is foreseen at the end of 2025. In figure 1 can be seen the ITER tokamak building which it will be 73 m high (60 meters above and 13 meters below) and in its centre (in purple) is the plasma with a volume of 830 cubic meters which it need to be heated to sustain the reaction.

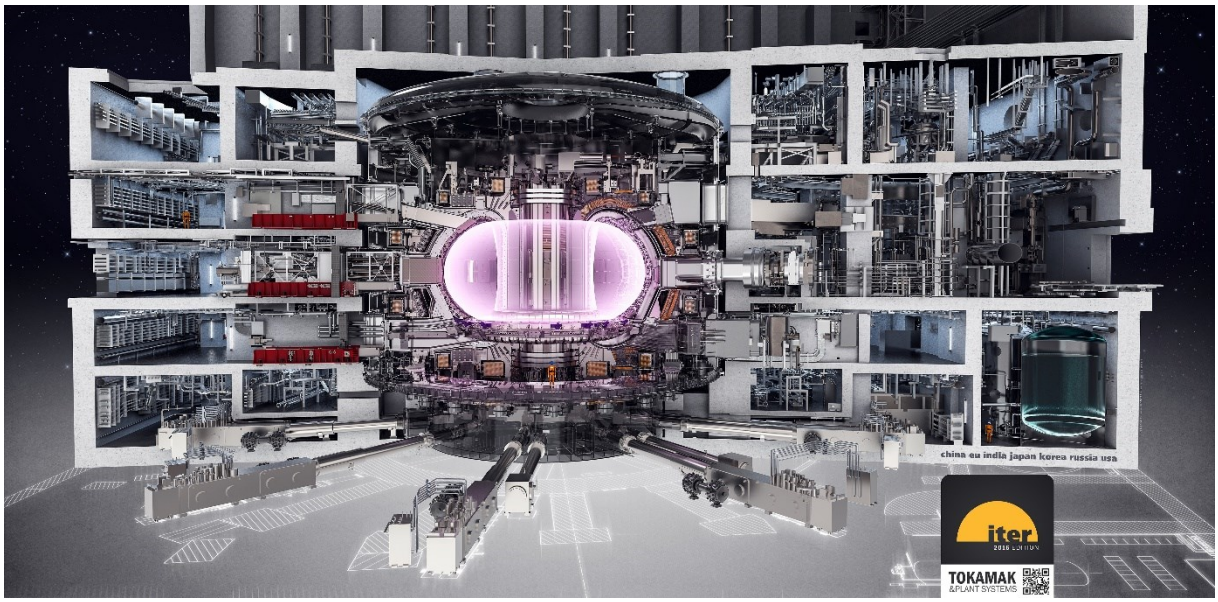

Figure 1 - ITER reactor [1]

In ITER, as in the other tokamaks, to prevent the fusion reaction to be extinguished, the plasma needs to be properly heated by external heating systems. The ITER plasma heating system, represented in figure 2, is consists in:

- Electron Cyclotron Resonance Heating (ECRH)
- Ion Cyclotron Resonance Heating (ICRH)
- Heating Neutral Beam (NBI)

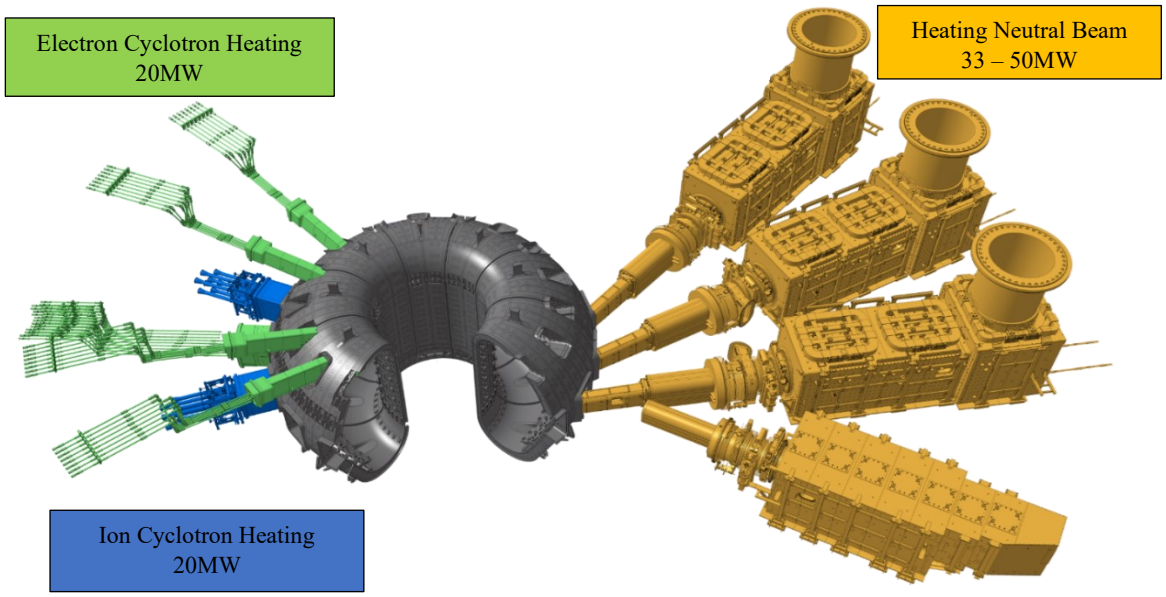

Figure 2 - ITER torus with the 3 different heating system

A mixed heating system is required to sustain the reaction for 1 hour. ICRH and ECRH are high intensity electromagnetic radiation heaters (to respectively heat ions and electrons to their respective cyclotronic frequencies), while the NBI (Neutral Beam Injector) injects accelerated neutral particles into the plasma. The NBI provides most of the heating power, with respect to the other heating systems. It is rated to deliver a power of $16{,}5\ MW$ for 1 hour to the plasma by accelerating deuterium ions beam up to the energy of $1\ MeV$ and then neutralizing it to penetrate and heat the plasma. The reference design consists in 2 NBI (with the possibility to install a third one to reach $50\ MW$). The figure 3 shows an open view of the NBI with its parts.

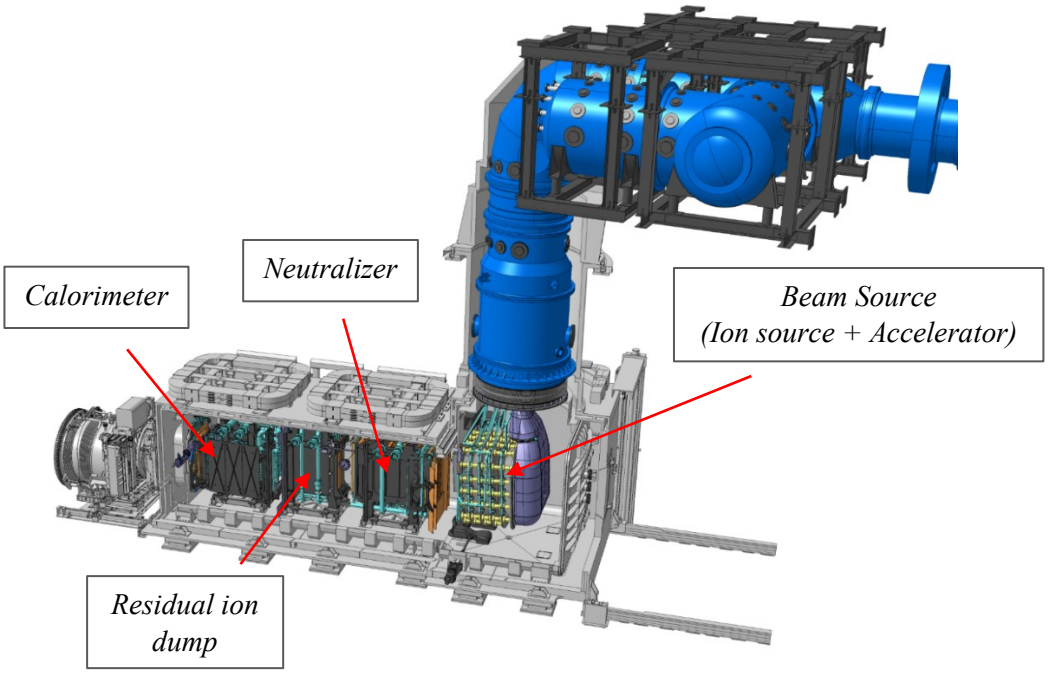

Figure 3 - Open view of the ITER Neutral Beam Injector

The aforementioned requirements have never been obtained experimentally in a single facility, hence the need to create a laboratory where to design, build and test such a complex device is justified.

The ITER Neutral Beam Test Facility (NBTF shown in figure 4) is hosted in Padova, Italy and includes two experiments: SPIDER (figure 5), the full-size prototype of the radio frequency negative-ions source, on which several experimental campaigns were carried out since 2018, and MITICA (figure 6), the full-scale prototype of the ITER NBI, currently in the power supplies integrated commissioning phase.

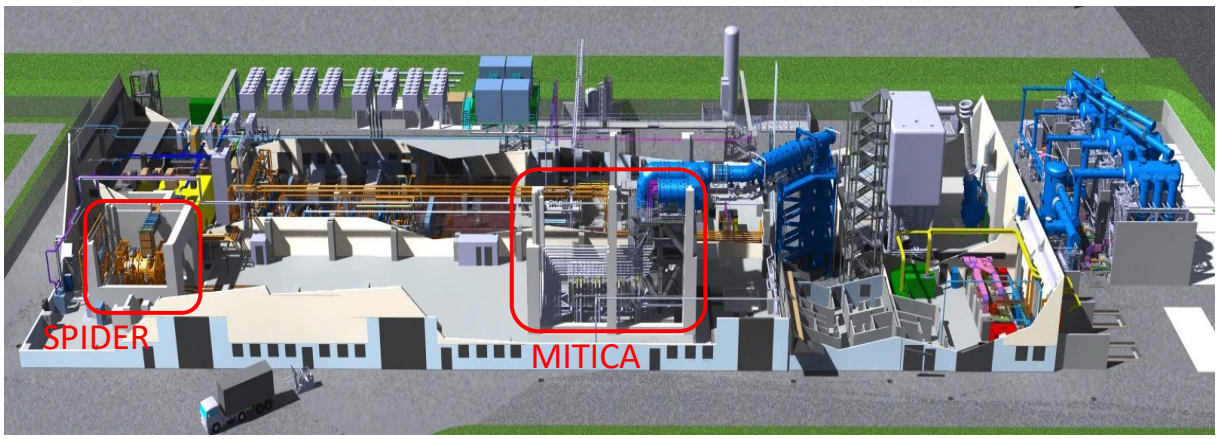

Figure 4 - Neutral Beam Test Facility arrangement [2]

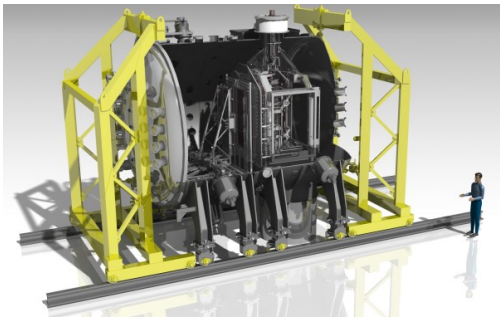

Figure 5 - NBTF SPIDER experiment [2]

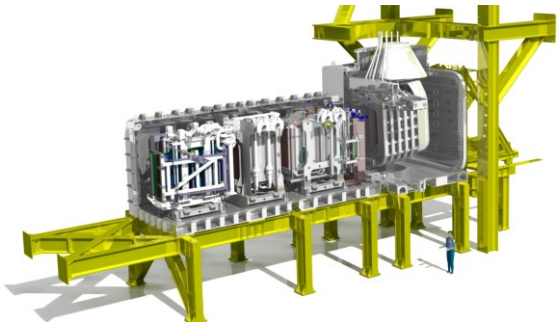

Figure 6 - NBTF MITICA experiment [2]

SPIDER, the full-scale prototype of the negative ion source of the NBI, include a Radio Frequency (RF) Ion Source which consist of 4 driver pairs (figure 8); the plasma is produced inside the drivers around which RF coils coupled with the plasma are wound. The RF power is supplied to the plasma by coupling these RF coils to the plasma contained within the drivers. Each coil is fed at 1 MHz up to a power of 200 kW, which corresponds to a voltage of about 17 kV rms, with nominal plasma parameters.

To provide high reliability of the source, such a high operating power requires accurate analyses of the potential issues related to breakdowns occurrence in the driver region due to the high electric field present on its components.

In figure 7, the exploded view of SPIDER experiment is provided. The grids system consists of various type of grids with different purposes. The plasma is generated inside the plasma source, and then negative ions are extracted, and accelerated (through the grid system) to create the ion beam.

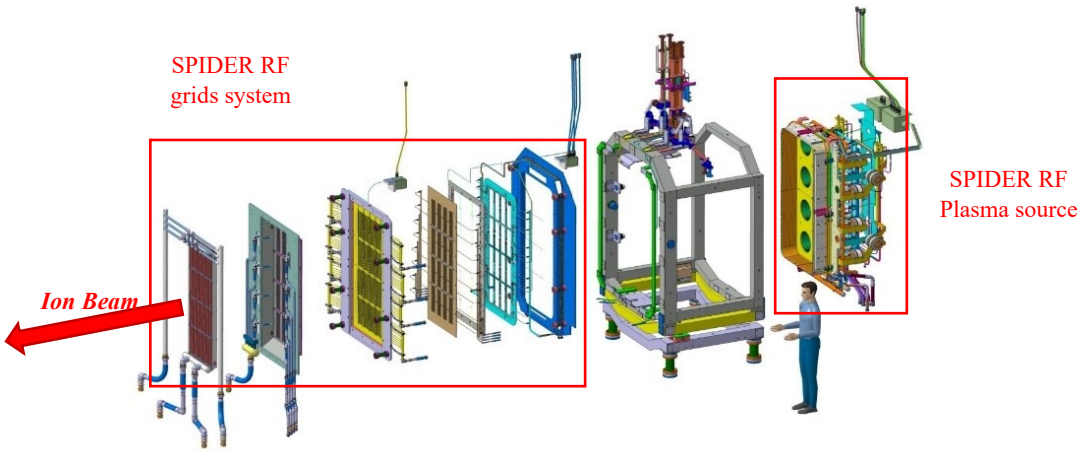

Figure 7 - Exploded view of the SPIDER experiment [2]

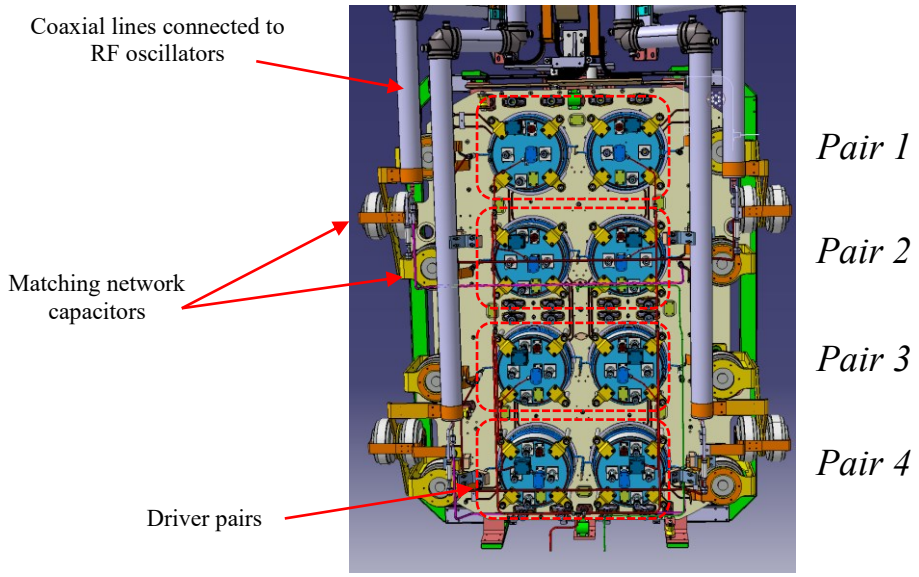

Figure 8 - Back view of SPIDER RF plasma source [3]

Figure 8 shows the back view of the SPIDER RF beam source with the coaxial line and the matching capacitor for the maximum power transfer. The four driver pairs are depicted in blue.

CHAPTER 2:

HVRFTF

2.1 Radio Frequency Test Facility

The High Voltage Radio Frequency Test Facility (HVRFTF) has been developed to be a flexible experiment used to characterize the electrical insulation at low pressure of components (like the drivers of the SPIDER and MITICA Plasma Sources) operating at radiofrequency, while reproducing the working conditions in terms of voltage, pressure ($< 0{,}3$ Pa), and E-field relevant to the RF circuits of SPIDER and MITICA ion sources.
HVRFTF consists of different parts. With reference to figure 9, we can see the auxiliary cubicle (RACK 1) which contains the waveform generator and other instruments, the control desk which is used to view the data obtained from the sensors and the yellow fence.

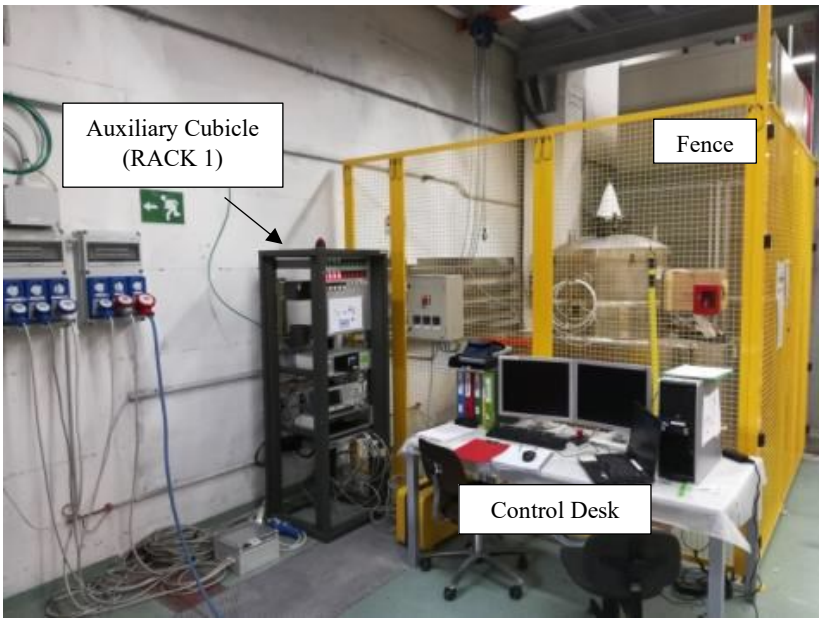

Figure 9 - HVRFTF front view

In figure 10, the diagnostic cubicle (RACK 2), which contains the diagnostics and the RF power amplifier, the vacuum vessel, and the EM shielding to mitigate the radiated disturbances are shown. The high voltage RF circuit, which will be described in detail in the next paragraph, is installed inside the EM shielding.

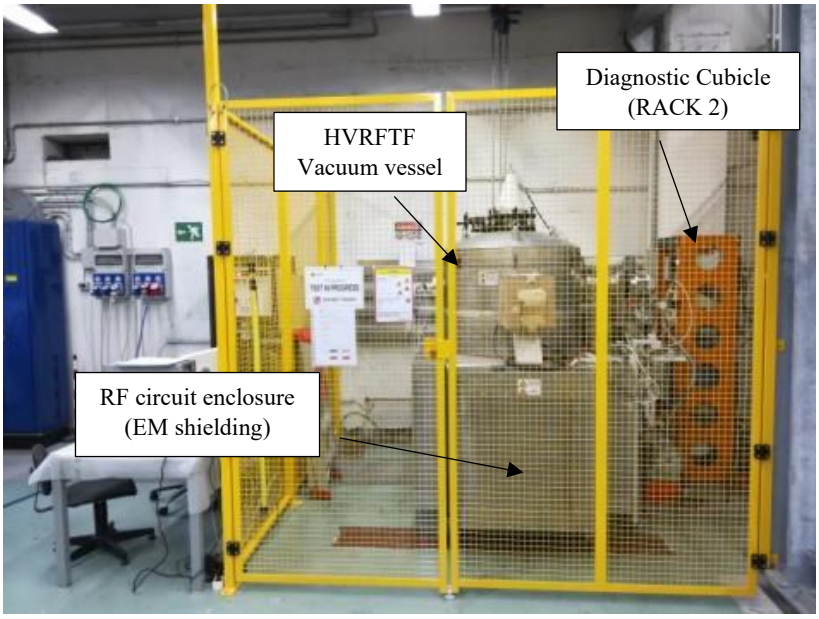

Figure 10 - HVRFTF side view

2.2 HVRFTF resonant circuit

To reproduce the working condition of SPIDER and MITICA RF driver coils in terms of operational voltage, the RF resonant circuit depicted in figure 11 is used. The nominal values of the components used in the HVRFTF resonant circuit are specified in table 1.

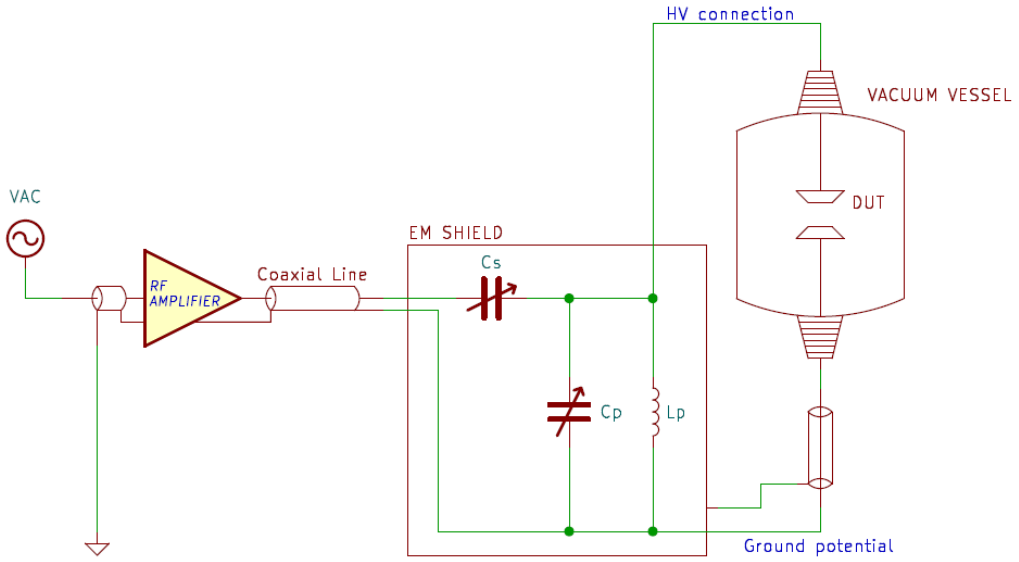

Figure 11 - Sketch of the HVRFTF RF circuit

Table 1 - Component values of HVRFTF RF circuit

The component values are:

Component	*Value*
Cs	55pF (Variable Cap.)
Cp + C_{DUT}	323pF (Variable Cap.)
Lp	67uH (Measured)
R_{Lp}	1.28Ω (Measured)

The high radiofrequency voltage required for the HVRFTF experiment is produced exploiting the series resonance between C_s and the LC parallel circuit ($L_p, C_p + C_{DUT}$) supplied by a low voltage power amplifier. Cs purpose is also to match the characteristic impedance of the RF line (50Ω) for the maximum power transfer from the supply amplifier to the load (the RF circuit with the Device Under Test, DUT).

The DUT consists of two electrodes with various geometry (the distance between them can be varied) with the goal to replicate as close as possible the E-filed present in the driver between the winding and the driver cases of SPIDER.

The plot reported in figure 12 shows the absolute value of the reflection coefficient over the frequency of the input signal (obtained with the circuit value presented in table 1). The plot (figure 12) was obtained with the formula: $\Gamma(f) = \frac{Z_{load}(f) - Z_0}{Z_{load}(f) + Z_0}$ where $Z_{load}(f)$ is the equivalent impedance of the resonant circuit and $Z_0 = 50\ \Omega$ is the characteristic impedance of the coaxial line. $\Gamma(f)$ represents how much of the input EM wave is reflected from the load (as a function of frequency). With the reflection coefficient equals to 1 everything is reflected back to the generator so no power will be transferred to the load, with 0 nothing is reflected so all the transmitted power is absorbed by the load. The reflection coefficient is calculated using impedances, which are function of frequency. The frequency at which the impedances lead to its minimum value is called matching frequency.

As we can see in figure 12 the matching frequency corresponds to 1MHz.

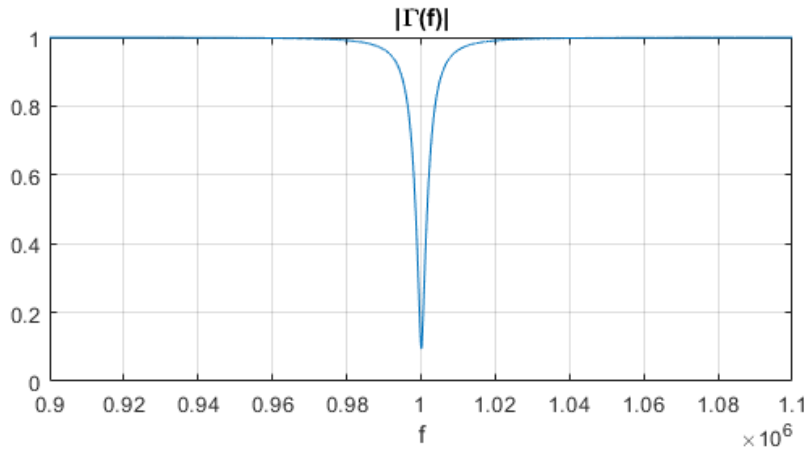

Figure 12 – Absolute value of the reflection coefficient over the working frequency

The values of C_p and C_s are tuned to produce up to $17kV$ rms in a frequency range of 0.9 to $1.1MHz$ (L_p is not a variable inductor whereas the are).

During operation, the amount of plasma produced can vary overtime changing the overall load impedance thus changing the matching frequency.

The high voltage produced is applied to the DUT with a variable distance and suitable shapes placed inside a vacuum vessel filled up with the desired gas at the desired pressure.

2.2.1 HVRFTF modelling and simulations

In the following paragraph a modelling of the transmission line in MATLAB Simulink will be realized.

The line modelling is necessary for all the upcoming simulations needed to characterize the steady state operation, the consequences of a fault and the effect of a presence of a passive protection in the system. Also, the steady-state simulations and the voltage and current transients generated by a DUT breakdown in the vessel are presented in this paragraph.

Figure 17 shows the circuit model of HVRFTF used for the steady-state simulations: on the left, there is the amplifier with a series resistor of $10^{-4}\ \Omega$, which is present only to correct computational results (required by Simulink); on the right, there is the resonant circuit which is connected with the amplifier through a coaxial line (grey square). A series of measurements are placed for measuring the most relevant waveform.

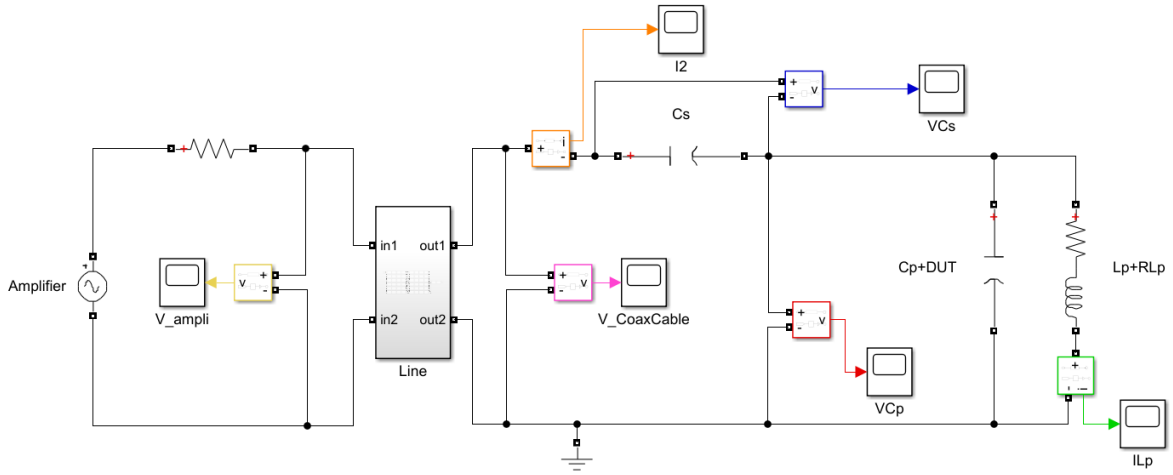

Figure 13 - HVRFTF steady-state working circuit

The transmission line that connects the power amplifier to the high voltage circuit is a $l = 5m$ length coaxial cable ([4]) for high-end RF applications.

Table 2 present the geometries and property of the line:

Table 2 - Values of the line parameters

	Dimensions	a	$4.5*10^{-3}$ m
		b	$11.3*10^{-3}$ m
Conductor	Copper	μ_c	$1.2566*10^{-6}$ H/m
		σ_c	$5.8*10^{7}$ S/m
Insulation	Foamed PE	μ	$1.257*10^{-6}$ H/m
		ε	$1.29*\varepsilon_0$ F/m
		σ	*Not used*

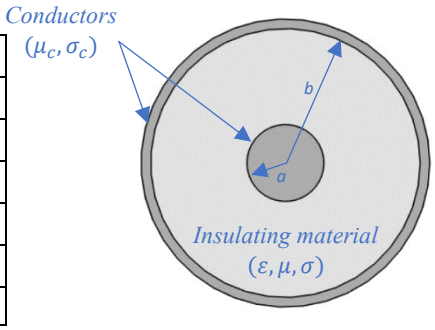

Figure 14 - Cross-section of a coaxial conductor

To provide a reliable representation of the behaviour of the cable to the voltage and current transients, a lumped parameters model with multiple cells was used. The figure 15 shows the circuit layout of a single cell.

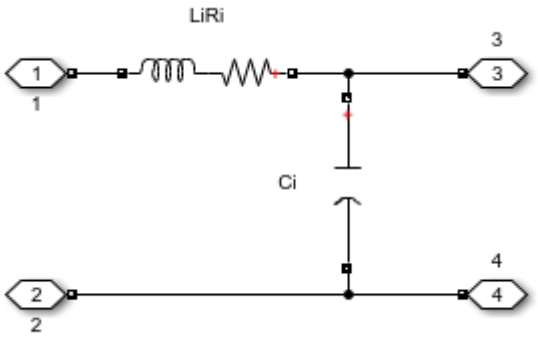

Figure 15 - Expanded view of a single pi-cell

To calculate the parameters of the single cell (L_i, R_i, C_i) first is needed to estimate the overall parameters of the line.

The parameters have been calculated with the following formulas ([5]):

- $R = \frac{R_s}{2\pi}\left(\frac{1}{a}+\frac{1}{b}\right) = 0.013\ {}^{\Omega}/_{m}$
  - $R_s = \sqrt{{}^{\pi * f * \mu_c}/_{\sigma_c}} = 261\mu\Omega$
- $C = \frac{2\pi\varepsilon}{ln(b/a)} = 77.37\ {}^{pF}/_{m}$
- $L = \frac{\mu}{2\pi} ln(b/a) = 0.185\ {}^{\mu H}/_{m}$

The line resistance R considers the overall resistance per unit of length of the inner and outer conductor. R_s represent the surface resistance of the conductors called intrinsic resistance. C is the capacity of the line per unit of length expressed as the ratio between the charge and the potential difference. L is the inductance of a coaxial line per unit of length.

The parameters of a single cell were calculated with: $X_i = {}^{X * l}/_{N}$.

N is the number of cells that need to be used, given the maximum frequency of the transmitted signal through the line.

For the steady-state simulations the working frequency is the same of SPIDER plasma source which is $1MHz$; N can be calculated with the formula [6]: $f_T = {}^{N * c}/_{8 * l}$ (with c the speed of light). f_T represent the cut-off frequency of the transmission line which can be seen as a low-pass filter. With $1MHz$, N turned out to be lower than 1, so 1 cell was used. A single parasitic capacitance of $4\ pF$ (figure 16) in parallel with the line was also introduced to account for the capacitance of the connector.

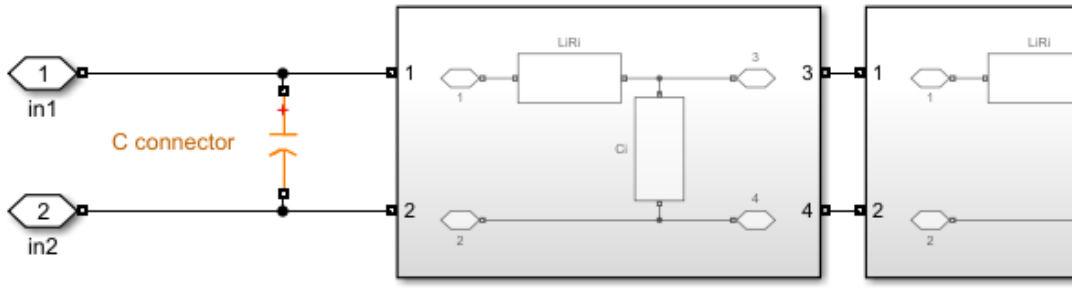

Figure 16 - Connector's parasitic capacitance

In the steady-state operation, the circuit can produce up to $17kV$ peak at 1MHz with an input voltage of $350V$ peak (provided by the amplifier). In figure 17, the relevant waveforms of the HVRFTF circuit in steady-state operation are shown.

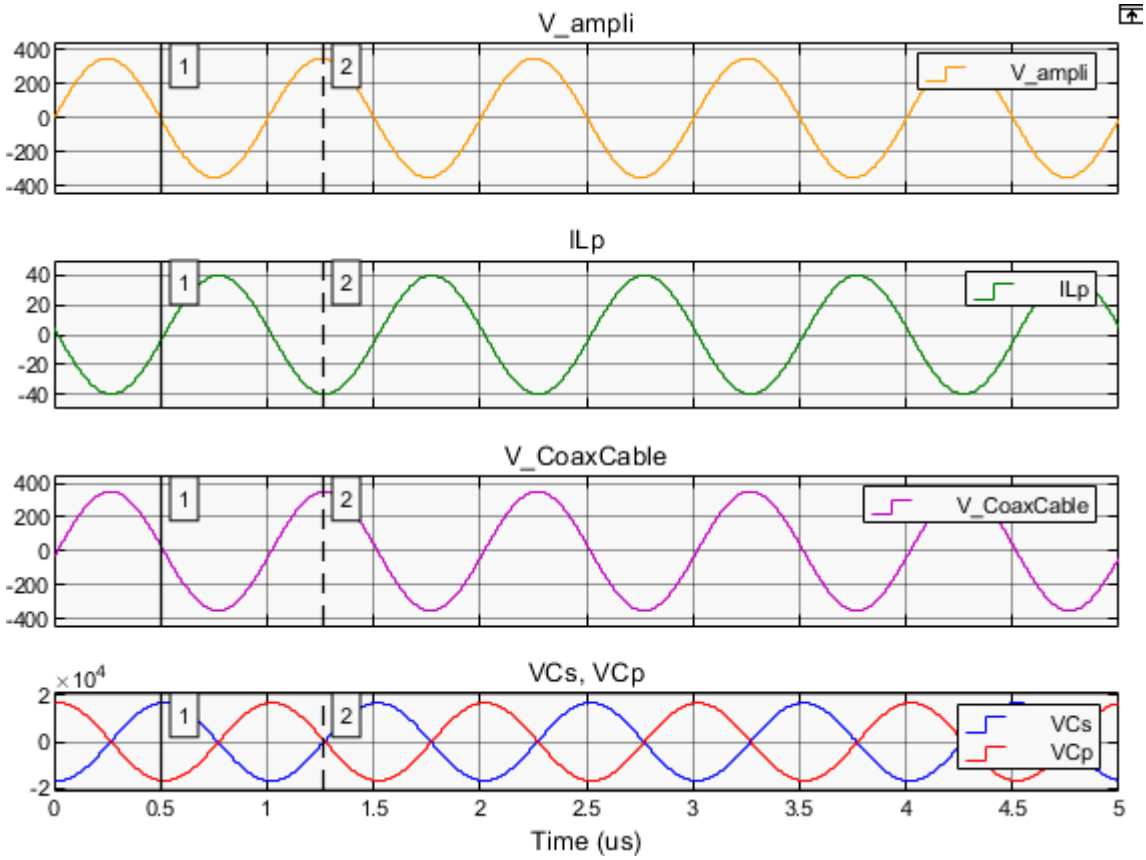

Figure 17 - HVRFTF steady-state waveforms

By observing the last plot in the bottom of figure 17, VCp and VCs are equal in magnitude and phase shifted by 180°. The phase displacement is due to the series resonance between Cs and the Load (the group of Cs, Cp and the DUT). The 90° phase shift between VCp and ILp is due to the parallel resonance within the Load group.

Regarding the DUT breakdown simulations, the maximum voltage and current transient frequency is unknown, and it can be very high. Therefore, several simulations were performed iteratively, by incrementing the number of cells until no more relevant high frequency peak appears. With this method, an overall of $N = 50$ cells were identified, which correspond to a maximum transient frequency of $f_T = {}^{50 * c}/_{8 * 5} = 375\,MHz$. Figure 18 shows the complete line model with 50 cells.

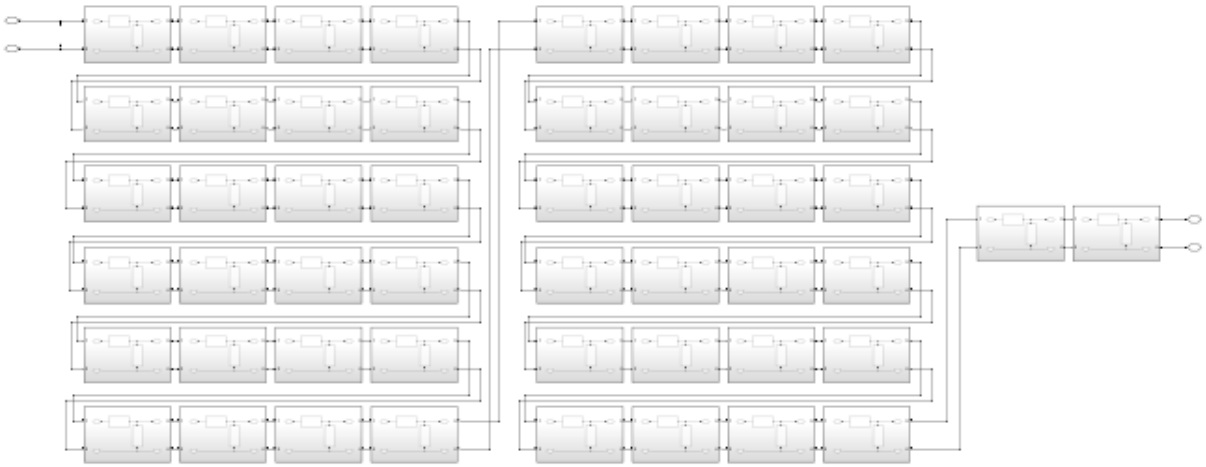

Figure 18 - Complete lumped parameter model of the transmission line

The DUT breakdown is implemented in the simulations using a short circuit in parallel with the DUT. This simulation was performed in the worst-case scenario assuming that the breakdown occurs during maximum voltage on the capacitor and minimum current in the inductor (cursor 1 figure 18). Also, the amplifier present in the steady-state simulations, was removed and replaced with an open circuit. The following paragraphs will cover those cases in more detail. Figure 19 shows the most relevant waveform during a DUT breakdown.

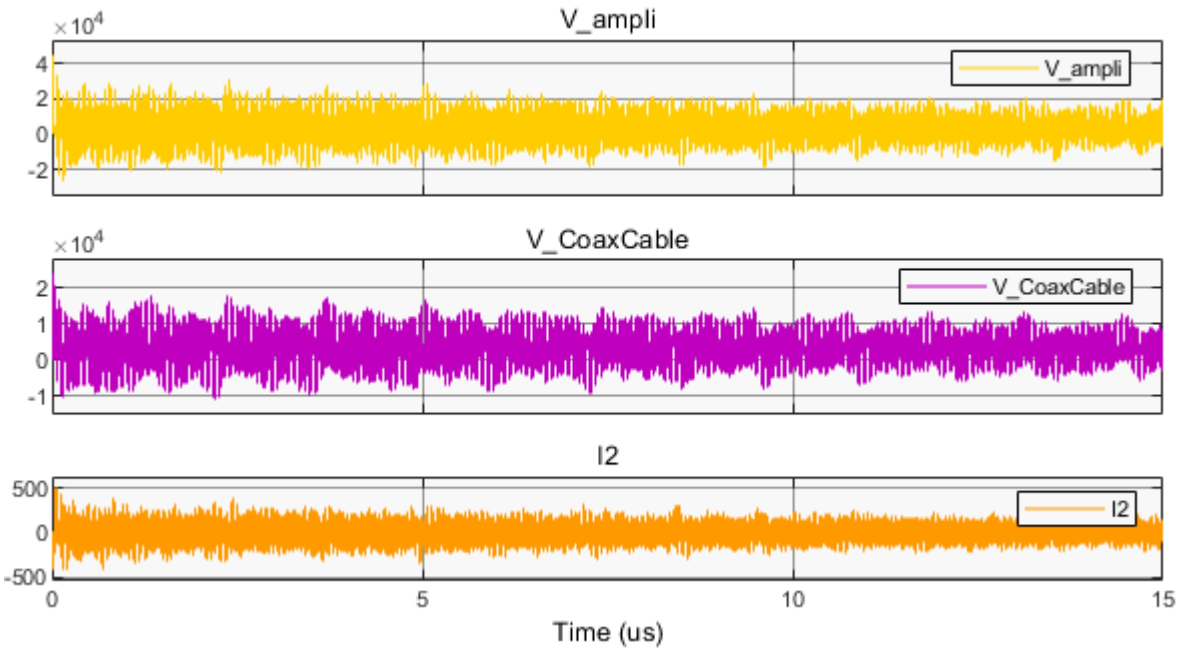

Figure 19 - Voltage and current waveform due to a DUT breakdown

As we can see, the voltage and current stresses at the output of the amplifier and on the transmission line are very high and a protection circuit is required.

2.3 Identification of possible faults

To provide an electrical qualification of the DUT in terms of maximum operative voltage it is necessary to test its voltage hold off up to the breakdown event. A set of breakdown events have been identified being either operational DUT breakdowns (already covered in the previous paragraph) or possible fault conditions on RF components. The relevant breakdown conditions, that will be investigated in the next sections of the thesis, are listed in the following and localized in figure 20:

1. Electric arc between the Cs terminals (subsequently called F1)
2. Electric arc between the Cp terminals (subsequently called F2)
3. Electric arc between an Lp part to ground
4. Electric arc between the DUT terminals (normal operation breakdown)

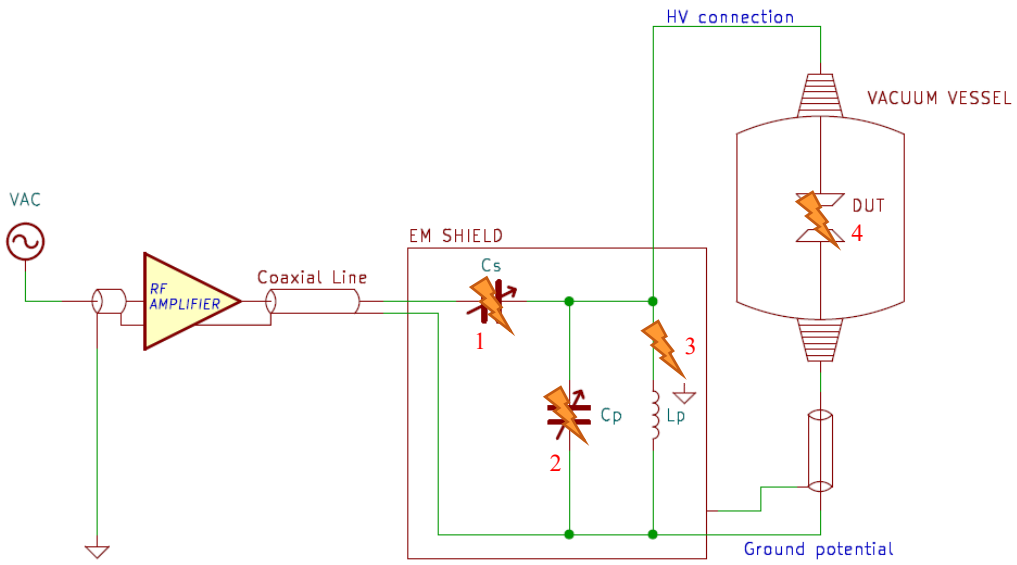

Figure 20 - Possible RF circuit faults

In the electrical analyses and in the following simulations the electric arc is represented by a short circuit in parallel to the faulty component. Since the fault on DUT, Cp and Lp (2,3,4) lead to the same circuit, just one type of fault is considered and named F2.

The analysis of the consequences of the faults will be done with simulations to study the fast transients that evolve over time, simulating the response of the circuit to specific initial conditions related to the voltage in the capacitors and currents in the inductors. As an initial condition in terms of voltage and current when a fault occurs, two cases were considered. With reference to the figure 20 the two cases are identified by the two cursors (1 and 2).

Figure 21 shows the current and voltage waveform (a zoomed version of figure 17) during steady-state operation.

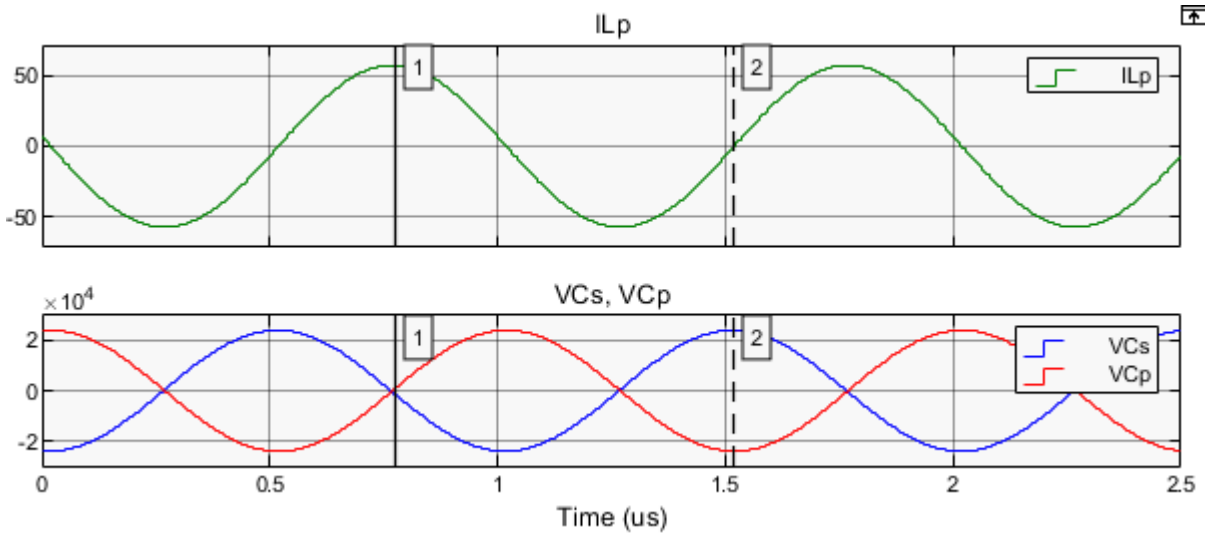

Figure 21 - Current and voltage waveforms of the RF circuit components in steady-state operation

In the analyses present in the next paragraph two other types of faults called F3, F4 were also considered, they are the same type of faults of F1 and F2 but in condition of maximum voltage and maximum current. Assuming they can be generated by a rapid change in the working frequency during normal operation that shifts 90° the phase of (for a short time) ILp with the phase of the voltage waveforms.

2.3.1 HVRFTF fault simulations

Since a scheme of the amplifier output was not available, it has been replaced in the model of figure 22 with an open-circuit equivalent scheme. In this condition the voltage measured in "V_ampli" port is overestimated with respect to the real case, so the results are conservative. The voltage and current initial condition of the components for the fault's simulation are here summarised in table 3:

Table 3 - Current and voltage peak value for each type of fault

Fault	VCs peak	VCp peak	ILp peak
F1, F2	-24 kV	24 kV	0 A
F3, F4	-24 kV	24 kV	60 A

To consider the worst-case scenario, the maximum peak voltage in figure 21 for the capacitors was used. The value of the current is the maximum peak value reached in a steady-state operation (see figure 21). Note that the condition of maximum current and minimum voltage (which is less than $500\,V$ for both VCs and VCp, cursor 1 in figure 21) is not considered because the voltage is too low to generate an electric arc. Also, the fault simulation in these conditions show that voltage and current stresses are significantly less than those developed with the other fault conditions.

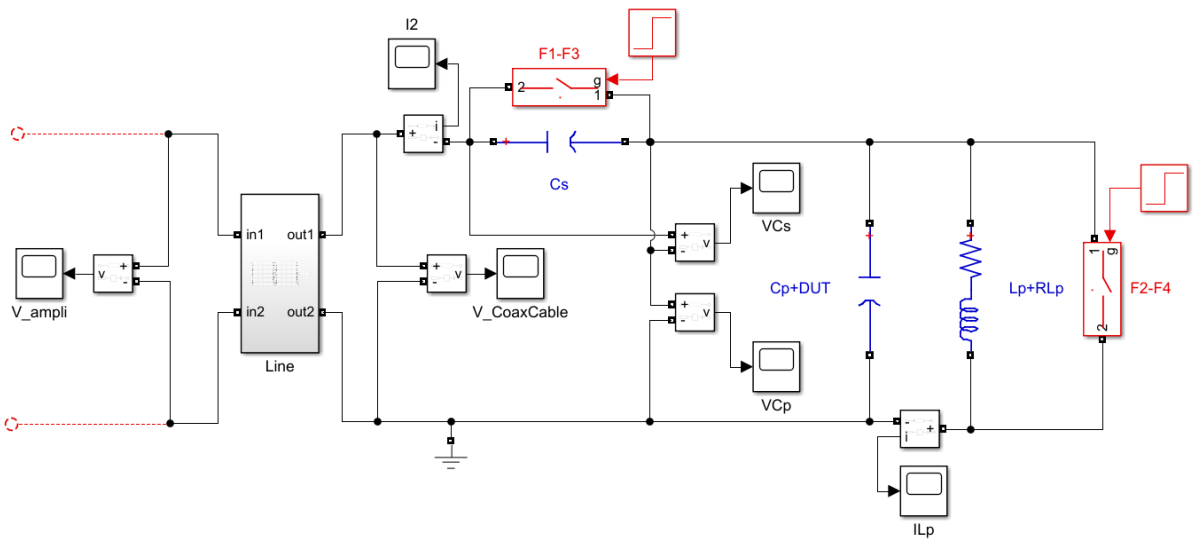

Figure 22 - HVRFTF circuit for the fault simulations

As aforementioned, the F1 and F2 faults (also for F3 and F4 which are of the same type) corresponds respectively to a short circuit in parallel to Cs and Cp. The two fault conditions are activated separately to study either one of the faults.

The obtained waveforms are shown below in figure 23-24-25-26, whose labels are the same as in figure 22:

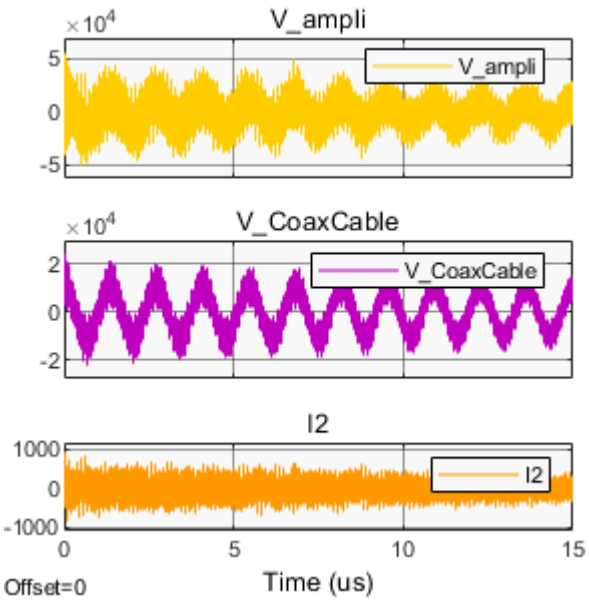

Figure 23 - F1 fault

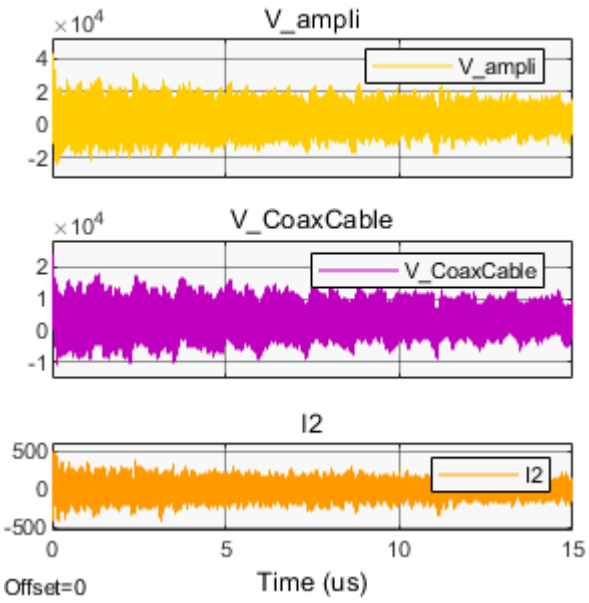

Figure 24 - F2 fault

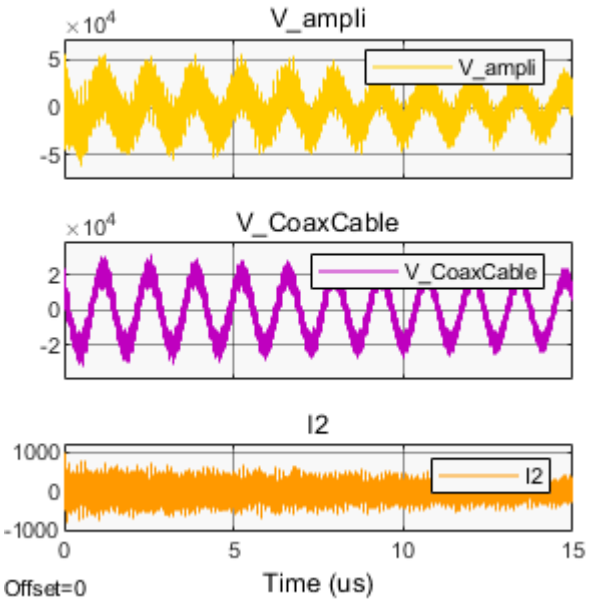

Figure 25 - F3 fault

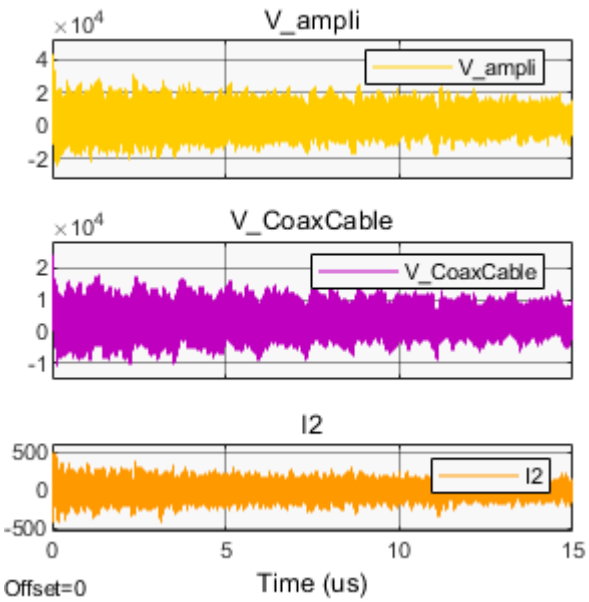

Figure 26 - F4 fault

The peak values are here summarised in Table 4:

Table 4 - Maximum peak value reached for each fault

	Maximum peak value		
Fault	V_ampli	V_CoaxCable	I2
F1	56.6 kV	24 kV	950 A
F2	43.9 kV	24 kV	500 A
F3	-61 kV	32.2 kV	991.7 A
F4	43.9 kV	24 kV	500 A

To be noted, during F1 and F3 faults the overall waveform of "V_ampli" and "$V\_CoaxCable$" consists of a $20MHz$ carrier and a $700kHz$ modulating signal.

The F1 fault will be considered the worst case instead of F3 since, considering the initial conditions for F3 and F4, they are too exotic and almost impossible to obtain experimentally during the test. Since F4 is obtained by shorting the inductor, the amount of energy stored in it, ideally produces no difference as all energy is dissipated through the short circuit. For these reasons, F3 and F4 will be no longer taken into consideration in future analyses and simulations.

2.4 Electrical rating of the main components

In this section the maximum electrical stresses for the main components of the RF circuits are summarised (see table 5) so they can be compared with those in table 4 to justify the need of a protection. It is necessary to take in consideration these values to evaluate how burdensome the transients due to faults are and then motivate the use of a protection circuit.

Table 5 - Maximum rating of HVRFTF principal components

Max peak voltage value RF Amplifier	1.2 kV
Max peak voltage value RF Coaxial cable	5 kV
Max peak voltage value on Lp, Cs, Cp	24 kV
Max RF power	2 kW

As shown in table 5, the peak voltage on the coaxial cable and on the output of the RF amplifier is highly over the limit, thus highlighting the need for a protection circuit. The design of the identified protection circuit will be presented and described in the next paragraphs.

2.5 Passive Protection Circuit

The Passive Protection Circuit (PPC) of HVRFTF needs to respect multiple requirements: it needs to limit over voltages and over currents when faults occur, but it also needs to provide minimum interferences during the normal operation of the RF circuit and without affecting the impedance matching. The PPC is already done and mounted it needs only to be tested.

It consists of 3 main components:

- Transient Voltage Suppressor (TVS [7])
- Gas Discharge Tube (GDT [8])
- Snubber circuit

The upgraded HVRFTF resonant circuit with the PPC is represented in figure 27.

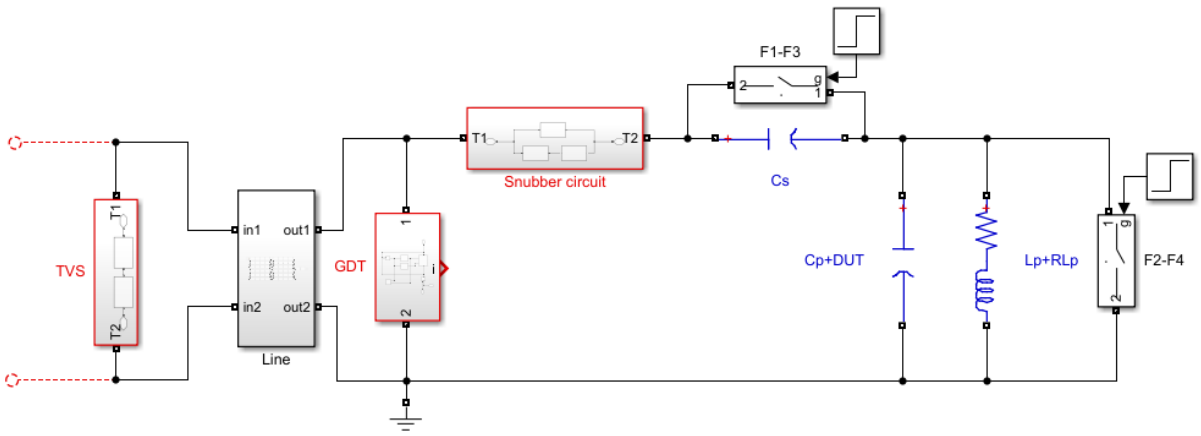

Figure 27 - HVRFTF circuit with the passive protection circuits

The snubber circuit is placed in series with Cs to reduce the high peak current transient (I2), while the GDT is placed in parallel to the coaxial cable to cut off all the voltage peaks higher than 1kV to protect the amplifier and the line. The TVS is placed in parallel to the amplifier output as backup protection. If for many reasons the GDT doesn't work correctly (fails to open) or if it is not able to limit the overvoltage on the amplifier side, the TVS shall intervene and protect the amplifier.

CHAPTER 3:

Verification of PPC performances through simulation

3.1 Modelling of the PPC components

In the next subparagraphs, a Simulink model for each of component of the PPC circuit will be presented with a brief description of how it works. In addition to the TVS and the GDT who do not have a dedicated library component also the snubber circuit (which consist of all passive library component) will be presented for completeness. The arc model will be presented as well but it will be used only in the paragraph 3.4, in all the other only the short circuit considered.

3.1.1 TVS modelling

The TVS is a bidirectional Transient Voltage Suppressor diode. This device offers bidirectional port protection by clamping the voltage at a specific value when the input voltage is higher than its rated voltage. Such a device is not present in the Simulink library (specialized power system), so an equivalent circuital model of the device (see figure 27) was designed to achieve a similar behaviour:

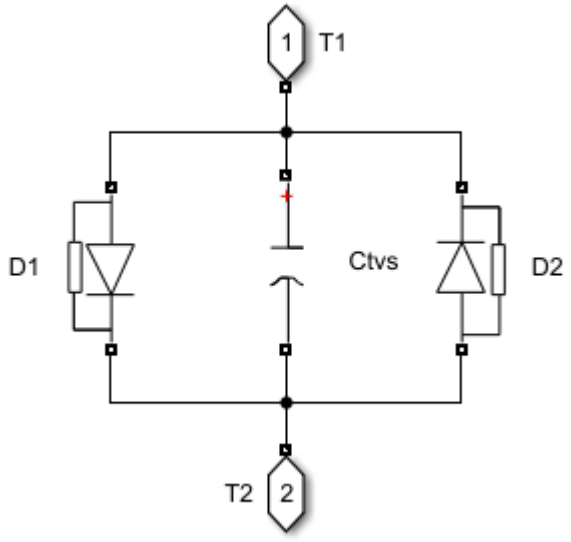

Figure 28 - TVS circuit model

The threshold voltages of each diode (D1, D2) were set to the clamping value of the real device, in this case $V_c = 520V$ (the snubber resistance in parallel with the diodes was not removed, it was set to $1G\Omega$ due to simulation issues; the breakdown voltage of each diode was set to a value larger than V_c).

When the input voltage is higher (lower) than V_c $(-V_c)$ the diode became an ideal voltage generator with a voltage equals to V_c. It was also added a stray capacitance (Ctvs) of 120pF indicated by the datasheet of component available on the market. In the real circuit will be used 2 devices so, in the simulation circuit will be 2 TVS in series as well. The clamping voltage will be at 1,04kV (maximum rating of the amplifier).

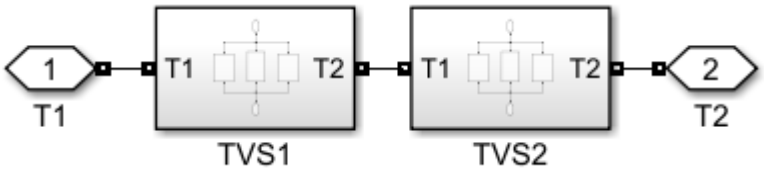

Figure 29 - TVS protection circuit group

3.1.2 GDT modelling

The GDT used in the PPC is not a properly Gas Discharge Tube but is a behavioural compatible bidirectional thyristor; the equivalent Simulink model of the GDT, based on the characteristics reported in the GDT datasheet [8], is schematized in figure 30.

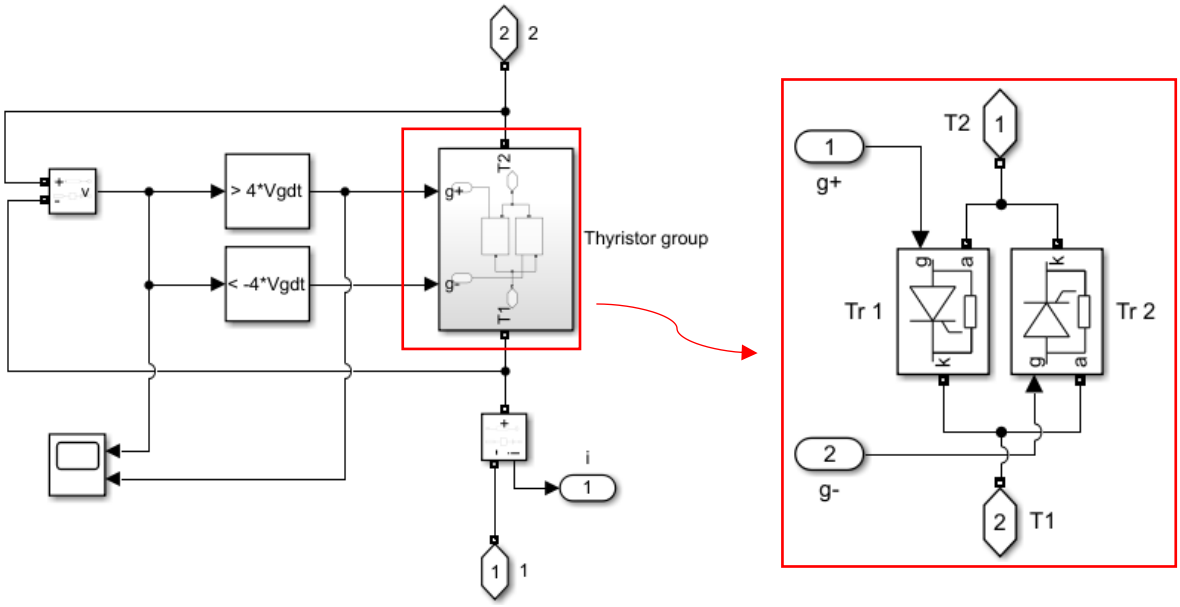

Figure 30 - GDT circuit model and the thyristor group expanded view

In the real circuit 4 GDT series connected are present, so, in the Simulink model, a single element with 4 times the threshold voltage ($250V$) has been used.

A control logic has been implemented: the voltage across the GDT is monitored across port 1-2 (shown in figure 30); as the voltage is higher (lower) than $4 * Vgdt = 4 * 250 = 1000V$ ($-1000V$) one of the two thyristors (Tr1 if the voltage waveform is positive, Tr2 otherwise) will turn on providing a low impedance path (shorting the connection). It will be short circuited until the current i goes down to 0. Then, the thyristor opens until the triggering command is sent to the thyristor gate once again.

The parasitic capacitance of each GDT specified by the datasheet of component available on the market is of $105\ pF$.

For this reason, each of the two thyristors of the equivalent GDT Simulink model has a parasitic capacitance of $105/8\ pF$ specified has a parameter of its block. The total capacitance of the GDT Simulink model is $105/4\ pF$.

3.1.3 Snubber circuit

The snubber circuit consists in the parallel connection of an inductor (L_{VS}) and the series of a capacitor and a resistor (C_{VS} and R_{VS}). The circuital model of the snubber circuit is represented in figure 31.

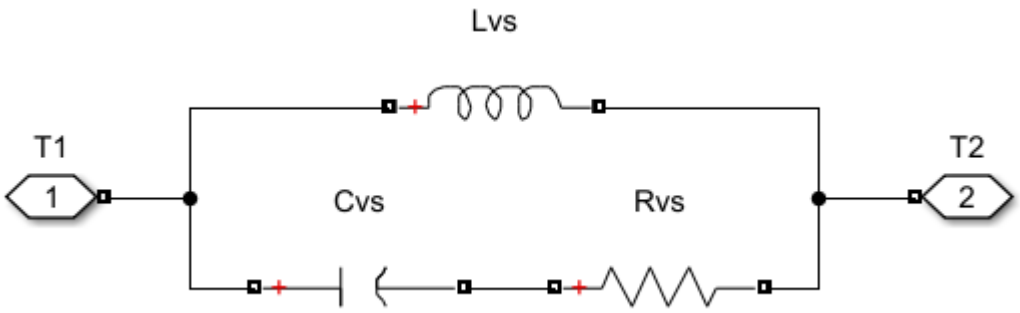

Figure 31 - Snubber circuit model

It works by introducing dynamically Rvs to dissipate the fast current transient into it (Cvs reactance low, Lvs reactance high), while in steady state operation ($1MHz$) the high reactance of Cvs and the low reactance of Lvs create an overall connection of few ohms (6Ω) to not interfere with the normal operation.

The values of the components were tuned iteratively by running several simulations to find the optimum (the first values):

- $Lvs = 1\mu H$ (optimum) $\rightarrow 0{,}95\mu H$ real component value (measured)
- $Cvs = 1nF$ (optimum) $\rightarrow 0{,}94nF$ real component value (measured)
- $Rvs = 100\Omega$ (optimum) $\rightarrow 94\Omega$ real component value (measured)

In the simulations the real value of the components was used beside the optimum to achieve a better representation of the real circuit.

3.2 HVRFTF fault simulations with PPC

In this section, the faults simulations, and results of the HVRFTF circuit with the passive protection circuit (figure 27) are reported. The type of faults considered during simulations are F1 and F2 (described in paragraph *2.3)* with the same voltage and current condition shown in table 3. On the amplifier side, an open-circuit equivalent scheme was used. The relevant waveforms in case of fault conditions F1 and F2, with the PPC, are summarized respectively in figure 32 and figure 33.

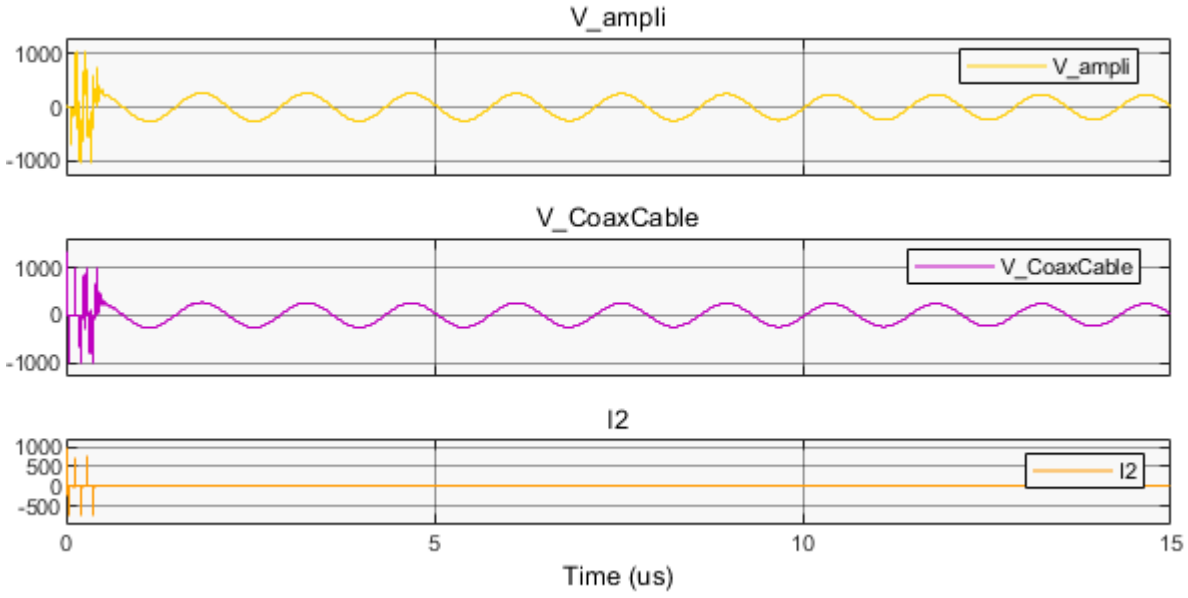

Figure 32 - F1 fault simulation waveform with the PPC

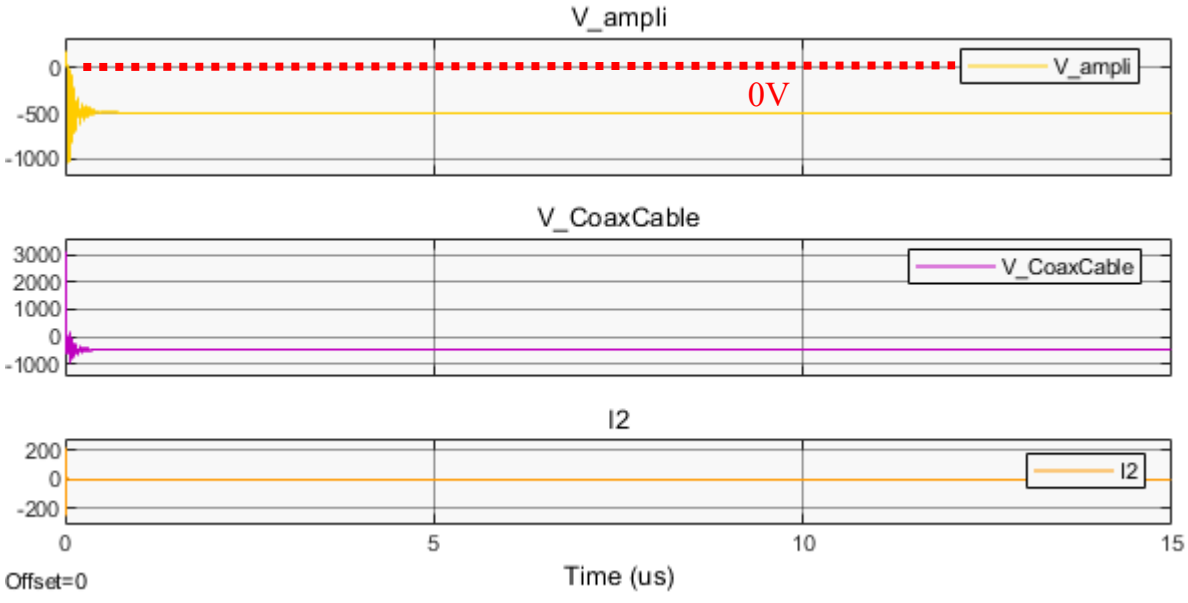

Figure 33 - F2 fault simulation waveform with PPC

Comparing with the waveforms in figure 23-24 the positive effect of the protection is clearly visible.

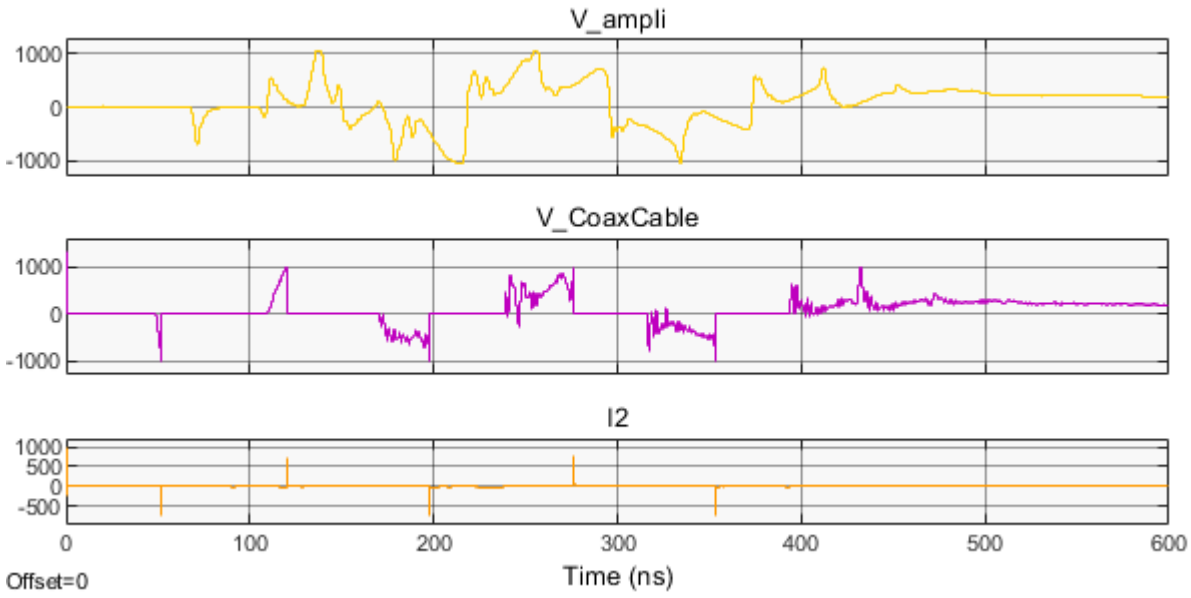

Figure 34 - Zoomed view of the F1 fault waveforms with the PPC

Looking at V_ampli waveform in the F1 fault in figure 32-34 (which correspond to the voltage seen by the TVS), we can see that the TVS intervenes by clamping the voltage at $1040V$. From the $V\_CoaxCable$ we can see the GDT working by shorting the connection (so the voltage goes down to 0) when $1kV$ is reached and opening it when the current flowing through it crosses $0A$. The snubber circuit is able to limit the current $I2$ from $950A$ to few pulses of $760A$ maximum.

For the F2 fault, the effect of the protection circuit is also clearly visible, moreover a voltage offset of $-500V$ (can be seen in figure 33) is present due to the left charge of Cs after the intervention of the PPC components. After the intervention of the GDT and TVS an almost open circuit (very high resistance) is present, so the capacitor holds its remaining charge.

Cs needs to be discharged before any type of interaction with the circuit.

3.3 PPC influence in the steady state operation

For the impedance matching, in the steady state operation, the GDT and TVS do not intervene, so the circuit only see the stray capacitance of each component. The effects of the stray capacitances an the snubber circuit on the reflection coefficient are shown in figure 35-36:

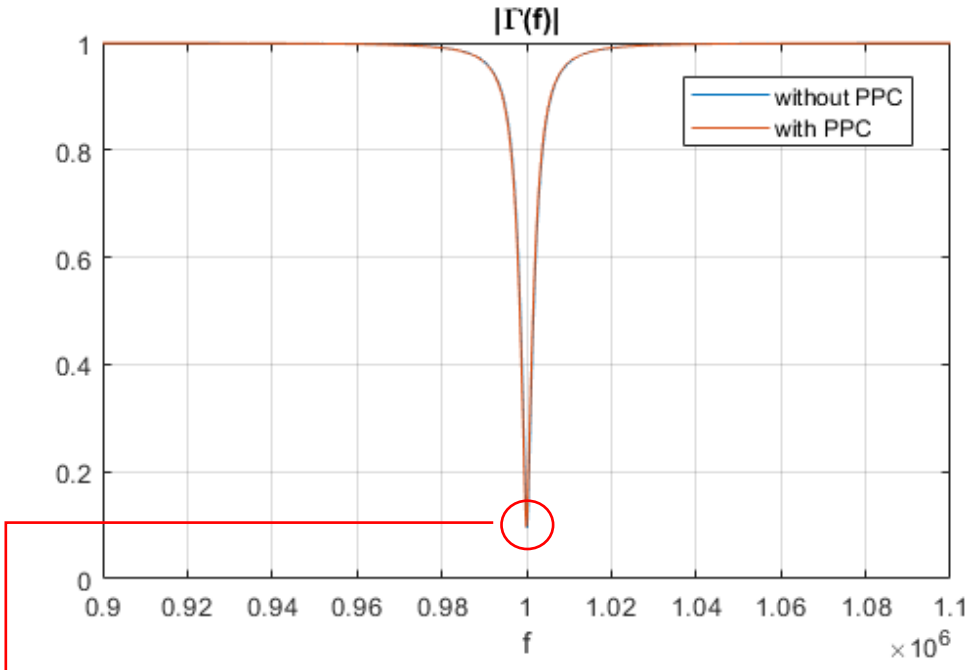

Figure 35 - Modulo of the reflection coefficient with PPC (orange) and without (blue)

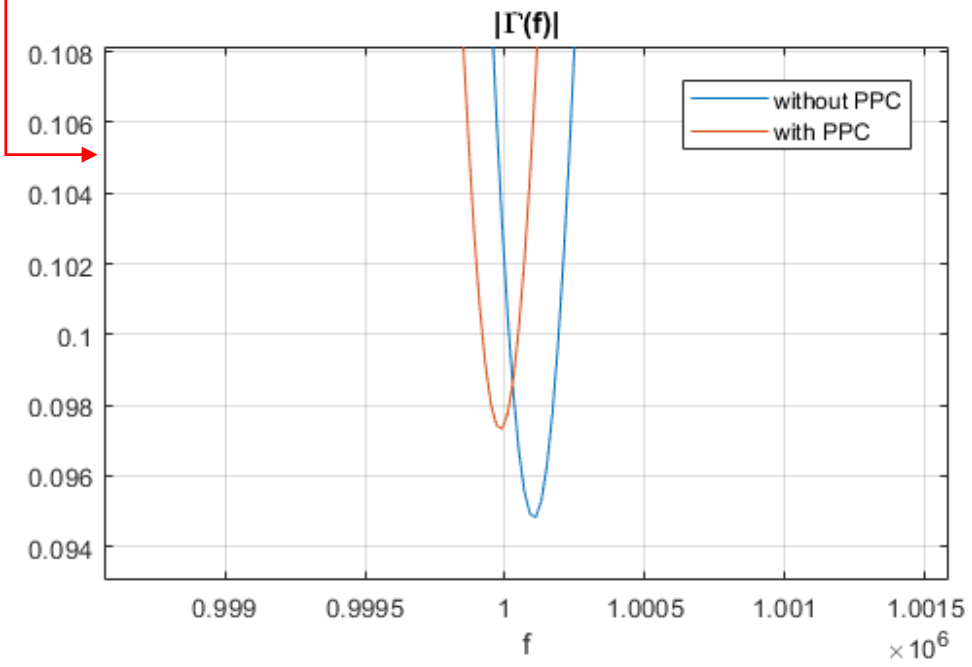

Figure 36 - Zoomed version of the figure 35

Other effects of the snubber circuit consist in a small voltage drop across it (blue waveform in figure 37), which can be seen in the following waveform:

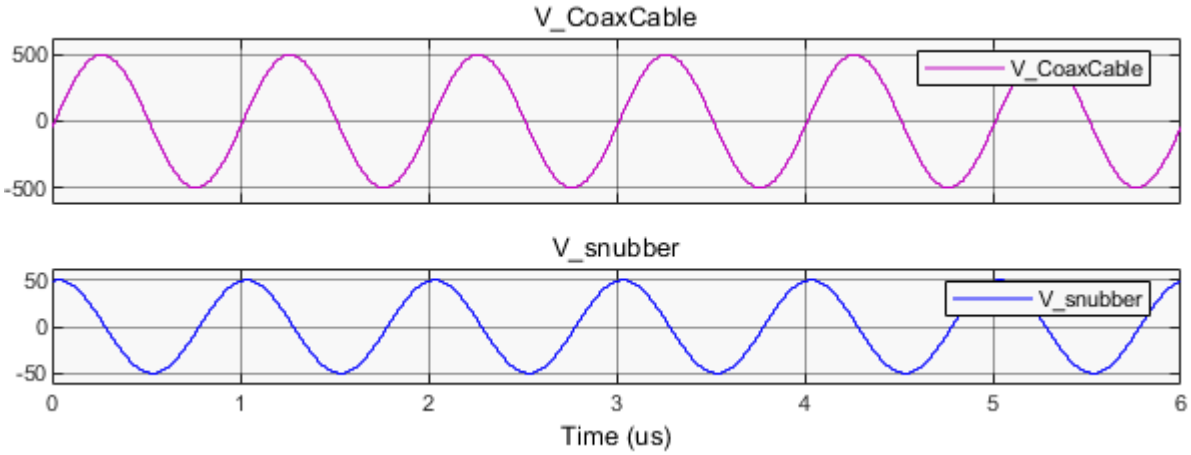

Figure 37 - Snubber voltage drop in the steady-state operation

In steady state operation, with nominal RF power, the power dissipated by the resistor Rvs is equal to $3.5W$.

3.4 Effects of stray parameters on PPC performances

For getting closer to the real circuit response, stray components are included in the RF circuit model at specific points. Considering the layout in HVRFTF and the connection of the PPC parts to the RF circuit, stray connection inductances are added in series with all the parts of the protection circuit to emulate the behaviour of a cable connection, see figure 38.

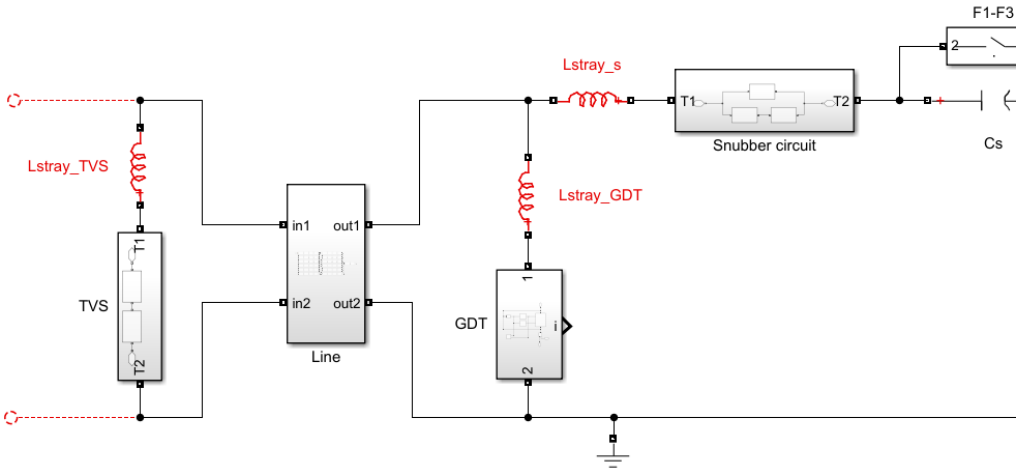

Figure 38 - HVRFTF circuit with the stray inductance wiring

The same simulations as before were done but *only the F1 fault waveforms will be shown* since the F2 voltage and current peak are less relevant than the ones of F1.

Given the difficulty of measuring the value of parasitic inductance relative to the wiring, it was decided to evaluate the effect of parasitic inductance on the waveforms of interest by considering three different inductance values:

- $1nH$
- $10nH$
- $100nH$

The first and the last are representative of so-called "short" and "long" wiring, while $10nH$ may be representative of an intermediate value.

The following fault simulations waveform are respectively done with 1nH (figure 37), 10nH (figure 38) and 100nH (figure 39) (with the short circuit):

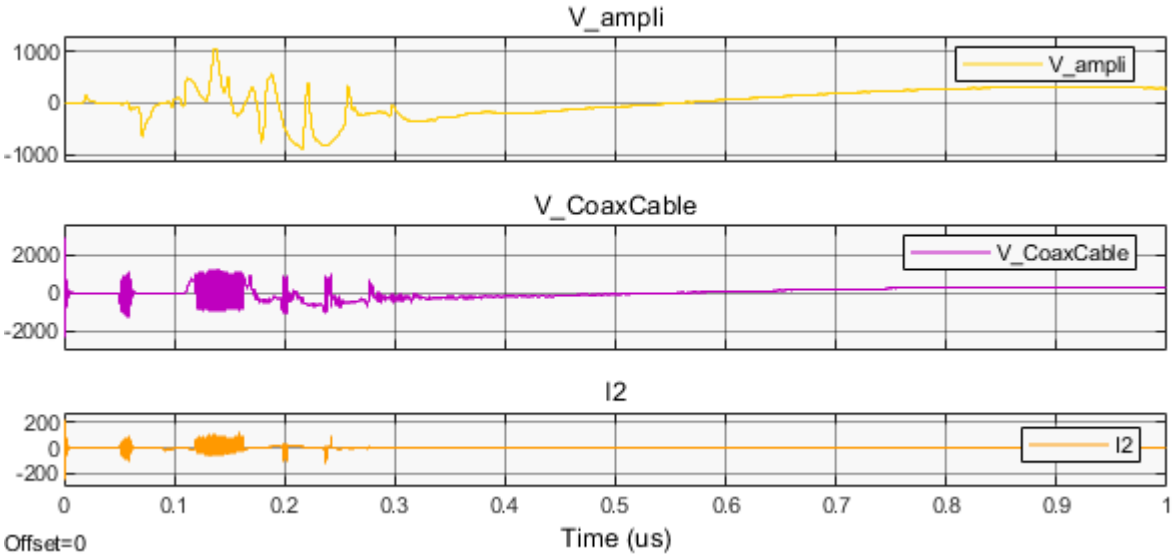

Figure 39 - F1 fault waveforms with a stray inductance value of 1nH

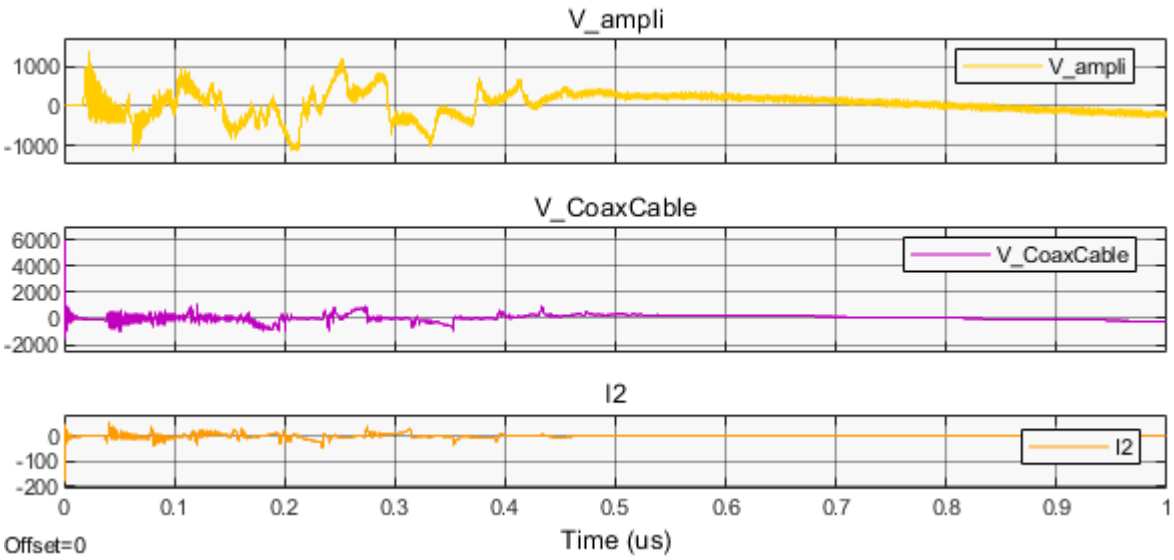

Figure 40 - F1 fault waveforms with stray inductance value of 10nH

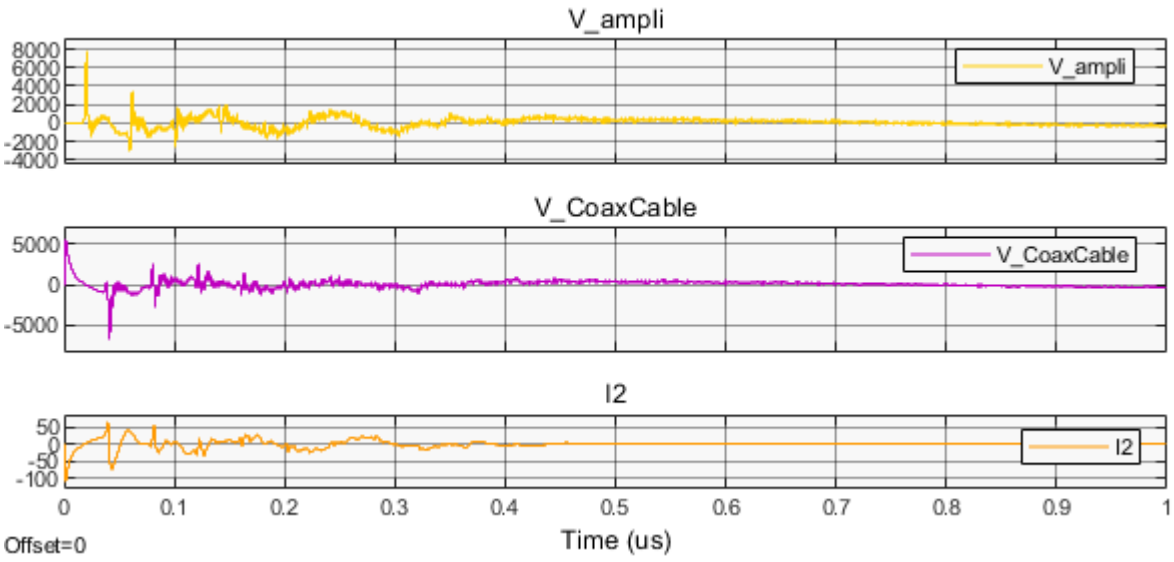

Figure 41 - F1 fault waveforms with stray inductance value of 100nH

As we can see with 1 and $10nH$ the overall voltage (V_ampli) is limited and the overshoot is acceptable with respect to the limits specified in table 5, but with $100nH$ the effect of the stray inductances of the connections produce voltage transients at the output of the amplifier up to $8kV$, despite the intervention of the TVS.

The series inductance plays a decisive role regarding the protection of the amplifier, so *it is mandatory check the connections and estimating its inductance (if it's possible) before proceeding with the real test.*

CHAPTER 4:

Thermal analysis of the GDT and TVS

4.1 GDT and TVS thermal losses

In this section, a brief study to evaluate the power dissipation in the TVS and in the GDT during their intervention is provided. It is important to evaluate if the power dissipated during each commutation of the components can lead to a gradient of temperature high enough to cause a component failure due to overheating. Due to the lack of data from the datasheet of the components, some problems during the analytics calculus were encountered and a possible solution will be provided in the next paragraphs.

4.1.1 Issues

To evaluate the dissipated power in the TVS and in the GDT some preliminary analytics calculus was tempted but due to missing data from the relative datasheet, assumptions needed to be done on their thermal capacity C_{GDT}, C_{TVS}, the junction to free air thermal resistance $R_{\Theta \mathrm{JA}}$ and their on-resistance R_{ON}. The idea was to set up a model in MATLAB Simulink, *with the estimated data*, that would allow us to obtain the temperature trend over time and the instantaneous power managed by the component, so as to rapidly evaluate if the component should be able to withstand the thermal stresses.

4.1.2 Thermal analysis

In this section, the design of the developed thermal model is provided; also, a brief description of the layout and the operation of the circuit will be done.

The thermal model, whose scheme is represented in figure 42, was built on the GDT parameters because more data were available from the datasheet, therefore fewer assumption were needed.

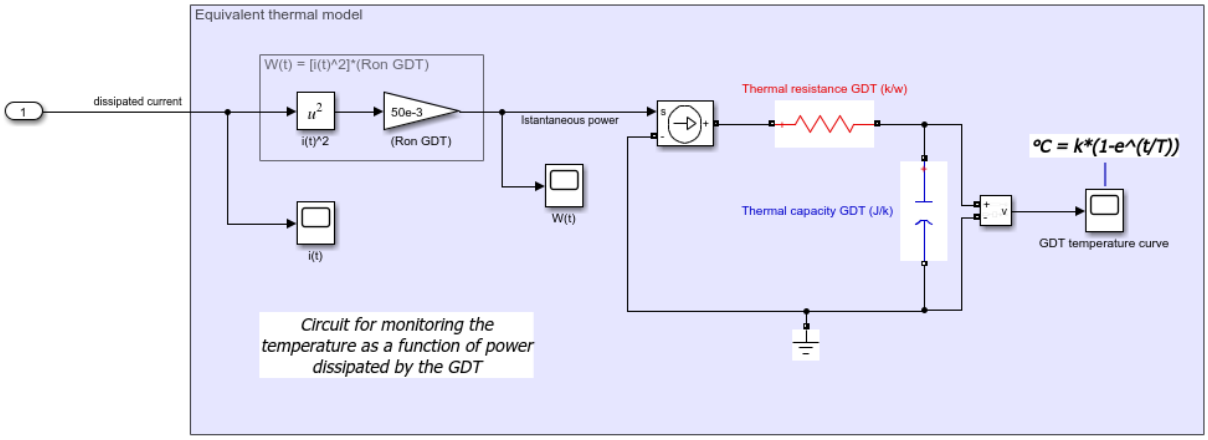

Figure 42 - Thermal model circuit layout

The thermal resistance and the R_{ON} are the parameters included in the GDT datasheet ($R_{\Theta JA} = 90\,{}^{k}/_{W}$, $R_{ONGDT} = 50\ m\Omega$), while in the TVS one, none of these was available. Otherwise, the thermal capacity (blue) was not present nor in the GDT datasheet nor in the TVS one. For this reason, a value of $6.5\frac{mJ}{k}$ was estimated for the GDT. The estimation of the thermal capacity was done by roughly calculating the volume of the component using the datasheet dimension: $V_{GDT} = 2mm * 2mm * 1mm = 4 * 10^{-9} m^3$. Knowing the density of the silicon ($\rho_{Si} = 2330\,{}^{kg}/_{m^3}$) and its specific heat capacity ($c_{Si} = 700\,{}^{J}/_{kg * K}$), its thermal capacity (C_{GDT}) can be estimated as: $C_{GDT} \cong c_{Si} * V_{GDT} * \rho_{Si} \cong 6.5\frac{mJ}{k}$.

Considering the worst-case fault F1 with the worst type of connection (stray inductance of 100nH), figure 43 shows the dissipated current waveform of the GDT.

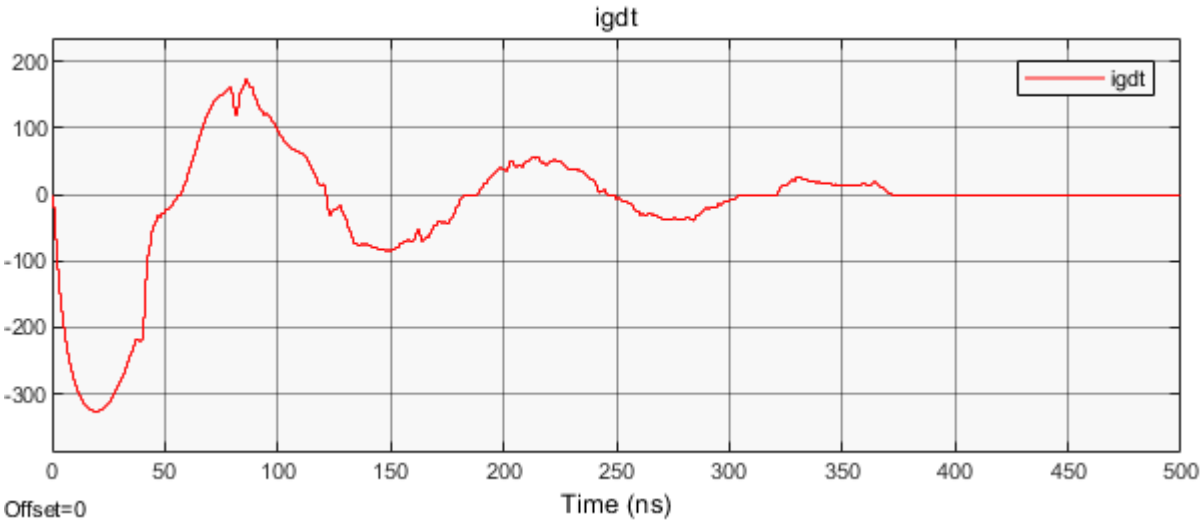

Figure 43 - GDT dissipated current waveform during the F1 fault

The instantaneous power is calculated using the formula: $W(t) = R_{onGDT} * [i(t)\text{^}2]$.

$W(t)$ is placed as the input signal of a controlled current source which impose the current in a RC thermal equivalent circuit of the GDT. The voltage drops on the thermal capacitance correspond to the temperature trend of the component. The results obtained with the thermal model are provided in the next paragraph.

4.1.3 Results

The temperature and the instantaneous power waveform are shown in figure 44.

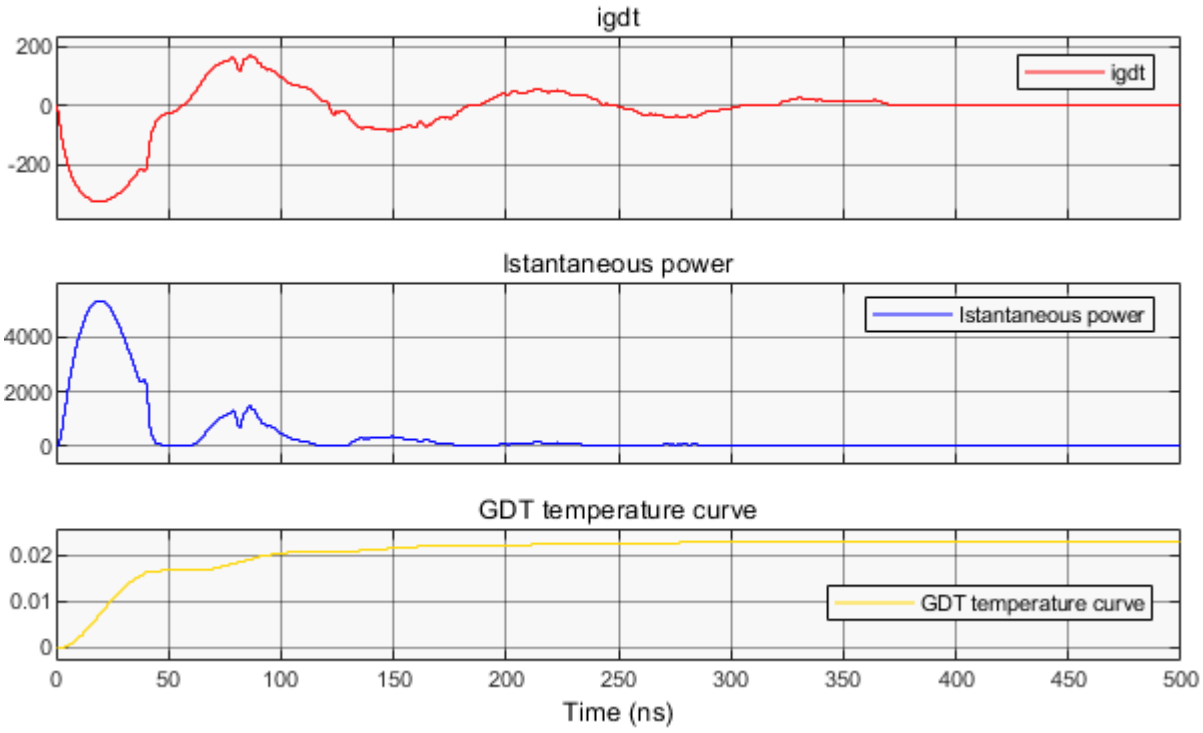

Figure 44 - Current, Instantaneous power and temperature trend over time of the GDT

Assuming the estimated parameters as inputs for the model and the GDT as an adiabatic system, the instantaneous power of the GDT reaches a peak of $5{,}3kW$, and the temperature, due to its thermal capacity, grows of 0,03 degree. The GDT specified maximum junction temperature is of $150°C$ (datasheet parameter) and in the hypothesis of starting with a worst-case ambient temperature of $40°C$, the maximum ΔT is equal to $110°C$. The heating of the component in a fault intervention seems to be limited.

CHAPTER 5:

Test procedures

5.1 Test setup and description

Figure 45 shows the complete test setup, and it will be used as reference image and better explained in the next paragraphs.

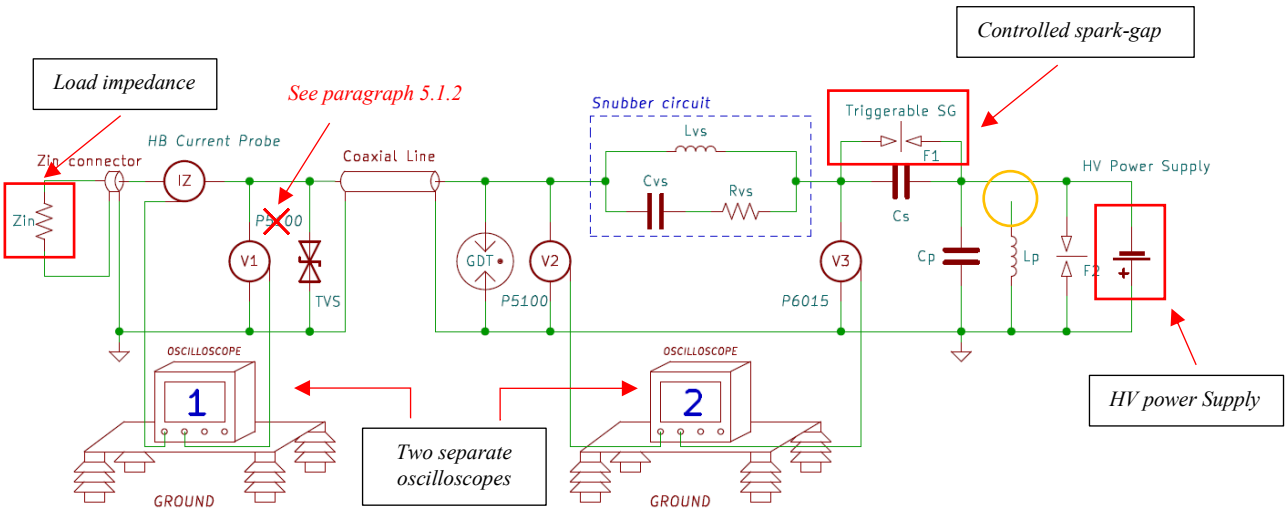

Figure 45 - Complete test circuit setup

As can be seen in figure 45, since the RF amplifier cannot be used to power the components, the fault voltage of the capacitors (Cs and Cp) will be set using a high voltage power supply. The triggerable spark gap is used to recreate the fault in one of those capacitors. The different probes are used to record all the relevant waveforms for a simulation's comparison. The type and their requirements will be covered in the next paragraph.

To perform the static test on the circuit some equipment is needed:

- High voltage power supply (up to $24kV$)
- Pressure-controlled spark gaps
- Two or more *battery powered* Oscilloscopes
- Voltage and Current probes (covered in paragraph 5.2.2)

Also, in the figure 45, can be seen that two separate battery powered oscilloscopes are used and placed on an insulation plane, this is to avoid ground loop and damage to the instruments due to the line that, during the fast transient, can create potential differences between the two ground references.

5.2 Design of the test procedures

This paragraph describes the design of the test procedures for the qualification of the PPC.

The faults will be done with four different voltage level:

- $10kV$
- $15kV$
- $20kV$
- $24kV$

As shown in figure 45, the capacitors will be charged by connecting the HV power supply in parallel with Cp, so Cp will be charged directly and Cs will be charged through the snubber circuit and through the parasitic resistance of the GDT. This is the key of the circuit setup since it requires the GDT and the snubber always connected in all the three different circuit configurations.

Following this charging method, the parallel inductor Lp shall be removed from the circuit. In fact, Lp will prevent the charge of Cp, by acting as a short circuit in parallel to it.

The following simulations were performed to verify if the removal of the inductor leads to significant changes in voltage and current fault waveforms (simulated with F1 fault).

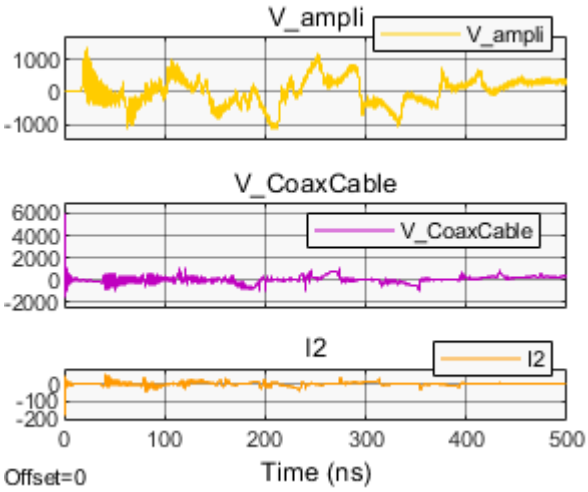

Figure 46 - F1 fault waveform with Lp

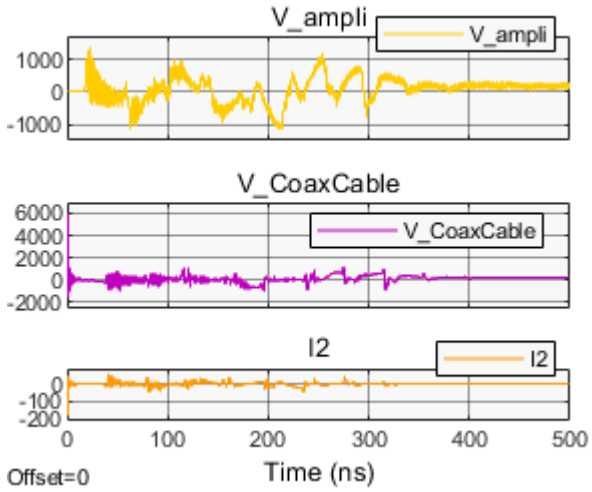

Figure 47 - F1 fault waveform without Lp

As we can see, the changes are negligible since the inductor impedance, at the transient frequency, is order of magnitude above the impedance of the capacitor Cp (kohm to ohm) letting the most severe current stresses to circulate through the Cp branch. This can be seen in figure uuuuu comparing the Lp waveform ranges (iLp) with the Cp waveform ranges (iCp).

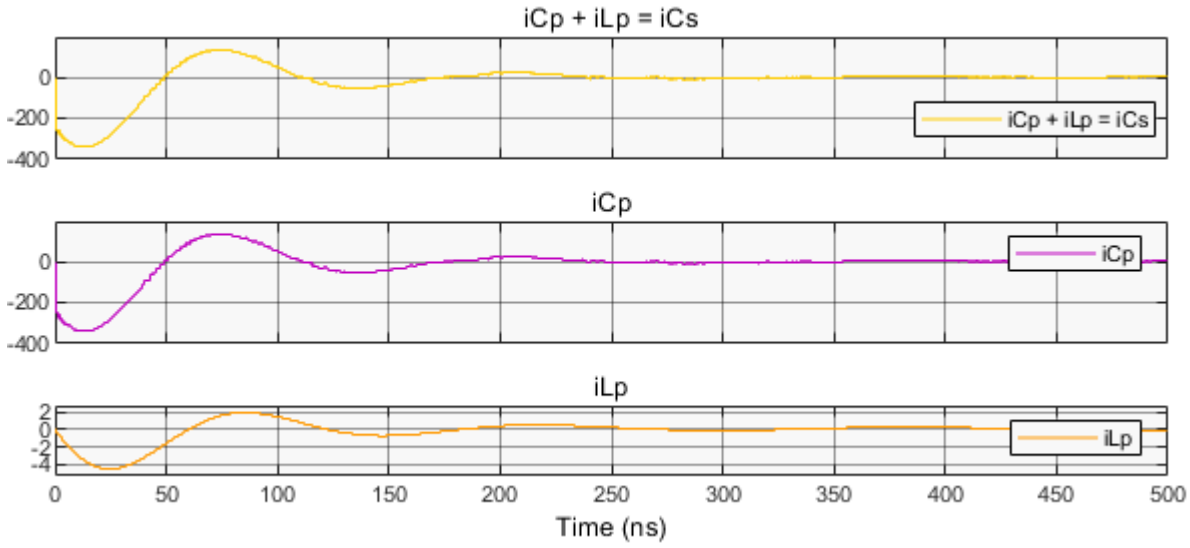

Figure 48 - Current waveforms of Cs (iCs), Cp (iCp) and Lp (iLp)

As a result, the capacitors charging method can adopted since the removal of the inductor will not affect transients during fault tests.

With the assumption of that the output impedance of the RF power amplifier is real, the tests will be performed by substituting the output stage of the amplifier with the impedance Zin which will be set to three different values:

- Short circuit
- 50Ω
- Open circuit

The short circuit is used to qualify the circuit in case of maximum current stresses while the open circuit in case of maximum voltage stresses. The 50Ω pure resistive impedance will allow testing the circuit in matching condition.

The circuit also will be tested in *three different configurations*:

1. Without the TVS and the line:

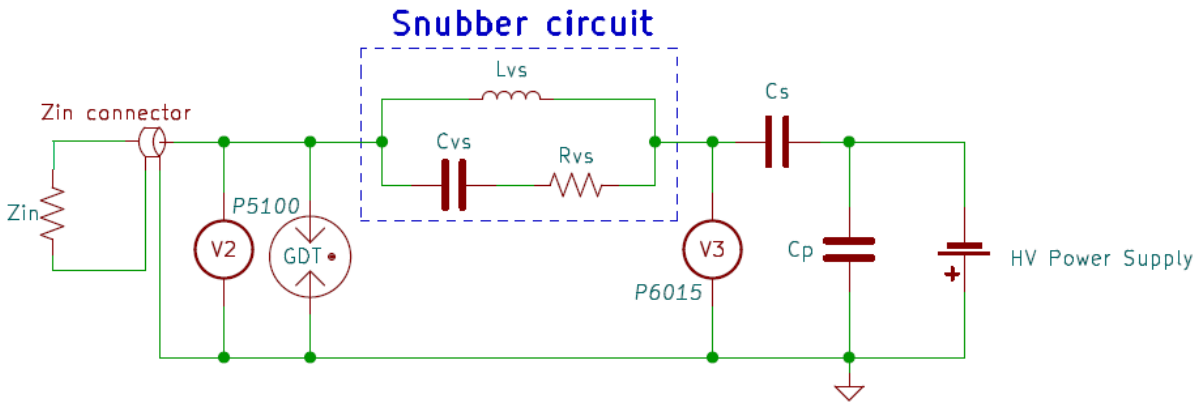

Figure 49 - Test circuit in the first configuration

2. Without only the TVS (connecting the line):

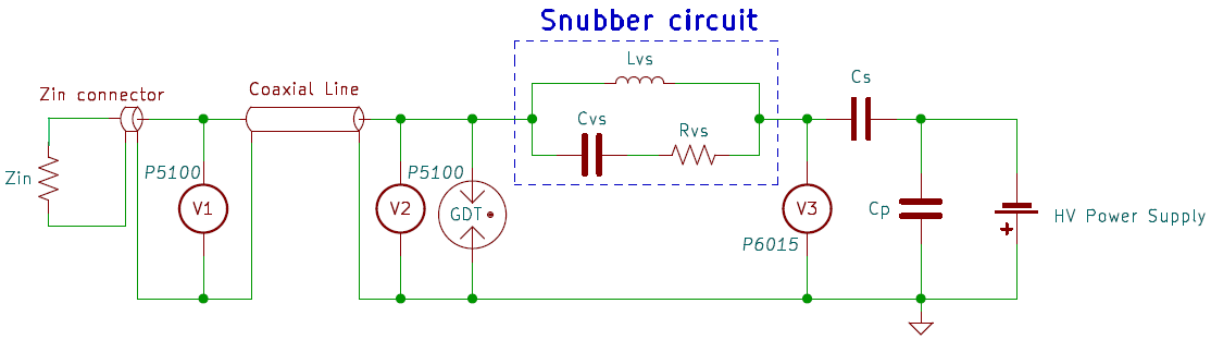

Figure 50 - Test circuit in the second configuration

3. Complete circuit:

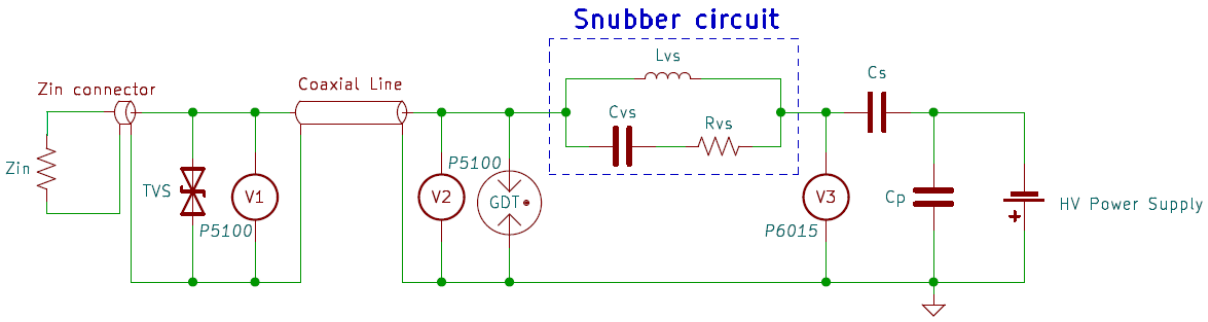

Figure 51 - Test circuit in the third configuration

The goal is to test the performances of the individual PPC components to verify their behaviour during fault transient. For each layout the voltage of the HV power supply and the value of the impedance Zin will be varied in the previously specified ranges.

5.2.2 Expected waveforms

In this paragraph the main waveforms from the simulation of the tests are shown also the definition and appropriateness of measuring probe will be done.

The following image are taken in specific condition (presented in the following) that leads to the maximum peak values. All the other combination brings to less severe cases which are not shown. The waveforms are taken in the three configurations (figure 49, 50, 51) with $24kV$ of fault voltage. A lower voltage implies lower overall values. The impedance values of Zin used are the short circuit and the open circuit to see the maximum stress of current and voltage on the base of the assumption made on the amplifier output stage.

The capacitors voltage was set to positive $24kV$ for Cp and Cs which is the same thing that will happen in the way we will charge them.

The fault considered was the most severe one, F1. Also, $10nH$ of stray wiring inductance, considered the most reliable (in the hypothesis of a short and cured connection), was used.

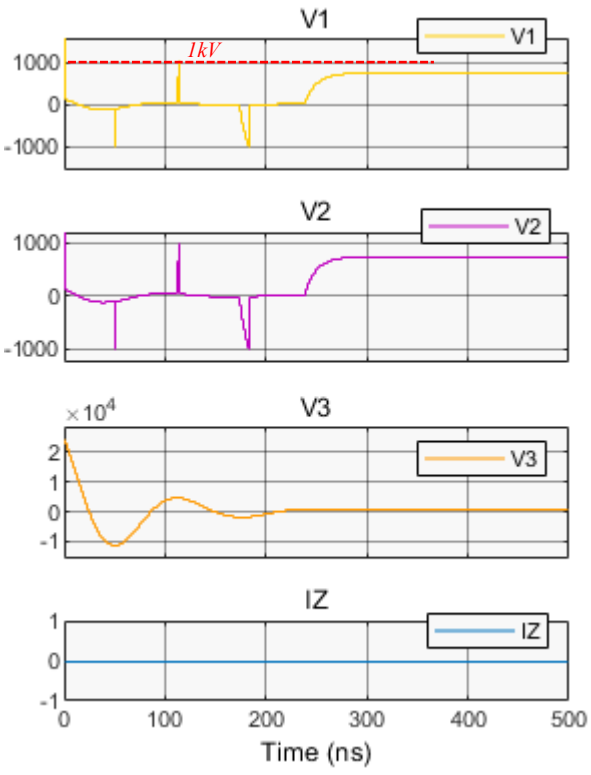

Figure 52 - First configuration with Zin = open circuit

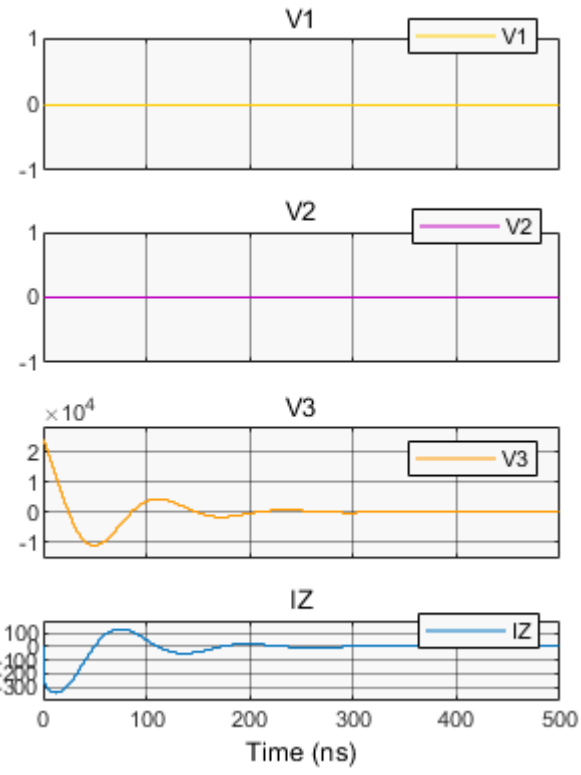

Figure 53 - First configuration with Zin = short circuit

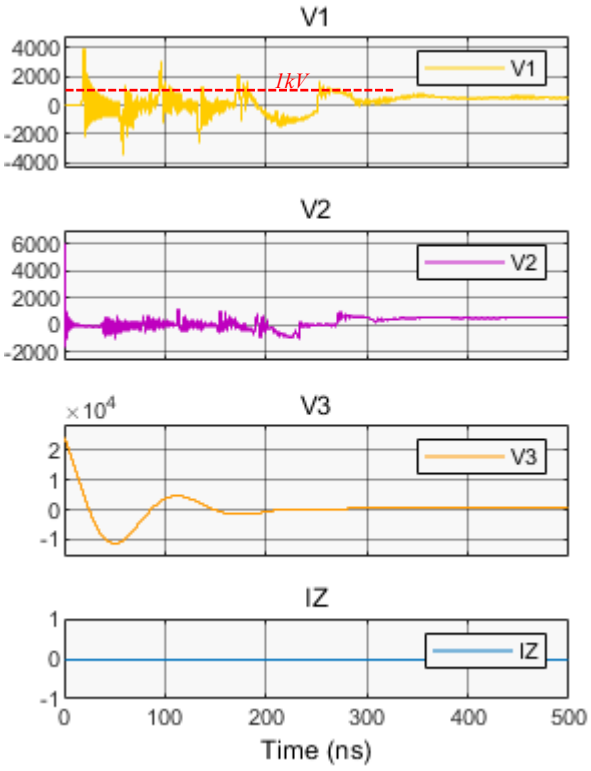

Figure 54 - Second configuration with Zin = open circuit

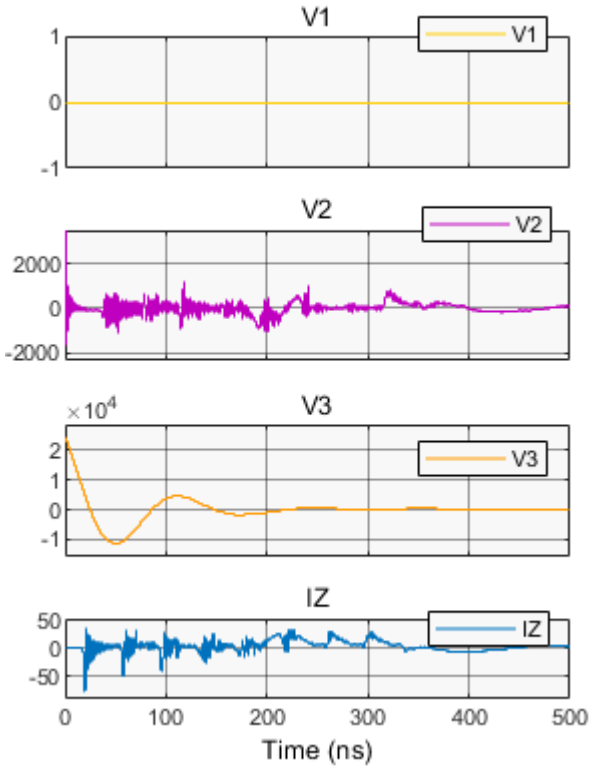

Figure 55 - Second configuration with Zin = short circuit

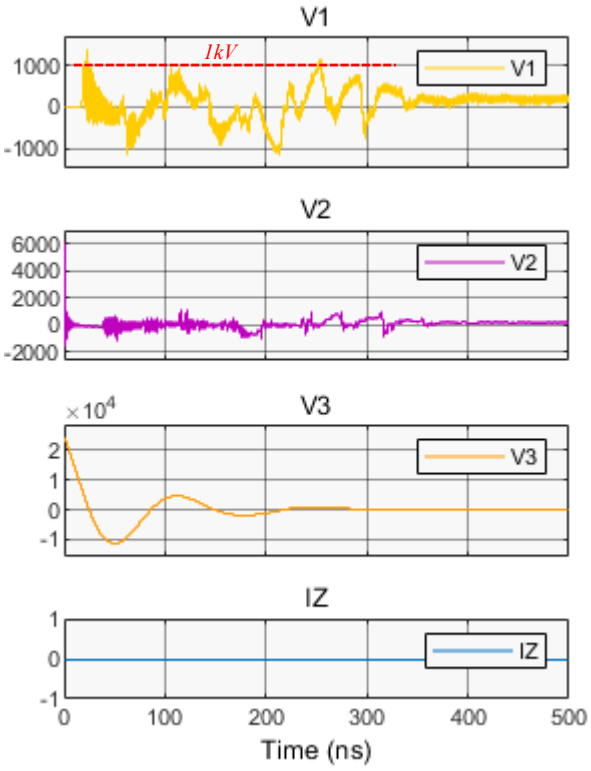

Figure 56 - Third configuration with Zin = open circuit

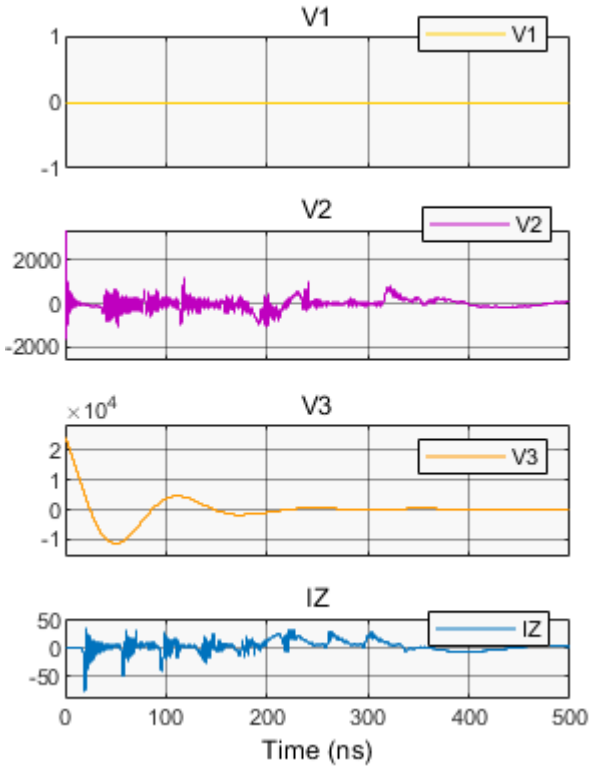

Figure 57 - Third configuration with Zin = short circuit

Comparing the figure 52 (without the line) and 54 (with the line) we can see the negative effect of the coaxial line in terms of over voltages on V1; contrarily comparing the figure 54 with 56 (with the line and TVS) we can see how the TVS intervene by clamping the voltage a little over 1kV. In figure 53 we can see that the first configuration with the short circuit create the maximum current stress. Table 6 summarises the peak values of the simulated waveforms.

Table 6 - Peak values reached with PPC for each circuit configuration

	F1 Fault with 24kV							
	Zin = open circuit				*Zin = short circuit*			
	V1	*V2*	*V3*	*IZ*	*V1*	*V2*	*V3*	*IZ*
1°	1kV	1kV	24kV	0	0	0	24kV	-344A
2°	4kV	1,5kV	24kV	0	0	1,7kV	24kV	-80A
3°	1,3kV	1,5kV	24kV	0	0	1,7kV	24kV	-80A

By reducing the stray inductance values, smaller peak values are obtained.

Regarding the probes, with reference to the figure 45, the voltage probe V3 monitors the voltage waveform due to Cp and Cs faults, for this reason, the probe needs to withstand high voltages up to maximum capacitors charging voltage for the tests ($24kV$) so a HV P6015 probe could be suitable (V3 transient do not exceed $15MHz$).

V1 and V2 probes are used to monitors respectively the TVS\Zin voltage waveform and the GDT voltage waveform. Assuming a correct operation of the components and good connection (small inductance less than $10nH$) the voltage peak on V2 should stay below $1.7kV$. The P5100 can measure voltages up to $2.5kV$ with a bandwidth of $250MHz$ which is suitable for the expected V2 transients. *After recent simulations it has emerged that, for V1, the voltage can reach values of* $4kV$ *which means that the P5100 can't be used, and other probes needs to be taken into considerations.*

For the probe IZ the current transient has a rising time around 1.5ns and in some cases the peak values can reach up to 344A. For these reasons the current probe has not yet chosen. The following table summarises the needed requirement for each point of voltage and current pickup and possibly a suitable probe for each one.

Table 7 - Voltage and current probes minimum requirements

	Minimum requirements of the Probe		
V-I meters	*Max Vpeak*	*Rising time (10%-90%)*	*Choosen probe*
V1	4 kV	< 2 ns	Tektronics P5100 can't be used
V2	1.7 kV	< 2 ns	Tektronics P5100
V3	24 kV	< 20 ns	Tektronics P6015A
IZ	340A	< 1.5 ns	*Not choosen yet*

CHAPTER 6:

Conclusions

This thesis is focused on the study and understanding of HVRFTF RF circuit behaviour in case of faults on its main components and on the effectiveness of the proposed protection circuit. Furthermore, the design of the procedures to test the protection circuit is discussed.

The summarised results are:

- Concerning the type of faults, only F1 and F2 will be considered whereas F3 and F4, being much less burdensome, will not be treated or reproduced in the test.
- The protection circuit is able to limit the voltage and current stresses under the required values unless the stray inductance of the connection is less than $10nH$. So, the connection needs to be taken care of to reduce at minimum its inductance value. The PPC influence in the steady state operation is negligible.
- Due to the behaviour of the main protection components of the protection (GDT and TVS) after the faults the capacitors can remains charged so it is mandatory to discharge every capacitor before interacting with the circuit.
- Regarding the thermal stresses of the PPC components, a brief study on the power dissipated by the GDT was performed. Due to the missing data of the components, some parameters have been estimated. The simulations shows that the temperature variations of the component are below hundreds of °C, so the overall heating should be limited.
- The protection circuit will be tested in three different configurations. For each configuration several subtests will be carried out by mimicking matched, open and short circuit conditions for capacitors charge voltage from 10 to 24 kV. The waveforms collected from different current and voltage probes are compared to the ones obtained through simulations.

REFERENCES

[1] https://www.iter.org/news/galleries

[2] Serianni, G., et al. "First operation in SPIDER and the path to complete MITICA." Review of Scientific Instruments 91.2 (2020): 023510
Toigo, V., et al. "The PRIMA Test Facility: SPIDER and MITICA test-beds for ITER neutral beam injectors." New Journal of Physics 19.8 (2017): 085004

[3] Maistrello, A., et al. "Studies on the requirements and design of the High Voltage Radio Frequency Test Facility." Fusion Engineering and Design 131 (2018): 96-104

[4] Spinner Flex LF7/8"-50-PE BN A73089

[5] F. Ulaby e U. Ravaioli, «Fondamenti di campi elettromagnetici», VIII Edizione, Pearson, 2021

[6] Cui, Wei, et al. "Lumped-element sections for modeling coupling between high-speed digital and I/O lines." IEEE 1997, EMC, Austin Style. IEEE 1997 International Symposium on Electromagnetic Compatibility. Symposium Record (Cat. No. 97CH36113). IEEE, 1997

[7] PTVS1-380C-TH high voltage, high current TVS diode

[8] ACTP250J1BJ AC Transient voltage protector