UNIVERSITÀ DI PADOVA **FACOLTÀ DI INGEGNERIA**

TESI DI LAUREA

Design of a Phase Locked Loop for a Low Power Transceiver

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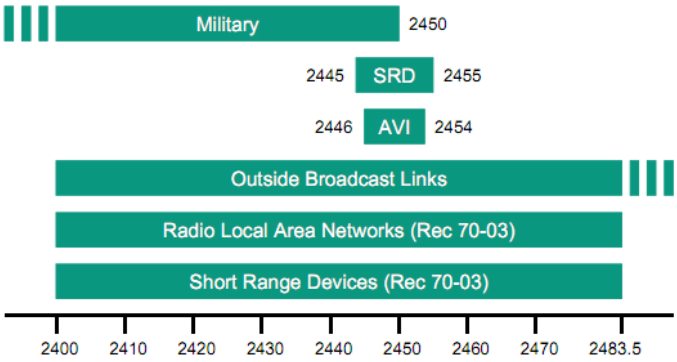
Abstract

ISM band (Industrial Scientific and Medical) is the name assigned by the International Telecommunications Union to a set of portions of the electromagnetic spectrum reserved for non commercial radio applications for industrial, scientific and medical fields. The international ISM bands are :

- 900 MHz band (902-928 MHz)
- 2.4 GHz band (2.400-2.4835 GHz)
- 5.8 GHz band (5725-5850 GHz)

The current use of the 2.4GHz ISM band is illustrated in the following figure.



: AVI - Automatic Vehicle Identification for railways. 500mW in 2446 - 2454 MHz.
Radio Local Area Networks - also used for Radio Fixed Access and planned to be used by Bluetooth.
SRDs - Short Range Devices. 10mW in 2400 - 2483.5 MHz; 500 mW in 2445 - 2455 MHz for movement detection
2445 - 2455 MHz also used for short range indoor data links (no analogue speech).

A phase locked loop (PLL) is one of the critical devices in a low power ISM band transceiver. It is used to generate stable output high frequency signals (in the 2.4GHz ISM band) from a fixed low frequency signal (the reference signal).
In this work different components of a PLL are analyzed and designed with particular regards to Phase Frequency Detector, Charge Pump and Loop Filter.

Contents

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Chapter 1

Introduction to PLL

PLL(Phase Locked Loop) is a feedback system which uses phase, or rather excess phase, to "lock" the frequency of its output with that of an input reference.

1.1 Basic PLL

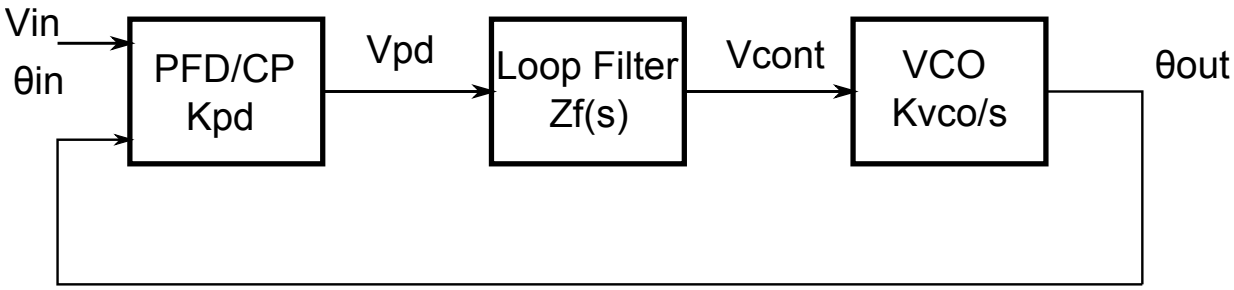

Figure 1.1: *Basic PLL Schematic*

The basic PLL consists of a phase detector (PD), a low pass filter (LPF) and a voltage controlled oscillator (VCO).
Ideally the phase detector produces an output voltage whose DC value is proportional to the difference between the phases of its two inputs $\Delta\varphi$ that is

$$V_{PD} = K_{PD}(\varphi_{IN} - \varphi_{OUT}) \tag{1.1}$$

where K_{PD} is the gain of the phase detector in units of V/rad. The low pass filter suppresses high frequency components in the PD output allowing the DC voltage value V_{CONT} to control the VCO frequency. The output of a ideal VCO oscillates at a frequency dependent on the input

voltage:

$$\omega_{VCO} = \omega_{fr} + K_{VCO}V_{IN} \tag{1.2}$$

where ω_{fr} is the free running frequency i.e. the output frequency when the control voltage is zero and K_{VCO} is the gain of the VCO in units of $rad/s/V$. So in this basic PLL the VCO will oscillate at a frequency equal to the input frequency and with a phase difference equal to $\Delta\varphi$.
To a better understanding about PLL working the initial conditions $\omega_{IN} = \omega_{fr}$ and $\Delta\varphi = \varphi_{IN} - \varphi_{OUT} = 0$ are supposed, so $V_{CONT} = 0V$. If unexpectedly the input frequency decreases initially $\Delta\varphi < 0$, being V_{CONT} directly proportional to $\Delta\varphi$ it becomes negative and since VCO output frequency is proportional to the control voltage, its frequency starts decreasing until it is the same as that of the input signal, keeping in this way the synchronism between input and output frequency. This condition is the locked state. Clearly the opposite occurs if the input signal frequency increases.
Hence the phase locked loop stays in lock because of the negative feedback of the loop in which the phase of the oscillator output is subtracted from the phase of the input signal.

1.1.1 Loop dynamics in locked state

If the input has a constant frequency ω_{IN} and a constant excess phase φ_1 the loop will reach a steady state condition where the output has a constant: frequency ω_{OUT}, excess phase φ_2, V_{PD} and V_{CONT}. In this case $\varphi_{IN} = \omega_{IN}t + \varphi_1$ and $\varphi_{OUT} = \omega_{OUT}t + \varphi_2$. So :

$$V_{PD} = K_{PD}(\varphi_{IN} - \varphi_{OUT}) = K_{PD} = ((\omega_{IN} - \omega_{OUT})t + \varphi_1 - \varphi_2) \tag{1.3}$$

In steady state

$$V_{CONT} = V_{PD} = K_{PD}((\omega_{IN} - \omega_{OUT})t + \Delta\varphi) \tag{1.4}$$

Being constant

$$\frac{\partial V_{CONT}}{\partial t} = 0 = K_{PD}(\omega_{IN} - \omega_{OUT}) \Longrightarrow \omega_{OUT} = \omega_{IN} \tag{1.5}$$

Hence $V_{CONT} = V_{PD} = K_{PD}\Delta\varphi$, and knowing that $\omega_{OUT} = \omega_{fr} + K_{VCO}V_{CONT}$

$$\Delta\varphi = \frac{\omega_{OUT} - \omega_{fr}}{K_{VCO}K_{PD}} \tag{1.6}$$

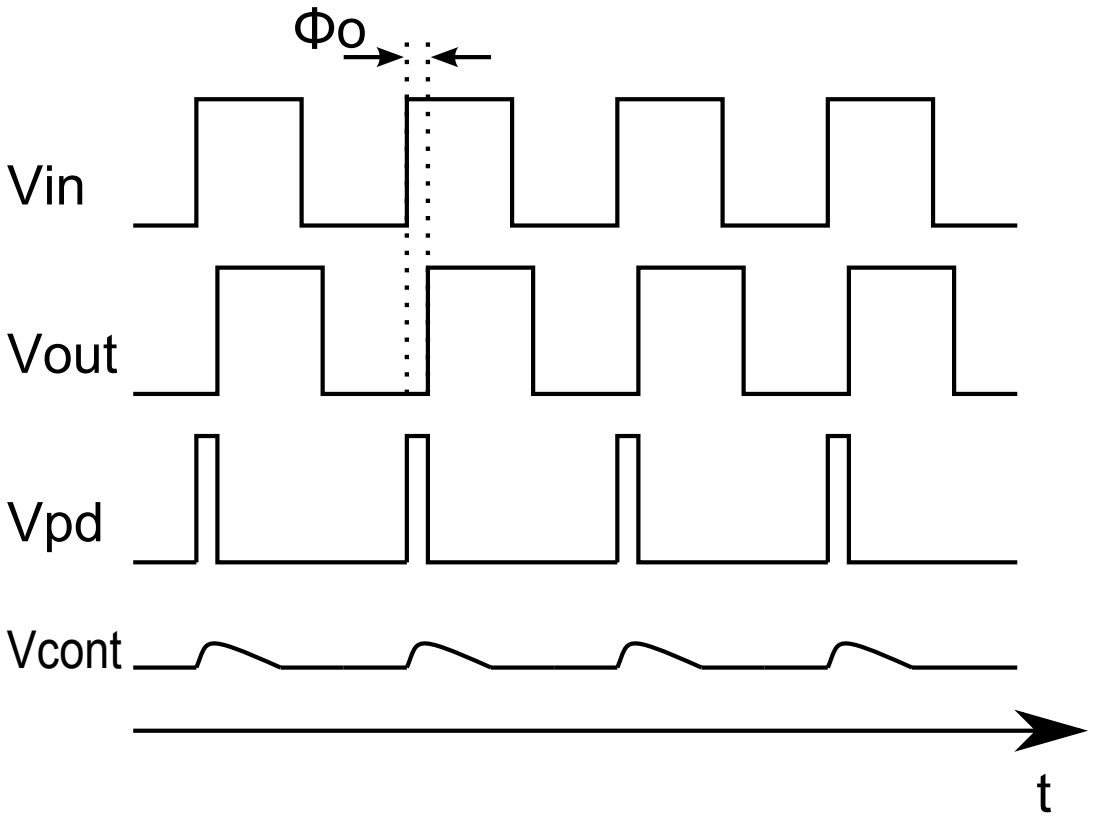

Figure 1.2: *Wafeforms in a PLL in locked condition*

In spite of $\omega_{IN} = \omega_{OUT}$ there is a difference between the input and output phase, this phase difference is sometimes referred to as sustaining the output frequency. This is the particular nature of the PLL system: it uses phase as the feedback quantity but it is frequency which is being matched exactly.

1.1.2 Transfer function

The simplest low pass filter has the transfer function $H_{LPF}(s) = \frac{1}{1+\frac{s}{\omega_{LPF}}}$.
Instead for a VCO

$$\varphi_{OUT} = \int \omega_{OUT} dt = \int_0^t (\omega_{fr} + K_{VCO} V_{CONT}) dt = \omega_{fr} t + K_{VCO} \int_0^t V_{CONT} dt \qquad (1.7)$$

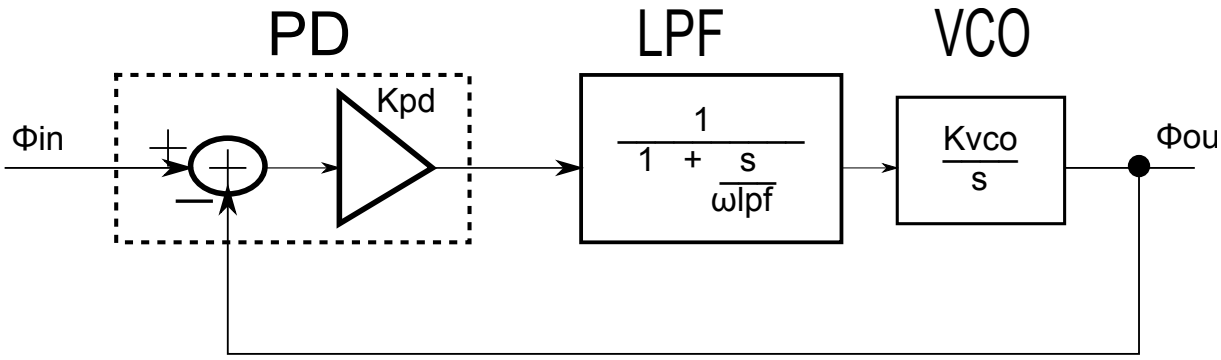

Figure 1.3: *Linear model of type 1 PLL*

Considering only the excess phase

$$\varphi_{OUT} = K_{VCO} \int_0^t V_{CONT} dt \tag{1.8}$$

Therefore in s domain the VCO has the transfer function

$$H_{VCO}(s) = \frac{\varphi_{OUT}(s)}{V_{CONT}(s)} = \frac{K_{VCO}}{s} \tag{1.9}$$

The open transfer function of the whole PLL is

$$H_{OPEN}(s) = K_{PD} H_{LPF}(s) H_{VCO}(s) = \frac{K_{PD} K_{VCO}}{s(1 + \frac{s}{\omega_{LP}})} \tag{1.10}$$

This has a single pole at the origin so this basic PLL is often called PLL type I (1 pole at the origin).
The closed transfer function is

$$H_{CLOSED}(s) = \frac{H_{OPEN}(s)}{1 + H_{OPEN}(s)} = \frac{K_{PD} K_{VCO} \omega_{LPF}}{s^2 + \omega_{LPF} s + K_{PD} K_{VCO} \omega_{LPF}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{1.11}$$

The natural frequency , damping factor and poles as respectively related to the PLL charac-

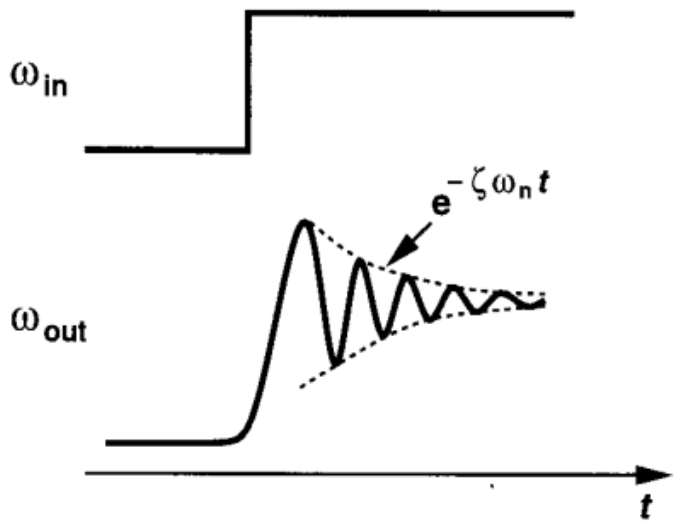

Figure 1.4: *Underdamped Response of PLL to a frequency step*

teristics as follows:

$$\omega_n = \sqrt{\omega_{LPF} K_{PD} K_{VCO}} \tag{1.12}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD} K_{VCO}}} \tag{1.13}$$

$$s_{1,2} = (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n \tag{1.14}$$

If $\zeta > 1$ the system is overdamped ,otherwise if $\zeta < 1$ the poles are complex and the response to a step change contains a sinusoid with frequency $\omega_n\sqrt{1-\zeta^2}$ which decays with a time constant $\tau = (\zeta\omega_n)^{-1}$.

1.1.3 PLL with integer divider

Using a frequency phase divider by an integer M in the feedback path it is possible change the output frequency changing the feedback divide ratio $\omega_{OUT} = M\omega_{IN}$ in steady state. M is an integer so the frequency resolution of the PLL is equal to the input frequency.

So the new closed loop transfer function is

$$H_{CLOSED}(s) = \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + \omega_{LPF}s + \frac{K_{PD}K_{VCO}\omega_{LPF}}{M}} = \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{1.15}$$

The natural frequency , damping factor becomes:

$$\omega_n = \sqrt{\frac{\omega_{LPF}K_{PD}K_{VCO}}{M}} \tag{1.16}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{M\omega_{LPF}}{K_{PD}K_{VCO}}} \tag{1.17}$$

Therefore changing the natural frequency and the damping factor also the loop dynamics change depending on the value of the divide ratio.

1.1.4 Limitations

Some limitations of the type I PLL are:

- To give a good stability the cut off frequency of the low pass filter is chosen to be $10\% - 20\%$ of the input frequency. This causes the settling time constant of the filter to be relatively high making the switching time from one to another frequency relatively slow;
- The phase offset between the output and the input is frequency dependent. If this phase offset has to be small then $K_{PD}K_{VCO}$ can be increased, but increasing $K_{PD}K_{VCO}$ gives a smaller damping factor and may cause instability;
- The frequency acquisition range can be very small: if there is a large frequency step at the input or if the input is substantially different from the VCO free running frequency then the loop may fail to lock.

1.2 Type II PLL

Type II PLL is used to overcome some limitations of Type I PLL. It is formed by a phase detector, a charge pump, a loop filter and a VCO.
This kind of PLL has desirable features: the input reference and the output oscillator waveforms are exactly in phase when the system is in lock, even when the input frequency is quite different from the free running frequency of the oscillator PLL attains lock quickly .

The capture range is only limited by the VCO output frequency range and the static phase error $\Delta\varphi$ is zero if mismatches and offsets are negligible.

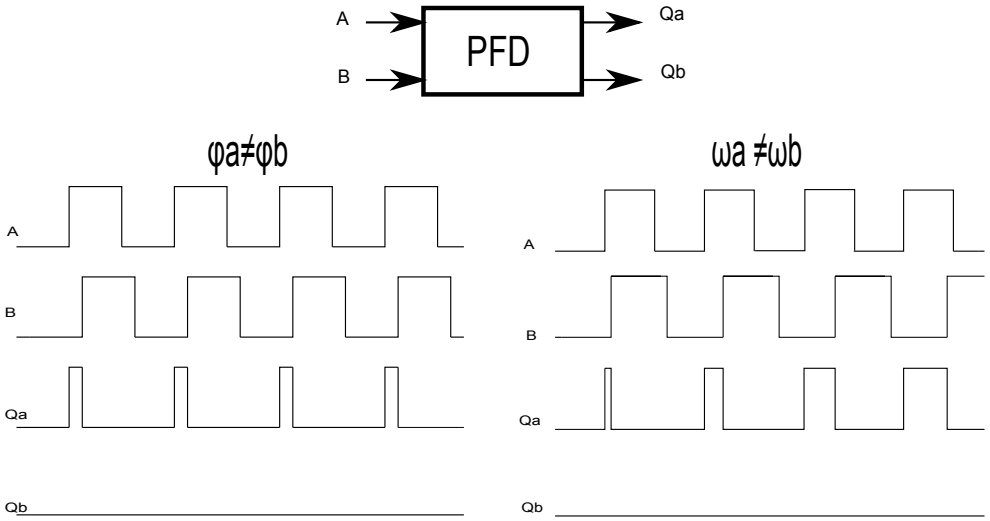

Figure 1.5: *Conceptual operation of a PFD*

1.2.1 Loop dynamics

The phase frequency detector (**PFD**) is a circuit that can be detect both phase and frequency difference. It proves extremely useful because it significantly increases the acquisition range and lock speed of PLL. The classical implementation is based on two D type flip flops and an AND gate. It generates outputs whose mark/phase ratio depends on the difference in frequency and phase of the two input signals.
If the frequency of the input A is greater than the input B (Fig. 1.5), then the PFD produces positive pulses at Q_A while Q_B remains at zero.Vice versa positive pulses appear at Q_B while Q_A remains at zero. If the two input signals frequencies are the same the circuit generates pulses at either Q_A or Q_B with a width equal to phase difference between the two inputs .
Thus the average value of $Q_A - Q_B$ is an indication of the frequency of phase difference between A and B. The output Q_A and Q_B are respectively called UP and DOWN.

The charge pump (**CP**) is used to convert the outputs of the PFD to an analog current that is converted to a voltage, via the loop filter, that will be the VCO input.It consists of two switches S_1 and S_2 controlled by the outputs of the PFD Q_A,Q_B and in the easiest case there is a capacitor C_P , i.e. the loop filter.

When Q_A is high S_1 is closed and the capacitor is charged with current I_{CP}, causing its voltage to rise and so the VCO frequency to increase. When Q_B is high S_2 is closed and the

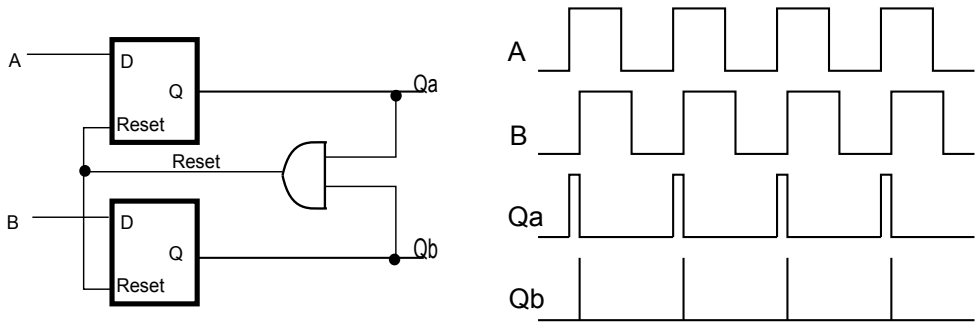

Figure 1.6: *Implementation of a PFD and circuit working*

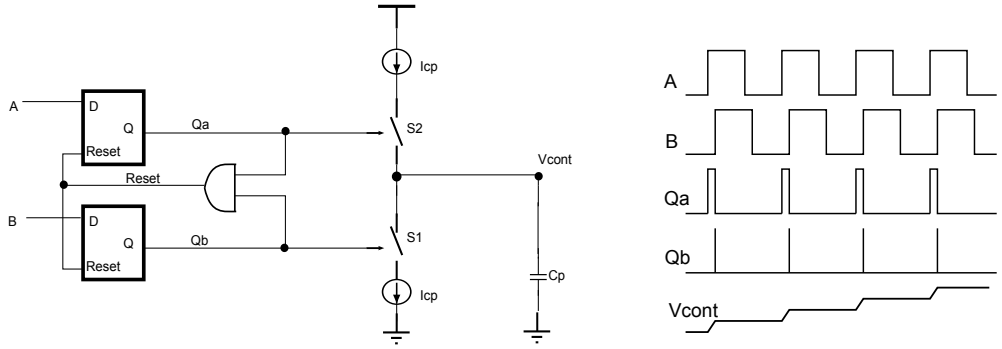

Figure 1.7: *PFD with Charge Pump*

capacitor is discharged with current I_{CP} causing its voltage to drop and the VCO frequency to decrease. Instead when Q_A and Q_B are both low, both switches are closed and the voltage remains constant.

Considering the case which A and B have the same frequency (and so the same period T), but A leads B and the difference phase is $\Delta\varphi$ then the time between their rising edges is $\Delta t = (\Delta\varphi/2\pi)T$. During this time switch S_1 is ON and the capacitor is charged with current I_{CP}. During the interval Δt the capacitor is charged with current I_{CP} giving a voltage rise rate of $I_{CP}/C_P[V/s]$. The total voltage rise in this interval is

$$\Delta V_C = \frac{I_{CP}}{C_P}\Delta t = \frac{I_{CP}}{C_P}\frac{\Delta\varphi}{2\pi}T \tag{1.18}$$

During the remainder of the period of A the switches are turned off and the voltage on the capacitor keeps constant. Thus on average the voltage rises by ΔV_C in the whole period T,

approximating the V_C as a straight line. Therefore

$$\frac{\partial V_C}{\partial t} \approx \frac{\Delta V_C}{T} = \frac{I_{CP}}{2\pi C_P}\Delta\varphi \Rightarrow V_C = \frac{I_{CP}}{2\pi C_P}\int \Delta\varphi \Rightarrow V_C(s) = \frac{I_{CP}}{2\pi C_P}\frac{1}{s}\Delta\varphi(s) \tag{1.19}$$

The closed loop transfer function of this system has two imaginary poles(2 poles at the origin $\Rightarrow$ Type II PLL) can be unstable. To avoid stability problems a zero is added to the open loop transfer function by placing a resistor in series with the charge pump capacitor. An extra smoothing capacitor is often used to smooth out the rapid voltage steps which would occur from the other capacitor being charged through a resistor by means of a switch which is opening and closing.

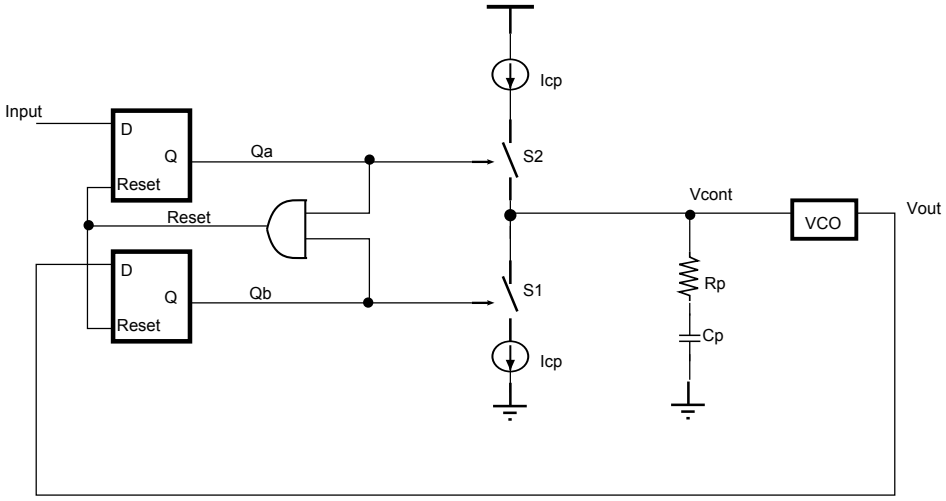

Figure 1.8: *Addition of zero to chrge-pump PLL*

1.2.2 Transfer function

If it is not considered the smoothing capacitor the transfer functions are:

$$H_{OPEN}(s) = \frac{\varphi_{OUT}(s)}{\varphi_{IN}(s)} = \frac{I_{CP}K_{VCO}}{2\pi s}(R_P + \frac{1}{sC_P}) \tag{1.20}$$

$$H_{CLOSED}(s) = \frac{H_{OPEN}(s)}{1 + H_{OPEN}(s)} = \frac{\frac{I_{CP}K_{VCO}}{2\pi s}(1 + sR_PC_P)}{s^2 + \frac{I_{CP}K_{VCO}}{2\pi}R_Ps + \frac{I_PK_{VCO}}{2\pi C_P}} = \frac{\frac{I_{CP}K_{VCO}}{2\pi s}(1 + sR_PC_P)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{1.21}$$

So the natural frequency and the damping factor are :

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi C_P}} \tag{1.22}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_{CP}C_PK_{VCO}}{2\pi}} \tag{1.23}$$

1.2.3 PLL with integer divider

Using a feedback divider, with a divide ratio M, the closed loop transfer function is:

$$H_{CLOSED}(s) = \frac{\frac{I_{CP}K_{VCO}}{2\pi\mathbb{C}_P}(1+sR_PC_P)}{s^2+\frac{I_{CP}K_{VCO}}{2\pi M}R_Ps+\frac{I_{CP}K_{VCO}}{2\pi C_PM}} = \frac{\frac{I_{CP}K_{VCO}}{2\pi\mathbb{C}_P}(1+sR_PC_P)}{s^2+2\zeta\omega_ns+\omega_n^2} \tag{1.24}$$

Then the natural frequency and the damping factor are:

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi C_PM}} \tag{1.25}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_{CP}C_PK_{VCO}}{2\pi M}} \tag{1.26}$$

Placing a divider M in the feedback loop decreases the natural frequency and the damping factor. To maintain the same stability as a PLL without a divider the other loop parameter such as K_{VCO} or I_{CP} have to be increased.
With or without divider if R_P is zero also the damping factor is zero, that is the system will not converge to a steady state solution on response to a step unit.

Chapter 2

Phase Frequency Detector (PFD)

Different PFD topologies are discussed in this chapter. PFD non ideality effects are treated in the first part of chapter five, whereas the PFD operational principle is explained in the former chapter. To make a phase frequency detector there are different solutions. Three different PFD implementations are here depicted: the first two ones are based on the typical scheme with two flip flop D (DFF), the third is based on SR latches and monostables. All these circuits were experimentally tested.

2.1 PFD made with DFF

These circuits are based on the circuit illustrated in Fig. 1.6. To a better understanding of the pulse timing it is supposed the inputs A and B are the same frequency but A leads B. The figure 2.1 shows at points

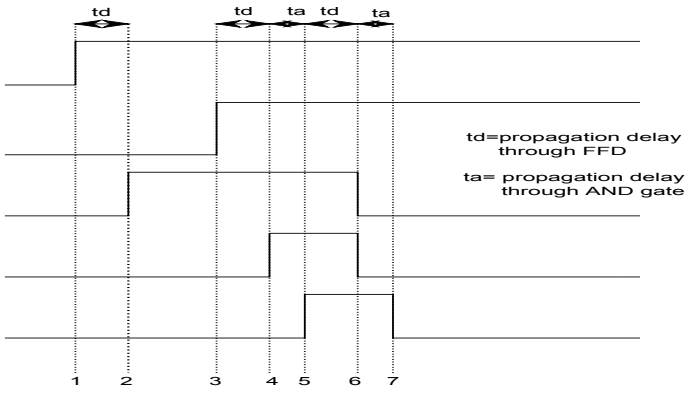

Figure 2.1: *Show Pulse Timing*

1. Input A goes high.
2. Signal A propagates through the DFF and the output Q_A goes high.
3. Input B goes high.
4. Signal B propagates through the DFF and the output Q_B goes high.
5. As Q_A is already high Q_B propagates through the ADN gate causing its output , the reset , to go high.
6. The reset signal propagates through both DFFs and their output go low.
7. Q_A and Q_B propagate through the AND gate so its output , the reset , goes low.

The DFF may employ different logics. Basically CMOS static logic and in dynamic logic are the two main categories. The second one can be implemented using different architectures like the TSPC(True Single Phase Clocked). TSPC is the only dynamic implementation considered in this work.

- In the CMOS static logic there is always a low impedance path between the output and either the supply voltage or the ground. Ideally there is no power static consumption, but direct path consumption due to the current that can flow across the pull up and pull down networks during the commutations and dynamic consumption due to charge and discharge of parasitic and load capacitances are present. The main limit of this logic is the high number of gates necessary. This logic has very low noise margins.

- In the dynamic logic there is not always a mechanism driving the output high or low. The output information is temporally stored as charge in the output capacitance, thus yields the circuit very sensible to the disturbs (e.g. capacitive couplings). It needs less transistors to implement the same logic function respect the static logic. Then the whole circuit is more compact and faster than one implemented in static logic since there are a less output capacitance, so the inputs has to charge and discharge smaller gate capacitances. This logic increases the number of transistors that are switching at any given time, increasing so the power static consumption over static CMOS.

In CMOS static logic the DFFs is a simple circuit such as that in Fig. 2.2 . It is made with two cross-coupled SR latches, both respond to the rising edges of CK and Reset respectively.

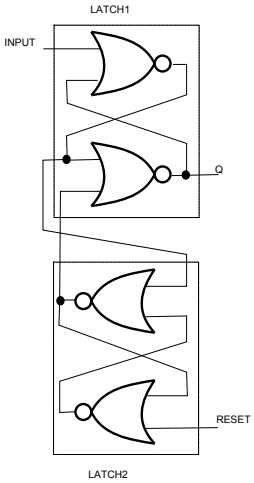

Figure 2.2: *DFF in CMOS technology*

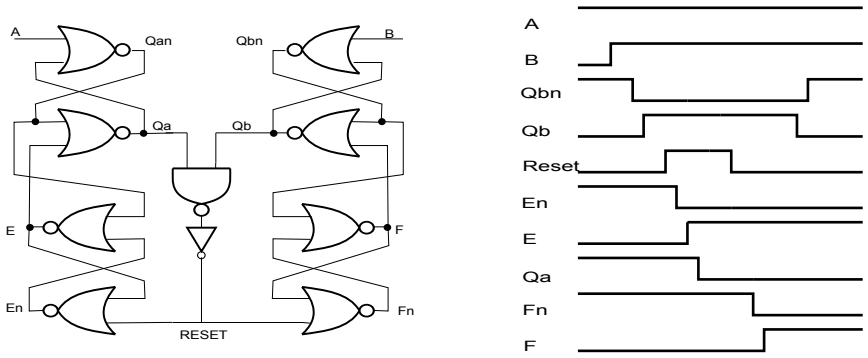

Figure 2.3: *PFD in CMOS technology*

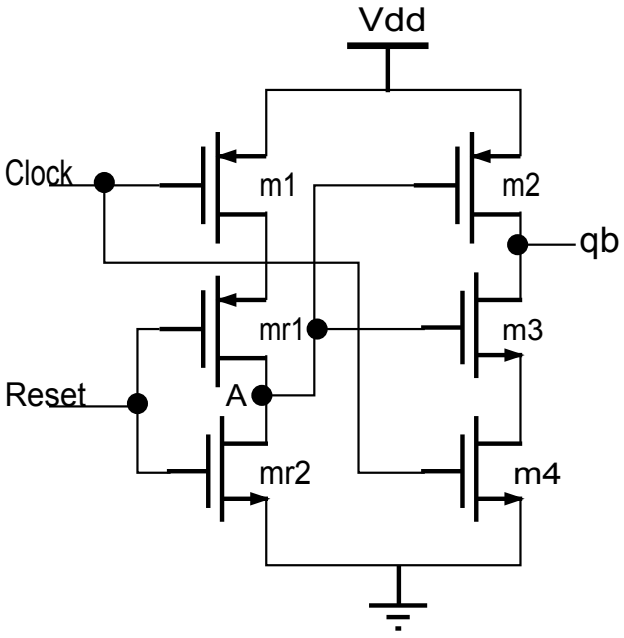

Figure 2.4: *DFF in TSPC technology*

Observing the Figure 2.3 due to the high gate numbers the propagation time is considerable. This circuit can not work at high frequencies but, as said before, for lower frequencies it has good performances because of the low power absorbed and the robustness.

As illustrated in Figure 2.4 a DFF, in TSPC logic, is made using six transistors. It has only the denied (complementary) output. When D, i.e. the input, and the reset are low, A is charged to Vdd by m1 and m2. The output qb is floating and it keeps is logic value. At the positive edge of D input, qb is connected to ground by m3 and m4. Till reset maintains the low logic, value A does not change and therefore also qb does not change. When reset goes high A is connected to ground through m2, m3 turns OFF, m2 turns ON and so qb goes high.

2.2 PFD with SR latches

All the blocks in this circuit are implemented using CMOS static complementary logic. In this phase frequency detector each DFF is substituted with a monostable and a SR latch. The feedback path is made with a NAND gate which inputs are the output of the latches SR, every one formed by two cross coupled NANDs. The monostable circuit generates a narrow pulse (high-low-high) when there is a positive edge at its. It is made as shown in Fig. 2.5 by a NAND gate and a chain with an odd number of inverter gates. When the input signal is constant the inputs of the NAND gate are opposites each other so its output is high. When at the input there is a transition low-high, for a brief period, depending on the delay produced by the inverter chain, both NAND inputs are high so the NAND output goes low. The outputs of the NAND gates are the SR latches set signals, instead of the reset signals of the two latches are controlled by a cascade of a NAND and two inverter gates. The reset consists on a pulse. It is always high except when both latches output goes high, in this case the NAND output goes low.
The number of the inverter gates into the monostable chain has to be a trade off between the output pulse width and the power consumption. Indeed if the number of the inverters is low the output pulse can not reach the low state, compromising so the work of the downstream circuit. Whereas if the number of inverter gates is to high the power consumption increases especially due to parasitic and load capacitances charging and discharging. On the other hand increasing the number of the inverters into the chain, the robustness of the circuit to rising and falling edges increases. Also the width of the output monostable pulse is bigger increasing the number of inverter gates.

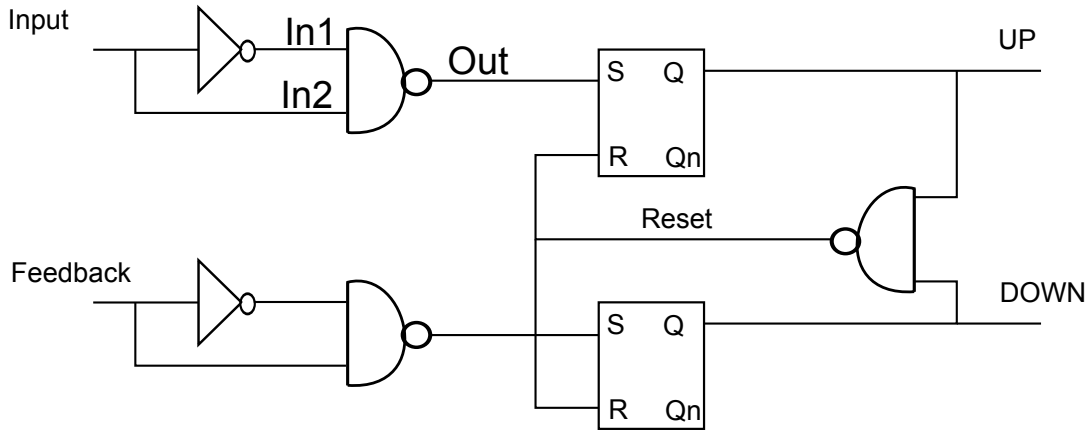

Figure 2.5: *PFD with latch SR*

For different inputs and number of inverter gates in the chain of the upper monostable in Fig 2.5 figure 2.6 shows the various working. In Fig. 2.6(a) the input has a rapid rise edge and the chain has a small number of inverter gates. In fig. 2.6(b) the input has a rapid rise edge and the chain has an adequate number of inverter gates. In fig. 2.6(c) the input has a slow rise edge and the chain has a small number of inverter gates. In fig. 2.6(d) the input has a slow rise edge and the chain has an adequate number of inverter gates.

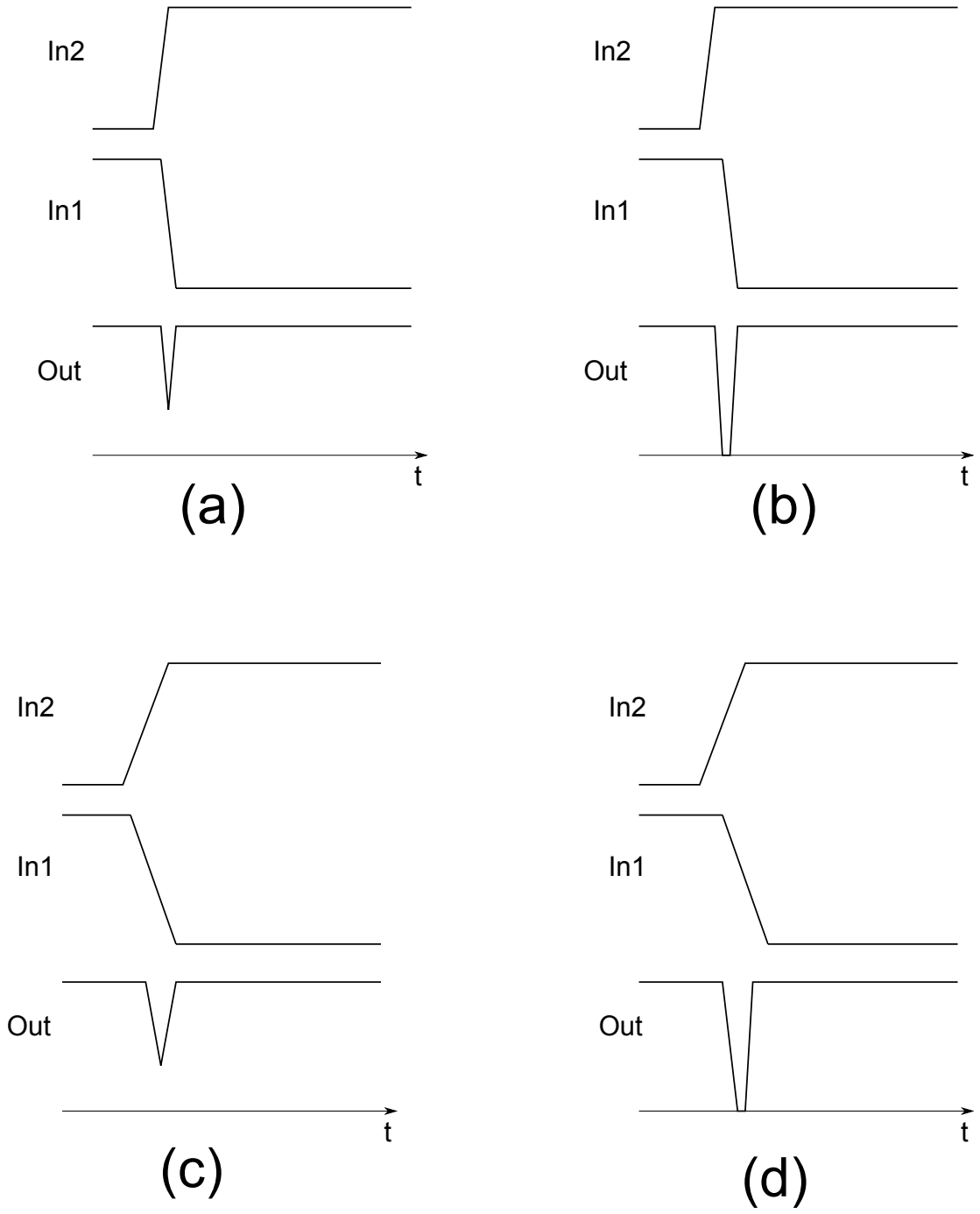

Figure 2.6: *Monostable working*

Chapter 3

Charge Pump CP

Different CP topologies are discussed in this chapter. CP non ideality effects are treated in the first part of chapter five, whereas the PFD operational principle is explained in the former chapter. Other issues that affect charge pump not discussed in the five chapter are current consumption and switching speed. They will be considered together the various CMOS architectures in the following sections.

3.1 Single Ended CP

Single ended charge pumps are widely used because of they do not need further loop filters and they have lower power consumption than other architectures. Three classical topologies are drawn in Figures 3.1.

Figure 3.1(a) illustrates the charge pump with the switch at the drain of the current mirror MOS. The pull down network is considered. When the switch controlled by DOWN signals is turned OFF, the charge stored inside drain of M1 is completely discharged and the drain voltage decreases to zero. After the same switch is turned ON, M1 is not in saturation region but in the triode region until the voltage at the drain of MI is higher than the minimum saturation voltage, Meanwhile the voltage at the drain of M1 increases from the low state to the loop filter voltage held by PLL. During this period, high current peaks are generated. In the pull up network the same situation occurs and the matching of this peak current is difficult since the amount of the peak current varies with the output voltage. So this circuit is typified by extra currents during the turning OFF and ON of the two switches.

Figure 3.1(b) shows the charge pump where the gate is switched instead of the drain. With this configuration the current mirrors are every moment in saturation region. Considering the pull

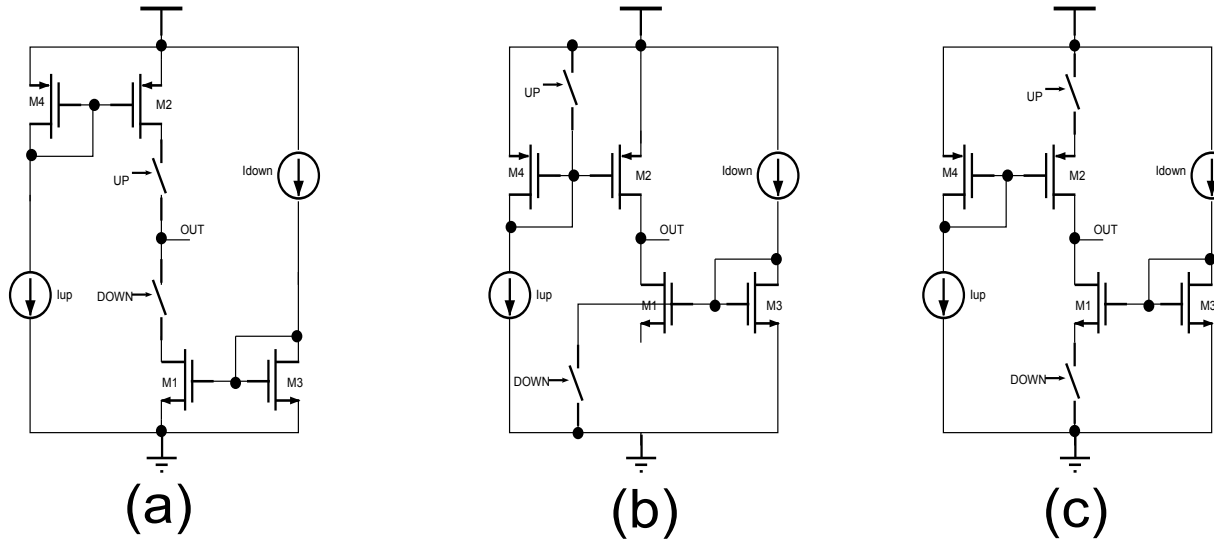

Figure 3.1: *Single Ended CP : switch in drain (a), switch in gate (b), switch in source (c)*

down network when the switch is turned ON the gate voltage of M1 goes to low state switching OFF M1. The completely discharging of the drain capacitance is so avoided and therefore when the transistor is returned ON it is already in saturation region, reducing so the current peaks. If $V_{gs} > V_{tn}$ M3 is in saturation. The switch transistor dimensions has to be bigger than M3 ones so that the current flows through the switch turning off M1 and M3. So the outputs of the phase detector have to charge and discharge capacitance no too small, decreasing the speed of the whole PLL.

In the third configuration the switch are placed in series with the source of the current mirror MOS as shown in Fig. 3.1(c). M1 and M2 are always are saturation. Different from the gate switching (Fig. 3.1(b)), low bias current can be used with high output current since it is not required transistor with large dimensions like in the previous configuration. This topology has a faster switching time than the gate switching because of the switch is connected to single transistor with lower parasitic capacitance.

In Figure 3.2 are depicted other configurations with some variations to improve the performance. In all these configurations there are also the complementary signals, so even if the output charge pump is floated the currents can flow using different paths. Therefore the transistors are always in saturation reducing the charge sharing and increasing the CP speed.

Figure 3.2(a) shows the charge pump with an active amplifier. This solution compensates the charge sharing problem seen in the circuit of the Fig. 3.1(a). With a unity gain amplifier, the voltage of the drain of the transistor driven by UP and the voltage of the drain of the transistor driven by DWB are set to the same voltage, i.e. the output voltage when the switch is OFF,

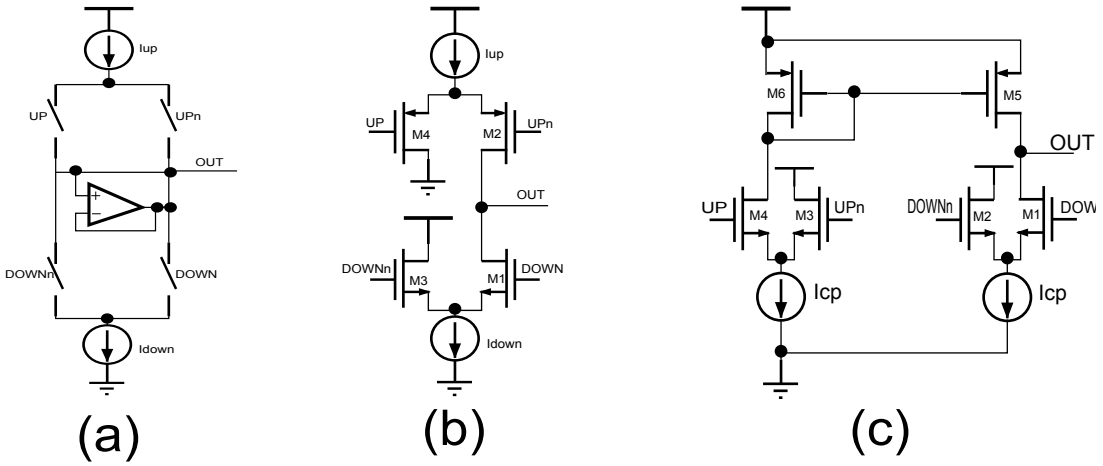

Figure 3.2: *Variations of single-ended charge pumps : (a) with active amplifier, (b) with current steering switch, (c) with nMOS only*

reducing so the charge sharing effect when the switch is turned ON.
The circuit in Fig. 3.2(b) has performance similar to the circuit in Fig. 3.1(b) but the switching time is improved by using the current switch. This structure provides high speed single ended CP.
In Fig. 3.2(c), the mismatch of PMOS and NMOS is avoided using only NMOS switches. Since the current does not flow in the current mirror, M5 and M6, when UP switch is turned OFF, the current mirrors can limit the performance unless large current is used. All the circuit just described are based on simple current mirrors made with only two transistors.

Figure 3.3 shows an improved schematic of Fig. 3.1(c). M4 - M13 are transistors of the current mirrors which are cascoded to increase the output impedance so that the current variation is less sensitive to the output voltage. In the other hand current mirror cascode reduces the values of the output charge pump voltage, and it is difficult used it in circuit with limited voltage sources.

In the fourth paragraph of the paper [6] there is a comparison between the performances of the different CP types. Here there is a brief summary of this paragraph.

- CP in Figures 3.1 , 3.2(a),3.3 have low power consumption , moderate speed and moderate clock skew .

- CP in Figure 3.2(b) has static current consumption high speed and moderate clock skew.

- CP in Figure 3.2(c) has medium power consumption , moderate speed and low clock skew.

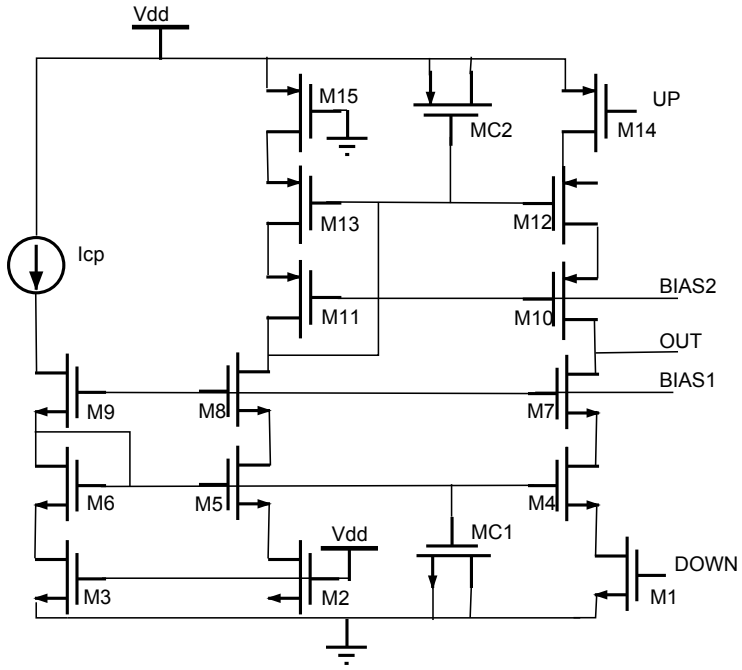

Figure 3.3: *CP with Cascode Current*

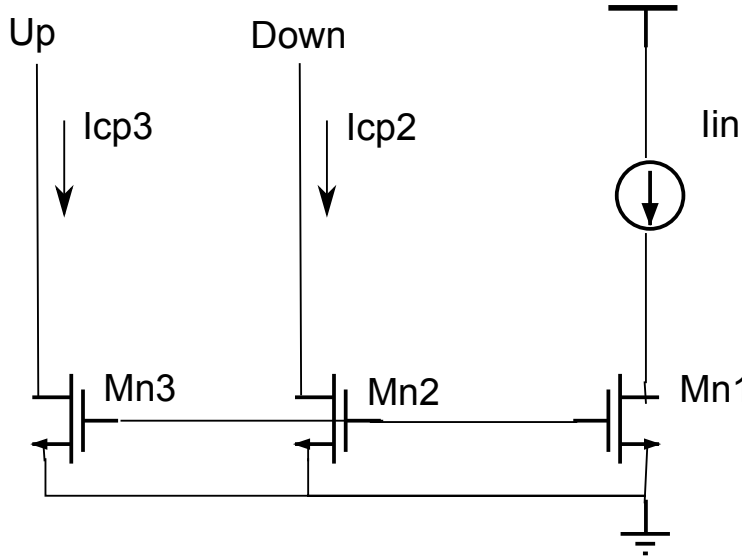

Figure 3.4: *Current Mirror*

3.1.1 Design of Current Mirrors

In this brief paragraph it is explained how designing the current mirrors (Fig. 3.4) for the circuit in Fig. 3.2(c). The two currents I_{CP} of this circuit are the outputs current of two current mirrors. Circuit in Fig. 3.4 is linked to Fig. 3.2(c) in this way : M1 source and M2 source are connected to Mn2 drain, while M3 source and M4 source are connected to Mn3 drain. The gate terminals of Mn1 is connected to its respective drain. This last transistor is always in saturation. Hence watching the circuit topology in Figure 3.4 is is easy to write $V_{DSn1} = V_{GSn1} = V_{GSn2}$ and $V_{DSn1} = V_{GSn1} = V_{Gn3}$. Assuming the absence of the channel length modulation , one finds:

$$I_{in} = I_{Dn1} = \frac{\mu_{n1} C_{ox1} W_{n1}}{2L_{n1}} (V_{GS_{n1}} - V_{tn1})^2 = I_{Dn2} = \frac{\mu_{n2} C_{ox2} W_{n2}}{2L_{n2}} (V_{GSn2} - V_{tn2})^2 = I_{CP2} \tag{3.1}$$

$$I_{in} = I_{Dn1} = \frac{\mu_{n1} C_{ox1} W_{n1}}{2L_{n1}} (V_{GS_{n1}} - V_{tn1})^2 = I_{Dn3} = \frac{\mu_{n3} C_{ox3} W_{n3}}{2L_{n3}} (V_{GSn3} - V_{tn3})^2 = I_{CP3} \tag{3.2}$$

Since transistors n type are identical

$$\frac{I_{CP2}}{I_{in}} = \frac{W_{n2}/L_{n2}}{W_{n1}/L_{n1}} \tag{3.3}$$

$$\frac{I_{CP3}}{I_{in}} = \frac{W_{n3}/L_{n3}}{W_{n1}/L_{n1}} \tag{3.4}$$

The small signal output resistances are :

$$r_{outn2} = 1/\lambda I_{CP2} \propto \frac{L_{n2}}{W_{n2}} \tag{3.5}$$

$$r_{outn3} = 1/\lambda I_{CP3} \propto \frac{L_{n3}}{W_{n3}} \tag{3.6}$$

So to increase the poor output resistance of the current mirrors is necessary increase the length of the current mirrors transistors.

Chapter 4

Loop Filter

Basing also on the exposition of the first chapter it is a plain fact that the minimum loop filter configuration in practice includes the additional capacitor (smoothing capacitor) in parallel to the RC section. So the transfer function of the loop filter impedance is

$$Z_f(s) = \frac{1}{s(C_1+C_2)} \frac{1+sR_1C_1}{1+sR_1(\frac{C_1C_2}{C_1+C_2})} = \frac{k}{s}\frac{1+s\tau_2}{1+s\tau_3} = \frac{k}{s}\frac{1+s\tau_2}{1+s\tau_2/b} \tag{4.1}$$

Where τ_2 is the time constant of the stabilizing zero, τ_3 is the time constant of the pole which is used to attenuate the reference frequency and its harmonics and $b = \tau_2/\tau_3 = 1 + C_1/C_2$.
In practice PLL is never a second order system, therefore it is not possible use the theory based on the natural frequency and damping factor concepts typical in a second order system analysis. So to dimension the loop filter parameters it will make use of the open loop bandwidth and phase margin concepts.
For ease of explanation it is here reported the linear phase model of a PLL .

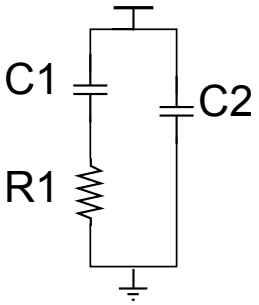

Figure 4.1: *Loop Filter $Z_f(s)$*

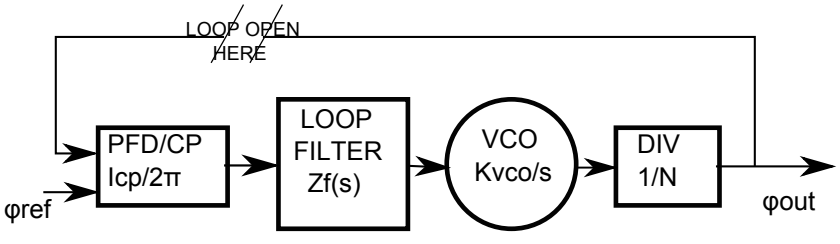

Figure 4.2: *Linear model of a PLL*

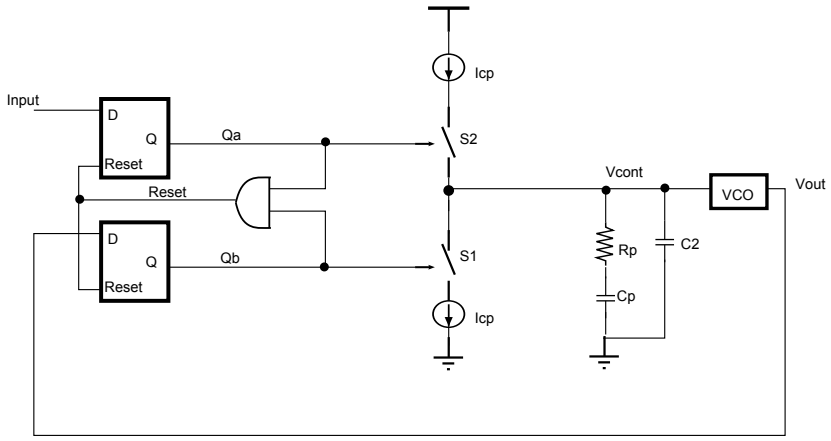

Figure 4.3: *PLL with a third order loop filter*

The open loop transfer function is expressed as

$$G(s) = \frac{\varphi_{OUT}(s)}{\varphi_{REF}(s)} = \frac{I_{CP}}{2\pi} Z_f(s) \frac{K_{VCO}}{s} \frac{1}{N}. \tag{4.2}$$

The open loop bandwidth $f_c = \omega_c/2\pi$ is the frequency when $|G(j\omega_c)| = 1(or = dB)$. The phase margin is defined as $\phi_m = \angle(G(j\omega_c)) + \pi$.
The open loop transfer function at ω_c from (4.2) yields

$$|G(j\omega_c)| = \frac{I_{CP}K_{VCO}k}{2\pi N} \frac{1}{\omega_c^2} \frac{|1 + j\omega_c\tau_2|}{|1 + j\omega_c\tau_3|} = \frac{I_{CP}K_{VCO}k}{2\pi N} \frac{1}{\omega_c^2} \frac{\sqrt{1 + (\omega_c R_1 C_1)^2}}{\sqrt{1 + (\omega_c R_1 \frac{C_1C_2}{C_1+C_2})^2}} = 1 \tag{4.3}$$

This happens when

$$I_{CP} = \frac{(C_1 + C_2)N\omega_c^2 2\pi}{K_{VCO}k} \frac{\sqrt{1 + (\omega_c R_1 \frac{C_1C_2}{C_1+C_2})^2}}{\sqrt{1 + (\omega_c R_1 C_1)^2}} \tag{4.4}$$

The phase of $G(j\omega)$ from (4.2) is denoted as

$$\Psi(j\omega) = -\pi + \angle(1 + j\omega\tau_2) - \angle(1 + j\omega\tau_3) = -\pi + tan^{-1}(\omega\tau_2) - tan^{-1}(\omega\tau_3) \tag{4.5}$$

The point of zero derivative of the phase response will be ω_{MAX}, this frequency corresponds to the maximum value of $\Psi(j\omega)$ for given values of τ_2 ans τ_3. It values

$$\omega_{MAX} = \sqrt{\frac{1}{\tau_2\tau_3}}. \tag{4.6}$$

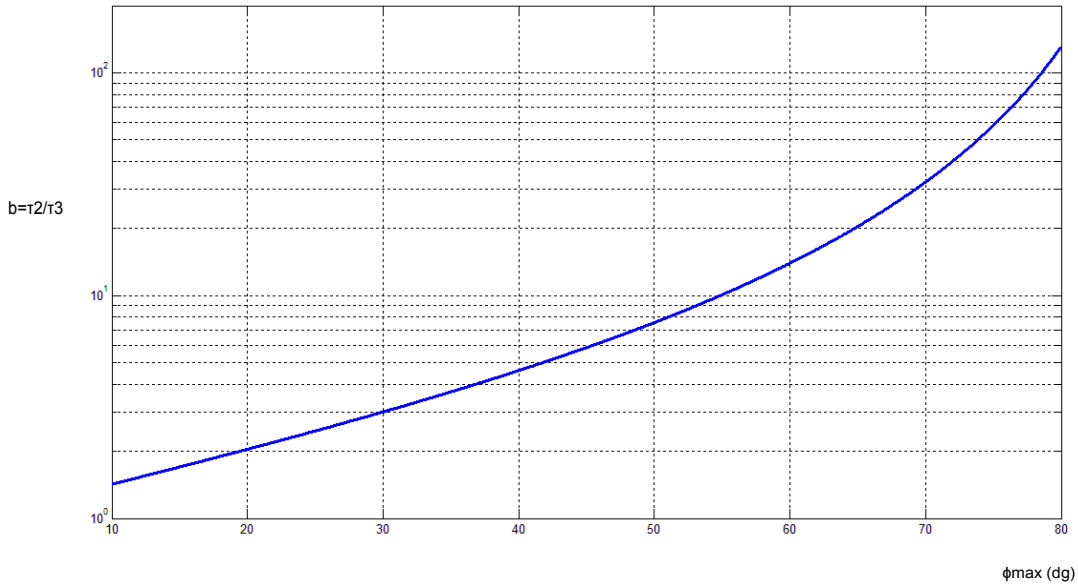

Figure 4.4: *Value of the ratio of the time constant $b = \tau_2/\tau_3$ as a function of the $G(j\omega)$ phase*

Using the last two equations it is calculated the value of the maximum phase advance

$$\phi_{MAX} = \Psi(j\omega_{MAX}) + \pi = tan^{-1}\left(\frac{\tau_2 - \tau_3}{2\sqrt{\tau_2 - \tau_3}}\right) = tan^{-1}\left(\frac{b-1}{2\sqrt{b}}\right). \tag{4.7}$$

Solving the equation for b as a function of ϕ_{MAX} yields

$$b = \frac{1}{(-tan\phi_{MAX} + 1/cos\phi_{MAX})^2} \tag{4.8}$$

The numerical values of b as a function of ϕ_{MAX} are plotted in figure 4.4.

Assuming $\omega_c = \omega_{MAX}$ then $\phi_m = \phi_{MAX}$. From equation 4.6 and knowing that $b = \tau_s/\tau_3$ results

$$\tau_2 = \frac{\sqrt{b}}{\omega_c} \tag{4.9}$$

$$\tau_3 = \frac{1}{\sqrt{b}\omega_c}. \tag{4.10}$$

Replacing the equations (4.9) and (4.10) into (4.3) yields

$$\omega_c = \frac{I_{CP}K_{VCO}k}{2\pi N\omega_c}\sqrt{\frac{1+\sqrt{b}^2}{1+\sqrt{1/b}^2}} = \frac{I_{CP}K_{VCO}}{2\pi N\omega_c}R_1\frac{b-1}{b} = K\frac{b-1}{b} \tag{4.11}$$

The value of the loop filter components can be calculated. The results are

$$R_1 = \frac{2\pi N\omega_c}{I_{CP}K_{VCO}}\frac{b}{b-1} \tag{4.12}$$

$$C_1 = \tau_2\, R_1 \tag{4.13}$$

$$C_2 = 1/R_1\frac{\tau_2\tau_3}{\tau_2-\tau_3} \tag{4.14}$$

The theoretical open loop transfer function bode diagrams are plotted in Figure 4.5 for different values of phase margin ϕ_m.

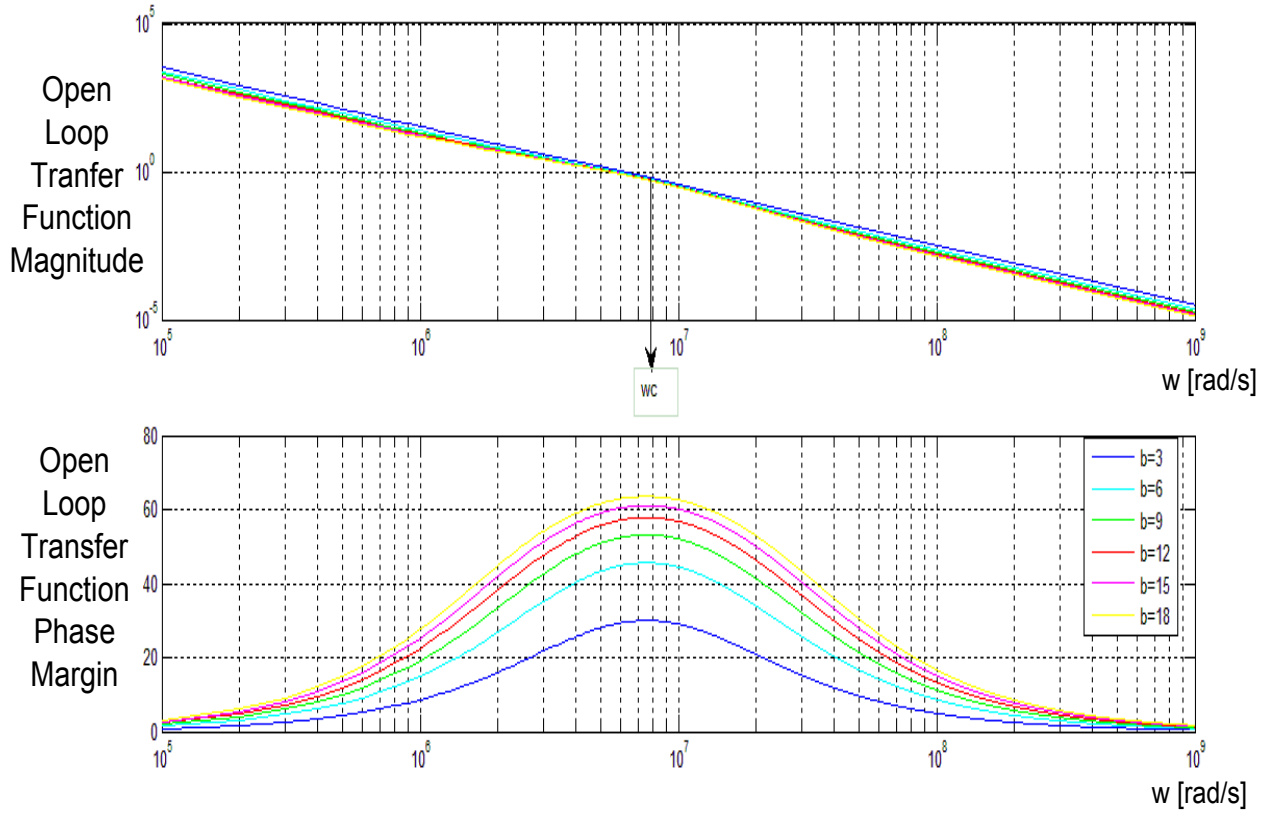

Figure 4.5: *Open loop frequency tranfer for different values of b*

Chapter 5

Imperfections in Practical PLL

5.1 Phase Frequency Detector and Charge Pump Nonidealities

Figure 1.6 illustrates the scheme and the working of a phase frequency detector(PFD). As explained in the former chapter when the input signals are out of phase, the system generates the pulses Q_A or Q_B, whose length is proportional to the phase error.

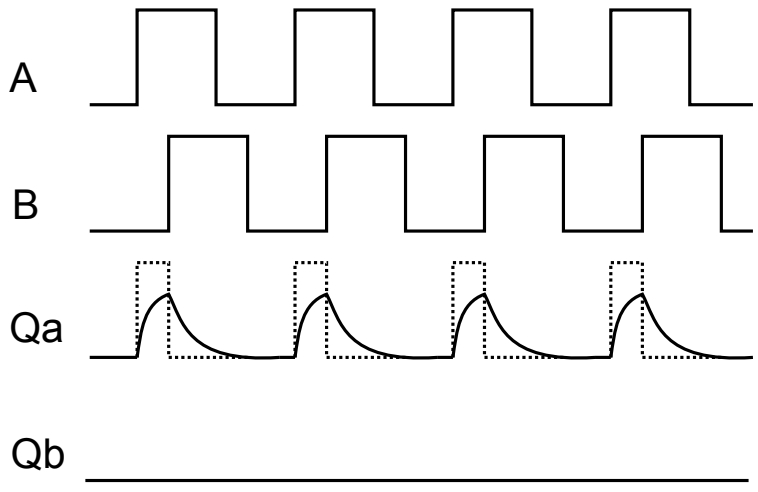

Figure 5.1: *Output Waveforms of a PD with a small input phase difference*

The Figure 5.1 shows the PFD outputs when there is a small phase difference between the two inputs. The system would provide very narrow pulses, but due to rising time, falling time and

delays the pulse is not able to reach completely the high state, hence the corresponding charge pump switch could be not ON. If the input phase difference $\Delta\theta$ falls below a certain value θ_0 then the output voltage of the charge pump is no longer a function of $\Delta\theta$. As depicted in Fig. 2.2 for $|\Delta\theta| < \theta_0$ the charge pump does not injects current. So the PFD charge pump circuit suffers from a dead zone, its width is $-\theta_0 \div \theta_0$. This phenomena is undesirable because it allows the VCO to accumulate as much random phase error as θ_0 respect to the input while receiving no corrective feedback. So this error is not rectified and the PLL output signal is attacked from jitter when $|\Delta\theta| < \theta_0$.

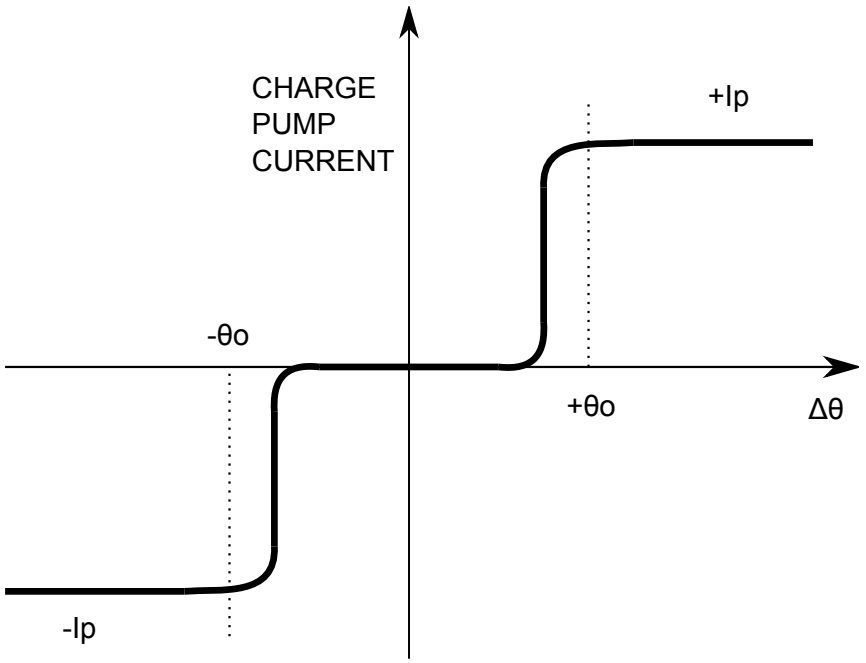

Figure 5.2: *Dead Zone*

In the ideal case the output charge pump current can be considered as current pulses of amplitude I_{CP}. As depicted in figure 5.3 the output pulses duty cycle δ_{CP} is $\Delta\theta/2\pi$, again $\delta_{CP} = \tau f_{REF}$ with τ the active time of the charge pump output and f_{REF} the frequency of the reference signal. The Fourier series expression for a periodic train of this pulses kind is:

$$I_{OUT}(t) = I_{CP}\delta_{CP} + 2I_{CP}\delta_{CP}\sum_{n=1}^{\infty}\frac{sin(n\pi\delta_{CP})}{n\pi\delta_{CP}}cos(2\pi n f_{REF}t) \tag{5.1}$$

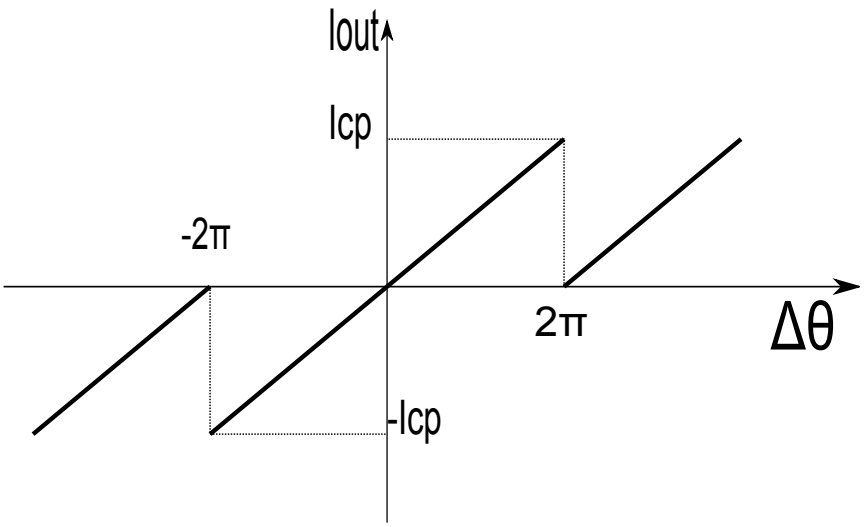

Figure 5.3: *Phase to current transfer of the PFDCP combination*

If δ_{CP} has a small value , it is possible to rewrite this equation like

$$I_{OUT}(t) = I_{CP}\delta_{CP} + 2I_{CP}\delta_{CP}\sum_{n=1}^{\infty} cos(2\pi n f_{REF} t) \tag{5.2}$$

Ideally in locking condition the phase error θ would be zero, so δ_{CP} would be zero and consequently also the output current would be zero. In practice this does not happen, generating therefore reference spurious breakthrough , basically because of the presence of :

- leakage currents in loop filter;
- mismatch in charge pump current sources.

5.1.1 Leakage Current

Leakage currents in the loop filter modify the voltage storage in the capacitor. The sources of these leakage currents are, the capacitor itself, the input of VCO and the charge pump output. In lock situation PLL has to have a tuning voltage constant for several periods of the reference input. As illustrated in Fig 5.5 this is achieved when the charge output current I_{OUT} equals the average value I_{leak}, that is the loop reacts to the leakage current I_{leak} restoring the charge lost during a reference period to the loop filter at the next correction moment. In lock condition

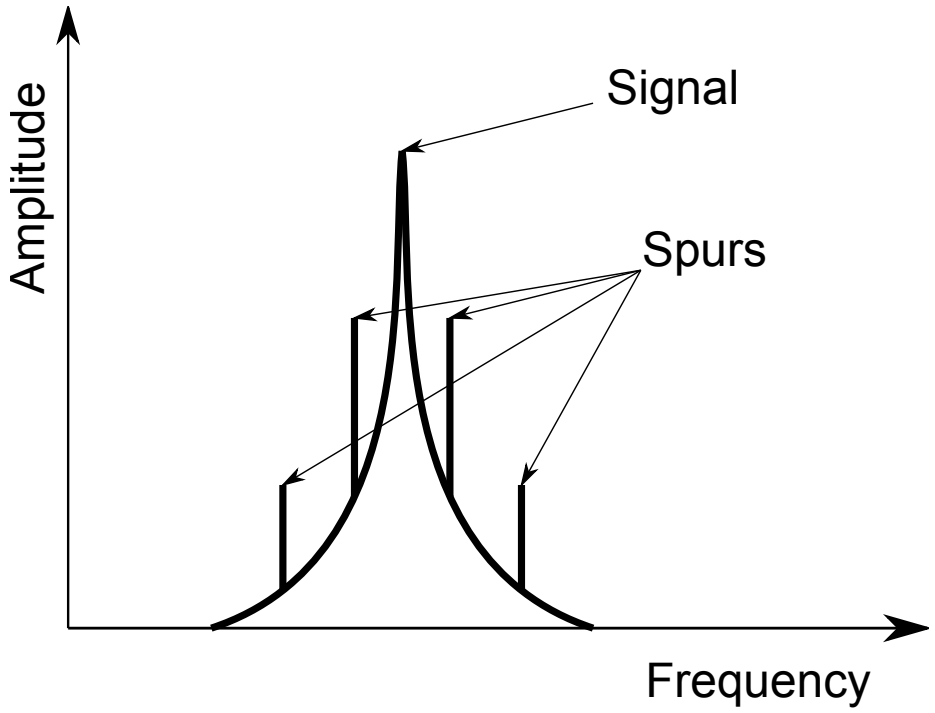

Figure 5.4: *Reference Spurious*

$I_{OUT} = I_{leak} = \delta_{CP} I_{CP}$, using this relation the equation can be rewritten as

$$I_{OUT}(t) = I_{leak} + 2I_{leak} \sum_{n=1}^{\infty} cos(2\pi n f_{REF} t) \tag{5.3}$$

The peak phase deviation $\Theta_p(f_m)$ is linked with the peak frequency deviation $\Delta_f(f_m)$ and the modulation frequency by the equation

$$\Theta_p(f_m) = \frac{\Delta_f(f_m)}{f_m} \tag{5.4}$$

The peak frequency deviation is the product of the magnitude of the spectral components of the ripple voltage at the tuning line $V_{ripple}(nf_{ref})$ with the VCO gain. Using equation 5.3, it is drawn immediately

$$V_{ripple}(nf_{ref}) = 2I_{leak}|Z_f(j2\pi nf_{ref})|. \tag{5.5}$$

With the help of the last two equations , it is possible to write the following equation

$$\Theta_p(nf_{ref}) = \frac{\Delta_f(nf_{ref})}{nf_{ref}} = \frac{V_{ripple}(nf_{ref})K_{VCO}}{nf_{ref}} = \frac{2I_{leak}|Z_f(j2\pi nf_{ref})|K_{VCO}}{nf_{ref}} \tag{5.6}$$

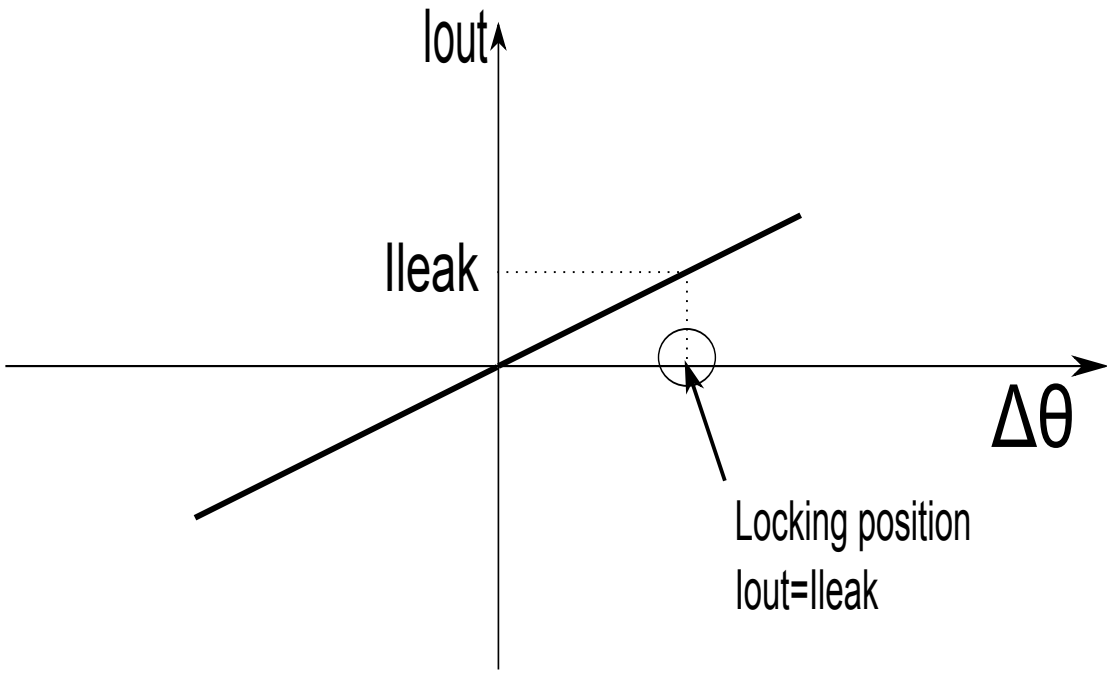

Figure 5.5: *The locking position is such that the average charge pump output current is equal to the average leakage current*

Each of the baseband modulation frequency nf_{ref} generates two spurious signals located in $f_{LO} \pm f_{ref}$ with f_{LO} carrier frequency. The ratio between the amplitude of each spurious signal A_{SP} and the magnitude of the carrier A_{LO} is:

$$\frac{A_{SP}(f_{LO} \pm nf_{ref})}{A_{LO}} = \frac{\Theta_p(nf_{ref})}{2} = \frac{I_{leak}|Z_f(j2\pi nf_{ref})|K_{VCO}}{nf_{ref}} \tag{5.7}$$

5.1.2 Mismatch in Charge Pump Current Sources

Mismatch originates in the different type of devices used to implement the N type current source which sinks current from the output node to ground and P type sources which sources current from the positive supply to the output node. Assuming the absence of the leakage currents in loop filter, phase lock occurs with a given phase difference at the input oh the PFD which results in an average output current from the charge pump of zero. This is depicted in the figure 5.6 which represents three possible locking situations for three different value of tuning voltage.
With a spectral analysis the amplitude of the spectral components $I_{OUT}(nf_{ref})$ at the fundamental and harmonics of the reference frequency f_{ref} may be found. Knowing $I_{OUT}(nf_{ref})$ the

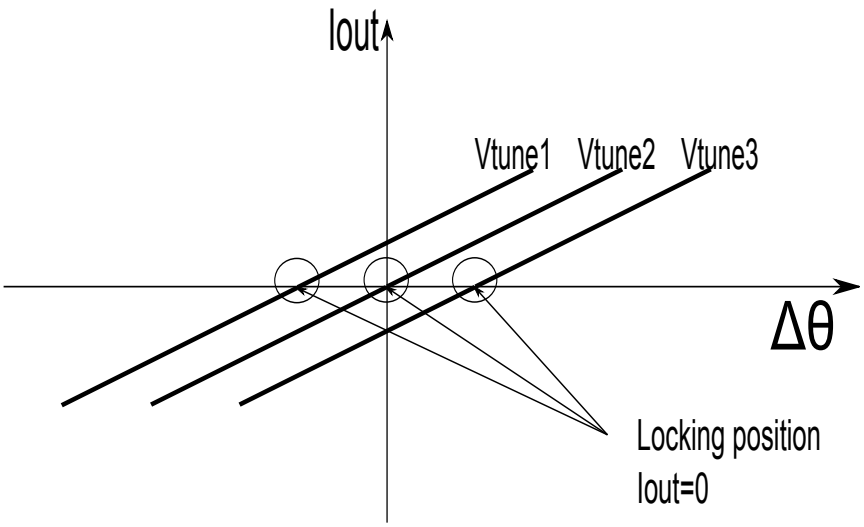

Figure 5.6: *Locking position is such that the average charge pump current is zero*

spectral components magnitude of the ripple voltage due to current sources mismatch are :

$$V_{mismatch}(nf_{ref}) = I_{OUT}(nf_{ref})|Z_f(j2\pi nf_{ref})|. \tag{5.8}$$

Using an equation similar to (5.6), the magnitude of the reference spurious breakthrough with respect to the carrier is :

$$\frac{A_{SP}(f_{LO} \pm nf_{ref})}{A_{LO}} = \frac{I_{OUT}(nf_{ref})|Z_f(j2\pi nf_{ref})|K_{VCO}}{2nf_{ref}} \tag{5.9}$$

5.1.3 Charge sharing

Another nonideality regarding on the charge pump is the phenomena called charge sharing. This problem is present between the filter capacitor and the parasitic capacitances between drain and source of switch transistors. As illustrated in Fig. 5.8 when S_1 and S_2 are off, the capacitance X can discharge itself to ground through M_1 and Y charge to V_{DD} through M_2. At the next step S_1 and S_2 turn on, so V_X rises V_Y falls and $V_X \approx V_Y \approx V_{cont}$ neglecting the voltage drop across the switch transistors. It is supposed a zero phase error, $I_{D1} = |I_{D2}|$, $C_X = C_Y$ and a V_{cont} relatively high. Well after that the switch transistor turns on, the tuning voltage does not keep constant because V_X changes by a large amount than V_Y. The difference between the two changes has to be supplied by the filter capacitor, decreasing in this way the tuning voltage.

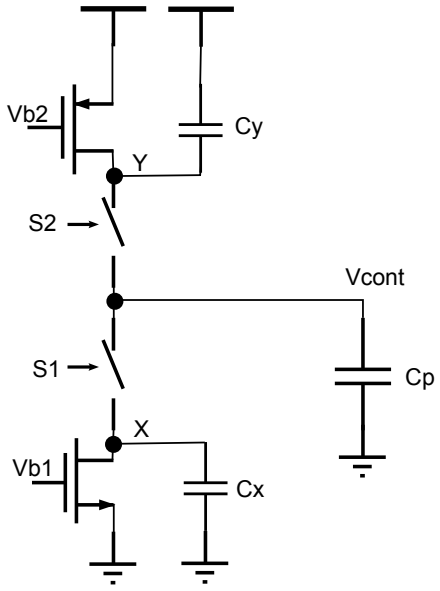

Figure 5.7: *Charge Sharing between filter capacitor and X and Y capacitances*

5.2 Noise Propagation in a PLL

Phase noise is the phase random variation of the signal. Phase noise and jitter are closely related, especially the first regards on the frequency domain, while the second regards on the time domain.

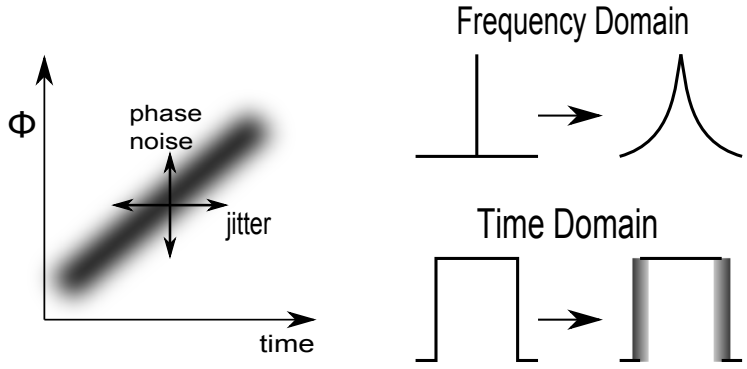

Figure 5.8: *Jitter vs. Phase Noise*

The phase noise generated by the PLL building blocks can be modeled with the help of additive noise sources, as shown in Fig. 5.9 . The rms phase noise power density of the divider, reference, phase detector and VCO are represented by $\theta_{div}(f)$, $\theta_{ref}(f)$, $\theta_{PD}(f)$ and $\theta_{VC0}(f)$, respectively. The dimension of these phase noise sources is $rad/\sqrt{Hz}$. The charge pump noise

is taken into account with noise current $i_{CP}(f)$ with dimension $A/\sqrt{Hz}$ and the noise of the loop filter components is represented by the noise voltage source $v_{LF}(f)$ with dimension $V/\sqrt{Hz}$. The rms phase noise power density of the PLL output is $\theta_O(f)$ with dimension $V/\sqrt{Hz}$, it is the sum of all noise sources modified by the action of the feedback loop on them. The output phase noise power density will be :

$$\theta_O^2(f) = \theta_{olp}^2(f) + \theta_{ohp}^2(f). \tag{5.10}$$

where $\theta_{olp}^2(f)$ is the phase noise power density generated by noise sources which are low pass filtered when transfered to the output node, and $\theta_{ohp}^2(f)$ represents the effect of the which are high pass filtered.

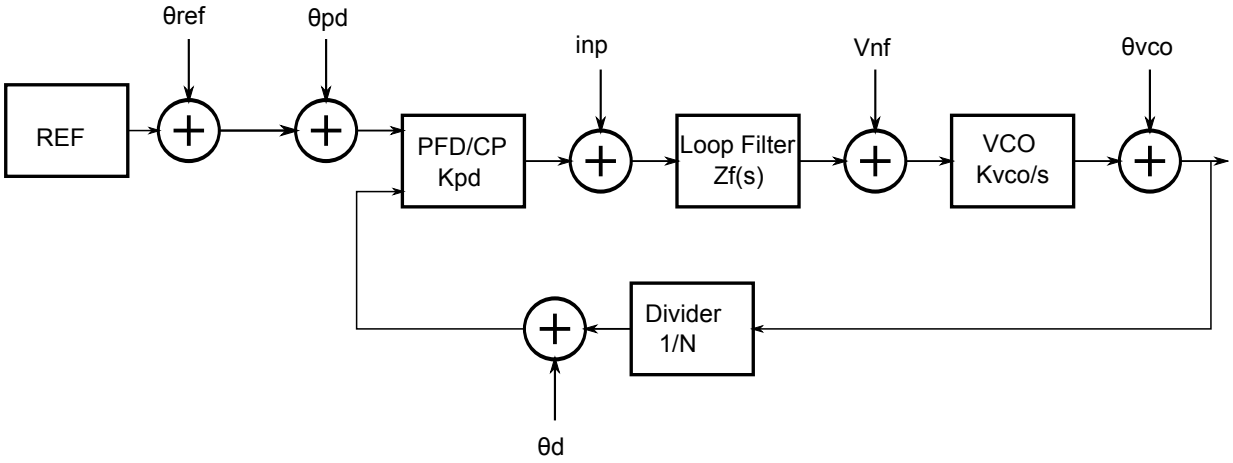

Figure 5.9: *Noise sources of the PLL*

The transfer function of the noise sources $\theta_{div}(f)$, $\theta_{ref}(f)$ and $\theta_{PD}(f)$ to the output node is the same and also using the equation (4.2), it is equal to

$$H_{LP}(s) = \frac{G(s)}{1+G(s)} = \frac{K_{PD}Z_f(s)K_{VCO}/N}{s + K_{PD}Z_f(s)K_{VCO}/N} = \tag{5.11}$$

The scaled contributors from the charge pump $i_{CP}(f)/K_{PD}$ is also subjected to the transfer function (5.11). So the low pass phase noise power component $\theta_{olp}^2(f)$ can be expressed as :

$$\theta_{olp}^2(f) = |H_{LP}(j2\pi f)|^2(\theta_{div}^2(f) + \theta_{ref}^2(f) + \theta_P^2(f) + i_{CP}^2(f)/K_{PD}^2) = |H_{LP}(j2\pi f)|^2(\theta_{eqLP}^2(f)) \tag{5.12}$$

The basic equation describing the phase noise power spectral density of an oscillator is

$$\theta_{VCO}^2(f) = \frac{1}{2}\left[1 + \frac{1}{f^2}\left(\frac{f_o}{2Q_L}\right)^2\right]\frac{FKT}{P_{avs}}\left(1 + \frac{f_c}{f}\right) \tag{5.13}$$

where Q_L is the loaded quality factor of the tuning circuit, f the carrier offset frequency, f_o the carrier center frequency, f_c the flicker corner frequency, T the temperature, P_{avs} the power of the oscillator signal, F the noise factor and K the Boltzman constant.
The noise from the loop filter $v_{LF}(f)$ is due to the resistance thermal noise. The open loop phase noise power density $\theta^2_{LF}(f)$ is related to the $v_{LF}(f)$ by the equation

$$\theta^2_{LF}(f) = v^2_{LF}(f)\frac{K^2_{VCO}}{f^2} \tag{5.14}$$

The transfer function of the noise sources $\theta^2_{LF}(f)$ and $\theta^2_{VCO}(f)$ to the output node is the same and with the help of the equation (4.2), it is equal to

$$H_{HP}(s) = \frac{1}{1+G(s)} = \frac{s}{s + K_{PD}Z_f(s)K_{VCO}/N} \tag{5.15}$$

Where the $_{HP}$ subscript expresses the high pass transfer character of $H_{HP}(s)$. So the high pass phase noise power component $\theta^2_{ohp}(f)$ can be expressed as :

$$\theta^2_{ohp}(f) = |H_{HP}(j2\pi f)|^2(\theta^2_{LF}(f) + \theta^2_{VCO}(f)) = |H_{HP}(j2\pi f)|^2(\theta^2_{eqHP}(f)) \tag{5.16}$$

Substitution (5.16) and (5.12) in (5.10) provides the following expression for the total phase noise power spectral density

$$\theta^2_O(f) = |H_{LP}(j2\pi f)|^2\theta^2_{eqLP}(f) + |H_{HP}(j2\pi f)|^2\theta^2_{eqHP}(f). \tag{5.17}$$

Chapter 6

Design of the PLL

As mentioned in the abstract, the aim of this work is designing the Phase Frequency Detector, the Charge Pump and the Loop Filter of a PLL. All these are implemented using a CMOS technology with 130 nm minimum feature size and 1.2V supply.
Before analyzing the design of each block, one must know the value of both K_{VCO} and the frequency reference input f_{ref} that is also the operational frequency of the PFD and CP.
The reference frequency is equal to $20MHz$ which is a standard frequency that can be produced by a crystal oscillator.
With the regard to the voltage controlled oscillator three working points are determined: when the input VCO voltage, is 0.3V, 0.6V and 0.9V the output VCO frequency will be 2.2GHz, 2.4GHz and 2.6GHz, respectively. Thus on the basis of the equation (1.2) the VCO gain is :

$$K_{VCO} = \frac{2.4 - 2.2}{0.6 - 0.3}\frac{GHz}{V} = \frac{2.6 - 2.4}{0.9 - 0.6}\frac{GHz}{V} = \frac{2.6 - 2.2}{0.9 - 0.3}\frac{GHz}{V} = 0.667\frac{GHz}{V} \tag{6.1}$$

Since the output PLL frequency f_{OUT} is greater than 2GHz and the reference frequency is fixed at 20MHz a feedback integer divider is necessary to have a right comparison at PFD input. In particular when the output frequency is 2.4GHz the output divider frequency must equalize the reference frequency. Hence the ratio of the feedback divider must be

$$N = \frac{f_{OUT}}{f_{ref}} = \frac{2.4GHz}{20MHz} = 120. \tag{6.2}$$

6.1 Loop Filter Design

As described in the Gardner paper[4] the expression that gives the stability limit of a third order type II PLL is:

$$K\tau_2 = \frac{4(1+a)}{\frac{2\pi(b-1)}{b\omega_{ref}\tau_2}\left[\frac{2\pi(1+a)}{\omega_{ref}\tau_2} + \frac{2(1-a)(b-1)}{b}\right]}. \tag{6.3}$$

where K , τ_2 and b are given in (4.1) and $a = exp(-\frac{2\pi b}{\omega_{ref}\tau_2})$.

The substitution of (4.8) and of (4.11) in (6.3) gives the maximum values of the open loop bandwidth ω_c (4.10) as function of $\omega_{ref} = 2\pi f_{ref}$,$b$ and $a = exp(-\frac{2\pi\sqrt{b}\omega_c}{\omega_{ref}})$.

$$\frac{\omega_c}{\omega_{ref}} = \frac{4(1+a)}{\frac{4\pi^2(1+a)\omega_c}{\sqrt{b}\omega_{ref}} + \frac{4\pi(1-a)(b-1)}{b}}. \tag{6.4}$$

Usually this relationship is satisfied if $\frac{\omega_c}{\omega_{ref}} < 10$. However in practice a rule of thumb is $\frac{\omega_c}{\omega_{ref}} < 15$.
So I have fixed f_c at a value equals to $f_c = f_{ref}/17$. Figure 4.5 shows the relationship between b and the phase margin. With $b = 15$ there is a phase margin slightly greater than 60. Since this is a good value I have used $b = 15$.
At this point the only unknown factor to calculate the values of the three loop filter components is the I_{CP}, i.e. the UP and DOWN charge pump currents. The main purpose of this work is obtaining a low power consumption by using low current sources. The best trade off between current consumption and the technology used is $I_{CP} = 40\mu A$ as it will be shown later. With this current value and the equations (4.11),(4.12),(4.13) the components values are found :

$$R_1 = 222.5K\Omega$$
$$C_1 = 2.338pF$$
$$C_2 = 0.159pF$$

If the $I_{CP} = 40\mu A$ is further reduced the transistors in the CP could subthreshold region work in reducing more I_{CP},thus risking the right charge pump working. Moreover a further reduction in the charge pump current would make the resistance value increase but the value of the resistor is already high. Since the maximum value of a resistor for this technology can be $R_{MAX} = 44.45K\Omega$, I have used a series of five R_{MAX} and no more to implement R_1.

6.2 PFD Design

In order to decide which kind of Phase Frequency Detector to implement in the whole PLL two main parameters are used: low power consumption and robustness to the rising and falling edges of PFD inputs. To understand the type of PFD to be used, among those listed in second chapter, I have made several simulations, using the circuit in Fig. 6.1.

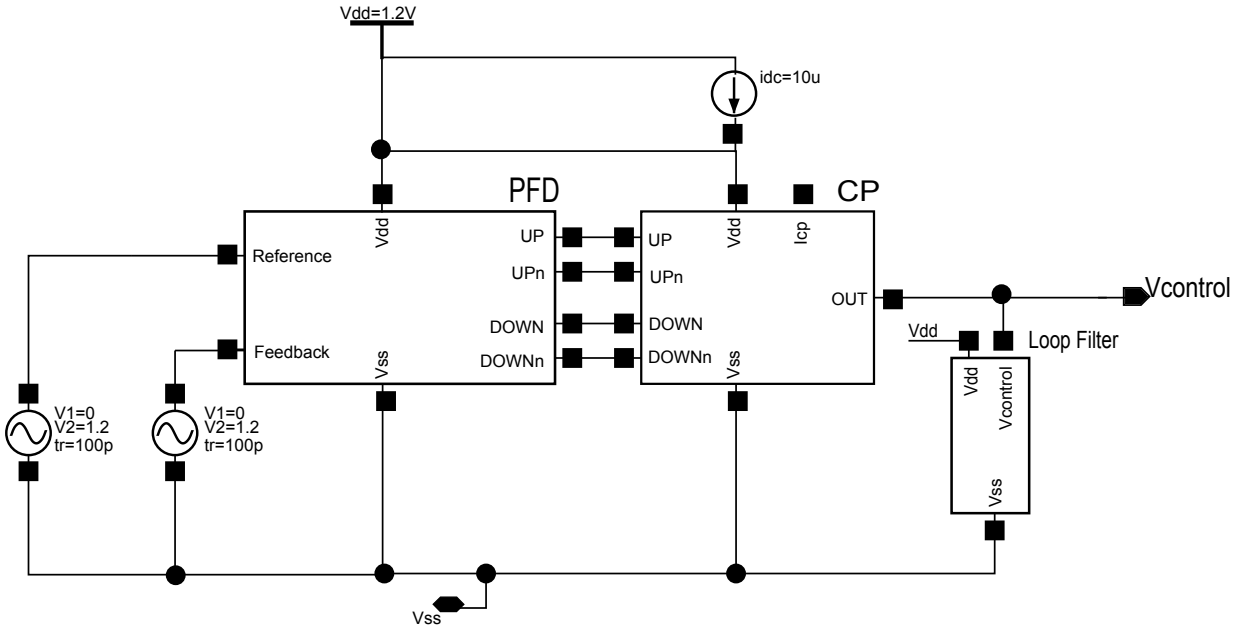

Figure 6.1: *Proof Circuit to simulate PFD and CP working*

The figures 6.3, 6.5 and 6.6 show the schematics of the three PFD checked in this work the PFD made with DFF in CMOS technology, the PFD made with FDD in TSPC technology and the PFD made with SR latches and monostable circuits, respectively. Each of these represents the insider of the block called PFD in fig 6.1. Inside the three PFD above pMOS and nMOS transistors have the same dimensions: channel length $l = 120nm$, channel width $w = 2\mu m$ with a finger.

The figures 6.2 and 6.4 show the schematics of the DFFs illustrated in the figures 6.3 and 6.5. The first one is the same of that in fig. 2.2 whereas the second one copies the schematic shown in fig. 2.4 with the addition of an inverter so that it has a direct output together with a denied one. In Fig. 6.6 every SR latch is implemented with two cross coupled NAND gates. The inverter chain inverts the monostable input and creates a delay path in every monostable placed before each SR latch. This inverter chain has been implemented with seven inverters, because the use of one or three inverter gates leads a too brief output pulse width. Especially with one inverter

the output does not reaches the low logic level. With five inverter gates the ability of the whole phase frequency detector to respond correctly to the rising edges is far comparable with that of the PFD shows in Fig. 6.3.

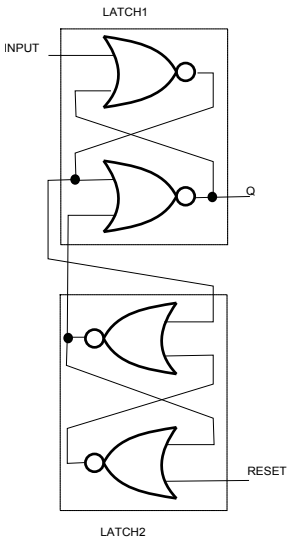

Figure 6.2: *DFF in CMOS technology*

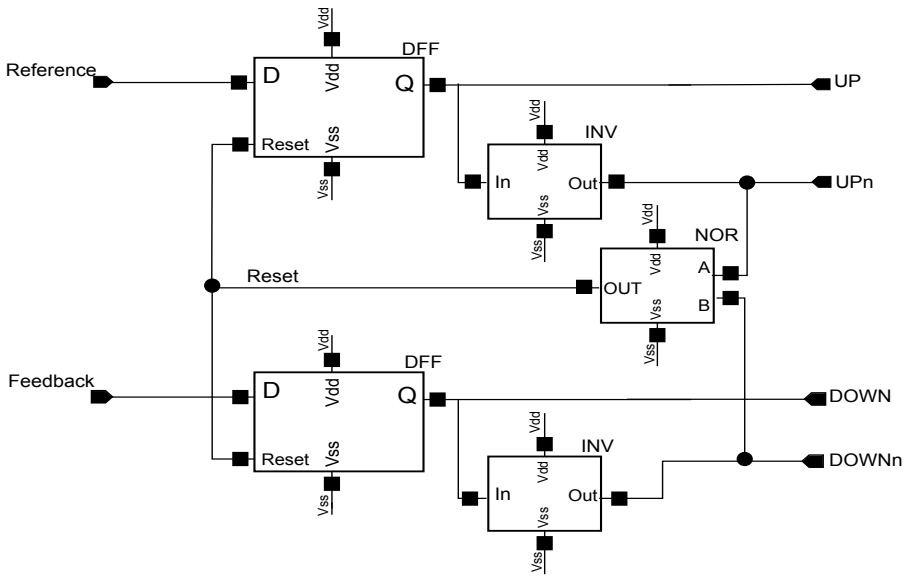

Figure 6.3: *PFD made with DFF in CMOS technology*

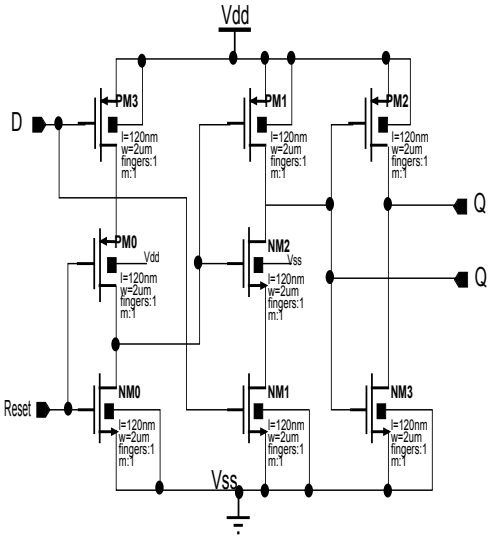

Figure 6.4: *DFF in TSPC logic*

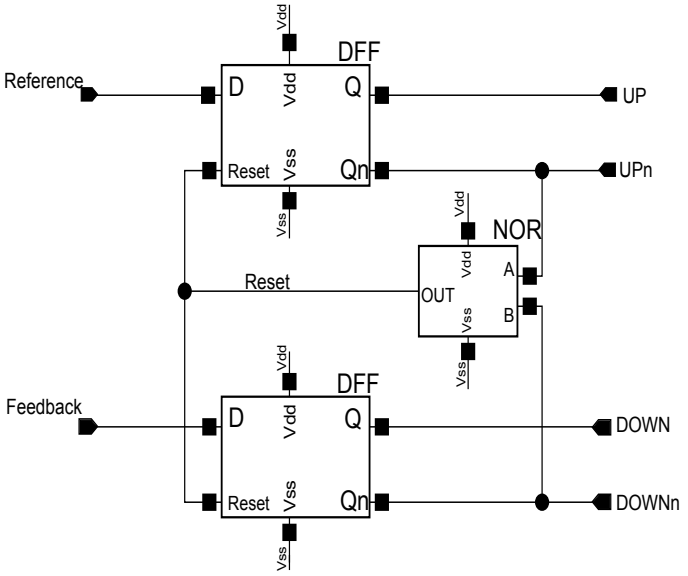

Figure 6.5: *PFD with DFF in technology TSPC*

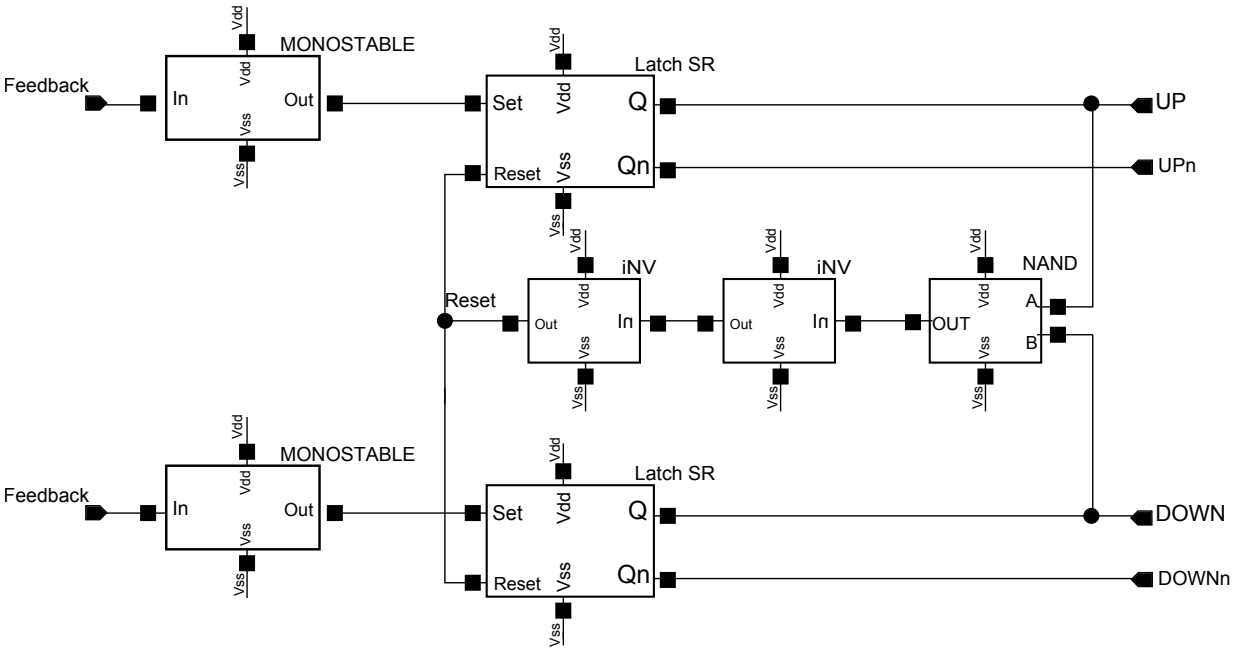

Figure 6.6: *PFD made with monostables and latches SR*

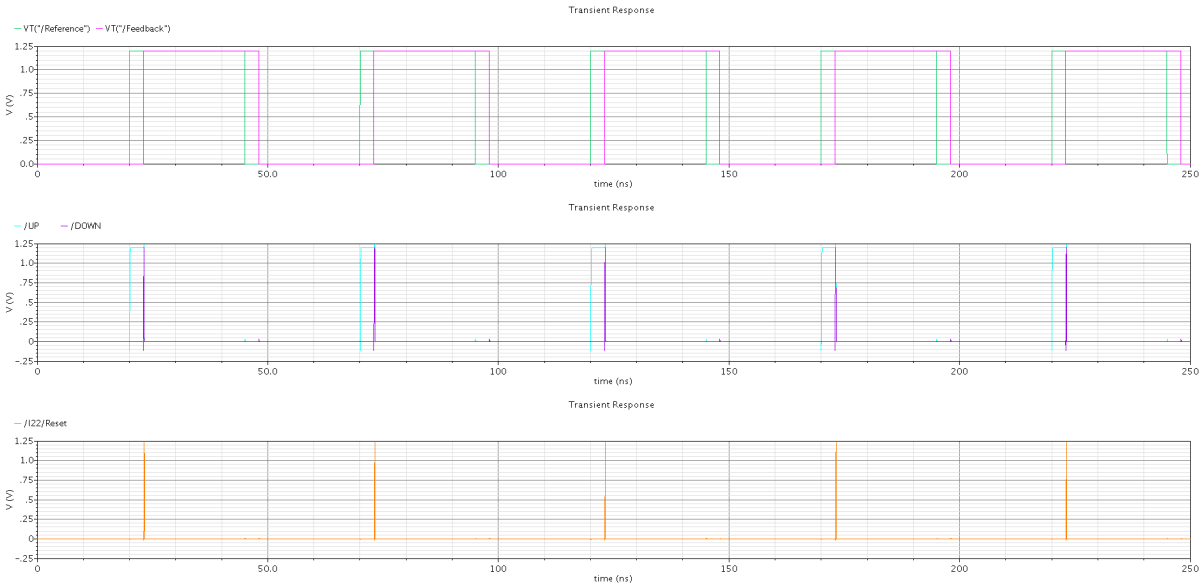

Figure 6.7: *Inputs, Outputs, Reset signals of PFD in Fig. 6.3*

For PFD made with DFF in CMOS technology and PFD made with SR latches the figures 6.7 and 6.8 illustrate input,output and reset signals when both circuit inputs have rising and falling times equal to $10ns$. The two generators in figure 6.1 represent the reference and the feedback signals. They have a frequency of $20MHz$ and the reference leads the feedback by $5ns$. These signals are not illustrated for the PFD with DFF in TSPC technology since in this work condition are substantially identical to the signals in figure 6.7.

Figure 6.7 is the virtually case already illustrated in Fig 1.6 and 2.1. The two input have the same frequency but one (the reference, the green waveform) leads the other by $5ns$(the feedback, the fuchsia waveform). The reference goes high, it propagates through the DFF hence the output UP(the blue waveform) goes high and the denied output UPn goes low. After $5ns$ also the feedback goes high, it propagates through the DFF hence the output DOWN(the purple waveform) goes high and its denied DOWNn goes low. In this moment the two denied outputs are low, they propagates through the NOR gate causing its output i.e. the Reset(orange waveform) to go high. The reset propagates through DFFs, whose output goes low, whereas denied output goes high, therefore the reset comes back low. In Fig. 6.7 five of the cycles just described are illustrated. In the figure 6.8 the same work conditions of fig. 6.7 are set. The two inputs are the reference (green waveform)and the feedback (fuchsia waveform). When there is a rising edge at the input the output of the monostable circuits shows a brief pulse high-low-high (red waveform in the second graph of fig. 6.8 is the output of the monostable driven by the reference, while the blue one is the output of the monostable driven by the reference). The monostable outputs are

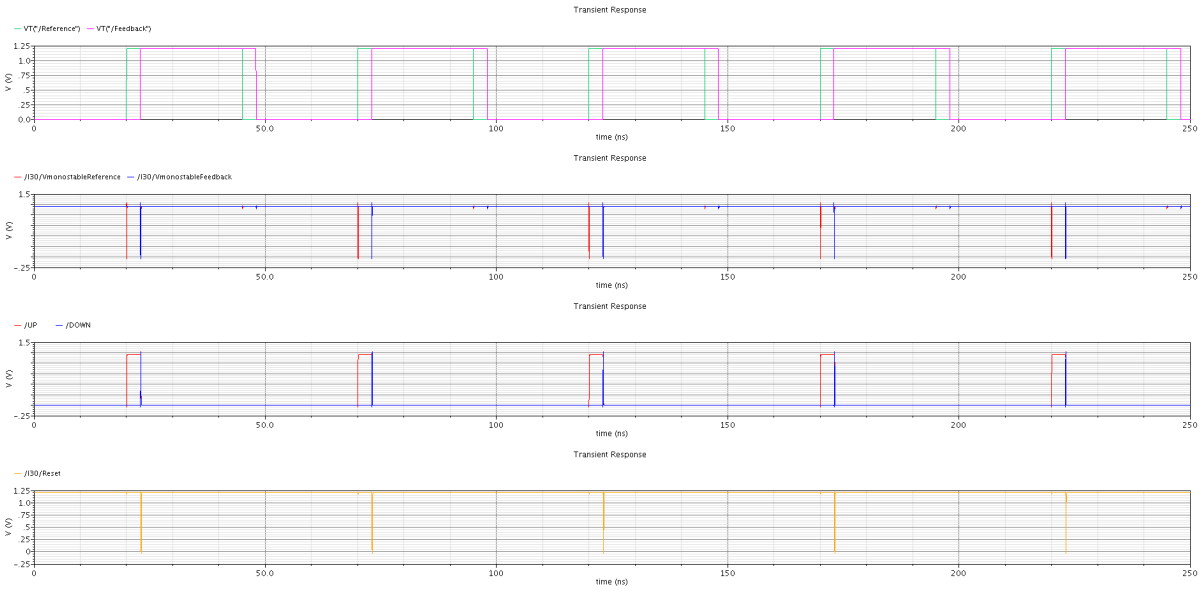

Figure 6.8: *Inputs,Outputs,Reset signals of PFD in Fig. 6.6 and output signals of the two monostable*

connected to the set inputs of the two SR latches, when a high-low-high pulse occurs at the set input the output latch(red waveform for the upper SR latch and blue waveform for the downer SR latch in the third graph of fig. 6.8) switches to a logic high value which is kept until the reset comes back to zero. The reset is the output signal of the cascode of the NAND gate and the two inverters. Only when the NAND gate inputs logic value are both high, the reset is at the low logic state. Consequently the two SR latches outputs go low, they propagate through the NAND and the two inverter gates bringing back the reset to the high state.

The robustness of the three PFD to the rising and falling edges is now being tested using the simulator. The rise and fall time of the two generators in Fig. 6.1 are modified until the operation of the circuit is no longer correct. These generators have a frequency of $20MHz$ and the reference leads by $5ns$ the feedback.

The fig. 6.9 depicts the results of the simulations on the PFD made with DFF in TSPC logic. In the first graph there are the input signals of the PFD: the waveforms represent the reference signal (the green one) and the feedback signal (the fuchsia one), both having a $t_{rise} = t_{fall} = 100ps$. The UP signal(red waveform) and DOWN signal(blue waveform) generated when the inputs have $t_{rise} = t_{fall} = 100ps$ are shown in the second graph of fig. 6.9. The third graph shows again the PFD input signals,but now both having $t_{rise} = t_{fall} = 500ps$. The waveforms represent the reference signal (the green one) and the feedback signal (the fuchsia one). The fourth graph of fig. 6.9 illustrates the PFD outputs the UP(red waveform) and DOWN signal(blue waveform)

generated by the signals in the third graph of fig. 6.9.
In fig. 6.10 there are the results of the simulations on the PFD made using SR latches and monostable. The first graph shows the input signals of the PFD: the reference signal (the green one) and the feedback signal (the fuchsia one), they have a $t_{rise} = t_{fall} = 2.5ns$. The second graph of fig. 6.10 shows the UP signal(red waveform) and the DOWN signal(blue waveform) when the signals have $t_{rise} = t_{fall} = 2.5ns$ at the inputs. The reference signal(the green one) and the feedback signal(the fuchsia one) are shown in the third graph, but in this simulation they have $t_{rise} = t_{fall} = 3.5ns$. In the fourth graph of fig. 6.10 the PFD outputs are illustrated: the UP(red waveform) and the DOWN (blue waveform) when $t_{rise} = t_{fall} = 3.5ns$ at the inputs.
The simulation results on the PFD made with DFF in CMOS logic are shown in the fig. 6.11. In the first graph there are the input signals: the waveforms represent the reference signal (the green one) and the feedback signal (the fuchsia one), both having a $t_{rise} = t_{fall} = 5ns$. In the second graph of fig. 6.9 the PFD outputs are represented: the UP(red waveform) and the DOWN (blue waveform). In the third graph there is the reset signal of the PFD. As expected the UP, DOWN and the Reset signals are identical to those in the fig. 6.7 but slightly late due to the higher rise and fall times (5ns vs 10 ps).

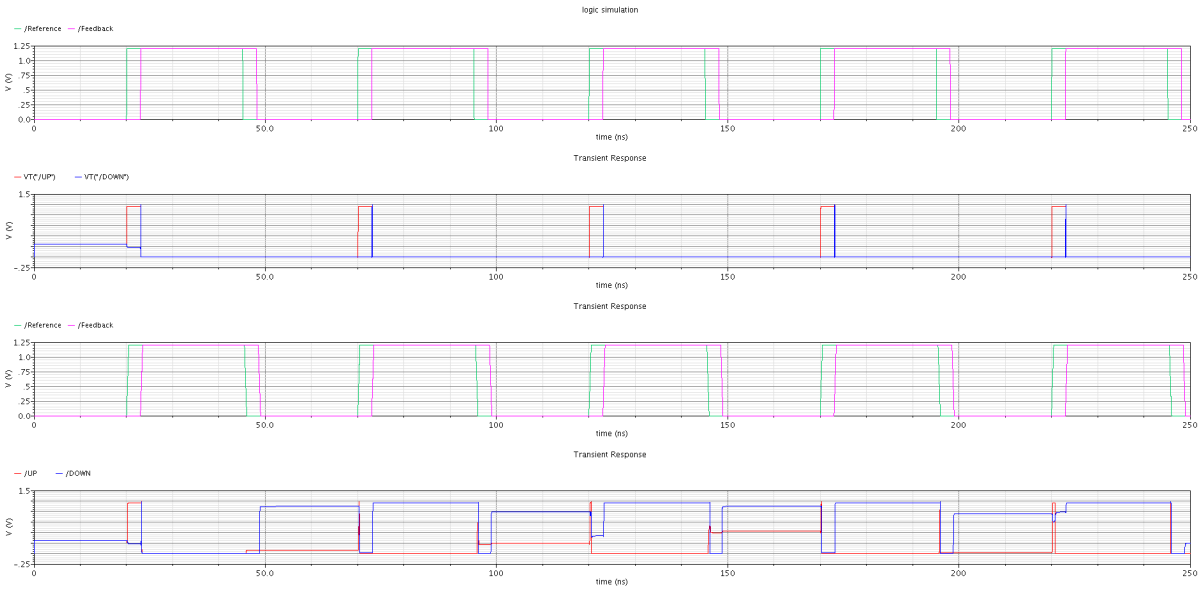

Figure 6.9: *Inputs and Outputs in PFD made with DFF in TSPC logic for t_{rise} and t_{fall} both equal to 100ps and 500ps*

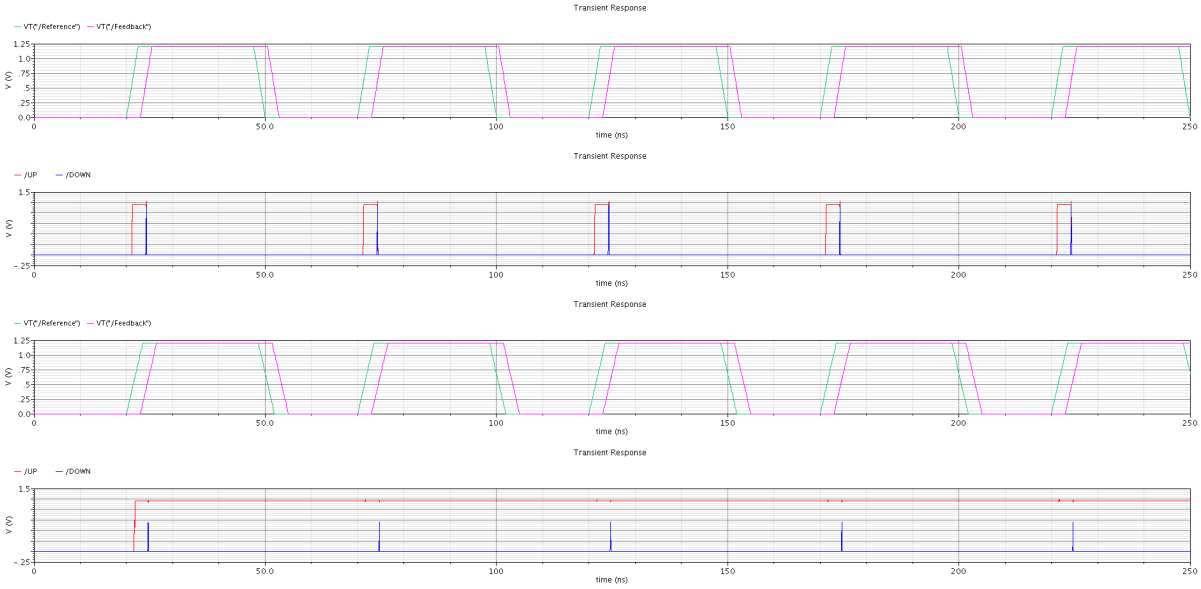

Figure 6.10: *Inputs and Outputs in PFD made with latchSR for t_{rise} and t_{fall} both equal to 2.5ns and 3.5s*

x

As the three figures above show there is already a wrong behavior of the PFD made with TSPC DFF for for t_{rise} and t_{fall} equal to $500ps$. Instead the PFD made with SR latches starts having wrong outputs with $t_{rise} = t_{fall} = 3.5ns$, while the PFD made with DFF in CMOS technology has still a right working for $t_{rise} = t_{fall} = 5ns$.
At this point the power consumption has been checked, using the current absorbed by the PFD from the voltage source. In particular I have made a transient simulation using the schematic in Figure 6.14. This schematic depicts the whole PLL circuit. In addition to the fig. 6.1 there are also the VCO and the Divider block located in the feedback path. Therefore to make a simulation in this circuit the feedback generator is not necessary, since the output signal of the Divider block is the feedback signal.

Fig. 6.12 shows the three currents waveforms absorbed by three types of PFDs implemented, when the reference signal has a frequency of $20MHz$ and $t_{rise} = t_{fall} = 100ps$. With the average function provided by the calculator tool of Analog Design Environment(ADE),the following average current absorbed values are found:

- $Iav_{latchSR} = 7.317\mu A$
- $Iav_{DFFTSPC} = 6.596\mu A$
- $Iav_{DFFCMOS} = 4.796\mu A$

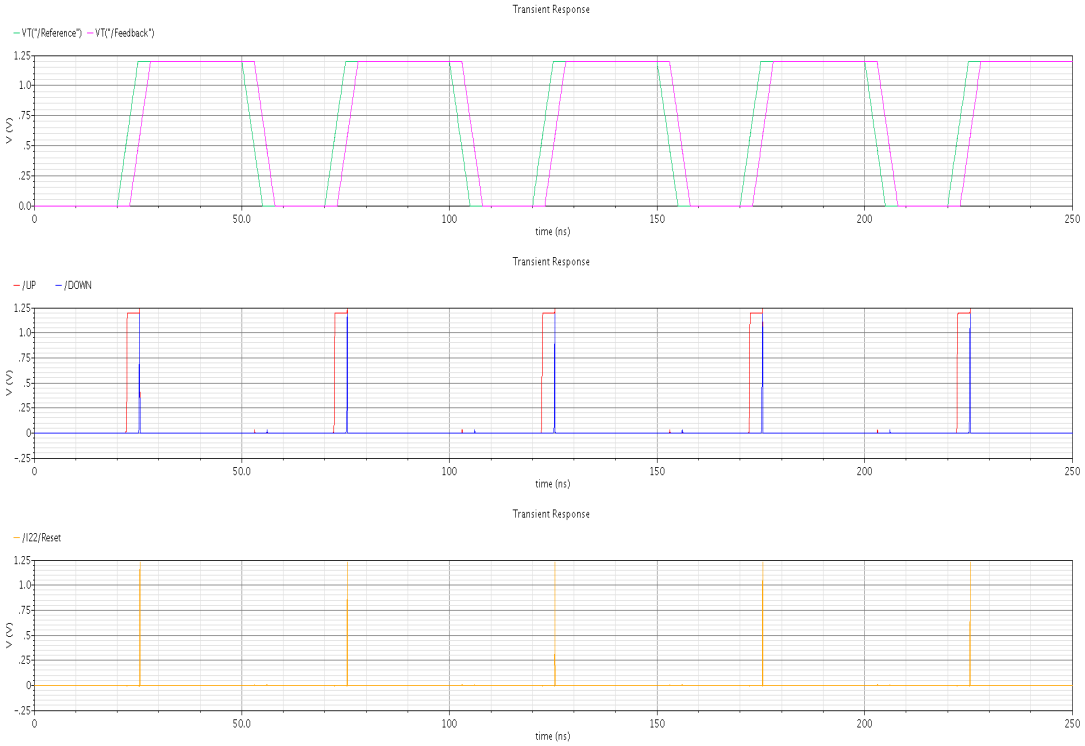

Figure 6.11: *Inputs and Outputs in PFD made with DFF in CMOS logic for* t_{rise} *and* t_{fall} *equal to 5ns*

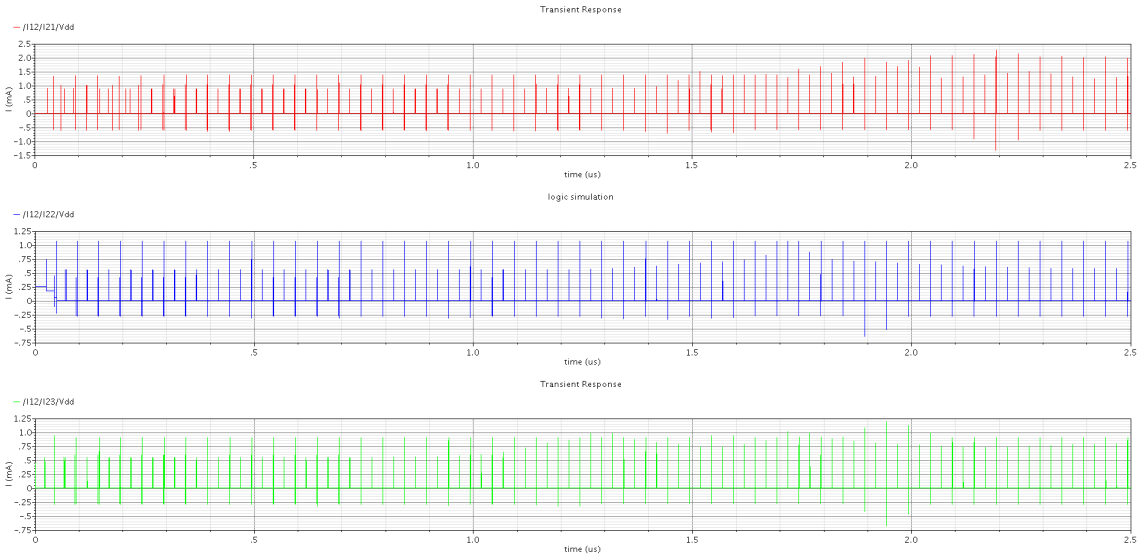

Figure 6.12: *Current absorbed by PFDS from Voltage Sources. Red line PFD with latch SR, Blue line PFD with DFF in TSPC logic, Green line PFD with PFD in CMOS logic*

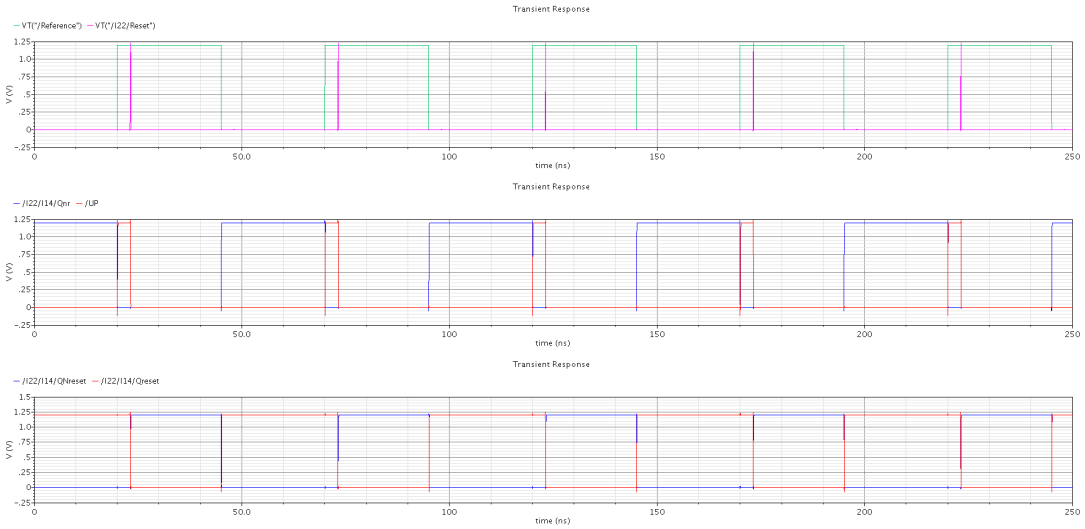

Figure 6.13: *Voltage Waveforms in the upper DFF(Fig. 6.2) of Fig. 6.3 , when the PFD inputs signals are the same of theFig. 6.7*

Hence the current absorbed by PFD made with CMOS DFF is the lowest one. This kind of PFD is also the most robust. For these two reasons this is the PFD used in this work.
The schematic of figure 6.3 can be seen that the DFF has only one direct output and not denied one. As it is shown in Fig. 6.13(obtained with a reference and feedback of $20MHz$ that are out of phase by $5ns$), for brief period times the outputs of the upper SR latch placed in the upper DFF are contemporary low(the direct latch output is the red waveform in the second graph, while the denied latch output is the blue one). This happens because the latch SR is in the forbidden state and in this situation only the direct output contains the right information. Finally the fig. 6.3 illustrates the direct output(red waveform) and the denied output(blue waveform) of the downer latch SR placed in the upper DFF in CMOS technology.

In the three figures(Fig. 6.15, 6.16, 6.17) some signals of the PLL(Schematic Fig. 6.14) are illustrated. The PLL is made with the three different PFDs considered and with the charge pump block illustrated in fig. 6.18. In the next three figures the reference is the green waveform and it is created by a generator at a frequency of $20MHz$ and $t_{rise} = t_{fall} = 100ps$, the feedback signal is the fuchsia waveform, the UP signal is the red waveform, the DOWN signal is the blue waveform and the tuning voltage is the orange waveform. In these simulations the PLL is going to lock its output. In fact at the beginning of each simulation the reference and the feedback are out of phase and have different frequencies and the tuning voltages(Vcontrol) oscillates considerably. Instead when the lock is reached the feedback signal and the reference signal are superimposed, the UP and DOWN signals are overlapped and the tuning voltage is roughly constant at around

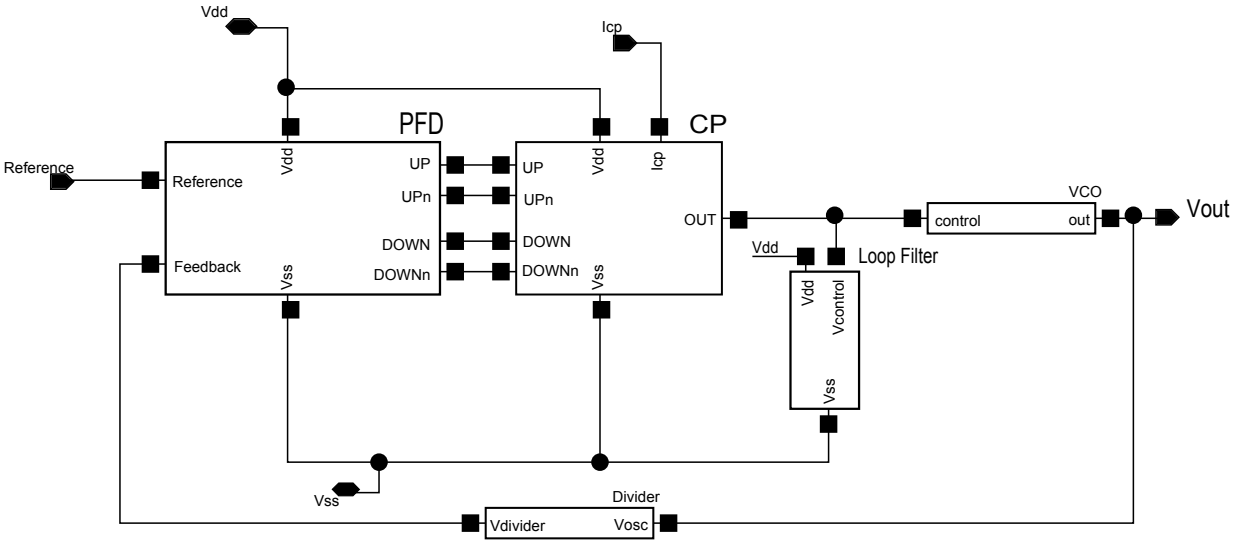

Figure 6.14: *Whole PLL schematic*

$0.6V$ with a small ripple.In these three cases the tuning voltage waveforms are similar to each other, although in Fig. 6.15(PFD with DFF in TSPC technology) the locking is the fastest one because of the TSPC technology is the fastest technology used in this work. At the frequency $f_{ref} = 20MHz$ the performances of the three blocks PFD+CP are close, although the lowest current consumption and the highest robustness to rising and falling edges occur in the PFD made with DFF CMOS.

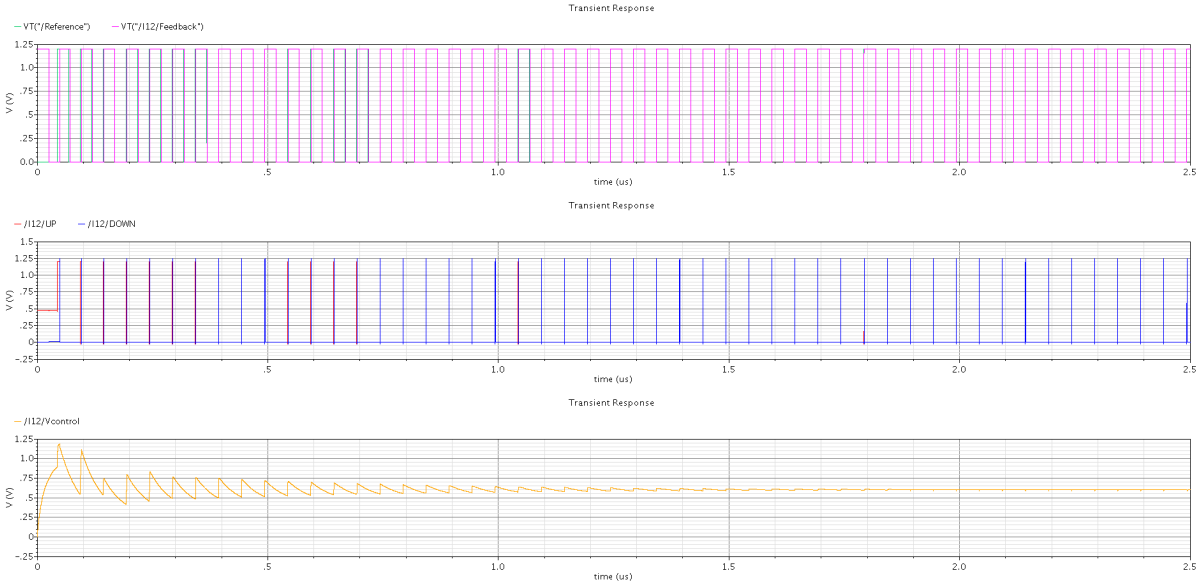

Figure 6.15: *Reference, Output Divider , Up , Down and Vtuning signals of the PLL with a PFD made with DFF TSPC*

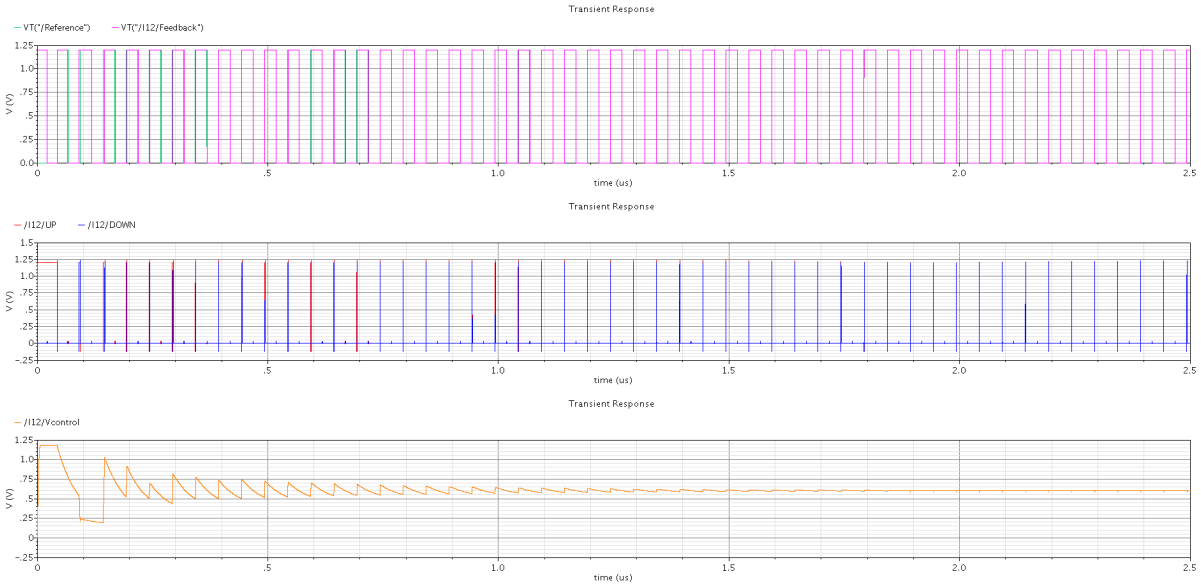

Figure 6.16: *Reference, Output Divider , Up , Down and Vtuning signals of the PLL with a PFD made with DFF CMOS*

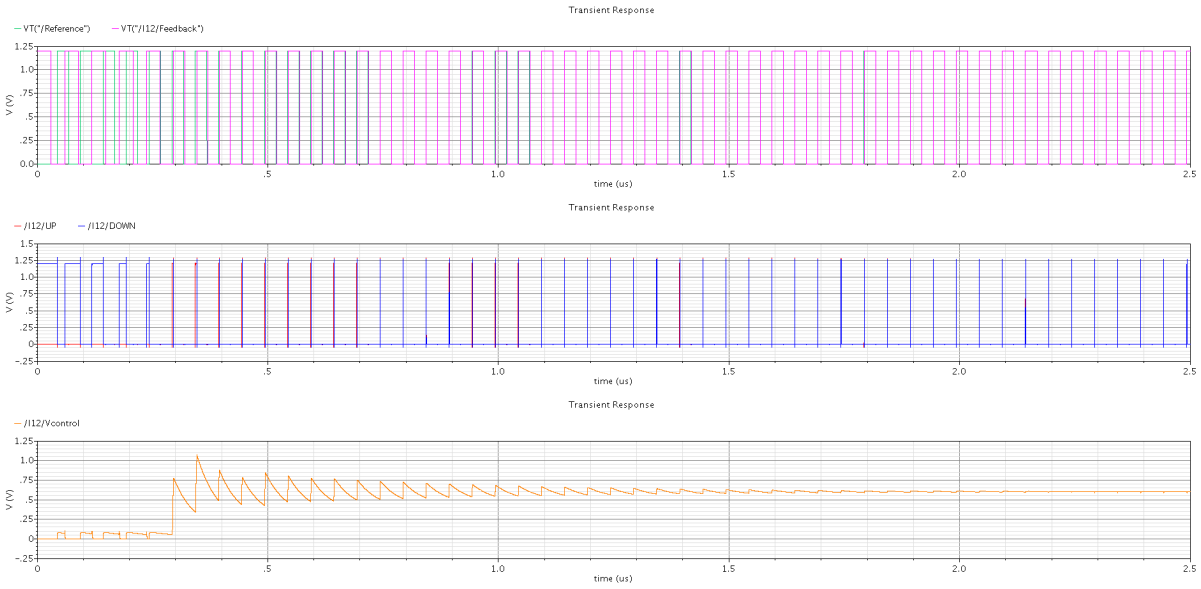

Figure 6.17: *Reference, Output Divider , Up , Down and Vtuning signals of the PLL with a PFD with latches SR*

6.3 Charge Pump Design

In this chapter some different Charge Pump configurations are treated. The circuits presented in Figure 3.1(a), 3.1(b), 3.1(c) were not considered as they have some problems such as charge sharing or low speed. Moreover performance of the circuits presented in Figure 3.2(a), 3.2(b), 3.2(c) are improved by using some variations [6]. The CP in Fig 3.2(a) has an active amplifier so that without simulations it is clear that this circuit has a greater current consumption respect to CP in Fig. 3.2(b) or 3.2(c). With regards to the cascode CP illustrated Fig. 3.3 it can not be implemented in this work due to the low voltage source(1.2 V). Both the Charge Pumps working in Fig. 3.2(b) and 3.2(c) inside the proof circuit (Fig. 6.1) and the whole circuit (Fig. 6.14) were tested. The schematics of the current steering CP(Fig. 3.2(b)) and of the CP with only nMOS(Fig. 3.2(c)) are depicted in figures 6.19 and 6.18, respectively. In order to understand how these Charge Pumps work in the proof circuit (fig. 6.1) their voltages and the currents waveforms are illustrated in the figures 6.20, 6.21, 6.22 and 6.23 when the reference and feedback signals of the fig. 6.1 have the same frequency $f_{ref} = 20MHz$, $t_{rise} = t_{fall} = 100ps$ and the reference leads the feedback by $5ns$.

In fig. 6.20 depicts the voltages at different nodes of the CP made with only nMOS. In the first graph of this figure there are the reference signal(green waveform) and the feedback signal(fuchsia waveform), in the second graph there are the UP and DOWN signals(respectively the

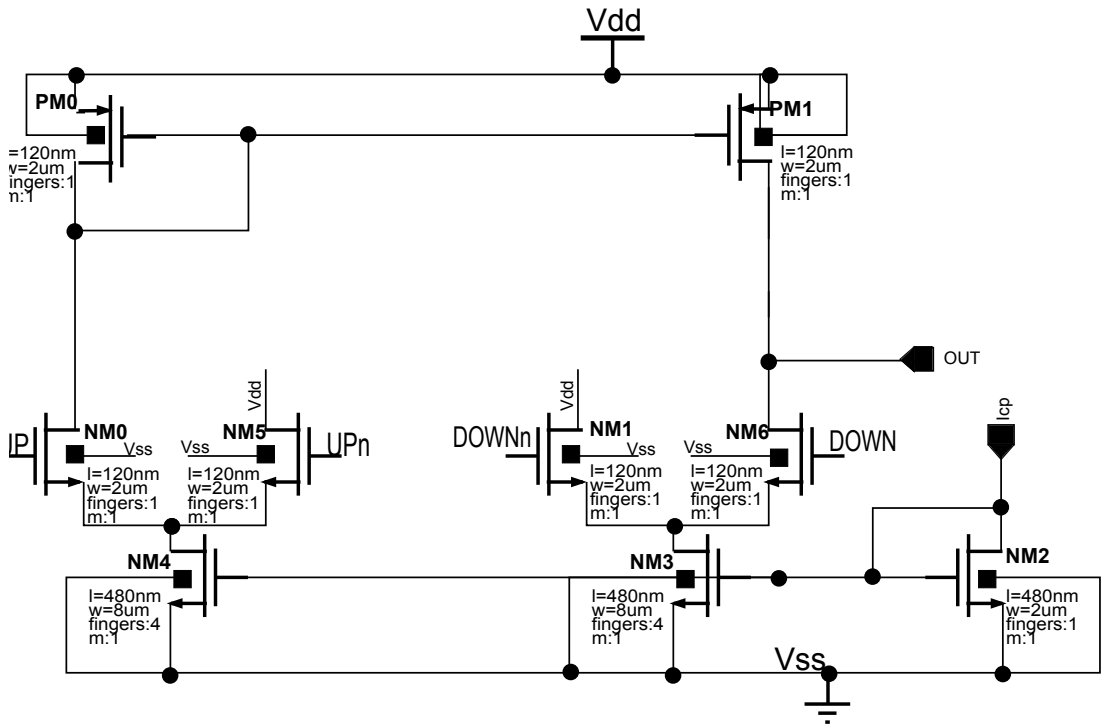

Figure 6.18: *CP made with only nMOS*

red and blue waveforms) produced by the PFD and finally in the third graph there is the tuning voltage (orange waveform), i.e. the voltage at the output of the charge pump. Figure 6.21 is obtained in the same way of the previous figure and contains the same waveforms of fig. 6.20 but using a current steering CP. Figures 6.22 and 6.23 show the currents at different branches of the CP with only nMOS and current steering CP, respectively. In the first graph of each figure the UP(red waveform) and DOWN(blue waveform) signals are reported.

With regard to the figure 6.22 the second graph shows the currents through the MOS NM6 of fig. 6.18 (blue waveform) and MOS NM0 (red waveform), whereas the third graph illustrates the currents of the current mirrors that flow through the MOS NM3 again in fig. 6.18(blue waveform) and MOS NM4 (red waveform). Finally the fourth graph of fig. 6.22 shows the output CP current.

With concern to the figure 6.23 the second graph shows the currents that flow through the transistor whose drains are connected to the CP output, i.e. MOS NM2 of fig. 6.19(blue waveform) and MOS PM2(red waveform). In the third graph there are the currents of the current mirrors that flow through the MOS NM3 again in fig. 6.19(blue waveform) and MOS PM3 (red waveform). Finally the fourth graph of fig. 6.23 shows the output CP current.

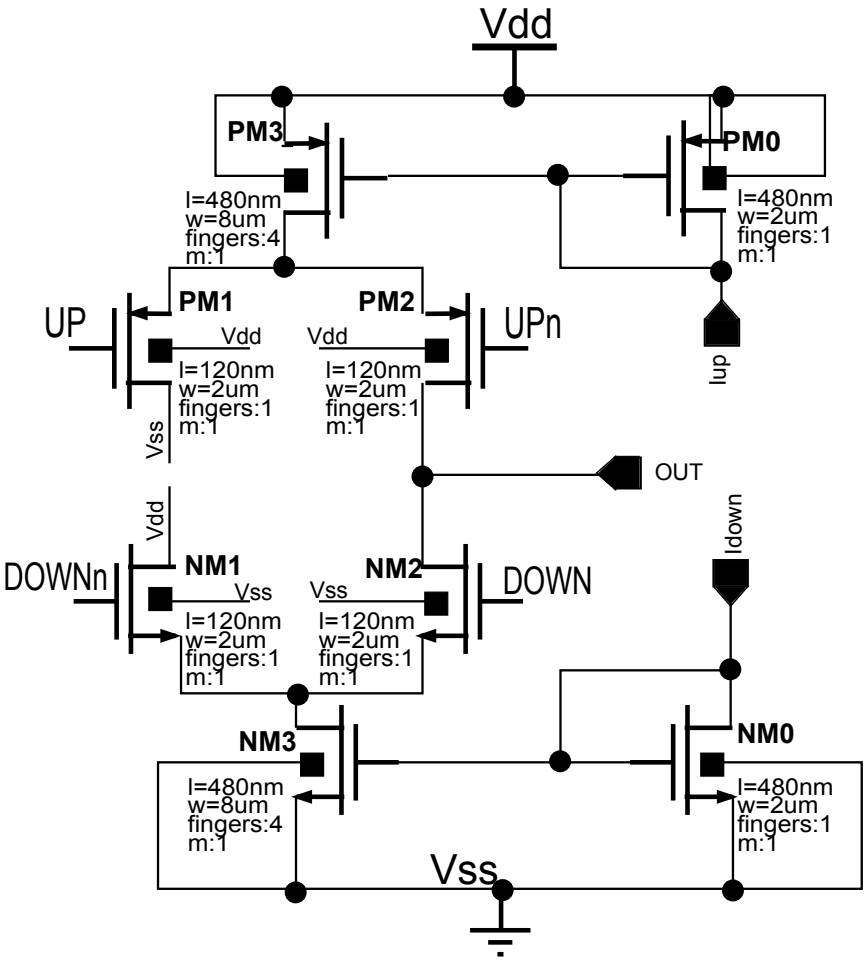

Figure 6.19: *Current Steering CP*

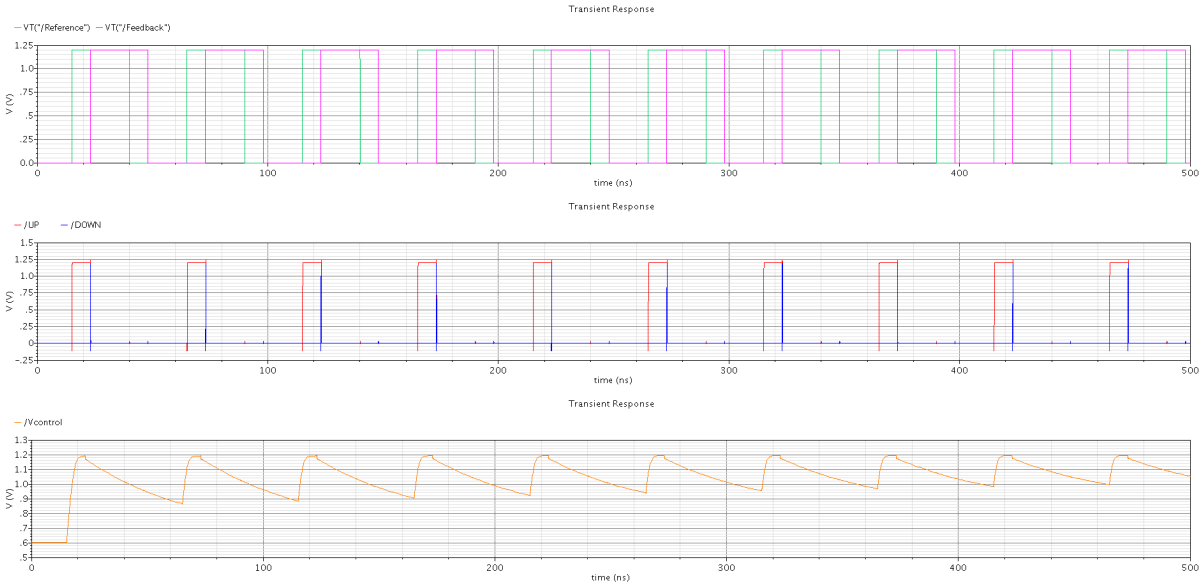

Figure 6.20: *Voltage waveforms at different nodes of the CP made with only nMOS(Fig. 6.18)*

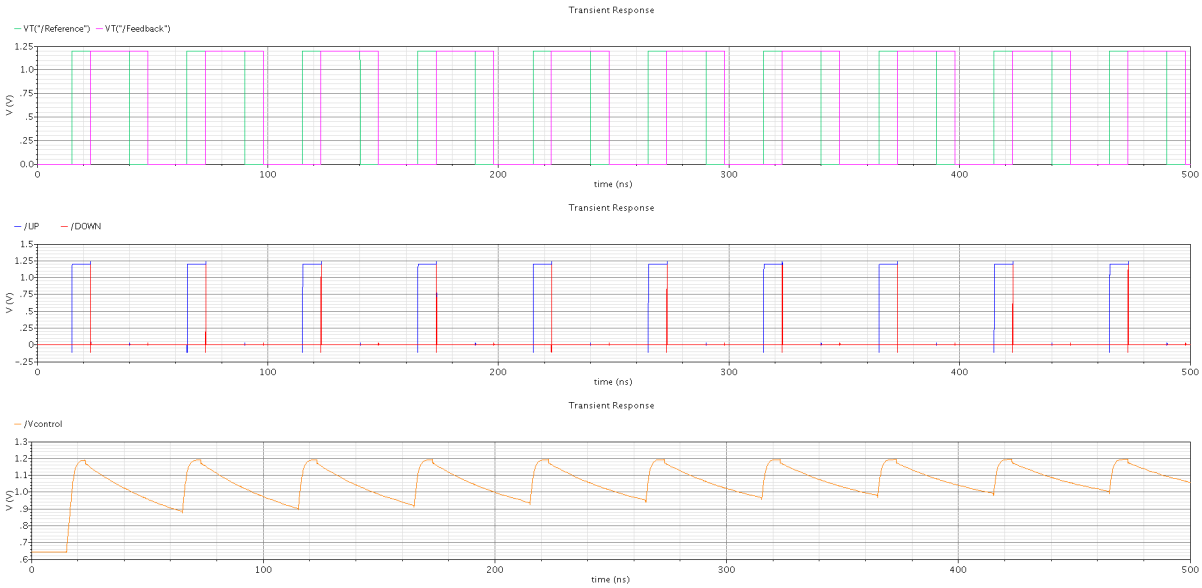

Figure 6.21: *Voltage waveforms at different nodes of the current steering CP(Fig. 6.19)*

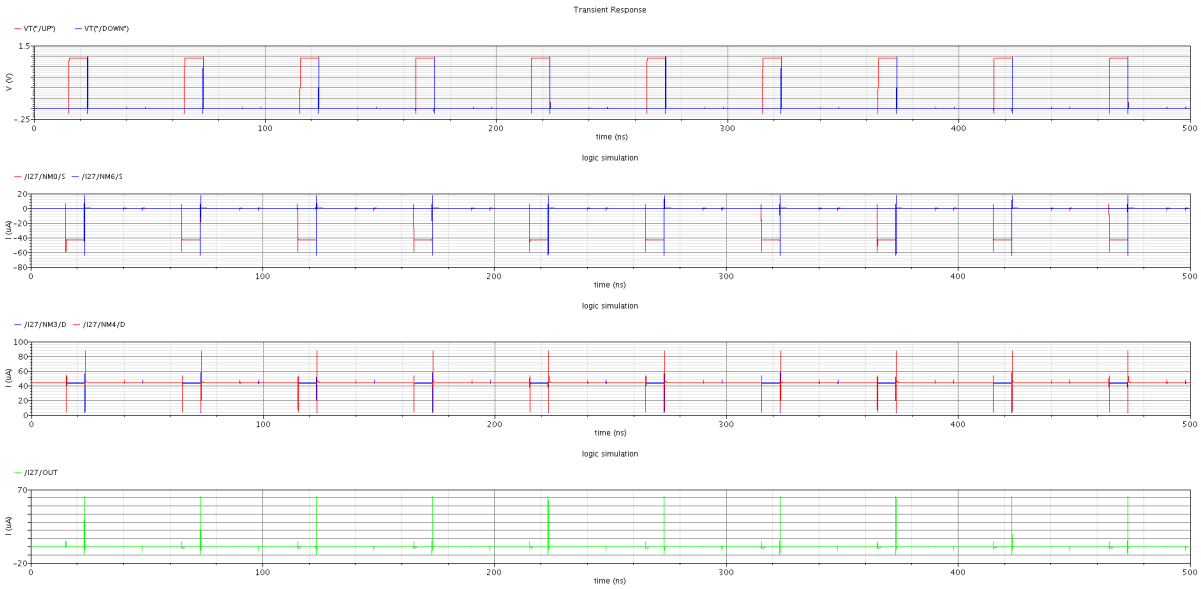

Figure 6.22: *Current waveforms at different nodes of the CP made with only nMOS(Fig. 6.18)*

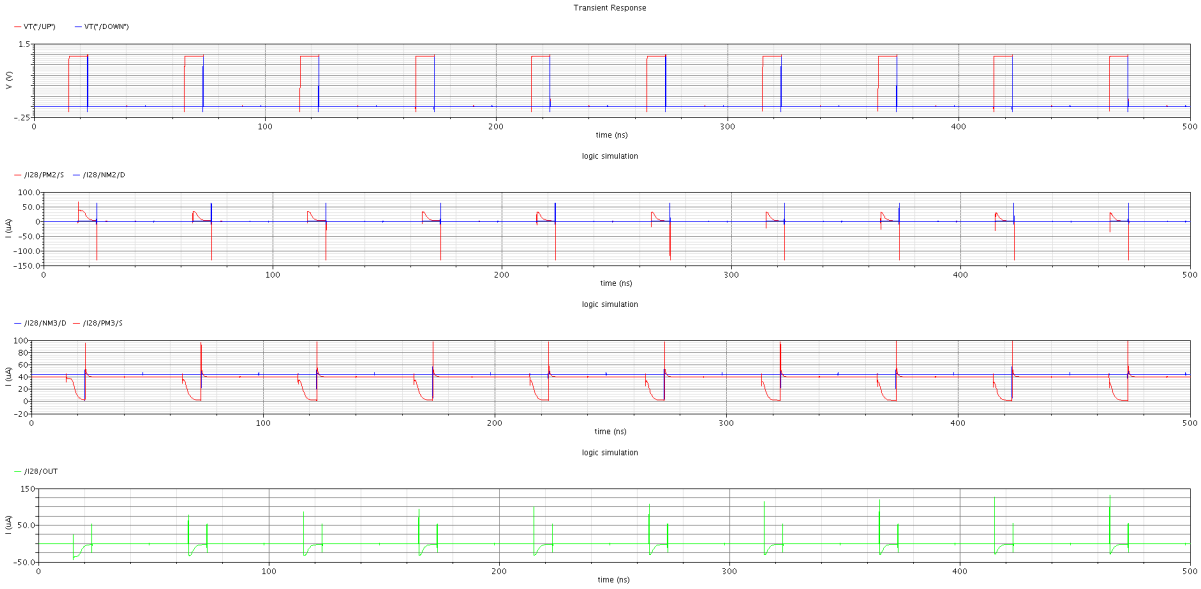

Figure 6.23: *Current waveforms at different nodes of the current steering CP(Fig. 6.19)*

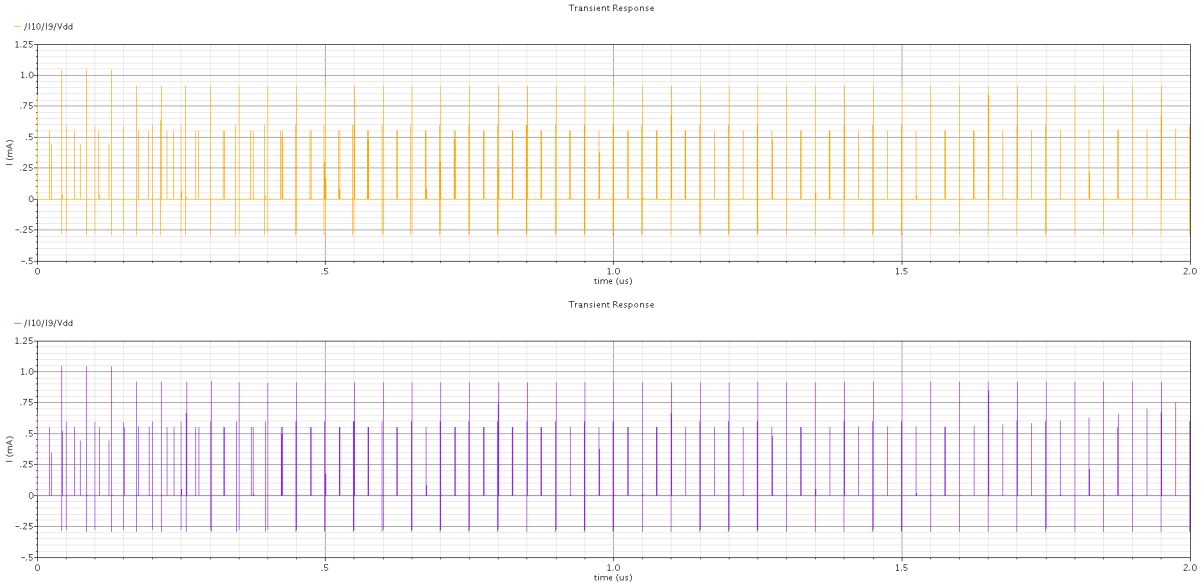

Figure 6.24: *Current absorbed by CPs from Voltage Sources. Orange line refers to CP made with only nMOS Purple line refers to current steering CP*

Comparing the current waveforms in Fig. 6.22 (only nMOS CP) and in Fig. 6.23(current steering CP) we can see that during the transient, the current peaks reaches in the current steering CP are greater than in the CP made with nMOS only. Whereas comparing the voltage waveforms of Fig. 6.20 and Fig. 6.21 the differences are negligible.
The current absorption of these two CPs is checked considering their current absorbed from the voltage source. To check it, a transient simulation in the whole PLL (Fig. 6.14) has been made when the reference is a square wave generator of frequency $f = 20MHz$ and $t_{rise} = t_{fall} = 20MHz$. Fig. 6.24 shows the two currents waveforms absorbed by the CPs realized. With the average function provided by the calculator of ADE, the following average current absorbed values are found:

- $Iav_{currentsteeringCP} = 90.71\mu A$
- $Iav_{CPwithonlynMOS} = 87.03\mu A$

The noise produced by the PFD and CP in lock condition is simulated by using the proof circuit Fig. 6.1 . The generators in fig. 6.1 must have the same output. From the figure 6.25 one may observe that the output phase noise of the two different CPs are very similar. Since the principal aim of this work is obtaining a low power consumption, the type of CP used for the definitive PLL circuit is the CP made with only transistors.

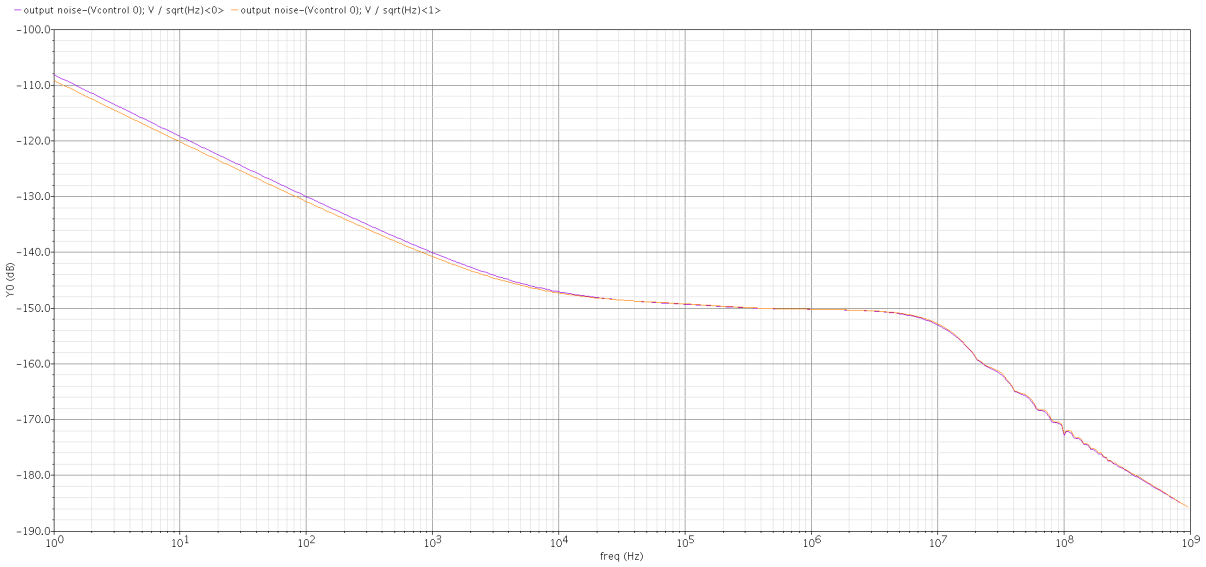

Figure 6.25: *Phase Noise at output CP. Orange line is the PN of the circuit with a CP with only nMOS , Purple Line is the PN at the output of the current steering CP*

In chapter three it has been stated that in current steering CP and in CP made with only nMOS transistors there are also the complementary signals of UP and DOWN. In this way even if the output charge pump is floated the currents can flow using different paths. So the transistors of the current mirrors are always in saturation, thus achieving a faster CP. The Fig. 6.26 shows the same waveforms of the Fig. 6.20. However in order to produce the Fig. 6.26 during the transient simulation the nMOS NM1 and NM5 (Fig 6.18), i.e. the transistors controlled by the complementary signals, were not in the CP. In Fig. 6.26 when UP signal is high and before DOWN signal goes high the tuning voltage V_{cont} reaches the top value $1.2V$ in all the cycles except the first one. Instead in Fig. 6.20 without MOS this never happens. This indicates that the circuit with MN1 and MN5 is faster than the same circuit designed without MN1 and MN5.

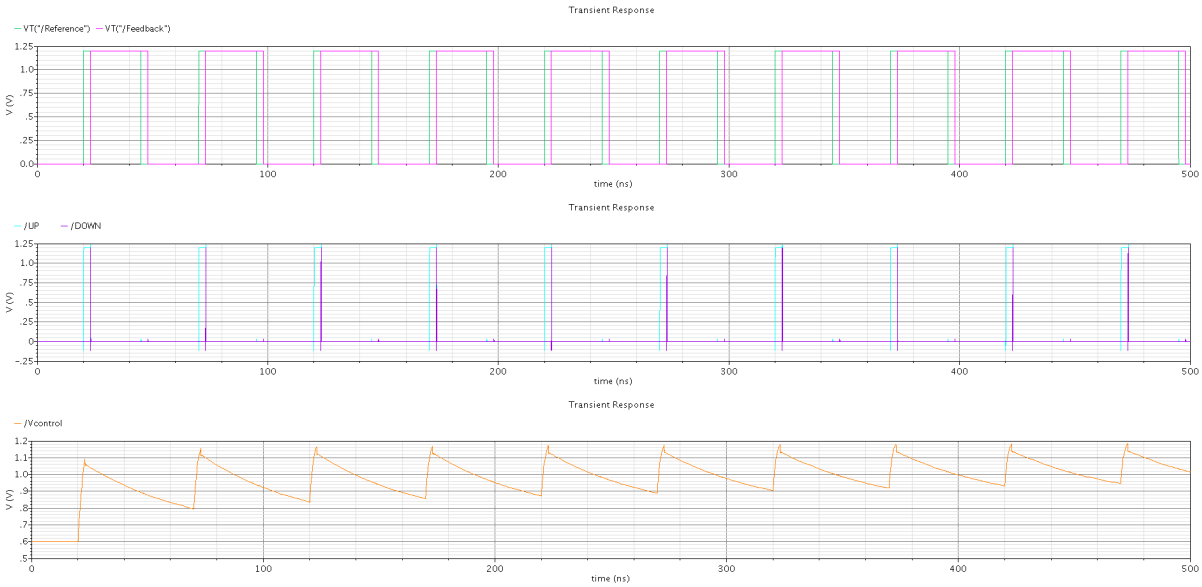

Figure 6.26: *Voltage waveforms at different nodes of the CP made with only nMOS(Fig. 6.14) without NM1 and NM5*

In the third chapter is shown that realizing a cascode current mirror is not possible. For this reason basic current mirrors, each one made with only two transistors, are used. Having small output resistance this type of current mirrors may modify the working of the circuit: since in this situation transistors work close to the subthreshold region, the current value may be too sensitive to the output current mirror voltage. To avoid this, the length of the current mirrors transistors are increased by four times respect to the standard value $l = 120nm$. In the previous paragraph the value of the charge pump current $I_{CP} = I_{UP} = I_{DOWN} = 40\mu A$ was found. To use a small current source of $10\mu A$ the current mirror must have a multiplication factor equals to 4. Then to implement a current mirror with this multiplication factor the channel width of NM3 and NM4 must be four times the channel width of NM2. Therefore NM3 and NM4 have four fingers of width $w = 2\mu m$, while NM2 has only one finger of width $w = 2\mu m$. Figure 6.27 shows the current waveforms obtained in the same situation of Fig.6.22 but without using the current mirror transistors with a length four time greater. In figure 6.26 we can note that the current values (wrong) are not the same of those in Fig.6.22: in particular the currents that flow in the mirrors are about $70\mu A$ that is almost the double respect to the theoretical value of $40\mu A$.

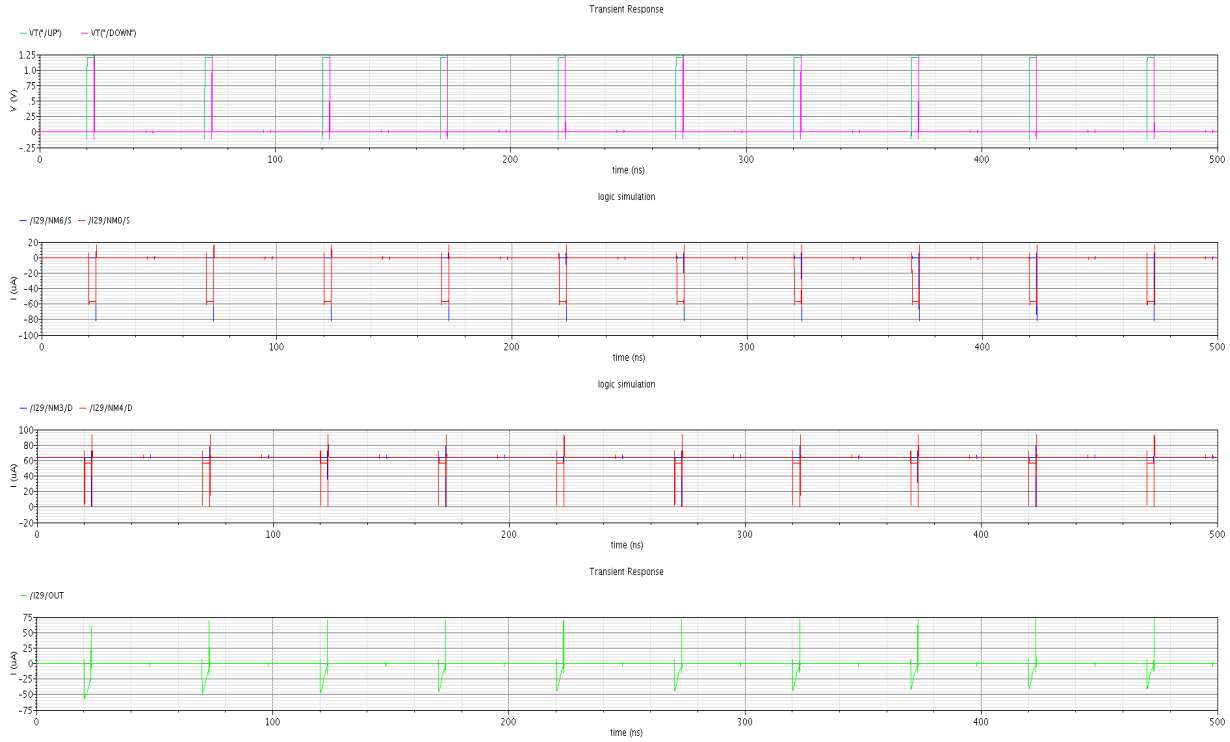

Figure 6.27: *Current waveforms at different nodes of the CP made with only nMOS(Fig. 6.14) with current mirrors MOS with a length* $l = 120nm$

6.4 VCO and Divider

In this work the Voltage Controlled Oscillator and the feedback Divider are not implemented using transistors. But they were necessary to make some simulations in the whole PLL circuit (schematic Fig. 6.14). With the help of the language VerilogA VCO and Divider behavioral models were created basing respectively on the equations (1.2) and (6.2). The two code pieces in VerilogA are the following:

6.4.1 VCO model

```
1  // VerilogA for Tesi, VCO_verilog, veriloga
2
3  `include "constants.vams"
4  `include "disciplines.vams"
5
6  module VCO_verilog(control,out);
7
8         input control;
9         output out;
10
11        voltage control,out;
12
13        parameter real offset=0.6,ampl=0.6;
14        parameter real ffr=2.0G,Kvco=0.6667G;
15
16        real Vc,wout;
17
18        analog begin
19
20                Vc=V(control);
21                wout=(ffr+ Kvco*Vc)*6.28;
22
23                V(out) <+ offset + ampl*cos(idt(wout,0.0));
24                $bound_step (1.0 / 1000);$
25
26        end
27
28 endmodule
```

6.4.2 Divider model

```
1  // VerilogA for Tesi, div, veriloga
2
3  `include "constants.vams"
4  `include "disciplines.vams"
5
6  module div( Vosc, Vdiv );
7
8         input Vosc; // input divider = output oscillator
9         output Vdiv;// output divider
10        voltage Vosc,Vdiv;
11
12        parameter integer N_RATIO =120; // f(Vdiv)=f(Vosc)/N_ratio
13
14        integer counter;    // inner counter
15        integer condition; // "boolean" variable
16
17        analog begin @(cross(V(Vosc)-0.6,1)) begin
18
19                    counter = counter+1;
20                    if(counter >= N_RATIO)
21                              counter =0 ;
22                              condition = (counter*2 >= N_RATIO);
23                    end
24
25
26              V(Vdiv) <+ transition(condition ? 0 : 1.2 , 0 , 10p); // 0 = V_low , 1.2 = V_high ,
27                                                                    // 0= delay time , 10p = fall and rise time
28
29        end
30 endmodule
```

Conclusion

Aim of this work was studying a Phase Locked Loop to be insert in a low power transceiver. The PLL has been used to stabilize the frequency of an oscillator (it will be in the $2.4GHz$ ISM band) when there is a low frequency signal at the input. The present work wanted to analyze the operations of both the PLL and its different blocks, by focusing mainly on Phase Frequency Detector , Charge Pump and Loop Filter. The whole circuit, i.e. the PLL, and its blocks have been studied and simulated in Analog Design Environment(ADE) from Cadence Framework II. The Loop Filter components were designed to guarantee a large stability. In order to design Charge Pump and Phase Frequency Detector, I have first looked at different CP and PFD topologies . For each of these I have made several simulations to detect and understand which one was the best. Simulations have been done by using parameters as the low power consumption and with regards to the PFD also the robustness to the input signal rising and falling edges. As a result I found that the best topology to implement a PFD is Phase Frequency Detector made with DFF in CMOS static technology, whereas the best topology CP is the one made with nMOS only.

Note that in this work The VCO and the integer feedback divider have been not implemented by using CMOS technology with $130nm$ feature size. Instead behavioral models have been created using VerilogA, to be able to do transient simulations in the whole PLL circuit.

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