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Implementation and testing of MHz-range digital conversion of phase current measurements for electric drives

Implementazione e sperimentazione di una conversione digitale alla frequenza dei MHz delle misure di corrente di fase in azionamenti elettrici

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Anno accademico 2018-2019

Abstract

This work deals with a practical implementation of stator current and voltage measurements in an electric drive. The measured signals are sampled at high frequency (in the MHz range), which is significantly higher with respect to the commonly employed sampling rate (in the tens of KHz range) in modern electric drives.

The sampling rate increase is due to several reasons. First, the increasing popularity of wide band gap devices (based on SiC and GaN) put them as a serious candidates for substituting silicon-based devices. Wide band gap devices, other than more efficient and lighter than Si-based devices, are characterized by a higher switching frequency. Naturally, current sampling would need to match the higher switching frequency with an equal sampling rate for the purposes of motor control. Secondly, higher sampling rates can be beneficial for sensorless algorithms that rely on the estimation of inductances by means of the online computation of the stator current time derivative. Thirdly, higher sampling rates of both currents and voltages can enable different condition monitoring algorithm. For example, the insulation status of the stator winding can be monitored by measuring the high-frequency stator current oscillations just after a switching instant has occurred. In order to measure these oscillations, a high-frequency sampling of the stator currents is needed.

In this work, the high-frequency sampling is implemented by means of a FMC112 ADC converter board, containing 12 ADCs operating in parallel, with 14 bit resolution each. The maximum sampling rate offered by this board is 125 MHz. The board is plugged into a Xilinx evaluation board, containing a Zynq System-on-chip unit. The FPGA part of the Zynq deals the low-level communication with the FMC112 ADC converter board, while the ARM cores of the Zynq retrieve the data from the FPGA side and handle the communication with an external data logging system.

Abstract

Questo lavoro di tesi consiste nella realizzazione di un sistema di misura di corrente e tensione di uno statore in un azionamento elettrico. I segnali misurati vengono campionati ad alta frequenza, nel range dei MHz. Questa frequenza è signficativamente più alta rispetto alla frequenza di campionamento comunemente usata, nei moderni azionamenti elettrici, ovvero nel range dei kHz. La decisione di utilizzare le alte frequenze per effettuare il campionamento è dovuta a diverse motivazioni, che verranno descritte di seguito.

Innanzitutto, i dispositivi wide band gap (basati su SiC e GaN), attualmente molto conosciuti/apprezzati/celebri, sono considerati dei possibili candidati, in grado di sostituire i dispositivi a base di silicio. Infatti, oltre ad essere più leggeri ed efficienti di quelli basati sul silicio, essi sono caratterizzati da una frequenza di commutazione più elevata. Naturalmente, l' aumento di frequenza di switching comporta, a sua volta, un aumento della frequenza di campionamento, tutto ciò permette un corretto controllo del motore elettrico.

In secondo luogo, frequenze di campionamento elevate sono utili per la realizzazione di algoritmi sensorless che si basano sulla stima dell'induttanza. Questa stima viene effettuata attraverso la valutazione della derivata temporale della corrente di statore.

In terzo luogo, frequenze di campionamento più elevate di correnti e tensioni possono consentire la realizzazione di algoritmi di condition monitoring. Per esempio, le condizioni dell'isolamento degli avvolgimenti statorici possono essere monitorate tramite la misura delle oscillazioni della corrente statorica ad alta frequenza, che hanno luogo quando si verifica un fenomeno di switching. Per misurare queste oscillazioni è necessario un sistema capace di campionare ad alta frequenza le correnti statoriche.

In questo lavoro di tesi, il campionamento ad alta frequenza è implementato grazie alla scheda di conversione A/D FMC112. Questa scheda contiene 12 ADC che operano in parallelo, ognuno caratterizzato da una risoluzione di 14 bit. Inoltre, la massima frequenza di campionamento è di 125 MHz. La FMC112 è collegata ad una scheda di valutazione della Xilinx, la ZC702, la quale è equipaggiata da un' unità System-on Chip Zynq. La parte FPGA del chip Zynq gestisce la comunicazione di basso livello con la scheda di conversione A/D FMC112, mentre, i due processori ARM dello Zynq recuperano i dati dalla parte FPGA e gestiscono una comunicazione di questi dati con un computer esterno.

La tesi ha la seguente struttura.
Il capitolo 1 è l'Introduzione e descrive le motivazioni e lo scopo della tesi. Il capitolo 2 descrive in dettaglio i componenti fisici scelti per la realizzazione di un sistema di conversione A/D ad alta frequenza.
Il capitolo 3 introduce il firmware alla base della scheda di conversione A/D. Inoltre vengono sottolineate le sue limitazioni che non rispecchiano lo scopo della tesi.
Il capitolo 4 analizza la ricostruzione del firmware portata avanti per ottenere un design modificabile per raggiungere lo scopo della tesi.
Il capitolo 5 mostra i test sperimentali condotti su sistema sperimentale di conversione A/D. Vengono descritte inizialmente le procedure iniziali di settaggio, come la regolazione dell' offset e successivamente vengono analizzati i risultati del campionamento il alta frequenza di diverse tipologie di segnali in ingresso.
Il capitolo 6 descrive i test condotti sul setup sperimentale connesso ad un azionamento elettrico. I risultati sono comprati con le misurazioni effettuate con un oscilloscopio.
Il capitolo 7 e 8 descrivono ripettivamente i lavori fururi e le conclusioni ottenute da questo progetto.

Contents

Abbreviations

ACP	**A**ccelerator **C**oherency **P**ort
A/D	**A**nalog to **D**igital
ADC	**A**nalog to **D**igital **C**onverter
APU	**A**pplication **P**rocessing **U**nit
ASIC	**A**pplication **S**pecific **I**ntegrated **C**ircuit
AXI	**A**dvanced e**X**tensible **I**nterface
CLB	**C**onfigurable **L**ogic **B**lock
CPLD	**C**omplex **P**rogrammable **L**ogic **D**evice
DMA	**D**irect **M**emory **A**ccess
ECC	**E**rror **C**orrection **C**oding
EMIO	**E**xtended **M**ultiplexed **I**nput **O**utput
FIFO	**F**irst **I**n **F**irst **O**ut
FMC	**F**PGA **M**ezzanine **C**ard
FPGA	**F**ield **P**rogrammable **G**ate **Array**
GPIO	**G**eneral **P**urpose **I**nput/**O**utput
HPC	**H**igh **P**in **C**ount
I2C	**I**nter **I**ntegrated **C**ircuit
ID	**I**dentity **D**ocument
I/O	**I**nput/**O**utput
IOB	**I**nput **O**utput **B**lock
IP	**I**ntellectual **P**roperty
JTAG	**J**oint **T**est **A**ction **G**roup
LPC	**L**ow **P**in **C**ount
LSB	**L**east **S**ignificant **B**it

LVDS	**L**ow **V**oltage **D**ifferential **S**ignaling
LVPECL	**L**ow **V**oltage **P**ositive/**P**seudo **E**mitter **C**oupled **L**ogic
MIO	**M**ultiplexed **I**nput **O**utput
PHY	**P**hysical **L**ayer
PL	**P**rogrammable **L**ogic
Pmod	**P**eripheral **mod**ule
PS	**P**rocessing **S**ystem
PWM	**P**ulse **W**idth **M**odulation
QoS	**Q**uality **o**f **S**ervice
RAM	**R**andom **A**ccess **M**emory
ROM	**R**ead **O**nly **M**emory
SD	**S**ecure **D**igital
SDIO	**S**ecure **D**igital **I**nput **O**ouput
S/H	**S**ample/**H**old
SoC	**S**istem on **C**hip
SPI	**S**erial **P**eripheral **I**nterface
TCP/IP	**T**ransmission **C**ontrol **P**rotocol/**I**nternet **P**rotocol
UART	**U**niversal **A**synchronous **R**eceiver-**T**ransmitter
USB	**U**niversal **S**erial **B**us
VHDL	**V**HSIC **H**ardware **D**escription **L**anguage
VHSIC	**V**ery **H**igh **S**peed **I**ntegrated **C**ircuits

Chapter 1

Introduction

1.1 Background

Among the research trends in the field of electric machines and drives, the topics of condition monitoring, wide bandgap switching devices and sensorless control are among the most researched in today's scenario.

Condition monitoring and diagnostics deal with the understanding of the electric drive life-time through the health status of its various components: power electronics switches, DC bus capacitor, stator winding of the electric machine, rotor bars, bearings, and more [1].

Switching devices based on wide bandgap semiconductors, such as Silicon Carbides (SiC) and Gallium Nitride (GaN), are offering improvements with respect to the traditional silicon-based devices in terms of losses, higher switching frequency and high-temperature capabilities [2].

Sensorless control consist on regulating the currents, torque and speed of an electric drive without placing a speed or position sensor on the rotor shaft. This provides cost benefits and improves drive reliability. Several methods have been studied for achieving sensorless control [3, 4].

Although at a first look these three research topics seem distant from each other, there is an improvement in the converter hardware that can be beneficial for all of

them. This consists in the possibility of sampling the electric drive currents and voltages at higher frequencies than it is traditionally performed.

In typical electric drives consisting of silicon-based switches, the required measurements are stator currents, DC bus voltage and optionally phase voltages and speed or position. These signals are usually sampled at the same rate of the PWM switching frequency, which is in the range of few kHz to few tens of kHz. These frequency values allow a good compromise between controllability of the system, current ripple, and the switching losses. For different reasons, the three above-mentioned topics can benefit from an increase of the sampling frequency to considerably higher levels, such as at the MHz range.

The reason why condition monitoring methods can benefit from a MHz-range sampling can be justified by methods for the health status analysis of the stator windings in electric machines. These methods are based on high-frequency oscillations of the stator currents appearing after a commutation of the power switches [5]. Such oscillations are a consequence of the parasitic capacitances between the stator winding turns. The values of the parasitic capacitances, in turn, depend on the winding insulation properties. Therefore, the stator winding insulation status can be monitored by analyzing the high-frequency oscillations of the stator currents.

As mentioned earlier, wide-bandgap devices allow designing a converter with high switching frequencies, above 100 kHz, which can be needed for high-speed drives. The sampling frequency of the measurements should also follow the switching frequency increase. Furthermore, the fast switching implies larger transient overvoltages that lead to an increasing stress for the machine insulation [6]. Therefore, the use of wide-bandgap devices not only need a faster measurement sampling but will also benefit from methods that monitor the stator winding insulation status.

Among the several methods for sensorless control, a possible approach relies on the stator current derivatives [7, 8, 9]. During the switching period, the currents have a ramp-like behaviour due to the PWM voltage. The useful information for such sensorless methods lies in the derivatives of these current ramps. However, having several ramps within each of the switching periods, the resulting time duration of each

ramp is relatively short, i.e. on the range of tens of μs. With conventional sampling rates of current measurements, i.e. only one sample per switching period, obtaining the derivatives of these short current ramps is not feasible. Thus, a higher sampling rate is necessary. Moreover, in order to obtain accurate derivatives, an increasing number of acquired points of the ramp is required. This leads to considerably higher sampling frequencies with respect to the typical switching frequencies.

As a summary, it has just been described how three different topics in the field of electric machines and drives can benefit from an increase of sampling rates of drive measurements. Nevertheless, a practical implementation of the sampling frequency increase pose significant challenges in the drive hardware. The measurement acquisition chain in an electric drive requires three fundamental components: a sensor, an analog-to-digital (A/D) data conversion and a data processing unit. All three elements need to cope with the increased sampling frequency.

The employed sensors should have a sufficient bandwidth in order not to cut the high-frequency content of the measurements. A possible implementation of sensors with extended bandwidth can be found in [10].
The components used for the A/D conversion should be fast enough to ensure the required sampling frequency. Naturally, this will increase the hardware cost.
All data generated by the A/D conversion stage need to be rapidly acquired by a processing unit, in order not to lose any of the samples, which come at a higher-than-usual data rate. Therefore, high throughput devices are required for this purpose.

1.2 Scope of the thesis

The scope of this thesis is to implement and test an experimental system, which include the A/D conversion and the processing unit stages, capable of high frequency sampling of drive measurements. The system is to be considered part of a laboratory setup for an electric drive control. Thus, a requirement for the processing unit stage is to host, other than the high-frequency samples acquisition, also the drive control algorithm.

1.3 Structure of the thesis

The thesis has the following structure.

The chapter 1 is the Introduction and it describes the motivation and the scope of this thesis.

Chapter 2 describes in details the physical components chosen to perform a high-frequency A/D conversion.

Chapter 3 introduces the firmware of the A/D conversion board and its limitation for the purpose of this thesis.

Chapter 4 analyses the firmware reconstruction in order to achieve a customisable design for the purpose of this thesis.

Chapter 5 shows the experimental testing of the A/D conversion system. It firstly describes the initial setup procedures such as the offset regulation and it finally analyses the results of high-frequency sampling with different input signals.

Chapter 6 describes the tests carried out on an experimental setup with an electric drive. The results are compared with measurements performed by an oscilloscope.

Chapter 7 and Chapter 8 describes the future works and the final remarks, respectively.

Chapter 2

Laboratory setup for high-frequency sampling of drive measurements

In this chapter the laboratory setup for an electric drive with high-frequency sampling is described. The schematic of the setup is shown in Figure 2.1. Other than high-frequency sampling capabilities, in the described setup a customisable control can be implemented and measurements can be logged to an external computer.

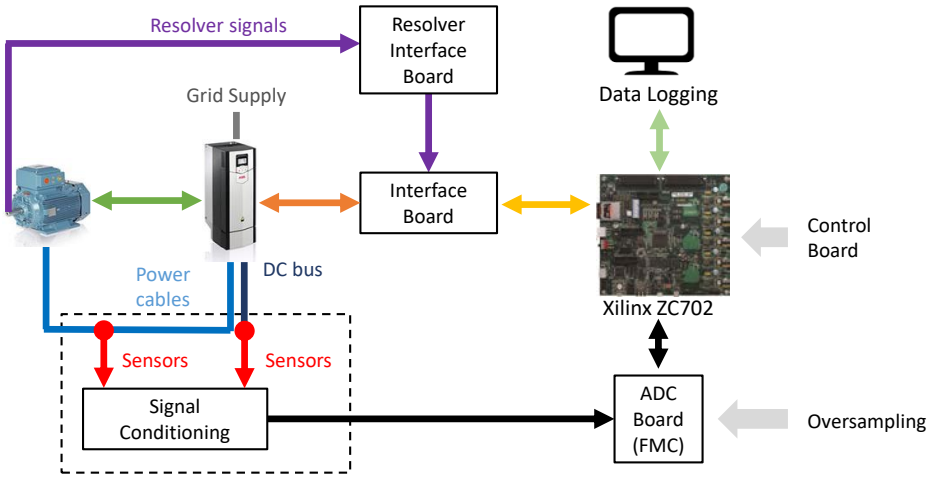


FIGURE 2.1: Schematic of the electric drive laboratory setup.

In order to obtain a high-frequency sampling it is necessary to choose a special equipment that guarantees a large bandwidth, reduced latencies and that is able to manage high-speed data. These requirements can be translated into requirements for the three principal elements of the system:

1. Current and voltage sensors, and their relative conditioning circuits, with a sufficiently large bandwidth.
2. Fast ADCs.
3. A high-speed processing unit.

The setup shown in Figure 2.1 is made of eight main components:

1. An electric motor in which its three-phase stator currents and voltages will be measured.
2. A frequency converter ABB ACS880 to provide variable frequency and variable amplitude three-phase voltages to the motor. The converter is supplied by the three-phase grid voltage that is internally rectified to obtain a DC bus voltage, which feeds a half bridge DC to AC inverter. Moreover, the DC bus voltage is measured in order to perform the PWM (Pulse-Width Modulation) technique.
3. A custom interface Board that couples the Control Board with the frequency converter, providing galvanic insulation. The data exchanged through the interface board are the IGBTs gate signals and few other protection signals of the frequency converter.
4. A Control Board that provides the computational power to the setup, giving the possibility to implement custom control algorithms that are independent from the employed frequency converter. For this purpose, a Xilinx ZC702 Evaluation Board, containing a Zynq-7020 chip, was used.
5. An ADC board, Abaco FMC112, that contains 12 parallel channels with a sampling frequency up to 125 MHz.

6. A Signal Conditioning Board to filter the sensor outputs and to adapt their voltage levels to the one accepted by the ADC board, as done in [10].
7. The voltage and current sensors.
8. An external computer for data logging purposes through TCP/IP protocol.

The voltage and current sensor outputs, after being conditioned, are digitally converted in two possible alternative ways:

- With a regular and relatively slow sampling (in the order of 10 kHz) to perform standard drive control algorithms.
- As a burst of fast sampled (in the MHz range) data that is sent to the external computer to be further analysed, in order to achieve conditioning monitoring.

In the remaining of this chapter, the components of Figure 2.1 which are more relevant for the purposed of this thesis will be described. Thus, section 2.1 will describe the ZC702 Evaluation Board while section 2.2 will show the ADC board characteristics.

2.1 Control board

The control board chosen for the experimental setup is the Xilinx ZC702 Evaluation Board, which is shown in Figure 2.2. The ZC702 Board offers a hardware environment suited for developing and evaluating designs. It is characterised by the presence of a Zynq-7020 System-on-Chip (SoC) as core and of many interfaces that increase the prototyping possibilities of this board. Furthermore, it provides common elements of an embedded processing system, as well as:

- DDR3 memory components;
- General purpose I/Os;
- 10/100/1000 Mbps Ethernet PHY;
- UART interfaces.

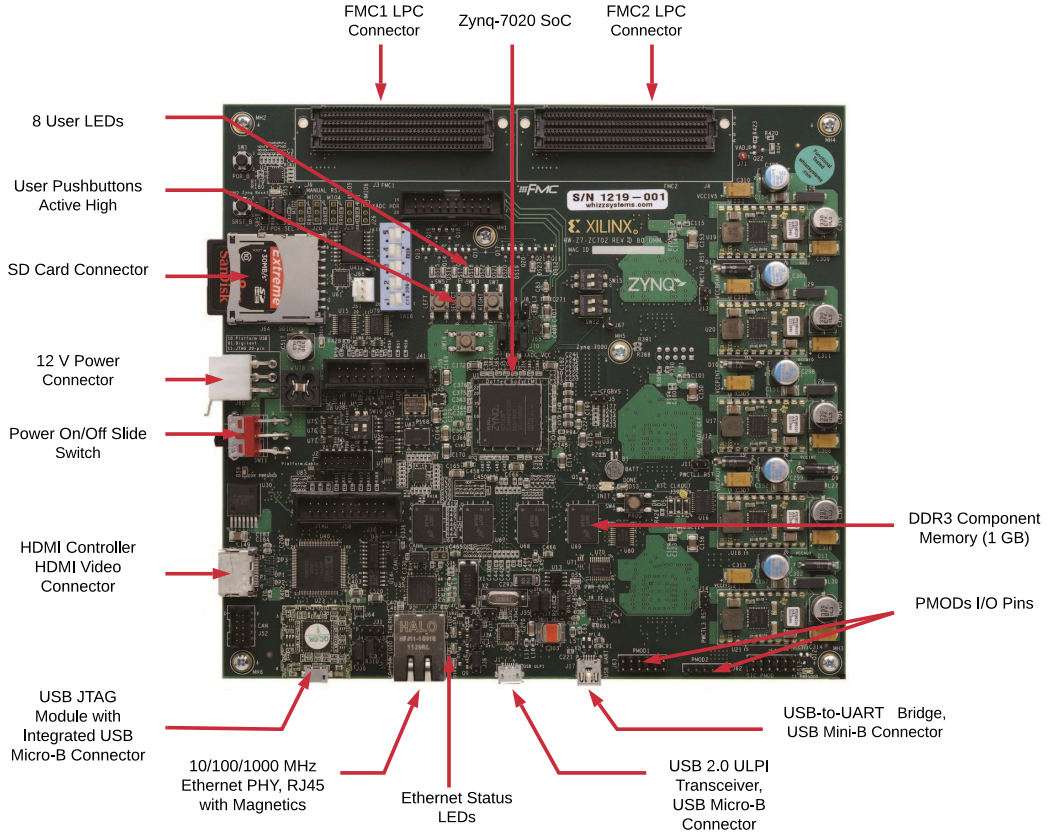


FIGURE 2.2: Xilinx ZC702 Evaluation Board.

In the following Table 2.1 the general characteristics are summarised:

TABLE 2.1: General characteristics of Xilinx ZC702 Evaluation Board [11].

Dimensions	19.685 X 18.161 cm
Operating Temperature	0°C - +45° C
Storage Temperature	-25°C - +60° C
Operating Voltage	12 V_{DC}

The Table 2.2 shows the key features of the ZC702 Board.

TABLE 2.2: Xilinx ZC702 Evaluation Board key features [12].

Memory	DDR3 Component Memory 1 GB Support 32 data width
Clocking	200 MHz Fixed PL Oscillator (Differential LVDS) 156.25 MHz I2C Programmable Oscillator (Differential LVDS) 33.33 MHz Fixed PS System Oscillator (Single-Ended CMOS)
Communication & Networking	Gigabit Ethernet GMII, RGMII and SGMII USB UART (PS)
Control & I/O	3 User Push Buttons 2 User Switches 8 User LEDs
Expansion Connectors	FMC #1-LPC (0 GTX Transceiver, 68 single-ended or 34 differential user defined signals) FMC #2-LPC (0 GTX Transceiver, 68 single-ended or 34 differential user defined signals) Single and double Pmods

The ZC702 board is the central element of the project as a result of the many features that play an important role in the development process. The presence of a variety of peripheral interfaces facilitates the design for data logging, the control system and also the acquisition system. The capabilities of the development board can be extended by attaching external modules. These extensions are possible by the presence of these main expansion connectors:

- **2 FPGA Mezzanine Connectors (FMCs)**: they are based on a standardized interface that permits the connection to external cards. They are characterised by a high-speed transmission (up to 10 GBit/s) and numerous differential or single ended I/Os available. Detailed information about the FMC connectors is given in section 2.1.2.

- **2 Peripheral modules (Pmods)**: peripheral modules are a simple interface type for the connection of additional modules to the FPGA. These modules can be simple push buttons, or more complex elements such as network interfaces or analog to digital converters. Pmods accept three main protocols: SPI, I2C and UART. The ZC702 is characterised by two Pmod headers, one single (6 pins, 4 signals) and one double (12 pins, 8 signals).

2.1.1 Zynq-7020 System-on-Chip

As mentioned above, the core of the ZC702 is the Zynq-7020 SoC, whose schematic is shown in Figure 2.3. The general architecture of the Zynq SoC comprises two sections: a dual ARM A9 Cortex core, referred as Processing System (PS), and 28nm Xilinx FPGA, referred as Programmable Logic (PL). These two parts can be used together or independently, but more benefits are reached by their simultaneous use. The Zynq SoC allows to create custom logic in the PL and custom software in the PS in order to implement unique and high-performance systems. The union of PS and PL in the same chip permits a communication between the two parts with extended bandwidth and low latencies with respect to the case of separate processor and FPGA components. Furthermore, the hardware design results simplified. The communication between PS and PL is based on the AXI protocol. This protocol is illustrated in section 2.1.1.3.

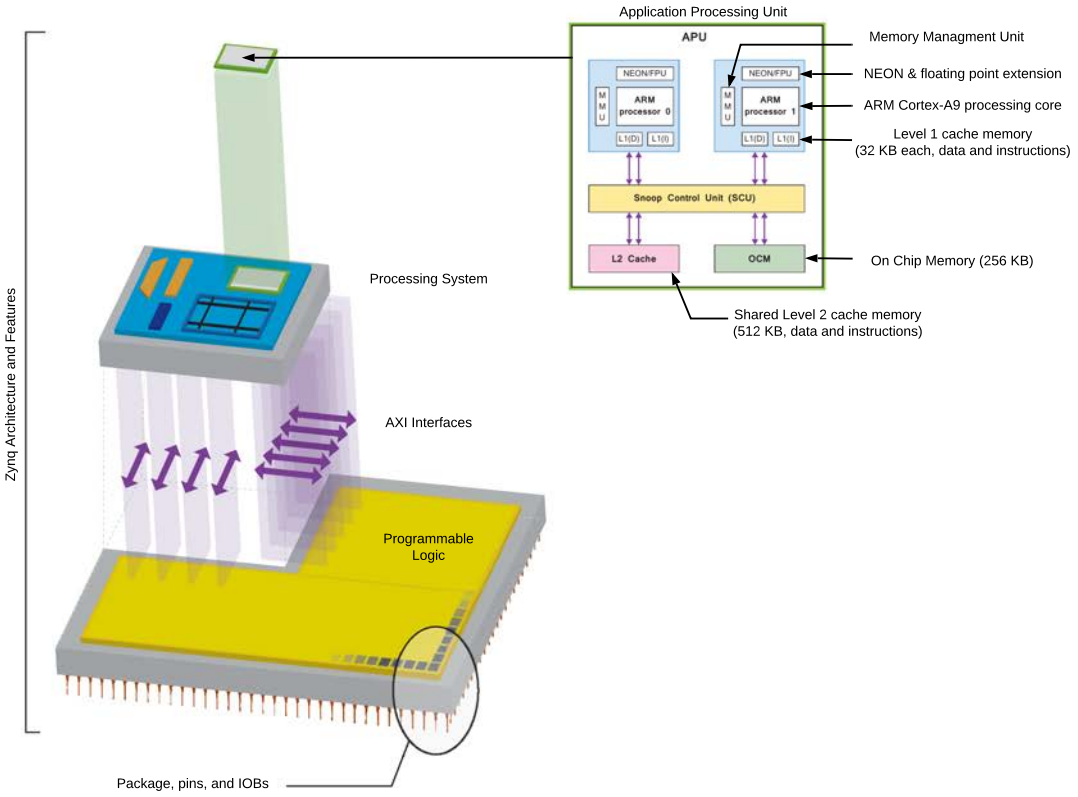


FIGURE 2.3: Zynq-7020 SoC interfaces, signal and pins [12].

2.1.1.1 Processing System

The heart of the PS part is the dual-core ARM Cortex-A9 processor , but in addition to it there are other elements, such as: APU, cache memory, memory interfaces, central interconnect, clock generation circuitry and I/O peripherals including USB, Ethernet, SPI, SD/SDIO, I2C, CAN, UART and GPIO as shown in Figure 2.4. The main features are listed in Table 2.3.

TABLE 2.3: PS main features.

Application Processor Unit (APU)	CPU frequency up to 1 GHz
Caches	32KB level 1 cache (independent for each CPU) 512KB level 2 cache (shared between the CPUs)
On-Chip Memory	256KB on-chip RAM
I/O Peripherals and Interfaces	Two 10/100/1000 Mbps Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support Two high-speed UARTs (up to 1 Mb/s) GPIO with four 32-bit banks (of which 54 bits controllable by the PS, 64 bits controllable by the PL and 54 bits for flexible pin assignments).

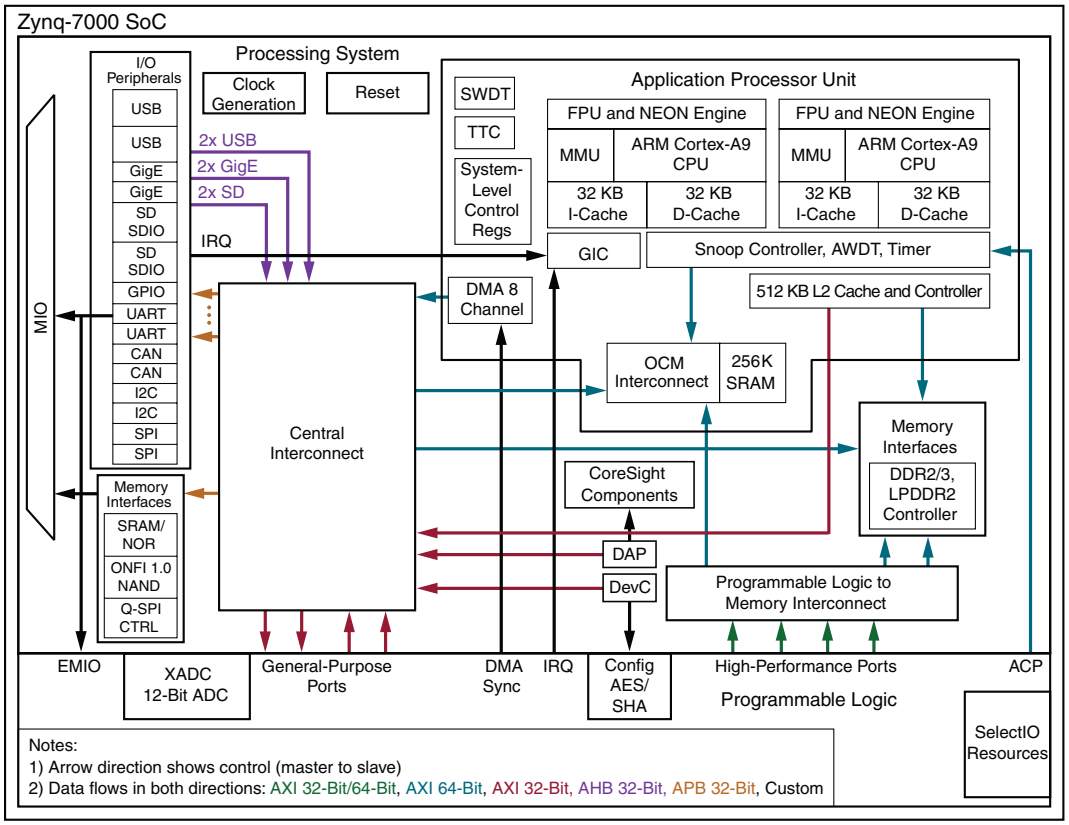


FIGURE 2.4: The Zynq-7000 architecture [12].

2.1.1.2 Programmable Logic

The PL is the FPGA part of the Zynq 7020 SoC. A representation of the PL is shown in Figure 2.5. The FPGA presence is beneficial when fast and parallel computation

with low latencies is needed. Its components are described in the following list:

- **CLB**: it is composed by logic elements, including two slices. They are connected to other similar resources by programmable interconnections.
- **Slice**: sub-unit of the CLB, which allows the implementation of combinatorial and sequential logic circuits.
- **Switch Matrix**: flexible routing to connect elements within CLB and other parts in the PL.
- **IOBs (Input/Output Blocks)**: resources that permit to connect the PL with the external world.

In addition to the general fabric two more types of blocks have been added in order to increase the capabilities of the system:

- **Block RAMs** that can implement RAM, ROM and FIFO for dense memory requirements. Each RAM block can store up to 36Kb and it can be used individually or it can be combined with other RAM blocks to form a larger capacity.
- **DSP48E1** slices for high-speed arithmetic.

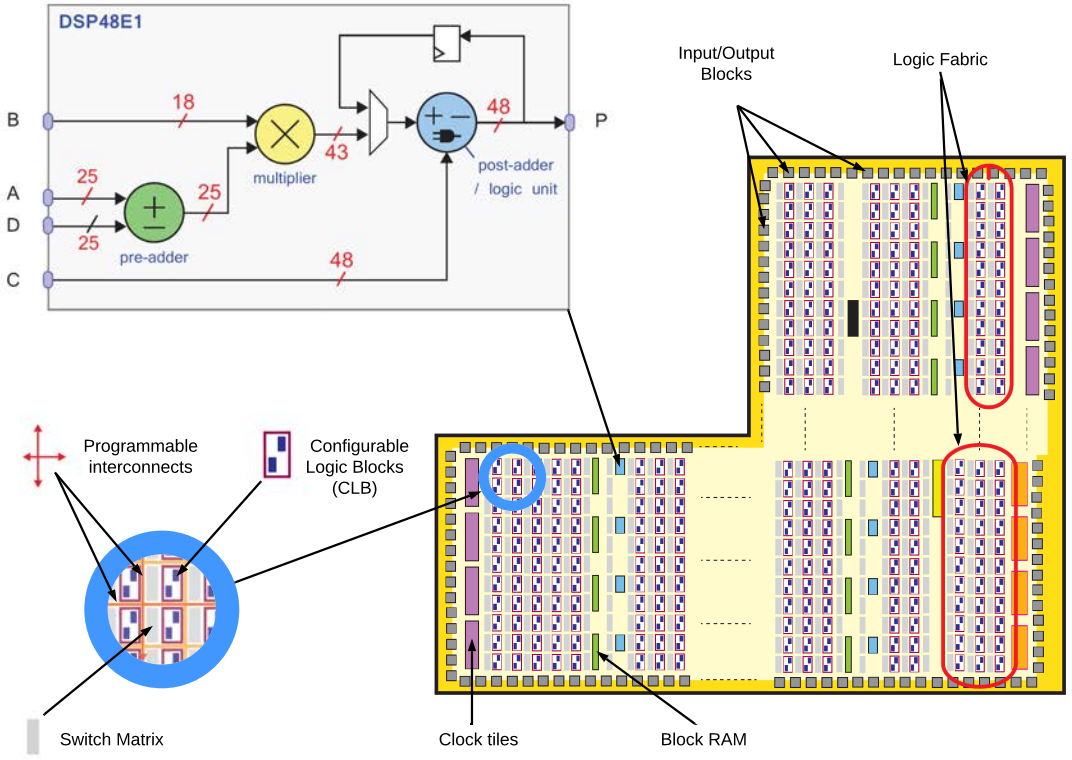


FIGURE 2.5: The Zynq Programmable Logic [12].

2.1.1.3 Communication between PS and PL

As previously described in section 2.1.1, a key element of Zynq-7020 SoC is the communication between PS and PL. The bridges that permit this easy and rapid communication are:

- **AXI Interconnect**, shown in Figure 2.4, as the Central Interconnect block. It implements the AXI Standard as communication protocol.
- **EMIO** is used for a direct connection of the PS with the external pins or with the PL.

The protocol AXI is part of the ARM AMBA 3.0 standard. AXI 4.0 was born in 2010 to realize high-performance system designs. The key features of this protocol are:

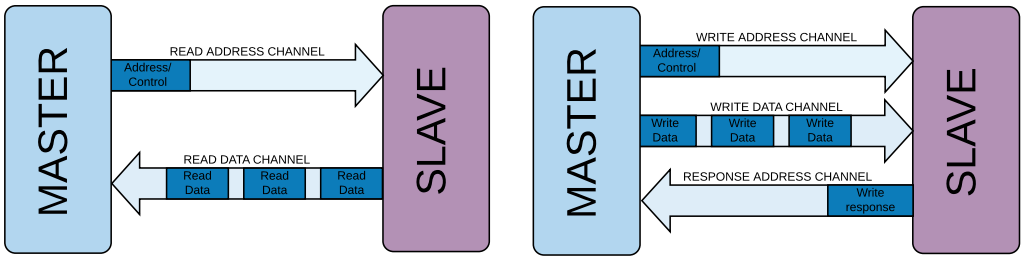
- High-bandwidth and low-latency communication;

- Separate address/control and data signals;
- Separate read and write data channels allowing Direct Memory Access (DMA).

The AXI protocol is based on a Master-Slave Control. This communication process is a burst-based communication that contains these following communication channels:

- Read address
- Read data
- Write address
- Write data
- Write response

Examples of a read and a write transaction are shown in Figure 2.6a and in Figure 2.6b, respectively.



(A) (B)

FIGURE 2.6: AXI protocol: AXI read (2.6a) and AXI write (2.6b).

The AXI protocol allows to choose three types of communication:

- **AXI4**: A high-performance interface, suited for memory mapped communication allowing bursts of up to 256 data transfer cycles, with just a single address. It is suited for high performance communications.
- **AXI4 Lite**: A lighter interface version, suited for single memory mapped transactions. It doesn't support burst data. It is ideal for a lighter communication and to reduce hardware utilisation.

- **AXI4 Stream**: It does not required an address, so it is not memory mapped, and it is characterised by an unlimited burst size. It is best suited for a constant stream of data packet communication.

The interfaces that permit the application of the protocol allowing to transfer data between PL and PS and vice-versa are listed in Table 2.4 and summarised in Figure 2.6.

TABLE 2.4: Interfaces between PS and PL.

Interface Name	**Interface Description**	**Master**	**Slave**
AXI_M_GP0	General Purpose (AXI_GP)	PS	PL
AXI_M_GP1		PS	PL
AXI_S_GP0	General Purpose (AXI_GP)	PL	PS
AXI_S_GP0		PL	PS
AXI_S_ACP	Accelerator Coherency Port (ACP), cache coherent transaction	PL	PS
AXI_S_HP0	High Performance Ports (AXI_HP) with read/write FIFOs	PL	PS
AXI_S_HP1		PL	PS
AXI_S_HP2		PL	PS
AXI_S_HP3		PL	PS

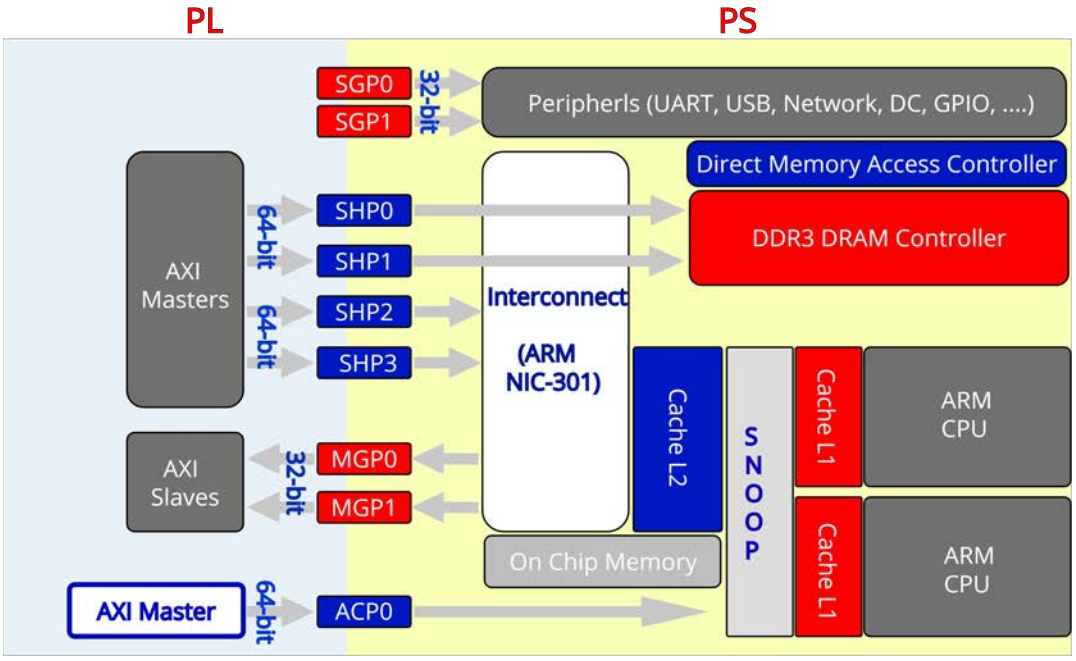


FIGURE 2.7: Interfaces between PS and PL.

For more information about the AXI protocol, see [13] and [14].

2.1.2 FMC Connector

FPGAs are characterised by a wide number of I/O and in order to expand the capabilities of their external I/O interfaces, the FPGA Mezzanine Card (FMC) connector has been realised by Xilinx.
The potential data throughput up to 40 Gb/s, the presence of low latencies, the design simplicity and the possibility of its reuse in other designs are some of its advantages. The VITA 57 standard defines the standardisation of this connector. It sets two mezzanine card form factor connectors: a sigle-width (69 x 76.5 mm) and a double-width (139 x 76.5 mm) form factor.

Once the form factor has been selected, there are two different type of connectors:

- **Low Pin Count (LPC)** connector with 160 pins. 68 user-defined, single-ended signals or 34 user-defined, differential pairs;

- **High Pin Count (HPC)** connector with 400 pins. 160 user-defined, single-ended signals or 80 user-defined, differential pairs, 10 serial transceiver pairs and additional clocks.

The Xilinx ZC702 Evaluation Board has been designed with two LPC connectors. The Figure 2.8 shows the FMC connector and its pins.

More information about FMC connector is reported in [15] and in [16].

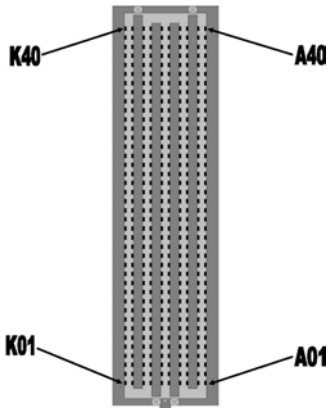
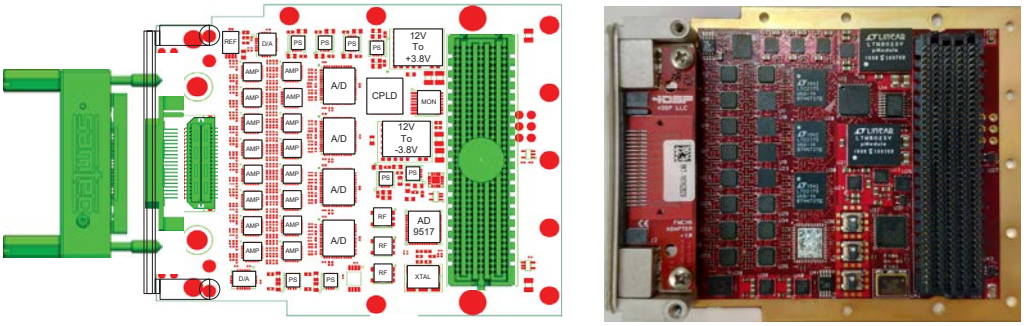


FIGURE 2.8: FMC connector view [16].

2.2 The ADC board



(A) (B)

FIGURE 2.9: Abaco FMC112 Board: components layout (2.9a) and board view (2.9b).

The FMC112 is a 12-channel ADC Board, designed by Abaco System. The board, shown in Figure 2.9, can be interfaced to the ZC702 control board through the FMC

LPC connector. The 12 ADCs in the board can work in parallel, each of them ensuring a 14-bit conversion with a sampling rate up to 125 Msps. The conversion is based on three components Linear Technology *LTC2175-14*, each of them containing four ADCs. The whole board is supplied by the Control Board via the FMC connector.

The characteristics of the FMC112 Board are listed in Table 2.5.

The analog input signals are connected to the board via a combination of *Samtec QSE* connector and a *SMA* breakout cable, which is shown in Figure 2.10. In turns, the *Samtec QSE* connector is coupled to the FMC112 Board as shown on the left part of Figure 2.9a.

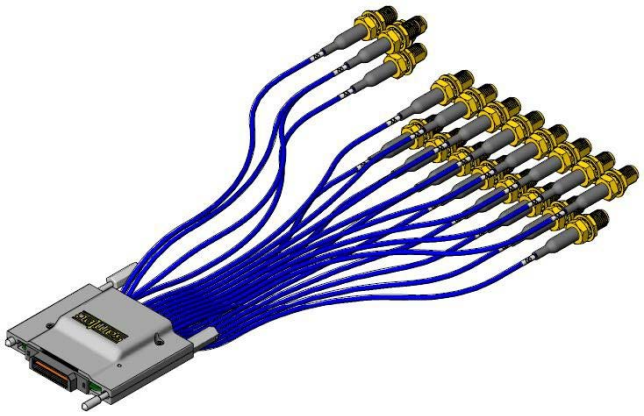


FIGURE 2.10: SMA breakout cable [17].

The FMC112 block diagram in Figure 2.11 shows the main channels and elements involved in the conversion process. The Samtec connector in the front panel accepts as inputs single ended DC coupled signals. Instead, the ADC components *LTC2175-14* present in the board accepts differential inputs. For this reason, an intermediate circuitry is placed in the board, with the component *ADA 4938* [18] converting the single-ended signals into differential ones. Other than this, in such circuitry it is implemented the possibility to insert a programmable offset correction of the input. This is a fundamental feature since the ADCs *LTC2175-14* [19] accepts unipolar signals with an input voltage range of $[0, 2]$ V, while the outputs of voltage and current sensors are typically bipolar. The programmable offset correction is due to the presence of two Linear Technology DAC *LTC2656* [20].

Moreover, the FMC112 Board provides the possibility to both generating the clock internally, through the Analog Devices *AD9517[21] Clock Generator*, or to obtain the clock externally, These options are handled by the bock "*Clock Tree*" of Figure 2.11. The external clock, together with optional input and output trigger signals, are carried by the *SMA* breakout cable.

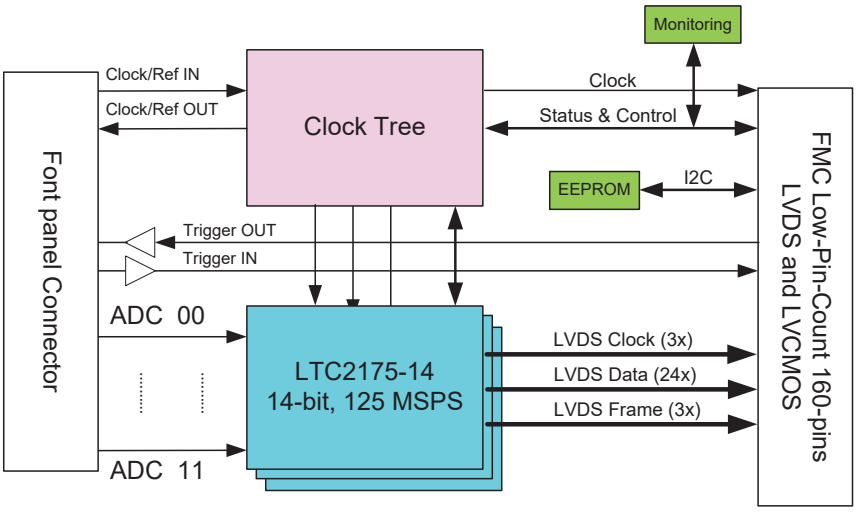


FIGURE 2.11: FMC112 block diagram [17].

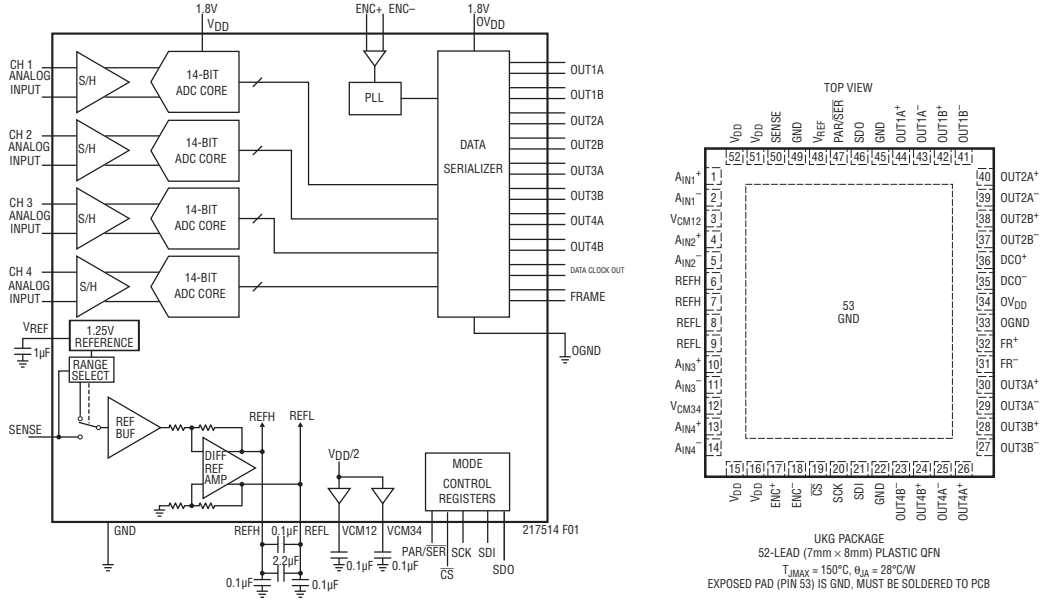
The FMC112 can be configured by the ZC702 via FMC connector and SPI protocol. The configuration is realised by writing into registers of a *CPLD* present in the FMC112 Board. These registers are described in section 2.2.2.

TABLE 2.5: FMC112 main characteristics.

Analog inputs	
Number of channels	12
Channel resolution	14-bit
Input voltage range	2 V_{P-P}
Input impedance (SMA cable)	50 Ω
Analog input bandwidth	DC-Coupled up to 62.5 MHz
ADC Output	
Output data width	2-pair DDR LVDS per channel Frequency 3.5 times the sample frequency
Data Format	Offset binary or 2's complement
Sampling Frequency Range	5 MHz to 125 MHz
FMC connector type	LPC
Internal sampling clock	
Format	LVPECL
Frequency Range	up to 125 MHz (software programmable)

2.2.1 ADC LTC2175

The FMC112 Board contains 3 *LTC2175-14* ADC chips as the key components of the conversion [19]. The *LTC2175-14* is a 4 channels, 14-bit ADC. The channels can sample simultaneously at up to 125 MHz. In Figure 2.12a and in Figure 2.12b the *LTC2175-14* Block Diagram and the chip package are shown, respectively.



(A) (B)

FIGURE 2.12: LTC2175 Block Diagram 2.12a and chip view 2.12b [19].

The 14 bits of the ADC digital output are serialised in Low Voltage Differential Signaling (LVDS) to minimised the data lines. It is possible to choose, depending on the sampling frequency, two bits output channel for high frequency sampling (2 lane mode) or a one bit output channel for lower sampling rates (1 lane mode). In the FMC112 Board, the 14-bit serialisation 2-lines output mode has been chosen and it is shown in Figure 2.13.

The main characteristics of this ADC chip are resumed in Table 2.6.

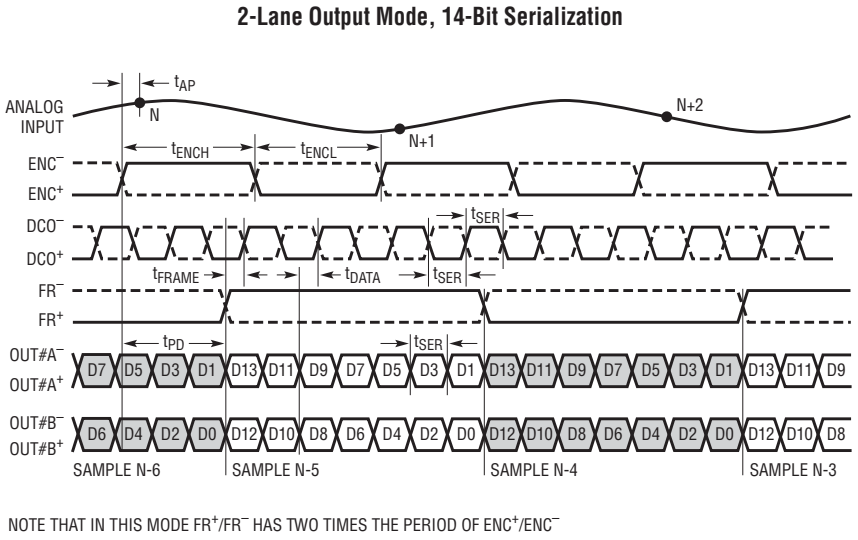


FIGURE 2.13: 2-Lanes Output Mode, 14-bit serialization [19].

TABLE 2.6: LTC2175-14 main characteristics [19].

SYMBOL	PARAMETER	CONDITIONS	VALUES	UNITS
Analog Input				
V_{IN}	Analog Input Range (A_{IN}^+ - A_{IN}^-)	Differential Analog Input	1 to 2	V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Analog Input	V_{CM}±100 mV	V
Timing characteristics				
f_S	Sampling Frequency		5 to 125	MHz
t_{AP}	Sample and Hold Acquisition Delay Time		0	ns
t_{SER}	Serial Data Bit Period	2-Lanes, 14 bit Serialization	1/(7*f_S)	s

2.2.2 CPLD

As mentioned in section 2.2, the FMC112 Board can be configured via SPI by writing into the registers of the *CPLD* present in the FMC112 Board. In turns, the *CPLD* distributes the SPI access to the components of the FMC112 Board and generates their reset signals. Moreover, it selects the clock to be used and stores the data monitoring. The registers used to configure the FMC112 Board are shown in Table 2.7.

TABLE 2.7: CPLD registers.

Register n°1								
Bt n°	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	'0'	SYNC	CLKR	LDAC	DACR	Reserved	CLKSRC	
Register n°2								
Bt n°	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	Reserved			IRQ	VM	STATUS	LD	REFMON
Register n°3								
Bt n°	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	CLKSRC			LED_SEL				

By changing the values of the various register fields it is possible to modify the settings in the FMC112 Board. The meaning of each register field is listed below:

- **Register n°1** controls the FMC112 Board.
- **Register n°2** is connected with the FMC board monitoring status.
- **Register n°3** is the register of the status signal.

The schematic of the *CPLD* component is shown in Figure 2.14.

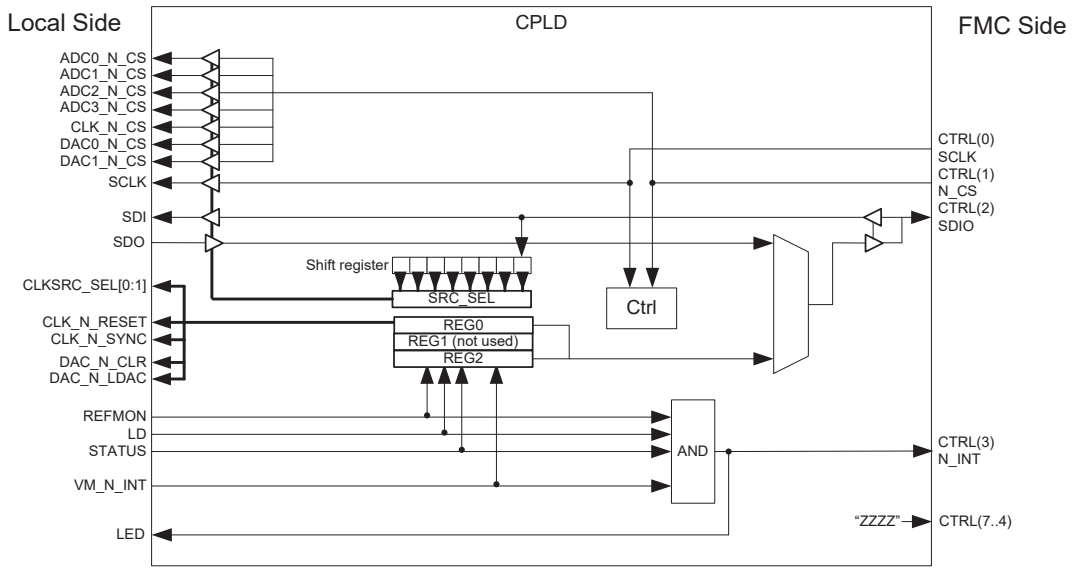


FIGURE 2.14: CPLD architecture [17].

Chapter 3

ADC board firmware

Abaco Systems, the FMC112 manufacturer, provided a software support package tailor made for the operation with the ZC702 Evaluation Board. This support package includes a software to program the PS part of the ZC702 Control Board, allowing a communication between the ZC702 and an external PC via TCP/IP. Moreover, the support package includes also a firmware to program the PL part of the ZC702. The main role of this firmware is to control the communication and data flow with the FMC112 Board. In this chapter, the provided firmware for the PL part is introduced, and it shortcomings are explained.

The firmware is given in the form of Intellectual Property (IP) blocks, which is the typical programming style of modern FPGAs. IP blocks performs a defined and documented logic task between their inputs and outputs. In this project the IP blocks are written in VHDL. Furthermore, Abaco Systems company adopts the following specific terms for the composition of its firmware:

- **Star**: An IP block with a specif task and a generic pin-out.
- **Wormhole**: A connection between two or more stars.
- **Constellation**: A group of stars, connected by Wormholes, which form the top level of a firmware design.

Using these terms, the final goal of the given support package is the creation of the constellation *ZC702-FMC112*, which is a Xilinx project file. This is done by means of a Abaco Systems' software tool, namely Stellar IP, that creates the Xilinx project file starting from the firmware source code, i.e. the IP blocks [22].

This chapter analyses the Xilinx project file created by Stellar IP. Precisely, the section 3.1 describes the Constellation layout of the entire system. After that, the illustration flow proceeds deeper with the analysis of each star. It is interesting to examine in depth the main stars: the ZC702 Host Interface star, namely *ZC702 Host If*, in section 3.1.1, the FMC112 star in section 3.1.2 and the Constellation ID star, called CID star, in section 3.1.3. Finally, the chapter underlines in section 3.2 the limitation related to the system and makes a comparison with respect to the needs of the thesis project target.

3.1 Explanation of constellation IP and star system

The constellation *ZC702-FMC112* is shown in Figure 3.1 and it is composed by the following seven top stars:

- **ZC702 Host If**: This star manages the communication of the ZC702 with the external computer through TCP/IP. Furthermore it receives data from the FIFO 64K star and it sends them to the external computer. All commands to the other stars, together with the clock and reset signals, are generated by the *ZC702 Host If* star [23].
- **FMC112 Star**: The FMC112 star handles the communication with the FMC112 ADC board, by managing its flow of data and commands [24]. It is the only star in the constellation that is physically connected to the FMC112 Board.
- **Constellation ID Star**: This star is composed by read-only registers and it contains information about the constellation. These data includes IDs of the elements of the system, addresses and address ranges [25].

- **I2C Master**: *I2C Master* star is the supervisor of the Inter Integrated Circuit (I2C) protocol [26] adopted for the management of the voltage and temperature circuitry present in the FMC112 board [27].
- **Router 12 to 1**: The *Router 12 to 1* routes data from a 12 channels input to a one output channel [28].
- **Multiplexer**: The *Multiplexer* star routes the commands from all the stars to a one output channel connected to the *ZC702 Host If* star [29].
- **FIFO 64K**: *FIFO 64K* routes the data from the input port to the output port offering a 64 KB FIFO as a buffer to store data in case of a slowing down of the communication due to a bottle neck or an interruption in the data channels [30].

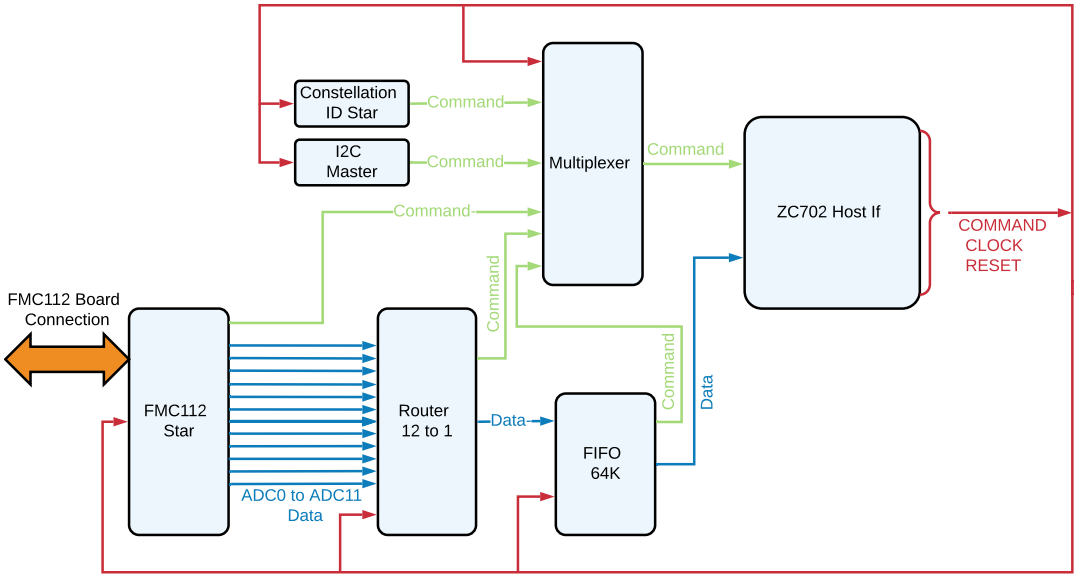


FIGURE 3.1: Abaco Firmware.

The protocol adopted for the communication among stars is a Stellar IP property protocol, which have three type of interfaces: Data Wormhole Inputs, Data Wormhole Output and Stellar IP Commands. As shown in Figure 3.1, the wormholes interconnections can be divided into three main functions, depicted with different colours:

- The red control channels have the purpose of sending control signals from the *ZC702 Host If* to the stars of the entire constellation. They consist in the command, the clock and the reset channels.

- The command channels are green. They are status signals about the application of the commands received by the stars. These channels pass through the *Multiplexer* star that selects between the several input signals and forwards it to a single output line. Finally this flow is addressed to the *ZC702 Host If* block.

- The data channels, in blue, is the flow of the acquired sampled data coming from the FMC112 Board. The 12 data wormholes, one for each ADC, start from the FMC112 star and they are routed into the *Router 12 to 1* star in order to forward all the data packages into a single output port. The routing of data can be set by registers present in the *Router* IP block. Afterwards the data traffic meets the *FIFO 64K*, which integrates into the data line a safety buffer FIFO in order to prevent data losses. This FIFO is implemented using Block RAM Memory IP blocks. Finally data reach the *ZC702 Host If*.

3.1.1 ZC702 Host Interface Star

The ZC702 Host Interface star is the core of the constellation and it contains the *Zynq Processing System* block, as shown in Figure 3.2. The *Zynq Processing System* block represents the PS part (dual ARM core) in the SoC fabric.

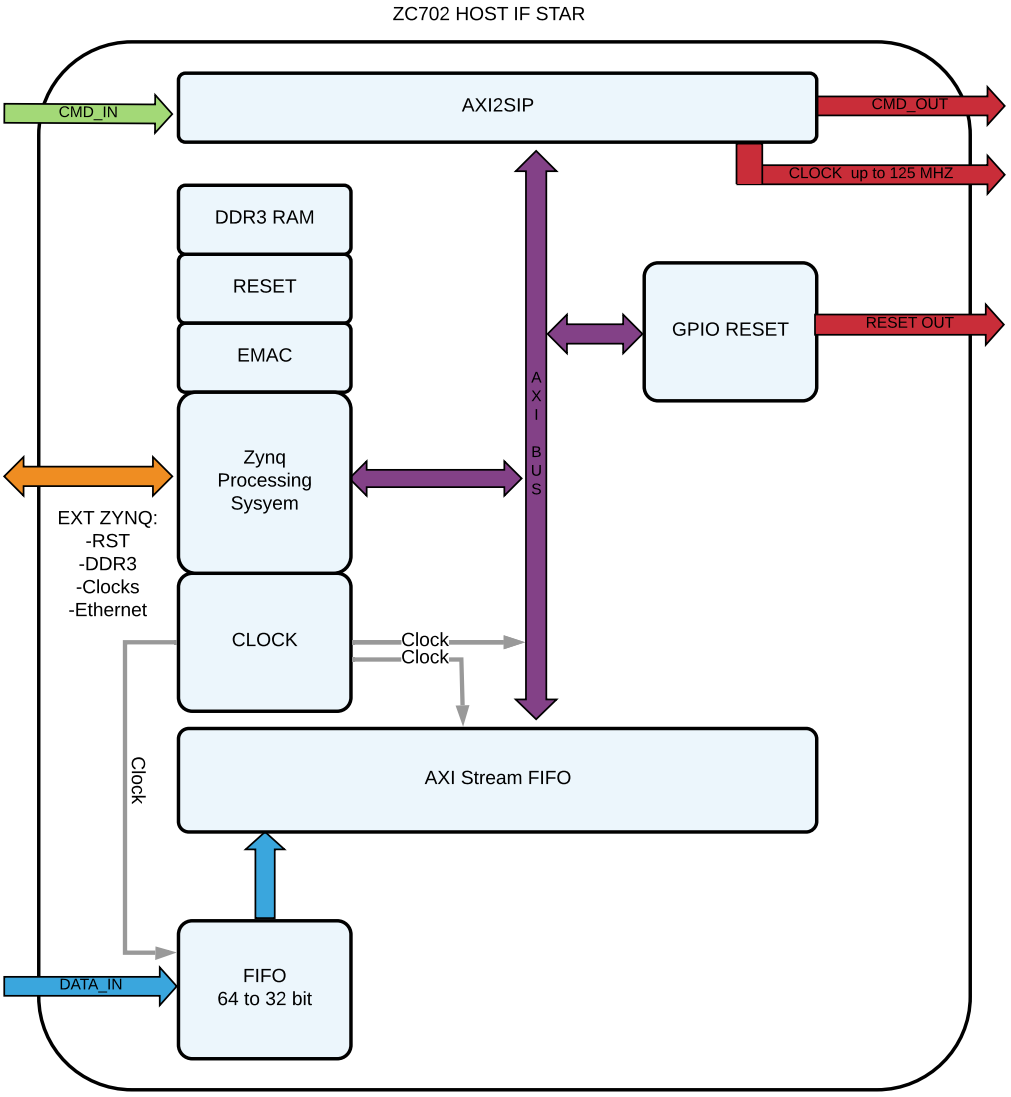


FIGURE 3.2: *ZC702 Host If*

The TCP/IP protocol, used for connecting the ZC702 Control Board with the external computer, is implemented in the *Zynq Processing System* block. By the use of this protocol, the communication channels between the sampling system and the external computer are set. The data logging process is explained in section 5.1.

As previously described in section 3.1, the constellation adopts a Stellar IP property protocol for the communication. However, the *ZC702 Host If* star, as shown in Figure 3.2, is governed by the AXI protocol, described in section 2.1.1.3. The implementation of two different protocols requires a conversion step for the data and for

the commands, respectively. These translation steps are realised into the *AXI2SIP* IP block for both the input and output command channels and into the *FIFO 64 to 32* block for the input data channel. Once translated into AXI protocol compatible signals, the data are acquired with the AXI Stream interface while the commands are handled by the AXI Lite.

The *ZC702 Host If* block produces the reset signal for its internal IP blocks and the reset signal to govern the constellation. The reset is produced by an *AXI GPIO* IP block and it is managed by the PS. The *clock tree* generates the clock and it is forwarded to the stars through the *AXI interfaces* and the *AXI2SIP* block.

3.1.2 FMC112 Star

The internal setup of the FMC112 star is shown in Figure 3.3 and it can be divided into two main parts: the first is composed by registers for the configuration of the FMC112 Board, the second is responsible to adapt data from the ADCs.

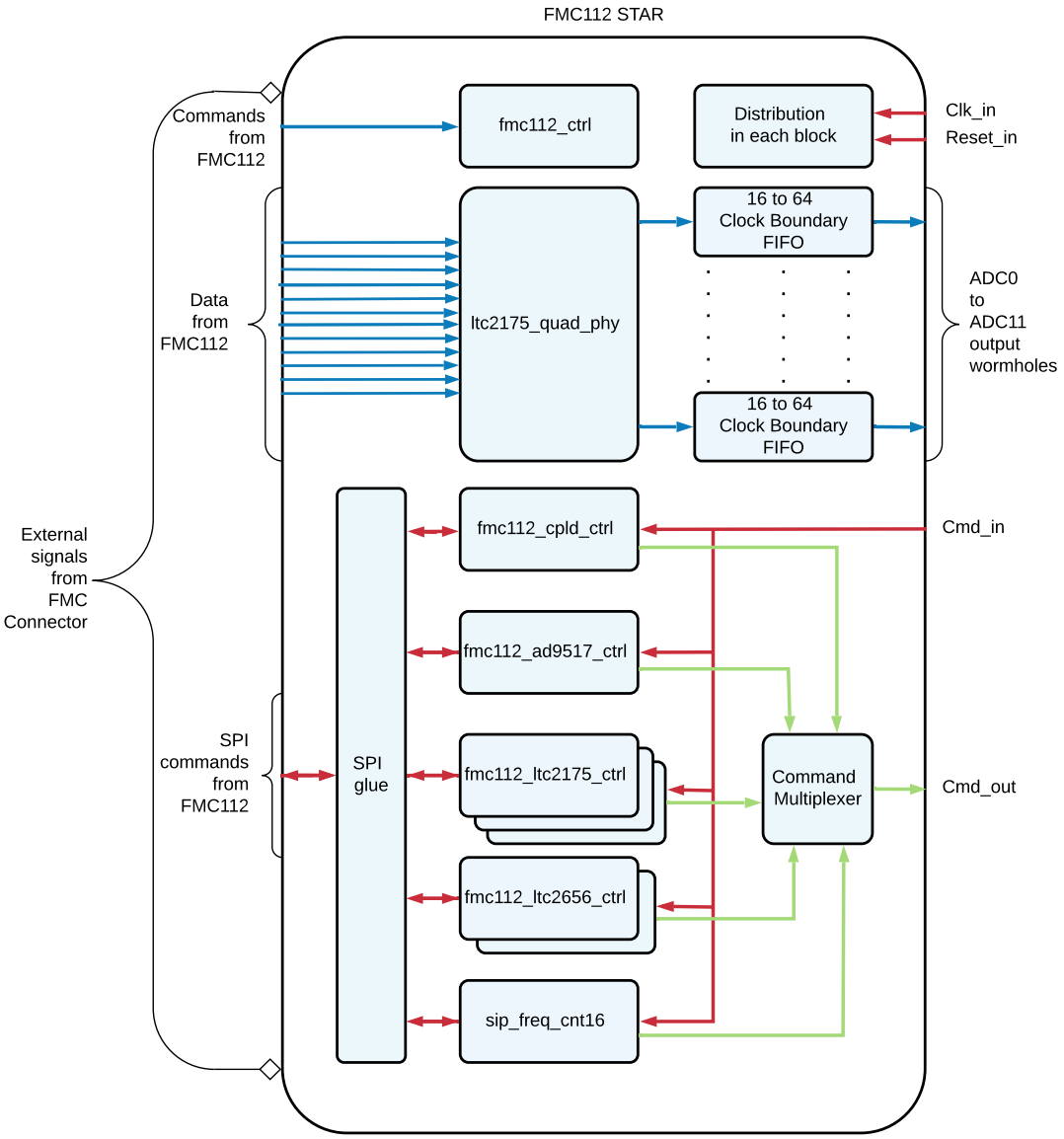


FIGURE 3.3: FMC112 Star.

The FMC112 Board configuration is managed by the Serial Peripheral Interface (SPI) communication. Through the SPI commands it is possible to write into the registers that are responsible for the programming of the A/D conversion. The main available functions that can be programmed are:

- Enabling and disabling the 12 ADCs and the DACs for the offset correction.
- The number of burst and the burst size of samples to acquire.

- Establishing the source of the clock, which can be generated into the FMC112 board or externally.
- Establishing the source of the trigger, which can be generated into the FMC112 board (namely software trigger) or externally.

The main programmable registers to set up the conversion board are shown in Figure 3.3 and they are described in the following list:

- **fmc112_ctrl** is responsable to set the number of burst, the number of samples per burst and to arm/disarm the ADCs LTC2175-14.
- **ltc2175_quad_phy** sets the delay among the data signals.
- **fmc112_cpld_ctrl** sets the distribution of the SPI access to the local elements implemented in the FMC112, selects a clock, sets the generation of the reset signal for the components present in the ADC board and stores condition data.
- **fmc112_ad9517_ctrl** sets and monitors the *AD9517 Clock Generator*.
- **fmc112_ltc2175_ctrl** sets and monitors the ADC devices, 0 to 2 (3 X ADC LTC2175-14).
- **fmc112_ltc2656_ctrl** sets and monitors the DAC devices, 0 to 1 (2 X DAC LTC2656).
- **sip_freq_cnt16** selects the frequency source for the sampling.

The sampled data from the 12 ADCs in the FMC112 board are the data input of the FMC112 Star, shown as the 12 blue lines in Figure 3.3. Each of these 12 channels carries serially the 14 bits of a specific ADC output. In the FMC112 Star, two bits are added to each of the 14 bits serial data channels and then all channels are demultiplexed to 64 bits, to be compatible with the other stars of the constellation. The resulting output wormholes of the FMC112 Star are called ADC0 to ADC11.

3.1.3 Constellation ID Star

In the firmware all stars and the constellation itself are assigned to specific IDs. Furthermore, independent address ranges are assigned to each star. The command bus (the red line in Figure 3.1) can in this way access to the different registers of a specific star. The information about IDs and address ranges is stored in the Constellation ID (CID) star, which is shown in Figure 3.4. The main registers in the CID star are listed in Figure 3.4.

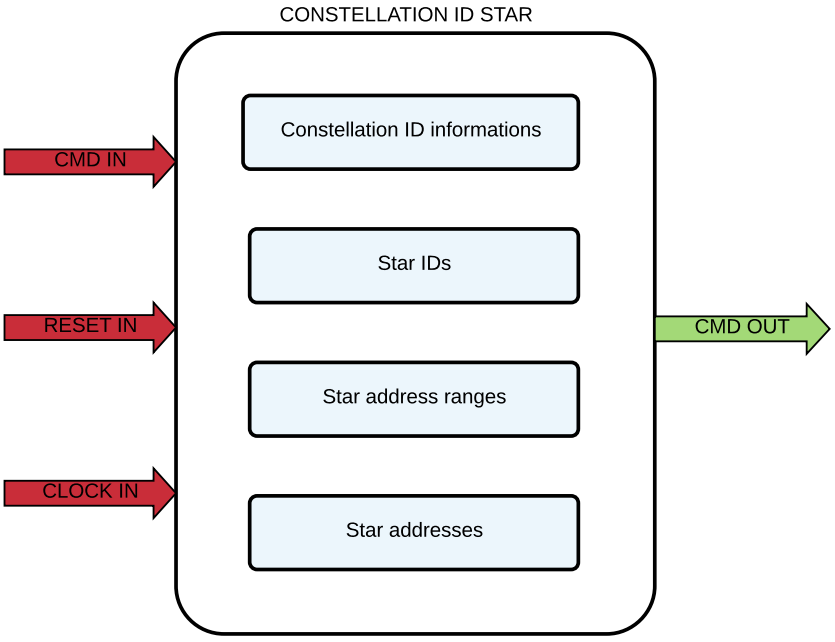


FIGURE 3.4: Constellation ID

3.2 Limitations of the firmware

In a typical PL design in the Zynq system, the various IP blocks can communicate to the PS via the *AXI interface*. In this way a design can be easily expanded with additional functions implemented by IP blocks. In the given firmware design, the PS (represented by the *Zynq Processing System* IP block) and the *AXI interface* IP block are already included in the *ZC702 Host If* star, as shown in Figure 3.2.

Furthermore, PS and *AXI interface* together with other IP blocks are locked in a so-called System entity, as the yellow box in Figure 3.5 suggests. Unfortunately, having the *Zynq Processing System* and the *AXI interface* IP blocks locked and inaccessible makes the firmware design not easy to expand with other IP blocks, to implement for example a drive control algorithm. These limitations are in contrast with the purpose of this thesis described in chapter 1, i.e. performing both drive control and signal acquisition on the same device. For this reason, the firmware will be modified as described in chapter 4.

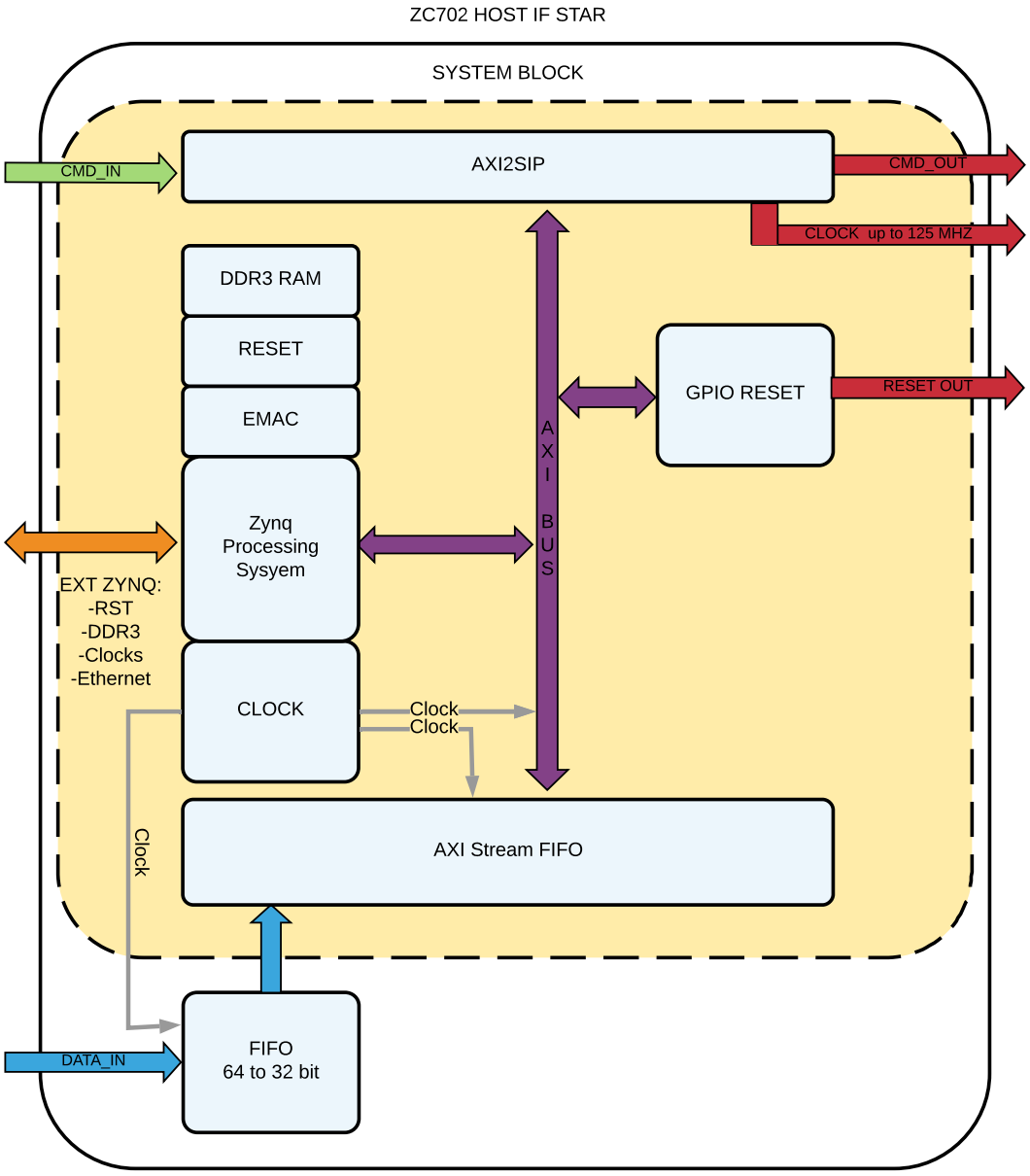


FIGURE 3.5: *ZC702 Host If* with System block

Chapter 4

Reconstruction and testing of the ADC board firmware

As previously explained in section 3.2, the Abaco firmware has some limitations that are in contrast with the project purposes. The analog-to-digital acquisition system required for the project must have the following characteristics:

- Clarity
- Easy to modify and control
- Easy to expand its features without limiting the base characteristics
- Multitasking, i.e. it can work in parallel to a drive control routine implemented in the same hardware

In order to reach these purposes a re-design of the firmware is needed. Section 4.1 introduces the first improvement, the creation of a new *ZC702 Host If* block. Section 4.2 explains how the new designed firmware is tested with a simulation software testbench.

4.1 Reconstruction of the firmware

The re-design of the the *ZC702 Host If* block starts from the analysis of the Abaco default block ([22], [23], [31], [32], [33]) and by the examination of its VHDL codes. As a result of the requirements listed in the beginning of the chapter, the IP block in Figure 4.1 has been designed. A comparison with the Abaco block in Figure 3.2 shows that the older star version has been substituted by two new stars. The first star, namely *ZC702 Host If Modified*, has the duty to receive/send signals from/to the stars of the constellation. The second one, namely *Customisable Design*, a future system expansion.

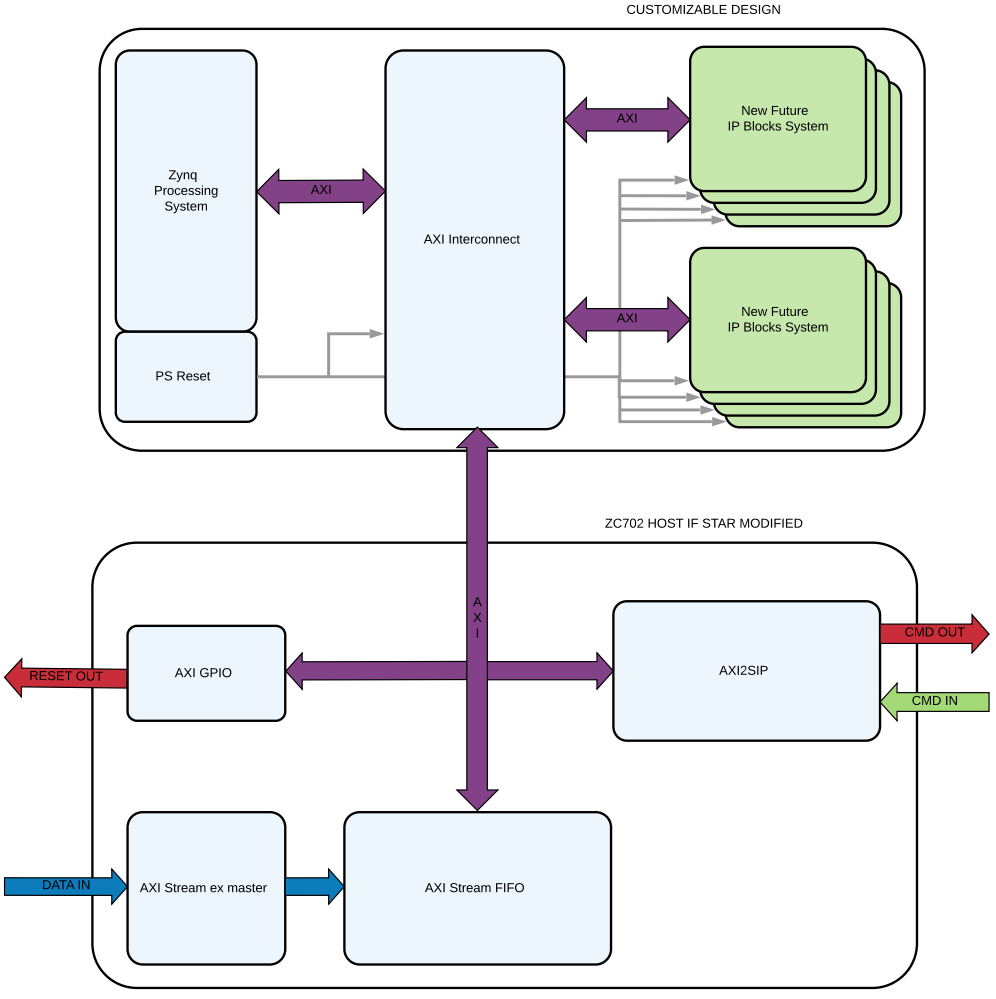


FIGURE 4.1: New design of the *ZC702 Host If* star

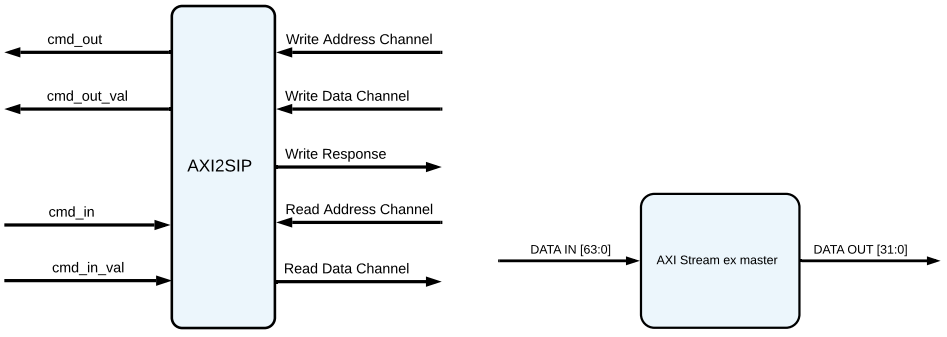
Let's observe more in detail the characteristics of each part.

In the same way of Abaco firmware, in the new system the AXI protocol has been implemented in the inner communication of the new *ZC702 Host If* star. As a result a conversion stage is needed due to the adoption of two communication protocols as previously described in the section 3.1.1. The *ZC702 Host If Modified* implements the conversion process of command signals from AXI protocol to SIP protocol for output signals and from SIP protocol to AXI protocol for input signals by the *AXI2SIP* IP block. The data conversion is lead by the *AXI Stream ex master* block, which converts an input data packet of 64 bits into a 32 bits output. These two blocks are represented in Figure 4.2a and in Figure 4.2b, respectively.

The *AXI Stream FIFO* block converts AXI4/AXI4 Lite transactions in AXI Stream ones. The *Zynq Processing System* block is placed as the key component of the *Customizable Design* block, being the centre of both the TCP/IP communication and the data reception. This block is strictly connected with the *PS Reset* block, which provides the reset signal for all the blocks of the expansion future systems.

On the other hand, the reset signal for the stars in the external constellation is generated by a *AXI GPIO* block placed in the *ZC702 Host If Modified* star.

The *AXI interconnect* assumes the role of intermediary among the *Zynq Processing System*, the *New Future IP Blocks Systems* and the outer constellation.



(A) (B)

FIGURE 4.2: *AXI2SIP* block in Figure 4.2a and *Axi Stream ex master* block in Figure 4.2b.

The footprint of the new firmware in the FPGA logic fabric of the Zynq-7020 is shown in Figure 4.3. The image represents the real Zynq-7020 chip and it can be compared

with the ideal one exposed in Figure 2.5.

In order to reach a correct interpretation, a legend is listed below:

- **Yellow** part is the PS and its connections with the PL.
- **Magenta** blocks are the memory blocks.
- **Light blue** squares are the logic cells.
- **Orange** blocks are the I/O PIN blocks for external connection.

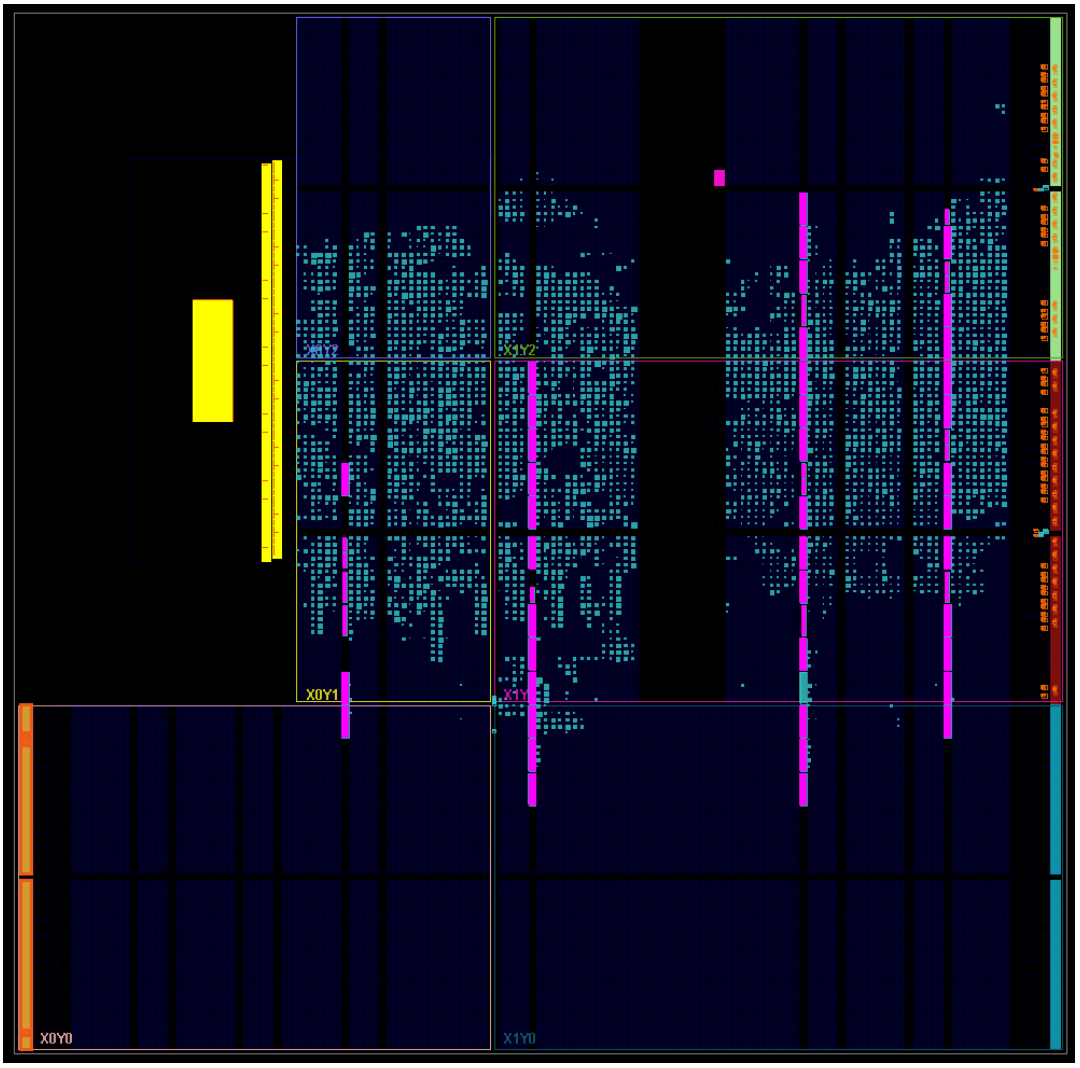


FIGURE 4.3: Footprint of the new firmware in logic fabric

The Zynq resources utilisation is presented in the chart of Figure 4.4. It is interesting to linger on the FPGA utilisation where it is underlined a high use of memory entities required for the high frequency sampling process.

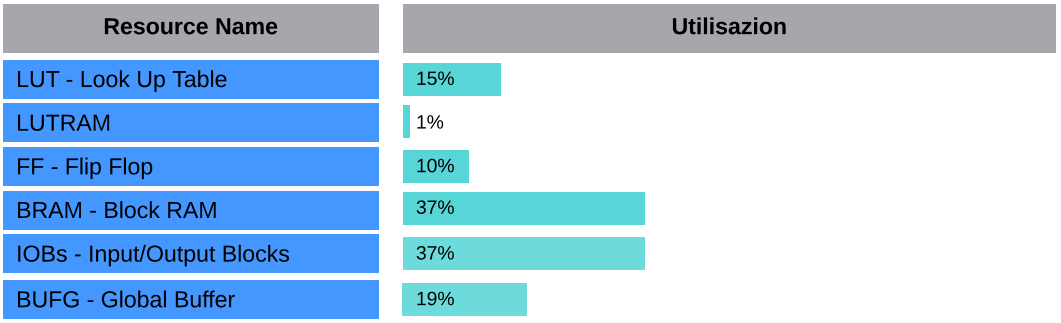


FIGURE 4.4: Zynq resources utilisation

4.2 Testbench recostructed firmware

As a result of the design of a new firmware, the functionality of the system has to be tested with a simulation software testbench.

The simulation tests the correct data flow and the command transmission between the FMC112 star and the *ZC702 Host If Modified*. The command and data flows of the firmware have been explained previously in section 3.1.

In order to test these functions of the firmware, the system represented in Figure 4.5 has been designed as a testbench. In addition to the normal system, the yellow blocks have been added.

The simulation of the FMC112 14 bit signals production has been entrusted to the *Simulated FMC112 Board* block on the left. This block emulates the real conversion process implemented into the FMC112 board.

The simulation of sampling-related commands is realised by the *Simulated ZC702 Host If* block on the right.

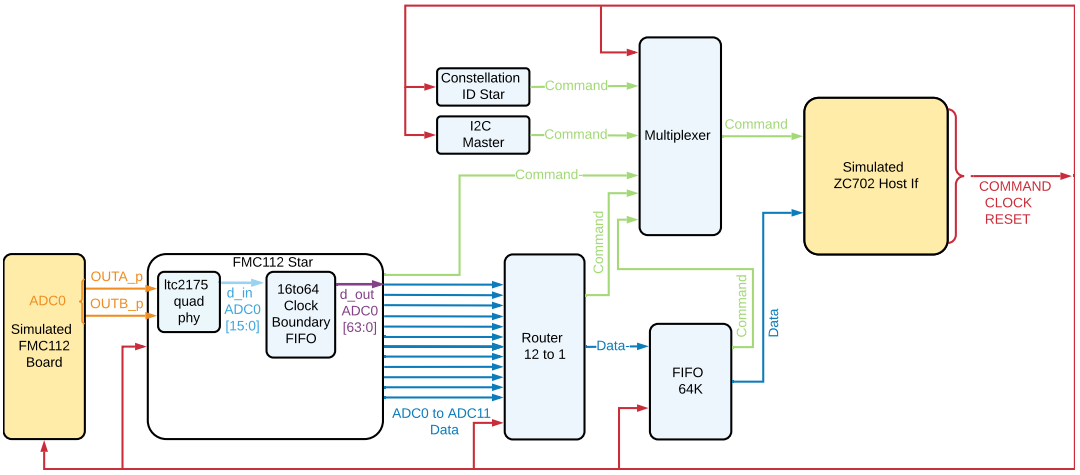


FIGURE 4.5: Testbench Firmware

Let's analyse the setting commands generated by the *Simulated ZC702 Host If*. The following commands are generated in series:

1. Reset the digital ADC data and clock input.
2. Set the number of burst to 1.
3. Set the burst size to 100 samples.
4. Set up the 12 to 1 Router to route data from the ADC0 to the *Simulated ZC702 Host If* block.
5. Send the enable signal to the ADC0.
6. Send the arm command and a software trigger signal to the ADC0.

The signal flow is described below and it is represented for a clear interpretation in the Figure 4.5. The ADC0 is simulated into the *Simulated FMC112 Board*, which produces a 14 bits signal, namely $PTTRN$.

$$PTTRN[13:0] = \{1\ \ 0\ \ 0\ \ 0\ \ 1\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\ \ 0\}$$

$$PTTRN[13:0] = \{PTTRN(13), PTTRN(12), ..., PTTRN(1), PTTRN(0)\}$$

The $PTTRN$ signal is serialised as represented in Figure 2.13 into 2 signals of 7 bits each, namely $ADC0\_OUTA\_p$ and $ADC0\_OUTB\_p$.

$$ADC0\_OUTA\_p[6:0] = \{PTTRN(13), PTTRN(11), PTTRN(9), \ \ldots \ , PTTRN(1)\}$$

$$ADC0\_OUTB\_p[6:0] = \{PTTRN(12), PTTRN(10), PTTRN(8), \ \ldots \ , PTTRN(0)\}$$

Then, the serialised signals of all the ADCs are compacted into the 2 signals, displayed in orange in Figure 4.5, namely $OUTA\_p$ and $OUTB\_p$.

$$OUTA\_p[11:0] = \{ADC0\_OUTa\_p(13), ADC1\_OUTa\_p(13), \ \ldots$$

$$\ldots \ , ADC10\_OUTa\_p(13), ADC11\_OUTa\_p(13)\}$$

$$OUTB\_p[11:0] = \{ADC0\_OUTa\_p(12), ADC1\_OUTa\_p(12), \ \ldots$$

$$\ldots \ , ADC10\_OUTa\_p(12), ADC11\_OUTa\_p(12)\}$$

This is the real behaviour of the FMC112 board. As a consequence of this type of transmission 6 clock cycles are required to collect all the 14 bits data packet of each ADC.

The block *ltc2175_quad_phy* brings these signals as input and a manipulation data process produces 12 signals, namely *d_in[15:0]*, each composed by 16 bits, one for each ADC. The *ltc2175_quad_phy* ideally produces a signal for the ADC0 channel composed by the *PTTRN[13:0]* left shifted of two bits.

$$d\_in_{\ with\ phase\ alignment} = \{PTTRN[13:0] \ \ 0 \ \ 0\}$$

Since the sampling is not phase aligned, the output *d_in* is the *PTTRN[13:0]* left shifted by two bits and shifted again by a casual number of bits.

After that, the *d_in* 16 bits signal is dispatched to the *16 to 64 Clock Boundary FIFO* that produces the 64 bits output signal, namely *d_out*, repeating the input signal for four times.

Finally the *Router 12 to 1* routes data to the *FIFO 64K* star, which is directly connected with the *ZC702 Host If* star. The data channel that reach the *ZC702 Host If* block is called *in_data_in_data*, a 64 bits wormhole. As a consequence of the command sent at the beginning of the testbench to enable the routing of the ADC0 data, the signal *in_data_in_data[63:0]* is equal to the *d_out[63:0]* of the ADC0.

The testbench behavioural signals are shown in Figure 4.6 and as aspected they follow the previous description. The representation shows:

- In red the command signal, namely *cmd_out_cmdout[63:0]* and the clock that controls the ADC conversion, namely *clk_to_adc*.
- In orange the data output of the *Simulated FMC112 Board* related only with the ADC0, namely *outa_p[11:0]* and *outb_p[11:0]*.
- In light blue the output of the *ltc2175_quad_phy*, namely *din[15:0]*.
- In purple the output of the *16 to 64 Clock Boundary FIFO*, namely *dout[63:0]*.
- In gold the start and the stop signals for the data transmission, namely *in_data_in_dval* and *in_data_in_stop, respectiely.*
- In dark blue the data signal that reaches the *ZC702 Host If* block, namely *in_data_in_data[63:0]*. It is interesting to linger over the correlation between *in_data_in_dval* and *in_data_in_data* at t=43,100.000 ns. In this case the status change of the first one implies the data flow in the latter.

As a consequence of these signals behaviour, the overall conclusion is that the re-designed firmware reflects expectations and the command and data flows are correctly reproduced.

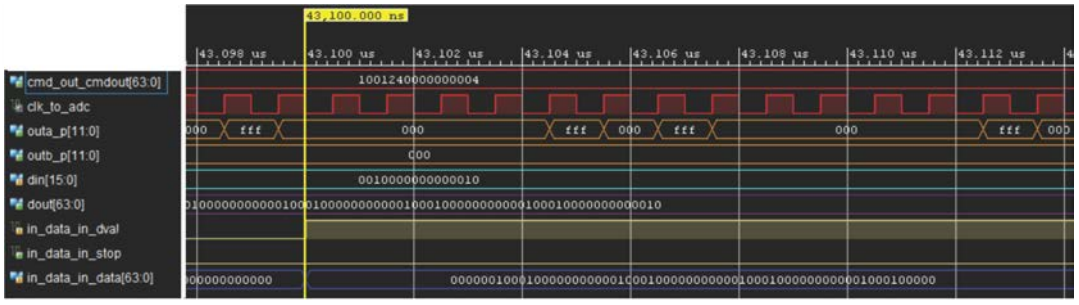


FIGURE 4.6: Testbench behavioural signals.

Chapter 5

Experimental Testing with waveform generator

This chapter describes the validation of the A/D conversion and the modified firmware that allows it.

In the first place, section 5.1 describes the network connection between the A/D conversion system and an external computer. Then the configuration setup implemented in the ZC702 Control Board and in the FMC112 board is detailed in section 5.1.1.
In order to obtain an adequate measurement system, the capability of correcting the offset is needed. This function and its working principles are explained in section 5.2. In addition to this, in section 5.2.1 it it is proposed a deeper analysis of DAC *LTC2656*, the component managing the offset correction.
The offset correction test is performed with the variation of the DAC output and it is analysed in section 5.3.1. This test is executed in order to evaluate the relationship between the input [micro-processor units] and the output signal [V] of the DACs.
Furthermore, section 5.3 shifts the attention to the tests performed with a waveform generator. First, the test design is described at the beginning of the section 5.3 and then the variation of a voltage input test and the response to a voltage step test are shown in section 5.3.2 and in section 5.3.3, respectively.
Finally, section 5.4 reports conclusive remarks on the waveform generator tests.

5.1 Data logging system

The Data Logging network is shown in Figure 5.1. The diagram illustrates the core of the physical design of the A/D conversion system. All the tests in this chapter and in the next one are based on this design. The FMC112 board is connected with the ZC702 control board by the FMC connector LCP1, as previously explained in chapter 2.

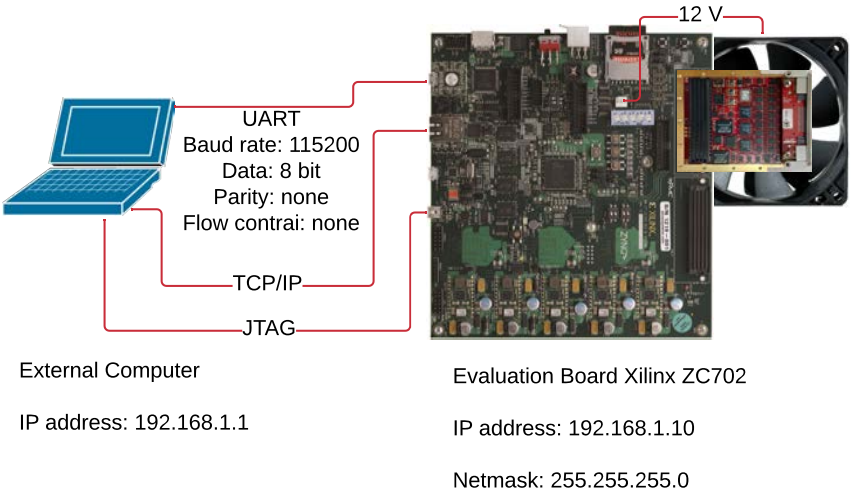


FIGURE 5.1: Data Logging Diagram.

The FMC connector pins are configured in order to implement [17]:

- 42 differential pairs channels for output data from *LTC2175* ADCs (clock, frame, conversion data output);
- 8 singe-ended channels for controlling of the FMC112 board;
- 2 single-ended channels for I/O power status signals;
- 2 single-ended channels for I2C protocol-based voltage and temperature signals in order to perform status monitoring for the FMC112 board (clock and data channels, respectively).

The FMC112 board, according to [17] and [22], requires a air flow cooling for standalone operation. A 12 V fan arranged under the ADC board ensures to obtain an

airflow of 300 LFM minimum. The fan is power supplied by a 12 V fan power-supplier positioned in the ZC702 control board [11].

The ZC702 control board is connected to an external computer for three main purposes:

1. Performing the Zynq-7020 PL and PS configuration by the upload of the bitstream (a file that contains the programming information for an FPGA) and of the C codes, respectively.
2. Monitoring the connection status;
3. Transmission of sampling data and commands between the external computer and the Control Board.

The PS and PL configuration is obtained by the JTAG connection. This connection type allows the download of the bitstream into a volatile memory in the FPGA, in order to program the logic cells. Furthermore, it transmits the C codes needed by the two ARM cores.
The UART connection manages the status signals transmission between the external computer and the ZC702 control board. This connection is characterised by the following setup:

- **Baud rate**:115200
- **Data length**: 8 bit
- **Parity bit**: none
- **Flow control**: none

The transmission of sampling data and commands is performed by a TCP/IP-based connection. According to TCP/IP architecture, IP addresses are assigned to the external computer and to the Control Board, 192.168.1.1 and 192.168.1.10, respectively. In order to identify which part of the address corresponds to the Network ID and which part to the Host ID, a Netmask is defined: 255.255.255.0. More information on the TCP/IP communication protocol is described in [34].

5.1.1 Configuration ZC702-FMC112

The bitstream and the C codes are uploaded to the Control Board by the external computer through the data logging network described in section 5.1. As a consequence of this procedure, the PS and PL are set up and ready ~~to~~for receiving commands in order to acquire data. Data acquisition is managed by the external computer that control the A/D conversion system too. An application, namely Fmc116APP.exe, has been created by Microsoft Visual Studio in order to set up the data acquisition setup. This application carries out the following main setups:

- Number of burst;
- Number of samples per burst;
- Sampling Frequency;
- Offset regulation by DACs;
- Configuration of the data routers;
- Display FMC116 diagnostics;
- Arming and triggering of the ADCs;
- Save the acquired data in a .txt file in binary or ASCII mode;
- Setting CPLD registers.

5.2 Offset Correction

As previously described in section 2.2, the FMC112 board accepts an input voltage range of 2 V_{P-P}. In order to adapt the input voltage to the accepted input range or to correct any offset error of the measurement system, an offset correction is needed. This is implemented in the FMC112 board for all ADC inputs signals. Each input signal, represented as V_{input} in Figure 5.2, is subtracted to the $V_{output\,DAC\,circuitry}$ signal, produced by the DAC circuitry of Figure 5.3, in order to perform the offset

correction. The input circuit is DC coupled using an *ADA4938* ADC driver [18]. The gain of the ADC driver is set to 1 to maximize the input bandwidth. As a consequence of the connection between the *LTC2175-14* ADC and the *ADA4938* outputs, a polarity twist is performed and therefore the ADCs outputs are inverted. A software correction will be applied in the future works.

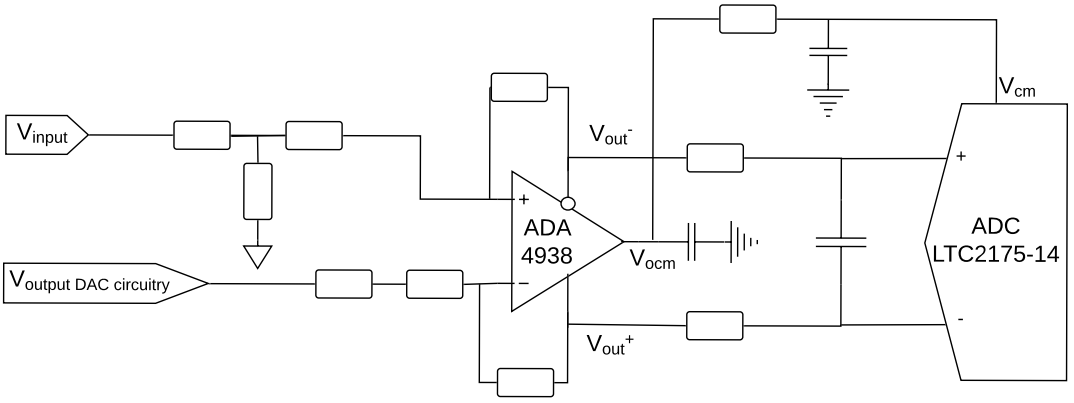


FIGURE 5.2: ADC Circuitry

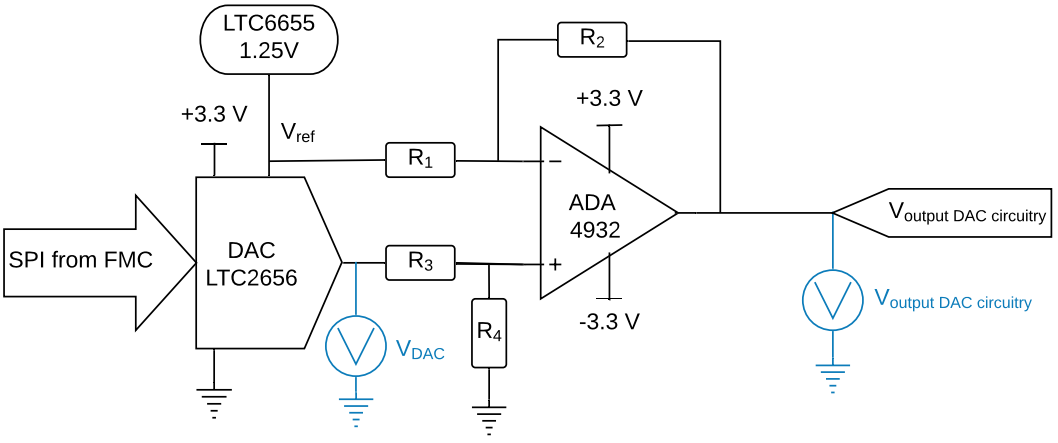


FIGURE 5.3: DAC Circuitry

The DAC circuitry is shown in Figure 5.3. Its principal element is Linear Technology *LTC2656* DAC [20], which is characterised by a V_{DAC} output swinging from 0 to $2 * V_{ref}$. This circuitry uses a $V_{ref} = 1.25$ V. The DAC output is:

$$V_{DAC} = DAC_{input} * \frac{2.5}{2^{16}} \ [V], \tag{5.1}$$

where the DAC_{input} is an integer number in the range $[0, 2^{16} - 1]$ that is sent to the FMC112 board by the ZC702 control board via SPI. The V_{DAC} and the V_{ref} are the inputs of a differential amplifier, which tries to minimize the common mode gain imposing:

$$\frac{R_2}{R_1} \approx \frac{R_4}{R_3} \tag{5.2}$$

Adding the relation:

$$R_2 = R_1 \tag{5.3}$$

the $V_{output\,DAC\,circuitry}$ is:

$$V_{output\,DAC\,circuitry} = V_{DAC} - V_{ref}\ [V] \tag{5.4}$$

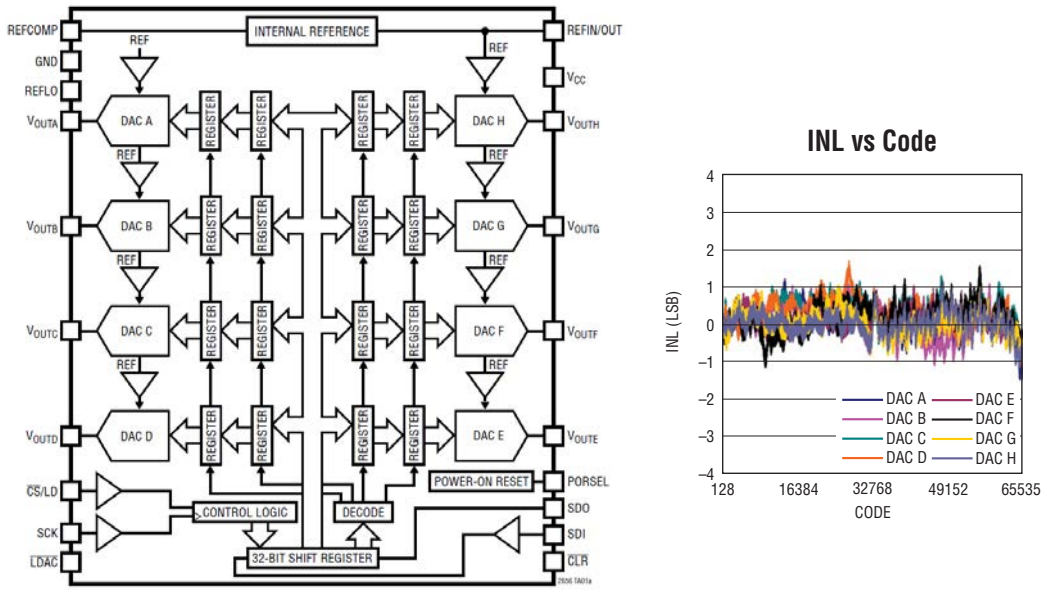
The DAC circuitry output can perform an offset correction that can swing from -1.25 V to +1.25 V. The *LTC2656* is a 16-bit DAC, so its voltage resolution is equal to:

$$\Delta V_{DAC} = \frac{2.5\,V}{2^{16}} = 38.1\,\mu V \tag{5.5}$$

This value corresponds to the voltage step related to the changing of a single bit in the DAC input.

5.2.1 DAC LTC2656

The FMC112 board contains 2 *LTC2656* DAC chips as the key components of the offset correction [20]. The *LTC2656* is a 8 channels, 16-bit DAC. It is characterised by a full scale output of 2.5 V. The *LTC2656* Block Diagram and DAC error estimations are shown in Figure 5.4a and in Figure 5.4b, respectively.
The Maximum Integral Non Linearity (INL) error is ±4 Least Significant Bit (LSB).



(A) (B)

FIGURE 5.4: LTC2656 Block Diagram 5.4a and the DAC error estimations 5.4b [20].

The DAC is managed by a SPI 4-wire serial interface and it accepts a clock up to 50 MHz. The main characteristics of this DAC chip are resumed in Table 5.1.

TABLE 5.1: LTC2656 main characteristics [20].

SYMBOL	PARAMETER	CONDITIONS	VALUES	UNITS
Resolution			16	bits
V_{OUT}	DAC Output Span	1.25 V Reference	0 to 2.5	V
t_S	Settling Time		4.2	μ s

The DAC control is performed by writing into the CPLD registers, as previously described in section 2.2.2. The data present in these registers are related to a specific task. These data are composed by the command and address code shown in Table 5.2 and Table 5.3, respectively.

TABLE 5.2: DAC command codes [20].

Command				
*n=address, see 5.3.				
A3	A2	A1	A0	
0	0	0	0	Write to Input Register n
0	0	0	1	Update (Power Up) DAC Register n
0	0	1	0	Write to Input Register, Update (Power Up) All
0	0	1	1	Write to and Update (Power Up) n
0	1	0	0	Power Down n
0	1	0	1	Power Down Chip (All DACs and Reference)
0	1	1	0	Select Internal Reference (Power-Up Reference)
0	1	1	1	Select External Reference (Power-Down Reference)
1	1	1	1	No operation

TABLE 5.3: DAC address codes [20].

Address(n)				
A3	A2	A1	A0	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

Table 5.4 described the relation between DAC outputs and the relative input channel. It is possible to notice that only 4 DAC outputs are used in the second DAC chip. Offset control is performed for each individual ADC channel.

TABLE 5.4: Offset control [17].

LTC2656 Channel	**LTC2656 1st chip**	**LTC2656 2nd chip**
VOUT_A	A/D 08	A/D 00
VOUT_B	A/D 09	A/D 01
VOUT_C	A/D 10	A/D 02
VOUT_D	A/D 11	A/D 03
VOUT_E	A/D 04	
VOUT_F	A/D 05	
VOUT_G	A/D 06	
VOUT_H	A/D 07	

The ideal transfer function through with the input k [μP] and the output [V] of the DAC are related is the following:

$$V_{DAC(IDEAL)} = \left(\frac{k}{2^{16}}\right) 2\,(V_{ref} - V_{ref-low}) + V_{ref-low} \;\; [V] \tag{5.6}$$

where k is the decimal equivalent of the binary DAC input code and its value can vary in the range $[2^{15}, 2^{16} - 1]$.
The values of the reference voltage values are:

$$V_{ref} = 1.25\,V \tag{5.7}$$

$$V_{ref-low} = 0\,V \tag{5.8}$$

Therefore, integrating the values of (5.7) and (5.8) in (5.6):

$$V_{DAC(IDEAL)} = 2.5\left(\frac{k}{2^{16}}\right) [V] \tag{5.9}$$

The 5.9 is the ideal transfer function and, in the following tests, it will be considered also for the real case. This is due to the impossibility to test directly the DAC outputs related to a changing of the DAC binary input. This impossibility derives from the small electronic parts in use and the possibility of accidental short circuits.

5.3 Testing with Waveform Generator

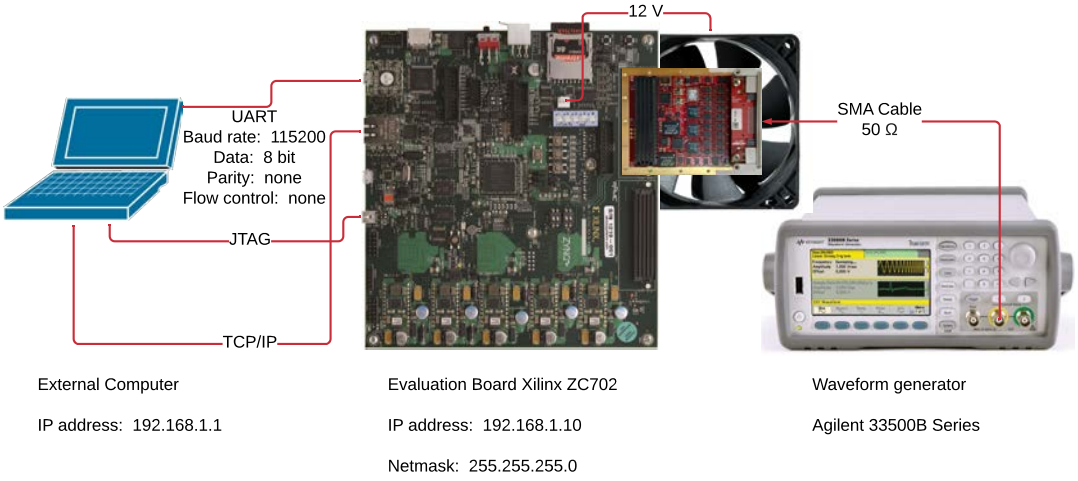


FIGURE 5.5: Network Diagram.

The setup previously described in Figure 5.1 is used as core for this experimental test. In Figure 5.5 it is depicted the waveform generator test design. As shown, the Agilent 33500B Series Waveform Generator [35] is added to this setup. The waveform generator is connected to the SMA connector of the FMC112 board by a BNC cable. The BNC cable is characterised by a 50 Ω impedance.

This is the experimental setup used in three tests for the A/D conversion:

- The first test has the purpose to find the offset error that affects the ADC conversion system and it is reported in section 5.3.1.
- The second one consist in sampling with a constant variation of analog voltage input. This test is used to calculate the real ADC input-voltage range and the conversion ratio between the input signal [V] and the output value [μP] and it is described in section 5.3.2.
- The third one, described in section 5.3.3, evaluates the time response of the A/D conversion system to a voltage step.

The setups used in these tests are the following:

$$N^o\, Burst = 1 \tag{5.10}$$

$$N^o\, Samples\, per\, Burst = 32768 \tag{5.11}$$

$$f_s = 125\, MHz \tag{5.12}$$

5.3.1 DAC Variation

As explained in section 5.2 the DAC circuitry is connected in parallel with the ADC circuitry. In order to conduct a first analysis of the DAC circuitry and of the relation between the inputs [V] and the ADC_{ouput} $[\mu P]$, the voltage input signal of the ADC *LTC2175-14* is stimulated with the DAC output variation. The first purpose of this test is to evaluate the offset error, namely V_{error}, which affects the A/D conversion system. This analysis is accomplished applying on the waveform generator a:

$$V_{input} = 0\, V \tag{5.13}$$

In order to determine this error, the DAC output is changed until $ADC_{output} = 0\, \mu P$ is reached.

After some attempts, it has been found that a $DAC_{input} = 33274\ \mu P$ corresponds to $ADC_{output} = 0\, \mu P$.
This DAC_{input} value corresponds to a $V_{OUTPUT\, DAC\, CIRCUITRY} = 19\, mV$. Therefore the A/D system is affected by an offset error equal to:

$$V_{error} = -19\, mV \tag{5.14}$$

As a consequence, it is possible to write a first equation that relates the DAC inputs to the ADC outputs. This equation is valid for a $V_{input} = 0\, V$.

$$ADC_{output} = m_{DAC} * (V_{DAC\, OUTPUT\, CIRCUITRY} + V_{error})\ [\mu P] \tag{5.15}$$

It is possible to evaluate an ideal m_{DAC} value:

$$m_{DAC(IDEAL)} = \frac{2^{14}}{V_{P-P}} = \frac{2^{14}}{2} = 8192 \ \frac{\mu P}{V} \tag{5.16}$$

In order to find the real m_{DAC} value and the ADC real input voltage range, a total range V_{DAC} linear variation is performed by the modification of DAC_{input} value in the range $[0, 2^{16} - 1]$. For each DAC_{input} value, and by always keeping $V_{input} = 0\,\text{V}$, a number of consecutive 32768 samples were taken and all their relative ADC_{output} values were recorded. Then, the average $ADC_{output,avg}$ value was obtained for each of the DAC_{input} value. The relation between DAC_{input} and $ADC_{output,avg}$ is shown in Figure 5.6. In the chart it is possible to see that the FMC112 board follows a linear conversion, as it is required.

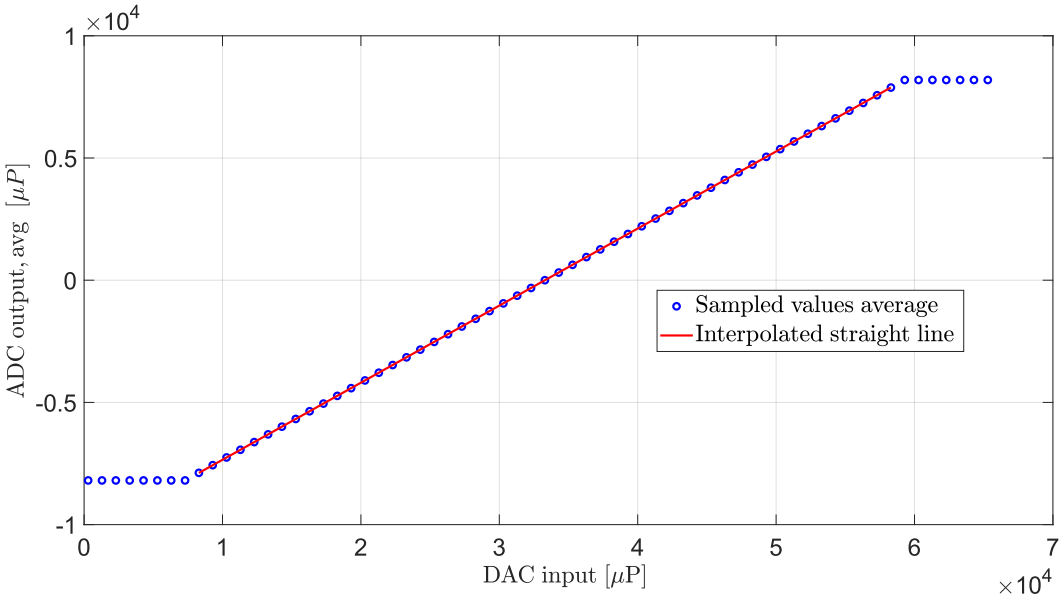


FIGURE 5.6: The ADC_{output} average value of 32768 samples as a function of different DAC_{input} values.

By further analysis it has been found that a saturation of ADC_{output} occurs just before the ±1 [V] ADC input range. As a consequence of this limitation, the ideal $m_{DAC(ideal)}$ calculated in 5.16 it can not be used anymore. As a result of the data analysis of the ADC_{output} values during the linear variation of the DAC_{ouput}, the sampled average values in the non-saturation zone has been interpolated in order to evaluate a straight line equation. The angular coefficient of this straight line is the

coefficient that relate the DAC_{input} to the ADC_{output}. It is possible to make explicit m_{DAC} through the use of 5.15 and the calculated angular coefficient is:

$$m_{DAC} = 8253 \, \frac{\mu P}{V} \tag{5.17}$$

Furthermore, by additional data analysis, for each of the the DAC_{input} values, a standard deviation value σ was obtained with the 32768 acquisitions, assuming a Gaussian error distribution. In Figure 5.7 it is shown the standard deviation along the ADC input range during the DAC_{input} variation. In red it is depicted the calculated global standard deviation average $\sigma_{avg} = 2.357 \, \mu P$.

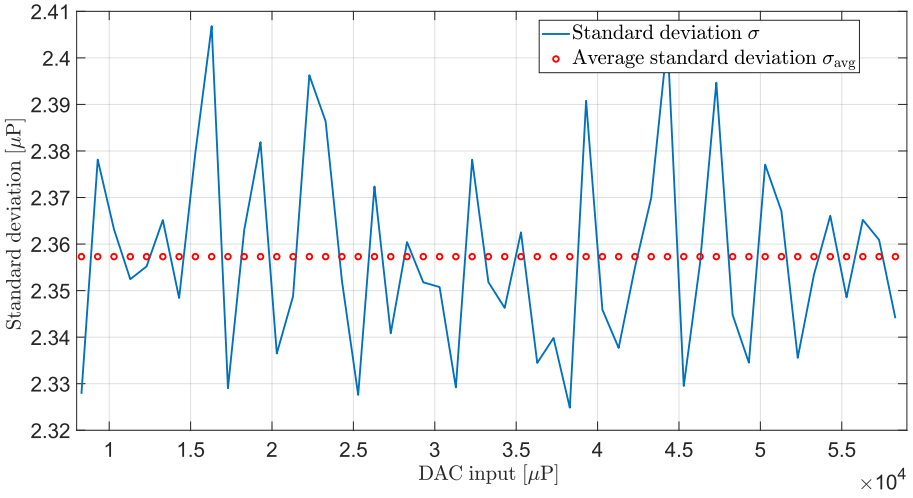


FIGURE 5.7: σ and σ_{avg} for all the input range.

Finally, the histogram in Figure 5.8 shows the values trend after the measurement with a $V_{input} = 0 \, V$ and a $DAC_{input} = 48294 \, \mu P$. In red it is reported the gaussian curve interpolating the histogram. Vertical lines with different colours represent different ranges, due to the standard deviation multiples, and they are underlined by light blue, green and black lines. The magenta line represents the ADC_{output} average that is equal to 4730.387 μP. Standard deviation σ is equal to 2.345 μP.

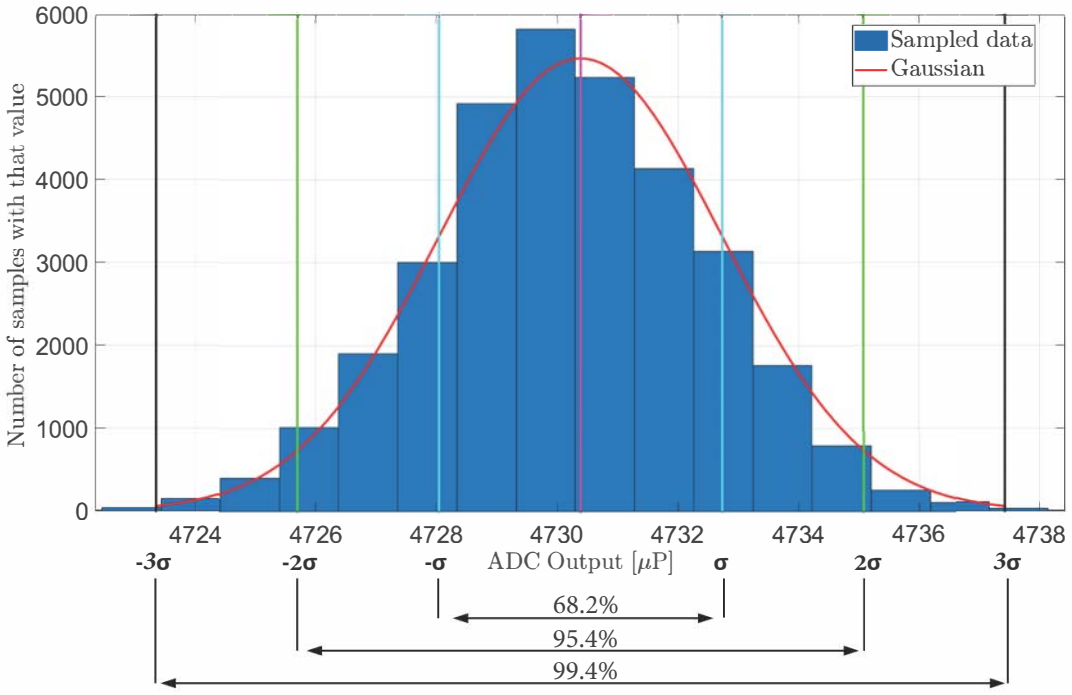


FIGURE 5.8: Distribution of ADC_{output} values with $DAC_{input} = 48294\ \mu P$ and its respective average value and standard deviation ranges.

5.3.2 Voltage Input Linear Variation

The second test that has been performed is the V_{input} variation. This experiment has the purpose of determining the conversion rate between the voltage input signal and the ADC_{output}. Firstly, the offset error has been corrected in order to avoid shifted results. Then, a V_{input} variation has been applied by the *Agilent 33500B Series*[35] waveform generator in the range from -1.1 V to 1.1 V. Figure 5.9 shows the results of the sampled values average, each measurement has a 100 mV variation.

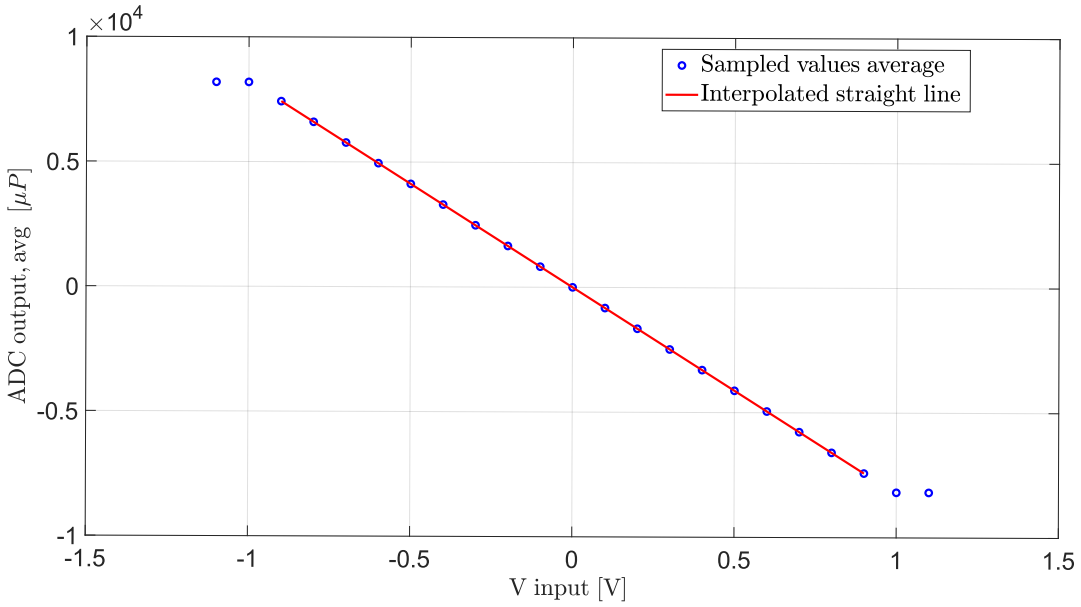


FIGURE 5.9: V_{input} Variation

The ADC saturation appears just before the ADC input limit range [-1 V,1 V], as described in the previous test in section 5.3.1. Each point has been interpolated onto a straight line which permits to evaluate the I/O relationship.

For this test the relation between input and output is the following:

$$ADC_{output} = m_{input} * V_{input}\ [V] \tag{5.18}$$

Where $m_{input(IDEAL)}$ can be estimated in this way:

$$m_{input(IDEAL)} = \frac{2^{14}}{V_{P-P}} = \frac{2^{14}}{2} = 8192\,\frac{\mu P}{V} \tag{5.19}$$

The consequence of the saturation the equation 5.19 isn't valid. The m_{input} coefficient obtained by the interpolation is :

$$m_{input} = 8250\,\frac{\mu P}{V} \tag{5.20}$$

It is comparable with the coefficient calculated in 5.17.

Similarly to the previous test, by additional data analysis, for each of the the V_{input} values, a standard deviation value σ was obtained with the 32768 acquisitions, assuming a Gaussian error distribution. In Figure 5.10 it is shown the standard deviation along the ADC input range during the V_{input} variation. In red it is depicted the calculated global standard deviation average $\sigma_{avg} = 2.349\,\mu P$. This result is comparable to the one calculated in the previous test.

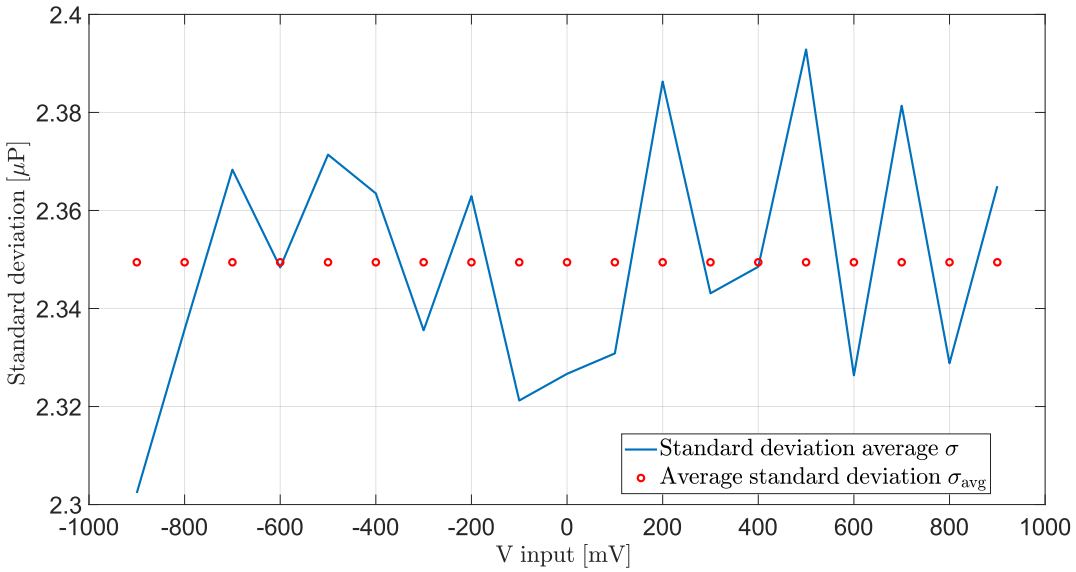


FIGURE 5.10: σ_{avg} for all the input range

Finally, in Figure 5.11 it is depicted a histogram reporting the values trend when the measures are done with a $V_{input} = -500\,mV$ and with the offset error compensation. The gaussian curve, depicted in red, interpolates the values of the histogram. The different ranges due to the standard deviation multiples are underlined by light blue, green and black lines. The magenta line represents the ADC_{output} average that is equal to 4125.325 [μP]. Standard deviation σ is equal to 2.371 μP.

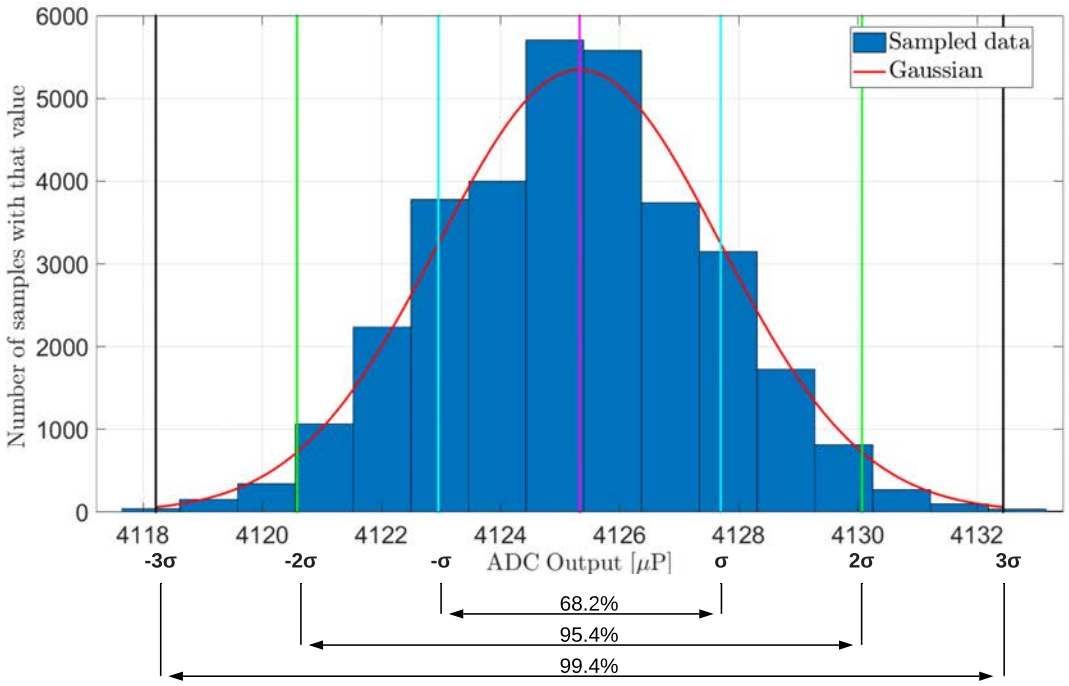


FIGURE 5.11: Distribution of ADC_{output} values with $V_{in} = -500\,mV$ measurement

5.3.3 V_in Square Wave

The aim of the last test was to to evaluate the time of the response of the A/D conversion system to a voltage step. The waveform generator has been set up to produce a voltage step from 0 mV to 900 mV. The results of this test are depicted in Figure 5.12. The output of the A/D conversion is negative quasi-step because, as mentioned in section 5.2, the FMC112 acquisition system hardware contains a sign inversion. The evaluation is performed with the maximum sampling frequency $f_s = 125\,MHz$. The rise-time obtained by this test is comparable with the one reported in the Agilent 33500B Series Waveform Generator datasheet [35]. In conclusion, since the rise time of the A/D conversion system is smaller compared to the sampling period this does not allow its evaluation.

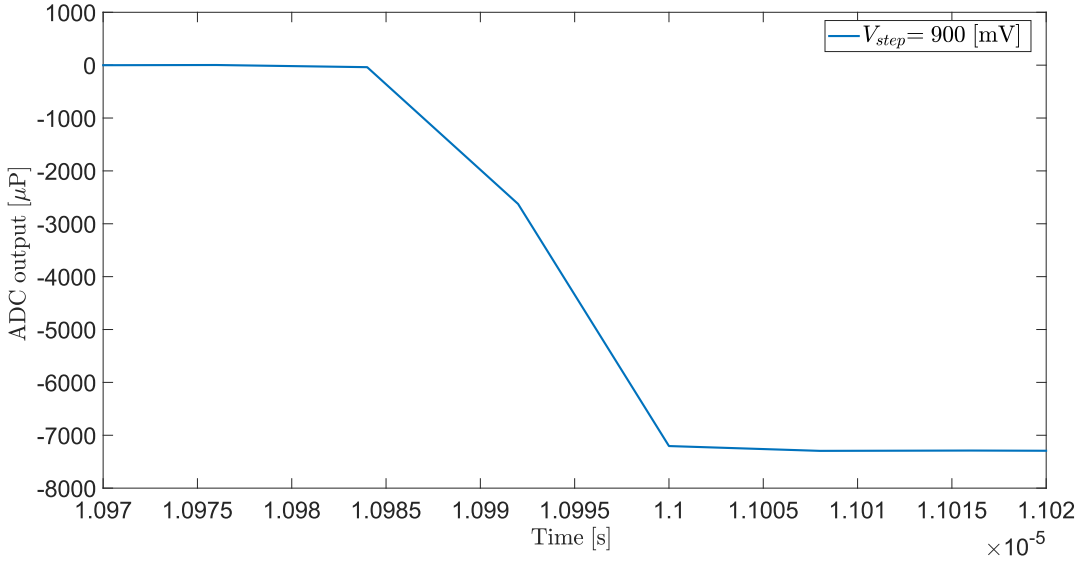


FIGURE 5.12: ADC output for a Voltage Step

5.4 Remarks of the results achieved with waveform generator

In conclusion, the principal results of this chapter are resumed. The equation that relates the input value [V] to the output value [μP] is:

$$ADC_{output} = m_{in-out} * (V_{DAC\,OUTPUT\,CIRCUITRY} + V_{error} - V_{input})\ [\mu P] \quad (5.21)$$

where $m_{in-out} = 8252\ \frac{\mu P}{V}$, $V_{error} = 19\,mV$ and $V_{DAC\,OUTPUT\,CIRCUITRY}$ is the signal explained in 5.9 The input voltage range of the experimental setup is minor than the one described in the datasheet, but it does not influence significantly the resolution. Moreover, the A/D conversion is linear all along the input voltage range. The σ_{avg} of the A/D conversion system has been estimated equal to 2,355 μP. The system response times are negligible for the purpose of the thesis.

Chapter 6

Experimental Testing with the electric motor

This chapter describes the second test used to validate the A/D conversion system with the modified firmware. This is done by comparing the FMC112 A/D conversion output with the acquisition by means of an oscilloscope. In the first place, section 6.1 reports the connection between the A/D conversion system, an induction motor and the oscilloscope.
Then, section 6.1.1 gives a description of the main datasheet characteristics of the oscilloscope used for this evaluation test.
Section 6.2 focuses the attention to the current and voltage measurement approach. Section 6.3 examines the induction motor voltage and current sampled by the FMC112-based A/D conversion system. First, section 6.3.1 shows the oscilloscope results and then, section 6.3.2 compares them with the FMC112-based A/D conversion system results. Finally, section 6.4 underlines the high-frequency phenomena present in the sampled data, which can be used for the purposes described in section 1.1.

6.1 Experimental setup with the oscilloscope

The experimental setup in Figure 5.1 is used as a core for the extended one represented in Figure 6.1. All the experimental tests described in this chapter are based

on this design.

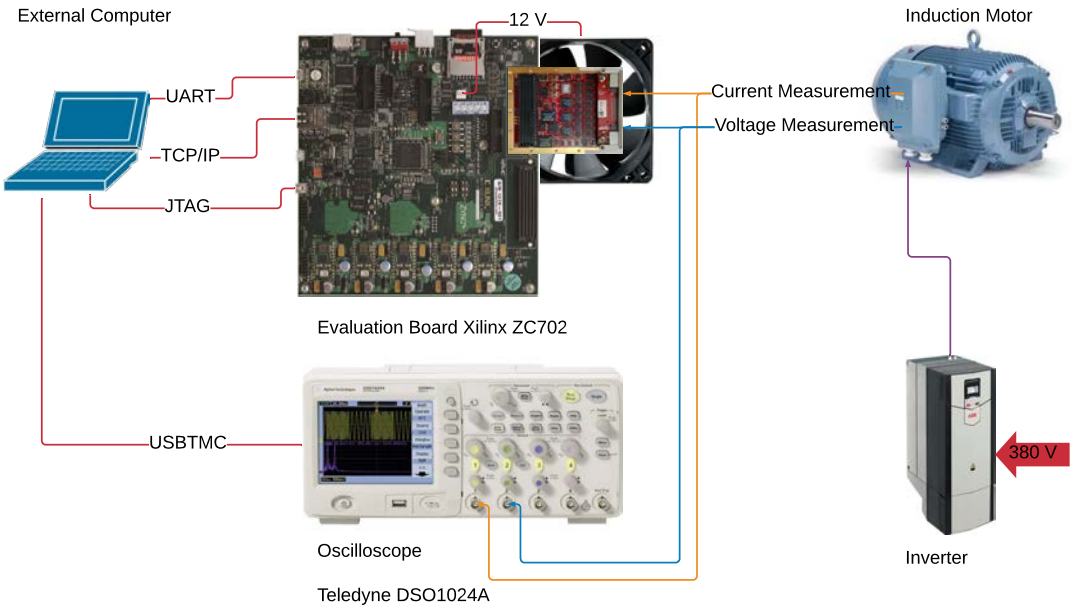


FIGURE 6.1: Elaborate experimental design.

An electric induction motor is used for these tests. The electric motor is supplied by a three-phase inverter connected to the grid.
One phase current and one phase voltage are measured by a Rogowski coil and a voltage probe. The probes outputs are connected to the two acquisition systems, the oscilloscope and the FMC112-based A/D system, by four BNC cables. These BNC cables are characterised by a 50 Ω impedance.

The external computer has been used to plot the sampled data and to control the FMC112-based A/D conversion system and the oscilloscope.

These measurements are performed on a not mechanically loaded electric motor since the phenomena explained in section 1.1 are not related to the current amplitude.

6.1.1 Osciloscope Agilent DSO1024A

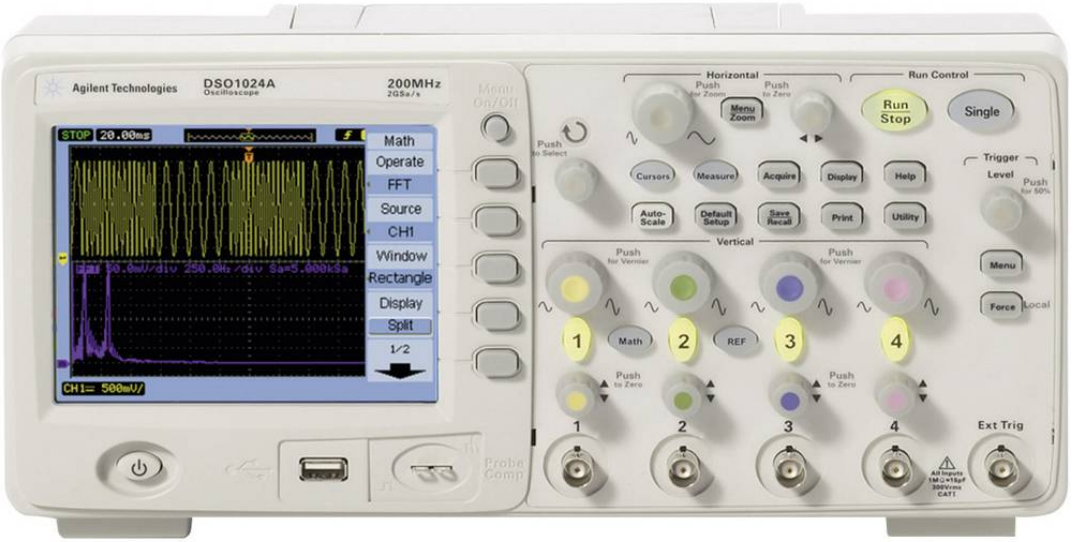


FIGURE 6.2: Osciloscope Agilent DSO1024A.

The following tests are performed using a 200 MHz bandwidth oscilloscope, the Agilent DSO1024A [36], shown in Figure 6.2. It is characterised by a maximum sample rate of 2 GSa/s and a maximum memory depth of 10000 samples. It has been connected to an external computer for a remote instrument control by an USB interface. A comparison of the main characteristics of the experimental sampling system and the oscilloscope are detailed in Table 6.1.

TABLE 6.1: FMC112 board and oscilloscope characteristics comparison.

	FMC112	**Agilent DSO1024A Oscilloscope**
Voltage range	±1	±5
bits	14	8
Max sampling frequency	125 MHz	2 GHz
Max n° samples	32768	10000

Due to the larger number of bits, the FMC112 is characterised by a better resolution than the oscilloscope. For example, with the same input voltage range $2\,V_{pp}$, the oscilloscope has a resolution equal to $Res_{oscilloscope} = \frac{2\,[V]}{2^8\,[\mu p]} = 7.8\,\frac{mV}{\mu p}$. Anyhow, the

input voltage range can be modfied and the resolution could improve. Instead, the FMC112 has a fixed resolution due to the constant input range value assigned, and it is equal to $Res_{FMC112} = \frac{2[V]}{2^{14}[\mu p]} = 122\,\frac{\mu V}{\mu p}$.

6.2 Current and voltage measurements introduction

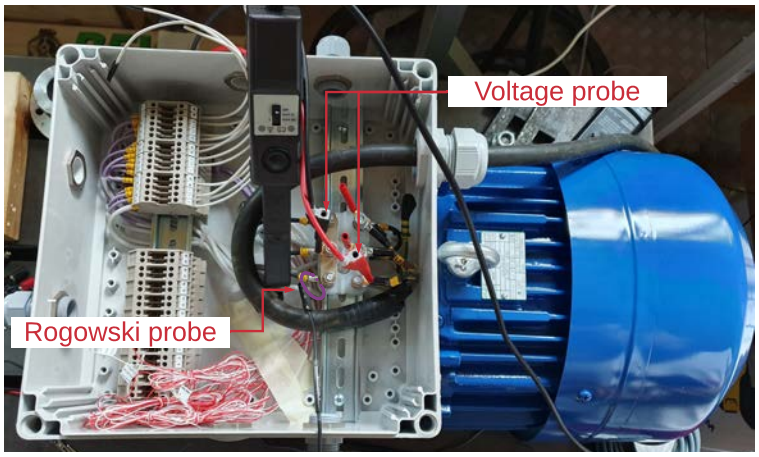


FIGURE 6.3: Probes connection.

Figure 6.3 represents the connection of the probes to an electric induction motor. A voltage probe is connected in order to measure the voltage of the phase a with respect to the wye point of the motor. It has been used a *GW Instek GDP-050* voltage probe, with a bandwidth of 50 MHz. Then, the *PEM CWT Rogowski* current probe, having a wide bandwidth of 20 MHz, was used to measure phase a current.

6.3 Current and voltage measurements

6.3.1 Oscilloscope measurements

The current and voltage probes are connected by BNC cables to the input channels of the oscilloscope. The oscilloscope is set up with a 125 kHz sampling frequency.

Figure 6.4 shows an entire period of the current and the voltage waveform. It depicts the trend of the waveforms in a period of 8 ms range.

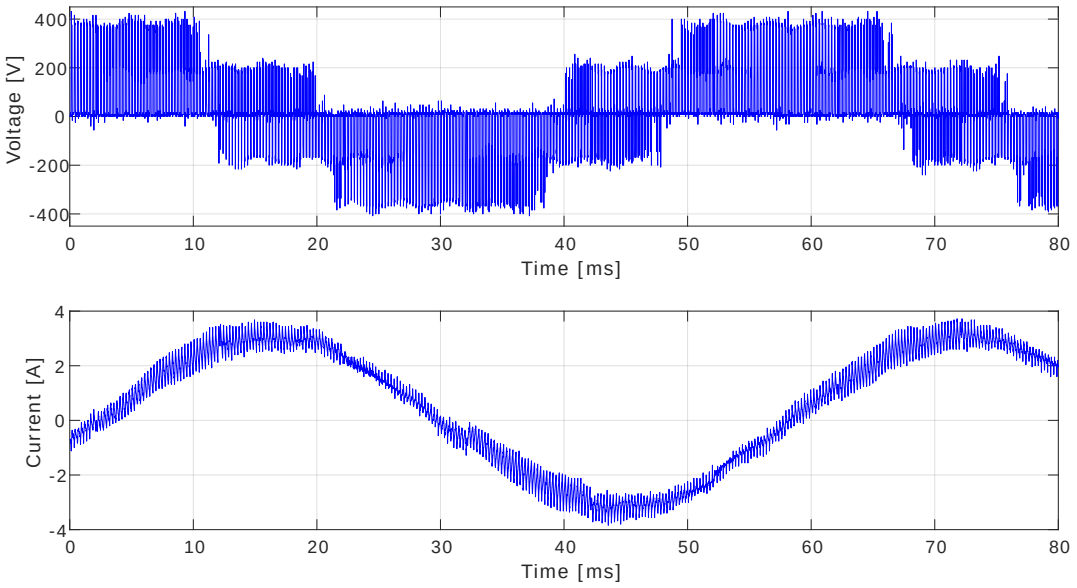


FIGURE 6.4: Scope measurements at 125 kHz by the oscilloscope, 80 ms time range.

Figure 6.5 focused the attention to the current and voltage PWM ripple zooming the previous sampled waveforms in a 3 ms window.

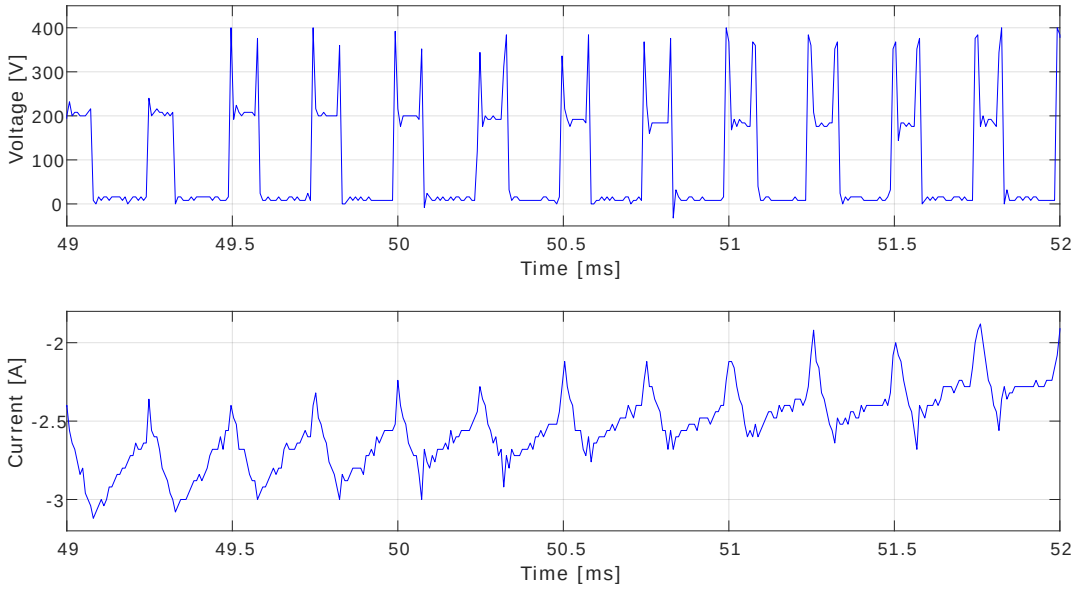


FIGURE 6.5: Scope measurements at 125 kHz by the oscilloscope, 3 ms time range.

Then, in order to analyse the switching phenomena, the oscilloscope has been set up with a 250 MHz sampling frequency.

Figure 6.6 underlines the current high-frequency oscillation of approximately 2 MHz in a 40 μs time window.

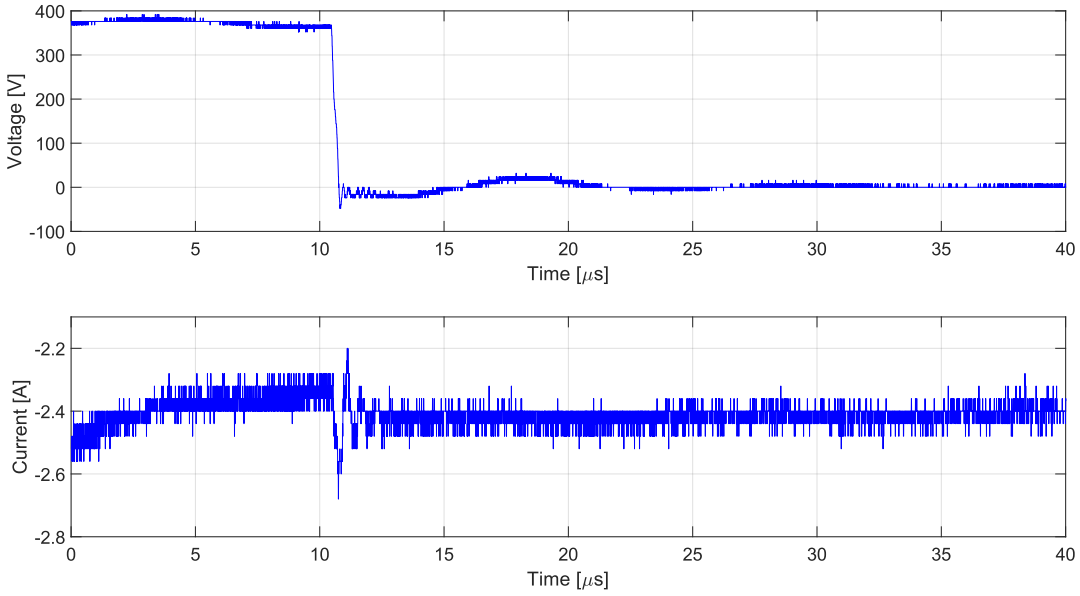


FIGURE 6.6: Scope Measurements at 250 MHz by the oscilloscope, 40 μs time range.

In order to estimate the resolution of the oscilloscope, Figure 6.7 shows a further zoom into the previous sampled waveforms with a time window of 3 μs.

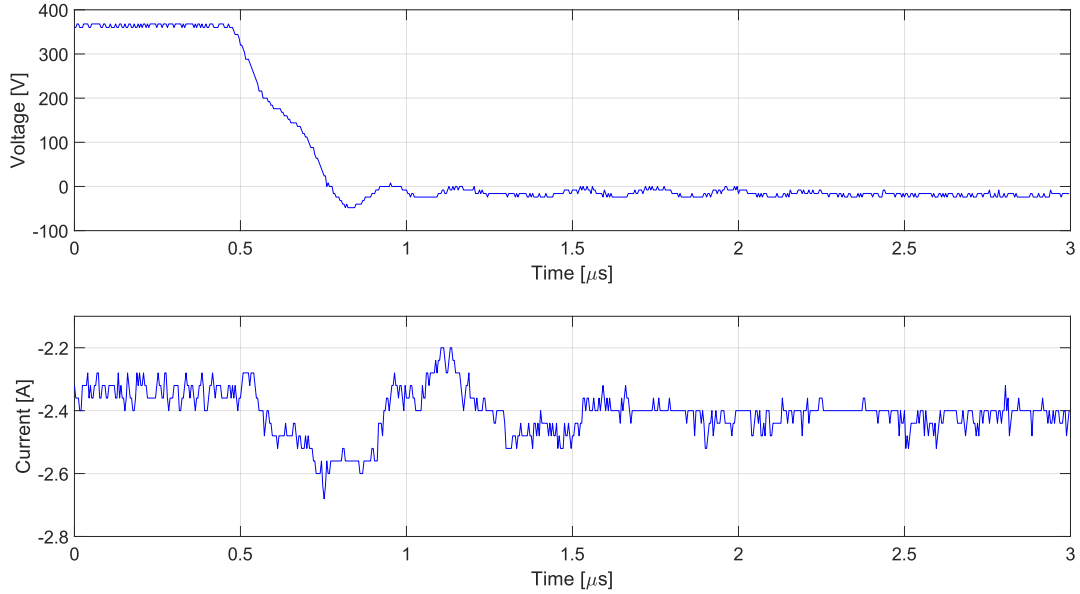


FIGURE 6.7: Scope Measurements at 250 MHz by the oscilloscope, 3 μs time range.

The current resolution of the oscilloscope has been estimated to be approximately $0.04\,A$, while the voltage resolution of the oscilloscope has been estimated to be approximately $8\,V$.

6.3.2 FMC112-based A/D conversion system measurements

Similarly to the oscilloscope measurements, current and voltage measurements have been performed by the FMC112-based A/D conversion system. Current probe and voltage probe are connected by BNC cable to the input channels of the FMC112 board. The experimental system has been set up by software with the following setup:

- N° samples = 32768
- Sampling frequency = 50 MHz

Figure 6.8 shows the current high-frequency oscillation in a $40\,\mu s$ time window. This figure is comparable with Figure 6.6 sampled by the oscilloscope.

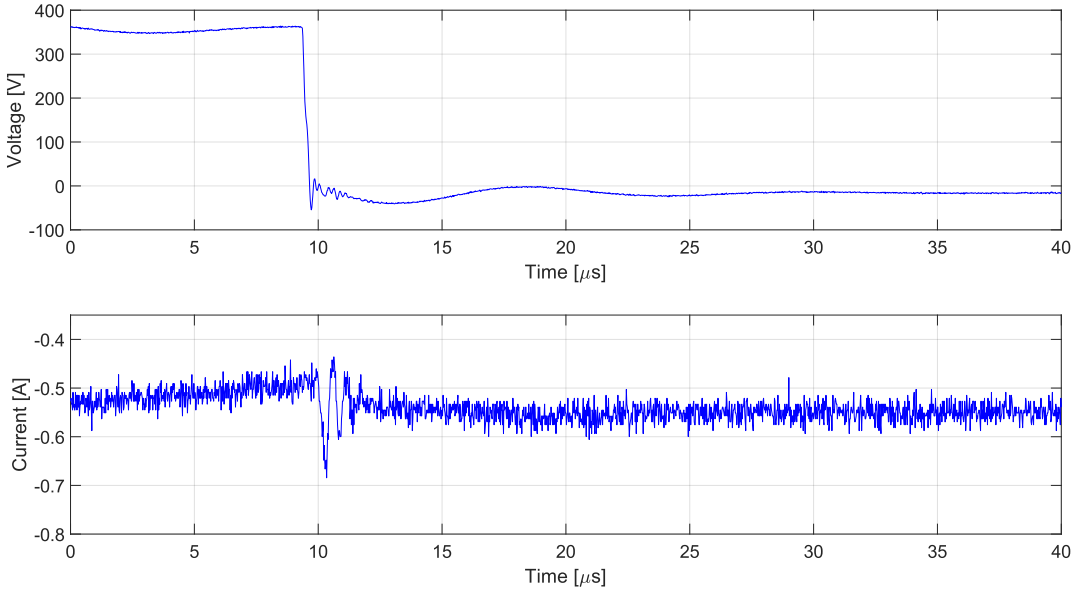


FIGURE 6.8: Scope Measurements at 50 MHz by FMC112 board, $40\,\mu s$ time range.

In order to measure the resolution of the FMC112-based A/D conversion system, Figure 6.7 zooms the waveforms in a $3\,\mu s$ window. This figure is comparable with Figure 6.7 sampled by the oscilloscope.

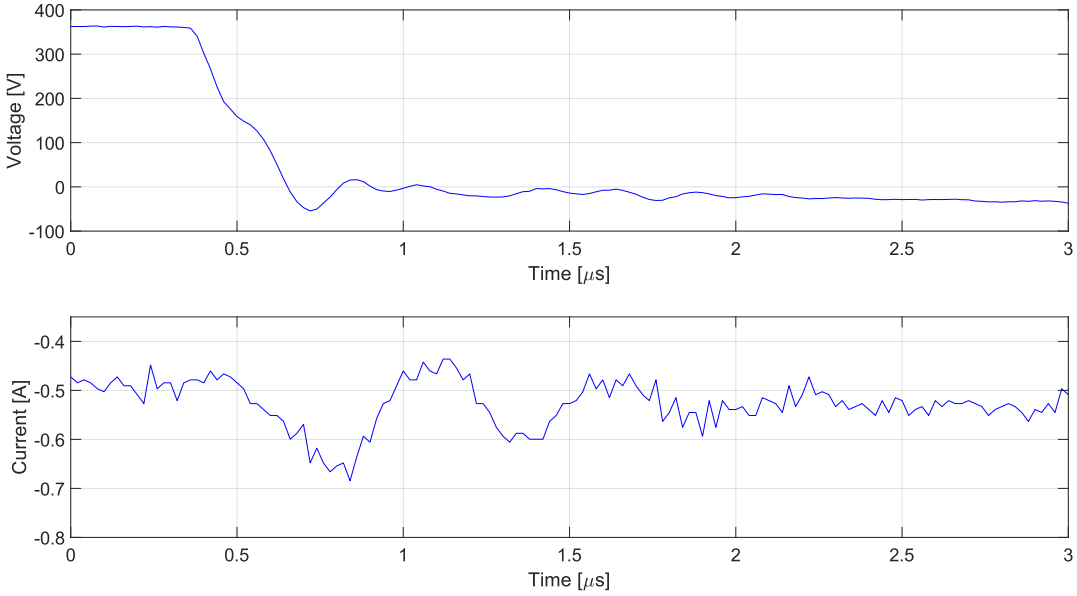


FIGURE 6.9: Scope Measurements at 50 MHz by FMC112 board, $3\,\mu s$ time range.

The current and voltage waveforms of Figure 6.8 and Figure 6.9 are manually aligned because the triggers of the different ADCs are not yet aligned. The current resolution of the described experimental setup is approximately $0.01\,A$, while the voltage resolution of the experimental setup has been estimated to be approximately $2\,V$.

6.4 Experimental remarks

These measurements are performed in an ideal condition for the oscilloscope due to the no-load condition. In this condition the phase current has the minimum value and the resolution of the oscilloscope is maximum. Then, when a load is connected to the electric motor, the current value increase and the resolution of the oscilloscope has a remarkable degradation. On the other hand, the developed A/D setup has a fixed resolution due to the fixed input voltage range accepted by the FMC112 board. This input voltage range is set to $2\,V_{P-P}$.

In conclusion, according to this final consideration, the experimental system has a better resolution in all the possible situations.

Chapter 7

Future Work

The A/D experimental conversion system designed in this thesis project is part of a drive control system with oversampling capabilities, as explained in the beginning of chapter 2.

Accurate control algorithms requires that the sampling of the currents is sampled at the beginning of the PWM period. Thus, the trigger signal has to be programmed to reach this purpose.

Moreover, oversampling capability is required for the condition monitoring purpose. The oversampling of current measurements has to be performed once a switching phenomenon appears. Thus, the acquisition system switches from a kHz-range sampling to a MHz-range one. This change will be performed in the FPGA. The oversampled data will be saved in memory blocks and then routed by the second ARM core to an external computer by TPC/IP protocol. The condition monitoring method based on the oversampled currents will be implemented in the external computer.

Finally, a signal conditioning PCB should be realised, in order to filter and amplify the outputs of voltage and current probes, so to be adequate for the FMC112 board input range.

Chapter 8

Conclusions

The work allows to obtain a experimental system characterised by a MHz-range sampling capability and an excellent A/D conversion sensitivity.

The FMC112 was used as A/D conversion board because it is characterised by a maximum sampling frequency of 125 MHz with a resolution of 14 bits. The firmware of the FMC112 board provided by the manufacturer limited a general manipulation of the IP blocks. Thus, it has been re-designed in order to reach a general firmware characterised by an easy future expansion possibility with new capabilities. As a result of the firmware modification, a testbench based simulation has been performed in order to test the behaviour of the new firmware, showing a correct simulated A/D conversion. The new firmware was then experimentally tested. A first test has been performed with a waveform generator in order to test the input voltage range, the equation that relates the input voltage and the output data and the time response of the A/D experimental conversion system. The real input voltage range is slightly smaller than the one listed in the FMC112 datasheet, but the difference does not influence the thesis purpose. Moreover, the offset correction system has been also tested.

The A/D experimental conversion system has been then compared with an oscilloscope outputs by means of phase current and voltage measurements on a three phases

induction motor. This last test shows optimal results for the FMC112 based experimental setup. The sensitivity is higher than the oscilloscope one due to the 14 bit of resolution of the ADC of the FMC112 board.

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