Master Thesis

Design of a Monostable for the controller of an innovative Buck regulator

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Declaration of Authorship

I, Nicola Rasera, declare that this thesis titled, 'Design of a Monostable for the controller of an innovative Buck regulator' and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.

- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.

- Where I have consulted the published work of others, this is always clearly attributed.

- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.

- I have acknowledged all main sources of help.

- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

May 4th 2014, Nicola Rasera

"As far as the laws of mathematics refer to reality, they are not certain, as far as they are certain, they do not refer to reality."

Albert Einstein

Abstract

In the last decades the spread of portable devices has carried electronic circuits to a higher level of challenges. In fact these products are continuously demanding for higher performances together with the longest possible battery life, that results in a low power consumption.

Texas Instruments MSP430 is a 32-bit micro controller capable of assuring a very low power consumption concurrently with high performances and for these qualities is one of the most used MCU. Its power management module (PMM) is very important for assuring these characteristics, since it needs to achieve the highest energy conversion efficiency possible. One or more low drop-out voltage linear regulators (LDO) are usually employed in PMM but their efficiency degrades as the difference between their input and output voltages increases. Unfortunately battery voltages has not scaled as much as the ICs internal supply, therefore LDOs yield poor efficiency.

Texas Instruments is developing a switched mode power supply and a controller for operating it with a Pulse Frequency Modulation in order to improve the MSP430 power management efficiency. The controller uses two monostable for generating the correct time pulses. These devices consume $25\mu A$ each.

The aim of this thesis is to improve their current consumption up to the lowest possible achievable. The new power management concept is described and the monostable consumption is analysed in order to understand how it can be optimized. Afterwards the various devices composing the monostables are analysed investigating various solutions. The final circuit has been design with a TI's $90nm$ CMOS process, and it shows the same characteristics of the previous design with a current consumption improved up to $5\mu A$.

Acknowledgements

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To whom believes always in me

Chapter 1

Introduction

In the last two decades we have faced an exponential increase of electronic applications in every field, from the automotive to everyday products like microwaves or washing machines.

A micro-controller is always hidden inside all these products. These circuits are small computers that control various applications and interaction of the users with the tool. In the last decades also the number of portable devices arose significantly. These devices increased continuously their computational power and applications. The most famous example is the smartphone. However, the increase of their complexity determined the increase of their power consumption. Therefore battery-powered devices need highly efficient circuits in order not to compromise their battery life time. Thus, micro-controllers capable of providing the desired functions together with a low consumption are highly desirable.

MSP430 is continuously decreasing its power consumption in order to allow portable devices to achieve higher performances. A solution for the optimization of this microcontroller is described (chapter 2). This involves the use of a switched-mode power supply regulator instead of a linear regulator for the power management of the device. In fact it can increase significantly the efficiency of the energy conversion circuit. Obviously it needs a controller that itself has to achieve a low power consumption so as not to affect the overall efficiency. The controller uses two monostables to fix the period in which the energy is transferred from the battery to the load. These are the most significant devices of the controller, both for their role and their current consumption. In this thesis the one-shot circuit will be analysed and its current consumption will be lowered.

In chapter 2 the premises and the motivations of the project will be explained.

In chapter 3 a comparator will be realized and both its performances and its current consumption will be optimized for the monostable.

In chapter 4 a circuit for the extrapolation of a current proportional to the difference between two voltages will be analysed and realized.

Finally in chapter 5 the monostable is designed using the devices obtained in the other chapters. Afterwards the circuit will be tested and the final results will be reported.

Chapter 2

Application description

In this chapter the application of the monostable realized will be explained. A brief introduction in the difference between an LDO and a SMPS circuit for ultra-low power MCUs will take place. Finally the requirements for the monostable will be set.

2.1   MSP430 power management

The MSP430 is a Texas Intruments 16 bit Micro Controller Unit. A microcontroller is a small computer integrated on a single chip that contains a CPU, memories and I/O peripherals. MCUs are usually employed on embedded systems for special purpose digital control.

Texas Intruments 4 bit TMS1000 (1972) was the first programmable system on chip employed in application such as calculators and oven. Towards the decades MCUs developed their processing power, thanks to higher levels of integration, while they reduced their power consumption. MSP430 main advantages are the low cost and the low power consumption. It can draw less than $1\mu A$ in idle mode, while it has 6 different low power modes, useful for a lot of low power applications. It requires, as every electronic device, an external supply voltage that usually is an external battery. Therefore the MSP needs a power management module, PMM, able to provide an internal supply voltage for the integrated circuit from the external battery. The present power management is realised by a Low Dropout voltage regulator (LDO). This device is mainly a constant voltage source that provides a constant voltage at its output varying its internal resistance to the variations that occurs in the load resistance. A circuit that does this simple task is reported in figure 2.1.

The key device is the error amplifier that compares a scale-down version of the output voltage to a reference (usually a bandgap type) and adjust its output voltage in order
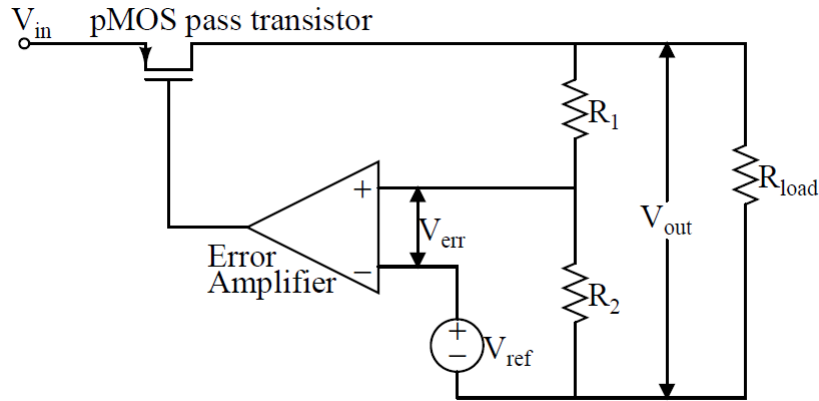
FIGURE 2.1: Basic linear voltage regulator.

to set its differential input voltage as close as possible to zero. Therefore it drives a pass transistor and varies its drain current so as to keep V_{err} close to zero through a negative feedback. The pass transistor is usually a pMOS since the gate source voltage that controls it is usually negative.

Many are the advantages provided by an LDO, such as its fast response to input and output transients, low output noise, small area; however its main drawback is its maximum theoretical efficiency that is

$$\eta_{LDO} = \frac{V_{out}}{V_{in}} \tag{2.1}$$

In fact as the difference between the output voltage and the input voltage increases, η_{LDO} drastically decreases. While the integrate circuit internal supply voltage has scaled through the decades, the battery supply voltage has remained constant. Therefore today LDOs present low cost, low complexity, but poor efficiency. Therefore switched mode power supply circuits become advisable since nowadays battery powered devices need high efficiency power regulators in order not to compromise the battery life.

2.2   Switched Mode Power Supply (SMPS) fundamentals

Switched mode power supply circuits are electronic devices used as regulators and for providing the necessary power to electronic circuits. Differently from linear regulators where there is an element (the pass transistor) that always conduct, SMPS devices continuously switches from on and off stage, remaining the lowest time possible (ideally zero) in high dissipation. For this reason the maximum ideal efficiency of such a circuit is 100%.

The basic DC/DC converters are the Buck converter and the Boost (figure 2.2). The first one is a step-down converter since $V_{out} < V_{in}$ while the second a step-up since $V_{out} > V_{in}$. The converter used to substitute the LDO is a Buck, therefore the analysis will focus on this circuit.
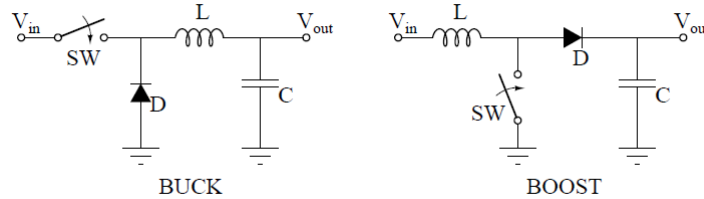
FIGURE 2.2: Basic Switched mode power supply DC/DC converters.

Buck operation fundamentals

A Buck converter is reported in the above figure. Assuming ideal switches and a current i_L always higher than zero, it is possible to evaluate the circuit operation in 2 phases:

- **Powering phase**: at the instant $t = 0$ the MOS is turned on while the diode is turned off. The voltage across the inductance is $v_L = V_{in} - V_{out}$ and its current increases linearly as

$$i_L(t) = i_L(0) + \frac{V_{in} - V_{out}}{L} t \qquad (2.2)$$

- **Freewheeling phase**: the MOS is turned off while the diode turns on. During this period the energy stored in the inductor is transferred to the output capacitor and to the load. The inductor voltage is $v_L = -V_{out}$, therefore its current linearly decreases as

$$i_L(t) = I_{LPK} - \frac{V_{out}}{L} t \qquad (2.3)$$

The steady-state condition states that the inductor current variation during each phase has to be equivalent, thus

$$\Delta I_L = \frac{V_{in} - V_{out}}{L} t_{on} = \frac{V_{out}}{L} t_{off} \Rightarrow V_{out} = \frac{t_{on}}{t_{on} + t_{off}} V_{in} = \delta V_{in} \quad \text{with } \delta = \text{duty-cycle} \tag{2.4}$$

This way of operating is called Continuous Current Mode (CCM). Equation 2.4 shows the step down characteristic of the Buck converter. The Buck time characteristics are reported in figure 2.3.
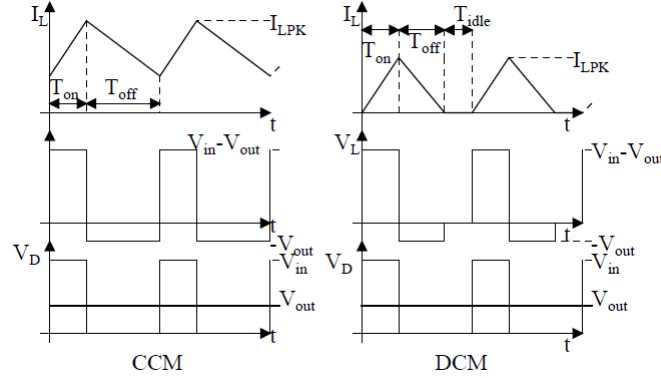
FIGURE 2.3: CCM and DCM Buck time characteristics.

The Buck behaviour varies with output current variations. As the load decreases, the inductor current becomes zero for a period and the Buck enters in Discontinuous current mode (DCM). In fact the diode does not allow i_L to become less than zero when the MOS is off. The way of operating is the same as for the CCM but there is a third phase called **idling phase** in which $i_L = 0A$ and the capacitor provides the output current. The output voltage is thus given by

$$V_{out} = MV_{in} = \frac{\delta^2}{\delta^2 + \frac{2f_s L I_0}{V_{in}}} = \frac{\delta^2}{\delta^2 + I_{oN}} \tag{2.5}$$

where f_s is the switching frequency of the system and $I_{oN} = \frac{2Lf_s \overline{I_{out}}}{V_{in}}$.

Output voltage control modulations

The output voltage has to be regulated and therefore an active controller is needed. In CCM the output voltage can be regulated varying the duty-cycle. Therefore a pulse width modulation (PWM) is employed; this utilizes a fixed switching frequency and varies the width of the on and off time in order to keep the output voltage regulated. The pulse width modulator is usually a comparator that compares a triangular waveform with a modulation signal proportional to the output voltage, in order to obtain a variable pulse square waveform used to control the switch (figure 2.4).

However CCM, and so PWM, is usually used for high load current since the Buck efficiency is higher in this mode of operation. In the case of light loads, other modulations
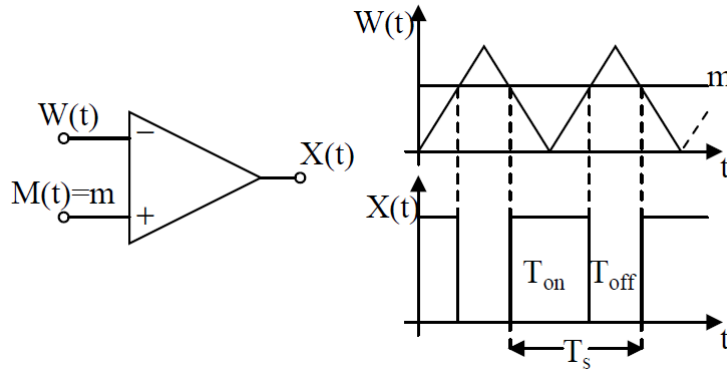
FIGURE 2.4: Pulse Width Modulation.

are used, like Pulse Frequency Modulation (PFM). Differently form PWM, in PFM the on and off times are fixed and what varies is their repetition frequency. Therefore when the output voltage is lower than the reference, the energy transferred to the load is increased enhancing the frequency.

2.3 Buck Converter for the power management

A DC-DC switching converter as a Buck has a higher efficiency than a LDO when the difference between input and output voltage is considerable. They are usually designed for showing a high efficiency at a set peak power level, while when operated in lighter load conditions their efficiency degrades. This is mainly related to the switching power losses. These losses can be reduced operating at a lower frequency, when a pulse width modulation (PWM) is employed, but results in higher peak inductor currents that determines an increased cost. The use of a discontinuous current mode (DCM) converter controlled by a frequency pulse modulation (PFM) results in a high efficiency for medium to light load conditions[1].

The converter that Texas Instruments is developing for the new MSP430 power management uses this concept[2]. A fast and stable control loop is needed. The solution proposed by Ph.D. Francesco Santoro is a power supply capable of providing the necessary energy when the digital core needs it and enter in an idle mode when the system absorbs only the leakage current[2]. For this reason a fast start up is desirable. Therefore he has designed a synchronous DCM Buck converter employing a predictive peak current controller (figure 2.5).

The inductor peak current is constant, thus the charge Q transferred every period to the load is fixed
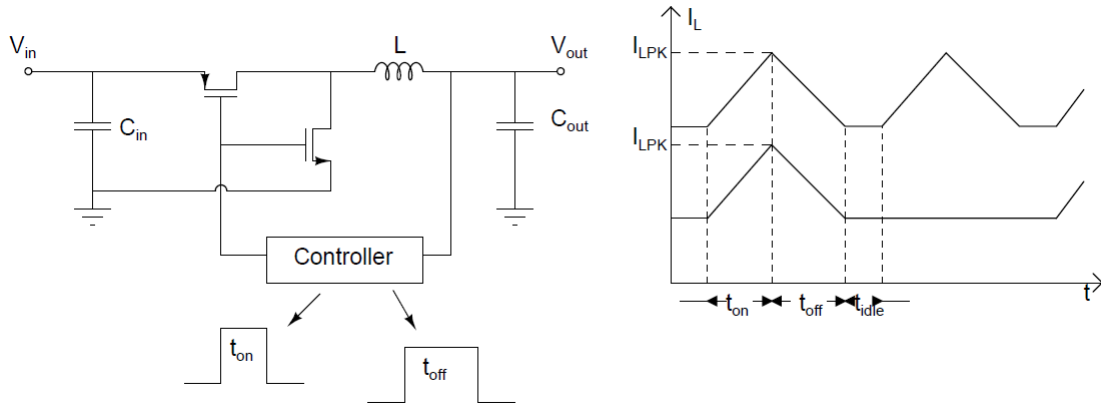
FIGURE 2.5: Buck converter with the controller that sets the variable on and off times.

$$Q = \frac{I_{LPK}T_{on} + T_{off}}{2} \tag{2.6}$$
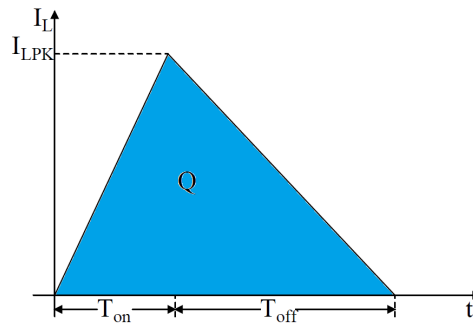
FIGURE 2.6: Quantity of charge transferred to the load every period.

Since this charge is known, it is possible to minimize the output capacitor and therefore obtain a fast start up.

The controller senses the input and output voltages of the converter, $V_{in,Buck}$ and $V_{out,Buck}$, to set the on and off time T_{on}, T_{off}. The on and off time of a Buck are given by:

$$\left.\begin{array}{l} T_{on} = \dfrac{I_{LPK}L}{V_{in,Buck} - V_{out,Buck}} \\[3mm] T_{off} = \dfrac{I_{LPK}L}{V_{out,Buck}} \end{array}\right\} \Rightarrow I_{LPK}L = \alpha = const \Rightarrow \begin{cases} T_{on} & \propto \dfrac{\alpha}{V_{in,Buck} - V_{out,Buck}} \\[3mm] T_{off} & \propto \dfrac{\alpha}{V_{out,Buck}} \end{cases}$$

$$(2.7)$$

Therefore the controller sets the correct on time depending on the difference between the input and output voltages.

The maximum inductor peak current I_{LPK} depends on the maximum DC load. The inductor dimension depends on the maximum load current, the maximum frequency of the digital circuit and the maximum output ripple voltage allowed (equation 2.8).

$$\left. \begin{array}{l} \overline{I_L} = \dfrac{I_{LPK}\left(T_{on} + T_{off}\right)}{2\left(T_{on} + T_{off} + T_{idle}\right)} \\[2em] \overline{I_{out}} = I_{load,max} \end{array} \right\} \Rightarrow \quad \overline{I_{out}} = I_L \Rightarrow \quad I_{LPK} = 2 I_{load,max} \dfrac{T_{on} + T_{off} + T_{idle}}{T_{on} + T_{off}}$$

$$\Delta V_{out} = \frac{\overline{I_{out}}}{C f_s}\left(1 - \frac{1}{2}\sqrt{\frac{I_{oN}}{M(1-M)}}\right) \tag{2.8}$$
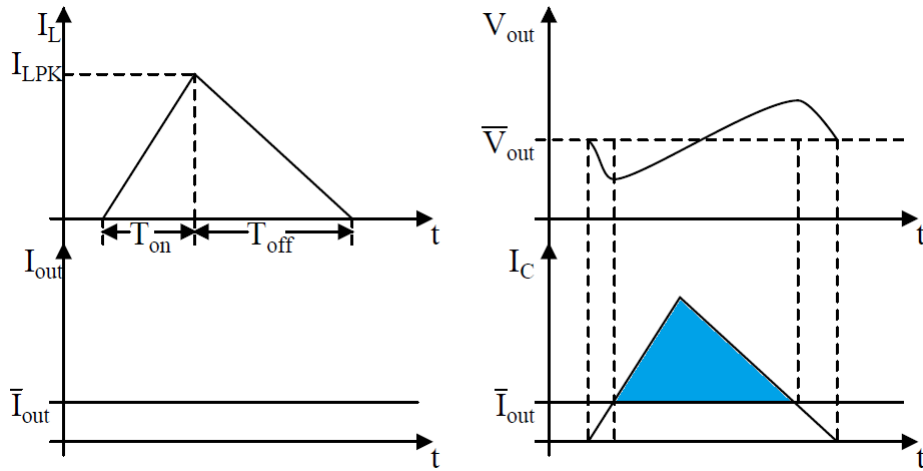
FIGURE 2.7: Output ripple voltage is function of the inductor peak current I_{LPK}.

Since $\overline{I_{out}} = 2.65mA$ and $I_{LPK} = 7.5mA$, the inductor has been set to $L = 7.4\mu H$. For this circuit the input voltages can vary from $1.7V$ to $3.6V$ (it is a battery) while the output voltage is fixed at $1.2V$. Therefore the on time varies from $T_{on} = \frac{7.5mA \cdot 7.4\mu H}{3.6V - 1.2V} \simeq 23.2ns$ and has been chosen equal to $24ns$ for simplicity, to $T_{on} = \frac{7.5mA \cdot 7.4\mu H}{1.7V - 1.2V} \simeq 111ns$. The off time is instead fixed to $T_{off} = \frac{7.5mA \cdot 7.4\mu H}{1.2V} \simeq 46.3ns \approx 48ns$. The controller is reported in figure 2.8.

A comparator senses the output voltage $V_{out,Buck}$ and compares it with a reference V_{ref}. When the output voltage goes under the reference, the comparator output goes to a digital control logic that wakes up the switching converter and triggers a monostable that fixes the on time. The on time monostable then triggers an off time monostable after a small delay so as to avoid cross conduction, since the two pulses drive the power stage. The signal is then sent to the control logic after a minimum delay time in order to assure that the converter does never enter in continuous current mode (CCM). Finally
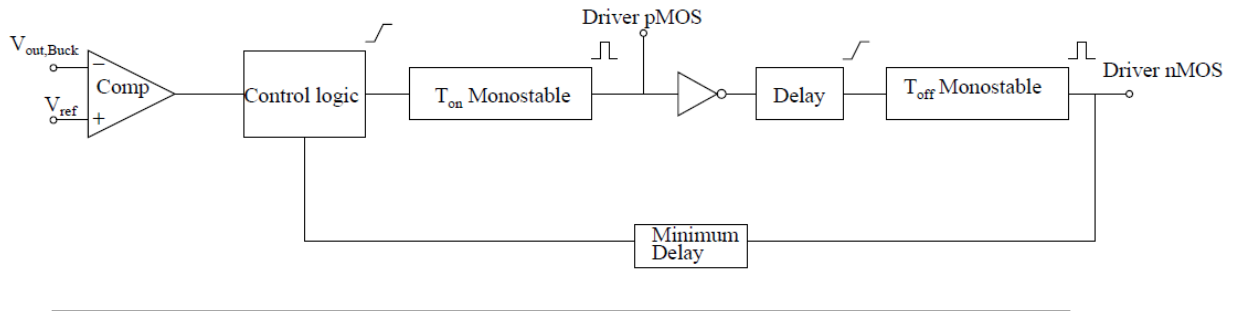
FIGURE 2.8: Controller realized for the DCM Buck converter.

the control logic allows the system to start again until the output voltage is higher than the reference voltage and the comparator switches again putting the converter in idle mode. In this way the resulting Buck period (considering the maximum current load) results to be $T_{Buck} = T_{on} + T_{off} + T_{idle} = 24ns + 48ns + 28ns = 100ns$ (for a 3.6V input voltage) and $T_{Buck} = T_{on} + T_{off} + T_{idle} = 111ns + 48ns + 91ns = 250ns$ (for the 1.7V input voltage).

2.4 Monostable

The key devices in the whole controller are the monostable circuits. In fact they have the important role of driving the Buck's power stage, therefore they regulate the amount of energy transferred to the load every period.

A *monostable* is a circuit that generates a pulse of a pre-defined time width in response to an external trigger input signal. The name of this device derives from its unique stable state, during its rest period. The external impulse causes the circuit to its quasi stable state for a period of time that is determined by the circuit internal parameters. Usually a one-shot circuit uses a device able to provide a delay that sets the pulse width. The simplest monostable is realized using the circuit in figure 2.9.
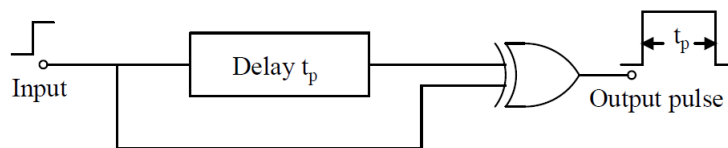
FIGURE 2.9: Simplest monostable design.

In the stable state the output is zero since the inputs are both at zero. When an impulse is applied, the output goes to 1 until the two XOR inputs return equal, time that is exactly the delay t_p introduced. In this way a pulse of width t_p has been generated.

A common mode to produce a delay cell is to introduce a RC time constant or use a cascade of elementary digital ports.

Another common way of design a monostable is that reported in [3] and [1]. The common concept is reported in figure 2.10.
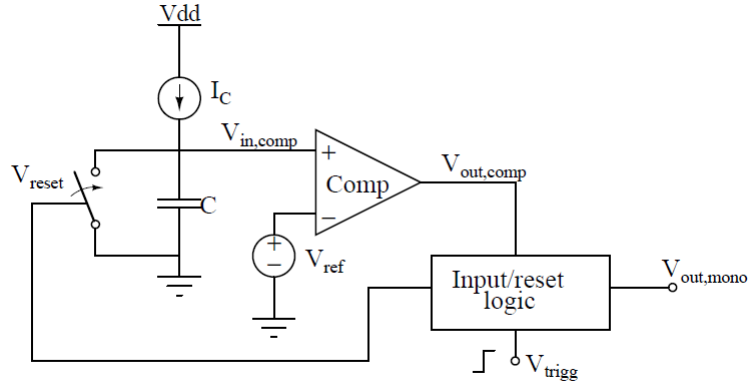
FIGURE 2.10: Monostable concept.

A triggering signal determines the input of the monostable pulse and turns off the switch that keeps the capacitor discharged. A constant current is therefore able to charge the capacitor and generate a ramp input voltage signal since

$$I(t) = C\frac{dV(t)}{dt} \implies V(t) = V(t_0) + \frac{1}{C}I_C(t - t_0) \tag{2.9}$$

This ramp input voltage has a constant slope and the monostable's time width can be set as the time took by the ramp to reach a defined voltage. Therefore a comparator is used to detect this event. It compares the ramp voltage signal with a voltage reference and its output goes from 0 to 1 when the input signal crosses the reference. A suitable digital circuitry uses this signal to determine the end of the pulse.

The Buck controller needs a monostable able to vary its pulse width depending on the input and output voltage of the regulator and obtain always the same I_{LPK}. The previous concept can be used for the realization of this device, but it has to be modified in order to be able to provide different pulses. The parameter that can be easily varied is the current that charges the capacitor. In fact it varies the slope of the ramp voltage, allowing it to cross the reference at different times. If this current varies proportionally to the input output voltage difference $V_{in,Buck} - V_{out,Buck}$, then the monostable varies its width proportionally to this parameter.

This concept has been developed by Ph.D. Francesco Santoro. The circuit that he realized is reported in figure 2.11. Two voltage regulators for the generation of the currents proportional to $V_{in,Buck}$ and $V_{out,Buck}$ are used. The two currents are then

subtracted using a current mirror. The current resulting from this operation is then used to charge a capacitor. Finally a comparator is used to detect the reference crossing. The current consumption of every device is reported in the figure. The resulting overall current consumption of the fist version of the monostable is

$$
\begin{aligned}
I_{cons} &= 2 \cdot I_{cons,OTA} + I_{V_{in}} + I_{V_{in},copy} + I_{V_{out}} + I_{V_{in}-V_{out}} + I_C + I_{cons,comp} \\
&\approx 2 \cdot 300nA + 2 \cdot 750nA + 250nA + 750nA + 2.5\mu A + 20\mu A = 25.6\mu A
\end{aligned}
\tag{2.10}
$$

The purpose of this thesis is therefore to reduce as much as possible the consumption of this monostable.

the requirements set for this circuits are:

- average current consumption in a period $\overline{I_{cons}} \leq 10\mu A$ as a fist goal

- input Buck voltage that varies from $1.7V$ to $3.6V$

- variable pulse width T_{on} from $24ns$ to $111ns$

- maximum allowable pulse jitter related to process variations and random mismatches $\sigma_{T_{on}} \leq 2.5\%$ of T_{on}

The comparator is the circuit that consumes more current since it has to be fast. Thus the optimization starts from this circuit.
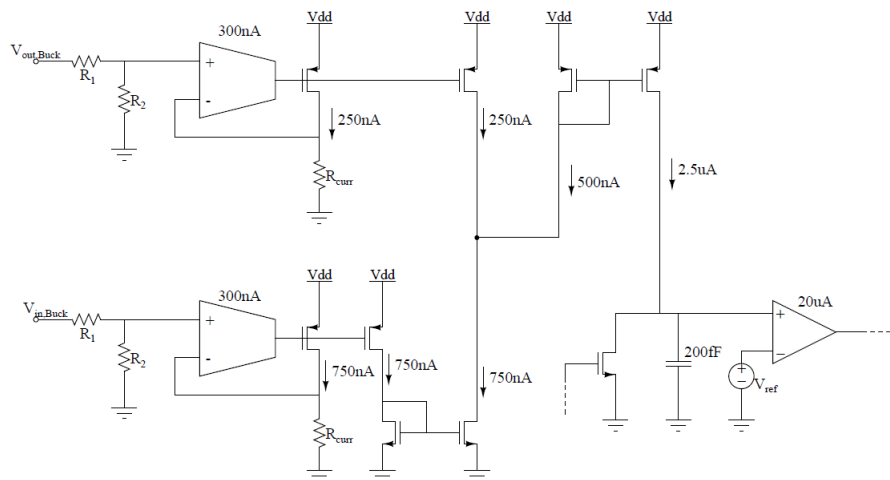
FIGURE 2.11: Francesco Santoro monostable design concept.

Chapter 3

Comparator

As explained in the previous chapter, the optimization began from the comparator, since it has to match very strictly requirements and it is the most current hungry device. In the first monostable version, the comparator was an open loop 2-stage OTA with an average current consumption of $20\mu A$.

This chapter will begin with the comparator fundamentals. After that, all the different suitable solutions will be described, each one with its pros and cons. The fundamentals and the relative considerations are based on [4].

3.1 Comparator fundamentals

Static characteristics

The comparator is a widely used circuit and it relates analog signals to digital ones; in fact it can be considered a 1-bit analog to digital converter.

This circuit, as the name suggests, compares its two input voltages, giving a binary output(0 or 1) depending on the result of the comparison. Therefore V_{out} equals a defined high voltage V_{oH} when the positive input $V_{i,p}$ is greater than the negative input voltage $V_{i,n}$, otherwise it is set to a defined low voltage V_{oL}. The behaviour of the ideal comparator is mathematically described in 3.1.

$$V_{out} = \begin{cases} V_{oH} & if\ V_{i,p} - V_{i,n} > 0 \\ V_{oL} & if\ V_{i,p} - V_{i,n} < 0 \end{cases} \tag{3.1}$$

The output of the comparator changes its state(from V_{oL} to V_{oH}) when there is a variation of $\Delta V = V_{i,p} - V_{i,n}$ (figure 3.1). The gain of the ideal comparator is

(a) *Comparator symbol.*   (b) *Ideal transfer voltage curve.*
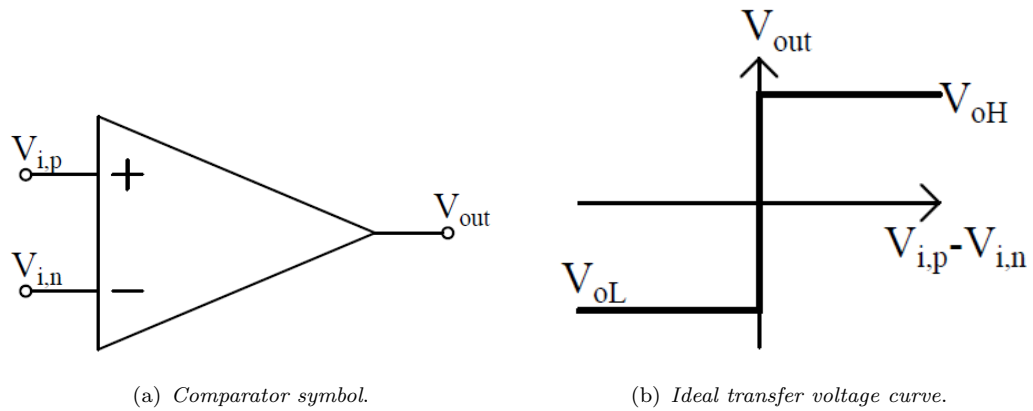
FIGURE 3.1: Comparator symbol and ideal transfer voltage curve.

$$A_v = \lim_{\Delta V \to 0} \frac{V_{oH} - V_{oL}}{\Delta V} = \infty \tag{3.2}$$

In figure 3.2 it is shown a more realistic transfer function of a comparator. In fact the gain is not infinite any more and there is a finite transition region. The gain is better defined as

$$A_v = \frac{V_{oH} - V_{oL}}{V_{iH} - V_{iL}} \tag{3.3}$$
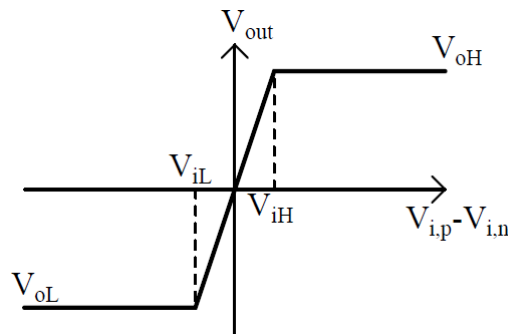
FIGURE 3.2: Tranfer voltage curve of a more realistic comparator.

Now it is also possible to introduce a paramenter, the *resolution*, that shows what is the minimum input change needed for the saturation of the output voltage. Of course the greatest gain possible is pursued in order to obtain the smallest transition region and the lowest resolution.

The input offset voltage V_{os} is another very important non-ideality of comparators. In figure 3.2, the output of the comparator changes state when the differential input crosses the zero voltage. However, the change of state happens at a defined voltage V_{os} (figure

3.3). This non ideal behavior should not be a problem if this voltage could be predicted. Unfortunately the offset voltage depends from the structure of the circuit, process variations and random mismatches that changes from die to die. These variations are related to the mismatches between every device that arise in the fabrication process.
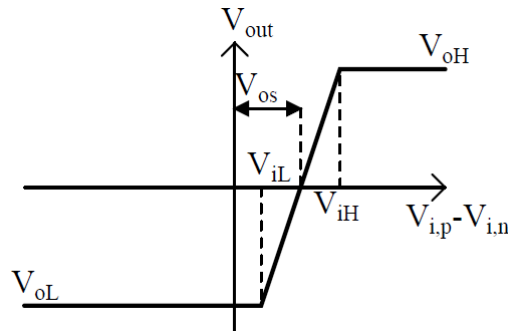
FIGURE 3.3: Tranfer voltage curve with input offset voltage V_{os}.

The ICMR, *input common mode range* is another parameter that has to be taken into account when designing a comparator. This parameter describes the range of common mode voltage in which the comparator works properly. Usually this ICMR is the range in which the transistors works in saturation region.

Dynamic characteristics

The static characteristics and the comparator's non idealities have been explained. The other very important and interesting parameters of this circuit are its dynamic characteristics, that include both large and small signal behavior.

The *propagation delay* is the most important dynamic characteristic of a comparator. This is the time that it takes to make a change in V_{out} signal in response to a V_{in} impulse. This delay is a really important and constraining parameter since it is often the speed limitation of an A/D converter. As it is possible to see from figure 3.10 the propagation delay is defined as the time elapsed from when the input signal in the positive (or negative) input becomes larger (or lower) than the negative one, to when the output reaches a defined threshold $V_{thr} = \frac{V_{oH}+V_{oL}}{2}$.

Usually the propagation delay varies in dependence of the input signal swing; a small delay time is obtained with a large input swing. This fact is simply understandable since, as it will be shown, the comparator input is usually a differential input pair; a large and fast change in its differential voltage determines a large and fast change in its drain current. This behaviour has a limit, otherwise every comparator would have
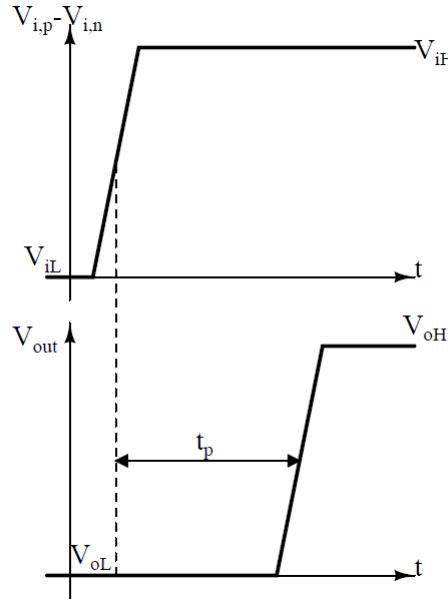
FIGURE 3.4: Output response to an input response with the delay time.

a zero time delay and this one would not be an important dynamic parameter. This upper limit is the *slew rate*, as it will be described.

Therefore when the input has a large voltage swing, and so a large change in the overdrive ($V_{ov} = V_{gs} - V_T$), we have a delay time that is mainly determined by the large-signal behaviour of the comparator. Differently, when a small differential input signal is applied (hence a small V_{ov}), the delay time is mainly determined by the small-signal behaviour of the comparator.

In this case the frequency response of the comparator relates the small-signal dynamics and the most simple model is a single pole response:

$$A_v(s) = \frac{A_{v0}}{1 + \frac{s}{\omega_p}} = \frac{A_{v0}}{1 + s\tau_p} \tag{3.4}$$

where A_{v0} is the DC gain and ω_p is the pulse of the pole, hence the -3dB frequency($\omega_p = 2\pi f_p$) of the comparator. This equation represents the variation of V_{out} in response of a small variation in the differential input. The time relation between these two variations is really important for this analysis. Then from $A_v(s) = \frac{\Delta V_{out}}{\Delta V_{in}}$ we obtain a first order exponential response:

$$\Delta V_{out} = A_{v0}(1 - e^{-t/\tau_p})\Delta V_{in} \tag{3.5}$$

The propagation delay is the time that passes from the input variations to when the output voltage crosses the threshold previously defined. Let us assume that the minimum input voltage capable of moving the output is applied. This minimum input voltage is:

$$V_{in,min} = \frac{V_{oH} + V_{oL}}{A_{v0}} \tag{3.6}$$

From 3.5 and 3.6 we obtain

$$\frac{V_{oH} + V_{oL}}{2} = A_{v0}(1 - e^{-t_d/\tau_p}) \left(\frac{V_{oH} + V_{oL}}{A_{v0}} \right) \tag{3.7}$$

Solving this simple equation it is possible to find a simple relation for the delay time

$$t_d = \tau_p \cdot ln(2) \simeq 0.69\tau_p \tag{3.8}$$

From the general hypothesis, this equation is valid for both positive and negative input variations. Moreover it is possible to relate the delay for input variations k times bigger than the minimum one.

$$t_d = \tau_p \cdot ln \left(\frac{2k}{2k - 1} \right) \tag{3.9}$$

As it is possible to see from equation 3.9, the bigger is the input voltage (and obviously the overdrive), the smaller is the propagation delay.

Obviously there is an upper limit to this behaviour. In fact, increasing the input overdrive voltage, leads the comparator to a large-signal mode of operation in which the maximum current for charging and discharging the capacitances is limited by the slew-rate. In this case the delay is

$$t_d = \frac{\Delta V}{SR} = \frac{V_{oH} - V_{oL}}{2 \cdot SR} \tag{3.10}$$

Sometimes it is useful to understand whether the delay is dominated by a small-signal or a large-signal dynamic and the overdrive at which occurs the change from small-signal to large-signal dynamics.

This change theoretically happens when the delay time is limited both by equations 3.9 and 3.10

$$\tau_p \cdot ln\left(\frac{2k}{2k-1}\right) \doteq \frac{V_{oH} - V_{oL}}{2 \cdot SR}$$

$$\Rightarrow k_{lim} = \frac{e^{\frac{V_{oH}-V_{oL}}{2 \cdot \tau_p \cdot SR}}}{2\left(e^{\frac{V_{oH}-V_{oL}}{2 \cdot \tau_p \cdot SR}} - 1\right)} \tag{3.11}$$

As an example we can suppose a comparator with $A_{v0} = 60dB$, $V_{oH} - V_{oL} = 1.2V$, a dominant pole at $2\pi f_p = \frac{1}{\tau_p} = 10^4 rad/s$ and a $SR = 300mV/\mu s$. We obtain that

$$k_{lim} = \frac{e^{\frac{1.2}{2 \cdot 100\mu s \cdot 300mV/\mu s}}}{2\left(e^{\frac{1.2}{2 \cdot 100\mu s \cdot 300mV/\mu s}} - 1\right)} \simeq 25$$

Since $V_{in,min} = 1.2mV$, we have that for an input smaller than $30mV$ the delay propagation is dominated by the small-signal dynamic, while after this value it is dominated by the large-signal dynamic.

The two families of comparators

Comparators are one of the most important and used circuit in ICs. They can be classified into two main families: time-continuous and time-discrete comparators.
The former, as the name suggests, compares the two inputs continuously in the time. The latter, instead, does the comparison in two different phases, each one decided by a clock signal. Hence there is a first phase of *evaluation*, and a second phase of *comparison*. This type of comparators are widely used for AD-converters and can guarantee a high speed and a low power consumption(in figure 3.5 there is an example of time-discrete comparator).

In general the DCDC comparator used to turn on the controller can be time-discrete since it can use the "clock" that results from the on and off time monostables. Instead the time continuous nature of these devices force the use of time-continuous comparators into them.

For this reason the comparators that will be considered in the following analysis will be only time-continuous.
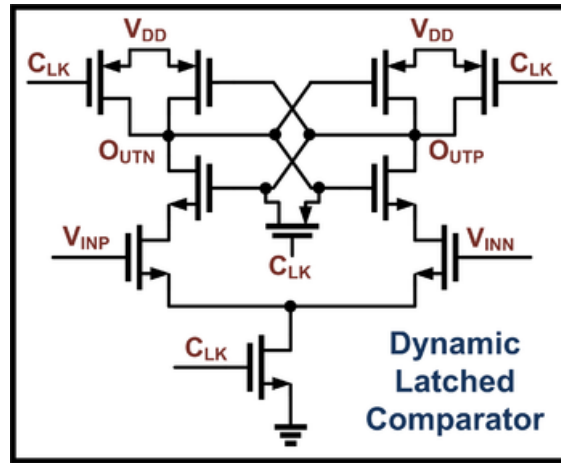
FIGURE 3.5: Time-discrete comparator.

3.2 Comparator requirements and simulation set-up

The monostable requirements have been defined in chapter 1. This circuit has to provide a pulse with a variable time width that varies from $24ns$ to $111ns$ depending on the Buck's input and output voltages. These pulses have then to show a low variability to process variations and random mismatches. Therefore a requirement concerning the statistical behaviour has been set: $\sigma_{T_{on}} \leq 2.5\% \quad of \quad \mu_{T_{on}}$. The other important requirement is the average current consumption in a period of operation, that has to be the lowest possible. Initially the consumption set as a first goal is $\overline{I_{cons}} \leq 10\mu A$. Afterwards this requirement will be lowered in order to obtain a circuit with the lowest possible current consumption.

Comparator requirements

The comparator is the most important device in the monostable. In fact it has to be very fast and produce the lowest possible delay time. For this reason the assigned power budget is the highest of the whole monostable. However the current consumption is not the only important requirement of the comparator; in fact it has even to show the lowest delay together with the lowest mismatch and processing variability. Being very precise and careful, even the comparator's offset is important, especially because its variations affect the delay and its precision. Luckily (as explained in A) its value decreases when bigger devices are used, as the use of bigger devices decreases the variation of the delay time.

The requirements set for the comparator are:

- maximum delay time t_d equal to $10 - 15\%$ of the total period. This means that $t_{d_{max}} = 2.4 - 3.3ns$ if $T_{on} = 24ns$ and $t_{d_{max}} = 11 - 16.6ns$ if $T_{on} = 111ns$;

- maximum standard deviation σ_{t_d} equal to the 10% of the propagation delay. It has to be noted that this 10% of t_p represents only the 1% of T_{on};

- average current consumption in a period $\overline{I_{cons}} \le 7\mu A$ (first goal).

Simulation set-up

In the following sections various comparator's topologies will be analysed in order to find the most suitable circuit that fulfils all the requirements described above. Firstly a theoretical analysis of them will be done and then the circuits will be simulated with Cadence, in order to check their behaviour. In order to obtain a simulation that is the closest possible to the real behaviour of the circuit, it is important to use a correct test bench.

For its realization it is essential to have a clear knowledge of the task of the circuit, the comparator in this case, and its actual inputs. A bad test bench design may lead to errors and a bad functioning of the designed circuit.

In chapter 1 it is shown the idea that stands behind the operation of the monostable. A current proportional to the difference of two voltages is driven into a capacitance, generating a ramp voltage that is compared to a steady reference voltage: the time from the beginning of the ramp to the instant in which it crosses the reference represents the pulse of the monostable.

Therefore the comparator has a single supply voltage of $1.2V$, a constant reference voltage $V_{ref} = 300mV$ connected to the negative input pin, and a ramp input signal. In the final circuit the load of the comparator is a digital port, then it is the input capacitance of this port. The comparator has even a bias current that is provided by a current mirror from a reference of $100nA$. The test bench is shown in figure 3.6; the current reference and the supply voltage are realized by an ideal current generator and an ideal voltage generator, respectively. For some realizations some ideal pulse generators will be used in order to switch on and off the comparator every period, and achieve a smaller current consumption.

The simulations used are:

- *transient analysis* in order to check the propagation delay and the current consumed

- *dc sweep analysis* for the measurement of V_{os}

- *Monte Carlo analysis* is used to check the fulfilment of statistical requirements. The number of runs for every Monte Carlo is set to 300 (appendix A).
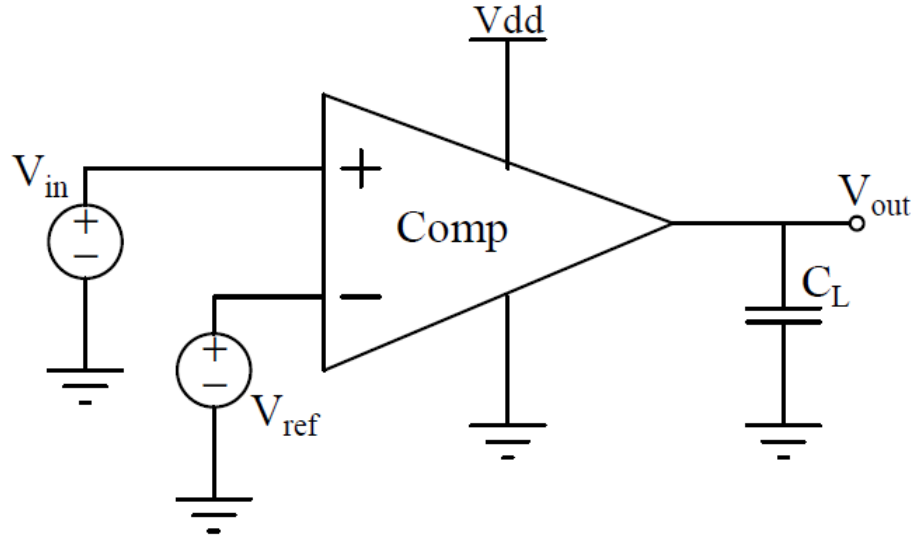
FIGURE 3.6: Test-bench used for the simulations.

3.3 Analysis and results of comparator topologies

In this section all the different analysed and simulated comparator topologies are examined. The work starts with the simple circuit and then the topologies evolve depending on the problems faced during the development of the solution.

3.3.1 Differential input pair with current mirror load

The comparator is mainly an amplifier with a differential input and a single-ended output. It is capable of amplifying the input differential voltage, saturating the output to V_{oH} or V_{oL} depending on the magnitude of $V_{id} = V_{in,p} - V_{in,n}$. The mode of operation of an OTA(figure 3.7) shows a transconductance region and a saturation region. While OTA are forced to operate on the former, a comparator has the simple task of saturating the output voltage to his maximum or minimum voltage. Therefore a comparator is usually an open-loop OTA. The advantage of this way of operation is that the comparator has a wider band and it does not show stability problems; as a consequence, it is not necessary a compensation path when a multi stage OTA is used as comparator[4].
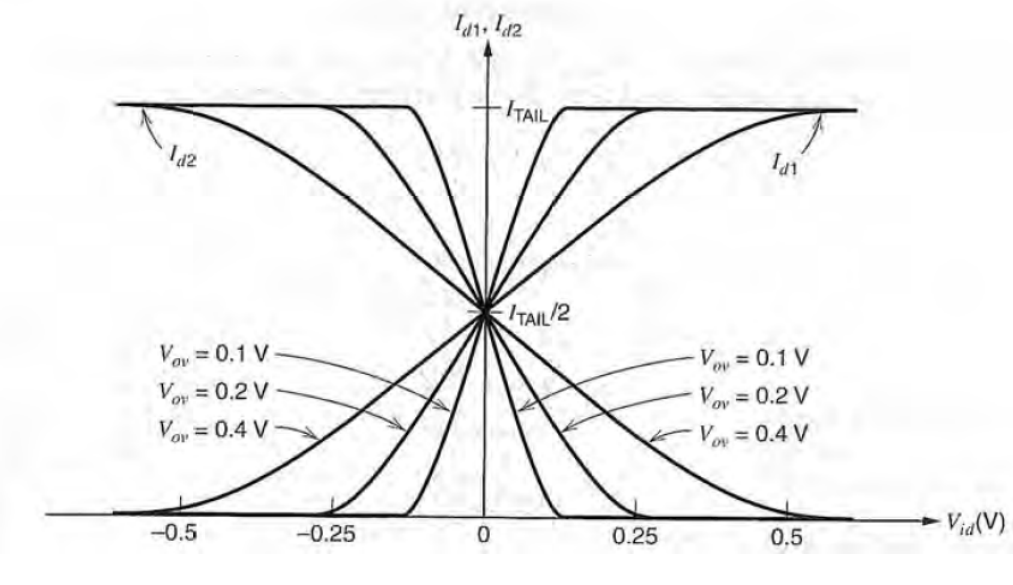
FIGURE 3.7: OTA transfer function[5].

The most simple OTA to implement is a differential input pair loaded by a two MOS in a mirror configuration (figure 3.8), in order to match the single-ended topology. The input common mode is closer to ground than to V_{dd} since the inputs are $V_{in,n} = V_{ref} = 300mV$ and $V_{in,p}$ is a ramp voltage starting from $0V$. This thing suggests the use of a pMOS input differential pair. For $V_{in} = 0V < 300mV = V_{ref}$ almost the entire tail current flows in transistor M1, with the consequence of a zero current flowing in the branch of M2 and M4. This means that M2 is turned off and M4 is in triode region, with zero drain-source voltage; therefore the output voltage in this case is zero, following correctly the comparator definition. As V_{in} approaches V_{ref} the tail current begins to steer from the branch of M1 to that of M2. When $V_{in} > V_{ref}$ the most of the current flows in M2 while little current is mirrored by the load since the current flowing through M1 is small. Therefore the output voltage is forced to raise from $0V$ to V_{dd} since the current charges the output capacitance.

In [4], [5] and [6], the frequency response of this circuit is given by a dominant pole and a couple zero-pole coming from the current mirror load. Therefore it is
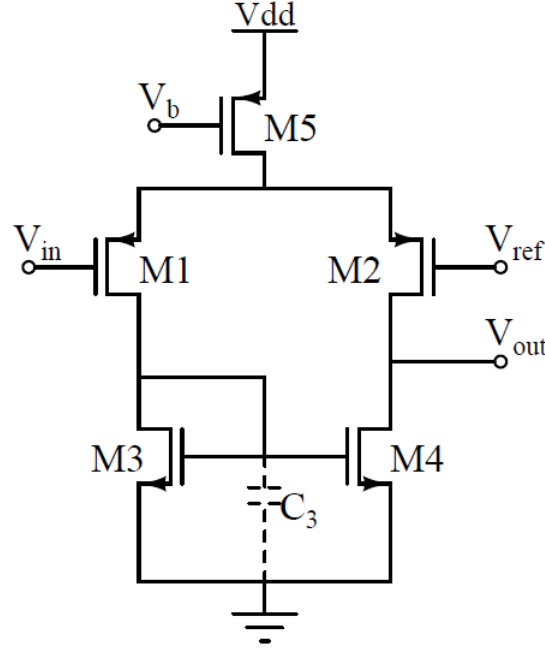
FIGURE 3.8: Differential pair with current mirror load comparator circuit. The parasitic capacitance C_3 responsible for the zero-pole couple is reported.

$$A_v(s) = \frac{V_{out}(s)}{V_{id}(s)} = A_{v0} \frac{1 + \frac{s}{\omega_z}}{\left(1 + \frac{s}{\omega_{p,D}}\right)\left(1 + \frac{s}{\omega_{p,ND}}\right)}$$

$$with \quad A_{v0} = g_{m1,2}(r_{o2} \parallel r_{o4})$$

$$\omega_{p,D} \simeq \frac{1}{(r_{o2} \parallel r_{o4})\, C_{out}} \tag{3.12}$$

$$\omega_{p,ND} \simeq \frac{g_{m3}}{C_3}$$

$$\omega_z \simeq \frac{2g_{m3}}{C_3}$$

The output capacitance $C_{out} \approx C_L$ and $C_3 \approx 2C_{gs,n}$, if the parasitic gate drain capacitances are considered negligible compared to C_{gs} and C_L. Therefore it is possible to assume that the 5-MOS OTA has a dominant pole frequency response, since the C_L is several times bigger than C_3. In fact the literature shows that $\omega_{p,ND}$ and ω_z come several decades after $\omega_{p,D}$. The frequency response Bode diagram of the comparator is reported in figure 3.9 demonstrating that it is a correct approximation. A single-ended OTA has even a pole and a zero that comes from the current mirrored by the active load; this pole-zero couple is usually at higher frequencies than the dominant pole and can be omitted in this basic analysis. The effect of pole-zero couple presence is that of slightly slowing the transient response.
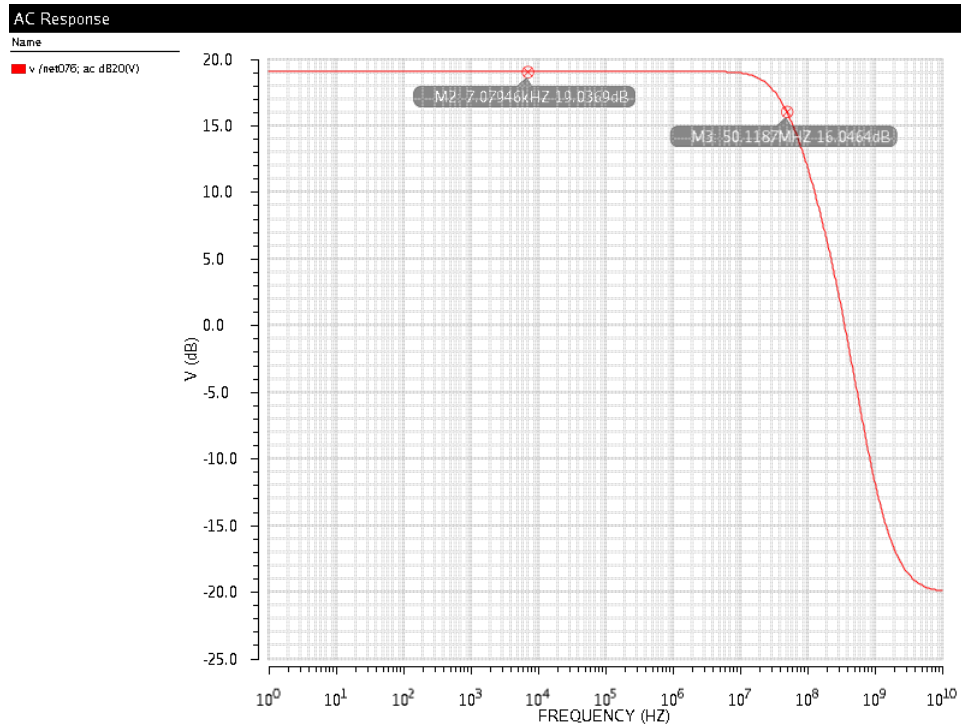
FIGURE 3.9: Transfer function of the comparator with the current mirror load.

Having made these premises, the transfer function is:

$$H(s) = \frac{A_{v0}}{1 + s\tau_c} \tag{3.13}$$

The step response of a first order transfer function is well-known and equal to:

$$V_{out}(t) = A_{v0}V_{step}(1 - e^{-t/\tau_c}) \tag{3.14}$$

However in this case the input is not a step but a ramp signal $V_{in}(t) = mt$ where $m = \frac{V_{ref}}{\Delta T}$ is the slope of the ramp. The Laplace-transform of the ramp is $\mathcal{L}^{-1}\{mt\} = \frac{m}{s^2}$. It is known from the signal theory that the transient response to a ramp input signal is simply the time integral of the step transient response, that is:

$$V_{out}(t) = \int_0^t A_{v0}m(1 - e^{-\tau/\tau_c})d\tau = A_{v0}m(t + \tau_c e^{-t/\tau_c}) \tag{3.15}$$

Once the time behaviour of the output voltage is obtained, it is possible to relate the propagation delay to the dominant pole of the comparator. In this way a relationship useful to find all the comparator's parameters can be obtained. However equation 3.15 is non-linear and not easy to solve; for this reason it is necessary to make an approximation,

substituting the exponential with its Taylor power series expression, interrupted at its second-order term.

$$V_{out}(t_p) = V_{THR} = A_{v0}m(t_p + \tau_c e^{-t_p/\tau_c})$$
$$\frac{V_{oH} - V_{oL}}{2} = V_{THR} = A_{v0}m\left(t_p + \tau_c \cdot \left(1 - \frac{t_p}{\tau_c} + \frac{t_p^2}{2\tau_c^2}\right)\right) \tag{3.16}$$

Considering $M = \frac{V_{THR}}{A_{v0}m}$ we obtain

$$2\tau_c^2 - 2M\tau_c + t_p^2 = 0 \tag{3.17}$$

Once the desired delay t_p is fixed, equation 3.17 gives two time constants as solution (with a condition on the maximum DC gain). The relation between time constants and poles is simple:

$$\omega_c = 1/\tau_c \tag{3.18}$$

As it will be shown in equation 3.20, the tail current directly depends on the pole frequency, therefore the lowest pole has been chosen in order to obtain the lowest current consumption.

The dominant pole is given by $\omega_c = \omega_{p,D} = \frac{1}{(r_{o2}\|r_{o4})C_L}$ (equation 3.12). Moreover it is known from MOSFETs' model that its output resistance can be expressed by $r_{o2,4} = \frac{1}{\lambda_{n,p}I_{d2,4}}$. Sometimes it is referred as $r_o = \frac{\eta_{n,p}L}{I_d}$ but there are no differences since in both cases the channel length L is a choice of the designer. The resistances' parallel is

$$r_{o2}\|r_{o4} = \frac{1}{(\lambda_n + \lambda_p)I_{d2,4}} \tag{3.19}$$

Combining equation 3.18 with 3.19 it is possible to find the tail current for the comparator, that is

$$I_{M1,2} = \frac{I_{M5}}{2} = \frac{\omega_c C_L}{\lambda_n + \lambda_p} \tag{3.20}$$

Afterwards, it is possible to find the transconductance of the differential pair and then $(W/L)_1 = (W/L)_2$

(a) V_{out}, V_{ref} and the 24ns input ramp.

(b) V_{out}, V_{ref} and the 111ns input ramp.
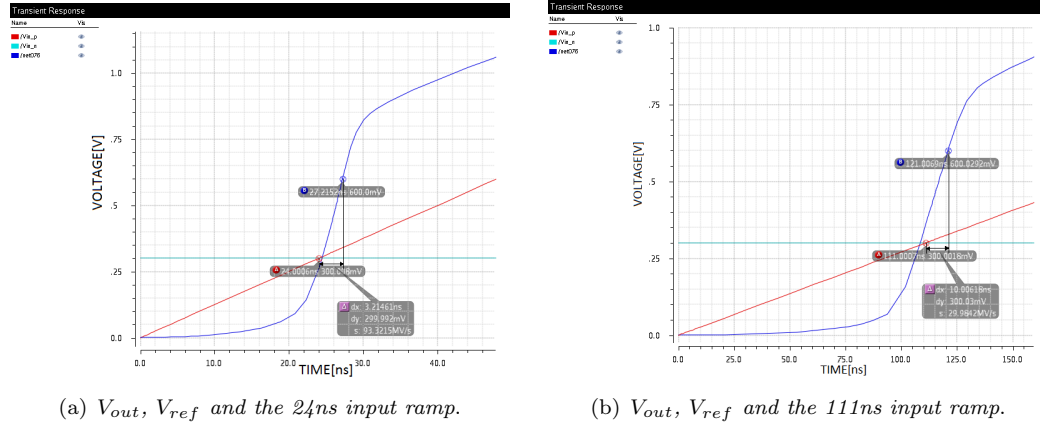
FIGURE 3.10: Output voltage and delay time with $24ns$ and $111ns$ input ramp.

$$g_{m1,2} = \frac{A_{v0}}{r_{o2} \| r_{o4}} \Rightarrow \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m1,2}^2}{2\mu_p C_{ox} I_{d1,2}} \qquad (3.21)$$

where the last equality has been derived from the well-known $g_m = \sqrt{2I_d \mu_{n,p} C_{ox} W/L}$. The dimensions of the load MOS M3 and M4 are the last parameters that has to be decided. Since $g_{m3,4} = \mu_{n,p} C_{ox} W/L (V_{gs3,4} - V_{Tn}) = \frac{2I_{d3,4}}{V_{gs3,4} - V_{Tn}}$ then we find

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{2I_{d3,4}}{\mu_n C_{ox}(V_{gs3,4} - V_{Tn})} \qquad (3.22)$$

Results

The comparator realized from the analysis above, shows a nominal delay $t_p = 3.21ns$ for the 24ns ramp and $t_p = 10ns$ for the 111ns ramp, with a tail current of $I_{tail} = 10\mu A$. In figure 3.10 the results are shown. It is possible to see the input ramp (for simplicity it stops raising at 400mV), the voltage reference and the output voltage. This voltage is full-swing but it has not a fast change in the logic state since it is not possible to obtain a high gain from the OTA we are using. This gain can be increased using two cascaded inverters as output stage. In this way a full-swing digital output signal can be obtained. These two inverters form a digital buffer with the capability of increasing the output current and driving faster the output capacitance. However it is necessary to design the first inverter with a W/L capable of sinking the output capacitance without loading the output node of the comparator. As more than one inverter is cascaded, it is important to increase the W/L of a 2.72 factor, so as not to load the previous stage and to obtain the lowest delay[4],[7].

(a) *Monte Carlo runs.* (b) *Gaussian distribution.*
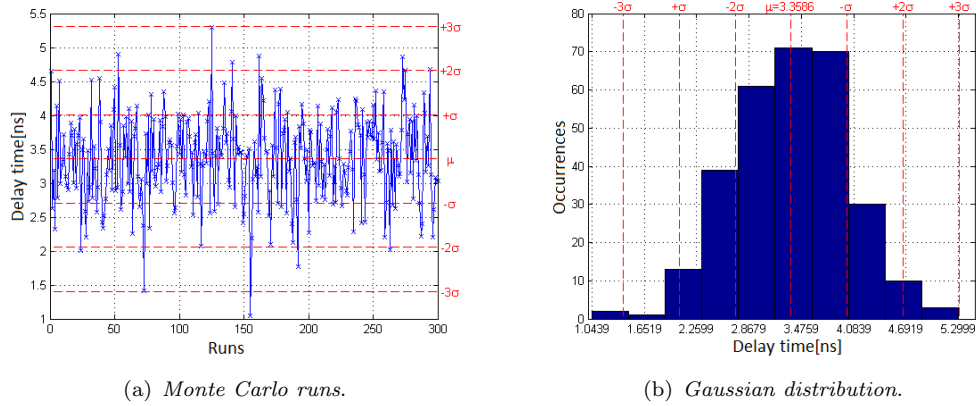
FIGURE 3.11: Statistical results for the $24ns$ period.

(a) *Monte Carlo runs.* (b) *Gaussian distribution.*
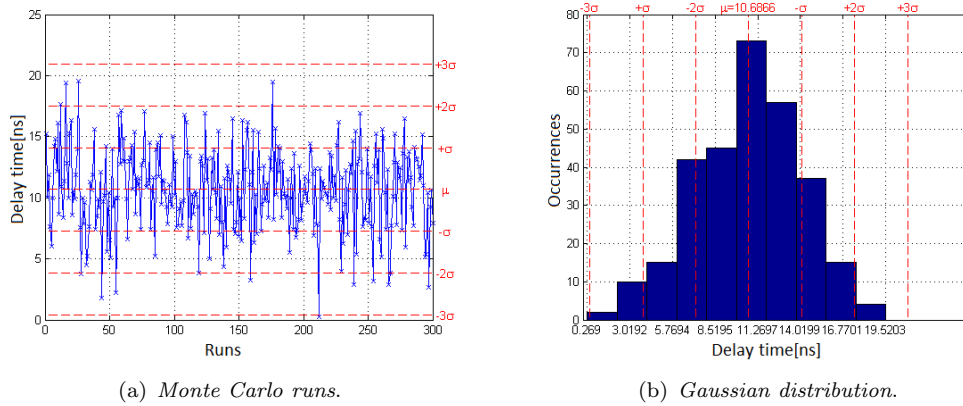
FIGURE 3.12: Statistical results for the $111ns$ period.

The requirements are nearly satisfied since the t_p is respectively the 14.04% for the $24ns$ and 9.46% for the $111ns$. The most difficult task is the satisfaction of the requirement regarding the smaller period delay. The other difficult point regards the current consumption. In this circuit it is equal to the $10\mu A$ of the tail current, plus the $1\mu A$ of biasing current mirror, therefore $I_{cons} = 11\mu A$; the consumption requirement is not fulfilled. However we will not focus much on the consumption, since it is possible to reduce the average consumption per period switching off the comparator during the time when it is not needed and switching it on when the ramp voltage begins. In this way it is however necessary to ensure that the comparator is able to turn on completely in $24ns$

The last requirements that need to be checked are the ones regarding random mismatches and processing variations. Therefore a Monte Carlo analysis is done obtaining the results in figure 3.11 for the $24ns$ period, and in figure 3.12 for the $111ns$ period.

In table 3.1the results are reported, showing that the circuit is not fulfilling the requirements.

$\mathbf{T_{on}}$	$\mu_{\mathbf{t_p}}$	$\sigma_{\mathbf{t_p}}$	$\sigma_{\mathbf{t_p}}$ **in** **%** **of** $\mathbf{t_p}$	$\mathbf{I_{cons}}$
$24ns$	$3.36ns$	$6.51 \cdot 10^{-10}$	20%	$11\mu A$
$111ns$	$10.69ns$	$3.42 \cdot 10^{-10}$	30%	$11\mu A$

TABLE 3.1: Mirror load comparator Monte-Carlo results

In order to understand how it is possible to improve these values, it is important to check the correlation table. This table shows the parameters responsible for the statistical distribution, together with their correlation factor. Therefore it is necessary to reduce the influence of the factors with the highest correlation in order to reduce the value of σ. In this case the random mismatches of the differential input pair transistors are the responsible for the high standard deviation. This result is easy to understand since the input devices are responsible for the steering of the current, and for the input offset voltage (in this case $V_{os} = 5mV$); therefore the variations in the current factor and input offset determine the variations in the propagation delay.

In order to reduce the standard deviation it is necessary to increase the gate area $(W \cdot L)$ of the input devices (appendix A). Unfortunately increasing the gate area keeping the same W/L (and so the same g_m) slows the transistors and so the steering of the current in response to the differential input voltage. This has the consequence of increasing the delay. A way to overcome this problem is to increase the tail current.

This set the designer in front of a strong trade-off between speed (and its mismatch and processing variations) and current consumption.

3.3.2 Differential input pair with cross coupled load

In the previous solution it is clear how the delay was fulfilling the basic requirements. However some problems arise when the circuit has to be optimized in order to reduce the mismatches and processes variability. Therefore a way to cope with this problem is to design a faster comparator, so that its delay can be increased when the statistical requirements have to be fulfilled.

A possible solution could be the use of a cross coupled configuration (Figure 3.13). In fact the cross couple introduces a positive feedback in the circuit, that provides a reduced propagation delay. Moreover this type of load can even present an hysteresis that comes from the positive feedback. However this function will not be used since the introduction of the hysteresis does not let achieve the lowest delay [4].

Inside this circuit there are two path of feedback: a negative feedback path, a current-series feedback through the common source node of M1 and M2, and a positive feedback,
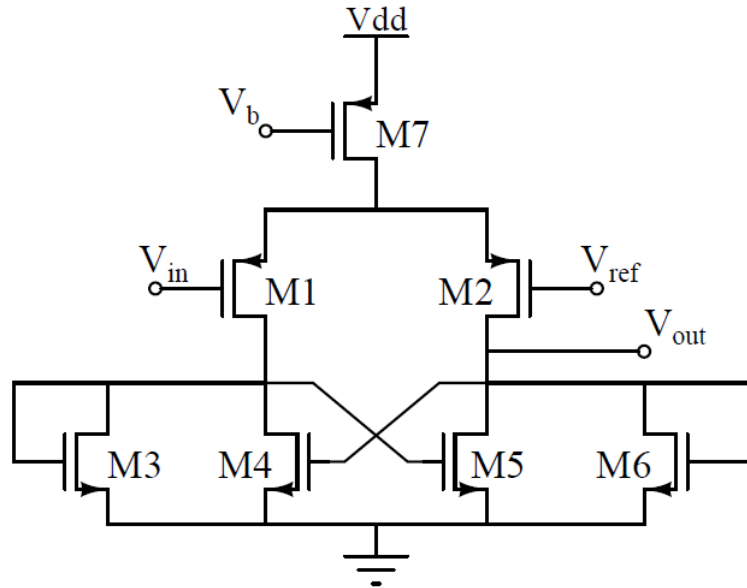
FIGURE 3.13: Cross coupled comparator circuit.

a voltage-shunt that takes place through the gate of M4 and the drain of M5 and vice versa[4].

The positive feedback can be easily understood looking at the small signal variations in the output voltage node. Assuming a small signal decrease of ΔV_{out}, it means a decrease of M4 gate voltage. This fact leads to a decreasing of I_{d4} (through g_{m4}). The drop of I_{d4} forces an increasing of I_{d3} with the result of enhancing the gate voltage of transistor M5, that leads to an increasing of I_{d5}. Therefore this enhanced current discharges the output capacitance and contributes to a further decrease in the output voltage. If the opposite initial assumption is made (small signal increase of ΔV_{out}) the effect and the analysis are analogous.

The same deductive reasoning is applied for the negative feedback path; assuming a small signal drop of ΔV_{out}, this leads to a decreasing of I_{d4} and therefore of I_{d1}. However the current biasing the input differential pair is constant and a I_{d1} drop forces an increase of I_{d2}. This current charges the output capacitance, working against the discharge carried out by the positive feedback.

If the positive feedback dominates over the negative feedback, then the circuit shows an hysteretic transfer function, while when the negative feedback dominates over the positive one the circuit shows no hysteresis. The circuit shows hysteresis when the W/L of M4 and M5 is bigger than that of M3 and M6.

An histeretic behaviour is not required in the comparator, therefore the cross couple

(a) V_{out} *of the 24ns ramp input.*

(b) V_{out} *of the 111ns ramp input.*
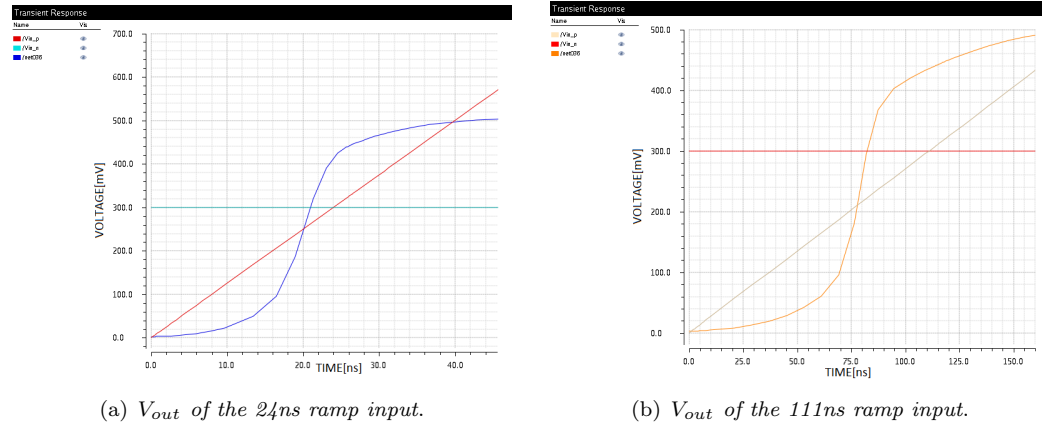
FIGURE 3.14: V_{out}, V_{ref} and V_{in} for the 24ns and 111ns ramp input.

load has transistor M4 and M5 smaller then M3 and M6.

The amplifier uses the negative resistance of the cross coupled to compensate the positive resistance of the diode load and achieve a higher gain [8]. The output resistance is

$$R_{out} \simeq \frac{1}{g_{m6} - g_{m5}} \tag{3.23}$$

The output transconductances of the transistor g_{o2}, g_{o6} and g_{o5} have been neglected since they are negligible compared to g_{m6} and g_{m5}.

Assuming $g_{m1} = g_{m2}$, $g_{m4} = g_{m5}$ and $g_{m3} = g_{m6}$, the dc gain is therefore

$$A_{v0} \simeq -\frac{g_{m1,2}}{g_{m3,6} - g_{m4,5}} = -\frac{g_{m1,2}}{g_{m3,6}} \frac{1}{1 - g_{m4,5}/g_{m3,6}} \tag{3.24}$$

From the equation above it can be seen that if $g_{m4,5}/g_{m3,6} = 1$ the gain could be infinite[8].

An important disadvantage of this amplifier is the limited output swing. In fact the diode-connected transistors clamp the voltage. Therefore, as it is possible to see from figure 3.14, the lower voltage V_{oL} is zero but the higher voltage V_{oH} is only a diode forward voltage over $0V$. Clearly this is not the way of operation expected from a comparator; it is necessary to add a second stage able to provide a higher gain and a full-swing output.

The simplest solution is to use a push-pull second stage (figure 3.15). This is mainly an inverter stage whose current is given using the diode load as a mirror and therefore uses the mirrors to perform a diffential to single-ended conversion. The gain will be higher than in the previous circuit and it is given by:

$$\frac{\Delta V_1}{\Delta V_{in}} = -\frac{g_{m1,2}}{g_{m3,6}}\frac{1}{1-R} \quad \text{with } R = \frac{g_{m4,5}}{g_{m3,6}}$$

$$\frac{\Delta V_{out}}{\Delta V_1} = -g_{m10}(r_{o10}\|r_{o11}) \tag{3.25}$$

$$\Rightarrow \quad A_{v0} = g_{m10}(r_{o10}\|r_{o11})\frac{g_{m1,2}}{g_{m3,6}}\frac{1}{1-R}$$

The transistor are chosen so as not to show an hysteretic behaviour, as it has been done in the previous case.
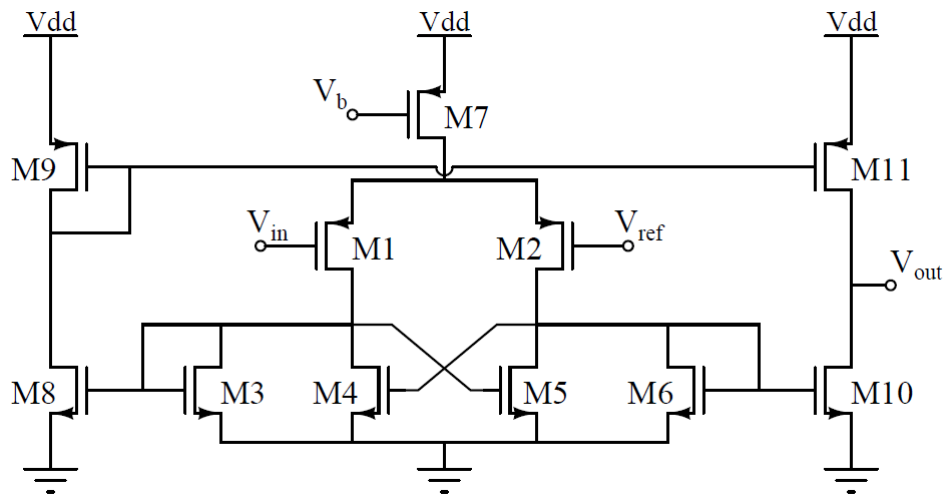
FIGURE 3.15: Cross coupled with push-pull output stage comparator circuit.

Results

The comparator realized with this topology shows a nominal delay time of $t_p = 2.87ns$ for the $24ns$ input ramp and $t_p = 6.76ns$ for the $111ns$ input ramp. These results have been accomplished using the same tail current of the previous circuit, $I_{tail} = 10\mu A$. Comparing the two results, it is possible to see how the choice of using a cross-couple load in order to decrease the time delay was correct. In figure 3.16 the output of the comparator for the two ramps is shown. Since the comparator has low gain, two output inverters have been added in order to give the correct output. It is possible to notice that they do not add a considerable delay time. Moreover the gain of the comparator is increased since they can sink a lot of current for a small period of time.

Figures 3.17 and 3.18 are obtained from a Monte Carlo analysis.

The results obtained are summarized in table 3.2.

(a) V_{out} *of the 24ns ramp input.*

(b) V_{out} *of the 111ns ramp input.*
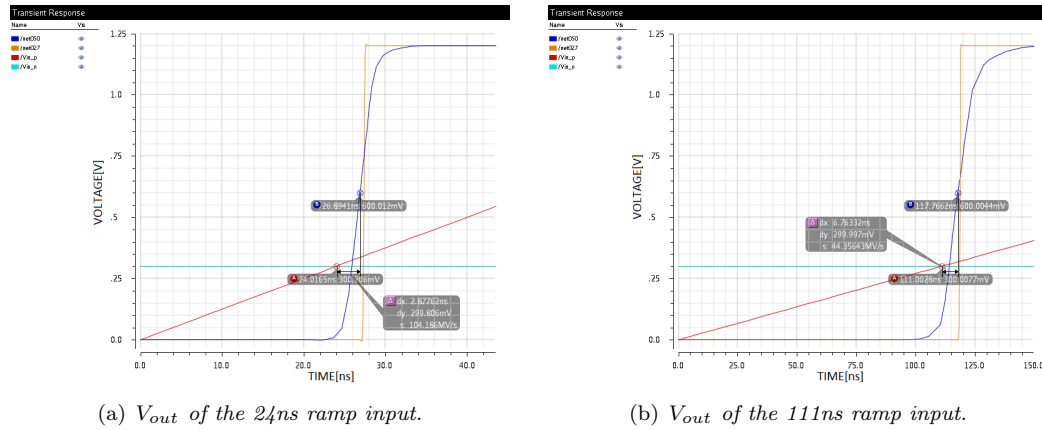
FIGURE 3.16: V_{out}, V_{ref}, V_{in}, delay time and the inverter output for the 24ns and 111ns ramp input.

(a) *Monte Carlo runs.*

(b) *Gaussian distribution.*
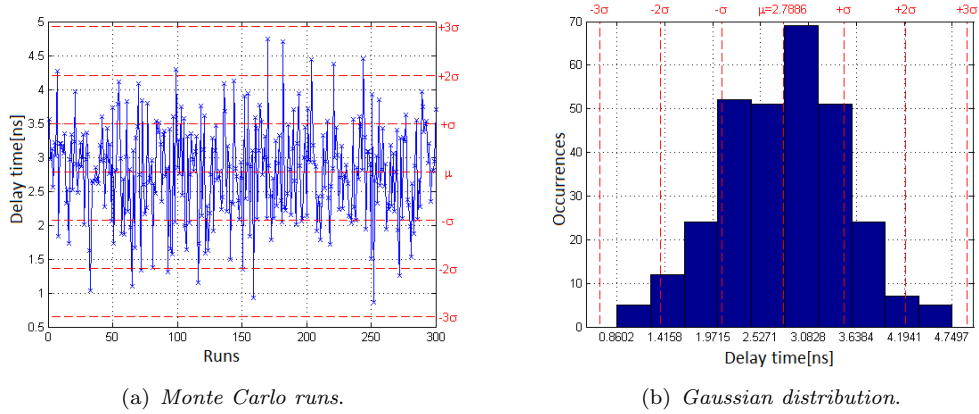
FIGURE 3.17: Statistical results for the 24ns period.

(a) *Monte Carlo runs.*

(b) *Gaussian distribution.*
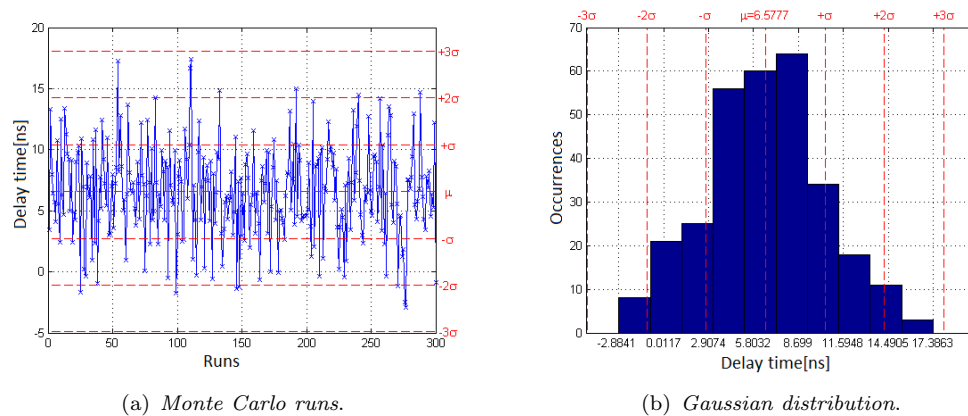
FIGURE 3.18: Statistical results for the 111ns period.

$\mathbf{T_{on}}$	μ_{t_p}	σ_{t_p}	σ_{t_p} **in % of** t_p		$\mathbf{I_{cons}}$
$24ns$	$2.79ns$	$7.1 \cdot 10^{-10}$	25%		$13\mu A$
$111ns$	$6.58ns$	$3.83 \cdot 10^{-9}$	58%		$13\mu A$

TABLE 3.2: Cross-couple push-pull comparator Monte-Carlo results

It has been found from the correlation table that in this case the devices responsible for the unsuitable standard deviation are the transistors that form the load (M3, M4, M5, M6). This is mainly related to the small dimensions of transistors M4 and M5. In fact small devices have been used in order to obtain a fast comparison and avoid the hysteretic behaviour. Unfortunately small devices have by definition a small gate area $(W \cdot L)$ and therefore they are more susceptible to random mismatches. As a consequence the delay time has a high variation that is related to the current factor and offset voltage mismatches. In fact an input DC sweep simulation reveals a relevant $V_{os} = 6.5mV$ (figure 3.19), and a Monte Carlo shows how its statistical variations are very important (figure 3.20).
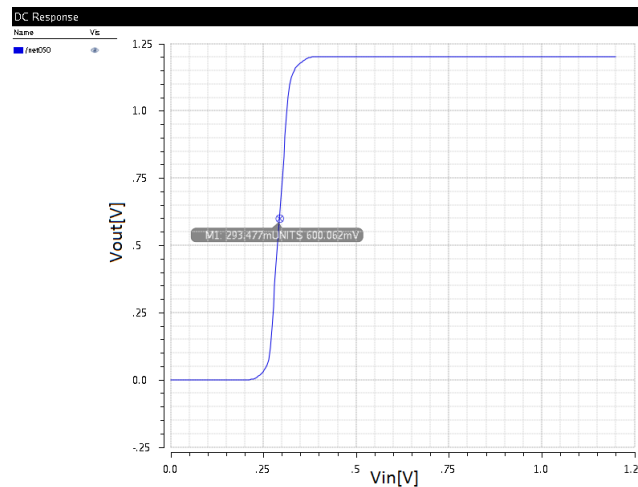
FIGURE 3.19: Input V_{os} of the push-pull cross-coupled comparator.

A way to improve these results is that of increasing the area of the cross-coupled transistors. Increasing the area of these devices leads to a higher delay. For example quadrupling the gate area of transistors M3, M4, M5 and M6 gives a delay time of $4.9ns$, but improves the statistical behaviour of the circuit giving a $\sigma_{t_p} = 0.6 \cdot 10^{-9}$.
Unfortunately the requirements lead to pursue a low delay time together with a limited statistical variation that this circuit is not able to provide. In fact the cross-couple gives the advantage of a fast comparison, but has many disadvantages. Again the limited output swing requires the use of a second stage, adding more delay time and current consumption; secondly the statistical variations are high when small delay time is needed.

(a) *Monte Carlo runs.*   (b) *Gaussian distribution.*
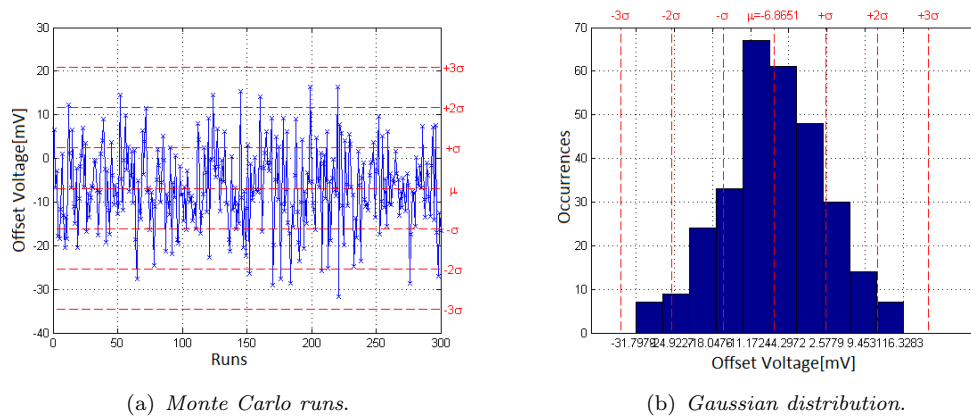
FIGURE 3.20: Statistical results of the input V_{os}.

The increase of the tail current could be a solution, but it is not possible since the fulfilment of the current requirement could not be satisfied.

3.3.3   Self-biased comparator

In the last two sections two different comparators have been analysed. In these two solutions high attention was given to the fulfilment of the delay time requirement, and very little to the consumption requirement.

Both circuits used a tail current of $10\mu A$ that itself exceeds the consumption requirement defined in section 3.2. In addition to the tail current even the current used by the push-pull stage has to be accounted in the average current consumption in a period.

It is therefore necessary to investigate on a way to reduce the current consumption. In the solutions seen, a tail current that continuously flows in the differential pair is used. This sets the minimum current consumption to the value of this current. Obviously it is not a good and efficient solution, since the comparator does not need to operate for most of the period. What really matters is that the comparator can be ready to sense the change of V_{id} sign and so to switch the output from $0V$ to V_{dd} or vice versa. The current that flows when the comparator has already switched and before it switches, can be accounted as a loss current. For this reason it is necessary to pursue an ideal solution able to provide a zero current consumption before and after the switch instant, while it is allowed to have an arbitrary high current in the few nanoseconds in which the comparator switches. In this way the average current consumption in a period can be really low since the circuit is biased only for a negligible time compared to the whole period. Clearly it is not possible to have a comparator that is completely off for the whole period except for the instant of the switch; such a solution implies the knowledge of the switching moment, fact that makes the comparator useless. Let us consider as an example the $24ns$ period; we are looking for a comparator that is switched off with

zero biasing current for $20ns$ and then in $4ns$ must be able to turn on and compare the two inputs, switching the output from V_{oL} to V_{oH}. A similar way of operation would require a suitable digital signal to turn on the biasing current and so the circuit just a few nanoseconds before the end of the period; of course this is quite impossible because we are designing a monostable to give a similar signal, otherwise the entire circuit would be useless. For this reason a good compromise would be to accept a low constant current biasing the comparator and then find a way to enhance this current only a few nanoseconds before the comparison event.

In order to achieve this result, a concept similar to how the push-pull second stage works was used, together with [9]. In fact the push-pull stage operates mirroring the current that flows in the load and uses it to obtain a full-swing voltage output signal. As the input ramp voltage increases, the current steers from M2 to M1, and so the current flowing in the diode load transistor increases. Unfortunately the diode load does not represent a high impedance node, and so a low current determines a low swing of the output node, such small that it does not ensure the saturation of the push-pull second stage output to V_{dd}. On the other hand a high current it is not available since low current consumption has to be pursued. A solution is to use a small biasing current and introduce a self biasing branch that is able to increase the tail current only when the comparator has to switch, which is exactly the moment when most of the current steers from M2 to M1. This self biasing branch mirrors the current of the diode load M6 and adds it as a tail current. In this way it is possible to obtain a current that increases itself as the circuit is approaching the switching point. Unfortunately once the comparator switches to V_{dd}, the self biasing branch continues to bias the circuit with a high tail current, which means a high and useless current consumption, since the comparison has already been done. If a switch is put in series to this branch (e.g. a pMOS), it can disable the self-biasing branch once the output node reaches V_{dd}. The gate of this transistor is then biased by the output voltage of the push-pull stage: when the output is low the self biasing is enabled while it is disabled when the comparator switches and the output goes to V_{dd}. The R_{on} of this switch does not represent a great problem so its W/L can be small. In figure 3.21 there is the entire circuit schematic.

The circuit is exactly the same of the previous section, with the only difference of the adaptive bias branch. Therefore the theoretical analysis is the same as the one done previously, but the calculus are more difficult since the current flowing in the circuit changes during the time of operation. The design process has been developed from the previous circuit. Since the target is to reduce the current consumption, the tail current is reduced from $10\mu A$ to $3\mu A$. The self biasing branch was designed as follows. As it is possible to see from the circuit the load current is mirrored two times, one with a K mirror factor and the other with a K' mirror factor. These two values are chosen such
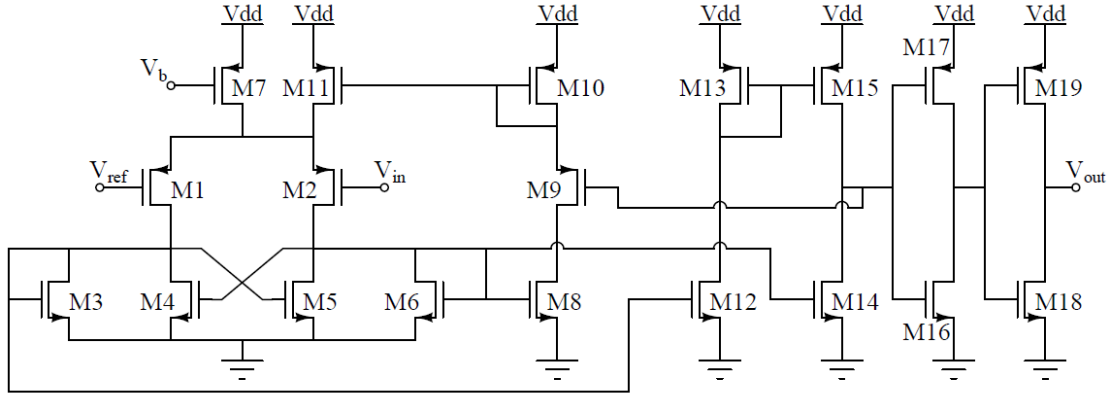
FIGURE 3.21: Auto-bias comparator circuit.

(a) V_{out}, V_{ref} and the 24ns input ramp.

(b) V_{out}, V_{ref} and the 111ns input ramp.
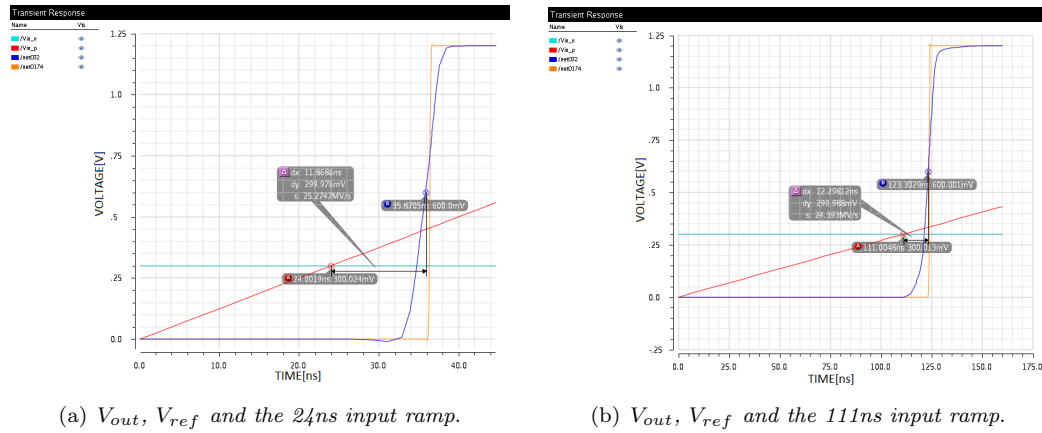
FIGURE 3.22: Output voltage and delay time with 24ns and 111ns input ramp.

that the total tail current (the continuous one and the auto-biasing one) is doubled, so as to keep the average current consumption really low. In figure 3.22 the simulation results are shown for the adaptive biasing current.

When the input voltage ramp crosses the reference, the current steers from M2 to M1 and so the self biasing branch begins to increase the tail current. This adaptive tail current stops to increase as the push-pull output voltage reaches V_{oH} and switches off the adaptive biasing branch. Using this circuit it was possible to reduce the average current consumption in a period, obtaining $\overline{I_{cons}} \simeq 5\mu A$. In this way the current consumption requirement is fulfilled. Unfortunately the circuit shows an increased delay. In fact it becomes $t_p = 11.87ns$ for the $24ns$ ramp and $t_p = 12.3ns$ for the $111ns$ ramp (table 3.3). Clearly the propagation time results are completely unacceptable for the $24ns$ ramp.

A way to reduce the propagation delay is to increase the tail current, but unfortunately then the current consumption increases. Keeping the same continuous tail current and increasing only the auto-biasing one does not greatly affect the overall consumption. In

$\mathbf{T_{on}}$	$\mathbf{t_p}$	$\mathbf{I_{cons}}$
$24ns$	$11.87ns$	$4.98\mu A$
$111ns$	$12.3ns$	$5.02\mu A$

TABLE 3.3: Self-biased comparator results
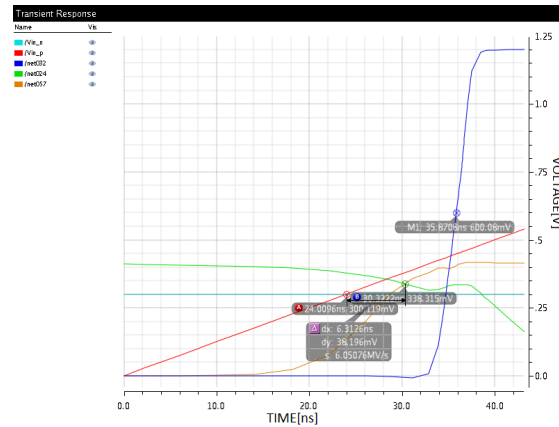
FIGURE 3.23: Output voltage, load voltages and delay time with 24ns input ramp.

fact the self-biasing current is active only for a few nanoseconds, with the consequence that it has a small affection to the average consumption. The design is therefore modified and the self-biased current is doubled; unfortunately the propagation delay does not change too much. The reason of this behaviour can be easily seen in figure 3.23; here the drain voltage of M1 and M2 are shown.

It is possible to see that the increase and decrease of these two nodes in response to the input ramp voltage, are really slow since the voltage gain of the first stage is really low, consequence of the little tail current of $3\mu A$. When the current steers from M2 to M1 branch, the two drain voltages are equal since the current flowing in the two transistor is identical. The self biasing branch begins to work in this moment. Unfortunately it can be seen that the circuit takes $6ns$ to reach the instant in which the two voltages are identical. Figure 3.24 shows that the self-biased current does not affect the voltage variation from the $24ns$ to the $30ns$, therefore the voltage behaviour before the current steering from M2 to M1 is only determined by the $3\mu A$ continuous current. For this reason the only way to reduce the delay time is represented by an increase of the continuous tail current. However this current directly affects the overall current consumption and represents the well-known tradeoff between current consumption and time delay seen in the other topologies.

In this section an auto-biasing comparator has been analysed. The solution has been investigated in order to reduce the current consumption using a bigger amount of current only when needed. This solution allows to comply with the consumption requirement

(a) V_{out}, V_{ref}, V_{in} and the self-biased current.   (b) V_{out}, V_{ref}, V_{in} and the self-biased current.
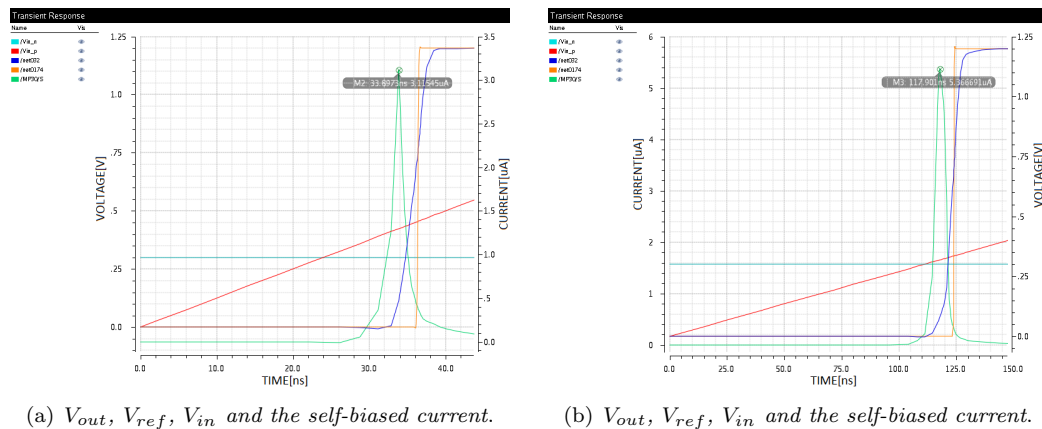
FIGURE 3.24: Self-biased current for $24ns$ and $111ns$ input voltage ramp.

while it does not comply with the delay time requirements. This behaviour is the opposite of the previous topologies. Clearly the sought solution has to be fast enough as the cross couple and the current mirror comparators, but has to employ a self biased current in order to obtain the lowest current consumption. In the next section a comparator able to fulfil all the requirements is described and developed.

3.3.4 Preamplifier with CSDA second stage

In the previous sections various comparator's topologies have been analysed and developed, but none of these fulfilled the requirements. However the tradeoff between delay time and consumption has been investigated and has to be overcomed in order to design a suitable comparator.

The idea of a circuit able to enable itself a biasing current that depends on its input signals has to be pursued, since it allows a great current saving. A circuit that acts itself like a comparator, and provide this characteristic, is the *Complementary Self-biased Differential Amplifier (CSDA)*, analysed in [4], [10] and [11].
The CSDA was firstly introduced by Bazes[10] in 1991. The circuit is obtained through two CMOS differential amplifiers, one with a nMOS and one with a pMOS differential input pair. The loads are deleted and the drains of the nMOS and the pMOS differential pair are connected obtaining the circuit in figure 3.25.

This circuit, however, has an external bias and the two tail transistors have to be biased such that the current that flows in M3 and M4 is identical. Obtaining a similar condition is really difficult, therefore Bazes suggested to connect the gates of M3 and M4 to the drains of M1a and M1b obtaining a self biasing structure with a bias voltage that is inherently stable since there is a negative feedback loop that stabilizes it[10].
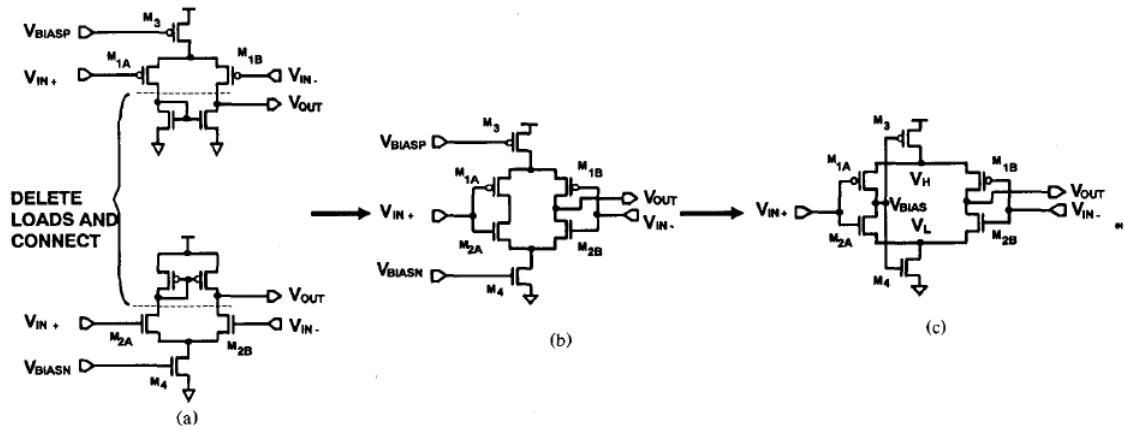
FIGURE 3.25: Derivation of CSDA [10].

The circuit works as follows (figure 3.26): as $V_{in,p}$ increases, the bias voltage V_{bias} drops. This in turn decreases the gate-source voltage of M3 while it increases the gate-source voltage of M4 which means that M3 is switched off while M4 is switched on and carries a great amount of current. On the other hand $V_{in,n}$ decreases (the input voltage is differential) switching off M2a and switching on M2b; in this way the great amount of current that flows from M4 is used to sink the output capacitance, and the output voltage increases and saturates to $V_{dd} - V_{on,M4}$. The advantage of this circuit is given by its ability of sinking a great amount of current obtaining a fast output switching without a large quiescent current. This way of operating is similar to that of the adaptive biasing circuit, but it has the advantage of providing a larger current for a smaller period of time and without "wasting" current in a mirror like the self-biasing branch does. The other advantage of the CSDA is its possibility of providing a full-swing output since transistors M3 and M4 operate in the linear region.

Like in [11] M1a and M1b are designed respectively equal in size and structure to M2a and M2b in order to obtain the identical behaviour for both CMOS inverters. When equal input voltages $V_{in,p} = V_{in,n}$ are applied, then $V_{out} = V_{bias}$, or more generally V_{out} is inclined to behave in the same way as V_{bias}.

In figure 3.27 the small DC signal model of the CSDA is reported. Since M3 and M4 work in the ohmic region, the voltage nodes V_H and V_L can be very close to V_{dd} and $0V$. Therefore a first small approximation in the small signal model could be that of considering $V_{up} = V_{down} = 0$ and neglecting the on-resistances. This approximation provides a little variation of the circuit's real behaviour, but it allows to obtain a simple equation for the DC differential gain, that is:
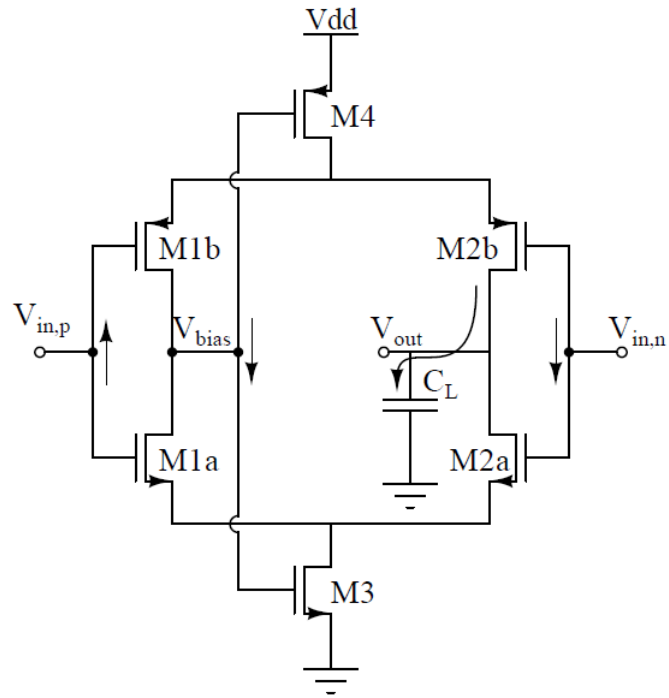
FIGURE 3.26: CSDA's mode of operation.
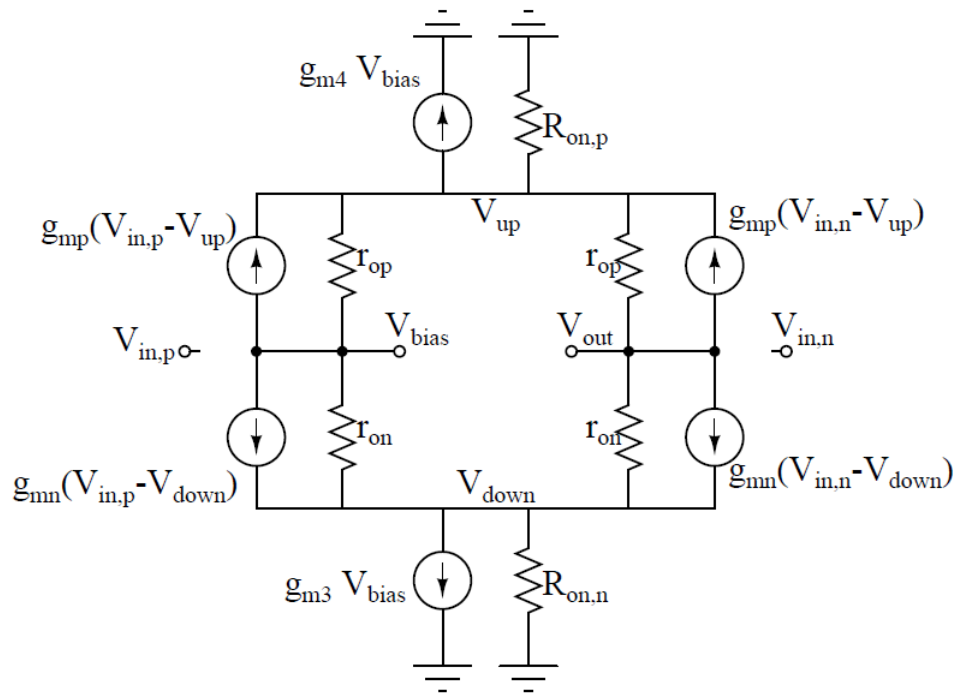
FIGURE 3.27: CSDA's dc small signal circuit.

$$V_{out} = \frac{g_{m,n} + g_{m,p}}{g_{o,n} + g_{o,p}} \left(V_{in,p} - V_{in,n} \right)$$

$$V_{bias} = 0 \tag{3.26}$$

This equation shows that the amplifier is symmetrical and the bias voltage is in a perfect negative loop. However a more accurate calculation of the DC gain is done in [11] and gives

$$V_{out} = \frac{(g_{m,n}g_{o,p} - g_{m,p}g_{o,n})\left[R_{on,n}\left(g_{m,n} + g_{o,n}\right) - R_{on,p}\left(g_{m,p} + g_{o,p}\right)\right]}{\left(g_{o,n} + g_{o,p}\right)^2}V_{in,p} - \frac{g_{m,n} + g_{m,p}}{g_{o,n} + g_{o,p}}V_{in,n} \tag{3.27}$$

The equation above highlights an inherent gain asymmetry of the amplifier, with a smaller gain from $V_{in,p}$ to V_{out}, compared to that from $V_{in,n}$ to V_{out}. The CSDA will be therefore used as an output buffer, as it is suggested in [4]. Its task will be that of amplifying a differential signal coming from a first stage pre-amplifier, and the inverting input will be used, with the consequence that the higher voltage gain has to be taken into account. However in the design, the gain is assumed to be equal to that of equation 3.26 for simplicity.

For what concerns the speed of the CSDA, the gain asymmetry results in a higher delay time from $V_{in,p}$ to the output than from $V_{in,n}$ to the output [4]. However in this case the delay time's difference is not important since the one introduced by the CSDA is much smaller than $3ns$. Moreover, in this case, the CSDA has not to provide a high gain since the buffer is intended to be used as a second stage where the signal has slightly been amplified by a pre-amplifier. Therefore it is possible to focus on a high speed optimization, obtained using devices with small channel length; in [11] it is proved that bigger devices increase the voltage gain but slow the transient response.

The second stage has been defined and described and now it is important to find a suitable first stage. In the previous sections many different amplifiers have been analysed, all suitable to be used as pre-amplifier for the CSDA. Clearly this device should be an amplifier with differential input and differential output, with a very low delay time and low consumption. The CSDA with its self-bias current and its high speed, has a small influence on the overall consumption and delay time. For this reason the pre-amplifier should add a small delay time and work properly with the lowest current consumption. Reviewing the analysed solutions, it is clear how the first comparator (differential pair with current mirror load) it is not suitable since it provides a single-ended output. An active load would not be taken into account because this requires the use of a biasing
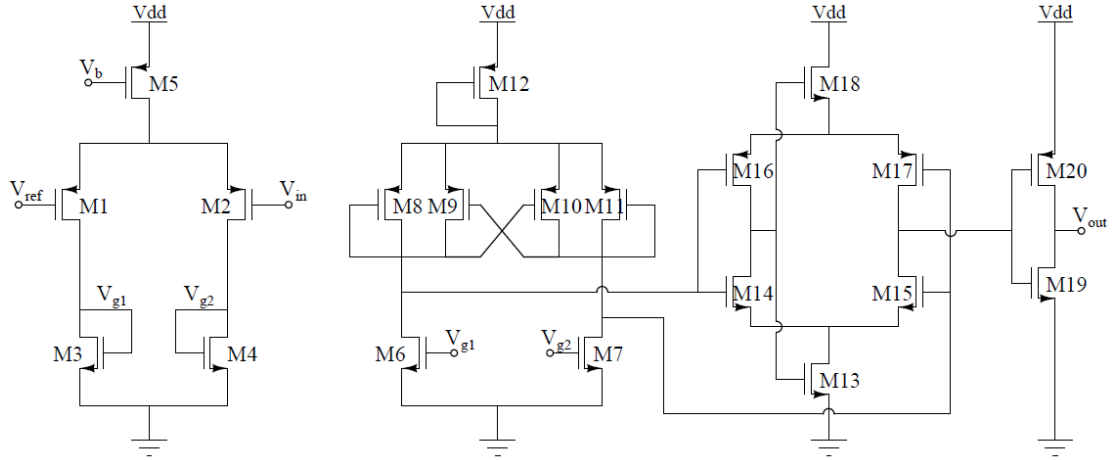
FIGURE 3.28: Comparator suggested in [4].

branch that increases the current consumption. Therefore it is possible to use two diode connected transistors or a cross coupled as load. However the CSDA has an input stage that is mainly an inverter, therefore the voltage at which it shows the maximum gain its around $V_{dd}/2$. This forces the stage before the CSDA to provide a voltage swing centred in $V_{dd}/2$. Unfortunately, as described in the previous sections, the diode connected transistor and cross-coupled loads does not provide a high voltage swing output. To overcome this drawback it is possible to use a second stage as suggested in [4] and reported in figure 3.28. This solution again increases the overall current consumption.

In a first solution two diode connected transistors are used as load. They have been designed such that the voltage output swing is the highest possible (figure 3.29), since the CSDA input common mode is close to $V_{dd}/2$. In order to fulfil this requirement, it is necessary that these diode connected transistors show the lowest g_m ($R_{out} = 1/g_m$) possible, so as to obtain the highest output voltage when $V_{id} = 0$ and $I_{d1} = I_{d2}$. Recalling the equation $g_m = \sqrt{2I_{d1}\mu_n C_{ox}W/L}$ it is necessary to have a low g_m to obtain a high R_{out}, therefore I_{tail} and W/L have to be chosen small. A low I_{tail} then, helps the lowering of the current consumption; however a small current has the consequence of a slower steer of it from one MOSFET to the other of the input differential pair, and so a higher delay. The tail current has been set at $5\mu A$, the W/L of the input transistors has been chosen to be 10, and the W/L of the load transistors is set to 1.

The result of this solution is shown in figure 3.30, where the delay time is equal to $t_p = 2.86ns$ for the $24ns$ ramp and $6ns$ for the $111ns$ ramp, with an average current consumption of $7\mu A$. As it is possible to see from the figure the voltage at which V_{g1} crosses V_{g2} is set to be the highest possible. The requirements are all fulfilled, except for the standard deviation of the time delay.
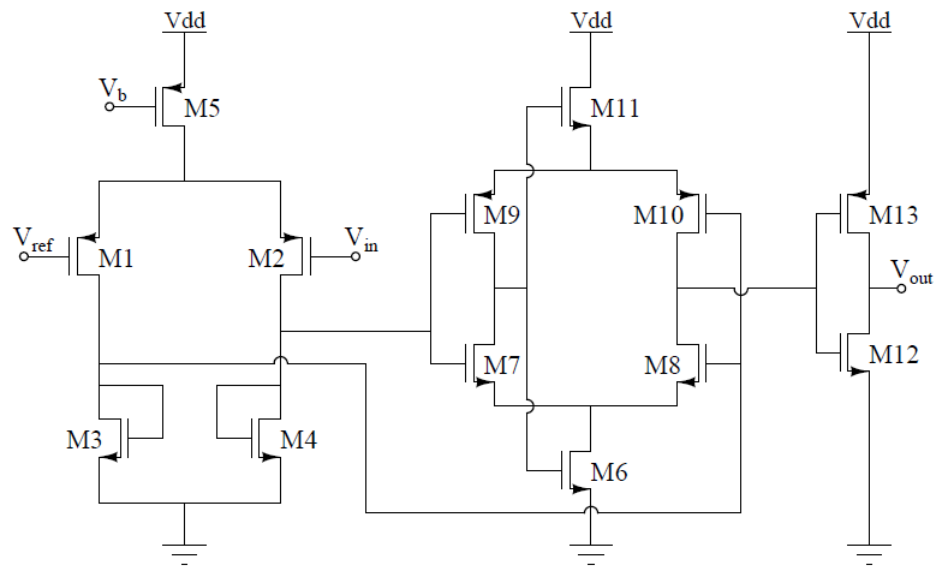
FIGURE 3.29: Schematic of the diode load with CSDA second stage.
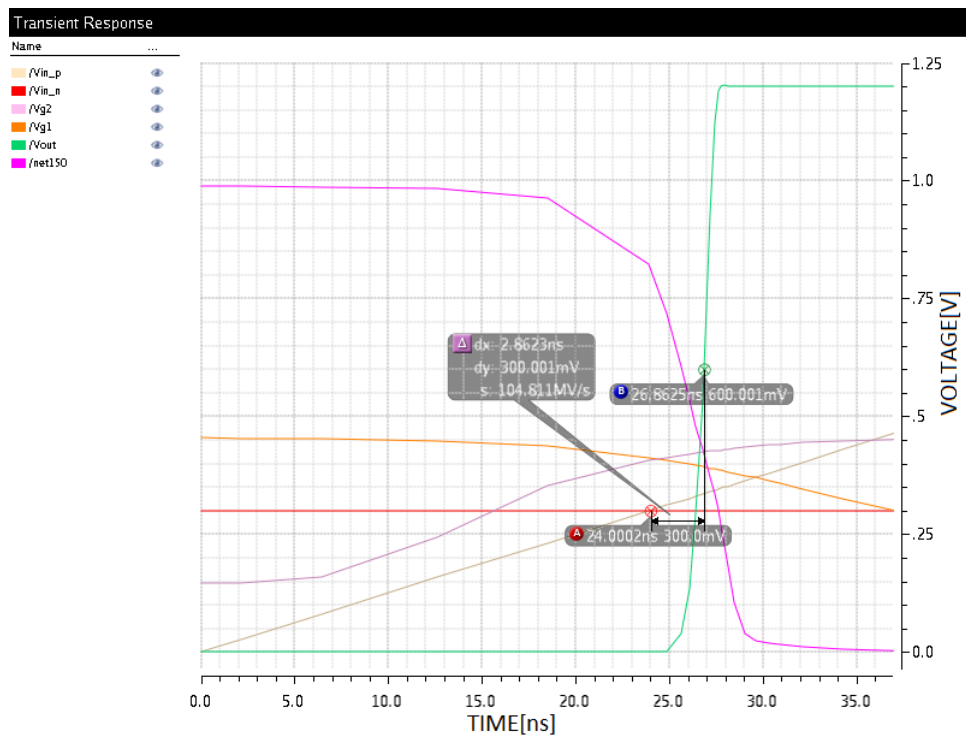
FIGURE 3.30: V_{out}, V_{in}, V_{ref}, $V_{out,CSDA}$ and the the drain voltages of the input pMOSFETs.

A Monte-Carlo analysis is done and the iterations are reported in table 3.4; for every iteration the devices' correlation are reported and therefore their W/L increased in order to match the requirement of $\sigma_{t_p} \leq 0.1 \cdot t_p$; the design optimization will be done for th3 $24ns$ ramp since the more difficult requirement to fulfil regards the faster input.

Iteration	$\mu_{\mathbf{t_p}}$	$\sigma_{\mathbf{t_p}}$	**correlation**	$(\mathbf{W} \cdot \mathbf{L})$ **increase**
1	$2.95ns$	$1.239 \cdot 10^{-9}$	$1.mn3\_vfb\_mm$ 0.513 $2.mn4\_vfb\_mm$ -0.45 $3.mn3\_nch\_mm$ 0.43	$(W \cdot L)_{init}$
2	$3.08ns$	$8.42 \cdot 10^{-10}$	$1.mn3\_vfb\_mm$ 0.514 $2.mn4\_vfb\_mm$ -0.322 $3.nvfb\_snd$ 0.29	$2 \cdot (W \cdot L)_{3,4,init}$
3	$3.55ns$	$6.364 \cdot 10^{-10}$	$1.mp1\_np\_mm$ 0.39 $2.mp2\_np\_mm$ 0.31 $3.mn3\_vfb\_mm$ 0.297	$2 \cdot (W \cdot L)_{3,4}$
4	$3.66ns$	$5.9 \cdot 10^{-10}$	$1.pvfb\_snd$ 0.40 $2.nvfb\_snd$ 0.35 $3.mp2\_np\_mm$ 0.34	$2 \cdot (W \cdot L)_{1,2,init}$
5	$3.81ns$	$4.38 \cdot 10^{-10}$	$1.mn3\_vfb\_mm$ 0.46 $2.mn4\_vfb\_mm$ 0.36 $3.mp2\_np\_mm$ 0.35	$2 \cdot (W \cdot L)_{1,2}$
6	$4.3ns$	$4.29 \cdot 10^{-10}$	$1.mn6\_np\_mm$ 0.45 $2.mp1\_np\_mm$ 0.38 $3.mp2\_np\_mm$ -0.33	$2 \cdot (W \cdot L)_{3,4}$

TABLE 3.4: Monte Carlo design iteration process

Table 3.4 shows how the design process for the improvement of the circuit's statistical behaviour works (explained in appendix A). The iterations necessary to match the requirements for the standard deviation were 6; as it was previously investigated, increasing the devices' area slows the circuit and the fulfilment of the statistical requirement forced the circuit to not be able of satisfying the delay time requirement. The same statistical behaviour is given by a cross-coupled load. Therefore it is necessary to find a different solution for the load. Its task is to amplify the input ramp voltage and obtain a voltage value as high as possible at the moment in which $V_{id} = 0$ and do that with the lowest propagation delay. A resistor is able to provide these tasks: therefore the circuit is redesigned using a resistor as a load. Its value has been decided such that when $V_{id} = 0$ the voltage across it should be around $500mV$ (the tail current is keep equal to $5\mu A$).

$$I_{d1} = \frac{I_{tail}}{2} + \frac{\mu_p C_{ox}}{4} \frac{W}{L} \sqrt{\frac{4I_{tail}}{\mu_p C_{ox} W/L} - V_{id}^2}$$

$$I_{d2} = \frac{I_{tail}}{2} - \frac{\mu_p C_{ox}}{4} \frac{W}{L} \sqrt{\frac{4I_{tail}}{\mu_p C_{ox} W/L} - V_{id}^2} \quad \Big\} \quad \Rightarrow \quad \text{when} \quad V_{id} = 0 \Rightarrow I_{d1} = I_{d2} = \frac{I_{tail}}{2}$$

$$V_{id} = V_{in,p} - V_{in,n}$$

$$\Rightarrow R_{load} = \frac{V_R}{I_{tail}/2} = \frac{500mV}{2.5\mu A} = 200k\Omega$$

$$(3.28)$$

This resistor allows the correct functionalities of the circuit even when all the tail current flows in one branch.

Apart from the propagation delay, the other requirement that needs to be improved is the average current consumption in a period. Therefore some switches are added so that the comparator is switched on when the input ramp voltage starts to increase, and turns off when its output has switched. A switch is added in series to the transistor that provides the tail current. Moreover two switches are used to keep V_{down} at ground and V_{up} at V_{dd} when the input pair is not biased, in order to avoid losses from floating gates. In this way the average current consumption could be lowered up to $3.36\mu A$.

The circuit is showed in figure 3.31.
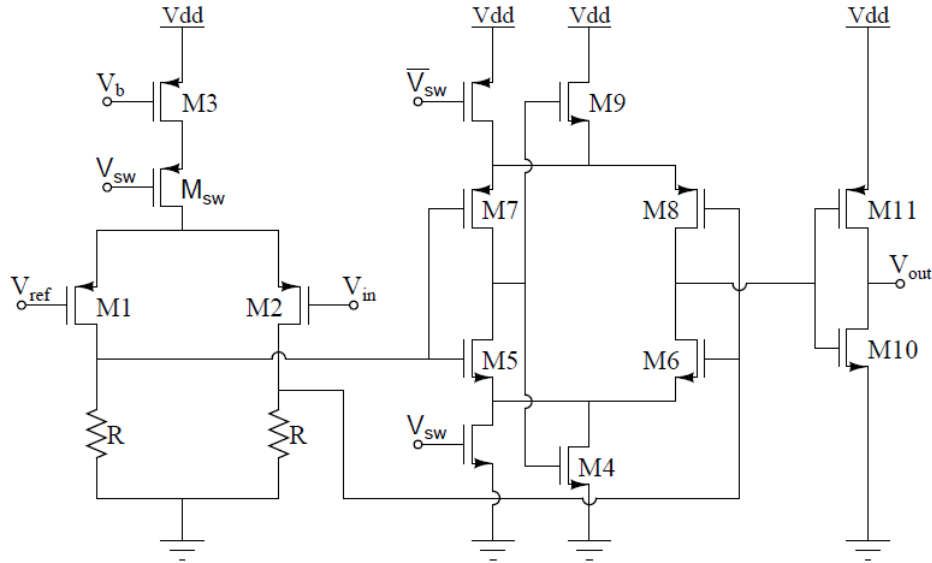
FIGURE 3.31: Schematic of the final comparator.

A transient analysis gives the result in figure 3.33, showing a delay time of $2.42ns$ for the $24ns$ ramp and $3.56ns$ for the $111ns$ ramp. As expected the delay time is lower and

fulfils the requirements.

The average current consumption result to be:

- $\overline{I_{cons}} = 3.36\mu A$ for the $24ns$ ramp, the period is $100ns$ as stated in section 2.3 (3.32(a))

- $\overline{I_{cons}} = 4.11\mu A$ for the $111ns$ ramp, the period is $250ns$ as stated in section 2.3 (3.32(b))

The consumption obtained is the minimum achievable. In fact a possible solution for obtaining a lower consumption could be that of decreasing the current biasing the differential pair. Unfortunately this determines an increased delay time since the input g_m decreases and an increased σ_{t_p} since the g_m/I_d increases (appendix A).

(a) *Comparator characteristic for the $24ns$ ramp and average current consumption (red).*

(b) *Comparator characteristic for the $111ns$ ramp and average current consumption (red).*
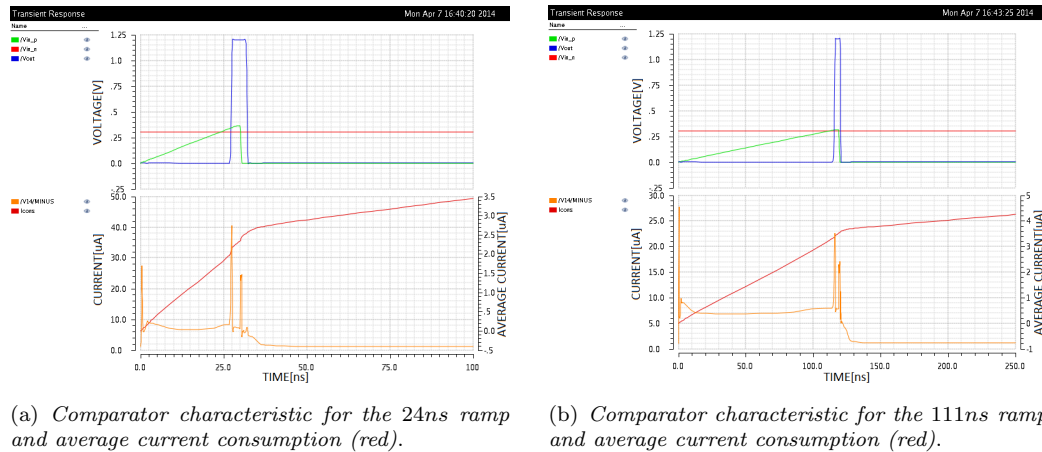
FIGURE 3.32: Comparator current consumption.

A Monte-Carlo analysis is then done as for the previous circuit, obtaining table 3.5.

(a) *Delay time for $24ns$ input ramp.*

(b) *Delay time for the $111ns$ input ramp.*
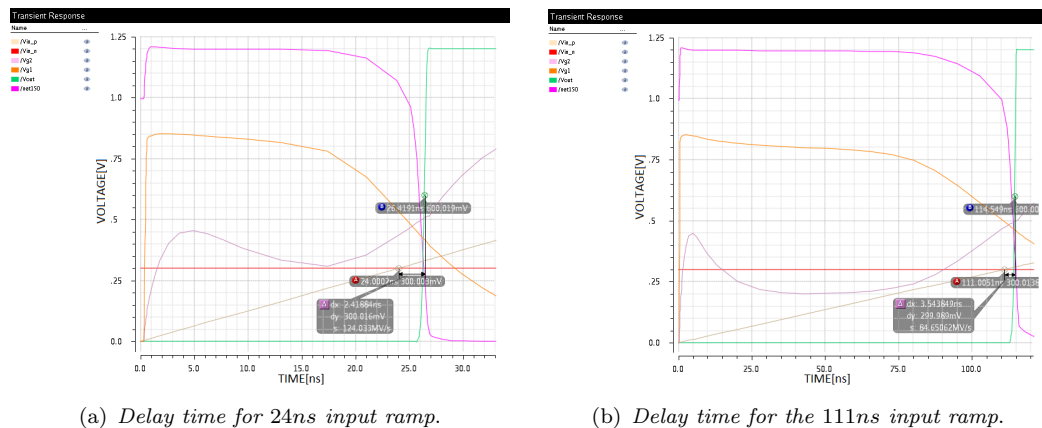
FIGURE 3.33: V_{out}, V_{in}, V_{ref}, $V_{out,CSDA}$ and the the drain voltages of the input pMOSFETs.

Iteration	μ_{t_p}	σ_{t_p}	correlation		$(\mathbf{W} \cdot \mathbf{L})$ increase
1	$2.42ns$	$6.28 \cdot 10^{-10}$	$1.mp1\_np\_mm$	-0.57	$(W \cdot L)_{init}$
			$2.mp2\_np\_mm$	0.52	
			$3.mp1\_vfb\_mm$	-0.41	
2	$2.56ns$	$4.28 \cdot 10^{-10}$	$1.mp1\_np\_mm$	-0.527	$2 \cdot (W \cdot L)_{1,2,init}$
			$2.mp2\_np\_mm$	0.508	
			$3.mp1\_vfb\_mm$	-0.28	
3	$3.19ns$	$3.89 \cdot 10^{-10}$	$1.mp1\_np\_mm$	0.41	$2 \cdot (W \cdot L)_{1,2}$
			$2.mp2\_np\_mm$	-0.40	
			$3.nvfb\_snd$	0.33	
4	$3.38ns$	$3.18 \cdot 10^{-10}$	$1.mp2\_np\_mm$	-0.35	$1.25 \cdot (W \cdot L)_{1,2}$
			$2.nvfb\_snd$	0.338	
			$3.mp1\_np\_mm$	0.30	

TABLE 3.5: Monte-Carlo design iteration process

Using a resistor as a load it was possible to match the requirements in 4 iterations; a delay $t_p = 3.38ns$, the 14% of the $24ns$ period has been obtained; it shows a standard deviation $\sigma_{t_p} = 3.18 \cdot 10^{-10}$, that is the 9.4% of the delay, and more important it is the 1.325% of the monostable time period of $24ns$.

A Monte-Carlo analysis is then done, with the final circuit, for the $111ns$ ramp voltage obtaining a delay time $t_p = 5.05ns$ (the 4.55% of $111ns$) with a standard deviation $\sigma_{t_p} = 1.08 \cdot 10^{-9}$ (the 20% of t_p). At a first sight it should be possible to conclude that the comparator fulfil the $24ns$ period requirements, but not the ones regarding the σ_{t_p} of the $111ns$ period. The correlation table suggests that an increase of the input device area can improve the standard deviation. Unfortunately a further increase of these devices' area slows the circuit, fact that determines a failure in the fulfilment of the smaller period's delay time. For this reason it can be seen how the standard deviation $\sigma_{t_p} = 1.08 \cdot 10^{-9}$ represents the 0.97% of the $111ns$ monostable period. In fact the purpose of the project is to design a monostable and the requirement about the time's precision regards the final monostable period; this consideration lets us conclude that all the requirements are fulfilled and the comparator designed is the solution chosen. In figures 3.34 and 3.35, the Monte-Carlo results for the final design are shown.

Finally it is important to test its statistical behaviour at different temperatures. In the previous simulations the temperature was always set at 27^oC. The circuit is then tested at two corner temperatures: -40^oC and 95^oC. Requirements are not set for these two temperatures, but it is only important to check that the standard deviation does not become greater than the 15% of the delay time. The results are reported in table 3.6, while in figures 3.36, 3.37,3.38 and 3.39 are reported the results of the two Monte-Carlo simulations.

(a) *Monte Carlo runs.* (b) *Gaussian distribution.*
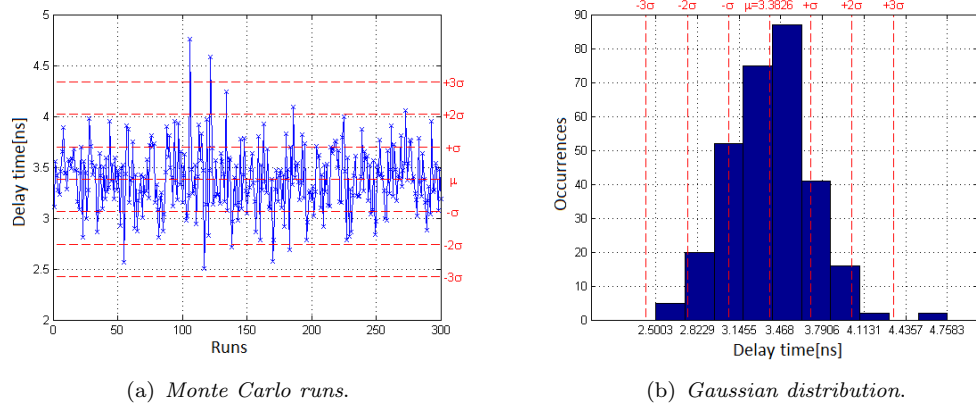
FIGURE 3.34: Statistical results for the 24*ns* period.

(a) *Monte Carlo runs.* (b) *Gaussian distribution.*
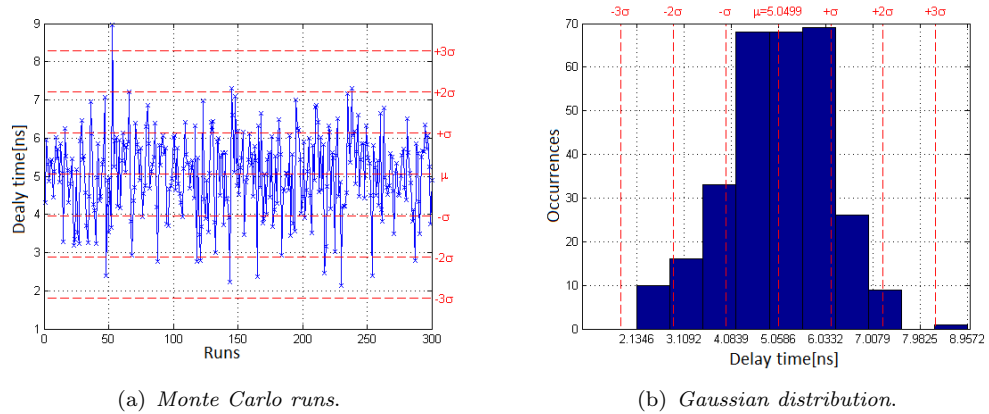
FIGURE 3.35: Statistical results for the 111*ns* period.

(a) *Monte Carlo runs.* (b) *Gaussian distribution.*
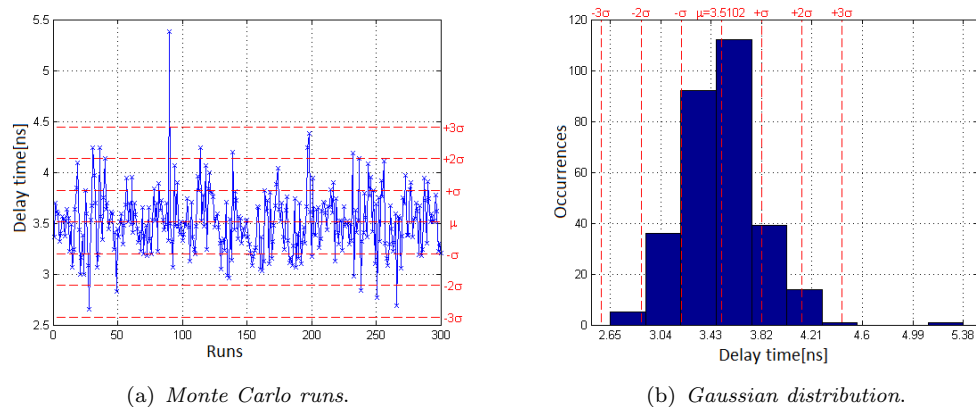
FIGURE 3.36: Statistical results for the 24*ns* period at -40°.

(a) *Monte Carlo runs.*

(b) *Gaussian distribution.*
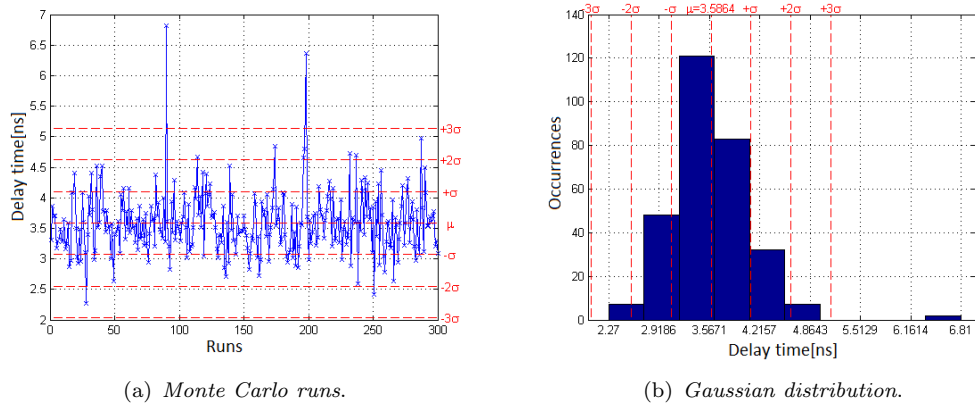
FIGURE 3.37: Statistical results for the $24ns$ period at 95°.

(a) *Monte Carlo runs.*

(b) *Gaussian distribution.*
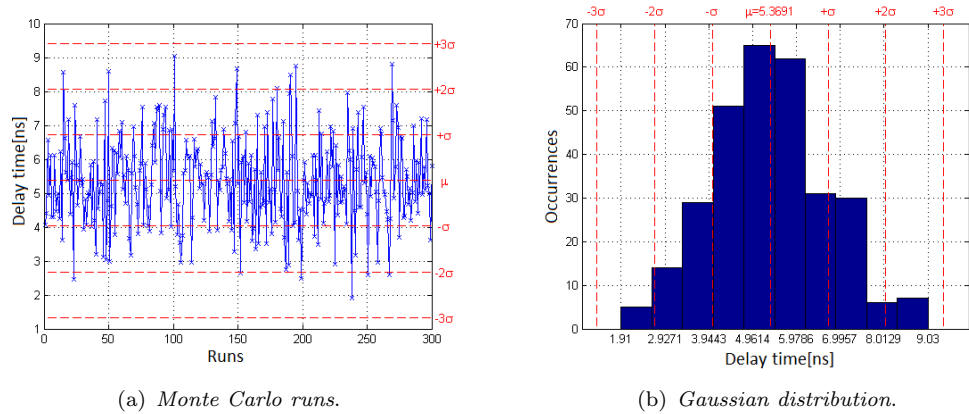
FIGURE 3.38: Statistical results for the $111ns$ period at -40°.

(a) *Monte Carlo runs.*

(b) *Gaussian distribution.*
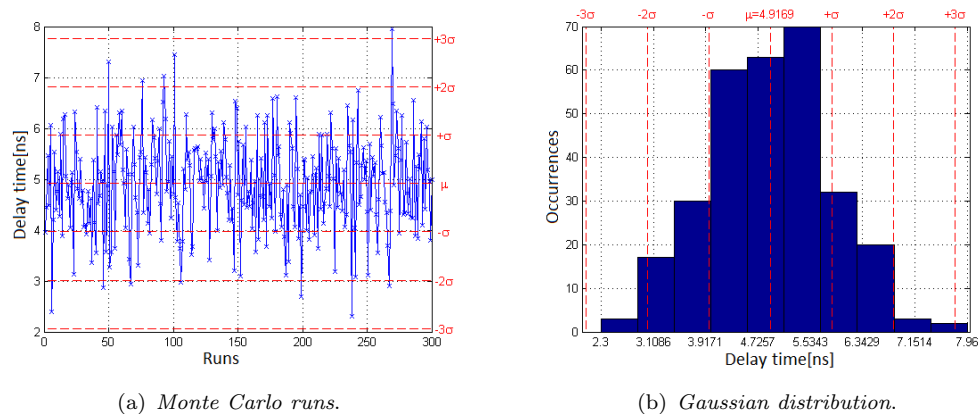
FIGURE 3.39: Statistical results for the $111ns$ period at 95°.

Temperature	μ_{t_p}	σ_{t_p}	σ_{t_p} in % of t_p
-40^oC	$3.58ns$	$5.15 \cdot 10^{-10}$	14.38%
27^oC	$3.38ns$	$3.18 \cdot 10^{-10}$	9.4%
95^oC	$3.51ns$	$3.11 \cdot 10^{-10}$	8.9%

TABLE 3.6: Monte-Carlo temperature analysis for the $24ns$ period.

Temperature	μ_{t_p}	σ_{t_p}	σ_{t_p} in % of t_p	σ_{t_p} in % of T_{on}
-40^oC	$5.37ns$	$1.34 \cdot 10^{-9}$	24.9%	1.2%
27^oC	$5.05ns$	$1.08 \cdot 10^{-9}$	21%	0.97%
95^oC	$4.9ns$	$9.52 \cdot 10^{-10}$	19.4%	0.86%

TABLE 3.7: Monte-Carlo temperature analysis for the $111ns$ period.

Chapter 4

Current generator

In chapter 2 the idea for the realization of the monostable is described. In this chapter the requirements for the voltage-dependent current generator will be set. A first solution with two OTAs used as voltage regulators and another one implemented with two super source followers are described.

4.1 Current generator requirements

The idea for the realization of the monostable is really simple. A capacitor being charged by a voltage-dependent current generator. The current generator is therefore really important because it has to provide a precise current; the statistical variations of this current should be as low as possible since they would directly affect that of the final monostable time period. The other important requirement about this device is the one regarding its current, since the overall current consumption is one of the most important monostable specification.

Therefore the requirements would be:

- $\overline{I_{cons}} \leq 3\mu A$, as a first goal

- $\sigma_{I_{out}} \leq 2.5\% \quad \text{of} \quad \mu_{I_{out}}$

4.2 OTA as voltage regulator

From a first point of view the current generator has to provide a current that depends on the difference between two voltages; this is exactly what a resistor does. Of course the two voltages could not be directly applied to the resistor but a voltage buffer would

be needed. An OTA could be used for the generation of a current proportional to its input voltage.

Therefore it is possible to realize the current generator as it is reported in figure 4.1. This circuit was proposed in the first version of the monostable. It consists of two OTAs used as voltage regulators; the OTA has a common source second stage that has its drain connected to the inverting input in a unity negative feedback loop. A resistor is connected to the drain of the second stage so that the OTA is forced by the negative loop to keep the voltage across the resistor equal to the voltage applied to the non-inverting input. In fact the OTA tends to remain in the operating point $V_{id} = 0$. In order to do that, it works against the small signal output voltage variations with small signal variations of the second stage drain current.

Therefore two currents proportionally dependent on V_{in} and V_{out} are available. These two currents are then copied and subtracted using two current mirrors (figure 4.1).
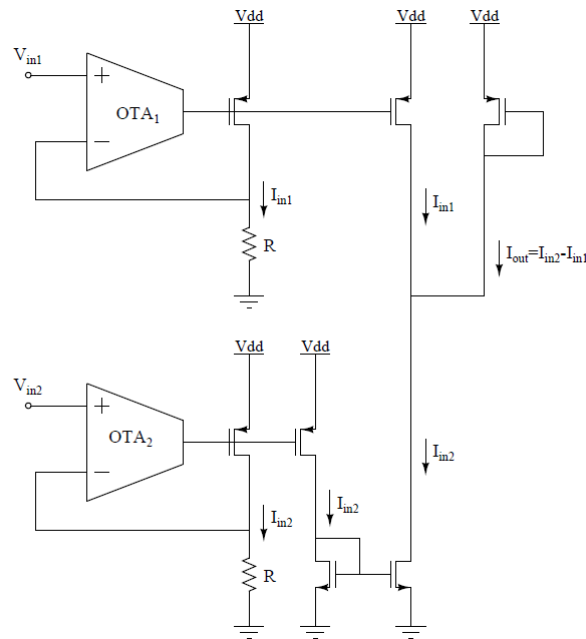
FIGURE 4.1: Circuit for the generation of the current.

4.2.1 OTA voltage regulator design

A voltage regulator is reported in figure 4.2. Usually this circuit is used to provide a reference current from a bandgap reference voltage. For the realization of this device some requirements have been chosen in order to obtain the best voltage regulator possible:

- the static error $\epsilon_0 \leq 0.001$ since it defines the difference between the output voltage and the input one

- the output resistor $R_L = 800K\Omega$ that defines the second stage dc current
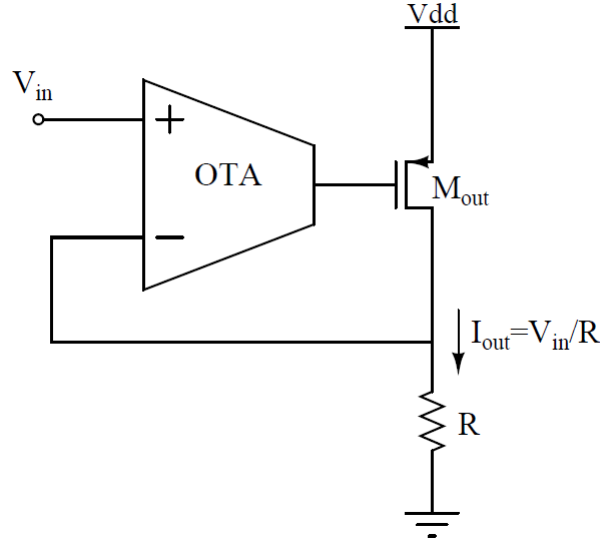
FIGURE 4.2: Linear voltage regulator circuit.

Since the circuit is in a negative feedback loop, it is possible to relate the static error to the dc loop gain $T_0 \simeq \frac{1}{\epsilon_0}$. From the circuit it can be seen that the loop gain is the gain of the OTA times the gain of the common source (figure 4.3, that is

$$T_0 = A_{v0,OTA} \cdot A_{v0,CS} = G_M \cdot R_0 \times g_{m,CS} \cdot (r_o \| R_L) \tag{4.1}$$
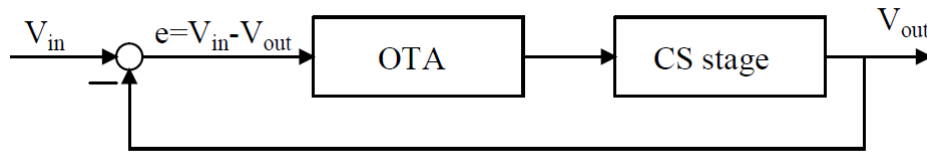
FIGURE 4.3: Voltage regulator block diagram.

The size of the common source transistor can be decided and therefore its gain can be found. In fact its current has previously been defined (e.g. $500nA$) and the overdrive voltage is chosen to be equal to the common value $V_{ov} = 150mV$. After this first assumptions the transconductance of the transistor and its size can be found from

$$g_{m,CS} = \frac{2I_{d,cs}}{V_{ov}}$$
$$\frac{W}{L} = \frac{2I_{d,cs}}{\mu_p C_{ox} V_{ov}} \tag{4.2}$$

With these parameters it is possible to find the gain of the second stage and therefore the gain of the OTA $A_{v0,OTA}$. Once the tail current I_{tail} of the OTA and its devices' channel length are fixed, it is possible to design the OTA such that it can achieve the dc gain found. A simple initial approximation is done assuming the same transconductance and output resistance for all the OTA's transistors. Since the output resistance is fixed by the choices about tail current and channel length, the W/L of the transistors can be found.

Once the circuit is designed, its stability is checked using the Bode criterion. The circuit is mainly a two stage OTA and the stability's considerations are similar to that of a two stage Miller OTA. As stated before, the closed loop gain is therefore given by the gain of the OTA and that of the common source stage. Following the theory of the Miller OTA ([4], [5]), it is possible to find a dominant pole ω_D, a non-dominant pole ω_{ND} and a right half plane zero ω_z that are responsible for the stability of the circuit.

$$
\begin{aligned}
\omega_D &\approx \frac{1}{R_{out,OTA}\left(C_{out,OTA}+C_c\right)+R_{out,CS}\left(C_{out,CS}+C_c\right)+g_{m,CS}R_{out,OTA}R_{out,CS}C_c} \\
&\approx \frac{1}{g_{m,CS}R_{out,OTA}R_{out,CS}C_c} \\
\omega_{ND} &\approx \frac{g_{m,CS}C_c}{C_{out,OTA}C_{out,CS}+\left(C_{out,OTA}+C_{out,CS}\right)C_c} \approx \frac{g_{m,CS}}{C_{out,OTA}+C_{out,CS}} \\
\omega_z &\approx \frac{g_{m,CS}}{C_c}
\end{aligned}
\tag{4.3}
$$

C_c is the compensation capacitor that in the first design is mainly the gate drain capacitance of the common source output transistor. The main problem for the circuit's stability is represented by the right half zero because it can reduce the phase margin. In order to understand if it leads to a non-stable circuit, it is necessary to compare the unity gain frequency of the loop gain with the frequency of the zero; if the latter comes some octaves after the former, then the zero does not represent a problem for the stability and the circuit instability is mainly determined by the two poles.

$$
\begin{aligned}
\omega_c &= T_0\omega_D \approx g_{m,in}g_{m,CS}R_{out,OTA}R_{out,CS}\cdot\frac{1}{g_{m,CS}R_{out,OTA}R_{out,CS}C_c} = \frac{g_{m,in}}{C_c} \\
\frac{\omega_z}{\omega_c} &= \frac{g_{m,CS}}{g_{m,in}}
\end{aligned}
\tag{4.4}
$$

In this case the OTA is a folded cascode (figure 4.4) and it results that $\frac{\omega_z}{\omega_c} \approx 5$. Therefore it is possible to state that the zero should not represent a problem for the stability. A

step input voltage is applied and the circuit's response its checked in order to test the stability and the considerations done.
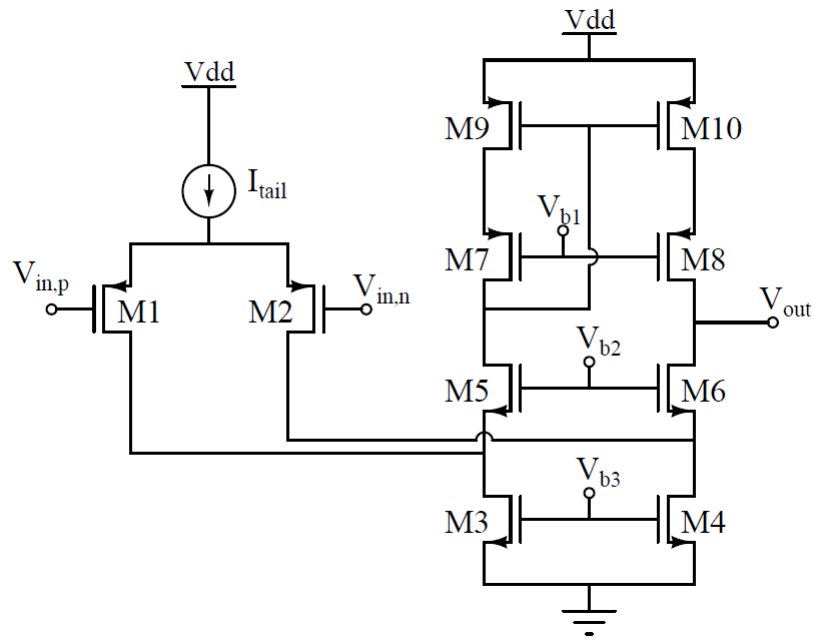
FIGURE 4.4: Folded cascode OTA.

The result of this simulation is reported in figure 4.5 and it comes out that the circuit is stable, confirming that the zero does not affect the stability. However the phase margin is not really high since the overshoot is quite significant.
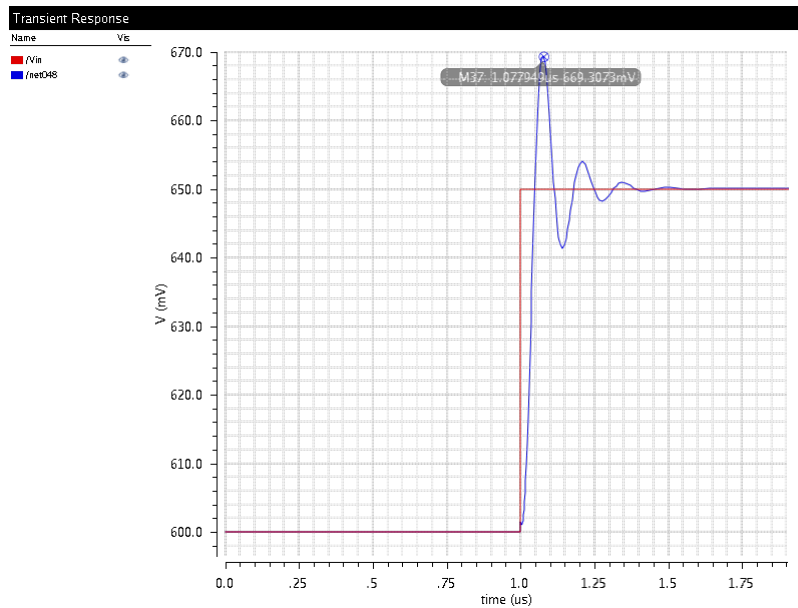
FIGURE 4.5: Step response of the voltage regulator designed.

Using the return ratio method it is therefore possible to simulate and find the magnitude and phase Bode diagram of the loop gain. From figure 4.6 it is possible to notice that the phase margin is only $\phi_M = 29.9^o$.
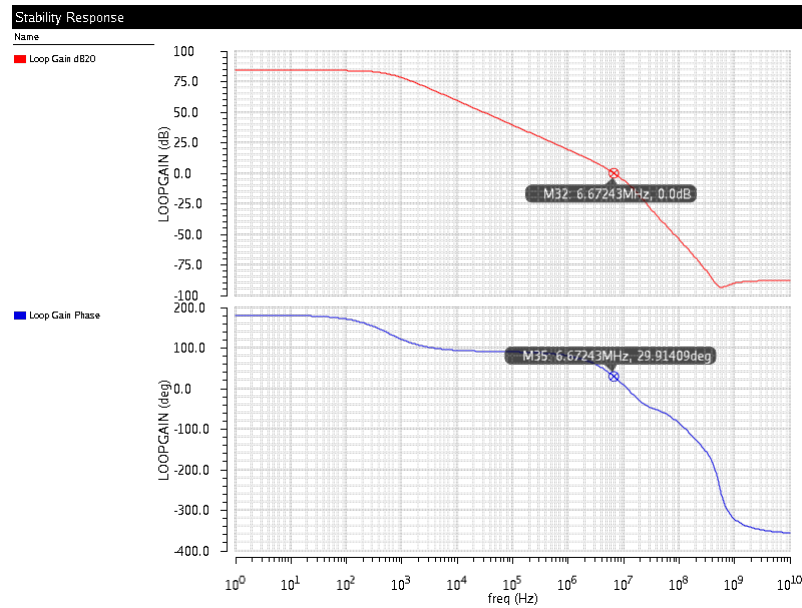
FIGURE 4.6: Voltage regulator's magnitude and phase Bode diagram of the loop gain.

A simple and quick way to increase this gain margin is to increase the pole splitting and anticipate the dominant pole. In this way the unity gain frequency is equally anticipated, with the result of an increased phase margin. A compensation capacitance has been added between the gate and the drain of the common source output stage in order to do that. In figure 4.7 the loop gain's Bode diagram of the compensated regulator is reported and it shows an improved phase margin of $\phi_M = 58.4^o$. The improvement is also evident in the step response of figure 4.8 that shows a reduced ringing. In both step responses it can be noticed a little initial step, consequence of a feed forward, and a little effect of the right half plane zero, since the voltage slightly decreases after the step.

This solution was the one adopted in the previous version of the monostable. Two voltage regulators were used, then the current was copied by a pMOS identical to the output common source device. The two currents were then subtracted by a current mirror. Finally the current for the charge of the monostable capacitance was obtained through another mirror. The main drawback of this solution is its current consumption, as it is possible to see from the figure 4.9. In fact the current that has to be taken into account for the overall consumption calculation is:

- $300nA$ circa for every OTA, since their tail current has been chosen to be $100nA$
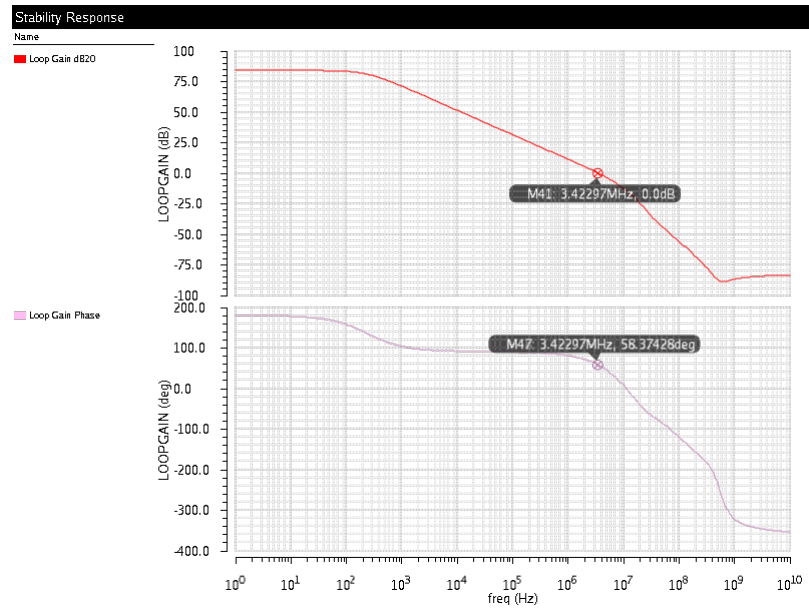
FIGURE 4.7: Compensated voltage regulator's magnitude and phase Bode diagram of the loop gain.
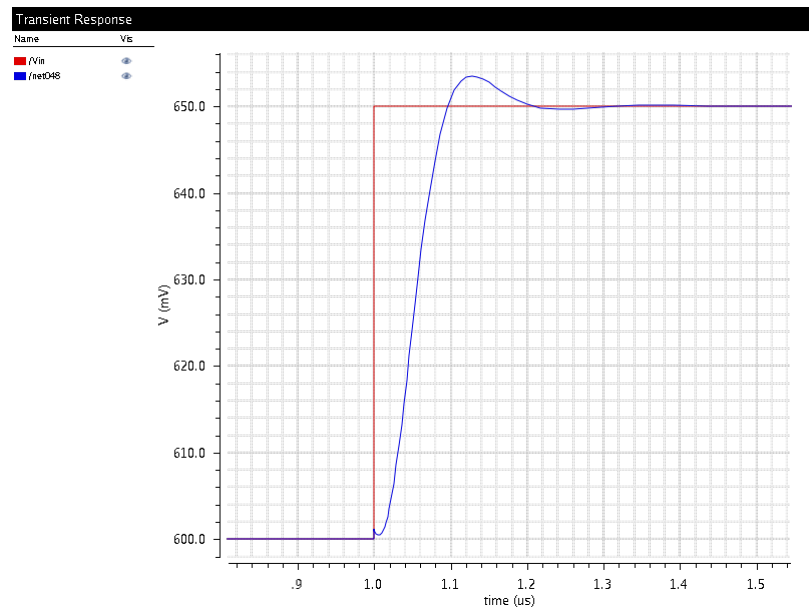
FIGURE 4.8: Step response of the compensated voltage regulator.

- the current flowing in the two output stages. The worst case is when the input voltage is $3.6V$. In this case the output current is $750nA$ while for the voltage regulator concerning the $1.2V$ input voltage the output current is $250nA$

- the current flowing in the mirrors for the extrapolation of the charging current
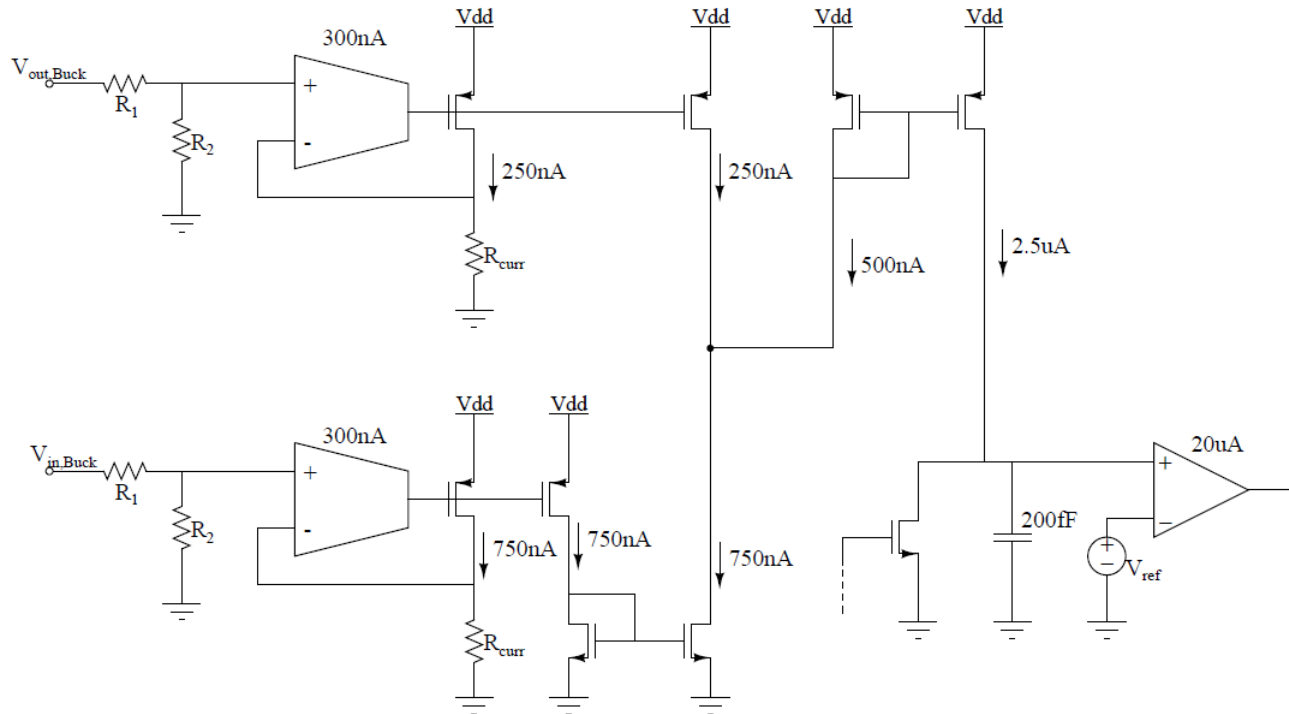
FIGURE 4.9: The previous realization of the current generator using two voltage regulators.

The overall current consumption of the current generator, without considering the final $2.5\mu A$ current, is therefore given by $I_{cons} = \overline{I_{cons}} = 2 \cdot 300nA + 2 \cdot 750nA + 750nA = 2.85\mu A$. This is a current that allows the fulfilment of the consumption requirement; however when the $2.5\mu A$ and the consumption of the comparator are added, it results that the requirement about the current consumption of the entire monostable is barely fulfilled. Therefore it is necessary to investigate on a possible different solution in order to achieve the lowest possible current consumption. From a quick view of this circuit it is clear that most of the current has been lost in the current routing through the mirrors. Thus it is necessary to find a circuit that does not need mirrors for the subtraction of the two proportional currents but is instead able to directly provide a current proportional to the difference between the two input voltages.

4.3 Voltage buffer

The task done by the voltage regulator was that of a voltage buffer. Simple circuits are usually the ones that allows the achievement of a low current consumption. The simplest voltage buffer is the common drain stage or source follower (figure 4.10(a)). In the dc mode of operation the transistor fixes the output voltage to be equal to the input voltage minus (for a nMOS) its gate source voltage $V_{out} = V_{in} - V_{gs}$. The small signal circuit is reported in figure 4.10(b) and it is used to find the small signal gain of the circuit.

(a) *Source follower.* (b) *Source follower's small signal circuit.*
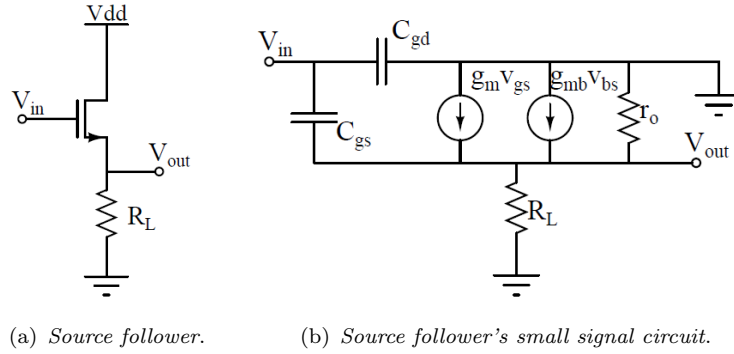
FIGURE 4.10: Common drain circuit.

From a simple analysis, as it is done in [5], it results that the voltage gain is

$$A_v(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{g_m}{g_m + 1/R'_L} \frac{1 + s\frac{C_{gs}}{g_m}}{1 + s\frac{C_{gs} + C_{sb}}{g_m + 1/R'_L}}$$

$$A_{v0} = \frac{g_m}{g_m + 1/R'_L}$$

(4.5)

where $R'_L = R_L \| r_0 \| 1/g_{mb}$.
Analysing the dc gain A_{v0} it is possible to see that it is:

- $A_{v0} = 1$ in the case of an ideal source follower $R_L \longrightarrow \infty$, $r_0 \longrightarrow \infty$ and $g_{mb} = 0$. This means that small variations of the input voltage are equally reported to the output voltage, that is exactly what a voltage follower has to do;

- $A_{v0} = \frac{g_m}{g_m + g_{mb}}$ if the body effect is important. For this reason pMOS source followers are usually preferred since source and bulk can be connected together, obtaining $V_{sb} = 0$ and avoid the body effect;

- $A_{v0} = \frac{g_m R_L \| r_0}{1 + g_m R_L \| r_0}$ in the case that $g_{mb} = 0$, $R_L < \infty$ and $r_0 < \infty$. The higher is the gain $g_m R_L \| r_0$ the closer to 1 is the dc gain.

The last case is the closest to the reality. Unfortunately it shows that it is important to have a high transconductance in order to obtain a good source follower; this implies the use of a high current and we should avoid it. However it is possible to combine high transconductance and low power consumption operating the transistor in a subthreshold region. From a discussion with an analog designer in Texas Instruments, a circuit used in a test chip came out and it was proposed for my monostable current generator. This circuit uses two source followers (super source followers) operating in subthreshold region. These voltage buffers fix the two voltages at the nodes of a resistor in order to extrapolate a current that depends exactly from the difference of the two voltages. In the next sections the subthreshold mode of operation will firstly be described; after that the super source follower and the circuit proposed will be analysed.

4.3.1   Subthreshold operation

Common analog circuits usually work with MOSFETs biased in a normal region of operation in which the drain current I_d is mainly carried by the drift current of majoriy carriers. This way of operation is called strong inversion: in fact when the gate source voltage $|V_{gs}|$ is higher than the threshold voltage $|V_{Th}|$, $|V_{gs}| > |V_{Th}|$, then the drain current depends on the gate source voltage V_{gs} with a square law, if we assume that $|V_{ds}| > |V_{gs}| - |V_{Th}|$ and the channel-length modulation is not important.

$$I_d = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{Th})^2 \tag{4.6}$$

This model suggests that when $|V_{gs}| < |V_{Th}|$, the drain current does not exist, thus $I_d = 0$. In the reality for $|V_{gs}| < |V_{Th}|$, but high enough to create a depletion region, the gate voltage is able to influence either the depletion region charge and the inversion region charge that is really small in this case. However, considering as an example a nMOS, the source n^+ electrons are able to cross the p substrate potential barrier and enter in the channel region. Therefore a transistor in this condition is able to provide a small drain current. In this situation the nMOS operates as a npn Bipolar Junction Transistor, where the source acts like an emitter, the substrate as the base and the drain as a collector[5]. This way of operation is called *weak inversion* or *subthreshold*. In figure 4.11 is plotted the $\sqrt{I_d}$ over V_{gs} characteristic of a nMOS, showing the square law characteristic (being $\sqrt{I_d}$ plot a straight line) and the small current when $V_{gs} \leq V_T$ is highlighted with a log-linear scale figure.

In [5] the weak inversion nMOS is analysed as a npn bipolar transistor and the subthreshold current is found to be

(a) $\sqrt{I_d}$ over V_{gs} transfer characteristic.

(b) $\sqrt{I_d}$ over V_{gs} transfer characteristic plotted in a log-linear scale.
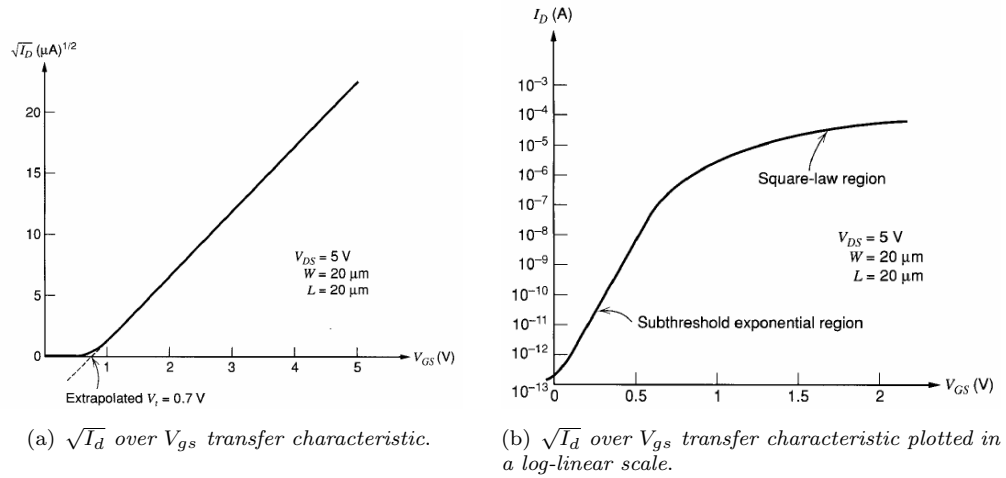
FIGURE 4.11: Transfer characteristic of a MOSFET that shows the weak inversion exponential behaviour [5].

$$I_d = \frac{W}{L} I_t exp\left(\frac{|V_{gs}| - |V_{Th}|}{nV_T}\right)\left[1 - exp\left(-\frac{|V_{ds}|}{V_T}\right)\right] \tag{4.7}$$

where I_t is a constant, $V_T = \frac{k_B T}{q} \approx 26mV$ is the thermal voltage and $n = 1 + \frac{C_{js}}{C_{ox}}$. This last factor models the control of the gate source voltage over the surface potential through a voltage divider over the depletion region capacitance C_{js} and the oxide capacitance C_{ox}; usually $1 < n < 3$[4]. From equation 4.7 it is possible to see that as V_{ds} increases, the last term approaches unity and when $|V_{ds}| > 3V_T$ the transistor can be assumed as a constant current source, assuming the channel-length modulation negligible. This fact shows that the minimum drain source voltage that allows the consideration of the weak inversion MOSFET as a current source is not dependent on the overdrive voltage, differently from the strong inversion model. Therefore as the overdrive decreases and becomes zero, it is necessary to switch from a strong to a weak inversion model. However it is important to point out that this transition does not come abruptly but in between there is a small operating area called moderate inversion, as stated in [5].

In the strong inversion region the transconductance parameter expresses the ability of the MOSFET to provide a drain current variation in response to a gate source voltage variation. Its expression is

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \mu C_{ox} \frac{W}{L}(V_{gs} - V_{Th}) = \frac{2I_d}{V_{V_{gs} - V_{Th}}} = \frac{2I_d}{V_{ov}} \tag{4.8}$$

Differently for the weak inversion operation it results

$$g_m = \frac{W}{L} \frac{I_t}{nV_T} exp\left(\frac{|V_{gs}| - |V_{Th}|}{nV_T}\right)\left[1 - exp\left(-\frac{|V_{ds}|}{V_T}\right)\right] = \frac{I_d}{nV_T} \tag{4.9}$$

In [12] it is highlighted that the maximum transconductance, for a given drain current, is provide by transistors operating in weak inversion region.

Another fact that deserves a small investigation is the statistical variation of weak inversion MOSFETs in relation to random mismatches that arises between two identically devices. As explained in appendix A these variations are responsible for statistical errors and deviations from the circuit typical behaviour.

Random variations of a transistor's parameter can be characterized by a Gaussian distribution. Once two identically devices are designed, the mismatches between these two transistors can be mainly characterized by a threshold voltage mismatch ΔV_{Th} with a standard deviation of $\sigma_{\frac{\Delta V_{Th}}{V_{Th}}} = \frac{A_{V_{Th}}}{\sqrt{WL}}$, and a current factor mismatch $\frac{\Delta \beta}{\beta}$ with a standard deviation of $\sigma_{\frac{\Delta \beta}{\beta}} = \frac{A_\beta}{\sqrt{WL}}$ [5]. The last two equations suggest that the mismatch is inversely proportional to the square root of the transistor area. In fact the bigger the transistor are, the more likely the random variations cancel them out in two matched transistors. Since the two variations are not correlated, it is possible to express the drain current mismatch of two transistor with equal V_{gs} and the gate source voltage mismatch of two transistors with the same drain current [13]

$$\sigma_{I_d} = \sqrt{\sigma_{\frac{\Delta \beta}{\beta}}^2 + \left(\frac{g_m}{I_d}\right)^2 \cdot \sigma_{V_{Th}}^2}$$
$$\sigma_{V_{gs}} = \sqrt{\sigma_{V_{Th}}^2 + \left(\frac{I_d}{g_m}\right)^2 \cdot \sigma_{V_{Th}}^2} \tag{4.10}$$

As said in precedence the transconductance and so the g_m/I_d factor has a maximum in subthreshold region; thus σ_{I_d} is usually large, while $\sigma_{V_{gs}}$ is instead small. Therefore when designing a circuit operating in subthreshold region, it is important to design current mirrors with large area transistors to improve the current matching.

4.3.2 Super source follower

Previously a source follower has been analysed. Its output resistance was not considered even if it is an important parameter for a voltage buffer, especially if it has to drive a resistor load as our circuit has to do. The output resistance of a source follower is approximately $R_{out} = 1/(g_m + g_{mb})$. Therefore this parameter is sometimes too high

when the transconductance has a small value.

In order to design a better voltage buffer a *super source follower* can be used (figure 4.12(a)). This circuit uses a negative feedback to obtain a lower output resistance.

(a) *Super source follower.* (b) *Super source follower's small signal circuit.*
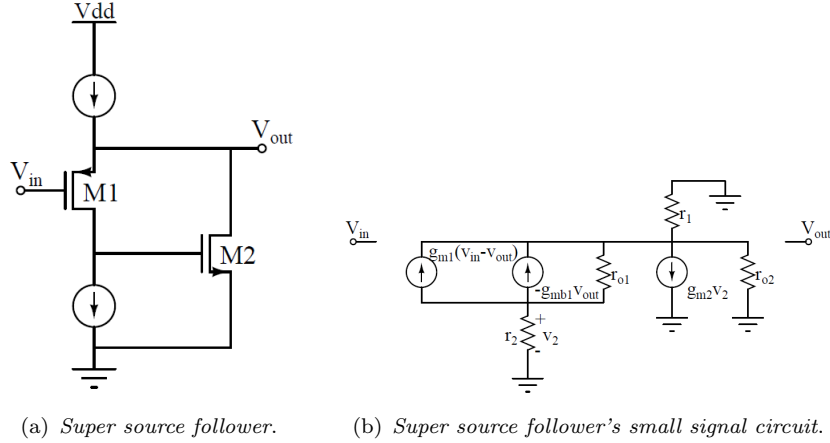
FIGURE 4.12: Super source follower circuit.

Assuming that the input voltage is constant and there is an output voltage increase, the gate source voltage of M1 raises, enhancing the drain current of M1 that in turns increases the gate source voltage of M2. The rise of $V_{gs,2}$ leads to a decrease of the output voltage as M2's current increase. The dc mode of operation is the same as for a normal source follower, with the output voltage equal to the input voltage shifted by the V_{gs} of M1. The dc current that bias M2 is given by the difference between the two current I_1 and I_2, therefore $I_1 > I_2$.

In figure 4.12(b) the small signal circuit of the super source follower is reported. Doing the KCL at the output node it is possible to find the dc gain that is

$$\frac{v_o}{v_i} = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{r_2 + r_{o1}}{(r_1 \| r_{o2})(1 + g_{m2}r_2)}} \tag{4.11}$$

Considering ideal current sources, therefore $r_1 \longrightarrow \infty$ and $r_2 \longrightarrow \infty$, the dc gain simplifies as follows:

$$A_{v0} = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{1}{g_{m2}r_{o2}}} \tag{4.12}$$

Comparing equation 4.12 to the dc gain of the source follower (equation 4.5), it is clear how the one of the super source follower deviates more from the unity gain. However if the factor $g_{m2}r_{o2} \gg 1$, the deviation is really small and it is possible to infer that the super source follower open-circuit behaviour is the same as the source follower[5].

The output resistance is then found. Let us consider a small signal voltage variation ΔV_2 at the output node of the super source follower. This variation has the effect of varying the gate source voltage of the input transistor (V_{in} is assumed to be constant). A variation of the gate source voltage produces a variation in the current flowing in the transistor, that is proportional to its transconductance, therefore $\Delta I_1 = \Delta V_2 g_{m1}$. This current, then, varies the gate source voltage of the second transistor, that determines a variation in its current, that is $\Delta I_2 = g_{m1} g_{m2} r_{o1} \Delta V_2$. The output resistance is then

$$R_{out} = \frac{\Delta V_2}{\Delta I_2} = \frac{1}{g_{m1} g_{m2} r_{o1}} \tag{4.13}$$

Using the Blackman formula or a KCL at the drain of M1, and considering $r_1, r_2 \longrightarrow \infty$ (as in [5]) the result is similar

$$R_{out} = \frac{1}{g_{m1} + g_{mb1}} \frac{1}{g_{m2} r_{o1}} \tag{4.14}$$

The output resistance of a source follower is $1/g_{m1}$, therefore the super source follower configuration reduces it by a factor $g_{m2} r_{o1}$.

The main potential problem of this circuit is its internal feedback loop, that results in instability when it drives a large capacitive load [5]. In this case the load is mainly resistive and it does not show instability. The closed loop gain magnitude and phase Bode diagrams of the super source follower show a phase margin of 47.7^o, figure 4.13. A step input voltage is then applied and shows the stability of the circuit, figure 4.14.
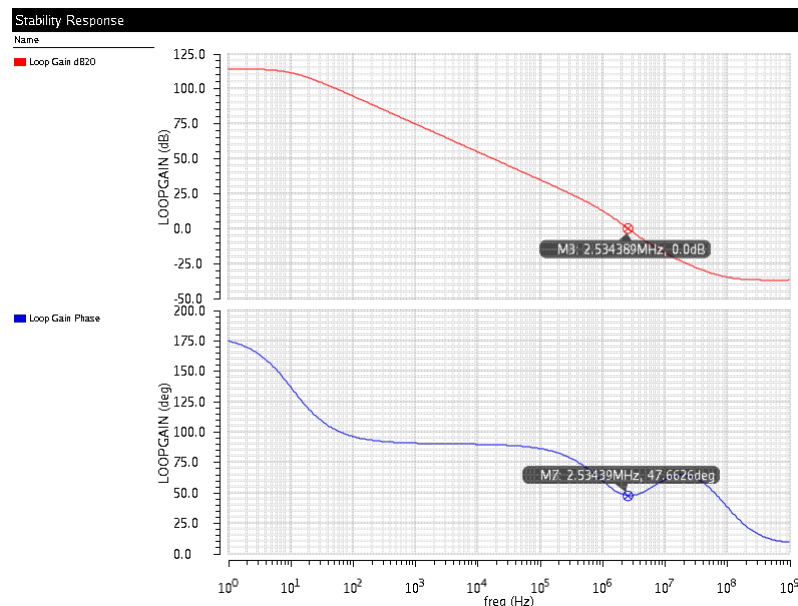
FIGURE 4.13: Super source follower's loop gain magnitude and phase Bode diagram.
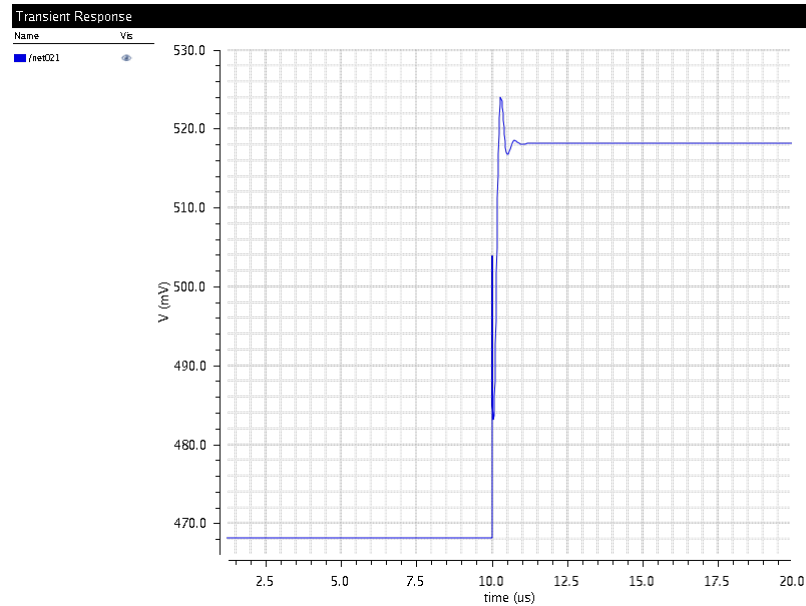
FIGURE 4.14: Step response of super source follower.

4.3.3 Super source follower current generator

Previously it was said that a senior engineer suggested the use of the circuit in figure 4.15 for the generation of the proportional current. The circuit was derived using two different super source follower topologies reported in [14] and [15].
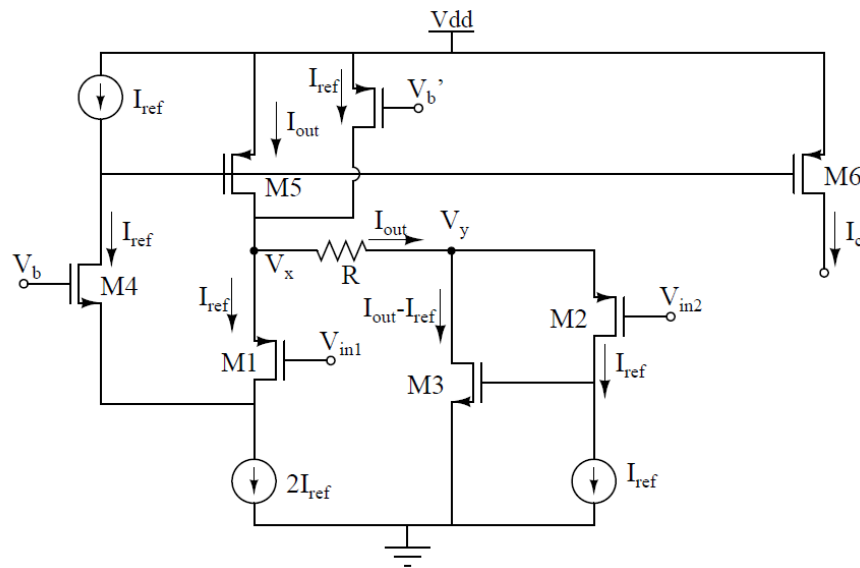
FIGURE 4.15: Circuit proposed for the generation of the $V_{in1} - V_{in2}$ dependent current (implemented from [14] and [15] revision).

How it is possible to notice, there is a super source follower (formed by M2 and M3) that fixes the node V_x the lower voltage $V_{in1} - V_{gs1}$. The other super source follower

is the one composed by transistors M1, M4 and M5 and fixes the higher voltage at $V_y = V_{in2} - V_{gs2}$. Its configuration is slightly different since M5 is used to extrapolate the differential current. The second source follower has therefore a "folded" configuration; in fact transistor M1 is the common drain that senses the input voltage, M4 is in a folded configuration and finally M5 is the actuator of the feedback loop; this configuration is mentioned in [15] as the cascoded flipped voltage follower. The resistor R has then a difference voltage applied at its nodes equal to $V_R = V_y - V_x = V_{in1} - V_{gs1} - (V_{in2} - V_{gs2})$; if $V_{gs1} = V_{gs2}$ then $V_R = V_{in1} - V_{in2}$ and it is therefore possible to obtain a current dependent from the difference of two voltage. This current flows through M5 and M3. The folded configuration enables then the extrapolation of the current using a transistor M6 that copies it.

In order to obtain the condition $V_{gs1} = V_{gs2}$, two pMOS have been chosen as input transistors of the two source followers, since they have the possibility of bonding together source and bulk and avoid body effect. The supply voltage is set to $1.2V$ while the input voltage are divided through a resistive divider by a factor of 6, obtaining $V_{in1} = 3.6/6 = 600mV$, $V_{in1} = 1.7/6 = 283mV$ and $V_{in2} = 1.2/6 = 200mV$. The advantage of this solution is that it can operate in weak inversion, using a low current $I_{ref} = 10nA$. Therefore the consumption is mainly determined by the output current. This has been chosen to be $I_{out} = 500nA$ (when $V_{in,1} = 3.6V$), using a resistor $R = \frac{V_R}{I_{out}} = \frac{V_{in1} - V_{in2}}{I_{out}} = \frac{400mV}{500nA} = 800k\Omega$, value available in the technology used.

The circuit is reported in figure 4.16 comprehensive of the biasing circuit.
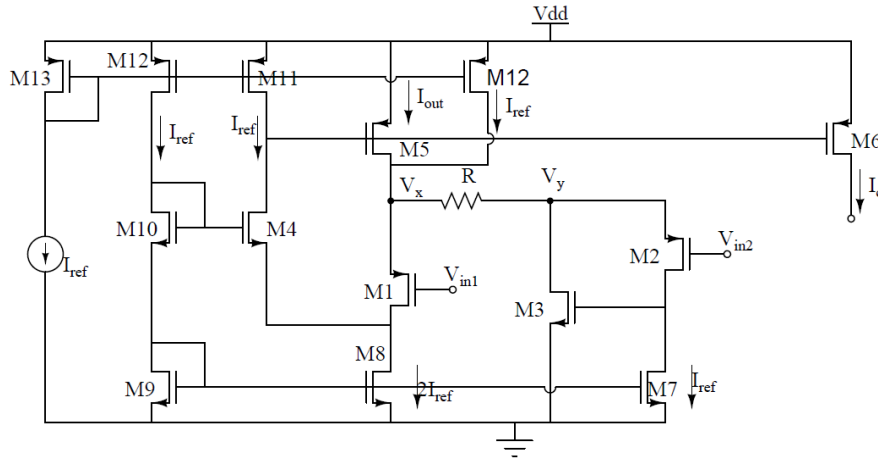
FIGURE 4.16: Circuit proposed for the generation of the $V_{in1} - V_{in2}$ dependent current with the biasing circuitry.

In the circuit design it is important to obtain a high $g_m r_o$ factor for the transistor that actuates the feedback, in order to obtain a voltage gain as closest as possible to 1, as found in equation 4.12. However, operating in weak inversion, it results that $g_m r_o = \frac{I_d}{nV_T} \frac{1}{\lambda I_d} = \frac{1}{n\lambda V_T} \approx 10^3$ that respects the condition $g_m r_o \gg 1$. The transistors

used in the mirror configuration for the biasing, must be chosen with a large gate area, in order to decrease the σ_{I_d}, as suggested in section 4.3.1. Once the circuit is designed, a Monte-Carlo analysis is done in order to verify the standard deviation of the output current in relation to process and mismatch variations. In table 4.1 the design process is reported.

Iteration	$\mu_{\mathbf{I_{out}}}$	$\sigma_{\mathbf{I_{out}}}$	**correlation**	$(\mathbf{W \cdot L})$ **increase**
1	$498.3nA$	$4.28 \cdot 10^{-8}$	$1.res\_siblk\_rb\_snd$ -0.77 $2.m8\_vfb\_mm$ -0.32 $3.m9\_vfb\_mm$ 0.24	$(W \cdot L)_{init}$
2	$496nA$	$3.62 \cdot 10^{-8}$	$1.res\_siblk\_rb\_snd$ -0.91 $2.lint1\_snd$ -0.22 $3.res\_siblk\_rh\_snd$ -0.18	$2 \cdot (W \cdot L)_{8,9,init}$
3	$499.1nA$	$3.53 \cdot 10^{-8}$	$1.res\_siblk\_rb\_snd$ -0.96 $2.lint1\_snd$ -0.19 $3.m13\_vfb\_mm$ -0.16	$2 \cdot (W \cdot L)$
4	$500.97nA$	$3.34 \cdot 10^{-8}$	$1.res\_siblk\_rb\_snd$ -0.967 $2nvfb\_snd$ -0.18 $3.lint1\_snd$ -0.18	$2 \cdot (W \cdot L)$
5	$498.2nA$	$3.28 \cdot 10^{-8}$	$1.res\_siblk\_rb\_snd$ -0.97 $2.lint1\_snd$ -0.20 $3m13\_nch\_mm$ -0.15	$2 \cdot (W \cdot L)$

TABLE 4.1: Monte Carlo design iteration process.

The results show a standard deviation equal to the 6.6% of the mean current. This value is higher than the requirement set in the beginning of the section. Unfortunately it is impossible to obtain a better result from this technology since the statistical variations of the output current are mainly given by the statistical variations of the resistor(97% of correlation). However the consumption of the circuit $I_{cons} = 550nA$ is much lower than the $2.85\mu A$ obtained by the voltage regulators circuit. The advantage given by the lower consumption is so important that suggests the use of this circuit for the generation of the differential current. In order to improve the statistical behaviour, a trimming technique can be used. In figure 4.17 the results of the Monte-Carlo are shown.

(a) *Monte Carlo runs.*

(b) *Gaussian distribution.*

FIGURE 4.17: Statistical results for the output current.
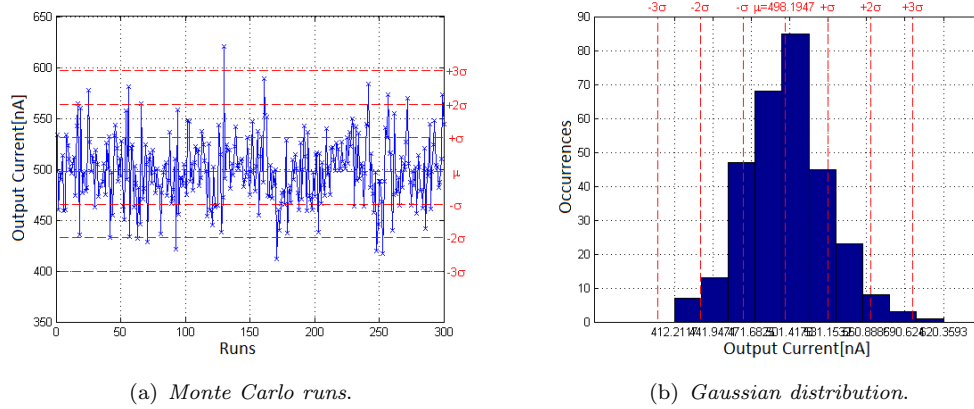
Chapter 5

Monostable implementation

This chapter describes the implementation of the monostable. Therefore the circuit designed are combined together in order to obtain a monostable that fulfils the requirements set in chapter 2.

5.1 Voltage ramp signal generation

The generation of the ramp voltage signal is needed for the timing of the monostable pulse. A ramp voltage signal can be easily obtained charging a capacitor. In fact when a constant current source charges a capacitor, the voltage at its nodes is a ramp with a slope that depends on the magnitude of the capacitor and of the current; in equation 5.1 this consideration is mathematically shown.

$$
\begin{aligned}
I(t) = C\frac{dV(t)}{dt} &\implies V(t) = V(t_0) + \frac{1}{C}\int_{t_0}^{t} I(\tau)d\tau \quad with \quad I(\tau) = I_C \\
V(t) = V(t_0) &+ \frac{1}{C}I_C(t - t_0)
\end{aligned}
\tag{5.1}
$$

Once a current and a capacitor are fixed, the voltage increases of a quantity $\Delta V = V(t_1) - V(t_0)$ in a time $\Delta t = t_1 - t_0$ (figure 5.1) hence

$$
\Delta V = \frac{I_C}{C}\Delta t
\tag{5.2}
$$

The voltage reference has been set to be $300mV$ knowing that its future bandgap realization assures a low current consumption. Therefore the time interval Δt and the voltage
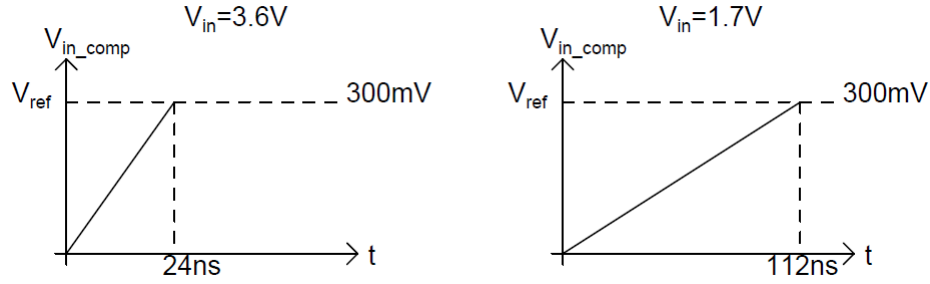
FIGURE 5.1: Ramp signal generated by the current generator circuit for the two extreme Buck's input voltages.

interval ΔV are known and set while the constant current I_C and the capacitor C have to be chosen. The current varies depending on the input and output voltage of the Buck converter and it increases as the difference increases. Differently as the time interval increases, the current I_C proportionally decreases, as equation 5.2 states. Therefore the maximum charging current is the one that defines the smallest period of $24ns$, while the lowest I_C is the one that defines the longest period of $111ns$. An important requirement is the one regarding the current consumption, therefore the value of the capacitor is chosen defining the maximum current.

In the previous implementation of the monostable, the maximum current was set to be $I_C = 2.5\mu A$, obtaining a capacitor of

$$C = \frac{I_C \Delta t}{\Delta V} = \frac{2.5\mu A \cdot 24ns}{300mV} = 200fF \tag{5.3}$$

The longest period results $\Delta t = \frac{\Delta V C}{I_C} = \frac{300mV \cdot 200fF}{520nA} = 115ns$, that is slightly higher than the $111ns$ of the requirements. In fact in chapter 2 the smallest period has been set to $24ns$ instead of $23.2ns$. However the difference between the two times is not significant both for the maximum and minimum on time since it does not provide a malfunction or a greater power loss of the Buck converter.

Analysing equation 5.2 it is clear that the slope of the ramp voltage depends on the ratio of I_C and C. Therefore a bigger capacitor forces the use of a bigger current and vice versa. The lowest current consumption is pursued in this design, thus the lowest current possible is used for the generation of the ramp voltage. With ideal circuits the current could be set to an arbitrarily low value, but unfortunately in the reality there are some constraints. In fact using a small current forces the use of a small capacitor but the comparator input capacitance has to be accounted at that node. In fact the comparator has a non-zero input capacitance that results in parallel to the capacitor that is used for the generation of the ramp voltage. Therefore the minimum capacitor

that can be used to obtain the timing signal is the comparator's input capacitance. In chapter 3 the designing for the realization of the comparator has been described and table 3.5 shows that the input MOSFETs area was increased in order to obtain a better result in response to mismatch variations. Unfortunately, the resulting input devices have a considerable gate area, determining an increase of the input capacitance; this results to be $C_{in,comp} = 110fF$. For this reason the lowest current results to be

$$I_C = \frac{\Delta V C}{\Delta t} = \frac{300mV \cdot 110fF}{24ns} = 1.375\mu A \tag{5.4}$$

Once the value of the capacitor has been chosen, the first thing to do is to obtain the I_C from the current generator circuit design. This is done through a pMOS M6 as in figure 4.15. The gate of this device is connected to that of M5, the device in which flows the current that depends on the difference between the input and output voltage of the Buck converter. Since the sources of both transistors are connected to V_{dd}, they have the same gate source voltage. Therefore their mode of operation is similar to that of a current mirror, that is

$$\left. \begin{aligned} I_{d5} &= \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L}\right)_5 (V_{gs,5} - V_{Th})^2 \\ I_{d6} &= \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L}\right)_6 (V_{gs,6} - V_{Th})^2 \\ V_{gs,5} - V_{Th} &= V_{gs,6} - V_{Th} \end{aligned} \right\} \Rightarrow \frac{I_{d6}}{I_{d5}} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_5} \tag{5.5}$$

Since $I_{d5} = 500nA$ then $\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_5} = \frac{1.375\mu A}{500nA} = 2.75$. Once the current generator is able to provide this current, the ramp signal generation is tested. In figure 5.2 is reported the ramp voltage signal generated with the current generator that charges a real capacitor $C = 110fF$ initially discharged, in blue, and an ideal current source charging an ideal capacitor $C = 110fF$, in red. It is possible to notice that the current generator works as an ideal current source in the voltage interval of interest; when the capacitor voltage increases, then the $V_{ds,6}$ decreases carrying M6 out from the saturation region and decreasing the current it can provide.

Non idealities of the reset switch

In the reality the monostable has to provide not only one but many pulses, then a device able to reset the capacitor and discharge it is necessary. This is done by a switch, turned on when the ramp voltage is not needed, it sets to zero the voltage across the

FIGURE 5.2: Ramp signal generated by the current generator circuit (blue) and with an ideal current source (red).

capacitor. Obviously the switch used is a MOSFET, that is a good switch, but it introduces some non-idealities. First of all when it acts as a short circuit, it shows a non-zero on resistance, differently from an ideal switch. In fact when a MOSFET is used as a switch it is biased in triode region, with a current that depends on the V_{ds} (V_{gs} is fixed at V_{dd}) from the equation $I_d = \mu C_{ox} \frac{W}{L} \left[(V_{gs} - V_{Th}) V_{ds} - \frac{V_{ds}^2}{2} \right]$. Assuming $V_{ds} \longrightarrow 0$, it is possible to avoid the $\frac{V_{ds}^2}{2}$ term and relate the on resistance as

$$I_d \approx \mu C_{ox} \frac{W}{L} (V_{gs} - V_{Th}) V_{ds} \Longrightarrow R_{on} = \frac{V_{ds}}{I_d} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{Th})} \qquad (5.6)$$

The on resistance represents a strong non-ideality since it forces the reset of the capacitor to a value different from $0V$. It introduces an offset voltage to the ramp signal equal to $V_{os} = I_{d6} R_{on}$. Therefore R_{on} has to be the smallest possible, in order to keep this voltage very low. For the achievement of this result it is necessary to increase the W/L of the nMOS transistor used as reset switch, as equation 5.6 suggests. Unfortunately the transistor size cannot be indefinitely increased because the parasitic capacitance that it adds is proportional to its gate area $W \cdot L$. This capacitor is then added to the comparator C_{in}. Moreover when a large gate is used, the charge sharing effect has to be accounted in the non ideal effects. In fact as W/L is increased the charge necessary to form the conducting channel also increases; this charge represents a problem when the nMOS is switched off since the channel has to be discharged. Thus a small amount of current flows in the transistor in order to discharge the channel, with the effect of

creating a small negative step in the capacitor voltage. A tradeoff determines the choice between small on resistance and small adding capacitance; a switch with a $W/L = 16$ was chosen, obtaining a $R_{on} \approx 600\Omega$ ($V_{os} = R_{on}I_{d6} \approx 800\mu V$) and a negligible capacitance of $3fF$. In figure 5.3 it is reported the ramp signal of the current generator and the ideal current source with the addition of the MOSFET switch; it is clear how the choices done make negligible the switch's non-idealities.
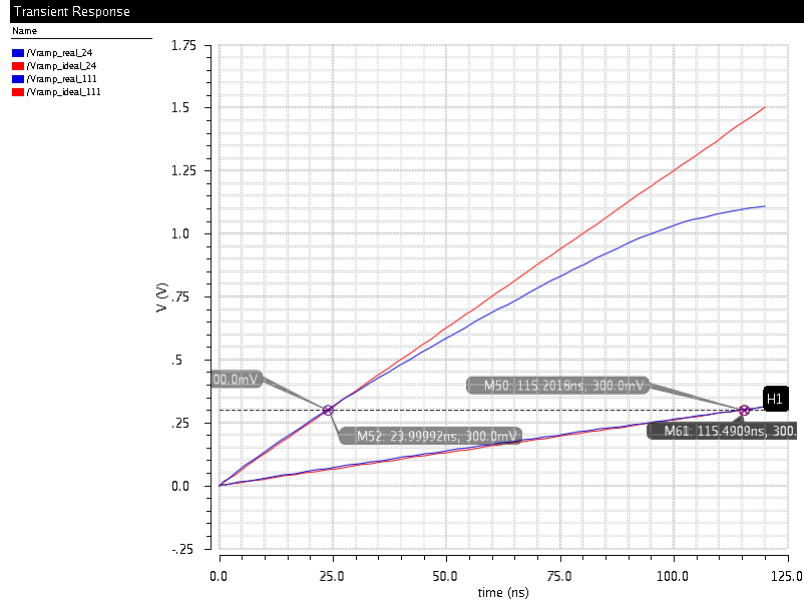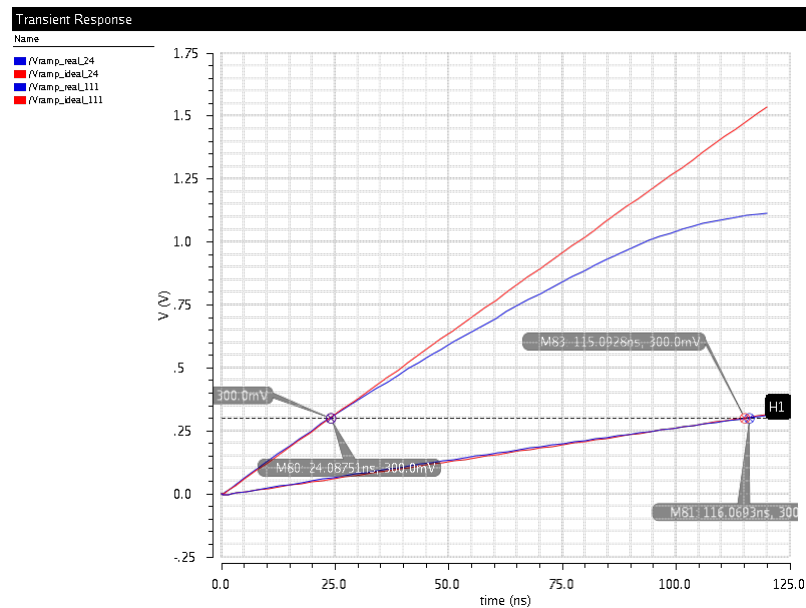

FIGURE 5.3: Ramp signal generated by the current generator circuit (blue) and with an ideal current source (red) introducing the nMOS as a switch.

Comparator insertion

Finally the capacitor is deleted and substituted by the comparator and the ramp voltage signal of figure 5.4 is obtained. The ramp signal is not the one pursued and moreover it has 2 very different slopes. This represents therefore a great non ideality. The effect is mainly determined by the switching behaviour of the comparator. In fact in chapter 3 a switch was added in the biasing branch, in order to obtain a lower consumption. Therefore when the switch is off, the comparator is not biased, the input gate is forced to zero while the other is fixed at the reference voltage. Thus the voltage at the drain of the transistor that provides the tail current is V_{dd}, while the voltage at the drain of the switch at $0V$. The comparator is then biased when the ramp voltage begins to raise. Therefore the triggering input signal turns off the capacitor's switch while it turns on the comparator's biasing switch. In this moment the comparator starts to be biased but its nodes are initially still discharged, and the tail current shows a transient behaviour with a dynamic current higher than the $5\mu A$ set in chapter 3. Since the input voltage

in much lower than the reference one, this current flows in M1 and determines a faster charge of the input capacitance, that last until all comparator's nodes are biased and the tail current is fixed at $5\mu A$. This higher current determines the higher slope of the ramp voltage.
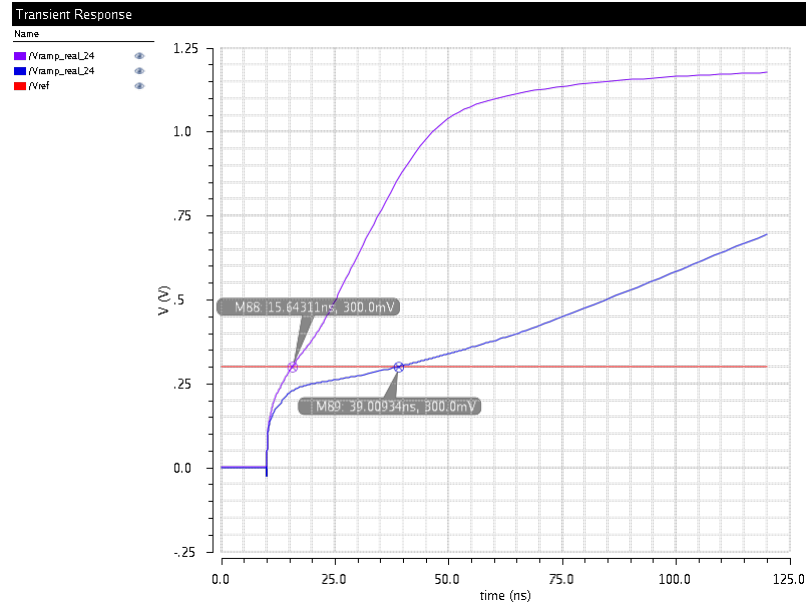
FIGURE 5.4: Ramp signal generated by the current generator circuit charging the comparator's input capacitance.

The comparator designed introduces a strong non ideality, that forces some considerations, in order to be able of overcoming it. A first possibility is that of decreasing the comparator's input capacitance so a small capacitor in parallel to it is enough to make negligible the transient effect. Unfortunately this is not a good choice since the comparator's input devices area has to be decreased, forcing a worsening of the comparator's statistical behaviour.

The other possibility is to add a big capacitor in parallel to the input node so that the input capacitance susceptible to the transient non ideal effect is negligible. A higher capacitor, however, needs a higher current for its charge, increasing the circuit consumption. In figure 5.5 it is possible to see how the transient effect becomes negligible with a capacitor of $220fF$ and a current of $4.125\mu A$.

However, in order to keep the current consumption low, it is possible to cope with this non ideal effect relating it as a kind of offset voltage. Observing the ramp voltage, it is possible to notice two ramps with different slopes, one that is determined by the transient current, and the other one determined by the total capacitance at the comparator's input node. Therefore it is possible to keep the same current and add a small capacitance whose approximative value has been found observing that the first ramp increases by $V_{os} \approx 180mV$ in $t_{os} \approx 5ns$. Therefore the capacitor that has to be added is
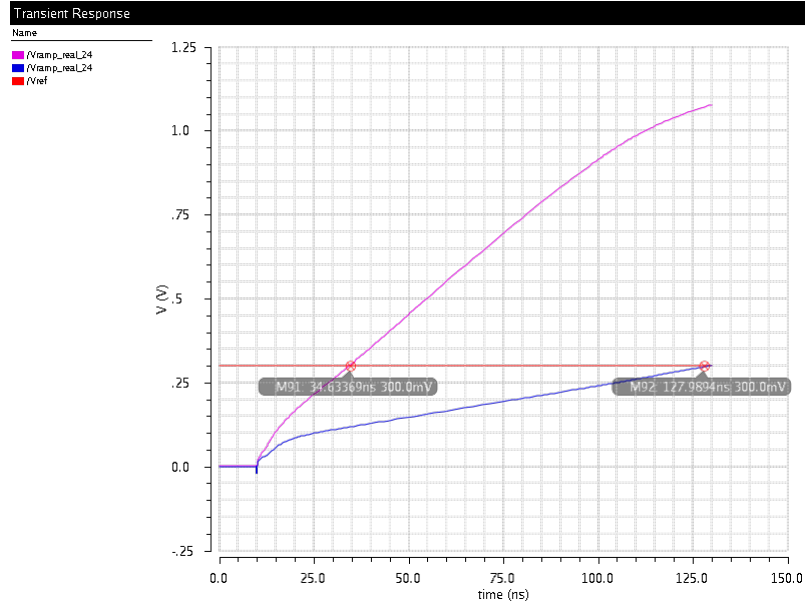
FIGURE 5.5: Ramp signal generated by the current generator circuit with a $220nF$ capacitor and a $4.125\mu A$.

$$C = \frac{I_C\,(t_1 - t_{os})}{V_{ref} - V_{os}} - C_{in,comp} \approx \frac{1.375\mu A\,(24ns - 5ns)}{300mV - 180mV} - 110fF \approx 100fF \qquad (5.7)$$

Adding such a capacitor satisfies the requirements and the two desired voltage ramps can be obtained, as it is possible to see in figure 5.6.
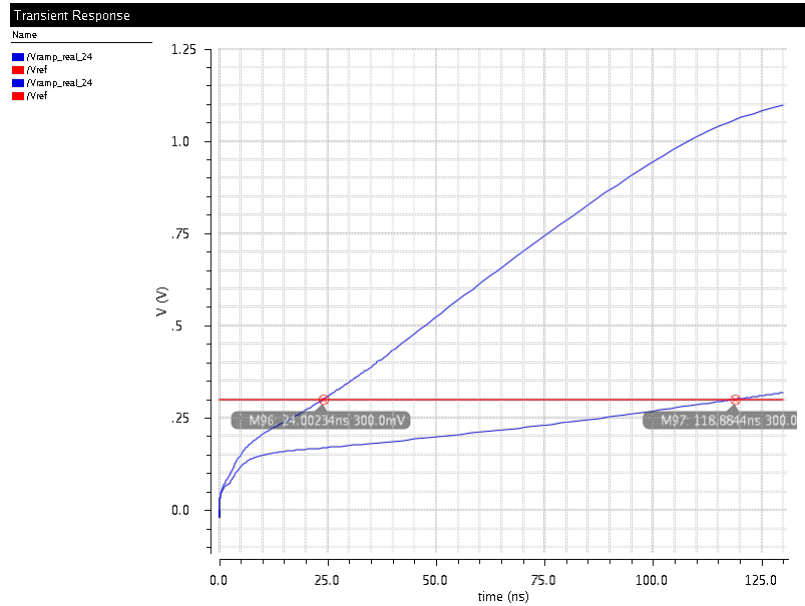
FIGURE 5.6: Ramp signal generated by the current generator circuit with the $100fF$ adding capacitor.

Finally it was possible to find a solution for the generation of the ramp voltage with a lower current consumption than the previous version. The overall old current was approximately $I_{cons,old} = I_{cons,currentgenerator} + I_C \simeq 2.85\mu A + 2.5\mu A = 5.35\mu A$, while in this case it was improved up to $I_{cons,new} = I_{cons,currentgenerator} + I_C \simeq 550nA + 1.375\mu A = 1.925\mu A$.

5.2   Digital reset

The ramp voltage signal that varies proportionally to the difference between the input and output voltage of the Buck converter has been designed. It is now needed a digital circuitry capable of providing the signal for driving the switch and reset the capacitor, together with the output monostable voltage pulse. The starting digital signals are reported in figure 5.7.
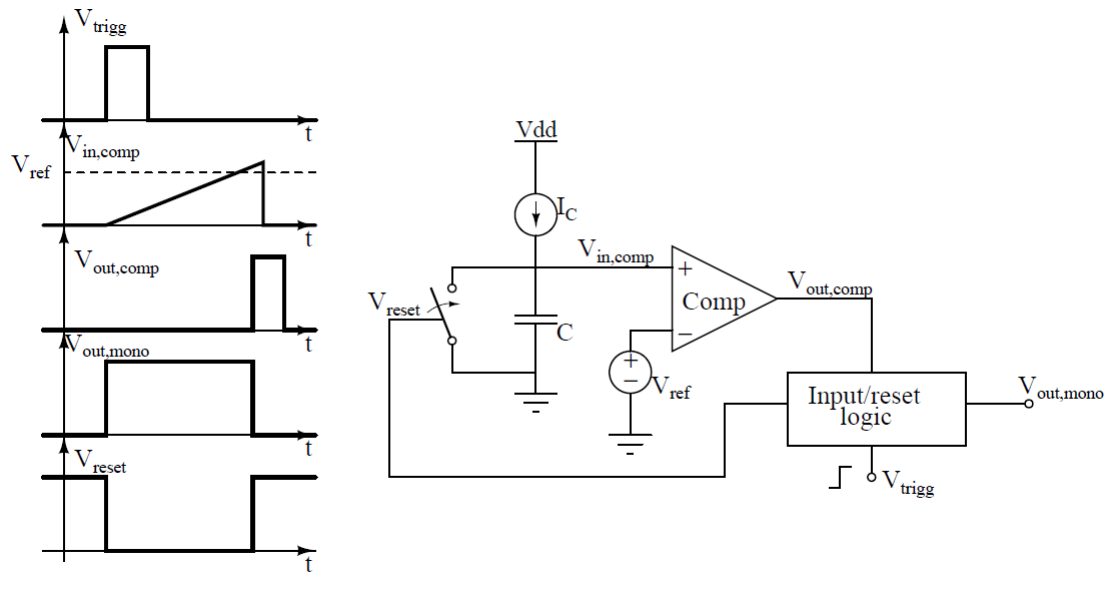
FIGURE 5.7: Signals available for the designing of the digital reset circuit.

The resetting switch is a nMOS and it needs a gate signal V_{reset} equal to V_{dd} when it has to reset the capacitor voltage, while it has to be at zero when the ramp voltage is generated. Differently the comparator's output $V_{out,comp}$ is at zero except after the moment in which the ramp voltage crosses the reference. The monostable output has to be at zero before the trigger signal, at V_{dd} after it and then return to zero after the comparator switches. This signal can be obtained through an **AND** port with $\overline{V_{out,comp}}$ and $\overline{V_{reset}}$ as input signal (figure 5.8. The monostable signal V_{mono}, then, is at V_{dd} when the **AND** input signals are at the logic 1.
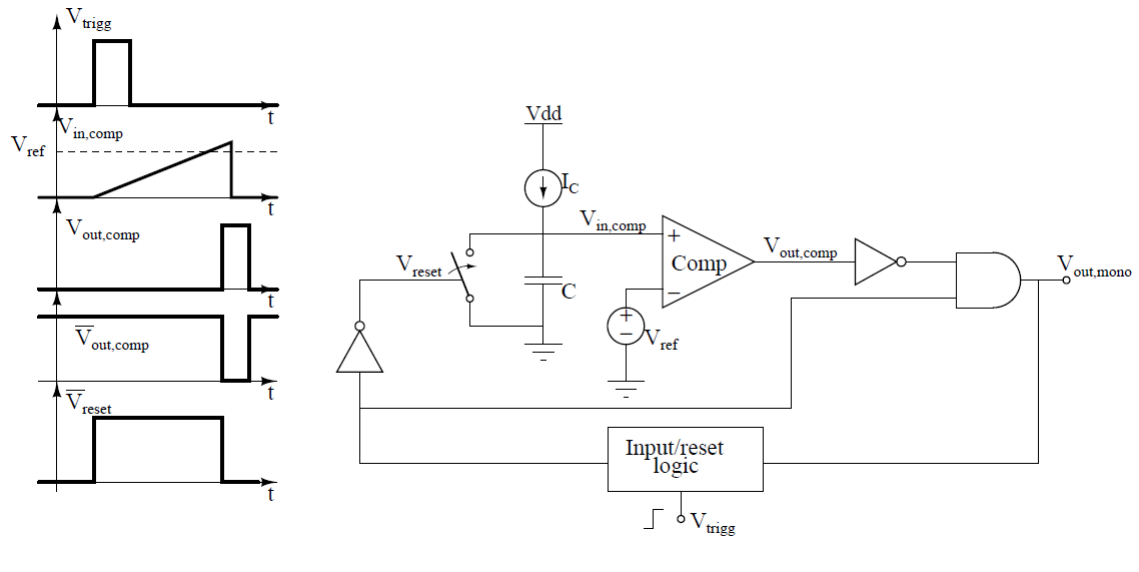
FIGURE 5.8: Introduction of the output circuitry.

It is now important to obtain a correct V_{reset} from the triggering input signal. The monostable has to be edge sensitive and not level sensitive, therefore a D flip-flop is used to provide the beginning of the reset signal. This device gives at the output **Q** the logic value at the pin **D** when the clock has a rising edge (the one of the trigger signal for example), while it gives 0 when the **CLRZ** is set to 0.
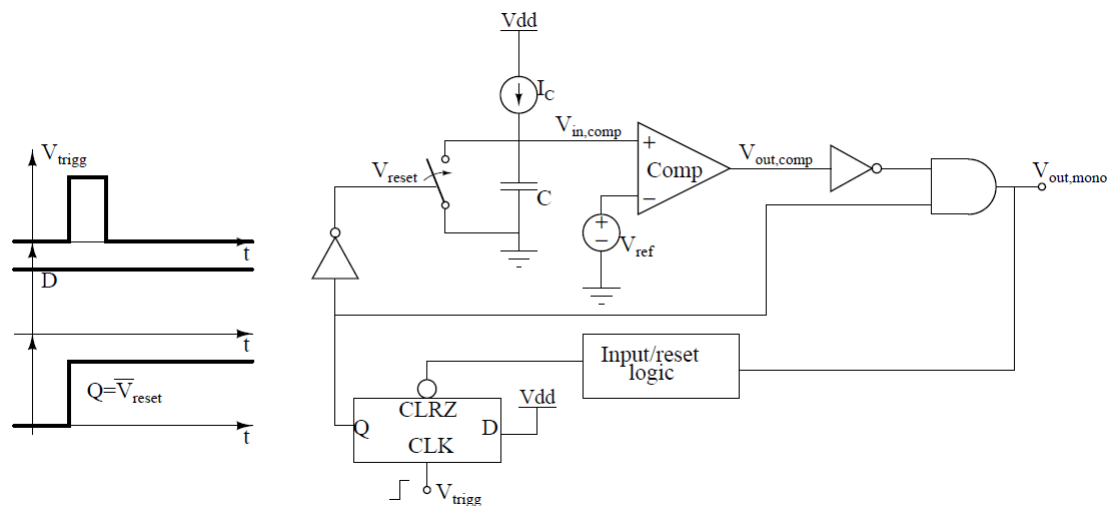
FIGURE 5.9: D flip-flop introduction in the digital reset in order to set the beginning of the capacitor reset signal.

Hence D is set at V_{dd} and given at the output **Q** when the trigger signal has a rising edge; the capacitor is then reset when the **CLRZ** is active and equal to 0 (figure 5.9. This last signal has to be equal to 0 only for a small time because after the capacitor has been discharged, the flip-flop has to be ready for the next triggering signal. In

addition the possibility of resetting the capacitor from an external **CLRZ** signal has to be added. Therefore the flip-flop **CLRZ** is given by an **AND** port with the external **CLRZ** (usually at 1 except for the initialization) as an input, and another signal that can be at zero for a small time sufficient to put the flip-flop output to 0; it can be provided by a monostable (figure 5.10).
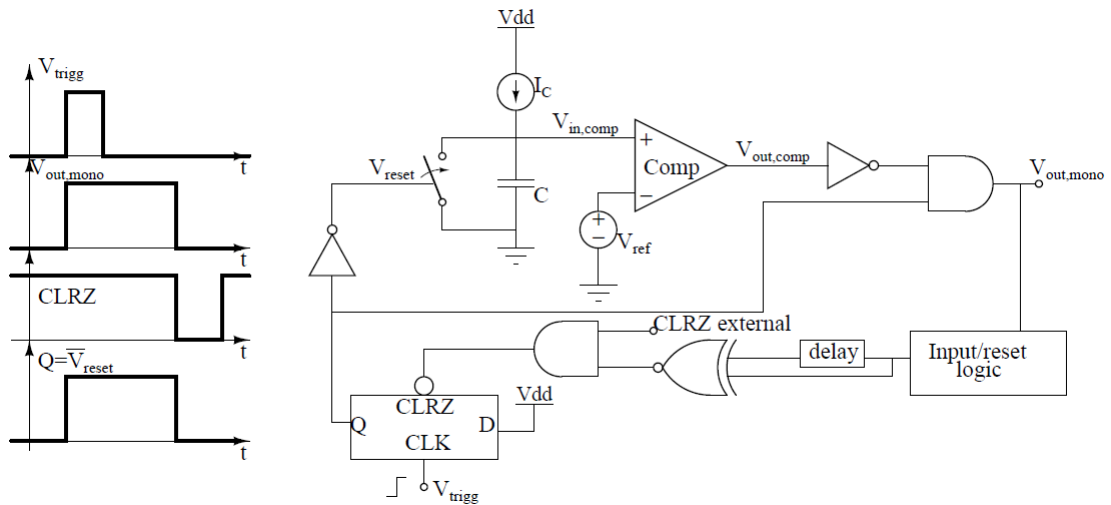
FIGURE 5.10: Introduction of the monostable to determine the end of the reset signal.

Thus it is employed a **XNOR** with two inputs that have a different logic value for a sufficient time that has to last less than the smallest period, hence $24ns$. This two inputs are generated applying the same signal, slightly delayed in one input and with no delay in the other. The delay is set to $5ns$. It has been realized by a two buffers and in between a resistor and a capacitor capable of providing the desired time constant. The resistor's value has been chosen in order to obtain the lowest current consumption. This results to be equal to $I_{cons,delay} \simeq 600nA$. This signal has to be provided only at the end of every period therefore it is generated from V_{mono} using a counter, a T flip-flop. The CLRZ pulse has to be provided only at the falling edge of the monostable output pulse. A counter, a T flip-flop positive edge-triggered, is used in order to trigger the CLRZ pulse only when it is needed, hence when the output pulse finishes. A T flip-flop is a toggle memory. It provides at the output **Q** the negated value of **T** for every positive edge that the **CLK** input sees. Hence this input is provided by $\overline{V_{out,mono}}$.
In figure 5.11 the digital reset circuit is reported.

5.3 Final circuit

After the designing the digital reset of the monostable, the whole circuit can be assembled, resulting in the one in figure 5.14. The monostable is then tested. The input

FIGURE 5.11: Digital reset circuit.

signals are:

- Buck's input voltage $1.7V \leq V_{in,Buck} \leq 3.6V$

- Buck's output voltage $V_{out,Buck} = 1.2V$

- triggering digital signal V_{trigg} for the beginning of the pulse

- external **CLRZ** for the initialization of the digital circuitry. It is initially set to 0.

The circuit is tested and the results of V_{mono} fulfils the requirements. In figures 5.12 and 5.13 the variable time pulses are shown and as it is possible to notice the monostable pulses varying proportionally to the difference between $V_{in,Buck}$ and $V_{out,Buck}$. The longer pulse results equal to $109ns$ since the comparator delay is in percentage lower than the one obtained with the $24ns$ ramp signal. Anyway a Buck T_{on} $2ns$ smaller does not represent a problem for the dc-dc converter and can be accepted.

The capacitor that is charged has been reduced in order to account the comparator's propagation delay and obtain the sought correct pulse width. The average current consumption per period is then the sum of the current generator current consumption, the current that charges the capacitor and the comparator's consumption. This results in an overall consumption of

$$\overline{I_{cons}} = I_{ref} + I_{currgen} + I_C + I_{comp} + I_{delaycell} \simeq 100nA + 550nA + 1.375\mu A + 3.36\mu A + 600nA$$

$$\simeq 5.98\mu A \quad \text{for the } 24ns \text{ pulse, Buck period of } 100ns \text{ (section 2.3)}$$

$$\overline{I_{cons}} = I_{ref} + I_{currgen} + I_C + I_{comp} + I_{delaycell} \simeq 100nA + 154nA + 286nA + 4.11\mu A + 250nA$$

$$\simeq 4.9\mu A \quad \text{for the } 111ns \text{ pulse, Buck period of } 250ns \text{ (section 2.3)}$$

$$(5.8)$$

The simulations, figures 5.12(a) and 5.12(b), show a consumption of $\overline{I_{cons}} = 6.34\mu A$ for $T_{on} = 24ns$ and $\overline{I_{cons}} = 5\mu A$ for $T_{on} = 111ns$. These values represent the lowest possible monostable current consumption that has been achieved. In the next paragraph the incredible improvements lead by this design in respect of the previous design are showed.

(a) *24ns output pulse with current consumption (blue).*

(b) *111ns output pulse with current consumption (blue).*
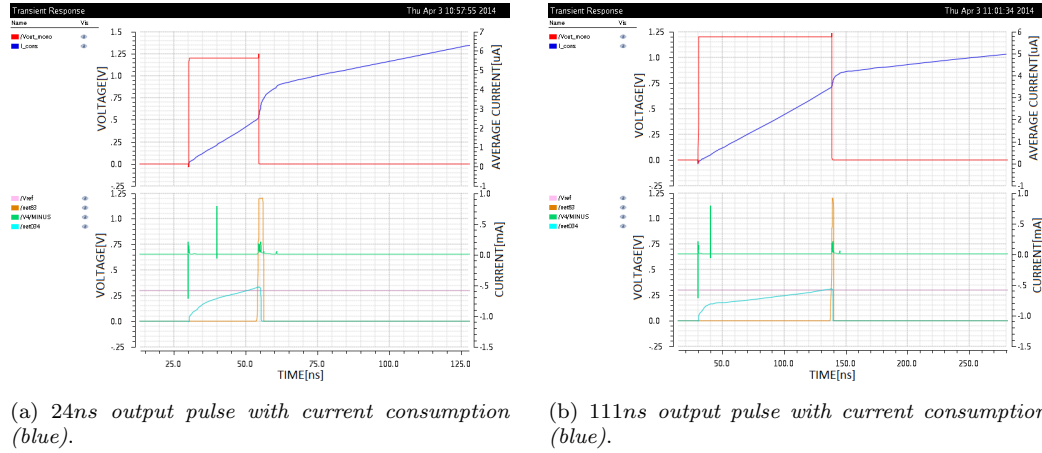
FIGURE 5.12: Output monostable pulses.

The last requirement that has to be fulfilled is the one regarding the circuit's statistical behaviour and it is tested by a Monte Carlo analysis. Since the standard variation of the current generator output current is approximately the 6.5% of its mean value, the same value is expected for the time width pulse. In tables 5.1 and 5.2 the results are summarized and it can be noticed that the expectations have been respected.

Temperature	$\mu_{\mathbf{T_{on}}}$	$\sigma_{\mathbf{T_{on}}}$	$\sigma_{\mathbf{T_{on}}}$ **in % of $\mathbf{T_{on}}$**
-40^oC	$25.86ns$	$1.88 \cdot 10^{-9}$	7.27%
27^oC	$24.18ns$	$1.597 \cdot 10^{-9}$	6.6%
95^oC	$22.64ns$	$1.357 \cdot 10^{-9}$	6%

TABLE 5.1: Monte-Carlo temperature analysis for the 24ns period.

A trimming technique will be necessary in order to fulfil the requirements. Using a ideal resistor for the generation of the current for the capacitor charge, it is possible
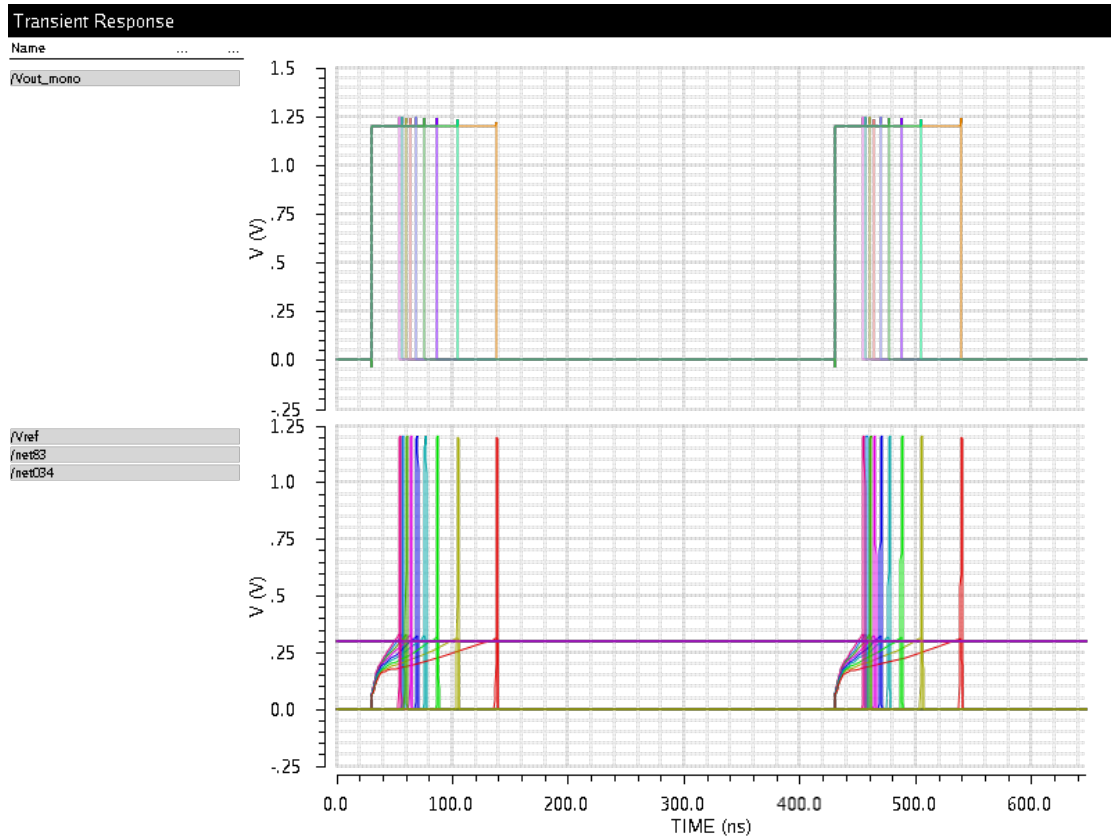
FIGURE 5.13: Monostable output pulses in response to $V_{in,Buck}$ that varies from $1.7V$ to $3.6V$.

Temperature	$\mu_{\mathbf{T_{on}}}$	$\sigma_{\mathbf{T_{on}}}$	$\sigma_{\mathbf{T_{on}}}$ in % of $\mathbf{T_{on}}$
-40^oC	$116.7ns$	$10.5 \cdot 10^{-9}$	9%
27^oC	$108.6ns$	$9 \cdot 10^{-9}$	8.3%
95^oC	$102ns$	$7.73 \cdot 10^{-9}$	7.5%

TABLE 5.2: Monte-Carlo temperature analysis for the 111ns period.

to fulfil even the statistical requirements. A Monte Carlo simulation shows in fact that $\sigma_{T_{on}} \approx 2.5\% \ of \ T_{on}$.

5.4 Monostables consumption related to the Buck load current

In chapter 2 the Buck regulator was described, together with its controller. After the realization of the monostable a significant analysis is represented by the evaluation of the two monostables current consumption impact on the Buck load current, in order to understand even its impact on the Buck efficiency.

The maximum current consumption of the monostables is achieved when $V_{in,Buck} = 3.6V$. The energy transferred from the input to the output is always the same, since I_{LPK}, T_{on} and T_{off} are fixed (chapter 2). The charge is then equal to

$$Q = \frac{I_{LPK}(T_{on} + T_{off})}{2} \simeq \frac{7.5mA \cdot (24ns + 46ns)}{2} = 262.5pC \qquad (5.9)$$

The load current is thus maintained at a defined value varying the frequency of the charge quantity transferred to the load. Therefore let us assume that a defined current $\overline{I_{out}}$ is required by the load for a period of $T = 10\mu s$. Then the number of single amount of charge $Q = 262.5pC$ delivered to the load in T are

$$\overline{I_{out}} = \frac{Q \cdot N}{T} \Rightarrow N = \frac{T \cdot \overline{I_{out}}}{Q} \qquad (5.10)$$

The current consumed by the monostables for every $100ns$ period, during which the charge Q is transferred to the load, is given by:

- $\overline{I_{cons,T_{on}}} \simeq 6\mu A$, T_{on} monostable average consumption in $100ns$ period

- $\overline{I_{cons,T_{off}}} \simeq 6\mu A$, T_{off} monostable average consumption in $100ns$ period

- $I_{cons,idle} \simeq 2.5\mu A + 2.5\mu A = 5\mu A$, current consumed by the constant references and the current I_C during the time in which on and off time pulses do not need to be set

The number of "charge pulses" needed in $10\mu s$ in order to obtain a load of $\overline{I_{out}} = 2.65mA$ are $N = 101$. Therefore the percentage of load current consumed by the two monostables is given by

$$\frac{I_{cons,monostables}}{\overline{I_{out}}} = \frac{12\mu A \cdot 100}{2.65mA} = 0.452\% \qquad (5.11)$$

Using the old monostables this would be $\frac{50\mu A \cdot 100}{2.65mA} = 1.9\%$, 4.2 times bigger.
Considering a $\overline{I_{load}} = 1mA$, we obtain $N = 38$, that means that the consumption is $12\mu A$ for $3.8\mu s$ and $5\mu A$ for $6.2\mu s$. Thus $I_{cons,monostables} = 0.766\%$ of $\overline{I_{out}}$, where with the previous version it was $\frac{I_{cons,monostables}}{\overline{I_{out}}} \simeq 5\%$.
Finally, considering a $\overline{I_{out}} = 26.25\mu A$, it is obtained $N = 1$ and $I_{cons,monostables} = 19.3\%$ of $\overline{I_{out}}$, while it was 190% for the previous design.
For lighter load than $26.25\mu A$ it will be necessary to turn off all the references in order to reduce the consumption of the monostables, with the consequence of slower monostables'

start-up.

The monostable's start-up time results to be approximately $70\mu s$. This time could be too high for some applications and it could lead to an excessive discharge of the output capacitance. Therefore a faster turn on time is needed and a way for reducing it has been investigated. A close investigation highlighted that the main problem was represented by the slow turn on of the current mirror used for the bias of the current generator (the biasing current is really low, $10nA$). In order to reduce the turn on, a sample and hold circuit has been used to provide a fast bias to the gate of the current mirror transistor, as it is commonly done in TI circuits. This device employs a capacitor with a voltage that is refreshed every a $T \approx 1ms$, so as not to add a significant current consumption. Moreover the current used to bias the current generator has been increased up to $30nA$ (from $10nA$) in order to reduce the turn on time, determining an increase of the overall consumption of $100nA$. Using these solutions, the turn on time has been reduced up to $19\mu s$; it could be reduced further increasing the current generator I_{ref}, but this determines an increasing in the current consumption of the entire monostable.
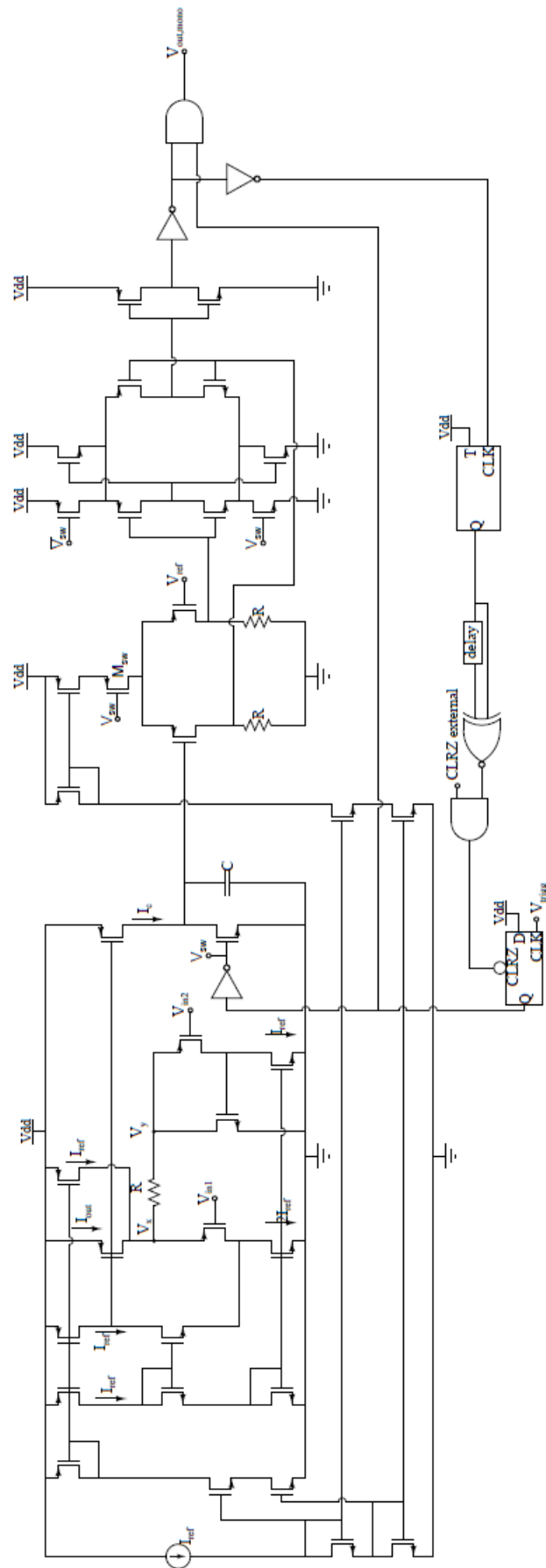
FIGURE 5.14: Monostable complete circuit schematic.

Chapter 6

Summary

A monostable for the controller of a Buck converter has been realized. This circuit can vary its pulse width proportionally to the difference between the input and output voltage of the regulator. In fact the controller is designed to set a constant peak inductor current and for this reason the Buck's on period must be able of vary in response to a variation of the input voltage.

The pulse of this device starts from an external triggering input. This causes the charging of a capacitor by a constant current proportional to the difference between the input and output voltage. A ramp voltage signal is obtained and when it crosses a fixed voltage reference, a comparator sets the end of the pulse. A digital reset is needed in order to discharge the capacitor for the next period.

The optimization started from the comparator. The requirements were fixed and many topologies have been analysed. A tradeoff between speed, consumption and statistical accuracy has been found and overcome. The adaptive bias of a CSDA (that is itself a comparator) has been exploited in order to obtain a low current consumption. The final solution employed a first pre-amplifier with a CSDA second stage in order to achieve a current consumption of $3.2\mu A$ with a delay of $3.3ns$.

Afterwards the circuit responsible for providing the proportional current has been optimized. Two circuits have been analysed: one employed two linear regulators for the extraction of two proportional currents then subtracted by a mirror, while another used two super source followers to fix the differential voltage on a resistor and generate directly the differential current. The second circuit has been chosen due to its lower current

consumption, $550nA$.

Finally the capacitor responsible for the timing of the entire circuit has been minimized in order to use the lowest current to charge it, that was $1.375\mu A$. A digital reset has been added for the discharge of the capacitor.

The circuit shows an average consumption in a Buck period of $5\mu A$, while the previous version consumed $25\mu A$. Monte Carlo analysis has shown a standard deviation equal to the 6% of the pulse width, but a careful review revealed that the responsible for this result was the resistor employed for the extrapolation of the proportional current. Therefore a trimming technique is suggested for the optimization of this result. Simulations using a trimmed resistor yield to an improved standard deviation of 2.5% of the pulse width.

Table of results

Comparators

	Previous design	Current mirror load	Cross coupled load	Self-biased	Final design
I_{cons}	$20\mu A$	$11\mu A$	$13\mu A$	$5\mu A$	$5\mu A$
t_p (24ns ramp)	$2.5ns$	$3.36ns$	$2.79ns$	$11.87ns$	$3.38ns$
σ_{t_p} (% of T_{on})	1%	2.7%	2.96%		1.3%
t_p (111ns ramp)	$11.5ns$	$10.69ns$	$6.58ns$	$12.3ns$	$5.05ns$
σ_{t_p} (% of T_{on})	1%	3%	3.45%		0.97%

Current generator

	Previous design	SSF current generator
I_{cons}	$2.85\mu A$	$550nA$
I_{out}	$500nA$	$500nA$
$\sigma_{I_{out}}$ (% of I_{out})	6%	6.56%

Monostable

	Previous design	New proposed design
I_{cons} (24ns pulse)	$25.6\mu A$	$6.34\mu A$
I_{cons} (111ns pulse)	$22.432\mu A$	$5\mu A$
$\sigma_{T_{on}}$ (24ns pulse)	6%	6.6%
$\sigma_{T_{on}}$ (111ns pulse)	8%	8.3%

TABLE 6.1: Summary table of the circuits designed.

Appendix A

Variability and mismatch

When an integrated circuit is manufactured, the random variations that affects important parameters like electrical properties and effective sizes, highly affect the accuracy of the designed device. These random mismatches play an important role in the design of analog integrated circuits. Therefore the derivation of accurate models, in order to understand the phenomena, helps the designer to minimize the effect of these variations on the accuracy of the circuits.

These effects can be divided into three categories: systematic variations, process variations and random variations[6].

Systematic variations

Systematic variations account for every systematic error during the manufacturing process. Integrated circuits are produced using lithographic techniques and many effects can determine the effective sizes of the devices to differ from the ones of the layout masks. Systematic variations are for example the ones that arise from the lateral diffusion under SiO_2 mask, from overetching and channel width narrowing (figure A.1). These effects are observed repeatedly when a circuit is mass-produced. Systematic variations can be avoided using appropriate layout techniques even if they determine some penalties in term of layout size and performances[6].

Process variations

Process variations affect the performances of different devices. These effects also arise during the manufacturing process; an example is the temperature at which integrated circuits are fabricated. Small temperature variations affect transistors parameters. In
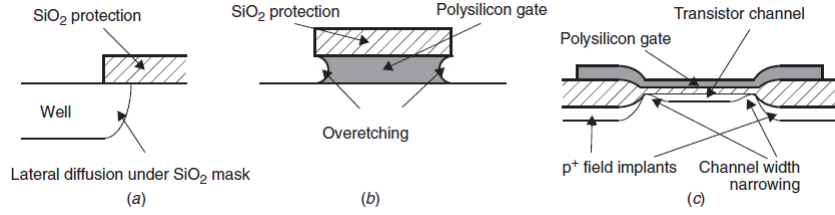
FIGURE A.1: Examples of two-dimensional effects that determine systematic variations[6].

spite of the efforts for reducing these changes, they persist and are important since they determine alterations in the oxide thickness, dopant concentration and other parameters. Since these problems cannot be avoided, every integrated circuit factory derives some models for accounting these variations and test the circuit functionalities through simulations.

Random mismatches

Even in the absence of process and systematic variations, it is impossible to ensure that two identical designed transistors will have the same number and locations of dopants since these parameters varies randomly. Therefore transistor parameters like voltage threshold, vary randomly from device to device.

In [16] a theoretical analysis of the statistical variations shows that the statistical distribution of random mismatches is a Gaussian distribution with a variance of

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2 \tag{A.1}$$

where ΔP accounts for the difference of a generic parameter P of two devices, while D is the distance between the two transistors, W and L the gate width and length, A_P and S_P are constants experimentally obtained. Since usually $D < 1mm$ the second term of equation A.1 can be neglected.

A precise and complete characterization and modeling of mismatch for MOS transistors is reported in [17]. They are usually operated in strong inversion, thus

$$I_d = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{Th})^2 = \beta (V_{gs} - V_{Th})^2 \tag{A.2}$$

The mismatches can be measured in variation of threshold voltage V_{Th} and conductance constant β.

The threshold voltage is given by $V_{Th} = \phi_{ms} + 2\phi_B + \frac{Q_B - Q_f + qD_I}{C_{ox}}$; the authors analyse analytically and experimentally its mismatch variations and derive a model for the standard deviation that is

$$\sigma_{\frac{\Delta V_{Th}}{V_{Th}}} = \frac{A_{V_{Th}}}{\sqrt{WL}} \tag{A.3}$$

where $A_{V_{Th}}$ is a proportional constant obtain from experimental results and W and L are the effective gate width and length. In figure A.2 is reported $\sigma_{\frac{\Delta V_{Th}}{V_{Th}}}$ over $1/\sqrt{WL}$ for pMOS and NMOS, and it shows the optimal accordance between the theoretical model and the experimental results. The most important outcome of this model is that an increasing in the transistors gate size, decreases the standard deviation of V_{Th} random mismatches.
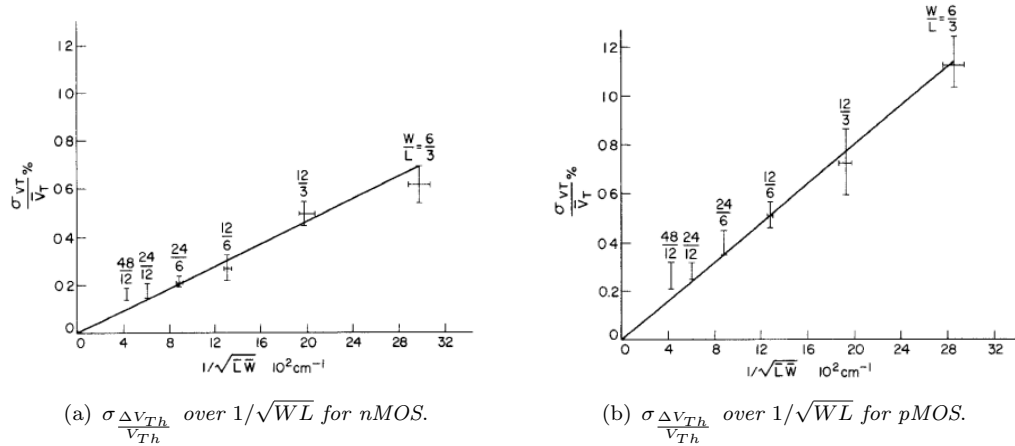

(a) $\sigma_{\frac{\Delta V_{Th}}{V_{Th}}}$ *over* $1/\sqrt{WL}$ *for nMOS.*   (b) $\sigma_{\frac{\Delta V_{Th}}{V_{Th}}}$ *over* $1/\sqrt{WL}$ *for pMOS.*

FIGURE A.2: Threshold voltage mismatch over transistor dimensions[17].

A similar model is derived for the conductance constant β, obtaining

$$\sigma_{\frac{\Delta \beta}{\beta}} = \frac{A_\beta}{\sqrt{WL}} \tag{A.4}$$

The last important result highlighted in [17] is the correlation between mismatches in V_{Th} and β. In fact both theoretical and experimental results show that its value is close to zero. Therefore it is commonly accepted that these two mismatch contributions are independent.

The two most common examples for the evaluation of mismatches in simple circuits are the current mismatch resulting from a current mirror (where the two MOS have same V_{gs}) and from a differential input pair. They results in a standard deviation regarding respectively the drain current and the offset input voltage, that are

$$\sigma_{\frac{\Delta I_d}{I_d}} = \frac{1}{\sqrt{WL}}\sqrt{A_\beta^2 + \left(\frac{g_m}{I_d}\right)^2 A_{V_{Th}}^2}$$

$$\sigma_{V_{os}} = \frac{1}{\sqrt{WL}}\sqrt{A_{V_{Th}}^2 + \left(\frac{I_d}{g_m}\right)^2 A_\beta^2}$$

(A.5)

These two equalities show again the connection between transistor size and random mismatches variations. Therefore an analog designer have to increase the area of the transistors in order to increase the circuit's accuracy. Unfortunately the gate area increase yields to the rise of parasitic elements that can directly affect the correct functionality of the integrated circuit designed. Thus an analog designer is always put in front of a tradeoff between speed and accuracy.

A.1 Accuracy analysis simulation method

When an integrated circuit is designed, it is important to evaluate its accuracy, therefore a method for its evaluation has to be used. This can be achieved by Monte Carlo analysis.

Halton defined in 1970 the Monte Carlo method as "representing the solution of a problem as a parameter of a hypothetical population, and using a random sequence of numbers to construct a sample of the population, from which statistical estimates of the parameter can be obtained". Therefore in every Monte Carlo run the transistor parameters are chosen randomly. In each simulation a defined element is evaluated and the results are used to derive its statistical distribution. In our case these are the mean value μ and the standard deviation σ, since the distribution is Gaussian. If the comparator is considered as an example, its delay time is evaluated for every Monte Carlo run and finally the statistical parameters are given as an output. Obviously the more are the runs, the more accurate is the evaluation of the statistical distribution. Unfortunately a great number of runs determines a long simulation time. A reasonable number of runs is 300, since it allows a sufficient accuracy in the distribution evaluation without causing a long time for its derivation. For this reason this is the number of runs adopted for the Monte Carlo simulations in this work.

When a Monte Carlo analysis is employed, it is provided the correlation table of the obtained statistical distribution. Therefore it is possible to obtain the correlation of every transistor parameter in the resulted standard deviation. In the simulations done the most recurring parameters are *vfb_mm* and *nch_mm*, mismatches that derive from the threshold voltage model. For this reason the increase of gate are WL determines

a decrease of *vfb_mm* and *nch_mm* influence and so a decrease of the overall standard deviation of the parameter evaluated.

The design procedure adopted for every circuit is reported in figure A.3. Monte Carlo analysis is applied at every topology, obtaining the mean value μ and the standard deviation σ. If these two parameters fulfil the requirements, then the circuit is the final one, otherwise the design has to be modified. This is done after evaluating the correlation table and increasing the gate area of the transistor with the strongest influence on σ. The Monte Carlo analysis and the design flow is applied again until the requirements are fulfilled.
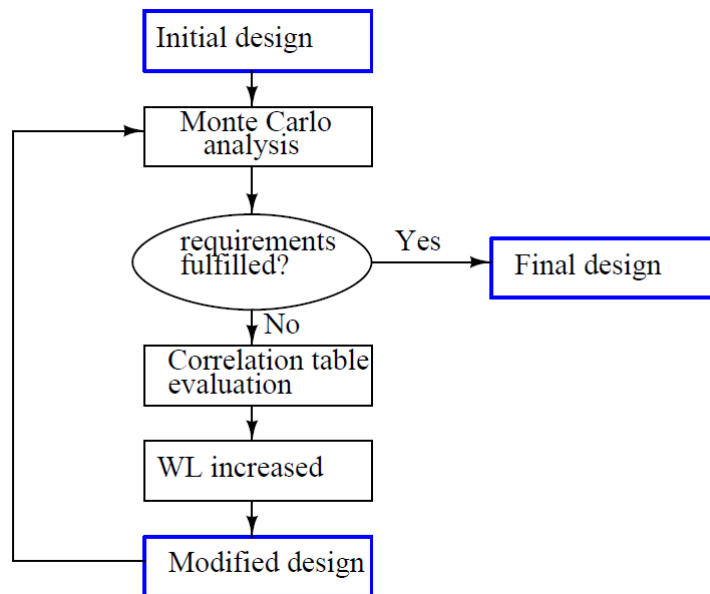

FIGURE A.3: Design procedure for the fulfilment of the statistical requirements.

Bibliography

[1] Biranchinath Sahu and Gabriel A. Rincón-Mora. An accurate, low-voltage, cmos switching power supply with adaptive on-time pulse-frequency modulation(pfm) control. *IEEE transactions on circuits and systems*, Frebruary 2007.

[2] R. Kuhn T. Tost B. Eversmann D. Schmitt-Landsiedel R. Bredelow F. Santoro, N. Gibson. A current-mode controller for hysteretic buck converters. *Workshop Analogschaltungen, TU Wien*, 24-25 Frebruary 2014.

[3] G. Caiulo G. Franchi A. Bigongiari, S. Brigati and F. Maloberti. An analog high-speed wide-range programmable monostable multivibrator. *IEEE international symposium on circuits and systems*, 1995.

[4] Philip E. Allen and Douglas R. Holberg. *CMOS analog circuit design*. Oxford University Press, 2010.

[5] S. Lewis P. Gray, P. Hurst and R. Meyer. *Analysis and design of analog integrated circuits*. John Wiley and Sons, 2010.

[6] D. Johns T. Carusone and K. Martin. *Analog integrated circuit design*. John Wiley and Sons, 1996.

[7] Anantha Chandrakasan Jan M. Rabaey. *Digital integrated circuits*. Prentice Hall, 2003.

[8] Mezyad M. Amourah and Randall L. Geiger. A high gain strategy with positive-feedback gain enhancement technique. *Circuits and systems*, 2001.

[9] Kosuke Isono et al. A 18.9-na standby current comparator with adaptive bias current generator. *Solid state circuit conference (A-SSCC)*, November 2011.

[10] Mel Bazes. Two novel fully complementary self-biased cmos differential amplifiers. *IEEE journal of solid-state circuits*, (no. 2), Febraury 1991.

[11] Vladimir Milovanovic and Horst Zimmermann. Analysis of single-stage complementary self-biased cmos differential amplifiers. *IEEE conference publications*, November 2012.

[12] Eric A. Vittoz. Weak inversion for ultra low-power and very low-voltage circuits. *IEEE Asian solid-state circuits conference*, November 16-18 2009.

[13] Christian C. Enz and Eric A. Vittoz. Cmos low-power analog circuit design. *Designing low power digital systems, emerging technologies (1996)*, 1996.

[14] Jaime Ramírez-Angulo et al. Ramón González Carvajal. The flipped voltage follower: a useful cell for low-voltage low-power circuit design. *IEEE transactions on circuits and systems*, July 2005.

[15] Jaime Ramírez-Angulo et al. Ramón González Carvajal. Comparison of conventional and new flipped voltage structures with increased input/output signal swing and current sourcing/sinking capabilities. *48th Midwest symposium on circuits and systems*, August 2005.

[16] A. Duinjamer M. Pelgrom and A. Welbers. Matching properties of mos transistors. *IEEE Journal of solid states circuits*, May 1989.

[17] Robert A. Hadaway Kadaba R. Lakshmikumar and Miles A. Copeland. Characterization and modeling of mismatch in mos transistors for precision analog design. *IEEE Journal of solid states circuits*, December 1986.