Design and Modelling of Tunnel Field Effect Transistor- using TCAD Modeling

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Abstract— The purpose of this research was to suggest a junction-less strategy for a vertical Tunnel Field Effect Transistor, which would increase the device's efficiency. In this study, we examine the similarities and differences between a negative capacitor TFET and a vertically generated TFET with a source pocket and a heterostructure-based nanowire gate. And how the channel transit impacts the output qualities of a sub-100 nanometer sized device. The Silvaco TCAD (a commercially available tool) was used to simulate a tri-layer high-K dielectric made of hafnium zirconium oxide (HZO) and titanium dioxide (TiO2) materials as gate stacking to the V-TFET and GAA-NC-TFET structures, and the tunnelling and transport parameters were calibrated experimentally. A short bandgap material, GaSb, in the home region to enhance carrier tunnelling via the mentioned three source (GaSb)-channel (Si) heterojunction at varying biases were utilized. Motion, tube length, and saturating velocity are only few of the transport channel characteristics that are investigated. As a result of the building's vertical orientation, the electric field is enhanced, allowing for an ION current of up to 104 Am2. The most unexpected result of this device is that a high ION/IOFF may increase mobility and reduce saturation velocity, perhaps reducing the drain voltage at saturation. The proposed biosensor's sensitivity was multiplied by 108 when vertical and lateral tunnelling were used in tandem. We apply a variety of optimisation strategies to deal with this problem, despite the fact that quantum confinement reduces the effect of mobility variations on device performance. When biomolecules were positively charged, the drain current increased, and when they were negatively charged, the drain current decreased.

Keywords- TFET, V-TFET, Junction less V-TFET, TCAD modelling, GaSb, H-TFET.

I. INTRODUCTION

Scaling CMOS has the potential to lower price, speed, and power consumption. When device dimensions are scaled in MOSFETs, very small channel effects, increased current leakage, hot carrier effects, reduced drain induced barriers, and reliability difficulties develop. Power dissipation in integrated circuits is reduced because the supply voltage scaling and inverse subthreshold slops (SS) of the MOSFET are capped at 60mV/decade. Since TFETs have such low standby power requirements, they are often employed in ultra-low power devices. Subthreshold slop in TFET of around 40mV/decade has recently been achieved.

Using Si-technologies, TFET-made devices may obtain an exceptionally low OFF current. Indirect and larger bandgaps are achieved via Si, making it more challenging to get adequate rich Oncurrents on Si devices. The effective tunnelling barrier length is reduced and increased On-current is confirmed in III-V (such as Ge, SiGe, InAs, and InGaAs) materials using transistors with a heterostructure for tunnelling. The practice of a negative capacitor with an all-around nanowire gate construction is presented to enhance the functionality of TFETs. TCAD simulation is used to propose and examine a nanowire-gate, negative-capacitance Tunnel FET based on a GaAs/InN heterostructure.

To accomplish the Negative capacitance effect, a Hf0.5, Zr0.5, O2 Ferroelectric material is used, and a tri-layer HfO2/TiO2/HfO2 higher K-dielectric is used as gate insulting oxide. Low current may make it difficult to see the TFET's tunnelling connection and channel transfer at work. They found a lot of interest due to smaller subthreshold swing and lower power dissipation compared to the conventional MOSFETs.

The primary flaw of the TFET is low ON-current than standard MOSFET. To improving the ION/IOFF ratio, various device architectures including vertical, L-shaped/U-shaped, and source pocket engineered have been investigated. The vertical Tunnel Field Effect Transistor is much easier to assemble than the conventional Tunnel Field Effect transistor from a manufacturing standpoint.

According to reports, the pocket source engineered TFET are more superior than standard TFET in terms of subthreshold properties. To decrease the tunnelling width and increase the drain current of a Si-channel based TFET, materials with low bandgap like germanium are acceptable close to source to design a hetero-junction at the expense of an increase in I_{OFF} (10⁻¹² A) that is significantly greater than the max value of I_{OFF} obtained in traditional Si-based TFET.

The proposed V-TFETs dc and analog/RF performances as well as the impact of temperature on their subthreshold characteristics have been examined. Analyzed, Finally, to show how the use of envisioned V-TFET. The proposed device was used to design an 11stage ring oscillator.

Although TFET subthreshold swing is significantly less than that of MOSFET. It displays low IOFF current, reduced current leakage and minimal power loss as a result of the high off-state tunnelling barrier.

An emerging technology for detecting biomolecules is a biosensor built on DM-FET technology. As a result, there are many benefits, such as downsizing and improved responsiveness with increased sensitivity. FETs have advantages, but they are less sensitive to biomolecules than other devices. Since it can no longer accurately identify the biomolecule, the device is less effective. TFETs are gaining popularity as a medical device in the modern era, especially among the ageing population. To keeping track of patient's health, accurate disease contamination prediction and early syndrome detection are crucial. To detect the presence of specific diseases, biomolecules like biotin-streptavidin (k2), charged amino acids like gluten (k11-20), keratin, and zein (k5-8) are required. On the other hand, the claimed sensitivity and Ion/Ioff ratio are both incredibly low.

DM-TFET structures rely on the formation of a nanocavity underneath the gate dielectric to perform their biosensing function. After having some of the gate dielectric-material removed, a nanocavity was formed. Target biomolecules trapped in the nanogap cavity may be identified by the TFET structure thanks to changes in the drain current caused by oscillations in the nanogap of the dielectric constant. Protein simulations often use a dielectric constant that is close to the value for the real biomolecule. Carrier dispersion from the basic source material to the channel area and back again makes it harder to achieve a sharp junction profile. The extensive doping in the TFET's Source and Drain regions makes device manufacturing more challenging.

The proposed Junction less VTFET structure can get over the constraint mentioned above. A uniformly doped silicon structure called a junction-less VTFET forms junctions using the charge-plasma principle. This research focuses mostly on I_{ON} current and sensing property improvement. For several biomolecules, simulation is carried out using various dielectric constants, k = 1, 5, 7, and 8. The impact of charged and neutral biomolecules on sensitivity is investigated.

The promising result of tunnel-FETs are lower sub-threshold slope and less Off-state current helped to replace MOSFET in IoT industry. Although TFETs undergo both Band-to-Band tunnel at the burrowing junction and Subsequent channel transfer throughout Channel, the former's contribution is sometimes lost due to the latter's lower On-current. The length of the channel in Heterojunction Tunneling Field Effect Transistors is also reduced to sub-100 nanometers. Currently, for practical and industrial design, H-TFETs need be studied in detail to determine how the channel transport effects their performance toward state-of-the-art. the fabrication process has advanced, encouraging results have been observed in III-V hetero-junction TFETs (H-TFETs), including SS of 48 mV/decade combined with 160 of 0.31 A/m and of 433 A/m higher on-current at 0.5 V of drain bias. Although channel transport affects have been discussed in earlier publications in-depth investigation and comprehension of its effects on the output characteristics of H-TFETs are still lacking.

Given that channel transit has the greater impact on output characteristics when TFET turn on, this topic requires deeper research.

II. DEVICE STRUCTURE

2.1. Tunnel devices

The proposed 2D&3D architecture and its equivalent capacity model in fig.1. In this structure, the radius of GaAs/InN nanowire is 10nm.The gate length (Lg), drain (Ld), source (Ls) as 90nm, 50nm, 50nm respectively.



Fig.1 Equivalent capacitance

2.1.1 Table

NAME OF THE PARAMETER	VALUE
Radius of the nanowire	10nm
Gate length	90nm
Drain length	50nm
Source length	50nm
Source doping concentration	1x10 ¹⁹ /cm ³
Drain doping concentration	1x10 ¹⁹ /cm ³
Channel doping concentration	1x10 ¹⁵ /cm ³
High-K gate oxide thickness	0.5nm+1nm+0.5nm
Dielectric constant of TiO2	80
Dielectric constant of HfO2	25
Contact of Source and Drain	5nm
Contact of Gate	1.5nm
Work function of the gate	4.06eV

Table 1: displays the additional, very particular and logical structural variables used in this architecture. To activate higher dielectric gate oxide on the InN channel, implemented a novel tricoating structure with TiO2 (ϵ TiO2 \approx 80) between two layers of

HfO2 (ϵ HfO2 \approx 25). The below table shows the used parameters in the proposed nanowire GAA NCTFET.

2.2 Tunnel devices

To make the discussion more straightforward, refer to the V-TFET without a source pocket as (WNP V-TFET) and with a source pocket as (WP V-TFET). Both devices as shown in Fig. 1 have their tunnelling characteristics more accurately predicted by using the nonlocal Band to Band tunnelling model, which incorporates local energy band variation. The heterojunction that is formed when GaSb and Si interact can have flaws due to lattice does not match and thermal co-efficient does not match.

A non-local trap-fixed heterojunction type has been added to our model statement considering this fact to improve the results.



Fig. 2. (a) GaSb/Si Vertical Tunnel Field Effect Transistor diagram without source pocket. (b) GaSb/Si Vertical Tunnel Field Effect Transistor diagram with source pocket. (c) VTFET cross-section without source pocket. (d) VTFET source pocket cross-section.

2.2.1 Table

Table 2: Different parameters of proposed heterojunction Vertical Tunnel FET.

NAME OF PARAMETERS	WNP (V-TFET)	WP (V-TFET)
Doping concentration of source	$2x10^{19}$ cm ⁻³	$2x10^{19}$ cm ⁻³
Doping concentration of pocket	-	$7 \times 10^{18} \text{ cm}^{-3}$
Doping concentration of channel	5x10 ¹⁶ cm ⁻³	$5 \times 10^{16} \text{ cm}^{-3}$
Doping concentration of drain	5x10 ¹⁸ cm ⁻³	5x10 ¹⁸ cm ⁻³
Thickness of channel	10nm	10nm
Thickness of gate oxide	2nm	2nm
Gate work function	4.2 eV	4.2ev
Al ₂ O ₃ gate dielectric permittivity	9.3	9.3
Gate length	20nm	25nm
Source length	20nm	20nm
Drain length	20nm	20nm
GaSb's Hole tunnel mass	0.4mo	0.4mo
GaSb's Electron tunnel mass	0.0410mo	0.0410mo
Silicon's Hole tunnel mass	0.24mo	0.24mo
Silicon's Electron tunnel mass	0.20mo	0.20mo
Length of pocket	-	5nm

2.3 Tunnel devices

SOURCE DRAIN CHANNEL 10n 5nr 35nm 35nm 40nm b

Drain currents at a constant VGS and VDS are suggested to be

Etching both sides of dielectric HfO2 creates nanogaps (Fig. 1b).

Junction less IDoff, k and IDoff, Air for nanogaps filled with

Nanogaps on both sides of HfO2 increase biomolecule marked area.

A 5 nm covering attaches biomolecules. Simulation biosensor is

VTFET.

biomolecules and empty, respectively.

Fig. 3 (a): Schematic of nano-gap integrated JL VTFET device (b): Cross sectional device structure of Junction less Vertical-TFET

2.3.1 Tables

Table 3.1 – calculated value for the suggested structure when k is less than 8.

Reported works	SS (mV/dec)	Ion /Ioff ratio	Sensitivity
DG-TFET	50	5.8×10^2	1.05×10^2
Conventional TFET	50.6	-	50
Lateral DMFET	74	101	10
Vertical DMFET	64	10 ²	40
Proposed structure	45.8	1.38×10^{10}	6.756x10 ⁴

Table 3.2 - Biosensor comparison with suggested structure.

Interface Charge	I _{eff} (A/µm)	Ion (A/µm)	V _{TH} (V)	Sub-threshold swing (mV/decade)	Sensitivity
0.00	7.88x10 ⁻¹⁵	1.09x10 ⁻⁵	3.40x10 ⁻¹	4.58x10 ¹	2.09×10^3
1.00x10 ¹¹	9.70x10 ⁻¹⁵	1.14x10 ⁻⁴	3.36x10 ⁻¹	4.59x10 ¹	1.70x10 ³
4.00x10 ¹¹	1.82x10 ⁻¹⁴	1.28x10 ⁻⁴	3.02x10 ⁻¹	4.61x10 ¹	9.07x10 ²
8.00x10 ¹¹	4.37x10 ⁻¹⁴	1.48x10 ⁻⁴	2.62x10 ⁻¹	4.64x10 ¹	3.78x10 ²
2.00x10 ¹²	6.42x10 ⁻¹³	2.08x10 ⁻⁴	1.53x10 ⁻¹	4.76x10 ¹	2.57x10 ¹
6.00x10 ¹²	2.29x10 ⁻⁹	4.00x10 ⁻⁴	1.32x10 ⁻¹	4.91x10 ¹	7.20x10 ⁻³
-6.00x10 ¹²	9.15x10 ⁻¹⁸	8.41x10 ⁻¹⁷	6.54x10 ⁻¹	4.81x10 ¹	1.80x10 ⁶
-2.00×10^{12}	2.44x10 ⁻¹⁶	2.90x10 ⁻⁵	5.58x10 ⁻¹	4.68x10 ¹	6.76x10 ⁴
-8.00x10 ¹¹	1.65x10 ⁻¹⁵	7.82x10 ⁻⁵	4.35x10 ⁻¹	4.71x10 ¹	1.00×10^4

2.4 Tunnel devices

Figure 1 depicts the construction of the n-double-gate type H-TFET that will be the subject of the investigation. GaAs(0.5), Sb(0.5), In(0.53), and Ga(0.47) were the inorganic components that were used for the source and channel, respectively. HfO2 is put to use as the gate dielectric in this device. We make use of the following characteristics wherever possible: body thickness ts equals 10 nm, oxide thickness tox equals 2 nm, channel length Lch equals 50 nm, source doping Ns equals 51019 cm3, and drain doping Nd equals 51018 cm3. The Sentaurus-TCAD simulator is used to do a numerical simulation of the H-TFET's functional capabilities. Inside the simulation domain of the Drift diffuse channel transport system,

dynamic non-local band-to-band tunnelling, bandgap shrinking, and fermi statistics are all at work at high field saturation.



2.4.1 Table

Table 4. Calibrated channeling parameters with experiment data

NAME OF PARAMETER	GaAsAb	InGaAs
Effective tunnelling barrier length	0.	42
Effective mass of electron	0.0447	0.041
Light hole effective mass	0.066	0.052
Tunnelling perfector	1.4×10^{20}	1.3x10 ²⁰
Tunnelling exponential factor	6.4x10 ⁶	5.7x10 ⁶



The negative capacitance property of HZO is shown in the preceding figures. First, we have a plot of polarisation vs electric field, and then we plot free energy versus polarisation. For both diagrams, the blue areas represent a negative capacitance scenario. Consider a FE layer of Hf1-xZrxO2 with x=0.5, using previously determined values for and. The following table details the HZO parameters used throughout the simulation.

Table 1. Shows the parameters of e	energy band with experiment dat
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NAME OF PARAMETERS	VALUE
Thickness of HZO layer	9nm
Dielectric constant	23
Remanent polarization	16.6 uC cm ⁻²
Spontaneous polarization	22.0 uC cm ⁻²
Coercive field	1.95 MV cm ⁻¹

The below figures show the Energy Band figure of N-channel gate all around nano-wire Tunnel Field Effect Transistor along Xposition; First, ON state band diagram. and OFF state band diagram.



The transfer features of the baseline NGAA TFET are revealed in the graphs that may be seen below. The second log10 (Ids) vs. Vg curve shows a low DIBL of 9.7 mV and is determined by varying the value of Vd. The first one depicts Ids in relation to Vg and reveals a significant saturation current of 17 A as well as a maximum ION/IOFF ratio of 1.132 109 when Vd is equal to 0.6V.



First, DC Analysis:

The simulation models were first calibrated in this environment. The Fig. 1 structures are required for using our suggested V-ATLAS TFET's TCAD tool. TCAD modelling results. It has been likened to a VTFET based on a Ge/Si heterojunction. The discrepancy between the experimental and theoretical outcomes is explained by the nonideal uniform properties of a real-world VTFET device with an oxide size of 2 nanometers (Fig.2). To think critically about gathered data. concordance, proving the viability of the chosen models.



Since β is typically employed in conjunction with 5.97×10^7 cm/s of sat as an empirical fitting factor, the odd and correct value of β = 1.395 is used. Fig. 2(a) displays the verified TCAD result in comparison to experimental data. Based on the calibrated TCAD,

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Fig. 2(b) illustrates the dependent of the Ids Vgs characteristic on the channel transport.

This proposed Junction less VTFET-based biosensor's simulation results for four different dielectric constants are researched in this area. Charged biomolecules' effects on current (Ion) are considered



In Figure 2, we observe the variation in drain current with gate voltage (VGS) for a JL VTFET for k = 1, 2, 5, and 8 and for k = 1 at VDS = 1 V and for wholly filled nanogaps. Additionally, we see this variation for nanogaps that are completely filled. Figure 2 displays, in a similar fashion, the I-V curve of neutral biomolecules for the values of k equal to 1, 2, 5, and 8.

3.6 The impact of Biomolecules with fully charged: -

Figures 3 and 4 demonstrate the outcome that fully charged biomolecules have on the gutter current when the gate voltage is held constant for JL VTFETs with k values of 1, 2, 5, and 8.



3.6.1 Negative-Charged Biomolecules Change Sensitivity: -

Fig. 3 – I-V properties of a negatively charged biomolecule shift.

3.6.2 Positive-Charge Biomolecules Change Sensitivity: -

The presence of biomolecules with a positive charge causes a change in drain current, as seen in Figure 4a, b, and c for k = 2, 5, and 8. The impact of biomolecules with a positive charge on the I-V



Fig. 4 - I-V properties of a positively charged biomolecule shift.

Because of the comparatively low current in the subthreshold region, it seems like channel transport scarcely influences the subthreshold slope SS of tunnel-FET. However, as Vgs and thus the current grow, the channel transport's influence gradually becomes more apparent, further demonstrating the need for this study.



Figure 5. (a) Shows Trap Assisted Tunnelling during sequential simulation with midgap trap density of 5×1011 eV-1cm-2. To demonstrate TCAD vs. Experimental data. Tables 1 and 2 provide band-to-band and channel transfer characteristics. Channel transit affects the Ids – Vgs distinguishing graph.



Figure 6. Ids - Vds characteristics under different mobilities and gate biases.

The Ids and Vds curves for their 3 sets of movement values reported in table2 are depicted in Figure 3. It is obvious from Fig. 3 that as µsc grows from 160 cm2/Vs to 1600 cm2/Vs, the drain current increases





 $V_{gs} = 0.5 V.$

Fig. 4 illustrates the current in the linear/saturation (Ids, lin/Ids, sat) area under diverse mobilities at Vgs=0.5V. This indicates how various operation shows rely on carrier transport.



Band-diagram illustrating linear and saturation regions for a variety of motions is shown in Figure 8. The profile of the electron's quasi-Fermi potential is shown by the dashed line. Band-diagram near the tunnelling joint, magnified and shown as an inset. Vgs = 0.5V.

At Lch 50nm, Ids, lin and Ids, sat are improved by 23.5 and 9.43 percent, respectively, when μ sc rises from 160 to 1600 cm2/Vs. Figure 5 displays the appropriate band-diagrams.

V. CONCLUSION

In this review paper, a general overview of tunnel field-effect transistors was provided. Firstly, the ferro-electric layer (HZO) in the gate stack is fused with transistor to produce a hybrid nanowire GaAs/InN baseline TFET structure. Second, how channel transport affects the output properties of sub-100 nm V-TFETs based on gaSb/si hetero-junction with and without source pockets. Hetero-junction-based Tunnel Field Effect Transistor studies using TCAD-simulation. Finally, their ac and dc characteristics, a biosensor built on a vertical TFET platform with 10 nanometer nanogaps on either side of the fixed dielectric material that is label-free (HfO2).

REFERENCES

- Q. Huang et al., "First foundry platform of complementary Tunnel-FETs in CMOS baseline technology for ultralowpower IoT applications: Manufacturability, variability and technology roadmap," in Int.Electron Devices Meeting (IEDM) Tech. Dig., Washington, DC, USA,2015, pp. 1–4.
- [2] Y.-H. Guan, Z.-C. Li, D.-X. Luo, Q.-Z. Meng, and Y.-F. Zhang, "Characteristics of cylindrical surrounding-gate GaAsxSb1-x/InyGa1-yAs heterojunction tunneling fieldeffect transistors," Chin. Phys. B, vol. 25, no. 10, Aug. 2016, Art. No. 108502.
- [3] H. W. Kim and D. Kwon, "Steep switching characteristics of L-shaped tunnel FET with doping engineering," IEEE J. Electron Devices Soc., vol. 9, pp. 359–364, 2021.
- [4] L. F. Pinotti, F. H. Cioldina, A. R. Vaza, L. C. J. Espíndolaa, and J. A. Diniza, "Vertical MOS and tunnel FETs in the same silicon pillar structure with Al and TiN gate electrodes," Microelectron. Eng., vol. 231, Jul. 2020, Art. no. 111399.

- [5] E. Memisevic et al., "Individual defects in InAs/InGaAsSb/GaSb nanowire tunnel field-effect transistors operating below 60 mV/decade," Nano Lett., vol. 17, no. 7, pp. 4373–4380, jun. 2017.
- [6] V. K. Chinni et al., "V-shaped InAs/Al0.5Ga0.5Sb vertical tunnel FET on GaAs (001) substrate with ION = 433μA/μm at VDS = 0.5V," IEEE J. Electron Devices Soc., vol. 5, pp. 53–58, 2017.
- [7] T. Rosca, A. Saeidi, E. Memisevic, L.-E. Wernersson, and A. M. Ionescu, "An experimental study of heterostructure tunnel FET nanowire arrays: Digital and analog figures of merit from 300K to 10K," in Int. Electron Devices Meeting (IEDM) Tech. Dig., San Francisco, CA, USA, 2018, pp. 1– 4.
- [8] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion implanted MOSFET's with very small physical dimensions," IEEE J. Solid-State Circuits, vol. SSC-9, no. 5, pp. 256–268, Oct. 1974.
- [9] G. A. Brown, P. M. Zeitzoff, G. Bersuker, and H. R. Huff, "Scaling CMOS: Materials & devices," Mater. Today, vol. 1, no. 7, pp. 20–25, 2004, doi: 10.1016/S1369-7021(04)00051-3.
- [10] G. E. Moore, Cramming More Components onto Integrated Circuits. New York, NY, USA: McGraw-Hill, 1965.
- [11] U. Dutta, M. K. Soni, and M. Pattanaik, "Design & optimization of gateall-around tunnel FET for low power applications," Int. J. Eng. Technol., vol. 7, no. 4, pp. 2263– 2270, 2018.
- [12] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthresholdswing tunnel transistors," IEEE Electron Device Lett., vol. 27, no. 4, pp. 297–300, Apr. 2006.
- [13] J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, 'Bandto-band tunneling in carbon nanotube field-effect transistors,' Phys. Rev. Lett., vol. 93, no. 19, Nov. 2004, Art. no. 196805.
- [14] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-nanowire n-type tunneling FETs with low subthreshold swing (50 mV/decade) at room temperature," IEEE Electron Device Lett., vol. 32, no. 4, pp. 437–439, Feb. 2011.
- [15] V. Saripalli, A. Mishra, S. Datta, and V. Narayanan, "An energy-efficient heterogeneous CMP based on hybrid TFET-CMOS cores," in Proc. 48th Design Automat. Conf. (DAC), 2011, pp. 729–734.
- [16] M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy efficient electronic switches," Nature, vol. 479, pp. 329–337, May 2011.
- [17] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-K gate dielectric," IEEE Trans. Electron Devices, vol. 54, pp. 1725–1733, Jul. 2007.
- [18] M. U. Sohag, M. S. Islam, K. Hosen, M. A. I. Fahim, M. M.H. Sarkar, and J. Park, "Dual source negative capacitance GaSb/InGaAsSb/InAs heterostructure based vertical TFET with steep subthreshold swing and high onoff current ratio," Results Phys., vol. 29, Oct. 2021, Art. no. 104796, doi: 10.1016/j.rinp. 2021.104796.

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- [19] Saeidi et al., "Near hysteresis-free negative capacitance InGaAs tunnel FETs with enhanced digital and analog figures of merit below VDD=400 mV," in IEDM Tech. Dig., Dec. 2018, pp. 13.4.1–13.4.4, doi: 10.1109/IEDM.2018.8614583.
- [20] Goel, S. Rewari, S. Verma, S.S. Deswal, R.S. Gupta, IEEE Sensor. J. 21 No 15, 16731 (2021).
- [21] N. Paras, S.S. Chauhan, International Conference on Advances in Computing and Communication Engineering (ICACCE-2019).
- [22] W.C. Ma, IEEE T. Electron Dev. 64 No 3, 1390 (2017).
- [23] A. Goel, S. Rewari, S. Verma, R.S. Gupta, IEEE Electron Devices Kolkata Conference (EDKCON-2018).
- [24] Y. Lu, G. Zhou, L. Rui, L. Qingmin, Q. Zhang, T. Vasen, S.D. Chae, IEEE Electron Dev. Lett. 33 No 5, 655 (2012).
- [25] M. Abdullah-Al-Kaiser, D.J. Paul, Q.D.M. Khosru, IEEE Region 10 Humanitarian Technology Conference (R10-HTC-2017).
- [26] L. Lin, C. Li, Z. Zhang, E. Alexov, J. Chem. Theory Comput. 9 No 4, 2126 (2013).

