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Analysis of Mechanical Strain in AlGaN/GaN HFETs

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Herein, the influence of mechanical strain induced by passivation layers on the electrical performance of AlGaN/GaN heterostructure field-effect transistor is investigated. We studied the physical mechanism of a threshold voltage (V_{th}) shift for the monolithically fabricated on/off devices reported earlier by our group. For that, theoretical calculations, simulation-based analysis, and nano-beam electron diffraction (NBED) measurements based on STEM are used. Strain distribution in the gate vicinity of transistors is compared for a SiN_x passivation layer with intrinsic stress from ≈0.5 to −1 GPa for normally on and normally off devices, respectively. The strain in epitaxial layers transferred by intrinsic stress of SiN_x is quantitatively evaluated using NEBD method. Strain dissimilarity $\Delta\varepsilon = 0.23\%$ is detected between normally on and normally off devices. Using this method, quantitative correlation between 1.13 V of V_{th} shift and microscopic strain difference in the epitaxial layers caused by 1.5 GPa intrinsic stress variation in passivation layer is provided. It is showed in this correlation that about half of the reported threshold voltage shift is induced by strain, i.e., by the piezoelectric effect. The rest of V_{th} shift is caused by the fabrication process. Therefore, various components/mechanisms contributing to the measured V_{th} shift are distinguished.

1. Introduction

Strain-engineered GaN heterostructure field-effect transistor (HFETs) have been studied for more than a decade.[1] However, only recently, it was practically shown that normally on/off GaN transistors can be realized through variation of intrinsic stress in the passivation layers.[2] The threshold voltage difference up to ≈1.4 V was reported for two types of transistors fabricated on the same wafer. This was explained by ≈1.5 GPa variation in the intrinsic stress of the first SiN_x passivation layer. Ambacher et al.[1] has theoretically described the piezoelectric properties of AlGaN/GaN heterostructures, where the transferred strain can enhance/reduce 2D electrons gas (2DEG) electron density. This means that the local strain in the vicinity of the gate trench of HFETs can produce positive/negative shift of the threshold voltage. In this work, we evaluated the actual strain/stress (ε/σ) in the fabricated transistors from Ref. [2] by means of theoretical calculation, simulation-based and nano-beam electron diffraction (NBED) analyses. The results for the normally on/off transistors were compared and a dependency of the threshold voltage on the mechanical strain/stress (V_{th} (ε/σ)) was analyzed. A simplified equation for V_{th} (σ), which defines the V_{th} shift for a given value of stress in AlGaN epitaxial layer, was derived. Stress/strain distribution in the vicinity of the gate contact (gate length ± 100 nm) was simulated. Finally, the strain distribution maps under the gate contacts in both fabricated normally on/off GaN HFETs were measured by NBED. Our results show to which extent V_{th} shift was created by the intrinsic stress difference in the first passivation layer. It was found that additional effects, for example, damage induced during the fabrication process, contribute to the reported V_{th} shift.

2. Monolithically Integrated Normally On/Off AlGaN/GaN HFETs

The transistors under study were fabricated on semi-insulating SiC substrate with MOVPE-grown epitaxial structure consisting of 2.2 µm $Al_{0.05}Ga_{0.95}N$ back barrier, 50 nm GaN channel, 10 nm $Al_{0.32}Ga_{0.68}N$ barrier, and 2 nm doped GaN cap. For the monolithically integrated normally on/off transistors fabrication, Osipov et al.[2] have used the following process steps. Initially, the active area of normally on devices was covered by 300 nm tensile plasma-enhanced chemical vapor deposition (PECVD) SiN_x with intrinsic stress of about 0.5 GPa. Later in the process, this nitride was structured on the wafer by optical lithography and etched from the selected positions by inductively coupled plasma (ICP) dry etching. This was followed by 300 s thermal treatment at 500 °C as the surface recovery step. These etched areas (normally off devices) were passivated with 300 nm compressive PECVD SiN_x (≈−1.0 GPa). Then, the standard FBH

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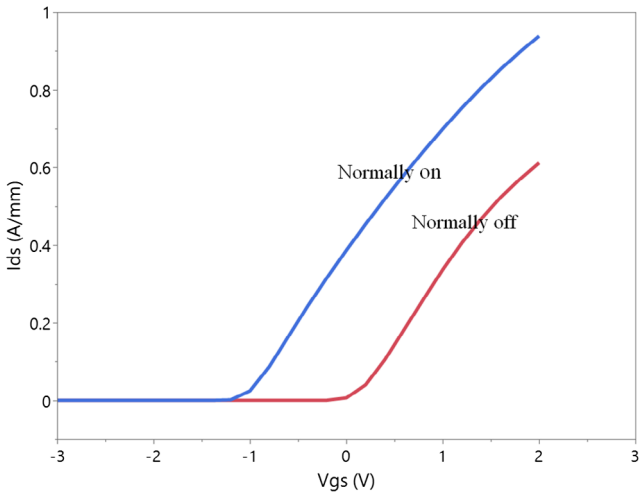

Figure 1. Transfer characteristics of the fabricated $2 \times 50\,\mu m$ transistors at $V_{DS} = 10$ V. The normally off devices were passivated with the compressive SiN_x passivation layer.

Table 1. DC characteristics of the fabricated transistors.

Parameters	Normally on	Normally off
V_{th} [V]	-1.01 ± 0.07	0.12 ± 0.05
I_{DS} (A mm^{-1}) at $V_{GS} = 1$ V	0.73	0.33
R_{on} [Ω mm]	2.1	4.2

fabrication technology[3] and device characterization was applied. The selected $2 \times 50\,\mu m$ transistors have 100 nm gate length, 0.5 μm gate–source distance, and 2.0 μm gate–drain distance.

The transfer characteristics of the fabricated transistors are shown in **Figure 1**. The measured threshold voltage shift is 1.13 V between two types of transistors with 300 nm SiN_x layer and 1.5 GPa stress variation. In **Table 1**, the mean values of measured DC characteristics are provided. The transistors are different in terms of maximum drain current (I_{DSmax}) and on resistance (R_{on}). The comparison indicates different electron density in the two types of transistors, which originates from the technological variations described earlier. The reduced electron density in normally off devices can be initiated from the area underneath the gate contact and/or the whole drain-to-source active area.

3. Theoretical Evaluation

To estimate the influence of mechanical strain on the threshold voltage, we used theoretical models from Ref. [1,4–7]. The total polarization-induced sheet charge density $\sigma(x)$ in a Ga-face AlGaN/GaN heterostructures can be calculated from Equation (1).

$$|\sigma_{(x)}| = P_{pz}(Al_xGa_{1-x}N) + P_{sp}(Al_xGa_{1-x}N) - P_{sp}(GaN) \quad (1)$$

where x is aluminum content in AlGaN barrier, P_{pz} is a piezoelectric polarization, and P_{sp} is a spontaneous polarization. It is assumed in Equation (1) that a GaN is fully relaxed. The value of P_{pz} ($Al_xGa_{1-x}N$) vector can be calculated according to Equation (2) for biaxial strain (ε_{xx}=ε_{yy}). In this Equation, e31 and e33 are piezoelectric coefficients and C_{11} to C_{33} are elastic constants. The biaxial strains ε_{xx} and ε_{yy} are induced by lattice mismatch between AlGaN barrier and GaN channel. In Equation (2), the ratio between polarization and strain is $-1.561\,Cm^{-2}$ for $Al_{0.32}Ga_{0.68}N$, which is calculated using the liner model from Ref. [1,4]. However, for a higher accuracy, nonlinear case according to Refs. [4-6] was considered. In the case of an external force, the induced strain/stress ($\varepsilon_{xx-external}/\sigma_{xx-external}$) in AlGaN barrier similarly leads to piezoelectric polarization. In our study, this strain is induced by the stressed passivation layer, and it is assumed to be biaxial.

$$P_{pz}(Al_xGa_{1-x}N) = 2 \times \varepsilon_{xx} \times \left(e_{31}(x) - \frac{e_{33}(x) \times C_{13}(x)}{C_{33}(x)}\right) \quad (2)$$

Figure 2 presents the dependency of in-plane strain induced by latticed mismatch between AlGaN barrier and relaxed GaN channel on Al mole fraction. To achieve a normally off devices, one needs to apply external stress, which at least compensates the tensile strain, that is, polarization charges, caused by the lattice mismatch. This strain value for $Al_{0.32}Ga_{0.68}N$/GaN is 8.99×10^{-3} or 0.89% (4.10 GPa based on tensor components in Ref. [1]).

The threshold voltage in an AlGaN/GaN high-electron-mobility transistor (HEMT) can be defined from Equation (3).[6] In this equation, $\varnothing_b(x)$ is Schottky barrier height. According to the electrical measurements, $\varnothing_b$ is about 1 eV for the both types of transistors. $\Delta E_C(x)$ is the conduction band discontinuity, N_D is the doping density, and d_d and d_i are the thicknesses of doped and intrinsic AlGaN barrier, respectively.

$$V_{th}(x) = \varnothing_b(x) - \Delta E_C(x) - \frac{qN_D{d_d}^2}{2\varepsilon(x)} - \frac{\sigma(x)}{\varepsilon(x)}(d_d + d_i) \quad (3)$$

$$V_{th}(\varepsilon_{xx-external}, x) = V_{th0} + \left(\frac{P_{pz}(Al_xGa_{1-x}N) \times (d_d + d_i)}{\varepsilon_0 \varepsilon_{Al_xGa_{1-x}N}}\right) \quad (4)$$

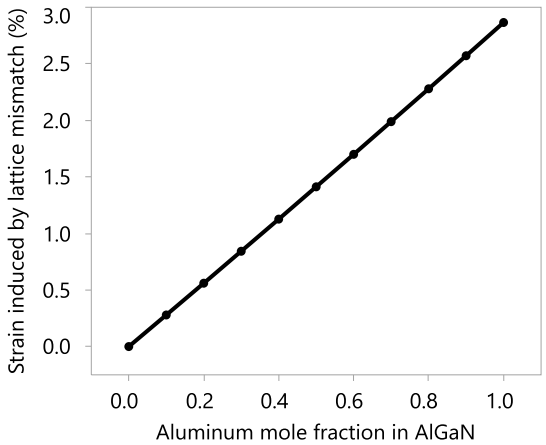

Figure 2. Strain (ε_{xx}) caused by latticed mismatch between AlGaN and GaN versus aluminum mole fraction in AlGaN barrier.

$$\Delta V_{th}(\sigma_{xx-external}(\mathrm{GPa}), 0.32) = -0.010 - 0.297\sigma_{xx} + 0.004(\sigma_{xx} - 1.5)^2 \quad (5)$$

Equation (4) is derived by inserting Equation (1) and (2) to Equation (3). There V_{th0} is the strain independent part of the threshold voltage, which is constant for a given Al content. In the case of our normally on/off transistors, the threshold voltage (V_{th}) is defined by Equation (4). The V_{th} shift (ΔV_{th}) between two types of devices can be calculated from Equation (5), when all parameters are the same except an external stress. This is valid for our experimental data since the transistors are fabricated on the same wafer. According to Equation (5), to achieve $\Delta V_{th} = 1.13$ V, at least ≈3.8 GPa stress (0.83% strain) difference is required in $Al_{0.32}Ga_{0.68}N$ barrier underneath the gate contact. It means that SiN_x should provide a minimum of 3.8 GPa stress, that is, 1.9 GPa from each side of the gate trench. However, the maximum theoretical intrinsic stress difference in the two types of transistors from Figure 1 is 3.00 GPa ($\Delta\varepsilon_{xx} = 0.66\%$ strain) for our case. Therefore, the calculations in this section show that the maximum stress/strain value in the fabricated transistors (3.00 GPa or 0.66%) was less than minimum required amount for normally off behavior (4.10 GPa or 0.89%). It was also lower than required amount for the measured threshold voltage shift of 1.13 V (3.8 GPa or 0.83%). This means the reported V_{th} shift was not induced only by the transferred stress from SiN_x passivation layers. To understand the nature of observed shift, we further analyzed the transistors.

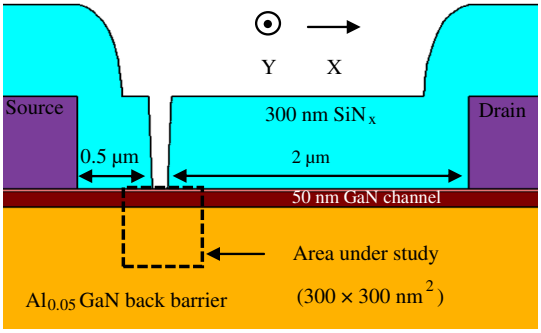

Figure 3. Cross section of the structures used for the simulation of transferred stress from SiN_x passivation to the selected area in epitaxial layers.

4. Strain Map Analysis and Discussion

In this section, the transistor's strain distribution maps obtained by simulation and NBED method are analyzed and compared. The results are discussed in Section 4.3.

4.1. Device Simulation

The mechanical properties of transistors under discussion (Figure 1) were simulated using Victory Stress in Silvaco CAD tools. From these simulations, we extracted the strain underneath the gate trench induced by 300 nm SiN_x passivation layer. We used a simplified structure of the transistors as shown in **Figure 3**, which corresponds to the transistors measured in Section 2. The simulation presents the transferred strain from the passivation layer (+0.5 GPa for normally on and −1.0 GPa for normally off transistors) to a selected area in the epitaxial layer shown in Figure 3. In this study, we assumed the intrinsic stress of the passivation layer to be biaxially transferred to the epitaxial layers and we neglected the influence of shear stresses and stress in Z direction. In our analysis, normal strain/stress XX ($\varepsilon_{xx}/\sigma_{xx}$) is considered. ε_{xx} represents strain, which is caused by a normal stress acting in X direction. The extracted strain/stress can be converted to the corresponding threshold voltage shift by Equation (5) when strain/stress is biaxial for wurtzite crystals ($\varepsilon_{xx} = \varepsilon_{yy}$). Nevertheless, one needs to consider, due to the geometry of the transistors, the stress from passivation layer to the epitaxial layers is neither fully biaxial nor uniaxial. However, our assumption helps to evaluate the minimum required $\varepsilon_{xx}/\sigma_{xx}$ that leads to the actual threshold voltage shift in the transistors.

In **Figure 4**, the strain distribution maps for normally on and off transistors, that is, for compressive and tensile passivation layers, are presented. The images are corresponding to a $300 \times 300\ \mathrm{nm}^2$ area in the vicinity of 100 nm gate trench. These maps show that the intrinsic stress of the passivation layer

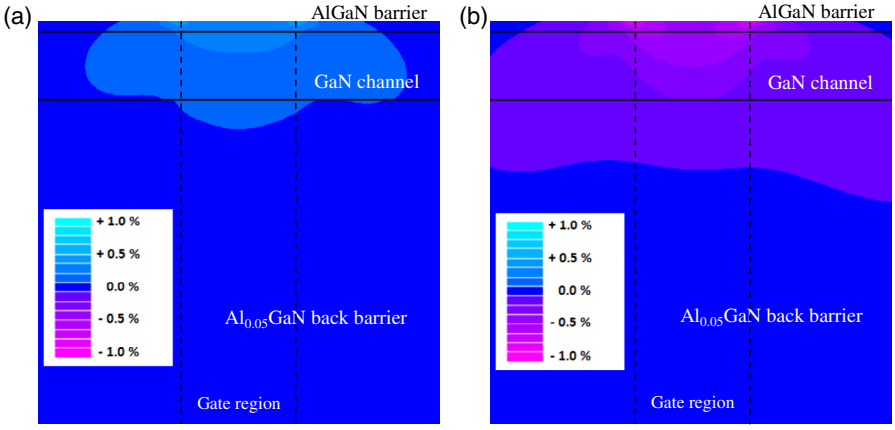

Figure 4. Simulated strain XX distribution maps for a) normally on and b) normally off transistors. The images are corresponding to $300 \times 300\ \mathrm{nm}^2$ area underneath the 100 nm gate trench marked in Figure 3 as the area under study.

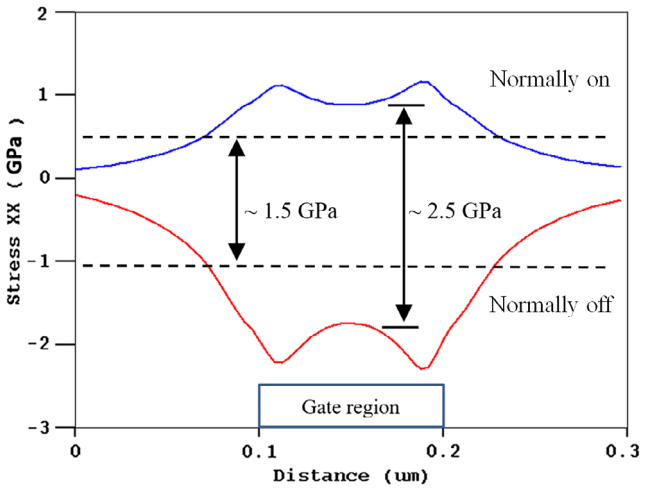

Figure 5. Simulated stress profile at AlGaN/GaN interface of normally on/off transistors.

was transferred to 10 nm AlGaN barrier and 50 nm GaN channel. The simulation shows that SiN_x stress is actually transferred into epitaxial layers and can influence electron density in the channel as explained in theory.[1]

The stress XX profile in **Figure 5** was extracted at AlGaN/GaN interface from the corresponding stress distribution maps. As can be seen in Figure 5, the maximum transferred stress is found at the gate trench edges. These maximum values are ≈2 GPa compressive and ≈1 GPa tensile for normally off and normally on transistors, respectively. These peaks are overlapping in the center of the gate trench. The overlapping of edge stress/strain reduces with the gate length increase and becomes negligible at a certain gate length. This emphasizes importance of the concept for radio frequency (RF) devices with gate length of 100 nm or shorter. As the stress is transferring to the epitaxial layers inhomogeneously, we consider two cases. First, we assume that the threshold voltage shift is caused by the average value of stress in the vicinity of the gate (gate length ± 100 nm). By this assumption, stress XX dissimilarity is about 1.5 GPa ($\Delta\varepsilon_{xx} = 0.33\%$) between normally off and normally on transistors. In the second assumption, the threshold voltage shift is considered to be caused by the average stress value only in the gate trench. In this case, the stress XX difference is between 2.5 and 3 GPa ($\Delta\varepsilon_{xx} = 0.55\%$ to 0.66%) comparing normally off and normally on transistors. Both assumptions result in stress/strain value difference below 3.8 GPa ($\Delta\varepsilon_{xx} = 0.83\%$), which was calculated in the theoretical section for the measured threshold voltage shift from Table 1. Even if we take the maximum difference of 3 GPa at the gate edge, the experimentally observed V_{th} shift cannot be fully explained.

4.2. NBED-Based Analyses

The NBED method was chosen for the stain measurements near the gate of the HEMT as suitable compromise between the field of view and the sensitivity for the expected strain.[8,9] For NBED measurements, electron-transparent classical H-bar samples were prepared by laser, plasma focused ion beam (FIB), and Ga FIB down to a thickness of 200 nm in the active area of HEMT (source, gate, drain). The NBED[10] experiments were performed at 300 KV in a probe-corrected TEM (FEI, Titan3 G2 60-300) in microprobe mode with 10 µm condenser aperture and 230 mm camera length. The strain values were extracted out of individual diffraction patterns in zone axis $B = [01\text{-}10]$ using a commercial software (FEI, Epsilon).[11] For the strain evaluation, the distances in the diffraction patterns were compared to a mean reference pattern calculated out of 400 diffraction patterns acquired 250 nm underneath the gate.

The strain XX distribution maps visualized by NBED for normally on and normally off transistors are presented in **Figure 6**. This figure shows different strain underneath the gate contacts for two types of transistors. The strain profile at AlGaN/GaN interface extracted from NBED images are shown in **Figure 7**. The average strain XX in gate vicinity (gate length ± 100 nm) is changed by 0.23% (1.05 GPa). This value is lower than the simulation-based estimation (≈0.33%) and it could be a result of stress relaxation during samples preparation. In NBED technique, the samples had to be prepared to the electron-transparent lamella (about 200 nm thickness measured by the electron backscatter yield). Some stress relaxation occurs at the sidewalls of the lamella due to missing forces normal to the cross sections. Additionally, the FIB preparation may have changed the strain due to Ga ion implantation or vacancy formation at the lamella sidewalls. Therefore, the actual stress value is expected to be higher than the observed 1.05 GPa. Nevertheless, this stress variation according to Equation (5) is corresponding to 0.3–0.4 V threshold voltage shift. Combining all previous calculations, this result shows that V_{th} shift at least partially was caused by transferring stress from passivation layer to the epitaxial layers, that is, direct piezoelectric effect.

4.3. Results Analysis and Discussion

As it was calculated, the theoretical V_{th} shift is underestimating the experimentally measured shift. The value of strain in simulation and extracted from NEBD analysis is lower than that what is required to explain the experimental results. This indicates that the intrinsic stress dissimilarity in the first passivation layer has only created a part of the threshold voltage shift in the fabricated GaN HFETs. To explain this discrepancy, we have considered the possible influence of the fabrication process on the device electrical performance. We propose that the back etching of tensile nitride, which was used for the fabrication of normally off devices, damages a GaN surface. This surface damage may contribute to the measured V_{th} shift for normally off transistors. Another process step, that potentially may damage surface, is nitrogen ion bombardment during deposition of compressive SiN_x in PECVD.[12]

The back etching of 300 nm tensile SiN_x was carried out by SF_6-CHF_3 ICP plasma at 300 W ICP and 20 W HF power for 210 s. This time includes an over etching. Therefore, the whole active area of normally off devices was subjected to a plasma-etching damage. To verify that, we have checked 2DEG sheet resistance (R_{sh}) on the wafer before and after fabrication. The initial sheet resistance was $586 \pm 27\ \Omega\,\square^{-1}$ measured by Eddy current

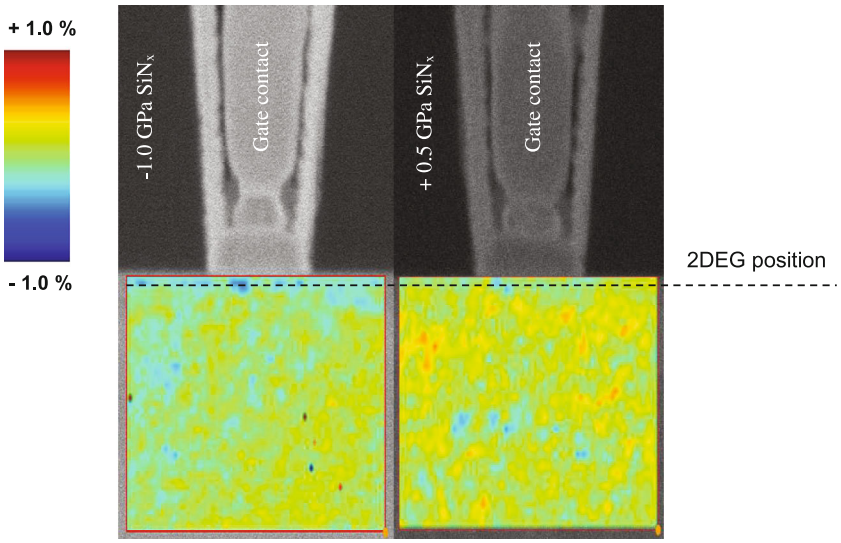

Figure 6. NBED strain distribution maps for normally off (left) and normally on (right) transistors. The images are corresponding to 300 × 300 nm^2 area underneath the gate contacts.

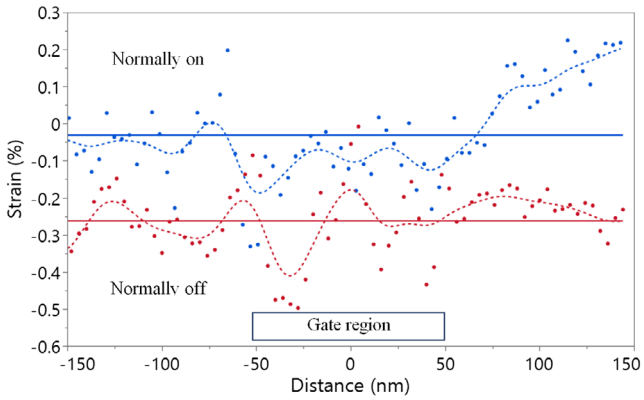

Figure 7. Strain values at AlGaN/GaN interface of the fabricated transistors. The solid lines are presenting mean value of all data points measured in this study. The dashed lines are the mean fitting given as a guide for the eye.

technique. The sheet resistance after fabrication was measured using fabricated van der Pauw structures. This measurement has shown mean R_{sh} value reduction to $458 \pm 21\,\Omega\square^{-1}$ in the active area covered with tensile passivation. In the areas with compressive passivation, the mean R_{sh} value increased to $980 \pm 123\,\Omega\square^{-1}$. The sheet resistance difference between these areas (2.13 times) indicates lower 2DEG electron density for the case of compressive nitride and this must have influenced the threshold voltage. The reduction of 2DEG density also explains the significantly higher on-resistance (R_{on}) in normally off transistors shown in Table 1. In an additional test replicating the discussed fabrication process steps, we used two bare samples of a similar epitaxial structure. This experiment proved that the etching recipe was highly destructive to the active area showing up to 5 times increase of the sheet resistance. An additional contribution to the discussed damage may come from the deposition of compressive nitride. In this type of passivation, a low-frequency excitation in PECVD system is required. Under this condition, nitrogen ion bombardment during SiN_x deposition is possible and this leads to a damage of semiconductor surface during initial phase of the passivation process.[12] In any case, the difference of 2.13 times in sheet resistance can lead to a 0.53 V shift in threshold voltage. This means from the total measured V_{th} shift of 1.13 V, maximum 0.60 V shift can be attributed to the piezoelectric effect. This value according to Equation (5) is equivalent to $\Delta\sigma_{xx} = 1.8$ GPa ($\Delta\varepsilon_{xx} = 0.39\%$), which is in the range given in our theoretical and simulation-based analyses.

5. Conclusion

In this work, using theoretical calculations, simulation, and NEBD measurements, we studied physical mechanisms of previously reported threshold voltage shift for monolithically integrated normally on/off AlGaN/GaN HFETs. Both theoretical considerations and experiment confirmed that the stress was transferred from a SiN_x passivation layer into the semiconductor epitaxial structure in the gate vicinity. In contrast, the induced strain is not sufficient to explain the value of reported V_{th} difference between normally on/off transistors. Both theoretically calculated strain and the strain extracted from simulation and NBED analysis were found to be responsible for $\leq$0.6 V from 1.13 V of total V_{th} shift between two types of transistors. The remaining part of the shift was attributed to the damage induced in the fabrication process. This was confirmed by a reduction of 2DEG density in the active area of normally off transistors. The measured 2.13 times difference in sheet resistance corresponds to maximum 0.53 V threshold voltage shift and explains the discrepancy obtained in this work.

The conventional trend in RF devices is a reduction of parasitic elements by transistor scaling and use of epitaxial layers with high electron concentration. This approach is limited by short channel effects. In our technology, compressive mechanical stress in the gate vicinity prevents short channel effects by providing a well-defined reduction of 2DEG electron concentration just underneath the gate. This technique is very efficient for shorter gates (100 nm or less). For longer gates (>250 nm), stressed nitride does not significantly shift the threshold voltage, but it can locally reduce the electron density, that is, enhance maximum electrical field at the edge of the gate contacts. Tuning of the mechanical stress at drain side of the gate is a way to improve breakdown voltage and also reliability of transistors.

The understanding of physical mechanisms, which is discussed in our work and which can influence device characteristics, paves the way for the future optimization and realization of AlGaN/GaN HFETs targeting specific applications.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D electrons gas (2DEG), GaN High-electron-mobility transistor, nano-beam electron diffraction (NBED), strain engineering, scanning transmission electron microscopy (STEM)

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[1] O. Ambacher, B. Foutz, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, A. Sierakowski, W. Schaff, L. Eastman, R. Dimitrov, A. Mitchell, M. Stutzmann, *J. Appl. Phys.* **2000**, *87*, 334.
[2] K. Osipov, I. Ostermay, M. Bodduluri, F. Brunner, G. Trankle, J. Würfl, *IEEE Trans. Electron Devices* **2018**, *65*, 3176.
[3] R. Lossy, H. Blanck, J. Würfl, in *2014 Int. Conf. on Compound Semiconductor Manufacturing Technology (CS Mantech)*, Denver Colorado, US **2014**, pp. 193–196.
[4] O. Ambacher, J. Majewski, C. Miskys, A. Link, M. Hermann, M. Eickhoff, M. Stutzmann, F. Bernardini, V. Fiorentini, V. Tilak, B. Schaff, L. Eastman, *J. Phys. Condens. Matter* **2002**, *14*, 3399.
[5] H. Morkoç, *Handbook of Nitride Semiconductors and Devices, Volume 3, GaN-Based Optical And Electronic Devices*, WILEY-VCH Verlag GmbH, Weinheim, **2009**.
[6] Rashmi, A. Kranti, S. Haldar, R. Gupta, *Solid-State Electron.* **2002**, *46*, 621.
[7] O. Ambacher, V. Cimalla, in *Polarization Induced Effects in GaN-Based Heterostructures and Novel Sensors* (Eds: C. Wood, D. Jena), Polarization Effects in Semiconductors, Springer, Boston, MA, **2008**.
[8] A. Béché, J. L. Rouvière, J. P. Barnes, D. Cooper, *Ultramicroscopy* **2013**, *131*, 10.
[9] V. B. Ozdol, C. Gammer, X. G. Jin, P. Ercius, C. Ophus, J. Ciston, A. M. Minor, *Appl. Phys. Lett.* **2015**, *106*, 253107.
[10] A. Béché, J. L. Rouvière, L. Clément, J. M. Hartmann, *Appl. Phys. Lett.* **2009**, *95*, 123114.
[11] M. Williamson, P. van Dooren, J. Flanagan, in *IEEE 22nd Int. Symp. on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, Hsinchu, Taiwan **2015**, pp. 197–200.
[12] H. Yazdani, S. Chevtchenko, I. Ostermay, J. Würfl, *Semicond. Sci. Technol.* **2021**, *36*, 055018.