University of Nottingham
UK | CHINA | MALAYSIA

THE UNIVERSITY OF NOTTINGHAM

Power Electronics, Machine and Control Group
Department of Electrical and Electronic Engineering
Faculty of Engineering

Design of High Reliability Power Converters for Aerospace Applications

Jayakrishnan Harikumaran

Submitted to the University of Nottingham
for the degree of Doctor of Philosophy

March, 2022

Abstract

Design of High Reliability Power Converters for Aerospace Applications

In this doctoral thesis, methods to design high reliability power converters for mission critical aerospace applications are studied. Aircraft platforms are increasingly being electrified necessitating usage of power converters for interfacing on-board sources and loads. Reliability of power converter systems is a key design requirement for future electric aircrafts.

This thesis concentrates on predicting wear-out and cosmic ray induced random failures of drive converters. Various system voltage levels as well as two converter topologies are studied. The predicted reliability curves under a short haul aircraft mission profile are presented. It is shown that cosmic ray induced random failures dominate at higher system voltages in silicon IGBT based power converters. It is noted that SiC devices are a natural choice due to their resilience against cosmic ray failures.

In order to address availability requirement due to the dominance of random failures, fault tolerance of multi three phase machines is presented. ABC domain model of a dual three phase machine is presented which can be extended to N three phase machines. The developed model can also represent fault states in the machine.

The fault mode operation of dual three phase machine demonstrated a limp-home functionality by extracting torque from the damaged winding set under open phase faults. Even under dual open phase fault, approximately 25% torque can be realized using the fault tolerant controller. Furthermore, the controller architecture using PR controllers are easily reconfigurable with minimal modification enabling faster and straight forward validation of firmware for certification purposes.

Acknowledgement

I would like to start by dedicating this thesis to Dr. Alessandro Costabeber. He recruited me to University of Nottingham and guided me in understanding the basics of doing a Phd and helped me to contain my natural tendency to look into too many things at same time. Secondly, I would like to share my gratefulness to my main supervisor, Prof. Giampaolo Buticchi who took over my supervision from Dr. Alessandro. I have learned so much from Prof. Giampaolo and he made the Phd journey truly special. Prof. Giampaolo's focus on practical aspects of power electronics is truly remarkable and I'll be forever grateful for the opportunity to work under his guidance. Thirdly, I would like to thank my co-supervisors Prof. Michael Galea and Prof. Pat Wheeler for their valuable suggestions to improve the work. I would also like to acknowledge the INNOVATIVE Doctoral Program, for financially supporting this Phd work through the Marie Curie Initial Training Networks.

Many thanks to all the colleagues from Institute for Aerospace Technology (IAT) and Power Electronics, Machines and Control (PEMC) group. Special thanks to Giovanni Migliazza for being a great friend who taught me how to approach PCB design and for being my guardian during a short stint in Reggio-Emilia. I would also like to thank Filippo Savi. His help was crucial in putting together the lab setup after the interruptions in 2020. It was a pleasure to work alongside Filippo and his technical excellence inspires me to push myself further. I would also like to acknowledge my fellow phds students in IAT/PEMC Milos, Hery, Sarah, Jiajun. I am really grateful for the support from Dr. Michele Degano in getting all the necessary equipment in PEMC lab to finish the experiments.

Last but not least I would like to thank my family, especially my mother who is the reason for all I am today and Monika, for pushing me to take risks and always being there for me.

Contents

List of Figures

List of Tables

Acronyms

3L-NPC Three Level Neutral Point Clamped.

ADC Analog to Digital Converter.

AEA All Electric Aircraft.

ALT Accelerated Lifetime Testing.

ATC Active Thermal Control.

CR Cosmic Ray.

EMF Electromotive Force.

EMIF External Memory Interface.

EOC End of Conversion.

FIT Failure In Time.

FPGA Field Programmable Gate Array.

HALT Highly Accelerated Lifetime Testing.

ISR Interrupt Service Routine.

MCU Micro Controller Unit.

MEA More Electric Aircraft.

PoF Physics of Failure.

PR Proportional Resonant.

PWM Pulse Width Modulation.

RUL Remaining Useful Lifetime.

SEB Single Event Burnout.

SEE Single Event Error.

SPI Serial Peripheral Interface.

TRM Technical Reference Manual.

VRR Voltage Ripple Reduction.

WBG Wide Band Gap.

Chapter 1

Introduction

Global demand for air travel is increasing year on year. In order to meet customer demand for point to point connectivity, airlines are introducing new flight routes. The order books from aircraft manufacturers reveals an unprecedented demand growth in the coming decades. Airbus estimates that the number of passenger aircrafts in operation would double by 2037 compared to the more than 20000 operational aircrafts in 2018 [2]. The demand growth with status quo in aircraft technology would result in increasing emissions and fuel consumption from aviation sector [3].

Increasing attention is being placed on reducing carbon emissions from mobility. Aviation sector as one of the fastest growing contributors to greenhouse gas emissions is being closely scrutinized by governments and regulatory bodies to satisfy global emissions reduction agreements. In 2019, global aviation industry accounted for around 2% of human-induced CO2 emissions [10]. Furthermore, fuel costs account for 25% of the overall operating costs of airlines [11]. The rising costs of jet fuel presents an even more pressing reason for airline operators to focus their attention on fuel efficient aircraft [12]. The reduction in fuel usage is increasingly necessary to meet license to operate requirements from regulatory bodies and to comply with environmental goals. Airlines have invested $1trillion in the 2009-2019 period to improve fuel economy of the aircraft fleet [10]. However, the air travel demand will accelerate in developing countries and will offset the gains in emissions reductions due to efficiency improvements as shown in

1.1. Domestic demand in fast developing economies like China would sustain the demand growth for air travel even after the pandemic induced slowdown.

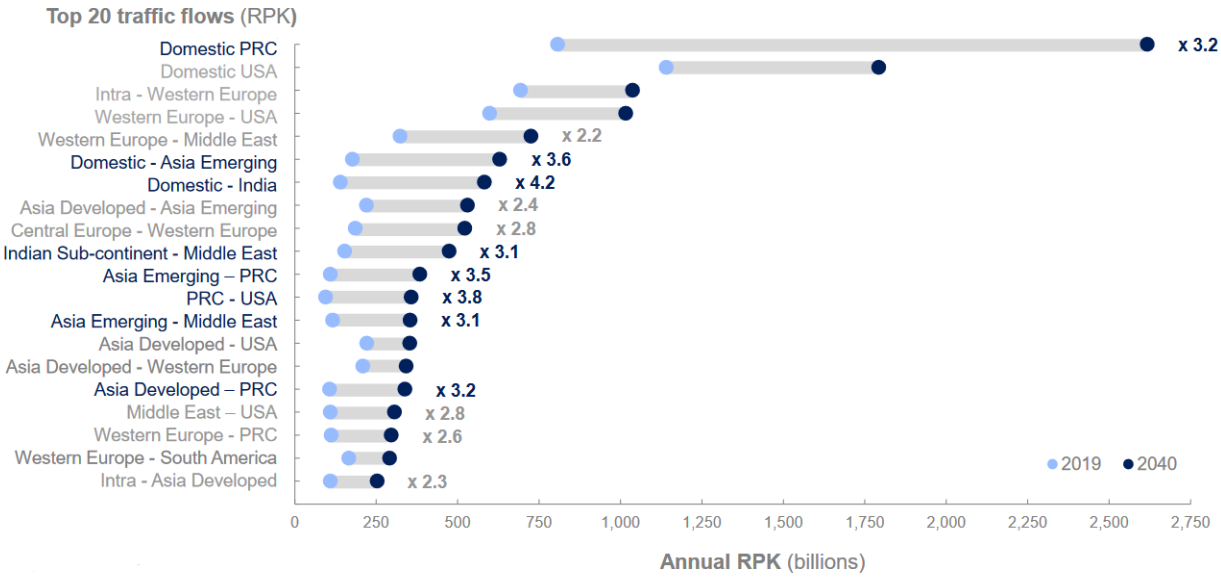


Figure 1.1: Projected passenger traffic to 2040 [2]

Various approaches are being adopted by aircraft manufacturers to meet the fuel economy and green goals. For instance, the retrofit of winglets have achieved considerable fuel savings of the existing aircraft fleet. Another key approach, towards which this thesis is focused on, is the More Electric Aircraft (MEA) and All Electric Aircraft (AEA) approaches [13]. The MEA concept is already making an impact on aircraft design by electrification of aircraft subsystems [3]. In the MEA concept, aircraft subsystems, such as hydraulic and pneumatic air systems, are replaced with electrical counterparts. It is envisaged that electrically-driven subsystems could achieve an improved overall efficiency while reducing aircraft weight compared to conventional solutions. Research efforts are also ongoing for electrification of taxiing to improve ground operations [14].

On-board power generation has exceeded 1MVA with B787 dreamliner [15]. The trend of on-board power generation shows the pivot to AEA and MEA concepts by aircraft manufacturers 1.2.

The power generation and distribution systems were based on the usage of electrical power as a utility system. The power system has also evolved over time as electrical

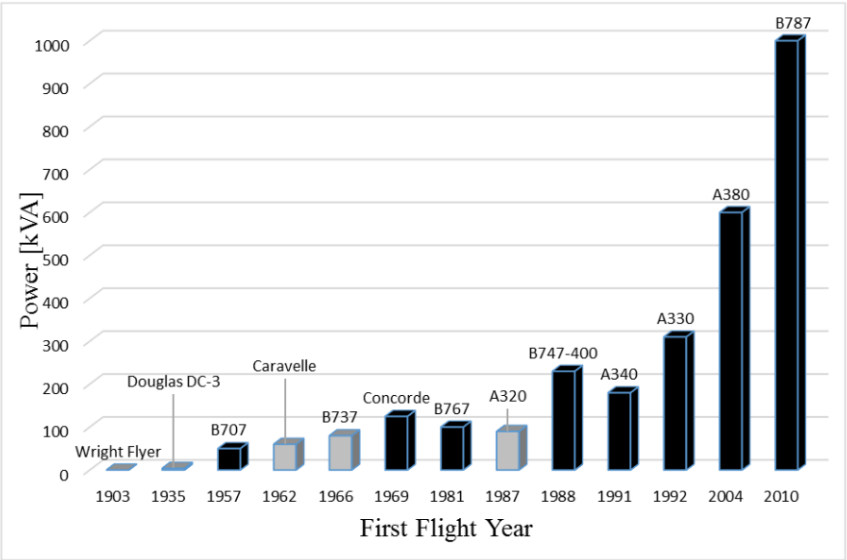
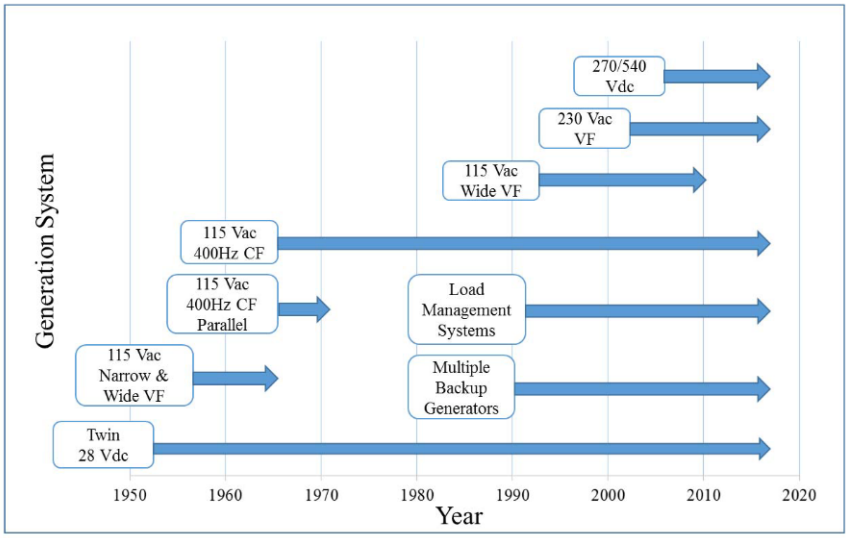


Figure 1.2: Evolution of electrical power need [3]

power requirements increased as shown in 1.3.



CF: Constant Frequency; VF: Variable Frequency

Figure 1.3: Evolution of electrical power system [3]

Future aircrafts which rely on electric propulsion would need to achieve higher efficiency and availability of the electrical system. Next generation of hybrid, AEA and MEA concepts would require adoption of power converters especially electric drives to interface the on-board generation and drive the electric propulsion motors. Such architectures are being explored to assure system level reliability requirements such as DC power distribution systems as presented in 1.4.

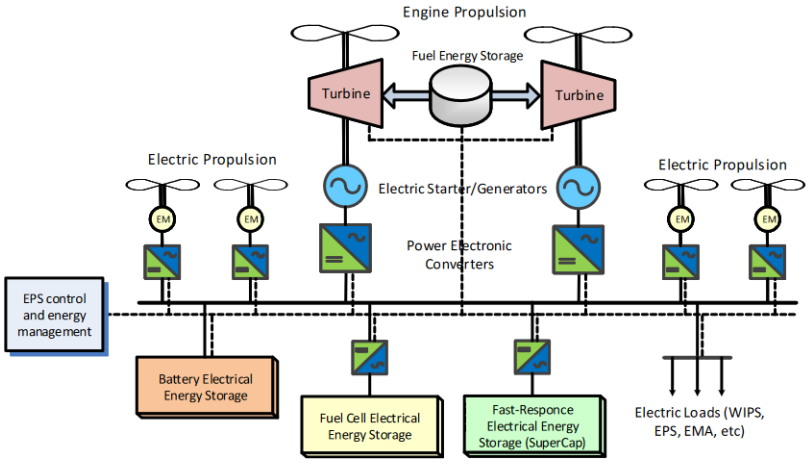


Figure 1.4: Potential future EPS for hybrid aircrafts [4]

Furthermore, motor drives are used for various other applications on aircrafts - actuators for flight controls including throttle control, interface for AC generators to future DC power sytems, auxiliary systems such as landing gear actuation, air conditioning and sanitation systems etc [16]. Hence the reliability of drive systems are critical for safe operation of current and future aircrafts. From among the various applications of the electric drive, a starter generator system is very interesting. It is already implemented in many aircrafts and is a stepping stone to future AEA and MEA concepts as it covers bi-directional power capability. Hence the starter generator is selected for further studies in this work.

The core of the electric propulsion system is the electric drive, which consists of electrical energy source [battery energy storage system(BESS), fuel cell systems or hybird sources with conventional energy], electric motors, power electronic converters, control platform and sensors [4]. A schematic representation of a drive system to interface with motors/generators is provided in 1.5. As the power distribution system evolves AC or DC coupled drive systems would be implemented on future aircrafts.

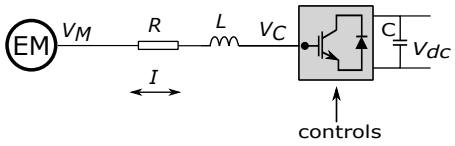


Figure 1.5: Typical electric drive system

In aerospace applications, electric drives must feature good efficiency along with a

remarkable power density. The latter is obtained by pushing component performance, thus exposing them to considerable stresses - thermal, mechanical and environmental, which might compromise both component and system level reliability. Aerospace sub-systems must meet very high reliability standards due to their safety critical nature. Hence in aerospace electric drives, reliability must be included as key design objective for simultaneously targeting the competing requirements of power density and reliability.

The main sources of failures in electric drive components include:

1. Energy source – BESS thermal runaway, fuel cell system breakdown etc;
2. Electric motors – bearing failures, insulation failures;
3. Power electronic converter – semiconductor switches, capacitors, gate driver, PCBs etc [17];
4. Connection components – cables, connectors.

The main research focus of this work is on the reliability of power electronic converter for aerospace applications while other components will not be addressed.

1.1 Research objectives

The main research objective of this work was centered around developing guidelines for design of future high voltage drive converters for aviation. The main objective was addressed by the following sub goals:-

1. Reliability estimation - Typically wear-out failures are only considered in Physics of Failure (PoF) based reliability estimation of power converters. Aerospace operating conditions include a random failure mode caused by Cosmic Ray (CR). Combining both failure modes for reliability estimation is one of the research goals of this work.
2. Reliability based converter design guidelines - This goal is aimed at generating design guidelines such as selection of components and toplogies for future aircraft

converter systems based on analysis of converter reliability at various system voltage levels.

3. Failure mitigation measures - One of the research goals is to identify methods to mitigate against random failures due to CR.

4. Availability - Fault tolerance and redundancy are key aspects of aircraft systems. Hence to conclude the system design angle from availability point of view, a study on fault tolerant drive system which can provide fault tolerant operation is also addressed.

1.2 Contributions of this work

The novel contributions from this work are summarized below:-

1. Reliability oriented design of aerospace converters - A case study was carried out accouting for the aerospace mission profile to establish appropriate topologies and devices suitable for aerospace application. Case study and results are presented in chapter 3. Cosmic ray failures are confirmed to be the dominating failure mode of aerospace converters based on the results from reliability estimation case study. Based on the case study, multi level converters such as 3L-NPC converter and Wide Band Gap (WBG) such as SiC devices are recommended for future high voltage aircraft converters.

2. Failure mitigation measures - Chapter 4 shows application of thermal control to trade-off wear-out reliability to improve robustness against CR induced failures.

3. Availability - Chapter 6 addresses fault mode operation of a multi three phase machine to address availability considerations for safety critical use case. A machine model in ABC domain for a dual three phase machine is presented. Key contributions are ABC domain controllers which enable operation in fault mode with minimal modification to control structure easing certification of control software.

1.2.1 Thesis organization

The thesis is organized into chapters and the key results in each and the relationships between them is summarized below:-

1. Chapter 2 - An overview of the state of the art in reliability assessment for power converters is presented. The lifetime models of key components and reliability estimation methodology presented is used in subsequent chapters.

2. Chapter 3 - A reliability case study of a starter generator drive converter is presented using the method introduced in chapter 2. The results highlights the prominence of CR induced random failures in high voltage aerospace converters. Hence multi level topologies and wide band gap devices are recommended as suitable candidates for aerospace application.

3. Chapter 4 - The mitigation measures against CR induced random failures are studied.

4. Chaper 5 - 3L-NPC converter is chosen as the topology to study further based on the results from chapter 3. An overview of the operation of the 3L-NPC topology and a critical aspect of its operation - the neutral point balancing is presented. This method is utilized for fault mode operation of 3L-NPC converter driving multi 3 phase machine.

5. Chapter 6 - Availability requirement is studied in this chapter. ABC domain model of a dual three phase machine and fault tolerant controllers in ABC domain are presented. Faulty and healthy mode operations are validated with simulations and an experimental prototype.

6. Chapter 7 - Thesis is concluded with key results and recommendations for future works.

1.2.2 Publications list

The following publications are results of the research investigations carried out as part of this thesis:

1. J. Harikumaran, G. Buticchi, G. Migliazza, V.Madonna, P.Giangrande, M. Galea, A. Costabeber and P. Wheeler, "Failure Modes and Reliability Oriented System Design for Aerospace Power Electronic Converters," in IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 53-64, 2021, doi: 10.1109/OJIES.2020.3047201.

2. J. Harikumaran, G. Buticchi, M. Galea, A. Costabeber and P. Wheeler, "Reliability Analysis of aircraft starter generator drive converter," 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), 2019, pp. 1-6, doi: 10.1109/COBEP/SPEC44138.2019.9065643.

3. J. Harikumaran, G. Buticchi, G. Migliazza, P. Wheeler and M. Galea, "Reliability oriented thermal management of aircraft power converters," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 1590-1594, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9367638.

4. J. Harikumaran, G. Buticchi, M. Galea and P. Wheeler, "Open Phase Fault Tolerant Control of Multi Three Phase Machines," in IEEE Open Journal of Power Electronics, vol. 2, pp. 535-544, 2021, doi: 10.1109/OJPEL.2021.3115404.

5. D. De Gaetano, J. Harikumaran, G. Sala, M. Degano, G. Buticchi and C. Gerada, "On Torque Improvement by Current Harmonic Injection in Isotropic and Anisotropic Multi-Phase Machines," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, doi: 10.1109/JESTIE.2021.3105337.

6. V. Madonna, P. Giangrande, J. Harikumaran, G. Buticchi and M. Galea, "System-Level Reliability Assessment of Short Duty Electric Drives for Aerospace," in IEEE Transactions on Transportation Electrification, vol. 7, no. 3, pp. 1888-1900, Sept. 2021, doi: 10.1109/TTE.2021.3053147.

7. F. Savi, J. Harikumaran, D. Barater, G. Buticchi, C. Gerada and P. Wheeler, "Femtocore: An Application Specific Processor for Vertically Integrated High Performance Real-Time Controls," in IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 479-488, 2021, doi: 10.1109/OJIES.2021.3112124.

Chapter 2

Introduction to Physics of Failure based Reliability Estimation of Power Converters

Abstract - An introduction to reliability assessment of power electronic converters and the methodology followed for reliability estimation in this work is presented. The state of the art in power electronics reliability estimation has transitioned from constant failure rate models published in military handbooks to Physics of Failure based models by utilizing component lifetime models. The key failure prone components in power converter systems are presented and the methodology for quantifying reliability based on expected mission profile of power converter is outlined in this chapter.

2.1 Reliability engineering and failure distributions

Reliability in an engineering sense is defined as the probability that a system will perform the intended function for a specified period of time under a given set of operating conditions [18]. It can also be defined as the chance of survival of devices in a large set of similar devices upto a certain usage period. Reliability has no meaning for a single device only as it is a population property. Hence it needs to be quantified using probability distributions. Based on the descriptions, we can see that reliability is a cu-

mulative distribution function (as it is relating to the survival probability upto a certain point). Reliability and its complimentary function unreliability is usually quantified using a probability distribution, for instance the Weibull distribution.

In the case of component manufacturers, it is not feasible to anticipate the operating conditions of every application. Hence, lifetime models are published after performing lifetime testing (typically Accelerated Lifetime Testing) on a batch of components [17]. Lifetime data thus obtained is statistically processed to provide a lifetime model dependent on applied stresses. Such lifetime models typically provide a median lifetime prediction of the component. The reliability assessment of a system combines lifetime models, mission profile and statistical uncertainty to provide time dependent lifetime predictions .

2.2 Reliability estimation of power electronics

Prior to the advent of PoF based methods, reliability engineering in electronics and power electronics was performed based on constant lifetime models published in handbooks, for instance Military Handbook 217-F. However, with the increased pace in introduction of new technologies and focus on developing physics based lifetime models have resulted in the cancellation of the Military Handbook 217-F in 1995. MIL 217 still stands cancelled and has not been updated since it was cancelled. Similar look up table methods still active, however has serious shortcomings due to the reliance on narrow data sets and invalid assumptions [19]. Power converter reliability assessment has progressively shifted from empirical safety margins from military hand books towards physics-of-failure based reliability estimation methods [20], [17]. These analyses are performed earlier in the design stages to feed into the detailed engineering phase of the converter system development. Mission profile based reliability studies have been reported in literature quantifying component deterioration and system reliability for different power converter use cases, i.e. railway traction [21], electric vehicle [22], wind power [23] and aerospace [24].

In this introduction an overview of the lifetime estimation methodology for power

converters are presented starting with the PoF models of lifetime limiting components.

2.2.1 Lifetime estimation of semiconductors

Wear-out failure mechanisms in semiconductors

During power converter operations, semiconductors experience cyclic power losses especially in electric drive due to the sinusoidal input or output waveforms. Repetitive power losses and consequent thermal cycles result in cyclic fatigue stresses in power modules as material properties (for instance, coefficient of thermal expansion) of semiconductor substrate, insulators and base plate metal are different [5]. Mean junction temperature of semiconductor also leads to thermal ageing by chemical processes [17, 25]. An additional failure mode of power semiconductors due to high energy cosmic radiation in the atmosphere was identified based on operational data from railway traction converters.

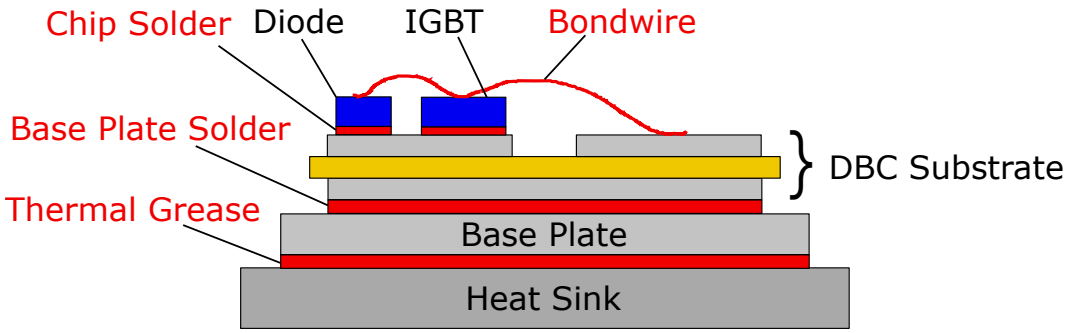


Figure 2.1: IGBT module cross section [5]

The key lifetime limiting sub-components in a power module are marked in red in 2.1. Most of the failure models have focused on the degradation of bondwire leading to lift-off and crack in the chip/base plate solder. Newer packaging concepts such as press-pack and silver sintering have been introduced to address both of the above failure modes respectively. Another important failure prone sub-component is the thermal grease. The dominant failure modes of thermal grease is summarized in [26] as pump-out or dry-out, presence and subsequent evaporating of viscosity lowering solvents, exposure to humidity etc. Thermal grease failure has not considered in this study.

The most comprehensive lifetime model for power modules was developed by Infineon named after Prof. Bayerer [27]. The model accounts for thermal stresses as well as

module specific characteristics. Semikron power semiconductor manual lists the lifetime model as reproduced in (2.1), where N_f is module lifetime in number of thermal cycles when subjected to thermal cycles of magnitude δT_j with minimum junction temperature $T_{j,min}$ during the thermal cycle with cycle heating time t_{on}. A is a curve fitting constant, I_B is current per bond wire, V_C is the voltage class of the module and D is the bond wire diameter in μm.

$$N_f = A \cdot \Delta T_j{}^{\beta_1} \cdot exp^{\left[\frac{\beta_2}{T_{j,min}}\right]} \cdot {t_{on}}^{\beta_3} \cdot {I_B}^{\beta_4} \cdot {V_C}^{\beta_5} \cdot D^{\beta_6} \tag{2.1}$$

The model parameters applicable to a wide range of modules are summarized as $A = 9.34E14; \beta 1 = -4.416; \beta 2 = 1285; \beta 3 = -0.463; \beta 4 = -0.716; \beta 5 = -0.761; \beta 6 = -0.5;$. The validity range of sub terms of the lifetime model is also provided in [5]. Lifetime models and parameters for SiC modules are not widely available in literature. One of the available lifetime studies on SiC devices highlight lower lifetime figures of SiC modules compared to Si [28]. The above work concludes that as the Young's Modulus of SiC material is higher than Si, the solder layer in a SiC module experiences higher fatigue stresses than in a Si module for the same junction temperature profile. The published results are valid in the temperature swing range of [90 - 140] °C. The lifetime model parameter is updated to $A = 4.67E14$ based on the results from [28] to reflect the increased thermal fatigue in SiC modules.

Cosmic ray induced random failures in semiconductors

Highly energetic atomic particles and ions are generated in the Earth's atmosphere due to cosmic radiation. The impact of CR on avionics and space systems originally drew the attention of system designers. In low voltage electronics, cosmic radiation predominantly results in Single Event Error (SEE), which is observable as bit errors in memory modules [29]. The mechanisms and the mitigation measures are well known for low voltage systems. The classic work from IBM on terrestrial cosmic rays [30] gives a comprehensive review on SEE mechanisms due to nucleon flux in semiconductor chips. SEE is not a breakdown event as there is not enough energy at low voltages.

In high voltage power semiconductors, these particles upon collision with atoms in semiconductor bulk, cause nuclear reactions [31]. The fission products of nuclear reactions deposit a charge in semiconductor bulk. Thus, the high electric field present during reverse blocking mode (as shown in Fig. 2.2) could result in development of a streamer of electrons and holes that might lead to a sudden device destruction, due to short circuiting of a phase leg [32], [33]. Wide band gap devices are more immune against CR failures since the breakdown field in the bulk semiconductor is higher. Furthermore, the device area required for same ratings are less compared to Si devices.

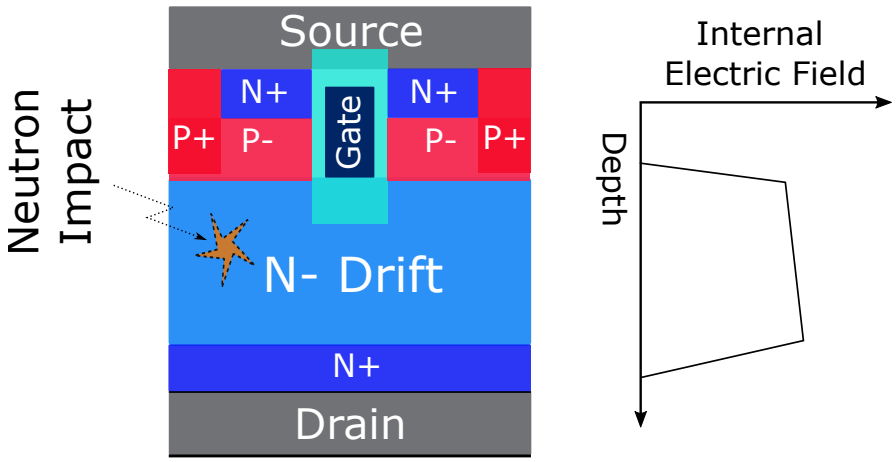


Figure 2.2: SiC Mosfet (trench stop) Cross section and internal electric field in blocking mode

The main factors influencing cosmic ray failure rate are reverse blocking voltage rating as well as particle flux intensity with sufficient energy. Emphasis is placed on atmospheric neutron intensity as it is the main contributor to cosmic ray failures in the Earth's atmosphere [31]. Cosmic ray failure is a complex physical phenomena and hence generalized failure models are not available. An analytical failure model for few specific modules considering blocking voltage, junction temperature and atmospheric altitude was proposed in [34].

The IEC standard 62396-4 specifically addresses SEB in high voltage power devices for aircraft applications [29]. According to IEC62396, the neutron flux density at any point in the atmosphere could be obtained by scaling the value given at a reference location specified by its latitude, longitude and altitude. A neutron flux of 6000 $/cm^2h$ is reported for neutrons with energy $> 10MeV$ at an altitude of 40000 ft at 45°latitude [35]. The

above value is recommended by IEC 62396 to evaluate SEB failure rate. The estimation procedure outlined in [29] relies on experimental measurement of cosmic ray failure rate during exposure to reference neutron flux intensity.

IEC recommendations are adopted in this work to predict cosmic ray failure rate from experimentally reported failure rates for selected modules [36], [37].

2.2.2 Lifetime estimation of capacitors

Reliability analysis of capacitors for power electronics is usually performed based on the well known Arrhenius degradation model [38], [39]. Along with temperature, applied voltage and humidity adversely affect capacitor lifetime [38]. The effect of humidity can be ignored when capacitors are hermetically sealed. A lifetime model addressing effects of temperature and voltage is provided in (2.2), where L is the capacitor lifetime under test conditions (hot spot temperature T and applied voltage U), while L_0, T_0 and U_0 are lifetime, hot spot temperature and applied voltage at reference conditions [40]. E_a is the activation energy term, k_b is Boltzmann constant and β is a curve fitting term based on device technology. The norm for high reliability applications is to select film capacitors for DC link capacitors. Lifetime model of film capacitors is shown in (2.2).

$$L = L_0 \cdot exp^{\frac{E_a}{k_b}\left(\frac{1}{T}-\frac{1}{T_0}\right)} \cdot exp^{-\beta\left(\frac{U-U_0}{U_0}\right)} \tag{2.2}$$

In the presented investigation these values are adopted: $L_0 = 1E5$ hours; $T_0 = 70C; \beta = 3.5; E_a = 9.891E{-}20; U_0$ = rated voltage of the capacitor under study. A key distinction is drawn to the attention of readers that, the lifetime model predicts an increase in lifetime as operational temperature is reduced. In the case of aerospace applications, the ambient temperatures can reach -50 °C or lower. The predicted lifetime figures would be unreasonably high. There are very few prior works in literature which reports capacitor lifetime at low temperatures. It was reported in [41] that film capacitors show very little degradation in electrical parameters at low temperatures. A clear

guideline on capacitor lifetime modelling at low temperatures is stated in IEC 61709 [42]. The standard specifies usage of a constant failure rate for capacitors based on expected lifetime at 25 °C.

2.2.3 Lifetime models to reliability prediction

Reliability assessment starts with establishing a mission profile which accounts for ambient conditions and operational requirements of the system. Converters are subjected to dynamic stress profile in operation due to variations in environmental conditions and system operation. Lifetime limiting stress components of individual sub-components are extracted from the mission profile. Reliability analyses of power converters place emphasis on prominent failure prone power electronic components - semiconductor switches and capacitors [43]. The dominant wear-out failure mechanism in those components is thermal stress degradation [17]. Electro-thermal co-simulation models are established of varying temporal resolution to establish the thermal stresses experienced in a period of time.

The mission profile based reliability estimation methodology considering wear-out failures of IGBTs is summarized in Fig. 2.3. The statistical variation of lifetime parameters is addressed with a Monte Carlo analysis. The results from Monte Carlo analysis is curve fitted to a Weibull distribution to obtain time dependent failure probabilities.

This is a widely adopted methodology in previous lifetime modelling studies considering only wear-out failures [44]. The same methodology is applicable for lifetime estimation of capacitors with slight modifications. This method is utilized in the following chapter 3 to estimate reliability of converter systems under study.

A brief description of the various steps involved in reliability prediction is provided here.

Mission Profile

Establishing the mission profile is the first step in estimating lifetime predictions of any component. As per [45], “It is a combination of influences that an electronic product is

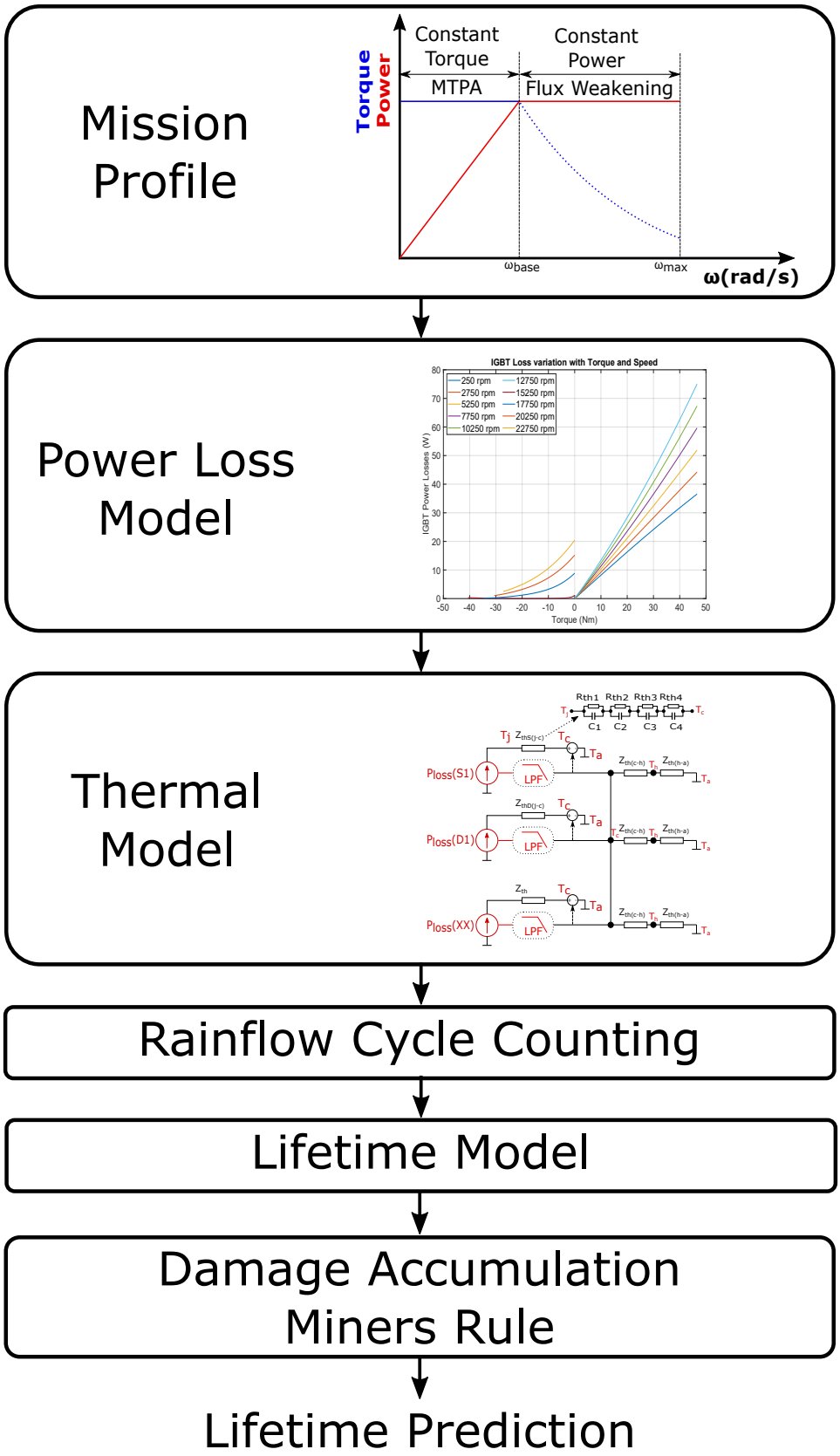


Figure 2.3: Mission profile based reliability estimation methodology for IGBTs

subjected to in its specific application during its service life, and which have an effect on its reliability. This may involve both environmental factors, such as temperature or vibration, as well as performance parameters such as current or voltage."

Mission profile for reliability assessment needs to provide intensity and duration of stress events. The resolution required is dependent on established lifetime models. For instance, high frequency vibrations are sometimes not considered for lifetime degradation as the design assumes only elastic deformation in the high frequency regime. In power electronics research field, mission profiles are established based on published environmental data and expected power demands on the systems. Research efforts are ongoing to establish a unified mission profile standard for various reliability assessment in line with automotive drive cycle standards [46].

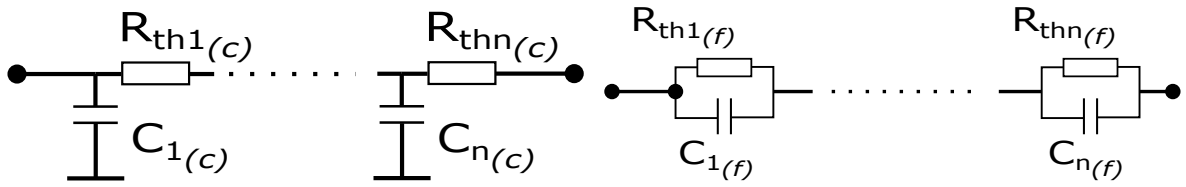
Thermal loading estimation

Once the mission profile is established, the next step is to translate that to stress factors of interest. In the lifetime models for power electronic components, thermal loading is a key lifetime limiting stress factor. Power losses during operation along with ambient temperature generate the thermal loads. Thermal model of components help in translating power losses to thermal loads. Conduction and switching losses are the chief mechanisms for generating power losses in power semiconductors, while conduction losses in ESR contributes to capacitor losses.

Based on the physical structure of the components, the thermal behaviour can be modelled as thermal resistances and capacitances in a similar manner to electrical networks. The advantage of this approach is the reuse of similar solvers to solve electrical and thermal simulations. However, unlike electrical properties, thermal models are only valid for a system as a whole. When multiple components are connected together, the behaviour of the system as a whole cannot be modellled by connecting together thermal models of individual parts due to thermal interaction between the components. Usually electronic part vendors provide the effective thermal behaviour of the semiconductor accounting for the substrate, packaging, and casing. As the size of thermal grease is much

smaller and the heatsink can be approximated as an infinite sink due to physical size, the effect of these two components are added to the model as if the effective thermal model does not change.

There are two main modelling paradigms followed in thermal models - Foster networks and Cauer networks. The make up of the models are shown in Fig. 2.4.



(a) Cauer Network Model (b) Foster Network Model

Figure 2.4: Thermal Models

Cauer network is more representative of the thermal behaviour of the devices however extracting the network parameters are not always possible. Foster network is computationally curve fitted to the experimentally measured thermal properties [47]. It is possible to convert between the two models depending on the modelling needs. A new approach has been proposed in [6] to overcome the limitations of the above introduced thermal models. It has been adopted in this work to improve the accuracy of the thermal modelling. This method plugs the shortcomings in Foster models by accounting for thermal storage effect. The thermal model for an IGBT module is shown in 2.5.

The method to extract the parameters of the Low Pass Filter (LPF) included in the above model. In order to account for the thermal storage effect an additional transfer function is defined as $G_{P_{in}P_{out}}(s)$ in addition to the thermal impedance $Z_{P_{in}T_{JC}}(s)$. It is shown in [6] that the dominant frequencies in the above transfer functions are closely related and by identifying the corner frequencies from $Z_{P_{in}T_{JC}}(s)$, the thermal response can be refitted with a new Foster network with same number of RC elements. The inverse of the time constants of the newly fitted Foster network provides the pole frequencies of the LPF represented by the thermal power flow transfer function - $G_{P_{in}P_{out}}(s)$. A detailed calculation following the above method is shown for one particular power module in 3.

The LPF parameters for the power loss transfer function is derived based on the relationship between foster thermal model corner frequencies and power loss transfer

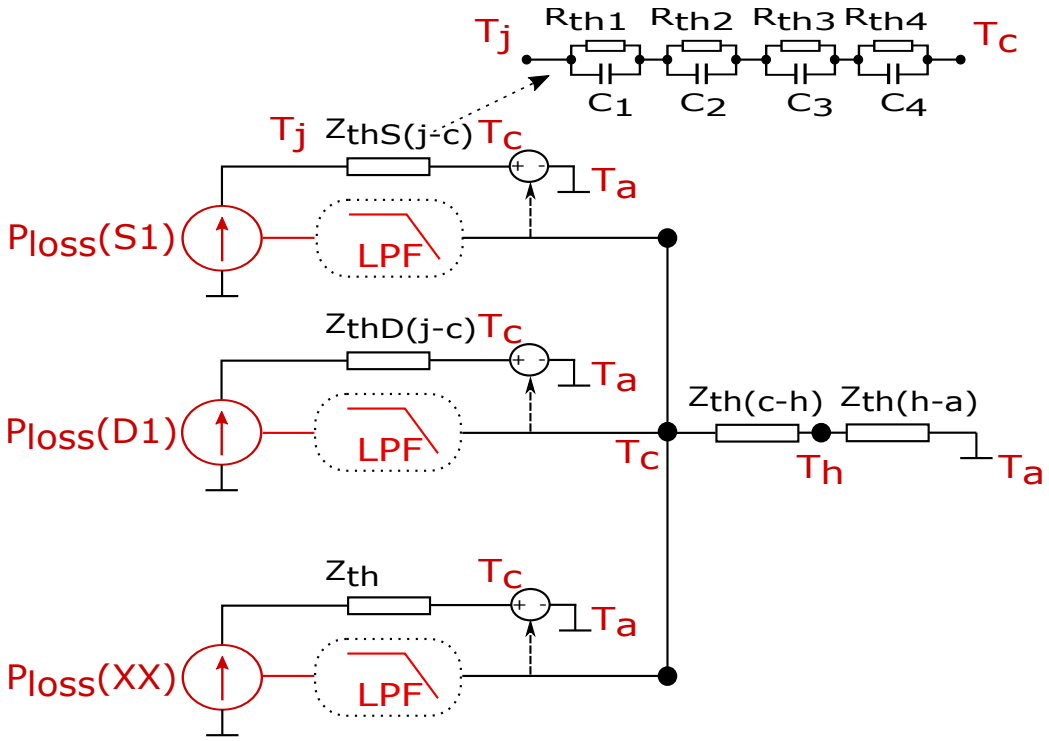


Figure 2.5: Modified Foster Network model [6]

function. Ignoring high frequency behaviours, the thermal impedance based on an exact Cauer network can be expressed as Eq.(2.4).

$$Z_{P_{in}T_{JC}}(s) \approx G_{P_{in}P_1}(s) \cdot R_{c(in--1)} + G_{P_1P_2}(s) \cdot R_{c(1--2)} + \cdots + G_{P_{n-1}P_n}(s) \cdot R_{c(n-1--n)} \tag{2.3}$$

The critical frequencies of the above relationship is equivalent for both Cauer and Foster representation. Thermal impedance as a function of Foster parameters is expressed in Eq.(2.4).

$$Z_{P_{in}T_{JC}}(s) = \sum_{i=1}^{n} \frac{R_{f(i)}}{\frac{s}{2\pi f_{cr(i)}} + 1} \tag{2.4}$$

Hence we can identify the critical frequencies making up the LPF of the power flow transfer function from the foster representation of the thermal impedance. A deviating

operator $F(x)$ is applied to $Z_{P_{in}T_{JC}}(s)$ to identify the corner frequencies.

$$F(x) = \frac{d^2}{dx^2} 20 \cdot log_{10}(|Z_{P_{in}T_{JC}}(x)|) \tag{2.5}$$

The corner frequenices from thermal impedance, $f_{cr(n)'}$ are closely related to the corner frequencies, $f_{cr(n)}$ of the LPF. The actual corner frequencies are obtained by refitting the $Z_{P_{in}T_{JC}}(s)$ with identified number of corner frequencies.

Rainflow cycle counting method

In cases where only the absolute temperature governs the lifetime of the device, the thermal loading information directly provides the temperature information. In the case of power semiconductors cyclic stress fatigue is identified as a failure cause and it is highlighted by the presence of the temperature cycling term in the lifetime model. Rainflow cycle counting is one of the methods most commonly used to count stress-strain cycles. It is defined in the ASTM E1049-2011 standard [48]. In reliability analysis of IGBTs, rainflow counting is used to count the temperature cycles (amplitude and duration) experienced by the IGBTs during operation. A comparative study on various cycle counting methods was conducted in [49] by comparing actual damage caused by thermal cycles to the damage predicted with the cycles counted by various algorithms. Rainflow counting method shows the lowest error compared to the actual damage. The algorithm is explained in [7] as well as various other sources. Matlab has implemented rainflow counting as a function from the 2018a release. A flowchart to implement the rainflow counting is presented in [50]. However a more simpler explanation is reproduced below.

- Find the first local minima or maxima in the data set (the order has no influence). In this eg: the local minima occurs first and the cycle counting will start from minima

    - The half cycle from the minima continues until the next minima which is **lower** than the starting value is encountered. The amplitude and duration is

the difference from the starting minima and **highest** maxima encountered in the half cycle. Half cycle A illustrates this case.

- Half cycle from minima also ends if it encounters another half cycle which started from a minima. Half cycle C illustrates this case. The duration and amplitude is then obvious from the figure.
- Repeat the steps until all minimas in the dataset are processed.

- Start cycle counting from the maximas
  - The half cycle from the maxima continues until the next maxima which is **higher** than the starting value is encountered. The amplitude and duration is the difference from the starting maxima and **lowest** minima encountered in the half cycle. Half cycles B and D illustrate this case.
  - Half cycle from maxima also ends if it encounters another half cycle which started from a maxima.
  - Repeat the steps until all maximas in the dataset are processed.

- Full cycles (post processing step)
  - Half cycles B and C together form a full cycle and the algorithm would output them as a full cycle with amplitude and duration. Another full cycle from this example is formed by half cycles E and F.
  - Full cycles can be directly used in lifetime models or stress-strain equations

- Half cycles which dont form a full cycle (post processing step)
  - Half cycles which dont form a full cycle needs to be handled in a post processing step. They are either combined together in cases where complimentary half cycles are found (one starting from a minima and another from a maxima with identical starting and end conditions)

- In some studies half cycles are handled by assuming they cause half the damage of a full cycle and the lifetime is doubled to account for the half cycle. This is not a trivial assumption.

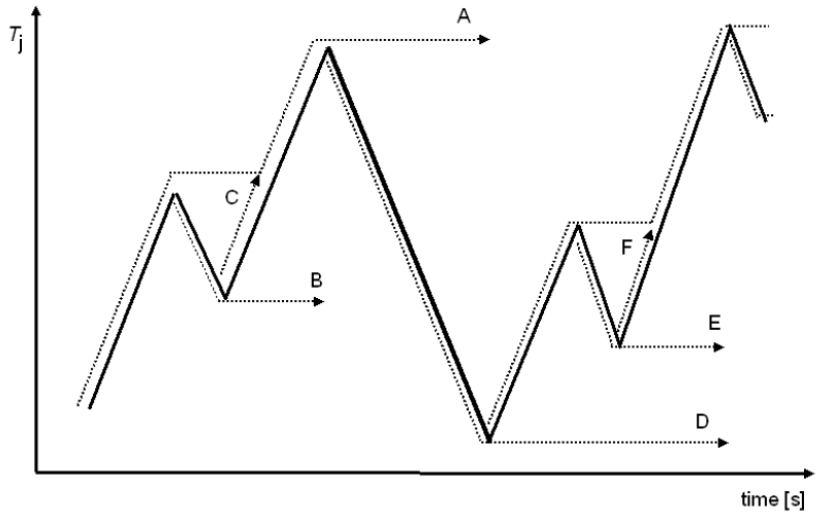


Figure 2.6: Rainflow method [7]

Monte-Carlo simulations

Monte-Carlo simulations are carried out to account for statistical variations in parameters. It is widely applied in various fields such as theoretical physics, financial modelling, pricing etc. In reliability engineering, Monte-Carlo simulations are performed to account for the statistical variations in the modelled mission profile and component lifetime model parameters. One of the key works in power semiconductor lifetime modelling is from Prof. Bayerer [27]. The Bayerer model provides the uncertainty range of the various coefficients in the lifetime model to account for modelling uncertainty and validates the necessity for Monte-Carlo simulations. It is widely adopted as a step in PoF based power electronics reliability assessment to obtain a time dependent failure distribution of components.

Monte-Carlo techniques involve three main steps [51].

- Setup the model or equation which links the prediction with independent variables. From Monte-Carlo simulation perspective, the lifetime is the dependent variable

which depends on independent variables such as model parameters and mission profile stress profiles.

- Specify probability distributions for the independent variables. The lifetime models are usualy published with expected uncertainty range and the distribution of the parameters. In the case of mission profile values, a normal distribution is typically employed.

- Run enough simulations by picking values for the independent variables based on their probability distribution. After enough simulation runs, the probability distribution for the predicted variable can be obtained.

2.3 Summary of reliability estimation methodology

The methodology described here is demonstrated with a case study in chapter 3. It must be noted that the above methodology relies on the veracity of the lifetime models, accuracy of thermal modelling and the applied mission profile. The lifetime models are usually provided by device manufacturers after performing Accelerated Lifetime Testing (ALT) or Highly Accelerated Lifetime Testing (HALT) testing of power modules. It is not straightforward or useful to verify the same by performing normal ageing on a module. The difficulty arises from how to monitor the ageing as the damage manifests either as increase in thermal resistance or increased stresses in the joints. The thermal modelling relies on the accuracy of the loss predictions and the thermal impedance of the module. In prior research efforts, the thermal model is validated by measuring the juntion temperature of the module as a validation approach. Even with the above caveats, the reliability modelling with PoF is accepted as the appropriate methodology for reliability assessment of power electronics.

Chapter 3

Reliability estimation for Aerospace Power Converters

Abstract - State of the art reliability estimation methodology for power converters is extended to aerospace mission profile in this chapter. Aircraft power distribution systems are evolving to HVDC systems which in aerospace context stands for system voltages higher than 270V. Reliability of voltage source power converters at different system voltage levels are modelled in this chapter based on a case study of a starter generator drive converter. The aim is to bring out the impact of system voltage levels on reliability metrics. Failures of power semiconductors and capacitors are considered in the case study. The chapter concludes with recommendations derived from the case study on power device selection based on voltage levels and topologies.

3.1 Introduction

The reliability analysis presented here fits in the PoF research framework, by analysing and quantifying through a physics-based approach the most critical failure modes in typical power converters installed in an 'aerospace environment'. Furthermore, two important gaps exist in literature regarding reliability estimation of aerospace power converters which are addressed in this chapter.

1. Aircraft on-board power systems are evolving from the conventional 400 Hz AC

grid [52] to HVDC distribution. In order to realize a light-weight electrical system, future aircraft power systems are expected to be designed for higher voltages with a possible DC grid. System voltage has a direct impact on component selection and consequently reliability estimation has to be performed at various voltage levels to give guidelines for system design choices.

2. Cosmic ray intensity at aircraft cruising altitudes is reported to be up to 300 times higher than that at sea level [30]. Impact of cosmic rays on semiconductors has been well established in literature and studied in detail for avionics (especially SEE leading to bit flips in DRAMs). Hence, as highlighted in [53], random failures due to cosmic rays must be included in reliability analysis for aerospace drive converters.

The effects of system voltage and cosmic ray failures are quantified with a case study on a starter generator drive converter. The key findings of the study are :

1. In high voltage systems (above 540V) without enhanced voltage derating, cosmic ray induced failures is the reliability limiting factor in Si IGBT based converters.

2. The results demonstrate that SiC devices are a suitable choice for future high voltage aerospace power converters. Multi level topologies must be employed to utilize Si IGBTs in order to meet reliability requirements.

The case study is carried out as follows:

- Define a mission profile;
- Perform an electro-thermal simulation to estimate wear-out failure lifetime;
- Validate electro-thermal simulation with experimental setup;
- Account for cosmic ray induced random failures;
- Execute a Monte Carlo analysis to account for statistical variation of component parameters.

A total of 7 cases were simulated to derive and compare reliability figures. Three system voltage levels - 270V, 540V and 810V were modelled, with 2L and 3L-NPC topology at each voltage level. An additional simulation case is included at 810V system voltage for 2L converter with SiC devices. The device selection of all 7 cases are summarised in Appendix A. The motor parameters, such as the back Electromotive Force (EMF) constant and the dq axes inductances, are linearly scaled with DC link voltage. The maximum electrical frequency of drive system is 1.6 kHz. The switching frequency is chosen as 20 kHz and 10 kHz for the 2L and 3L-NPC converters respectively. Switching over voltage and DC link voltage ripple are not accounted for in the analysis.

3.1.1 SG drive converter system

Starter generators are used in aircrafts to spin up the main turbine. After the main turbine has achieved operational speed, the system mode is changed to generation to feed the aircraft electrical network. A starter generator system aimed at future high speed applications was developed at The University of Nottingham [54]. The key parameters of the SG system are listed in Table 3.1 [55]. The SG drive converter was designed for a system voltage of 270V and was realized using a 3L-NPC Si IGBT converter.

Table 3.1: Starter generator parameters

Maximum Power	45 kW
Phase and pole numbers	3 phase, 6 pole
Maximum mechanical speed	32000 rpm
Stator resistance	1.1 mΩ
d-axis, q-axis inductance	99 μH
Back EMF constant, Ke	0.0259 V·s/rad

3.2 Modelled Aerospace Mission Profile of SG system

A mission profile is the defined operating conditions of a system which includes internal parameters (power, voltage, speed etc.) and external parameters (ambient temperature, humidity, altitude etc.). Mission profile is utilized to quantify the net stress applied during the lifetime of the system. In the specific case of aerospace converters, the mission profile should include altitude, ambient temperature and output power of the converter.

The following assumptions are made to generate a mission profile for a short haul aircraft. The mission profile data is generated based on publicly available information. Typical cruise altitude of 30,000 ft for short-haul flights is mentioned in [56]. The typical climb/descent rates are extracted from publicly available flight data logs from FlightAware website [57].

- The flight time at cruise altitude is approximatively 1 hour;
- Cruising altitude is fixed at 30,000 ft (9,144 m);
- Total flight duration accounting for flight preparation, taxi, take-off, landing etc. is equal to 1 hour 40 minutes;
- The same aircraft is modelled to operate 6 short haul flights a day.

A summary of the flight stages are illustrated in Fig.3.1, while the simulated durations of each flight phase are summarised in Table 3.2.

Table 3.2: Flight phase duration

Flight Phase	**Duration (mins)**
Taxiing time	10
Cruise time	45
Climb/Descent time	Based on climb rate

The climb/descent rates of commercial airlines are typically widely variable and thus are not readily available in literature. Hence, reasonable assumptions are made for the

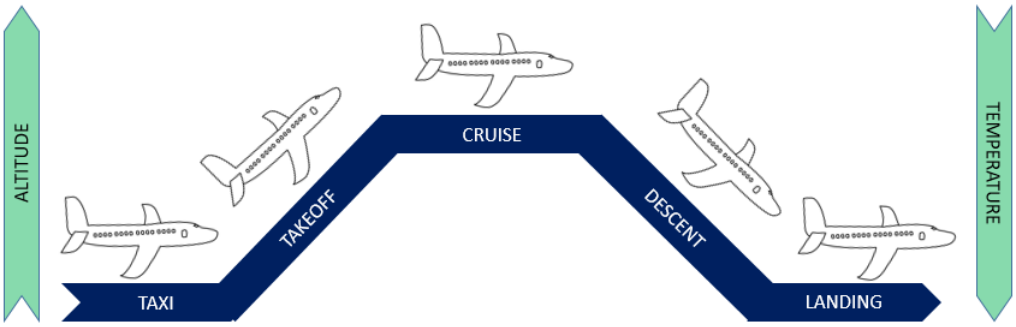


Figure 3.1: Flight stages of an aircraft

case studies as detailed Table 3.3.

Table 3.3: Climb/descent rate of aircraft

Altitude Range (feet)	**Climb Rate (ft/min)**
0-15,000	2,400
15,000-30,000	1,500
30,000-24,000	-1,000
24,000-10,000	-3,000
10,000-0	-2,000

The ambient temperature profile during flight is generated from atmospheric models. According to US standard atmosphere 1976 [58], the thermal gradient in the lower atmosphere up to 36,000 feet (11,000m) is -6.5 °C/km. Monthly average ground temperature data of London for the period Aug 2018 till July 2019 is obtained from NCEP [59].

The output power requirement of the SG system is provided in [54]. During the start-up phase, the SG works in motoring mode, while for the cruising phase, the SG operates in generation mode at 90% of rated output power (i.e. 40 kW) and 18,000 rpm. To account for operational variations during cruise conditions, 5% random variation in both output power and operating speed is modelled.

3.3 Electro-thermal simulation

The simulation model is setup in Matlab® as a two-step model. In the first (computationally intensive) step, power losses of semiconductors, output current, power factor, thermal cycles of semiconductors at fundamental electrical frequency etc are pre-calculated and stored in a 3D lookup table for a range of machine speeds and output torque. Flux weakening is also included for operation beyond base speed. This database enables fast estimation of reliability figures at different mission profiles. A simplification is performed in thermal simulation by assuming loss figures at a junction temperature of 125 °C which is a conservative approach to reliability modelling [60].

3.3.1 Loss modelling in electric drive

The main losses in a power converter are semiconductor losses [switching and conduction losses], capacitor losses [esr losses, dielectric losses] and losses in inductors and transformers [conduction losses and core losses]. Typically in electric drives, magnetic components are not required as the machine windings are sufficient to act as line filters.

Typical loss values for semiconductor devices are published in device datasheets. The losses are usually dependent on various parameters. Switching energy can be expressed as $E_{SW} = f\left(V_d, I_d, R_{gate}, T_j\right)$, while conduction losses can be expressed as $P_{cond} = f\left(V_d, I_d, T_j, V_{gate}\right)$. In this work, widely used simplified loss models are used instead of the look-up table based approach.

$$P_{SW\_IGBT} = f_{sw}(E_{on} + E_{off})\left(\frac{I}{I_{ref}}\right)^{K_i}\left(\frac{V_{off}}{V_{ref}}\right)^{K_v} \tag{3.1}$$

$$P_{cond} = Vce_{on}I \tag{3.2}$$

Ki is assumed to be 1 and Kv is taken as 1.3 in (3.1).

The main source of loss in capacitors is the effective series resistance (ESR). The DC link capacitor carries the high frequency switching components in the current spectrum. The rms value of the dc link capacitor current for 2L inverters is derived in [61] and given in Eq.(3.3) while that of 3L inverters can be estimated following the equation provided in [62] and given in Eq.(3.4).

$$I_{Crms} = I_{mrms}\sqrt{\left[2M\left\{\frac{\sqrt{3}}{4\pi} + \cos^2\phi(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M)\right\}\right]} \tag{3.3}$$

$${I_{Crms}}^2 = \frac{3Im^2M}{4\pi}\left(\sqrt{3} + \frac{2}{\sqrt{3}}.\cos(2\phi)\right) - \frac{9}{16}(I_mM)^2\cos^2(\phi) \tag{3.4}$$

The thermal model for the capacitor is a simple thermal resistor connecting the hotspot in the capacitor bulk to the ambient as shown in fig. 3.2. The thermal resistance values are published in the device datasheets.

3.3.2 Extended foster thermal model

Particular attention was paid to device thermal impedance modelling. Direct connection of Foster networks ignores the effect of thermal capacitance leading to erroneous estimation of junction temperature profile. An accurate approach of modelling thermal impedance proposed in [6] has been adopted. The thermal impedance generation for one particular device is elaborated below. The foster network parameters for the device "SKM400GB07E3" with ratings of 650V and 400A are as shown in Tab. 3.4.

The thermal impedance frequency response of the above foster parameters is shown in Fig.3.3.

The deviation operator provided in Eq.(2.5) is applied to the thermal impedance with the foster parameters listed in Tab.3.4. The gain slope change frequencies correspond to the corner frequencies of interest for the power flow transfer function and it can be identified from fig.3.4.

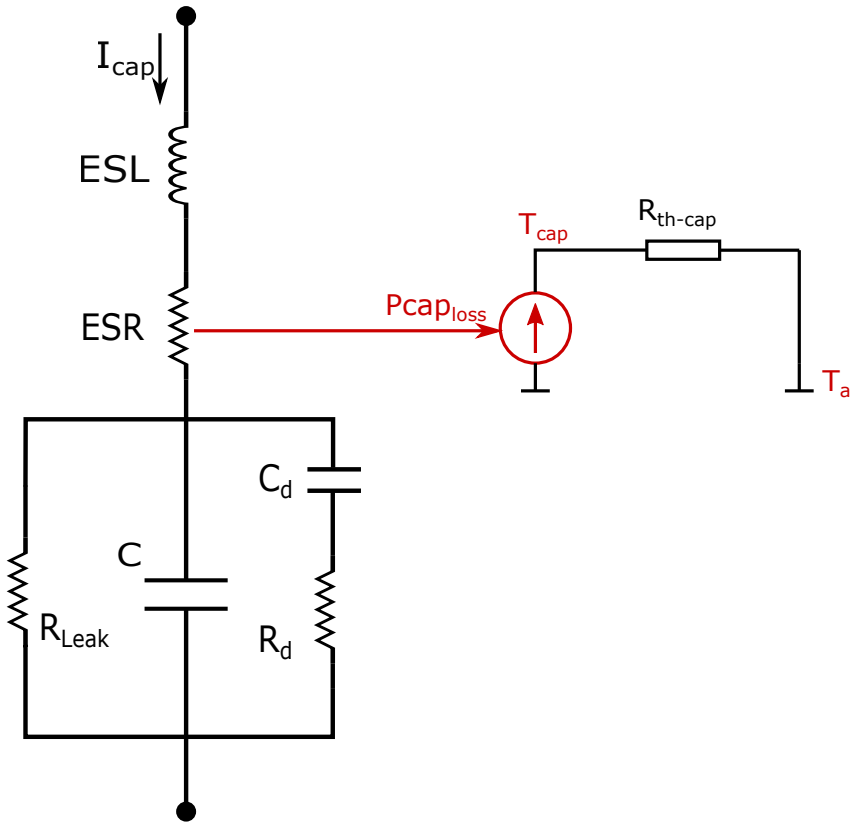


Figure 3.2: Loss model of a capacitor

Three corner frequencies including an insignificant corner frequency from fig.3.4 are identified as $f_{cr1'} = 3.11Hz$, $f_{cr2'} = 18.51Hz$ and $f_{cr3'} = 529.66Hz$. The three corner frequencies for the heat gain can be obtained by refitting $Z_{P_{in}T_{JC}}(s)$ with three foster layers. The corner frequencies of the heat gain transfer function (LPF) are $f_{cr1} = 3.53Hz$, $f_{cr2} = 14.41Hz$ and $f_{cr3} = 419.85Hz$. The frequency response of the heat gain transfer function for this particular module is shown in fig. 3.5.

Similar exercise is carried out for the other power modules under study to obtain heat

Table 3.4: Parameters of the foster thermal network from device datasheet

Foster Network	
Thermal resistance Rf1-4 K/W	Thermal capacitance Cf1-4 J/K
0.0078	0.3107
0.0883	0.6088
0.0231	10.4069
0.001	32.7869

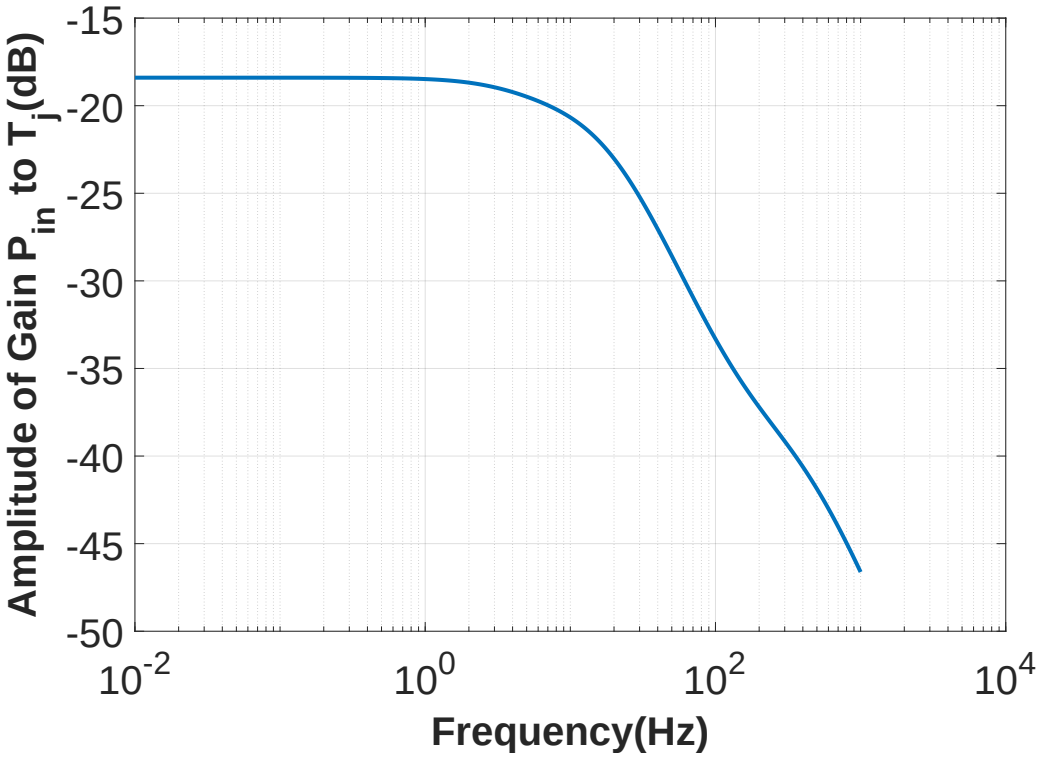


Figure 3.3: Thermal impedance frequency response of SKM400GB07E3 module

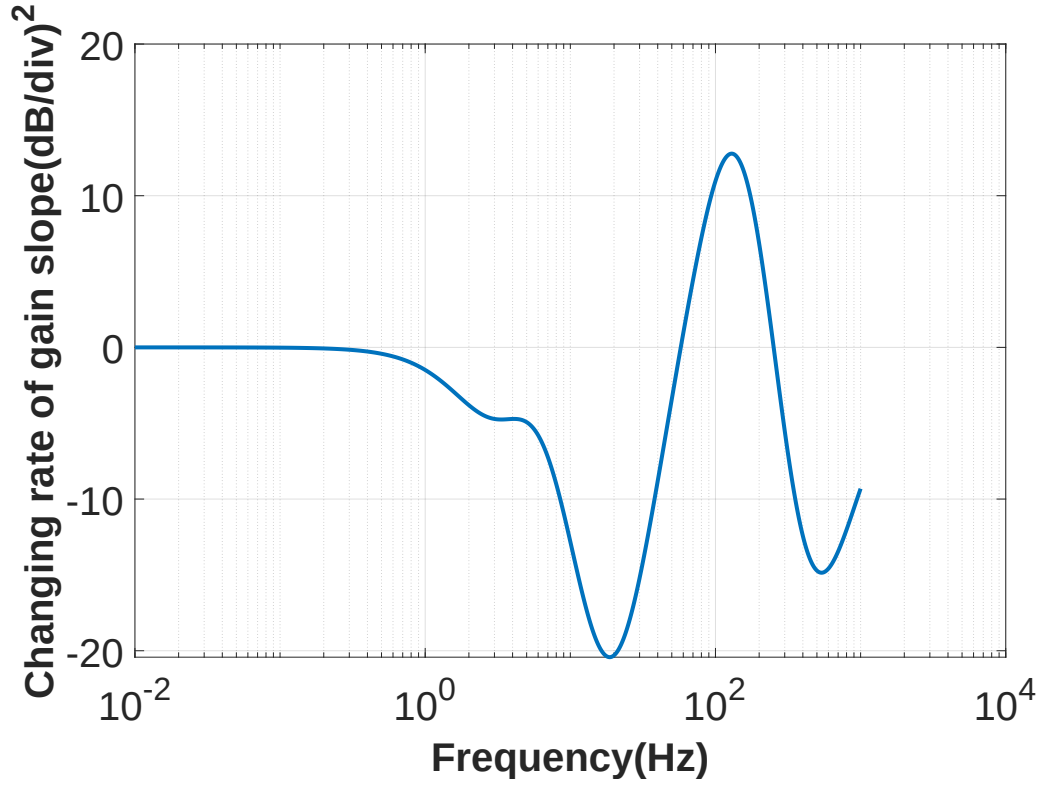


Figure 3.4: Output of deviation operator on Thermal impedance of SKM400GB07E3 module

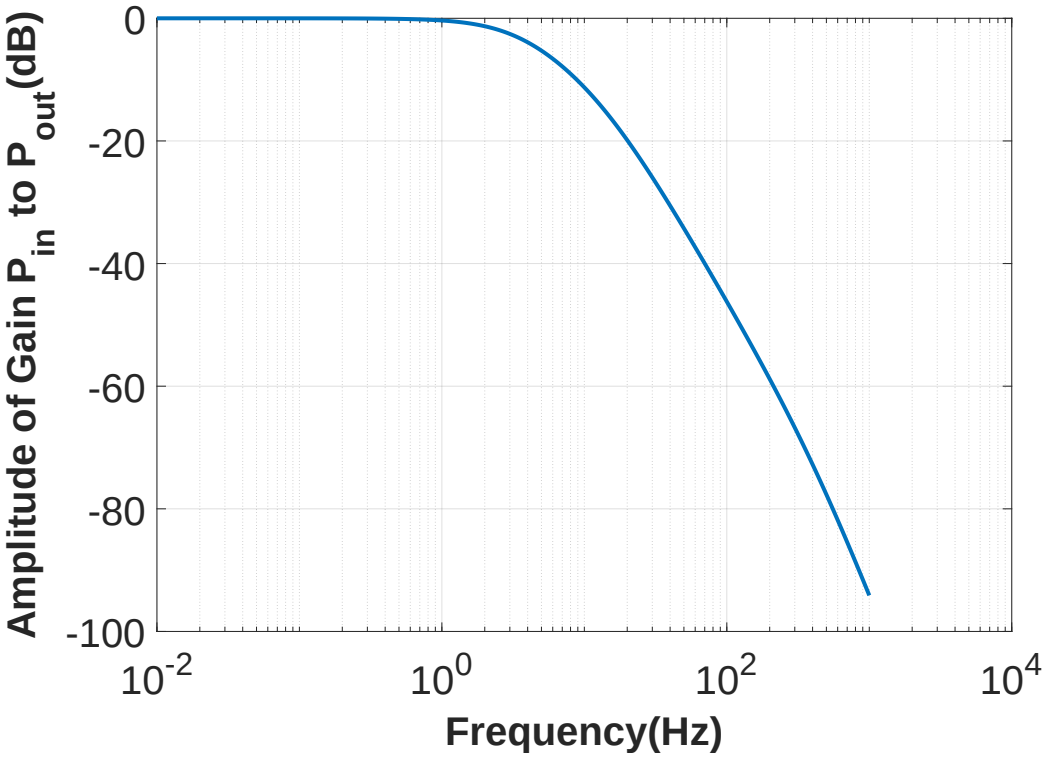


Figure 3.5: Frequency response of heat gain transfer function (LPF) of SKM400GB07E3 module

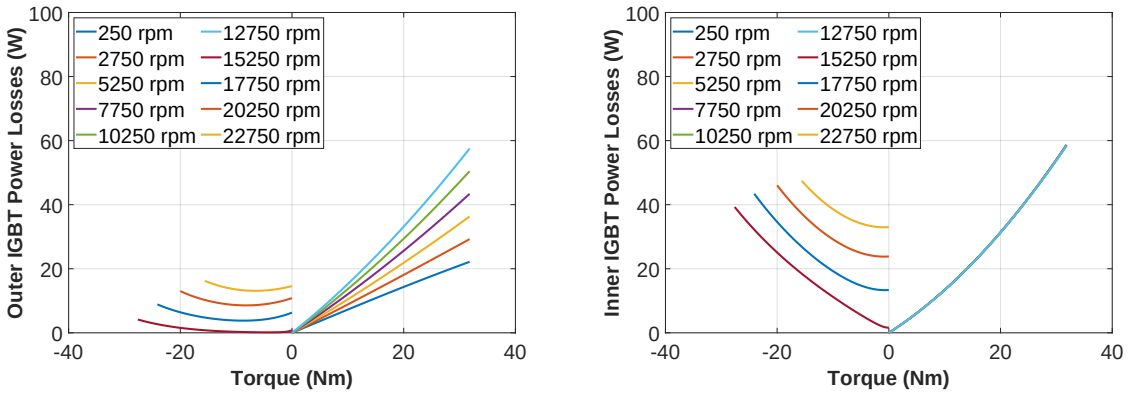
gain transfer function to be utilized in the electro-thermal model.

3.3.3 Modelled thermal data of drive components

The pre-estimated power loss profile for the outer IGBT of the 3L-NPC converter operating at 540V is shown in Fig. 3.6. The loss profiles in generation and motoring mode are different as expected. The current flow switches from IGBTs to diodes during generation mode. The loss profile also shows that the inner IGBTs are subjected to more thermal loading as they carry current even during generation mode. Flux weakening affects the operating range of the drive converter at higher speeds and maximum achievable torque is consequently lower.

In the second step, a specific mission profile is simulated including atmospheric model to account for ambient temperature and altitude profile. The ambient temperature profile/altitude profile during a typical flight for one simulation run is reported in Fig. 3.7.

The average power losses of semiconductors are defined from the 3D lookup table



(a) Outer IGBT loss profile

(b) Inner IGBT loss profile

Figure 3.6: IGBT loss profile at 540V system voltage

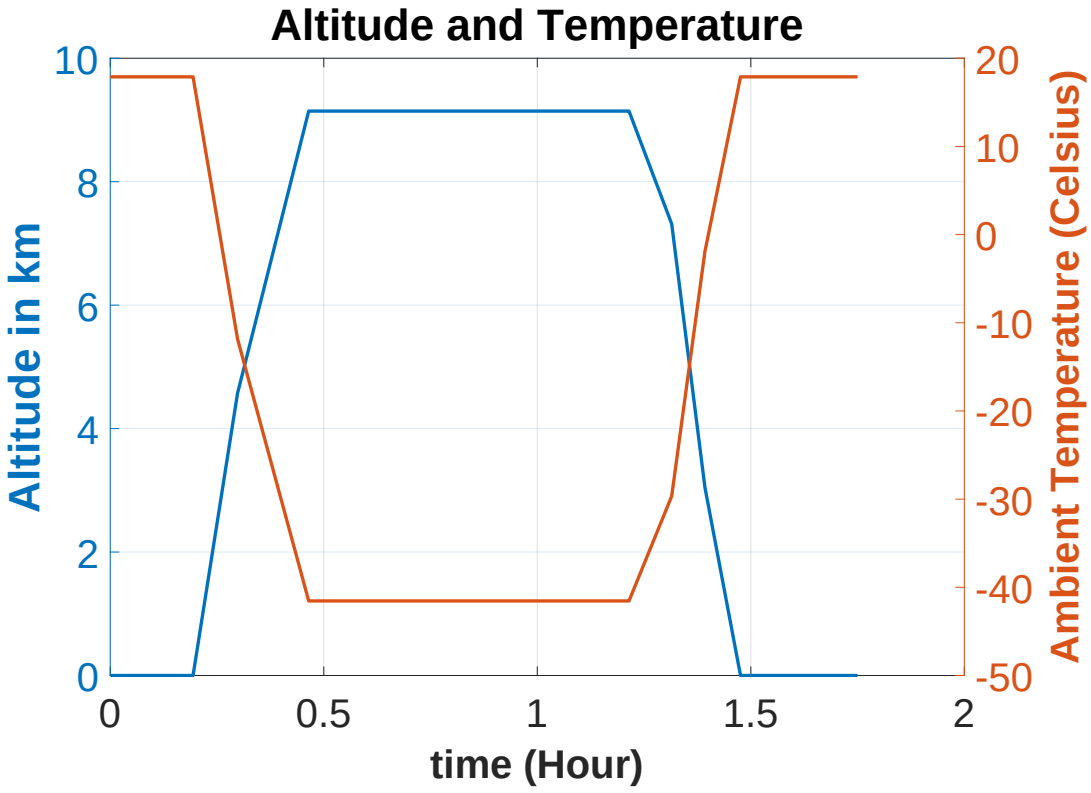


Figure 3.7: Altitude and temperature variation during flight

generated in the first step. Combining the above variables in a modified foster thermal simulation network [6], the medium frequency (duration of minutes to hours) junction temperature profile for semiconductors is obtained. Fundamental frequency thermal cycles are directly looked up from the lookup table as they follow the sinusoidal heating and cooling pattern as shown in [60]. It must be noted that the thermal cycles arising due to fundamental electrical frequency component are not considered for lifetime estimation. The amplitude of thermal cycles due to fundamental electrical frequency is low and furthermore the lifetime models are not valid at thermal cycles of frequency higher than 1-10Hz [27] [63]. Furthermore it is shown in [63] that as the thermal cycle frequency goes higher, the impact on stress buildup is lower. Junction temperature variation due to medium frequency cycles for 2L converters at various system voltages is shown in Fig. 3.8. The effect of speed and power variations in steady state operation can be seen during cruise period. The thermal interface material (TIM) is modelled with a thermal impedance of 0.07 K/W. Heatsink to ambient thermal impedance is modelled with a thermal resistance of 0.1 K/W (0.2 K/W in the case of SiC converter) and the heat capacity of 1 kg of Aluminium (900 J/K).

The rainflow counting results for some of the simulated designs are shown below. The rainflow function from Matlab displays the mean value and the cyclic range of the variable under study - in this case junction temperature. A further output is the duration of the cycle which is also required for the lifetime estimation of semiconductor modules.

It is clear from the rainflow histogram that IGBT design at 810V is operating at thermal limits which would lead to very low operating lifetime. The thermal stress on inner and outer devices in a 3L-NPC converter is different as the inner IGBT is conducting during more time that outer IGBT. The rainflow analysis results for 3L-NPC converter is shown in fig.3.10.

The RMS current through the DC link capacitors is required to estimate the thermal stress applied on capacitors. The DC link capacitor RMS current is evaluated as reported in literature for 2L converter topology [61] and 3L-NPC topology [62]. The necessary variables for rms current calculation is also available in the lookup table. RMS current

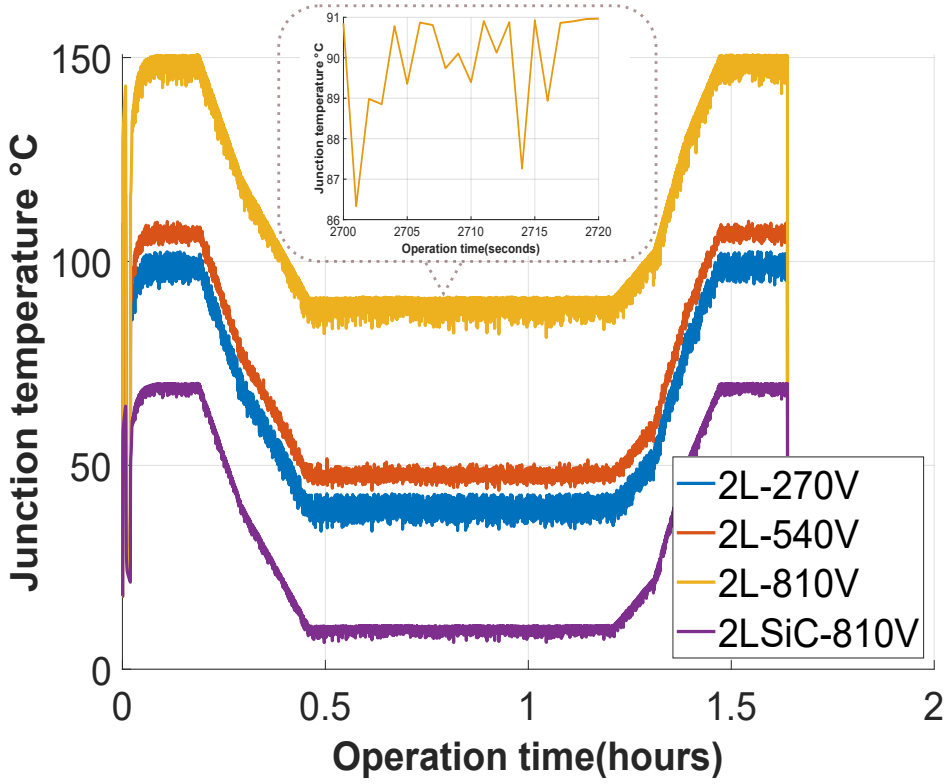
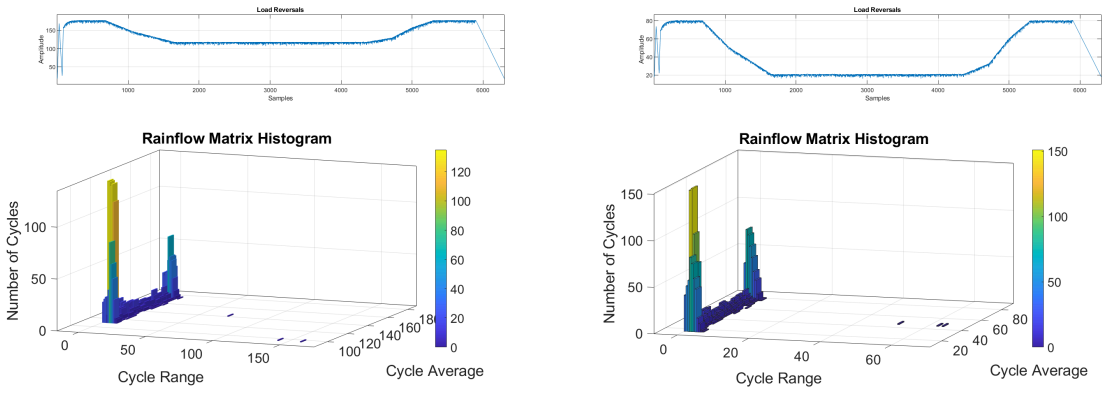


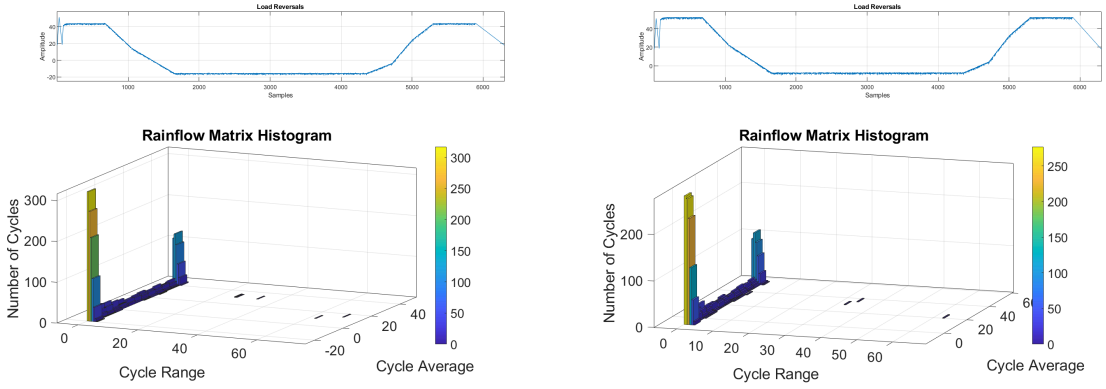
Figure 3.8: IGBT junction temperature variation



(a) 2L IGBT rainflow results

(b) 2L SiC rainflow results

Figure 3.9: Rainflow analysis results of semiconductors in 2L converters at 810V



(a) 3L-NPC outer IGBT rainflow results (b) 3L-NPC inner SiC rainflow results

Figure 3.10: Rainflow analysis results of semiconductors in 3L-NPC converters at 810V

and ESR of capacitor is combined to generate power loss profile of the capacitors. The power losses are translated to a hotspot temperature by a simple thermal resistance model. The capacitor bulk temperature profile of 2L converters are given in Fig. 3.11.

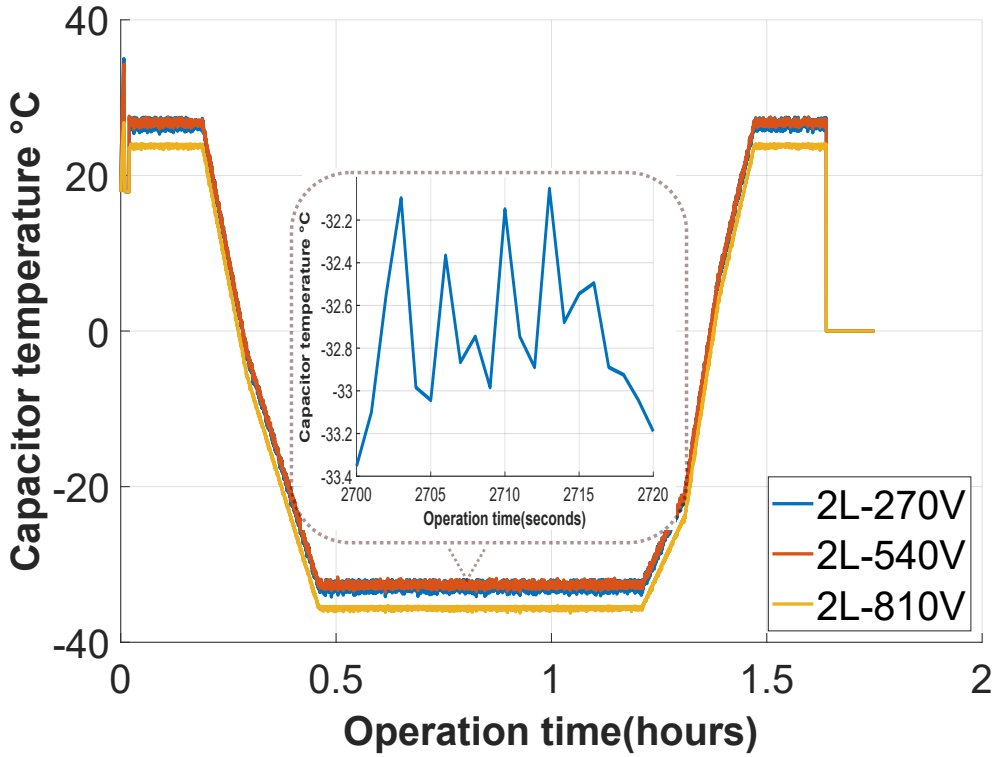


Figure 3.11: Capacitor temperature variation

3.3.4 Experimental validation of power loss estimation

The power losses in a 2L SiC converter prototype are experimentally measured to validate loss estimation. The test setup is depicted in Fig. 3.12.

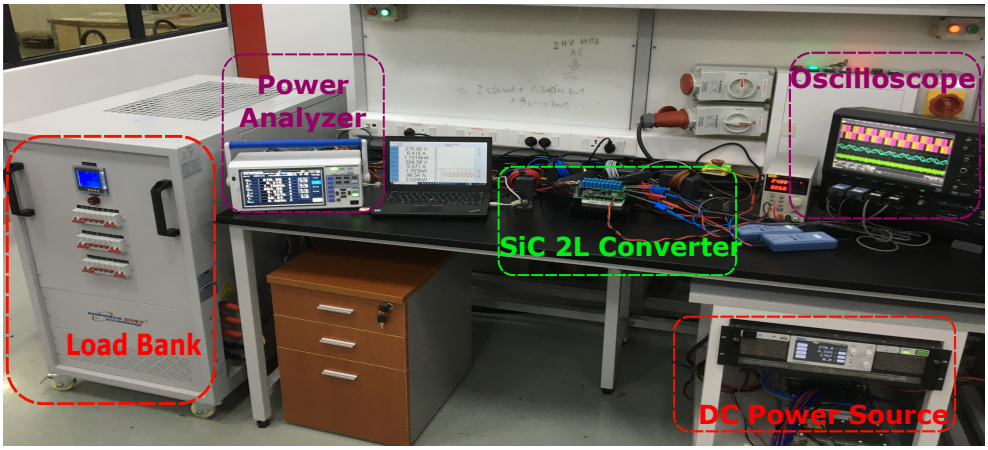


Figure 3.12: Test setup for SiC inverter power loss verification

The setup consists of a DC power source, an RL load with an inductance of 0.5 mH and a variable resistor bank, Hioki PW3390 power analyzer and prototype SiC inverter. CCS050M12CM2 SiC power module from CREE rated at 1.2 kV and 87A is used while the DC link is composed of 20 capacitors from TDK Epcos (B32652A4474J000) rated at 470 nF, 400V. The output fundamental frequency is set to 400 Hz with a DC link voltage of 270V. The output current waveform in two output phases at highest load power is shown in Fig. 3.13.

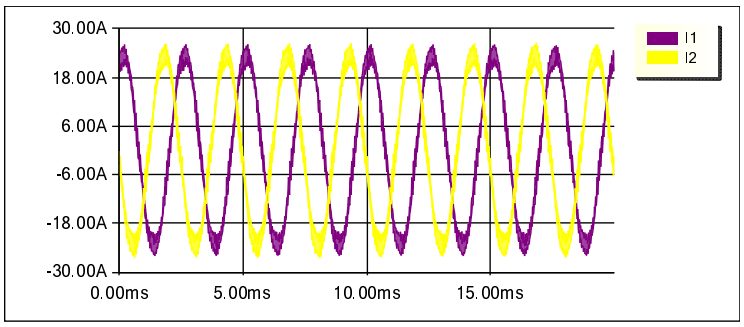


Figure 3.13: Phase A and B current output waveform at highest test load - 270V 19A DC input

The method of loss estimation is essentially differential measurement of input and output power. This method is suitable when the efficiency is less than 98%. When the converter efficiency is higher than 99%, calorimetric measurement method is required to

achieve acceptable errors in loss measurement. In the test frequency range, the power meter has an error margin of 0.1% maximum scale. The voltage and current measurements range for input and output power are set as 300V and 20A respectively. Hence, the errors in both power and loss measurements are 6W (0.1% of 6000W) and 12W respectively.

The measured and estimated power losses of the SiC inverter are plotted in Fig. 3.14. Datasheet values for typical power module was used for loss estimation which introduces an error considering the particular module under test. It is not practical to characterise each device especially mass produced commercial modules. Hence the error observed in power loss validation is considered acceptable as it is the industry norm. However, a further analysis is performed to bring out the dominance of cosmic ray failures on system reliability of aerospace converters even if wear out failures are under estimated due to statistical variation of device parameters. In Section 3.4, the reliability estimates are recalculated with 20% higher losses, in order to account for potential errors in power losses modelling and how these affect the system reliability predictions (i.e. sensitivity evaluation).

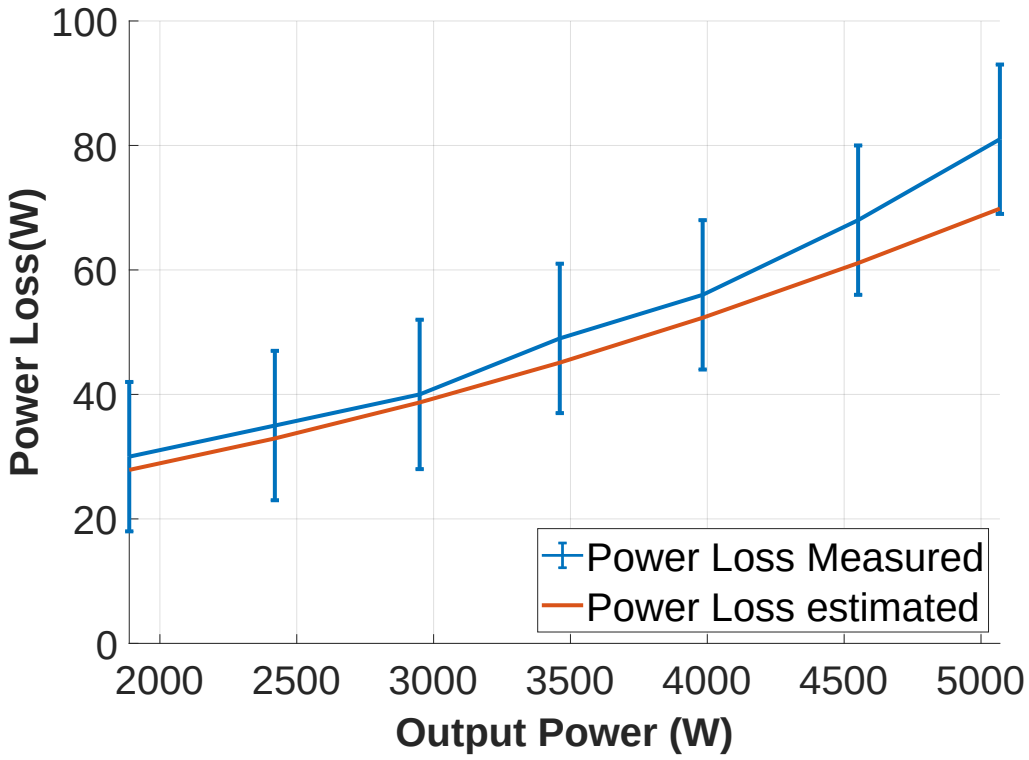


Figure 3.14: Power loss estimation versus measured loss

3.4 Wear-out failure lifetime estimation

The stress profiles evaluated in subsection 3.3 are applied to lifetime models introduced in section 2.2 to obtain lifetime estimates for both semiconductors and capacitors. In the case of semiconductors, a rainflow cycle counting algorithm is employed to generate thermal cycle data as shown in Fig. 2.3.

Bayerer model specifies the range of t_{on} parameter as 1 to 15 seconds. Infineon published an extension method, [63], as summarized in (3.5).

$$\frac{N_{cyc}(t_{on})}{N_{cyc}(1.5s)} = \left(\frac{t_{on}}{1.5s}\right)^{-0.3}, 0.1s < t_{on} < 60s \tag{3.5}$$

In order to account for the thermal cycling time, t_{on}, appropriately in IGBT lifetime model (2.1), the thermal cycles are separated into three different time scales - sub second cycles (below 0.1s) are classified as drive fundamental frequency cycles, thermal cycles of duration 0.1s to 60 s are classified as fast thermal cycles and above 60 seconds are classified as slow cycles. The Bayerer model with the extension proposed by Infineon is only valid in the fast thermal cycles range. Thermal cycles and their origins are classified in Fig. 3.15. The thermal cycle classification separates the sources of the various stresses based on their origins. Sub-second level cycles are caused by operation of the power converter. The amplitude of such cycles is dependent on the load levels. The medium frequency scale variation which are in the seconds to minutes range is caused by mechanical or electrical load variations. The longer duration cycles are caused by slow variations in the environmental conditions and due to operating point variations over time.

The fundamental frequency component cycles are below the lower bound of the lifetime model validity. The contribution from those thermal cycles are very low as the power modules are sized to handle those fluctuations. The lifetime model predicts the same, even though caution must be exercised as it is outside the validity range. The slow thermal cycles pose a different challenge. They are smaller in number but cause the most amount of damage. The lifetime model cannot simply be extended as shown by

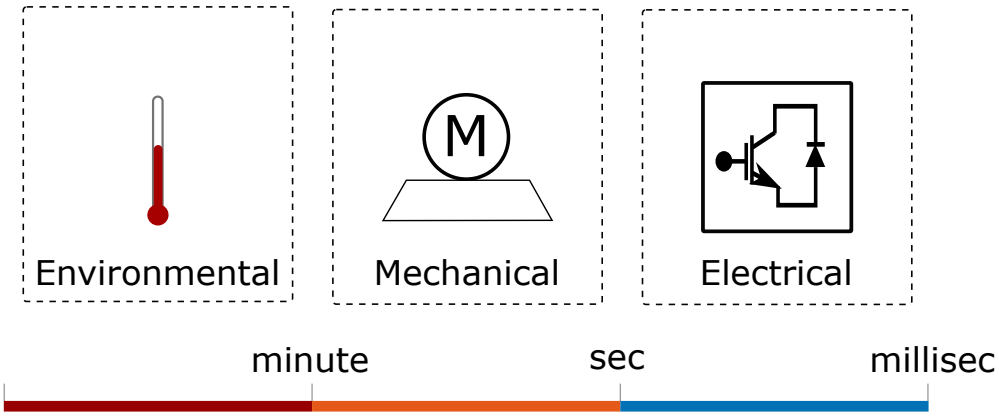


Figure 3.15: Junction thermal cycle classification of power modules

ABB in [64]. In a prior work on wind converter reliability assessment, the ABB HiPak lifetime data was directly applied to quantify lifetime consumption due to long thermal cycles [23]. A closely related but different approach is adopted in this work.

The coefficient term of t_{on} in (2.1), β_3 is estimated using the lifetime figures published in [64]. The estimated coefficient termed $\beta_3(slow)$ is utilized to account for thermal stress due to long thermal cycles.

Lifetime estimates of semiconductors and capacitors without accounting for statistical variations for the 7 cases are listed in Table 3.5. Sub-zero ambient temperature at aircraft cruising altitudes coupled with reduced voltage stress, result in very high predicted lifetime for capacitors. The lifetime model for capacitors is saturated to a constant failure rate model when capacitor hotspot temperature is below 25 °C as recommended in IEC 61709. The high predicted lifetime of capacitors indicate that thermal stress is not a lifetime consuming factor for capacitors under this mission profile. As listed in [65], further to applied voltage and hot-spot temperature, humidity is another stressor consuming lifetime of MPPF. Lifetime model utilized accounts for voltage and temperature induced stresses, humidity related failure modes could dominate in this particular case. Humidity induced lifetime consumption has been not considered in this work due to the following reasons - assumed hermetic sealing of capacitors, and low humidity conditions inside fuselage. It can be concluded that capacitors would not be the reliability bottleneck for aviation power electronic converters.

BVR is also included to show switch blocking capability utilization which would be

utilized for cosmic ray failure rate estimation.

Table 3.5: Predicted lifetime values

DC Link Voltage	2L			3L			
	S1	Capacitor	BVR	S1	S2	Capacitor	BVR
270V	17.5 years	2461 years	0.46	56 years	38 years	6666 years	0.23
540V	9.8 years	1892 years	0.5	230 years	196 years	1284 years	0.46
810V	2.8 years	1533 years	0.74	309 years	304 years	1559 years	0.69
810V(SiC)*	96.9 years	1533 years	0.74	-	-	-	-
810V(SiC)**	71.8 years	1533 years	0.74	-	-	-	-

* Lifetime parameters in [5] utilized

** SiC Lifetime parameters extracted from [28] utilized

The revised lifetime estimates of semiconductors and capacitors accounting for 20% higher power losses are listed in Table 3.6. Comparing the lifetime predictions of Tables 3.5 and 3.6, the very strong impact on lifetime prediction due to loss estimation error is evident. In practical reliability estimates, such statistical parameter deviations are accounted for by a Monte Carlo simulation to estimate system reliability over the population of such systems.

Table 3.6: Lifetime estimates with 20% higher losses

DC Link Voltage	2L		3L		
	S1	Capacitor	S1	S2	Capacitor
270V	8 years	2443 years	31 years	16 years	6310 years
540V	4.5 years	1876 years	170 years	136 years	922 years
810V	1.3 years	1533 years	231 years	230 years	1432 years
810V(SiC)*	60 years	1533 years	-	-	-
810V(SiC)**	42.8 years	1533 years	-	-	-

3.5 Cosmic ray failure rate estimation

Experimental results in [37] highlight that Si IGBTs suffer from cosmic ray failures above 60% BVR, while the impact on SiC devices is negligible below 80% BVR. Cosmic ray failures are strongly dependent on switch voltage rating and device construction. The above observations are valid for switch voltage ratings up to 1200V. The values could

also be confirmed from the guide on cosmic ray failures from Semikron [33]. From Table 3.5, it is concluded that cosmic ray failure is only of concern for 2L and 3L-NPC Si IGBT based converters operating at 810V. Cosmic ray failure rate is tabulated and listed in Table 3.7 based on experimental Failure In Time (FIT) rates (number of failures per 1 billion hours) at estimated BVR of devices from [37] scaled to account for increased neutron flux intensity at altitude. Neutron flux intensity at 30,000 ft is 130 times higher than at reference conditions [35].

Table 3.7: Cosmic ray failure rate per switch

	2L	3L
BVR	0.74	0.69
FIT rate/cm^2 (Reference)	200	0.1
FIT rate/cm^2 (Cruising)	26000	13
Die area (cm^2)	1.42	0.76
FIT rate Switch	36920	9.9

FIT rates listed in Table 3.7 are valid for a semiconductor during blocking mode. The blocking duration for the converter topologies are derived from the sinusoidal modulation pattern. It would be different based on other modulation patterns.

In the case of a 2L converter, gated on period of top switch in positive and negative half cycle of a fundamental electrical period can be shown as in Eq.(3.6).

$$\begin{aligned} S1Cond_{pos-halfcycle} =& \frac{Vm}{V_{dc}} \sum_{n=0}^{\frac{F_s}{2\cdot f}-1} sin(\omega n \cdot T_s) \\ S1Cond_{neg-halfcycle} =& \frac{1}{2\cdot f} - \frac{Vm}{V_{dc}} \sum_{n=0}^{\frac{F_s}{2\cdot f}-1} sin(\omega n \cdot T_s) \\ =& \frac{1}{2\cdot f} - S1Cond_{pos-halfcycle} \end{aligned} \tag{3.6}$$

where T_s is the switching period, F_s is the switching frequency, f is the fundamental electrical frequency, ω is the electrical angular frequency, V_{dc} is the dc link voltage and

V_m is the fundamental output voltage magnitude.

The total conduction as well as blocking duration of a switch in a 2L converter over a cycle can be easily seen to be 50% of the time from Eq.(3.6).

In the case of 3L-NPC, the gated-on time duration for the outer and inner switches on upper phase A is as follows.

$$\begin{aligned} S1outerCond_{cycle} =& \frac{Vm}{V_{dc}} \sum_{n=0}^{\frac{F_s}{2\cdot f}-1} sin(\omega n \cdot T_s) \\ S1innerCond_{cycle} =& 1 - \frac{Vm}{V_{dc}} \sum_{n=0}^{\frac{F_s}{2\cdot f}-1} sin(\omega n \cdot T_s) \\ =& 1 - S1outerCond_{cycle} \end{aligned} \tag{3.7}$$

Taking the limit on Eq.(3.7) such that $\frac{F_s}{f} >> 10$, the summation can be replaced by an integral as shown.

$$\begin{aligned} S1outerCond_{cycle} =& \frac{Vm}{V_{dc}} \int_0^{\frac{T}{2}} sin(\omega t) dt \\ =& \frac{Vm}{V_{dc}} \frac{1}{\pi f} \\ S1innerCond_{cycle} =& 1 - S1outerCond_{cycle} \end{aligned} \tag{3.8}$$

where T is the fundamental electrical period.

Taking the limit of $\frac{Vm}{V_{dc}} = 1$, we obtain that the minimum blocking duration of the 3L-NPC switches as

$$\begin{aligned} S1outerBlock_{cycle} =& 1 - S1outerCond_{cycle} \\ =& 1 - \frac{1}{\pi} \\ =& 68.17\% \\ S1innerBlock_{cycle} =& 31.83\% \end{aligned} \tag{3.9}$$

Accounting for modulation limits in the 3L-NPC converter case, the following scaling factors corresponding to percentage of time spent in blocking mode are applied for the switches in this study.

- 50% for the devices in 2L converter;
- 75% for the outer switches in 3L-NPC;
- 25% for the inner switches in 3L-NPC.

The FIT rate is essentially a contant failure rate value corresponding to an exponential failure probability function. The probability density function (pdf) of exponential failure model is expressed in Eq.(3.10).

$$f(t) = \lambda exp^{-\lambda t} \tag{3.10}$$

The above pdf can be converted to reliability function and hazard functions from standard definitions as:

$$\begin{aligned} R(t) &= 1 - F(t) = 1 - int_0^t f(t)dt \\ &= exp^{-\lambda t} \\ H(t) &= \frac{f(t)}{R(t)} = \lambda \end{aligned} \tag{3.11}$$

Approximating the time at cruising altitude to be 1 hour for every flight, cumulative failure rate, $F(t)$ caused by cosmic rays is:

- 2L converter - 24.3% / year;
- 3L-NPC converter - 0.0013% / year.

Hence at 810V, designing with 1200V devices for a 2L converter is simply not an option for aerospace converters. The failure rate of 3L-NPC converter due to cosmic ray failures, albeit smaller than that of 2L converter, is still significant for the overall converter reliability, as discussed in section 3.6.

3.6 Reliability results and Discussion

Estimated lifetimes in section 3.4 do not account for statistical parameter variations of the converter components. In order to obtain time dependent reliability of converter system, a Monte Carlo simulation is carried out. The resultant reliability in time figures of individual components are combined together using reliability block diagram method to predict the converter reliability at system level.

3.6.1 Monte Carlo Simulation for wear-out failures

The Monte Carlo methodology applied in this work for semiconductors is described in [44] and for capacitors, is described in [66]. A virtual thermal swing, which would result in an equivalent amount of damage caused by the mission profile, is derived for semiconductors. This approach needs to be expanded if thermal heating time, i.e. ton, is also accounted for in lifetime model [67]. In the case of capacitors, a virtual hot spot temperature is estimated which corresponds to total damage imposed by mission profile. This is an established procedure based on reliability physics [68].

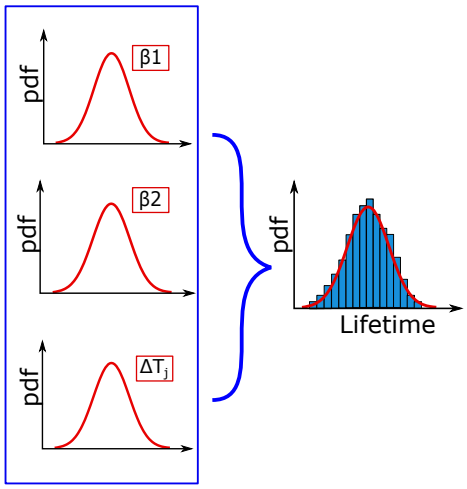
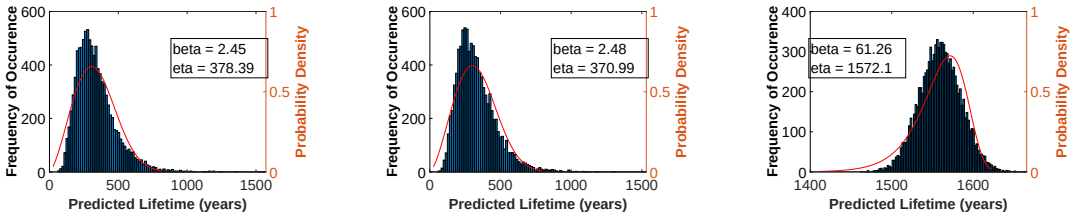


Figure 3.16: Monte Carlo analysis with variation in lifetime parameters and thermal simulation results of IGBT

Once virtual effective stress values are determined, a Monte Carlo simulation is carried out assuming a 5% variation in all parameters of lifetime model as well as effective stress value [25]. A graphical overview of the Monte Carlo process highlighting the variation of parameters in the lifetime model is given in Fig. 3.16.



(a) Outer IGBT (b) Inner IGBT (c) Capacitor

Figure 3.17: Monte Carlo simulation results for 3L-NPC converter at 810V

In the case of capacitors, only the lifetime value reported at nominal conditions is varied as failure model saturates to a constant failure mode due to low hotspot temperature. Monte Carlo simulation results showing wear-out failure reliability of sub components of 3L-NPC converter with DC link voltage of 810V is provided in Fig. 3.17.

3.6.2 Reliability block diagram method

The reliability figures derived in subsections 3.5 and 3.6.1 are combined using the RBD method to estimate overall converter reliability. As no redundancy is factored in the converter design, the failure of a single component leads to complete system failure. The above assumption is held valid to develop RBD for all 7 cases. A reference RBD is illustrated in Fig. 3.18.

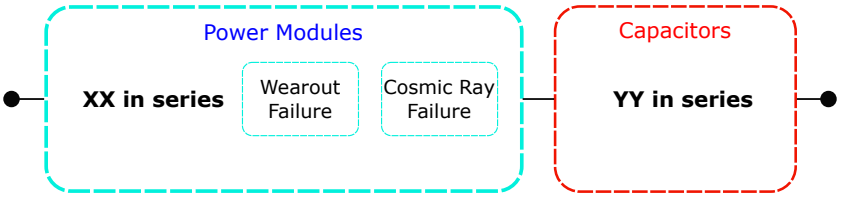


Figure 3.18: Reliability block diagram

Reliability figures from case study

The RBD based converter reliability for all cases is provided in Fig. 3.19.

The following conclusions could be drawn:

- At low system voltages (up to 270V), Si based 2L and 3L-NPC have similar reliability, with 2L providing higher reliability;
- Above 540V, 3L-NPC is able to achieve higher system reliability;

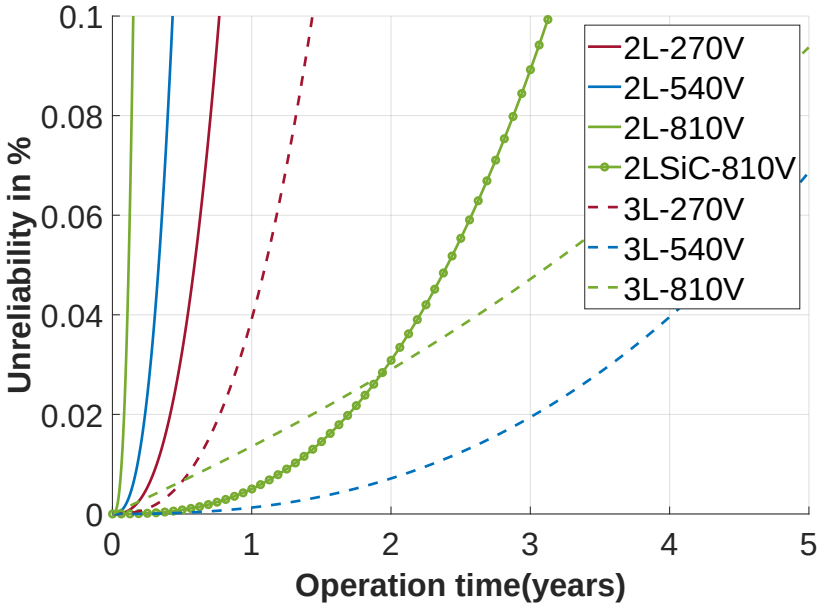


Figure 3.19: Reliability comparison of case study

- Above 810V, 2L Si is not an option due to the very low system reliability. 2L SiC outperforms 3L-NPC in terms of reliability albeit only in the initial years of operation. The wear-out reliability of SiC converters are easier to improve by paralleling modules as they are inherently more robust against cosmic ray failures.

The impact of power loss estimation errors on component lifetimes was presented in Table 3.6. In Fig. 3.20, the reliability of the 3L-NPC topology at the modelled system voltages is plotted along with estimated reliability considering 20% higher power losses. Considering 270V and 540V, the overall reliability is lower at higher power losses as expected. At those system voltages, the dominant failure mode is wear-out failure as BVR for switches is sufficiently low. An obvious choice to improve converter reliability at those voltage levels is higher current derating of sub-components.

In order to explain the lower reliability performance of 3L-NPC converter at 810V, system unreliability along with contribution from various failure modes to unreliability are plotted in Fig. 3.21 to identify the reliability bottleneck. Cosmic ray failure rate is assumed to be unchanged due to loss variation by ignoring the impact of junction temperature. System unreliability contribution due to wear-out of semiconductors and capacitors show a strong dependency to modelled losses. Inspite of that, overall system

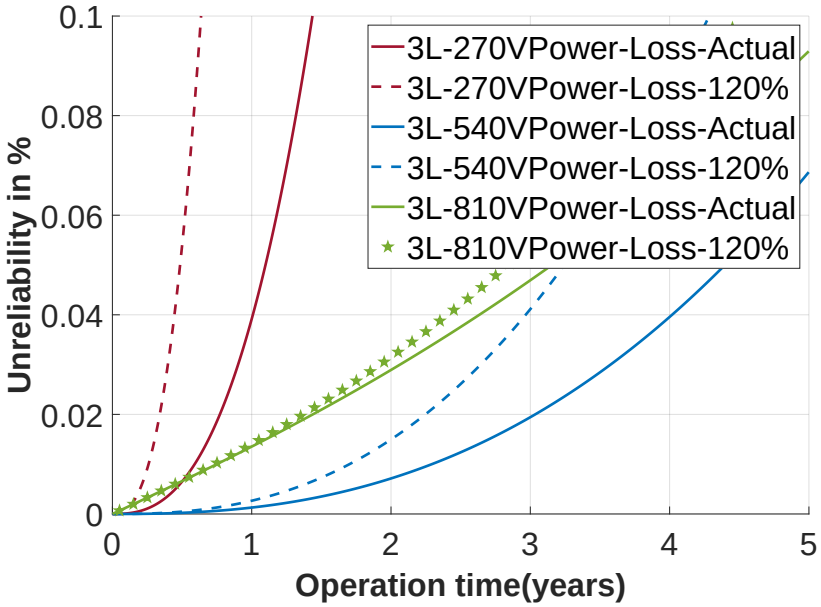


Figure 3.20: Reliability comparison of 3L-NPC topology with power loss variation

unreliability is unchanged as cosmic ray failures are the dominant failure mechanism.

Table 3.8: Device/topology selection guide considering reliability

	2L	3L-NPC	2L-SiC
270V	✓	✓	-
540V	✓	✓✓	-
810V	✗✗	✓	✓✓

This result highlights the necessity for fault tolerance of high voltage converters based on Si IGBTs as dominant failure mode switches to cosmic ray failures (contant failure rate) instead of wear-out failures. Designers of future kV class aerospace power converters, must factor in tolerance against cosmic ray failure (sufficient voltage derating) along with fault tolerance as key design requirements. Designs with Si IGBTs for high voltage converters should derate the semiconductors for current as well as voltage to mitigate against wear-out failures and cosmic ray failures. Selection of higher current rated devices of same voltage rating would enhance wear-out failure performance at the expense of higher cosmic ray failure rate due to larger device surface area. A summary is provided in Table. 3.8 to assist system designer in making appropriate choices for devices/topologies at various voltage levels.

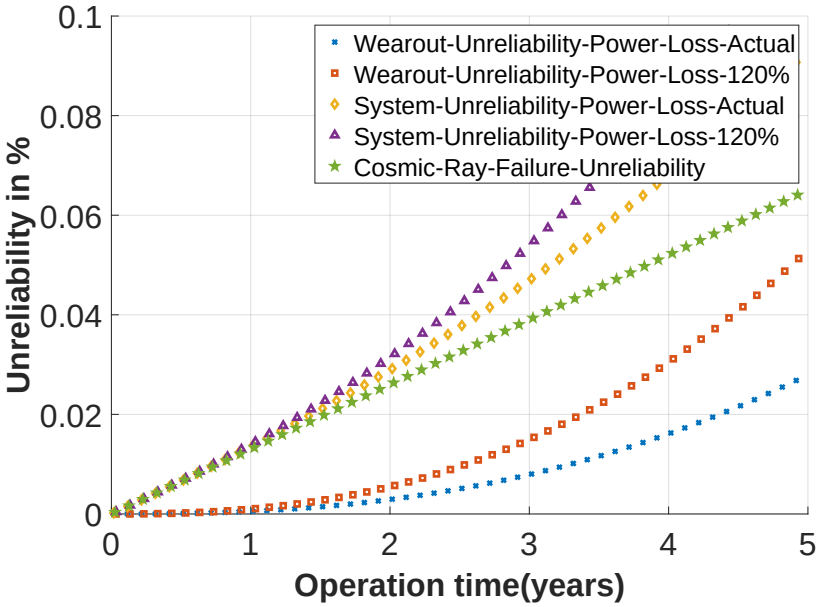


Figure 3.21: Reliability sub-components of 3L-NPC @ 810V

3.7 Summary

Extending the existing lifetime models to aerospace conditions, aerospace drive converter reliability for a steady power output system has been presented. It has been demonstrated that aerospace mission profile lies outside the validity range of widely accepted lifetime models of power electronic components - especially in the case of film capacitors and SiC modules. New research is necessary to identify lifetime models valid in aerospace conditions. Simulated stress profiles indicate that at higher voltage levels, major failure mode for power electronics shifts from wear-out to cosmic ray induced random failures, mandating the adoption of multilevel topologies. At higher voltage levels the reliability limit is dictated by cosmic ray failure. Hence the reduced die area, wide bandgap and consequent higher tolerance to cosmic ray failures of SiC devices make them ideal candidate for power converters operated at altitude.

Chapter 4

Investigation of cosmic ray failure mode

Abstract - Power system voltage on aerospace platforms is on a steady upward trend. High voltage power converters suffer from SEB failure caused by CR. The impact of CR on failure rate is shown in chapter 3. The established standards propose voltage de-rating of power modules as a mitigation measure. In this chapter, in-situ mitigation measures - thermal control and dynamic voltage control, against CR induced failures are studied. It can be concluded that dynamic voltage control is the preferred mitigation approach.

4.1 Introduction

The most important components of CR in the atmosphere of the Earth are Galactic Cosmic Rays (GCRs) and Solar Energetic Particles (SEPs). The GCR are low-intensity fluxes of high-energy particles coming from the interstellar medium. 98% of GCR are fully ionized atoms of different elements, mostly hydrogen (89%) and helium (12%). The GCR intensity varies inversely with solar activity. The SEPs are high-intensity fluxes of particles (mainly protons) accelerated during sporadic solar flares, which are more probable during solar maximum.

The importance of cosmic ray failures is considered critical for high-reliability systems on the ground - semiconductor wafer processing machines being one [69]. The operat-

ing conditions are harsher and need for reliability is stricter for aerospace applications. International Electrotechnical Commission (IEC) standard [29] specifies the calculation method to estimate cosmic ray induced failure in airborne systems. The IEC standard provides a scaling factor dependent on the altitude.

Failure rates during solar events were highlighted as a concern in literature and mitigation measures such as voltage reduction [70] have been proposed. Thermal control approaches have been proposed in literature to minimize thermal ageing of power components [71], [72].A typical design aim of thermal control for reliability management is to minimize junction temperature cycles of semiconductors or equalize junction temperature of semiconductors and/or capacitors to maximize system lifetime. Due to semiconductor properties CR induced failure rate accelerate, when junction temperature decreases. Hence there is a requirement to control junction temperature of semi-conductors in an optimal range to balance failure rates due to wear-out failure and CR failures. During times of cosmic ray peaks, an active converter thermal management is performed taking into account estimated CR flux at altitude. An experimental setup validates the proposed approach. In discussion section, impact of thermal control on CR failure rate is quantified and compared.

4.1.1 SEB failure rate estimation

Interaction of "Cosmic rays" with earth's atmosphere (mainly nitrogen and oxygen molecules) generates secondary ionizing particles [73]. The most damaging of secondary particles for avionic systems is found to be neutrons [31]. Hess in his pioneering work in 1959 quantified neutron flux profile in atmosphere [74]. Boeing published neutron and other particle flux density and energy spectra variations due to altitude and latitude in [75]. From these prior works, neutron flux is found to increase with altitude and reach its maximum around 60,000 feet (named Pfotzer maximum). CR intensity is also dependent on latitude - with flux intensity almost double near poles compared to intensity at equator.

As CR failure is a complex phenomenon, analytical models are not readily available. Neutron flux, device reverse blocking voltage capability and device physical properties

determine CR failure rate. The relation to neutron flux is linear while relation to blocking voltage and device characteristics is highly non-linear. An analytical expression for cosmic ray failure, given in Eq.(4.1), was proposed by ABB for a particular class of power modules [34]. As reported by ABB, the temperature and altitude dependency is module independent for Si devices while voltage dependency is experimentally curve fitted for particular modules. The temperature dependency of the CR failure rate was found to be an inverse relationship. This phenomenon can be explained due to the increase in mean free path for charge carriers at lower temperatures. The chance of a streamer formation due to cosmic radiation is higher at lower temperatures.

$$\lambda\big(V_{DC}, T_j, h\big) = C_3 \cdot exp\bigg(\frac{C_2}{C_1 - V_{DC}}\bigg) \cdot exp\bigg(\frac{25 - T_j}{47.6}\bigg) \cdot exp\bigg(\frac{1 - \big(1 - \frac{h}{44300}\big)^{5.26}}{0.143}\bigg) \quad (4.1)$$

The coefficients in Eq.4.1 are summarized below:

- C_1, C_2 and C_3 account for device specific characteristics and blocking voltage. These parameters have no physical meaning as they are derived by curve fitting. The unit of V_{DC} is in volts. The equation is only valid for V_{DC} greater than C_1. The failure rate is regarded as zero otherwise.
- T_j is the junction temperature in degree celsius.
- h is the height in meters above sea level.

The effect of temperature and height on failure rate are independent of device type.

4.2 Motivation for thermal controller

The CR failure rate in chapter 3 is derived at a reference junction temperature of 25 °C. The temperature dependence from (4.1) shows that the cosmic ray failure rate at a junction temperature of 70°C reduces by 39%, while the failure rate increases by 209% when junction temperature is -10°C. Considering ambient temperature reduces with altitude, temperature dependence must also be accounted for in reliability estimations.

4.2.1 Thermal control in power electronics

Thermal controllers have been implemented for improving relaiblity of power converters. The main concern of reserach in state of the art thermal controllers is managing wearout failure mode. The key motivation is to reduce or balance the ageing of the converters in a paralleled system or distribute the stresses between components within a converter. The goals of such optimization are varied - increase lifetime, minimizing maintenance visits by equalizing wearout [71], reduce total cost of ownership or assure increased operation for maximum energy extraction [76]. Equalizing Remaining Useful Lifetime (RUL) across various components of a converter system would be beneficial for multi level converters with similar building blocks or paralleled converter systems. A schematic overview of applying Active Thermal Control (ATC) and Voltage Ripple Reduction (VRR) along with condition monitoring and power routing to achieve system level reliability goals are showin in 4.1.

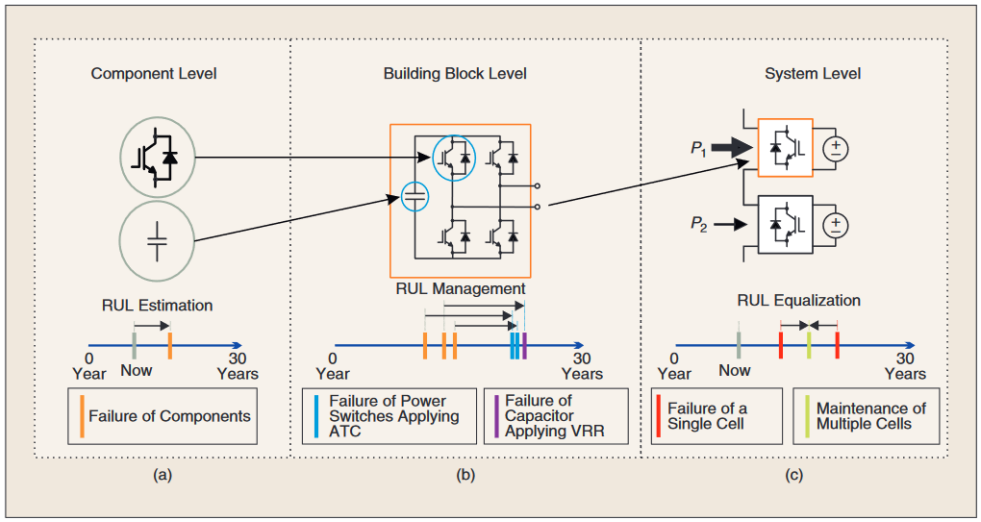


Figure 4.1: System RUL management: (a) condition monitoring, (b) ATC/VRR, and (c) power routing. ATC: active thermal control [8]

In order to implement thermal controllers, accurate measurement or estimation of junction temperature is a pre-requisite. Accurate junction temperature measurement is also useful for RUL estimation and predictive maintenance scheduling. This topic is not further explored in this thesis and reference is provided to related works [77], [78], [79]. Temperature measurement could be augmented with an observer to improve the accuracy.

The various levels at which thermal control can be implemented are outlined in 4.2.

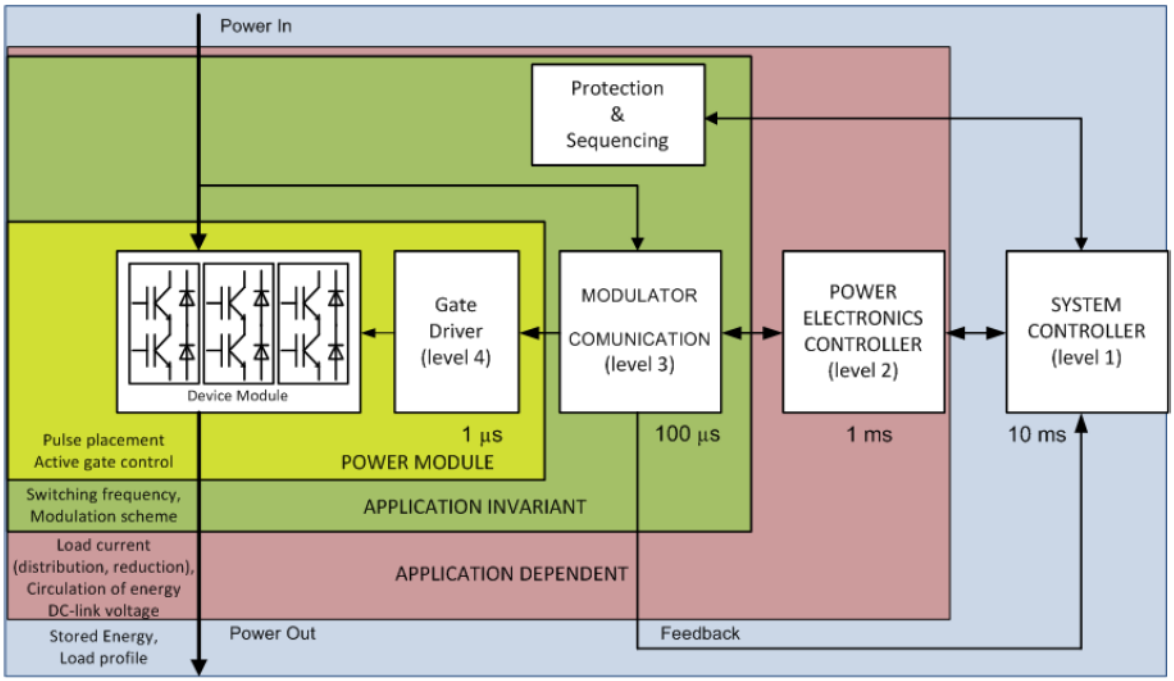


Figure 4.2: Thermal controller options [9]

The levers available can be used depending on the level of complexity and other prerequisites for implementing the scheme as summarized in [9], [72]. A straightforward approach is to adjust the switching frequency as it has a direct effect on the device power losses. The other levers include DC link adjustment, thermally conditioned gate driver which can modulate either the turn on voltage or the gate resistance, thermally modified modulation, system level power routing etc. The above approaches establish a basis for implementing ATC in power electronics.

4.2.2 Thermal controller for aerospace conditions

A thermal controller is proposed with the aim of maintaining junction temperature of semiconductors in an optimum range. There are many handles to vary junction temperature in a switching power converter - switching frequency, cooling system design, device selection etc. Switching frequency variation is utilized in this work. It must be noted that other methods are also feasible.

The thermal controller is implemented as a simple P-controller with saturation for the

maximum and minimum switching frequency values. The temperature set point could be generated in multiple ways - based on measured atmospheric flux at altitude stored in lookup tables being one of the simplest methods. The thermal controller structure is shown in Fig. 4.3. The most critical as well as practically difficult measurement is the junction temperature measurement. Junction temperature measurement is also relevant for wear-out failure logging for predictive maintenance. Most common junction temperature measurement method is using an NTC based thermo-couple mounted on the module DBC and estimating junction temperature using knowledge of the thermal impedance of the module. Many other junction temperature measurement approaches have been reported in literature - fiber-optic based direct measurement and infra-red camera are useful for experimental validation of a one of setup while in-situ measurements are usually based on thermo-couples. Newer in-situ methods are being adopted such as thermal dependent device parameters such as gate resistance variation, on-state voltage based estimation, switching time, gate threshold voltage variation etc. which are summarized in [80].

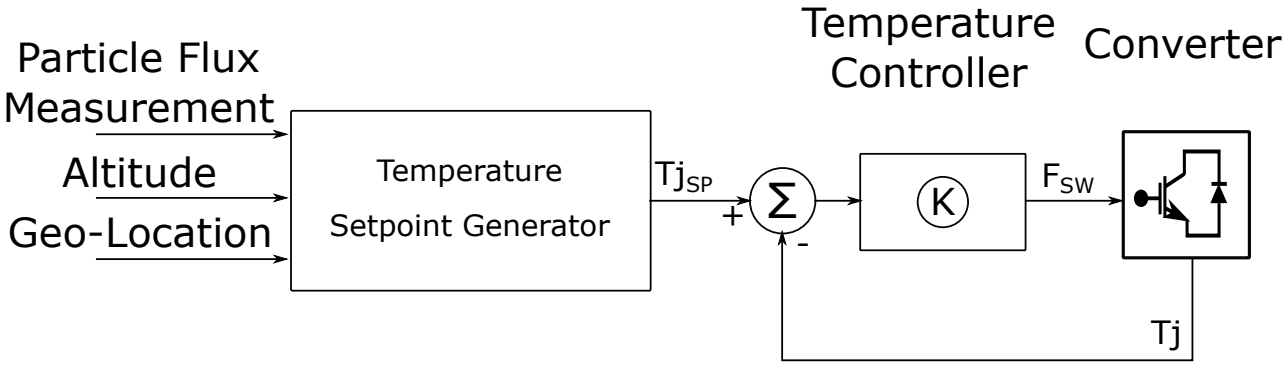


Figure 4.3: Junction temperature controller

The above diagram is one such option available for cosmic ray failure mitigation. It is clarified here that, variation of switching frequency is only proposed as a concept. There are various other means to achieve thermal control such as active gate driving - variation of R_{gate} to influence switching times and hence switching losses or variation of V_{gate} to influence the on resistance and hence conduction losses.

4.2.3 Experimental Verification of thermal control

Performance of thermal controller is experimentally validated using a 2L SiC drive converter. The test setup is shown in Fig. 4.4. The setup includes a DC power source to drive SiC inverter, an RL load with an inducatance of 0.5 mH and a variable resistor bank, Hioki PW3390 power analyzer, oscilloscope and SiC inverter. SiC module used is CCS050M12CM2 from CREE rated at 1.2 kV and 87A and DC link is composed of 20 capacitors from TDK Epcos (B32652A4474J000) rated at 470 nF,400V. The fundamental frequency of AC output is 100 Hz and on chip NTC is used to measure case temperature of the module. The control was implemented on a Texas Instruments Fixed point MCU - TMS320F28027 which can achieve a clock rate of 60MHz (16.67ns) which is sufficient to achieve the required control execution speed.

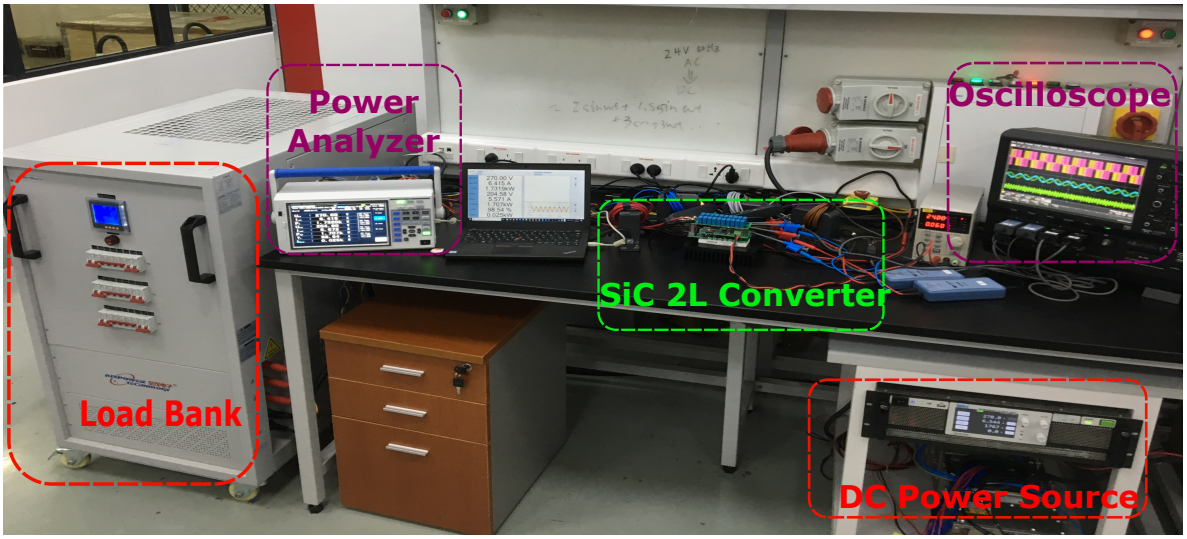


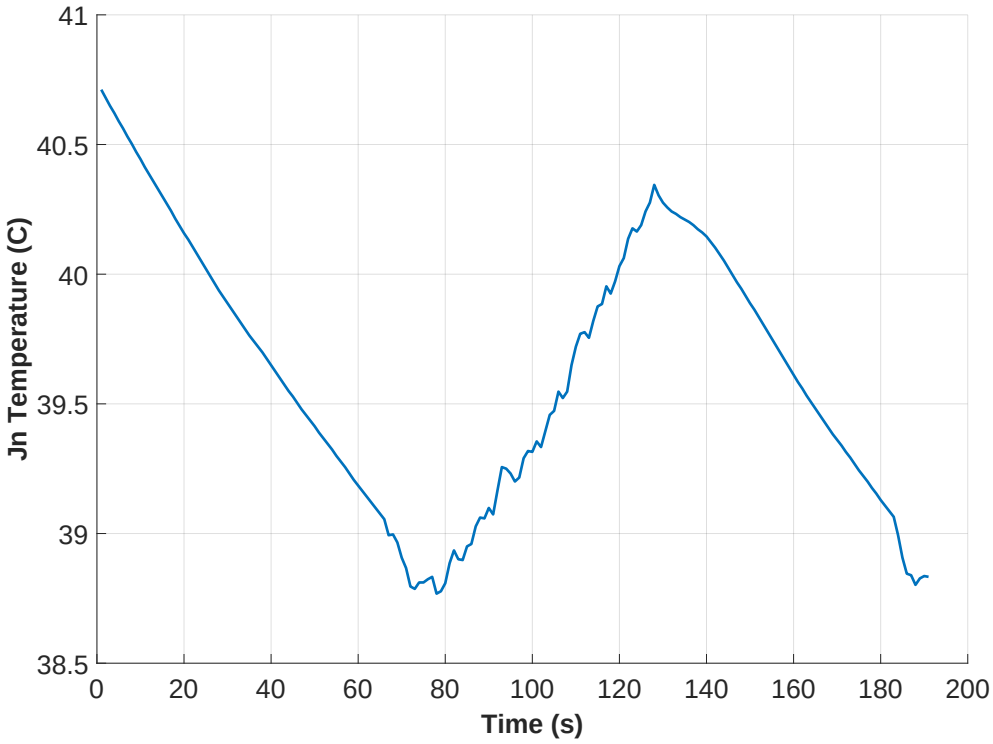
Figure 4.4: Test Setup for thermal controller

The on-chip NTC is characterised to obtain resistance variation relationship with temperature. On-chip ADC samples to provide the temperature of the module which is used in thermal controller.

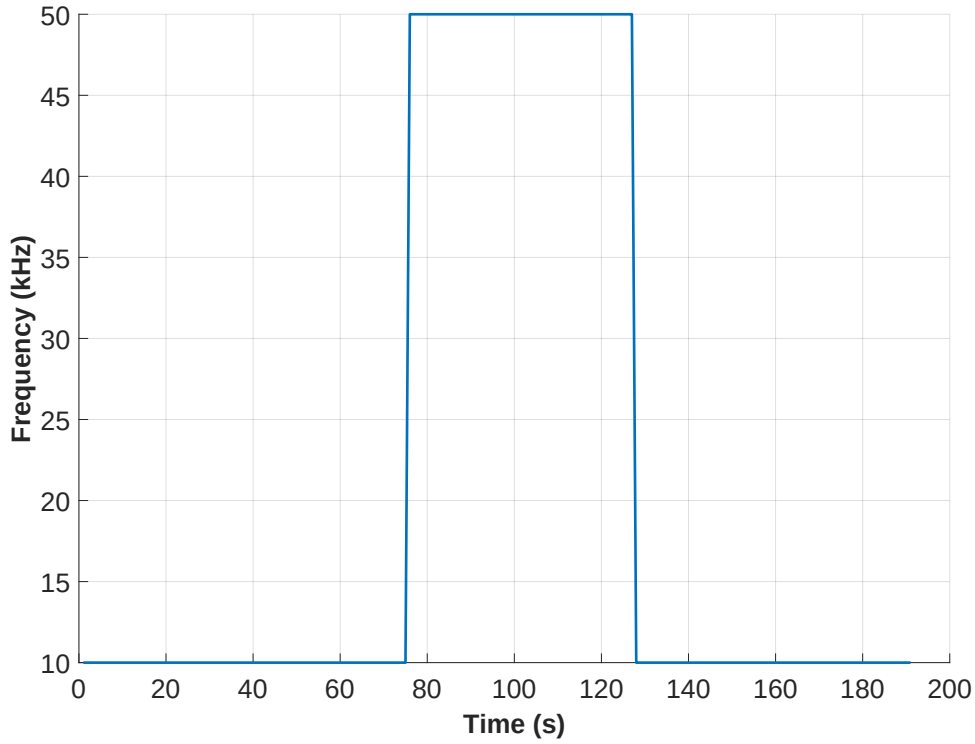
4.2.4 Experimental results

Thermal controller test result is captured in Fig. 4.5a and Fig. 4.5b. The switching frequency is varied by the controller to maintain the module temperature in the control

range. The switching frequency limits are set to 10 kHz and 50 kHz.



(a) SiC Module temperature



(b) Converter switching frequency

Figure 4.5: Thermal controller action

However a more suitable mitigation measure is the voltage modulation approach proposed in [70]. Hence a further study is carried out for an aerospace generator drive system with significant benefits for short duration high neutron flux events.

4.3 Voltage control for cosmic ray mitigation

One of the earliest recommendations from the IEC 62396 standards committee was to derate the power semiconductors for aviation to 50% [81]. Unlike static derating during design phase, dynamic voltage variation was proposed in [70] during high solar activity. In this section, the impact of dynamic voltage variation on system performance is presented.

4.3.1 Starter Generator System

A schematic of a 2L-SiC based starter generator system is shown in Fig. 4.6.

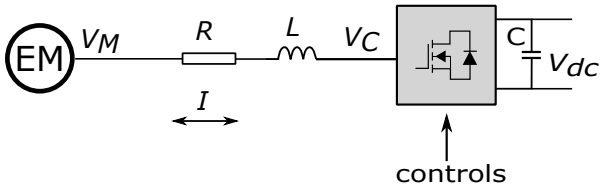


Figure 4.6: Starter Generator Drive Schematic

The nominal parameters of the electrical machine and the drive is summarized in Table. 4.1. Based on the machine parameters, flux weakening is necessary below DC link voltage of 700V to maintain nominal output power.

Table 4.1: Starter generator parameters

Nominal Power	30 kW
Phase and pole numbers	3 phase, 6 poles
Nominal mechanical speed	12000 rpm
Stator resistance	1.1 mΩ
Ld (d-axis inductance)	250 μH
Lq (q-axis inductance)	350 μH
Back EMF constant, Ke	0.1065 V·s/rad

The drive converter parameters are summarized in Table. 4.2.

Table 4.2: Drive parameters

Nominal DC Link, Vdc	840 V
SiC Device	CAB016M12FM3
Device Rating	1200V,78A
Thermal Resistance [Case to Ambient]	0.2 K/W
Ambient Temperature	50 degC
Switching Frequency	40 kHz
DC Link Capacitance	400 μF
Capacitor ESR	5 mΩ

4.3.2 Simulation of Starter Generator System

The system parameters at DC link voltages from 600V to 900V with 30V granularity is simulated to evaluate the impact on drive converter stresses against CR mitigation benefit. The key stresses considered are semiconductor losses and capacitor losses. SiC mosfets are bidirectional devices and hence diode losses are not considered. The switching losses are calculated by scaling the reference turn-on and turn-off loss figures from datasheet with the simulated turn-on and turn-off currents during a fundamental electrical cycle.

In order to bring out the relative variation of losses, thermal stresses and cosmic ray failure rate, normalized plots are provided in the simulated dc link voltage range. The nominal values at reference dclink voltage of 840V is provided in Table. 4.3.

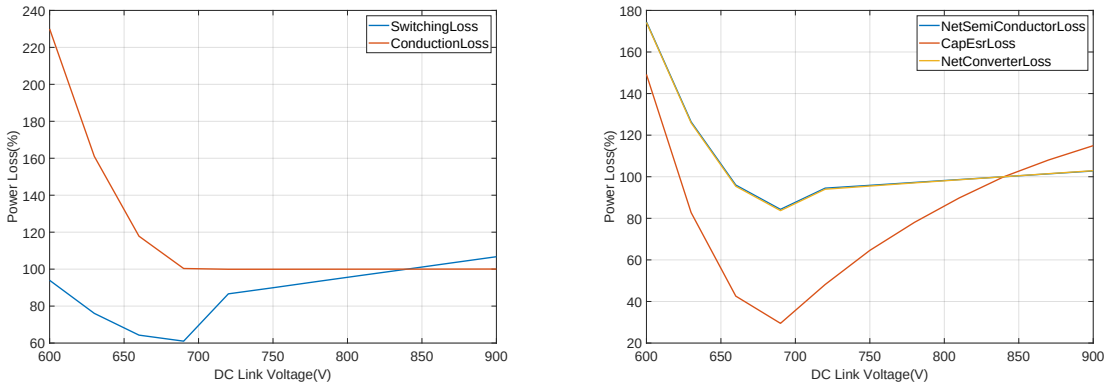
Table 4.3: Drive Nominal Values

Torque	-24.5 Nm
Power	30.6 kW
Switching Losses	69.4 W
Conduction Losses	100.8 W
Capacitor Losses	1.9 W
Junction Temperature	99.99 degC
Winding Current	51.15A
FIT Rate	$8.35e+04^{*}$ /cm2
CR Temperature Coefficient	0.21

* The failure rate is specified at 40,000 feet altitude based on IEC 62396 recommendation.

It is highlighted that the FIT rate is normalized with respect to the SEB cross section area which is different from the physical cross sectional area of the device. This is different from the analysis performed in chapter 3 as it was performed based on experimentally measured FIT rate of devices including the effect of SEB cross section. SEB cross section is also a function of applied bias voltage and varies in the range of 10^{-11} to $10^{-}6$ cm^2 for few sample devices referred to in IEC-62396 [29]. A typical device SEB cross section of roughly 10^{-5} cm^2 is estimated in [82] for SiC devices.

The variation of switching and conduction losses as well as overall converter losses including capacitor ESR losses are shown in Fig. 4.7. The variation in switching and conduction losses can be attributed to the machine winding currents due to DC link variation.



(a) Semiconductor Loss Profile

(b) Converter loss profile

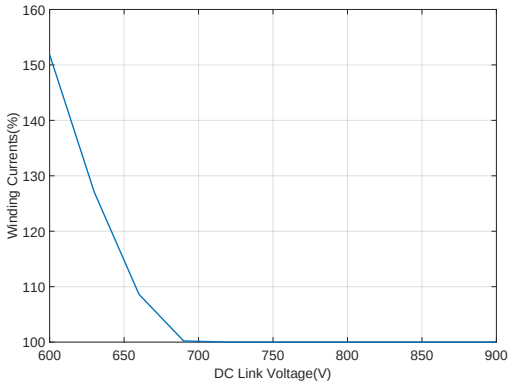
Figure 4.7: Drive system loss variation with DC link Voltage

The machine winding current variation and output power is shown in Fig. 4.8.

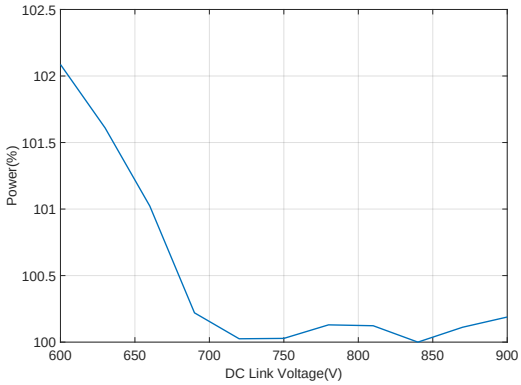
Applying the universal trend identified in [82] for SiC CR failure rate, the following trend is obtained for device FIT rate due to DC link variation as shown in fig. 4.9. More than 20X reduction in CR FIT rate can be achieved by reducing the DC link from 840V to 700V which is a significant mitigation option during high Solar activity.

DC link voltage variation impacts the losses in the drive system. The impact of this on semiconductor junction temperature is extracted and shown in Fig. 4.10. This information is necessary to assure operating within device safe operation limits.

Higher device losses provide an additional reduction in CR FIT rate due to the inverse



(a) Semiconductor Loss Profile



(b) Converter loss profile

Figure 4.8: Drive system loss variation with DC link Voltage

relationship of CR failure rate on device temperature. The nominal operating point (840V dclink voltage) CR failure rate temperature coefficient is shown in Table. 4.3 shows a reduction of 20% from reference failure rate at 25°C . In Fig. 4.11, normalized temperature coefficients of CR failure rate shows that at lower DC link voltages, we get an additional reduction of upto 2X in CR failure rate.

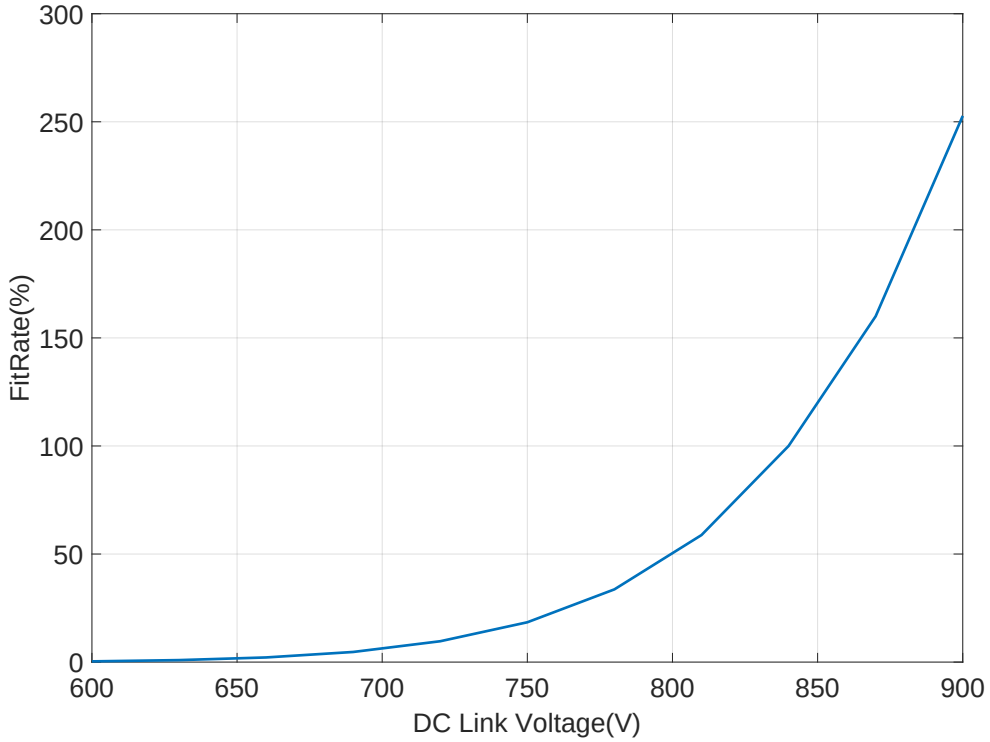


Figure 4.9: Normalized FIT rate of SiC devices at various DC link voltages

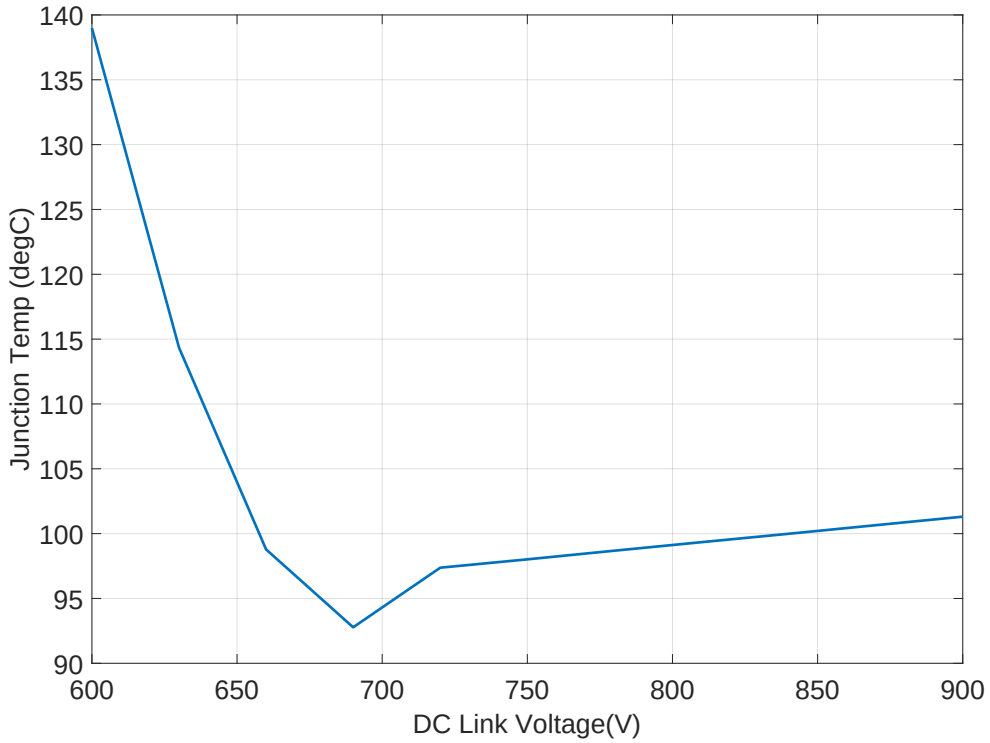


Figure 4.10: Junction temperature of semiconductors under various DC link voltages

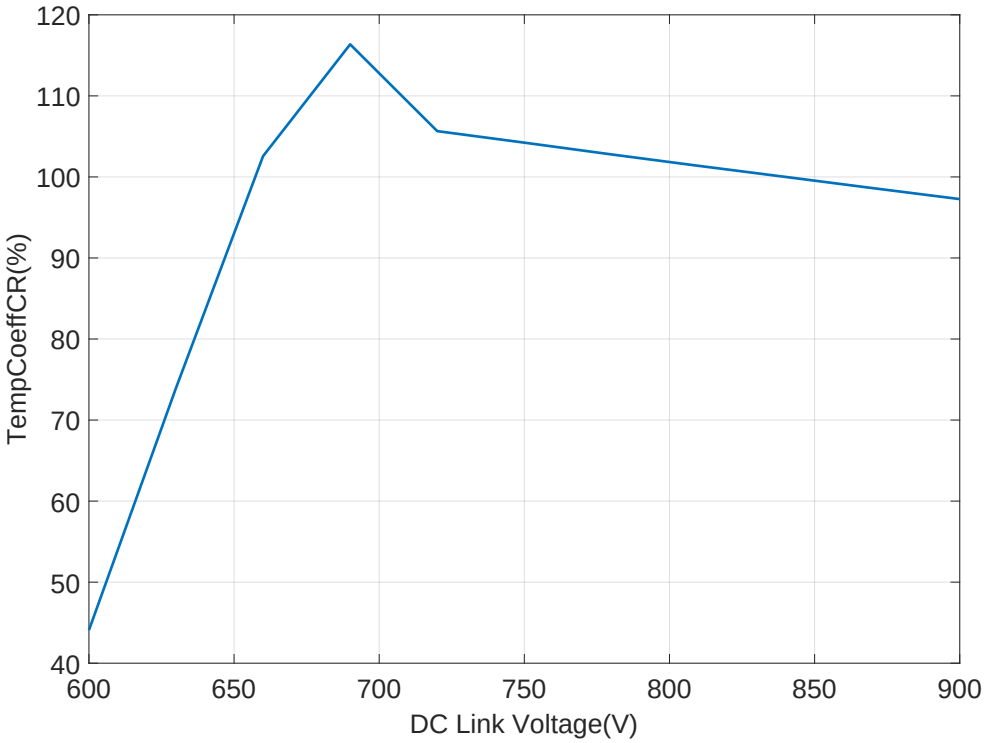


Figure 4.11: Normalized CR failure rate Temperature Coefficient

4.4 Summary

Cosmic ray induced failures is an important failure mode to consider for aerospace power converters. Hence a detailed case study is carried out to consider thermal control as well as voltage derating to mitigate CR failures during solar events or at geographic regions of low geomagnetic rigidity. It is shown using a universal trend of CR failure rate of SiC modules that voltage control is the more suitable approach compared to thermal control. CR failure mitigation measures are usually applied for short durations during high background radiation periods and hence the impact on wearout reliability is minimal and can be safely ignored.

Chapter 5

Operation of Three Level Neutral-Point Clamped Converters and Neutral Point Balancing

Abstract - Multi level topologies are a suitable topology for higher power converters with high DC link voltages for future electric aircrafts. 3L-NPC is one of the robust multi-level topologies and hence it is studied for a motor drive application. In this chapter, neutral point balancing which is a fundamental requirement for 3L-NPC converter operation is studied. A first principles based theoretical foundation for DC link unbalance and impact of output phase currents on neutral point potential is presented. Furthermore, a new approach was independently developed for DC link balancing of carrier based PWM controlled 3L-NPC converters (no novelty is claimed as it was already published before it could be presented by the author of this work). Differently from the state of the art balancing methods, the proposed algorithm is a best effort cycle by cycle balancing approach which can be easily extended to other multi level topologies. Experimental validation and comparison against a state of the art balancing algorithm is presented. As an additional benefit, the best effort balancing can be easily extended to single phase 3L-NPC converters as well as to converters operating in fault mode.

5.1 Introduction

Higher operating voltages can be adopted in electrical systems to achieve higher efficiencies. For example, the latest solar PV systems are designed with 1500V as the DC link voltage. In the case of electric car fast chargers, 1000V as output DC link voltage is already the standard while wind turbine size have reached 12 MW for individual units with corresponding increase in DC link voltages to medium voltage levels. At higher DC link voltages, multi level topologies are a natural choice [83] for power converters.

The 3L-NPC is a popular converter topology at DC link voltages above 1000V. The basic operational principles of the 3L-NPC are summarized in [84]. Balancing the neutral-point potential is a fundamental operational requirement for 3L-NPC converters. It has been a widely studied subject since the topology was first proposed. In [85], an analytical calculation for the DC link voltage fluctuation based on neutral point current is given. It has been shown that in the absence of non-idealities, neutral point current contribution from output phase currents are zero [86]. Electrical component tolerance in the converter results in DC link unbalance in closed loop current control mode. These variations can be due to tolerance of capacitance values, variation in phase impedances, sensor characteristics etc. Hence DC link balancing is essential to achieve stable operation of 3L-NPC converters.

One of the early mitigation measure identified to balance the neutral point is to add a zero-sequence voltage to the phase voltage modulation references. A PI controller is widely reported as the controller acting on the voltage imbalance and generating the zero-sequence voltage. Instead of a PI controller, another approach has been adopted in [87] wherein an offset is added to the modulation signals to apply the appropriate zero sequence voltage. A similar approach has been adopted in [88] and [1] wherein the neutral point duty cycle is varied based on the phase current direction and the voltage imbalance. In the case of SVPWM, reducing the dwell time at small voltage vectors are reduced or substituted with another vector which would increase or decrease neutral point current to achieve voltage balance [89], [90], [91]. The key difference between the zero sequence injection method and re-routing of the neutral point current as described

in references [87] - [91] is the bandwidth of the balancing controller. As zero sequence injection does not optimally modify the neutral point current, the balancing controller must have a very low bandwidth. The reason for the non-optimality would be clarified in this chapter. In [87] - [91], switching cycle by cycle balancing is achieved by modifying the modulation signals.

In [87] and [1], an inverter centric balancing technique is presented. The concept of per phase balancing in introduced. The theoretical analysis is performed for CB-PWM mode. SV-PWM case is not studied further as equivalence to CB-PWM has been demonstrated in [92]. It would be shown via the analysis that, all the balancing efforts in a 3L-NPC converter is achieved by redirecting the neutral point current utilizing the additional degree of freedom in the 3L-NPC - the extra voltage level. Based on the theoretical framework, a simple algorithm is proposed to achieve neutral point voltage balance. This novel algorithm achieves a best effort balancing per phase. The per phase balancing approach is a key differentiator from state of the art methods and enables seamless transition to fault mode operation. The new algorithm is applicable with no modification for single phase 3L-NPC converter as well.

5.2 Theoretical estimation of neutral point current and balancing

In this section, a brief introduction to the 3L-NPC operation is provided. The power circuit of the 3L-NPC converter is shown in Fig. 5.1.

Each phase leg can be in 3 different states - connected to positive rail, negative rail or neutral rail. The phase states and corresponding switch states are summarized in Table. 5.1.

The possible current paths in various switching states are graphically shown in Fig. 5.2.

It can be clearly seen that, the zero state contributes to neutral point current flow and neutral point imbalance. One of the most obvious method for avoiding neutral

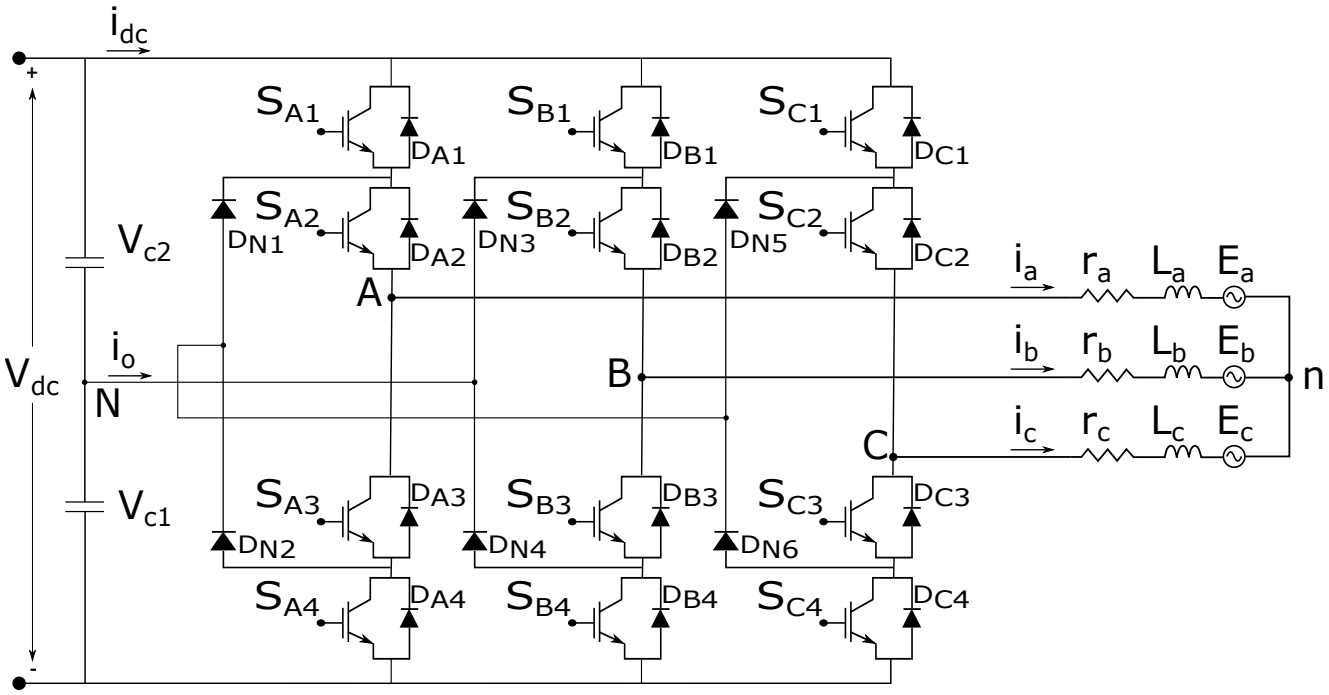
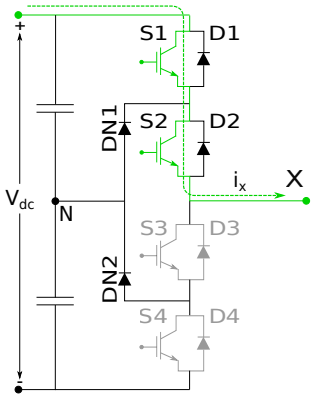


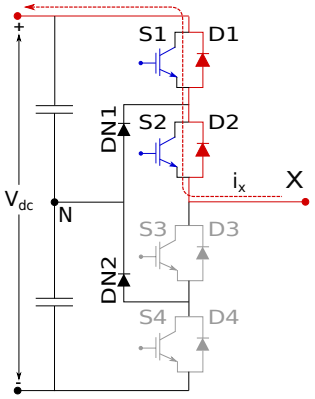
Figure 5.1: 3L-NPC power circuit

Table 5.1: Switch States and Pole Voltages

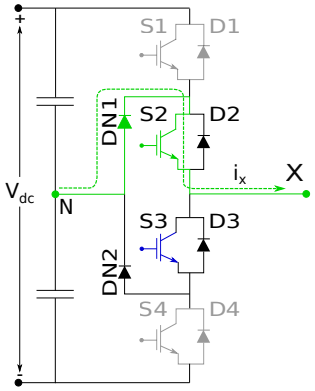
Switching State	Switch Status x = a,b,c				**Pole Voltage**
S_x	S_{x1}	S_{x2}	S_{x3}	S_{x3}	V_{xN}
(+)	1	1	0	0	$V_{DC}/2$
0	0	1	1	0	0
(-)	0	0	1	1	$-V_{DC}/2$



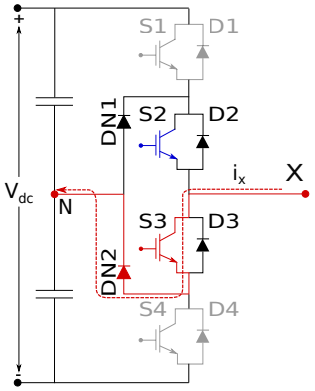
(a) Positive Voltage Positive Current



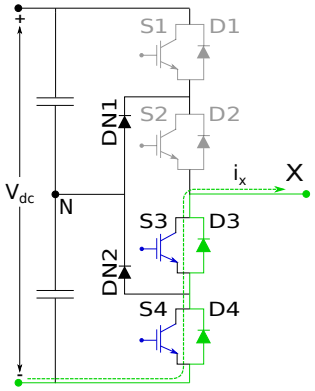
(b) Positive Voltage Negative Current



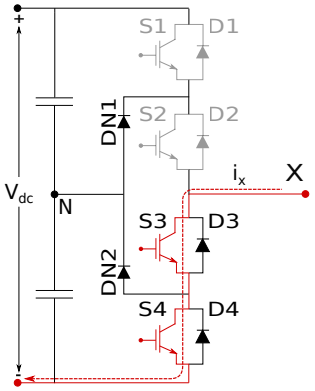
(c) Zero Voltage positive current



(d) Zero Voltage negative current



(e) Negative Voltage Positive Current



(f) Negative Voltage Negative Current

Figure 5.2: NPC switch states and current paths

point imbalance is to avoid the zero state altogether - in effect operate the converter as a 2L converter. Increasing the modulation index reduces the dwell time in zero state and correspondingly reduces neutral point current. However, the balancing effect is also dependent on the phase current and that is not accounted for in the PI controller based zero sequence injection approach. While operating in SVPWM, balancing effect can be achieved by selection of appropriate voltage vectors to obtain desired neutral point current [91]. In carrier based PWM mode, balancing effect can be achieved by utilizing all the voltage states - [(+), 0, (-)] to generate a particular modulation value [1]. An analytical method to calculate the appropriate offset to apply to the modulation signals are provided in [1]. A generalized method for offset generation is presented with simple steps.

5.2.1 Sine carrier PWM for a 3L-NPC converter

A short overview of carrier based PWM for a 3L-NPC is presented in order to present the balancing method. In carrier based PWM for a 3L-NPC, two approaches are possible to generate the switching states. In dual carrier method, the modulation signal is compared against two carriers, cr_P and cr_N as shown in Fig. 5.3. The logic table is provided in Eq. (5.1) and (5.2).

$$m_x > cr_P \Rightarrow S_{x1} = 1 \text{ else } S_{x1} = 0 \tag{5.1}$$

$$m_x > cr_N \Rightarrow S_{x2} = 1 \text{ else } S_{x2} = 0 \tag{5.2}$$

Switch pairs $S_{x1} - S_{x3}$ and $S_{x2} - S_{x4}$ are operated complementarily.

The carrier modulation can be performed using a single carrier by generating a second modulation signal from the original modulation waveform as outlined in Eq. (5.3) and (5.4). The single carrier based modulation is shown in Fig. 5.4.

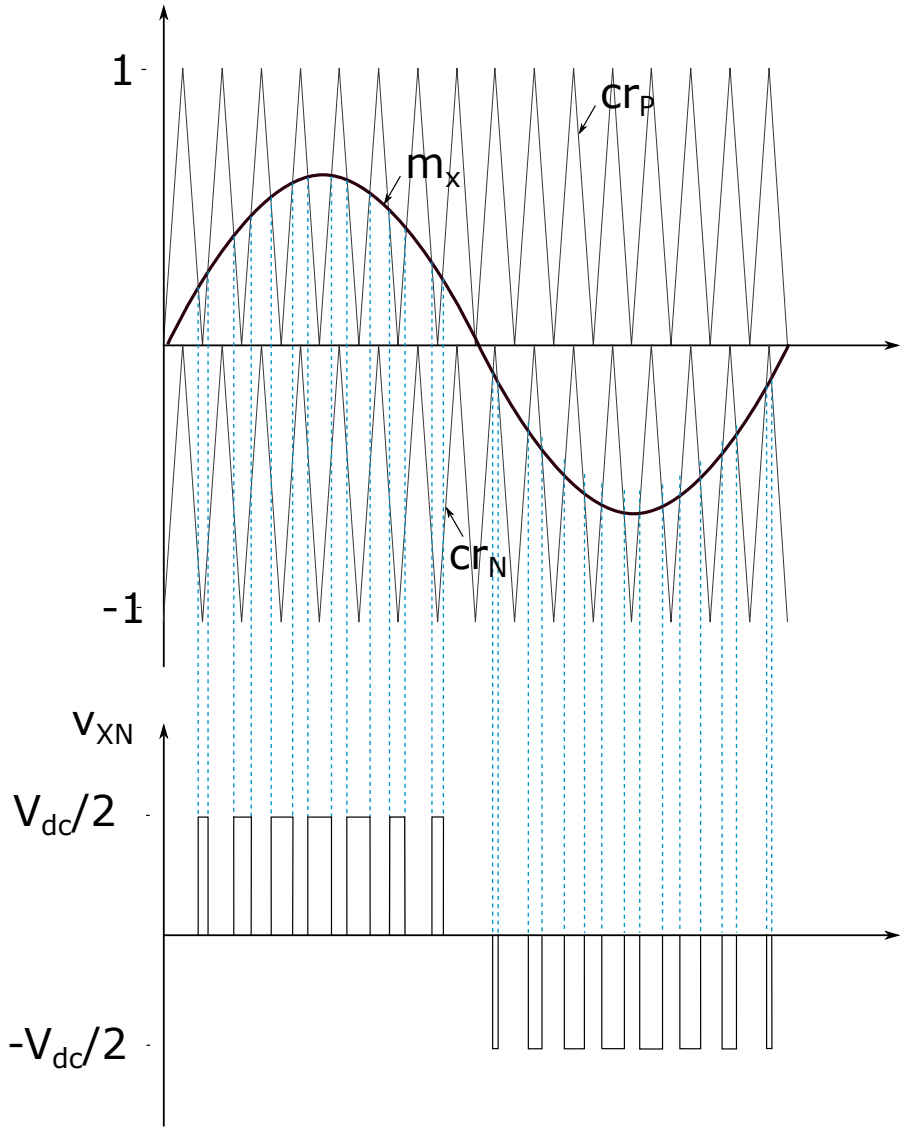


Figure 5.3: Dual Carrier Modulation

$$m_x > 0 \Rightarrow m_{xP} = m_x \text{ and } m_{xN} = 1 \tag{5.3}$$

$$m_x < 0 \Rightarrow m_{xP} = 0 \quad \text{and } m_{xN} = 1 + m_x \tag{5.4}$$

The required output modulation value can be expressed in terms of the derived modulation signals as Eq. (5.5).

$$m_x = \ m_{xN} + m_{xP} - 1 \tag{5.5}$$

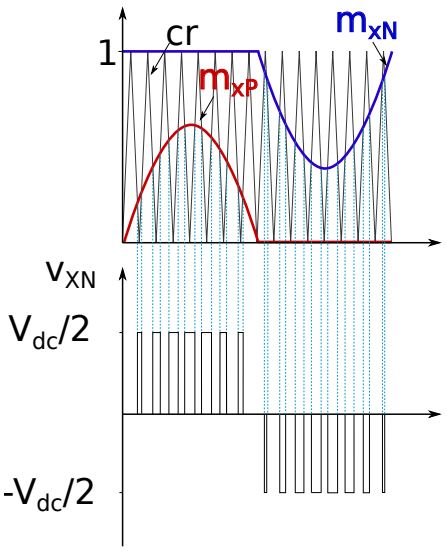


Figure 5.4: Single Carrier Modulation

A key point to note in single carrier modulation method is the ability to generate all 3 voltage states during a switching interval by adding an offset to m_{xP} and m_{xN} as long as the restriction in Eq. (5.6) is satisfied.

$$m_{xP} <= m_{xN} \tag{5.6}$$

5.2.2 Levers for Neutral point balancing

The duty cycle of the neutral point can be obtained from Eq. (5.1) and (5.2) and is given in Eq. (5.7).

$$\begin{aligned} d_{xNP} &= (1 - |m_x|) \\ &= m_{xN} - m_{xP} \end{aligned} \tag{5.7}$$

Based on the neutral point duty cycle, neutral point current induced by output phase currents is analytically derived as Eq. (5.8).

$$\begin{aligned} i_{o-ph} &= \sum_{x=a,b,c} (1 - |m_x|) i_x \\ &= \sum_{x=a,b,c} d_{xNP} \cdot i_x \\ &= \sum_{x=a,b,c} (m_{xN} - m_{xP}) \cdot i_x \end{aligned} \tag{5.8}$$

From Eq. (5.8), the only lever available to influence the neutral point current is to modify the neutral point duty cycle. The following restrictions apply as to how much offset can be applied to modify the neutral point duty cycle.

- d_{xNP} must be in the limit $0 <= d_{xNP} <= 1$
- d_{xNP} can only be reduced by adding an offset in order to achieve the desired modulation value
- The maximum offset must satisfy the limit specified in Eq. (5.6)
- In order to maintain the required output voltage, the condition specified in Eq. (5.5) must be satisfied.
  - An equal offset must be applied to m_{xP} and m_{xN} in the form of Eq. (5.9)

$$m_{xP}{}' = m_{xP} + m_{xoff} \tag{5.9a}$$

$$m_{xN}{}' = m_{xN} - m_{xoff} \tag{5.9b}$$

$$d_{xNP}{}' = m_{xN} - m_{xP} - (2 \cdot m_{xoff}) \tag{5.9c}$$

The effect of applying the offset is shown in Fig. 5.5. There is no direct transition from positive to negative state as long as d_{xNP} is not reduced to zero.

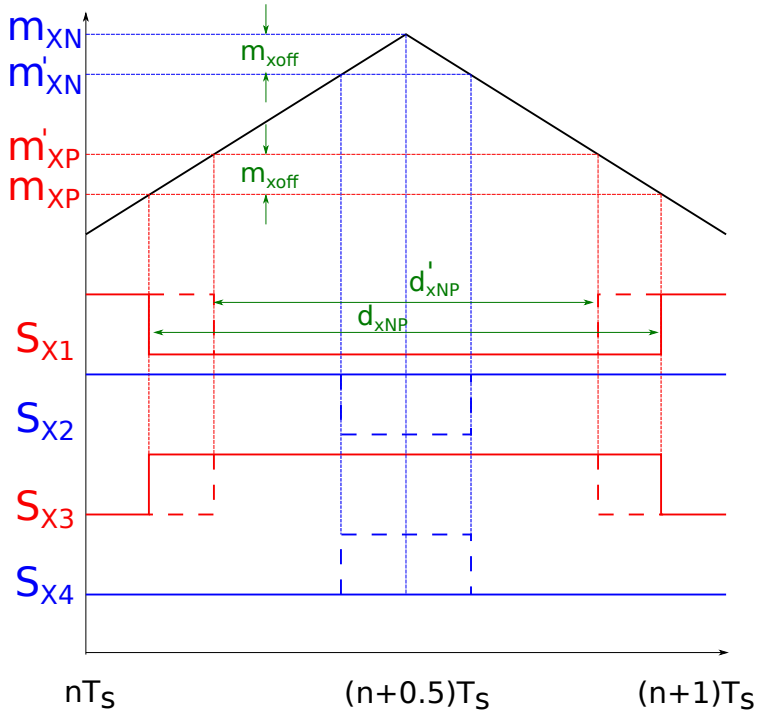


Figure 5.5: Neutral point duty cycle variation with offset

The balancing algorithm is developed based on the above theoretical foundation. In order to balance the capacitors with voltages v_{c1} and v_{c2}, the required balancing current in a switching period can be calculated as in Eq. (5.10):

$$i_{o-req} = \frac{v_{c1} - v_{c2}}{T_s} \tag{5.10}$$

Using Eq. (5.8) and (5.10), a new variable - i_{o-err} can be defined which denotes the amount of neutral point current required to achieve balancing within a switching interval.

$$i_{o-err} = i_{o-req} - i_{o-ph} \tag{5.11}$$

It can be seen from Eq. (5.8) that, the i_{o-ph} is decreased by reducing d_{xNP} if the particular phase current i_x is positive and vice versa if i_x is negative. The control action and effect is presented in Table . 5.2.

Table 5.2: Effect of Neutral point duty cycle reduction

	i_{o-ph}	i_{o-err}
$i_x(+)$	↓	↑
$i_x(-)$	↑	↓

5.2.3 Proposed Neutral point balancing algorithm

Combining Eqs. (5.11), (5.7) and (5.9), the neutral point offset necessary per phase is derived easily as a ratio of i_{o-err} and i_x. The offset will reduce the amount of current flow to the neutral point. Whether an offset could be applied in a beneficial manner for control is dependent on the phase current direction. It is summarized in Table . 5.2. The amount of offset that is required can be calculated directly from Eq. (5.12).

$$m_{xoff} = \frac{-i_{o-err}}{2 \cdot i_x} \tag{5.12}$$

The above calculation is performed for each phase and appropriate offset is generated dependent on the phase current direction and adhering to duty cycle limits. The proposed best effort balancing method is outlined in a flowchaart in fig.5.6. The algorithm is explained with comments in Appendix 1.

The key aspects of the algorithm are discussed here. The algorithm requires phase currents and DC link voltages to calculate neutral point current error as per Eq. (5.11). The algorithm would function as long as phase current measurement and duty cycle are

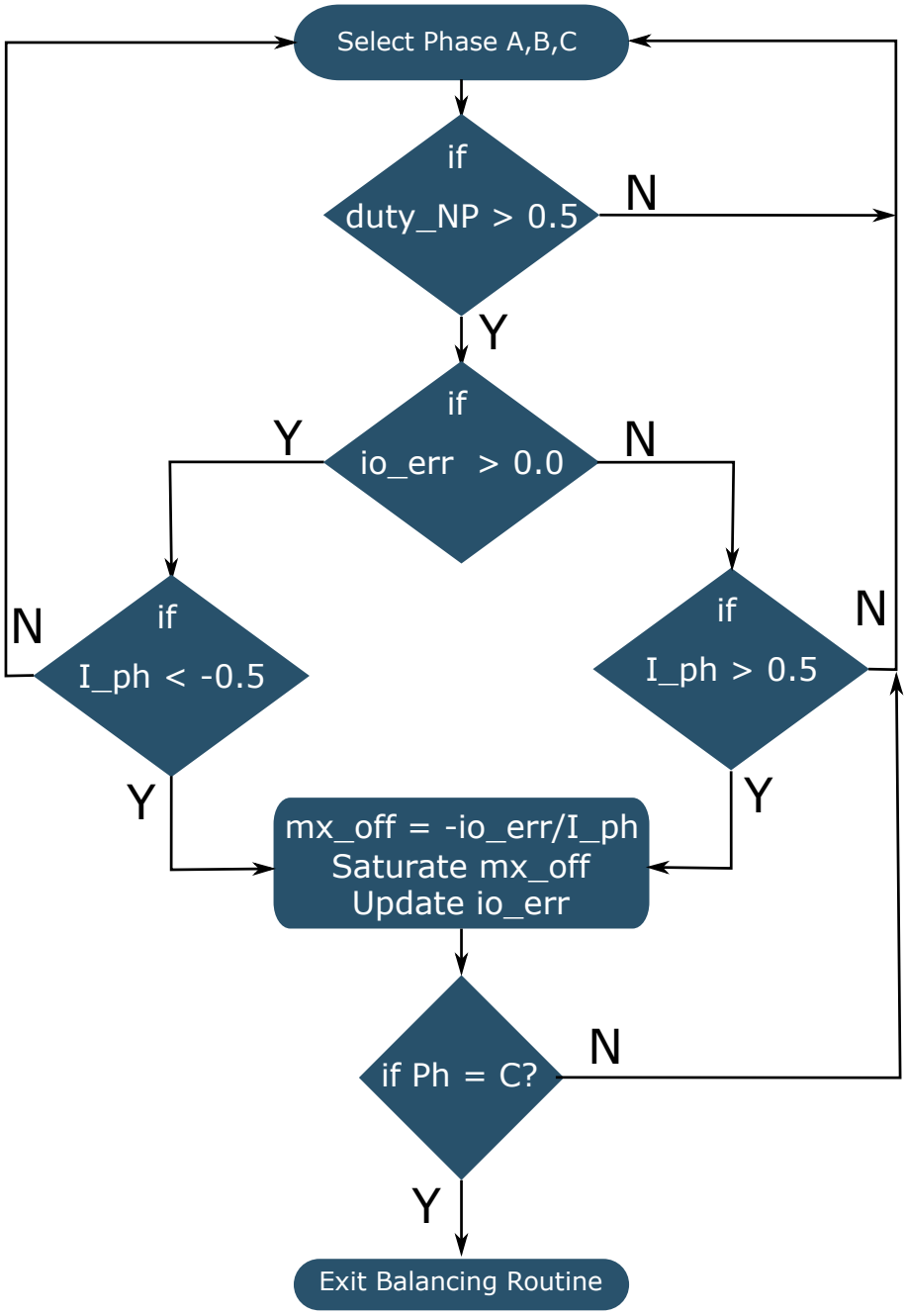


Figure 5.6: Neutral point balancing logic flowchart

accurate. In the case of fault reconfiguration, the algorithm is easily adapted by removing the balancing offset generation for the affected phase. The offset is only generated if the phase current is above a certain threshold as low phase curents has minimal impact on DC link imbalance and could provide minimal balancing effect. A further limit on balancing offset is applied based on neutral point duty cycle - d_{xNP}. This serves to limit the additional switching due to the balancing algorithm.

5.3 Simulation and Experimental Results

The proposed algorithm was validated using simulations and experiments and compared against a state of the art balancing algorithm specified in [1], hereinafter referred to as literature balancing method. The current control is implemented in ABC space utilizing proportional resonant controllers with possibility to suppress higher order harmonics if necessary. The controller structure including balancing is shown in Fig. 5.7.

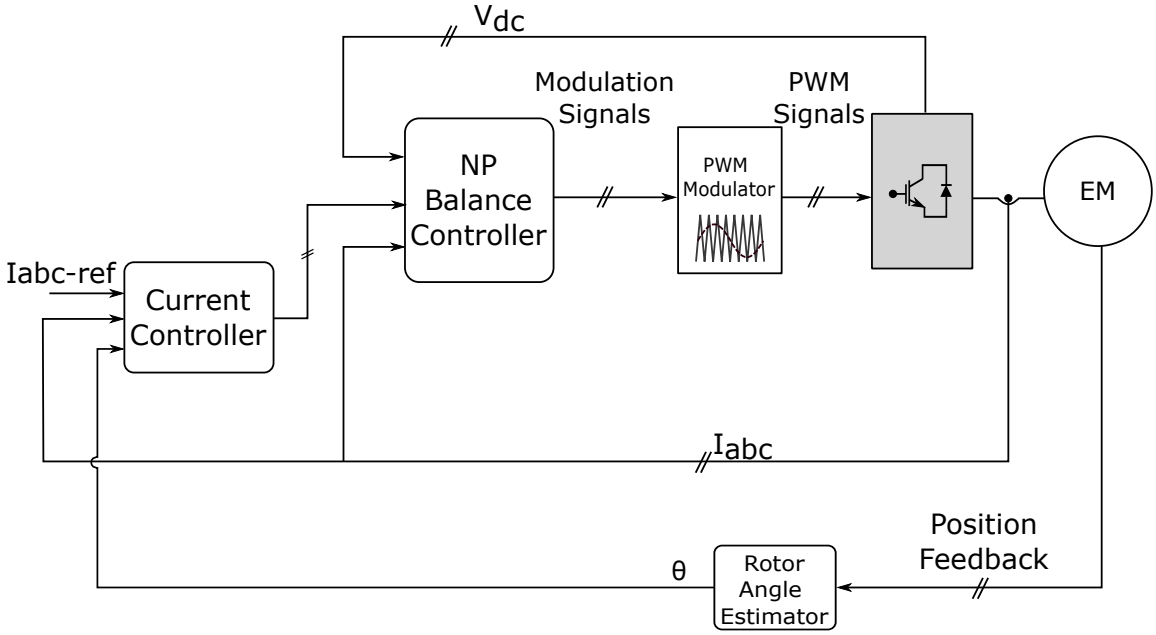
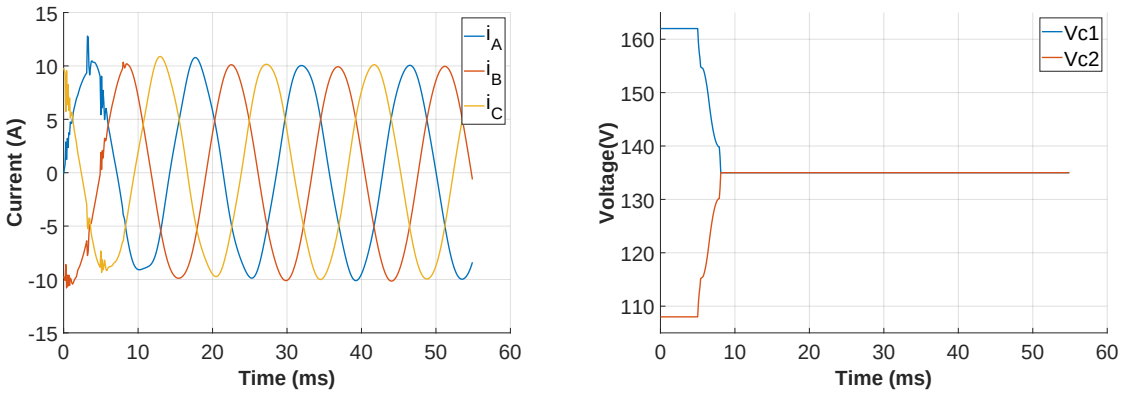


Figure 5.7: 3L-NPC controller structure

5.3.1 Simulations

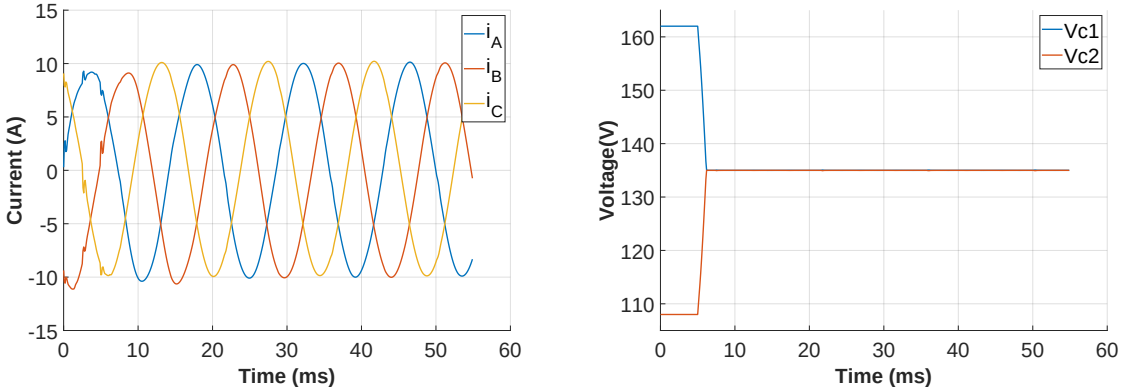
The simulation studies are carried out in PLECS software. The simulated phase currents and DC link voltages are shown for literature based balancing technique in Fig. 5.8 and

for the proposed approach in Fig. 5.9. The same parameters listed in Table . 6.1 for the experimental setup is programmed in the simulation model. A DC link unbalance is injected and maintained upto 5ms from the start of the simulation. At 5ms the injected unbalance is removed and the dc link balancing algorithms take effect to equalize the voltage across the capacitors. It must be noted that the simulated machine is not identical to the experimental machine and does not include anisotropies. Simulated harmonic spectrum of phase currents are nearly identical while the balancing speed is slightly better for the proposed method.



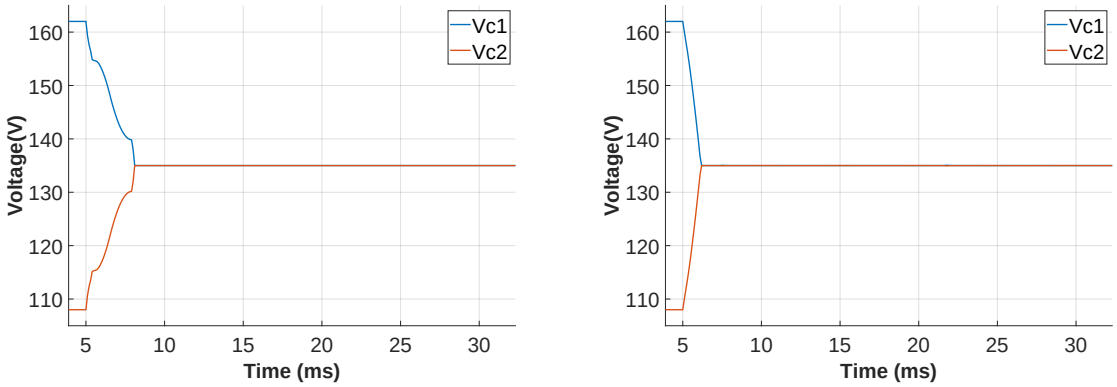
(a) Output Phase Currents (b) DC link Voltage

Figure 5.8: Simulated phase current and dc link capacitor voltage waveforms with literature balancing



(a) Output Phase Currents (b) DC link Voltage

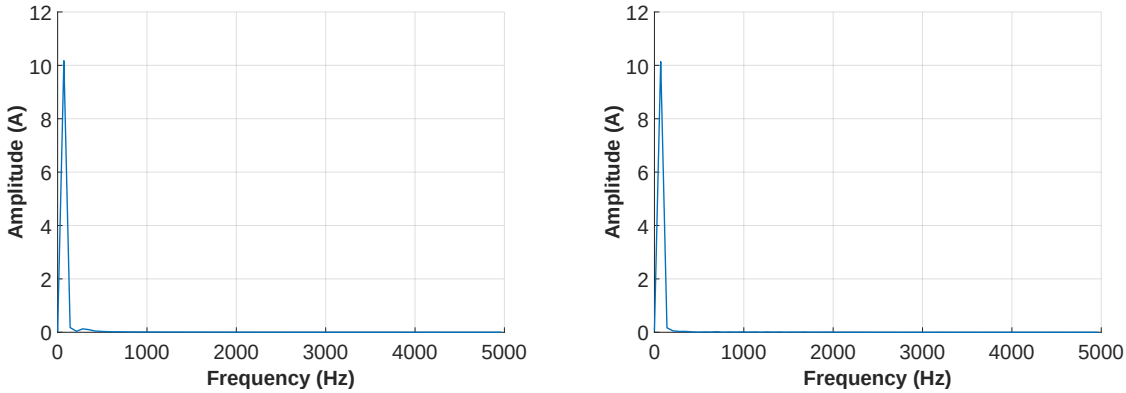
Figure 5.9: Simulated phase current and dc link capacitor voltage waveforms with proposed balancing



(a) DC link voltage balancing duration- literature balancing

(b) DC link voltage balancing duration- proposed balancing

Figure 5.10: Balancing speed comparison between literature and proposed balancing methods



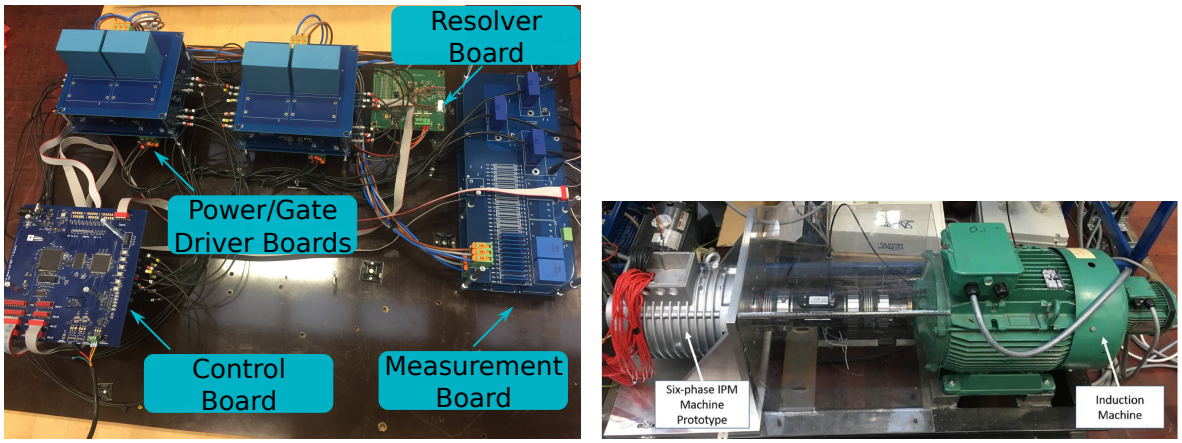
(a) Harmonic spectrum literature balancing

(b) Harmonic spectrum proposed balancing

Figure 5.11: Harmonic spectrum of simulated phase currents

5.3.2 Experimental setup

A short description of the experimental setup is provided here. A 3L-NPC converter prototype was developed using the "FS3L30R07W2H3F_B11" power module from Infineon rated at 650V and 30A. The converter is used to drive an IPM machine. The machine can be configured as multi-3 phase machine and hence has some inherent anisotropy which manifests as higher order harmonics. The converter control is performed in abc domain with Proportional Resonant (PR) controllers. Two additional resonant controllers are tuned to eliminate 5_{th} and 7_{th} harmonic current components. The controller board can control two 3L-NPC converters. The control code is run on a C2000 family floating point DSP (F28377D) clocked at 200 MHz. The experimental setup is shown in Fig. 6.14.



(a) 3LNPC Converter Prototype (b) IPM Machine Setup

Figure 5.12: NPC based Drive Setup

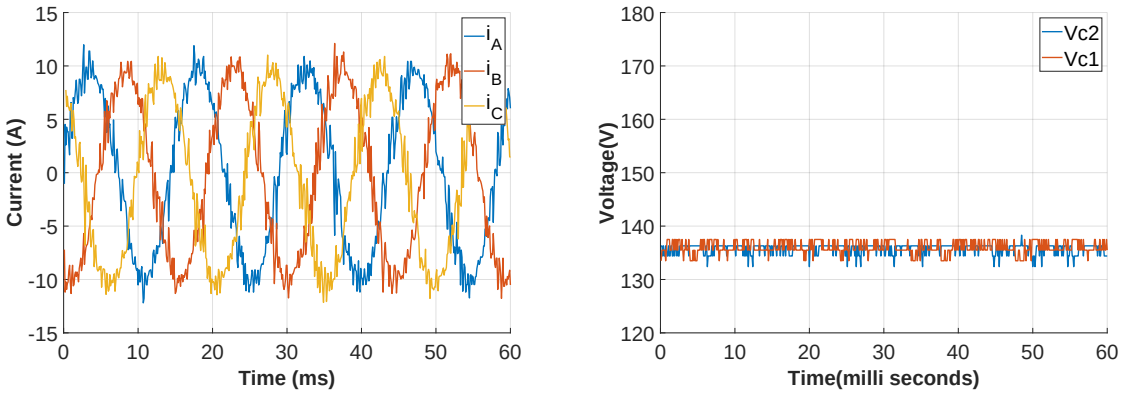
Key parameters of interest are summarized in table below:

Table 5.3: Converter/Machine parameters

DC link Voltage	270V
DC link Capacitance	101.1uF
Machine pole pairs	4
Machine operating speed	1050 rpm
Converter Switching Frequency	20 kHz
Datalogger Sampling Frequency	10 kHz

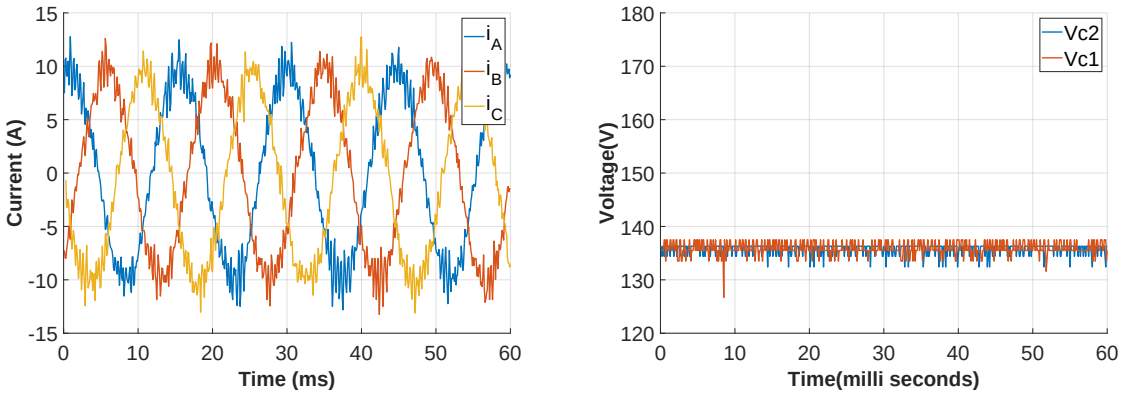
The 3 phase output currents and the DC link voltages are shown for literature based balancing in Fig. 5.13 and for the proposed approach in Fig. 5.14. The voltage resolution

of the DC link voltage sensing circuit is approximately 1V. Hence, the small ripples present in the DC link mid-point potential can be attributed to resolution and measurement noise.



(a) Output Phase Currents (b) DC Link Capacitor Voltage

Figure 5.13: Experimentally measured output phase currents and DC link capacitor voltages with literature balancing

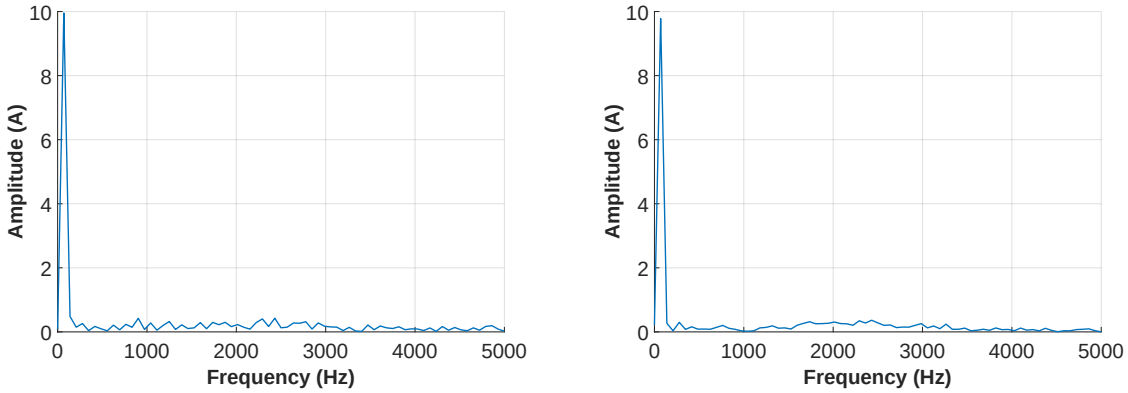


(a) Output Phase Currents (b) DC Link Capacitor Voltage

Figure 5.14: Experimentally measured output phase currents and DC link capacitor voltages with proposed balancing

The execution speed for both balancing approaches were measured by toggling a GPIO on the controller board before and after entering the balancing routine. The measured execution time for the proposed balancing method was 5.36 us while that for the literature balancing approach was 7.48 us. The functions implemented on the Micro Controller Unit (MCU) are provided in Appendix. B for reference. A further comparison of the harmonic spectrum of measured phase currents is provided for both the balancing approaches in Fig. 5.15. The experimental current harmonic spectrum confirms the simulation results.

It can also be observed that the 5_{th} and 7_{th} harmonic components are absent in the spectrum.



(a) Harmonic Spectrum Literature Balancing (b) Harmonic Spectrum Proposed Balancing

Figure 5.15: Experimentally measured output phase current harmonic spectrum

5.4 Summary

A theoretical basis for neutral point imbalance correction is outlined. A simple algorithm is proposed to balance the neutral point potential. The balancing effect of the proposed method is validated in simulation and experiments. The simplified calculations result in faster execution time in comparison to literature based balancing approach. Phase current harmonic spectrum is unaffected by the balancing effort especially in the low order harmonics.

Chapter 6

Open Phase Fault Tolerant Control of Multi Three Phase Machines

Abstract - Multi three phase machines are a known solution to provide redundancy and fault tolerance capability in high power applications. Control of multi three phase machines is typically implemented in DQ domain or VSD domain. An alternate control approach is per phase current control using proportional resonant controllers in ABC domain. In this chapter, ABC domain current controllers are utilized to demonstrate key advantages in high reliability applications - fault reconfigurability with minimal controller modifications and ability to control multiple harmonic components. ABC domain control structure enables seamless transition from healthy mode to fault mode with only algebraic operations at the controller output unlike DQ/VSD domains. Furthermore, single-phase operating mode in ABC domain provides an additional emergency operating mode which is complicated to realize in DQ/VSD control domains. The Fault mode operation under open circuit fault of one phase in each winding set is demonstrated. Simulation and experimental results validate the normal and fault condition operation of the proposed control method.

6.1 Introduction

The backbone for electrical propulsion is the electric drive consisting of:- electric motors/-generators, power electronic converters, control platform and sensors [4]. In order to meet aerospace fault tolerance requirements [93], redundancy and fault tolerance must be built into the propulsion system. Fault tolerance in applications requiring process continuity, for instance process industry, multi-phase machines and multi three phase systems have been gaining increasing popularity [94]. The key advantage of a multi three phase machine in comparison to a conventional 3 phase machine is the ability to generate a rotating MMF and consequently, a smooth torque after failure of one or more phases [95], [96]. Recently multi-phase machines are being considered for future MEA/AEA propulsion applications.

The fundamental system equations in terms of flux linkages for a multi-phase machine was shown in [97]. Typically, a transformation is applied - Clarke transformation in the case of three phase machine and VSD transformation is performed for multi-phase machines and current control is carried out in the transformed space.

Prior literature has extensively studied the two methods of multi three phase machine control - DQ control, where each three phase set is considered independently ignoring mutual coupling between winding sets [98] and VSD based control [99], [100]. The mismatch in torque estimation and reduction in control performance of independent DQ control when inter winding coupling is not accounted for is shown in [101]. A comparison between VSD and DQ control and the conditions under which the two are equivalent is shown in [102]. DQ control is chosen when independent control of 3 phase winding sets is a requirement. This feature is important from a safety certification point of view for high reliability applications, where a single point failure (controller in VSD method) could lead to failure of the whole system. The work in [103] provides a model for independent DQ control based on some approximations. The model is similar to the one derived from VSD transformation. Another approach was proposed by [104], a distributed control scheme based on VSD analysis. Both the above approaches provide the ability to perform independent current control of each winding set. The above methods do not propose a fault

mode reconfiguration mechanism other than disabling the faulty winding set.

Fault tolerance method for a multi three phase machine with common neutral was proposed in [105]. The current references of remaining healthy phases are modified to generate a rotating MMF. In [106], fault mode control of a dual three phase machine with two isolated neutrals is presented. The current controller is reconfigured such that the machine is operated with two single-phase winding sets operating in quadrature to each other. This approach is very interesting and a mathematical method of estimating the fault current references is presented in this chapter.

In this section, control of a dual three phase machine using PR controllers is implemented. It would be shown that, controller implementation in ABC domain is comparable in computational complexity with respect to DQ or VSD methods. The key contributions in this section are the fault mode controller reconfiguration and current reference generation to maximize torque in fault mode. The controller in ABC domain is easily reconfigurable for fault mode control. Single open phase fault and dual open phase fault operation is presented and experimentally validated.

6.2 Multi 3 phase drive system

An asymmetrical six-phase machine with isolated neutrals is analysed in this study. The analysis can be easily extended to higher winding set configurations. The machine drive system is showin in Fig. 6.1. Each three-phase set is fed by a 3L-NPC converter.

6.2.1 Machine modelling and control

The equivalent per phase model of the machine is derived in this section. The phase progression angles are shown with the reference axis aligned with phase a1.

$$\begin{aligned}[\Theta] &= \begin{bmatrix} 0 & \frac{\pi}{6} & \frac{2\pi}{3} & \frac{5\pi}{6} & \frac{4\pi}{3} & \frac{9\pi}{6} \end{bmatrix} \\ &= \begin{bmatrix} \theta_{a1} & \theta_{a2} & \theta_{b1} & \theta_{b2} & \theta_{c1} & \theta_{c2} \end{bmatrix} \end{aligned} \tag{6.1}$$

The stator voltage equation matrix with permanent magnet flux λ_m can be expressed

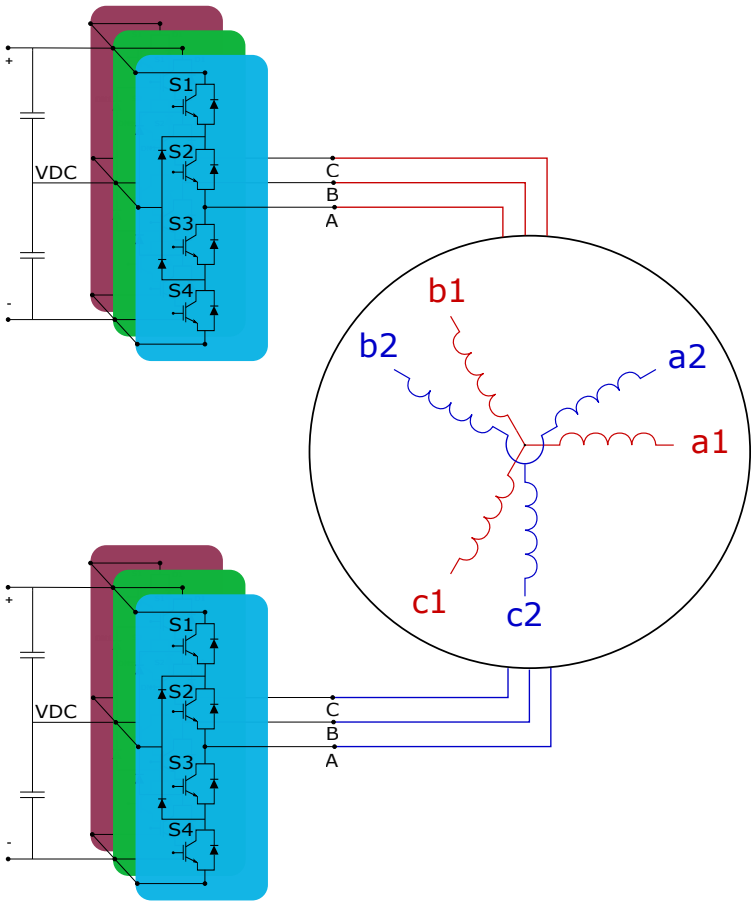


Figure 6.1: 6 phase machine with isolated neutrals

in most general form as

$$\begin{aligned}[V_s] &= [R_s]\cdot[i_s] + p\cdot[\lambda_s] \\ &= [R_s]\cdot[i_s] + p([L_{ss}][i_s] + \lambda_m cos[\omega t - \theta_x])\end{aligned} \tag{6.2}$$

where, the voltage and current vectors are defined as

$$[V_s] = \begin{bmatrix} V_{a1} \\ V_{a2} \\ V_{b1} \\ V_{b2} \\ V_{c1} \\ V_{c2} \end{bmatrix} \quad [i_s] = \begin{bmatrix} i_{a1} \\ i_{a2} \\ i_{b1} \\ i_{b2} \\ i_{c1} \\ i_{c2} \end{bmatrix}$$

The resistance and inductance matrices in (6.2) are defined as follows.

$$R_s = r_s \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix} \tag{6.3}$$

$$
\begin{aligned}
L_{ss} =& L_{ls}\begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix} + \\
& L_A \begin{bmatrix} cos[\Theta_{a1}] \\ cos[\Theta_{a2}] \\ cos[\Theta_{b1}] \\ cos[\Theta_{b2}] \\ cos[\Theta_{c1}] \\ cos[\Theta_{c2}] \end{bmatrix} - L_B \begin{bmatrix} cos[2(\omega t - \Theta L_{Ba1})] \\ cos[2(\omega t - \Theta L_{Ba2})] \\ cos[2(\omega t - \Theta L_{Bb1})] \\ cos[2(\omega t - \Theta L_{Bb2})] \\ cos[2(\omega t - \Theta L_{Bc1})] \\ cos[2(\omega t - \Theta L_{Bc2})] \end{bmatrix}
\end{aligned} \tag{6.4}
$$

L_{ls}, L_A, L_B is the stator leakage inductance, average value of magnetizing inductance and variation amplitude of magnetizing inductance respectively.

The angle matrices $[\Theta_{a1}], [\Theta_{a2}]$... represent the relative angle difference between any particular $phase_{xn}$ with other phases. They are given by

$$[\Theta_{xn}] = [\Theta - \theta_x]$$

The $[\Theta L_B]$ matrix of each phase accounts for variation in magnetizing inductance for different phases. It is computed as half of the angle between the phases x and y added to the absolute angle from reference of phase x. For instance, $\theta L_{Ba2-a3} = \theta_{a2} + \frac{\theta_{a3} - \theta_{a2}}{2}$. The $[\Theta L_B]$ matrix for phases $a1$ and $a2$ are provided for reference.

$$
\begin{aligned}
[\Theta L_{Ba1}] &= \begin{bmatrix} 0 & \frac{\pi}{12} & \frac{4\pi}{12} & \frac{5\pi}{12} & \frac{8\pi}{12} & \frac{9\pi}{12} \end{bmatrix} \\
[\Theta L_{Ba2}] &= \begin{bmatrix} \frac{\pi}{12} & \frac{2\pi}{12} & \frac{5\pi}{12} & \frac{6\pi}{12} & \frac{9\pi}{12} & \frac{10\pi}{12} \end{bmatrix}
\end{aligned}
$$

Direct and quadrature inductance values, L_d, L_q in case of a synchronous reluctance machine are related to L_{ls}, L_A, L_B as follows

$$L_d = L_{ls} + \frac{3N}{2}(L_A - L_B) \tag{6.5}$$

$$L_q = L_{ls} + \frac{3N}{2}(L_A + L_B) \tag{6.6}$$

Eq. (6.2) to Eq. (6.4) is a complete representation of the asymmetrical 6 phase machine. Typical control approaches perform a Clarke transform or a VSD transformation to the machine model to derive a rotating reference frame equivalent model of the system. In order to further develop the machine model in ABC domain, the following conditions which apply to synchronous reluctance machine is considered. In a machine without inherent asymmetries only the fundamental harmonic is useful for torque generation. In order to generate a smooth mechanical torque, the stator currents must sum up to generate a rotating MMF. Hence the current references in a 6 phase machine can be expressed as

$$[i_s] = \begin{bmatrix} K_1 \cdot I \cdot cos[\omega t - \theta_{a1} + \phi] \\ K_2 \cdot I \cdot cos[\omega t - \theta_{a2} + \phi] \\ K_1 \cdot I \cdot cos[\omega t - \theta_{b1} + \phi] \\ K_2 \cdot I \cdot cos[\omega t - \theta_{b2} + \phi] \\ K_1 \cdot I \cdot cos[\omega t - \theta_{c1} + \phi] \\ K_2 \cdot I \cdot cos[\omega t - \theta_{c2} + \phi] \end{bmatrix} \tag{6.7}$$

Applying Eq. (6.7) in Eq. (6.2), the voltage equation per phase can be written as

$$\begin{aligned} V_x = &\Big(r_s + pL_{ls}\Big) i_x + pL_A \sum_{y=1}^{3N} i_y cos(\theta_y - \theta_x) \\ &- pL_B \sum_{y=1}^{3N} i_y cos(2\omega t - \theta_x - \theta_y) + p\lambda_m cos(\omega t - \theta_x) \end{aligned} \tag{6.8}$$

The electrical model showing the modelled components are graphically shown in fig.6.2.

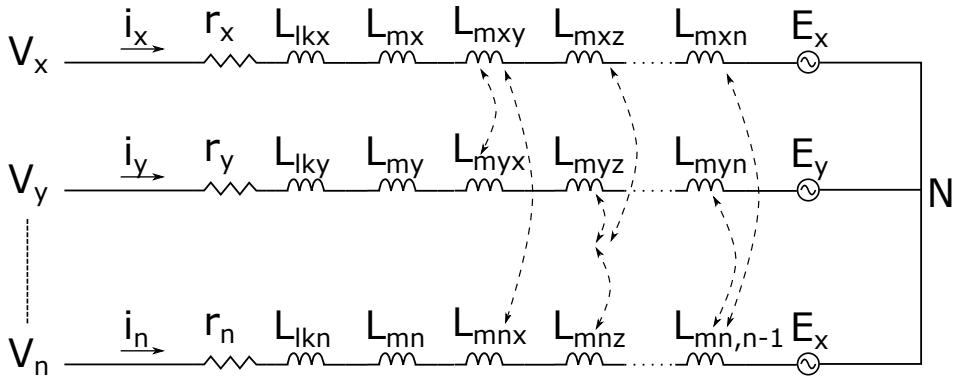


Figure 6.2: Electrical model of multiphase machine showing magnetizing flux linkage between phases

In the above figure, r_x is the stator resistance, L_{lkx} is the stator leakage inductance, L_{mx} is the self magentizing inductance, L_{mxy} is the magnetizing inductance due to flux linkage of phase y in phase x, E_x is the back-emf due to permanent magnet flux. L_{mx} and L_{mxy} together account for the average and reluctance induced magnetizing inductance term.

$$i_x = K_w I cos(\omega t - \theta_x + \phi) \tag{6.9}$$

$$\begin{aligned} V_x =& r_s \cdot i_x + p\left(L_{ls} + \frac{3}{2} L_A \sum_{w=1}^{N} \frac{K_w}{K_x}\right) i_x \\ & - p\left(\frac{3}{2} L_B I cos(\omega t - \theta_x - \phi) \sum_{w=1}^{N} K_w\right) \\ & - \omega \lambda_m sin(\omega t - \theta_x) \end{aligned} \tag{6.10}$$

As can be noted, the sum of current sharing coefficients equal number of winding sets, the equations can be written in a form which is identical in form to the VSD equation.

$$V_x = r_s \cdot i_x + p\left(L_{ls} + \frac{3N}{2 \cdot K_x} L_A\right) i_x - p\left(\frac{3N}{2} L_B I cos(\omega t - \theta_x - \phi)\right) - \omega \lambda_m sin(\omega t - \theta_x) \tag{6.11}$$

The first two terms in Eq. (6.11) account for machine flux dynamics represented in a per phase basis. The third term and fourth terms account for reluctance generated back emf, denoted as E_{xrel}, and permanent magnet flux generated back emf, denoted as E_x respectively. The reluctance generated back emf cannot be ignored in IPM machines. Reluctance generated back emf has a phase shift of -2ϕ with respect to the applied current. The phase voltage equation illustrates the inter-winding set interaction. System transfer function dependency on K_x, should be accounted for in the current controller.

The system model is very similar to the Clarke or VSD transformed system equations with only the reluctance variation accounted for as a separate potential term. This result in the present form is obtained due to the spatial and time dependence of the phase currents. It should be mentioned that this approach can be generalized to any spatial distribution of coils and current references. Any current distribution in a three-phase winding set with isolated neutral can be expressed as a positive and negative sequence combination.

Net mechanical torque developed is easily calculated by summing the power transferred by each phase. In healthy mode, the system torque is given by Eq. (6.12). This expression is in fact identical to the equations derived in DQ or VSD domain. The torque expression can be used to setup the speed/flux control loop in an identical manner to the DQ/VSD domains. Instead of providing I_d and I_q setpoints to regulate torque and flux, phase current amplitude and phase angle, ϕ are the setpoints required in ABC domain. Hence the calculation complexity or lookup tables necessary for the outer speed/flux controllers are identical compared to the conventional synchronous reference frame approaches.

$$T_m = \frac{3N}{2}\frac{p}{2}\left(\lambda_m I sin(\phi) - \frac{3N}{2} L_B I^2 sin(2\phi)\right) \tag{6.12}$$

6.3 ABC domain control structure

The detailed control structure for a single converter in normal operation is shown below in fig. 6.3. Only 2 PR controllers are necessary per inverter and control signal for third phase is obtained by an arithmetic relation.

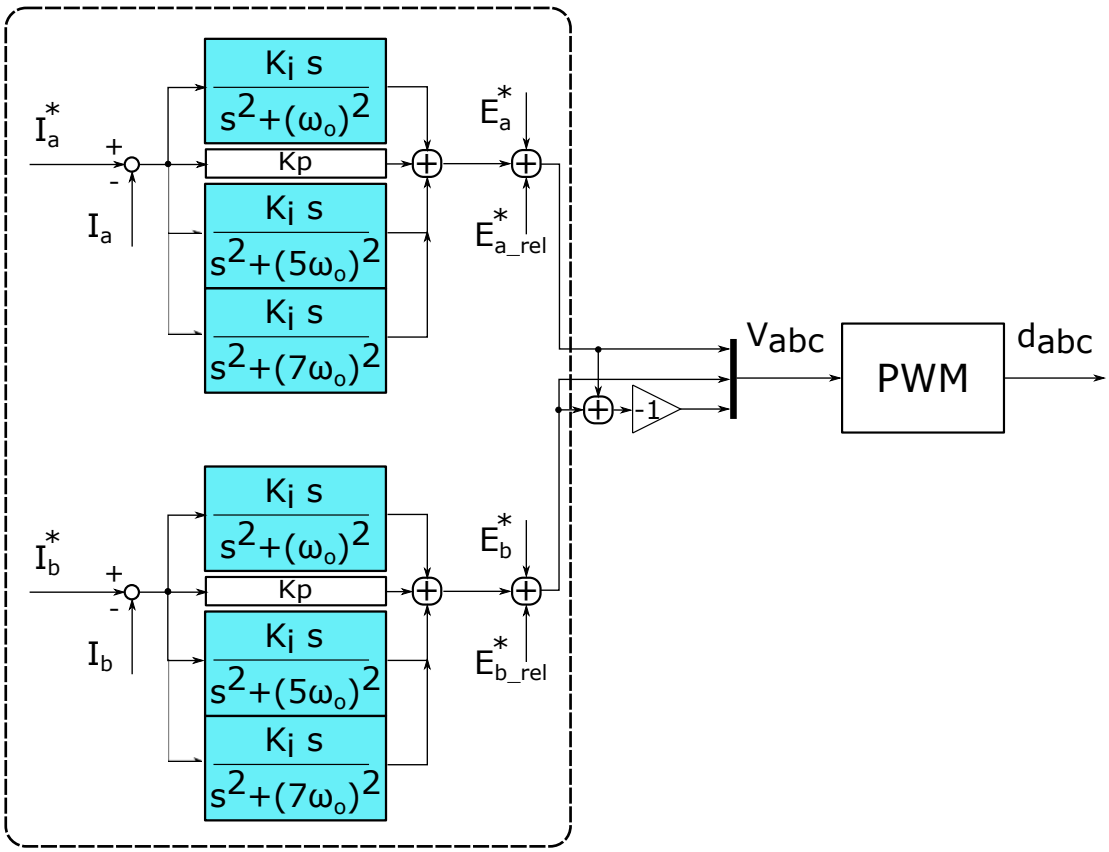


Figure 6.3: PR control structure per inverter

Multiple resonant terms can be added within the controller bandwidth to eliminate higher order harmonics. The necessity for multiple resonant controllers is due to the inherent asymmetries in multi phase machines which result in higher than normal harmonic contents in the back EMF.

The PR controller structure is easily reconfigurable for fault conditions as shown in

section 6.3.1.

6.3.1 Dominant fault modes of drive systems

The dominant fault modes in industrial drives have been described and quantified in [107]. Approximately 40% of the faults are attributed to power circuits with a large portion caused by power semiconductors. Semiconductor faults are either open circuit fault or short circuit fault. According to [108], the predominant failure mode in IGBTs is open circuit fault. The above is valid in the case of wire bond based IGBT modules while for press-pack modules, short circuit failure mode is more common. In the case of 3L-NPC converter, fault modes of inner and outer IGBTs presents different options for fault reconfiguration. Practically, inner switch fault prevents fault reconfiguration for motor drive applications, even though it can be mitigated for grid connected applications [109]. Short circuit fault of the outer IGBT can be potentially destructive for the inner IGBT as the entire DC link voltage would be applied across it. Fault reconfiguration is a possibility under open fault of outer IGBTs.

In the case of multi three phase drive systems with 3L-NPC converters, the fault reconfiguration option is to operate the faulty three-phase winding set in single-phase mode. Two different fault modes are studied - open phase fault in phase C2 alone and open phase faults in phases C2 and C1 of a dual three phase machine.

Single open phase fault

In the previous section, fault reconfiguration options for 3L-NPC based drive systems were described. Operating the healthy phases as a single-phase winding set is considered as the fault mode operation.

As one phase is open, the two remaining windings carry the same current and behave as a single winding set.

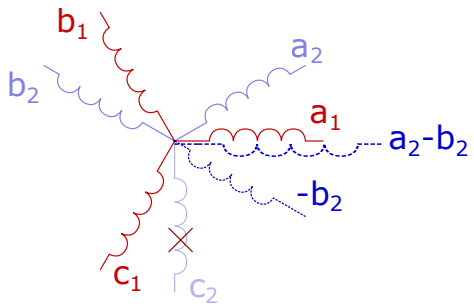


Figure 6.4: Fault mode machine

$$i_{a2} = K_{S2} I cos(\omega t + \phi_{S2}) \tag{6.13a}$$

$$i_{b2} = -K_{S2} I cos(\omega t + \phi_{S2}) \tag{6.13b}$$

The system equations for the healthy winding sets and the faulty set in single-phase operation is derived for development of controllers. The individual phase voltages after fault can be derived from Eq. (6.8). The single-phase set voltage equation takes the form of a line to line voltage equation.

$$\begin{aligned} V_{a_2 b_2} =& 2r_s \cdot i_{a2} + p\left(2L_{ls} + 3L_A\right) i_{a2} \\ &+ p\left(\sqrt{3}\frac{3(N-1)}{2} L_A\right) I cos(\omega t - \theta_{a2} + \frac{\pi}{6} + \phi) \\ &+ p\left(3L_B i_{a2} cos(2\omega t - 2\theta_{a2} - \frac{2\pi}{3})\right) \\ &- p\left(\sqrt{3}\frac{3(N-1)}{2} L_B I cos(\omega t - \theta_{a2} + \frac{\pi}{6} - \phi)\right) \\ &- \sqrt{3}\omega\lambda_m sin(\omega t - \theta_{a2} + \frac{\pi}{6}) \end{aligned} \tag{6.14}$$

The healthy winding set voltage equations are also impacted by the faulty winding.

$$
\begin{aligned}
V_x =& r_s \cdot i_x + p\left(L_{ls} + \frac{3}{2} L_A \sum_{w=1}^{N-1} \frac{K_w}{K_x}\right) i_x \\
&+ p\left(\sqrt{3} L_A i_{a2}\right) cos(\theta_x - \theta_{a2} + \frac{\pi}{6}) \\
&- p\left(\frac{3}{2} L_B I cos(\omega t - \theta_x - \phi) \sum_{w=1}^{N-1} K_w\right) \\
&- p\left(\sqrt{3} L_B i_{a2} cos(2\omega t - \theta_x - \theta_{a2} + \frac{\pi}{6})\right) \\
&- \omega \lambda_m sin(\omega t - \theta_x)
\end{aligned}
\tag{6.15}
$$

The loss of three phase symmetry leads to harmonics in phase voltages. The healthy winding set continues to generate a rotating MMF. The faulty winding set in single-phase mode can add an additional torque component albeit a pulsating torque contribution.

From the machine stator voltage equations, it can be observed that the machine reduces to a four winding set system with a new effective winding set a2-b2. The effective winding set in case of the six-phase machine is aligned with phase a1 given by vector summation of flux generated by the currents through phase a2 and b2. Hence the current reference of the single-phase winding must be set with a phase shift to reflect the effective orientation of the fictitious winding set a2-b2 as shown in Eq. (6.16). The magnetizing current and inter winding magnetizing inductance due to the single-phase set is scaled by a factor of $\sqrt{3}$ for the fundamental component.

$$
\phi_{S2} = -\theta_{a2} + \frac{\pi}{6} + \phi \tag{6.16}
$$

The control structure in the single-phase case is very similar to the healthy mode as seen in Fig. 6.5. The faulty phase is left uncontrolled while only a single PR controller is required to control the single-phase set.

The net torque of the 4 winding set operation can be derived as Eq. (6.17).

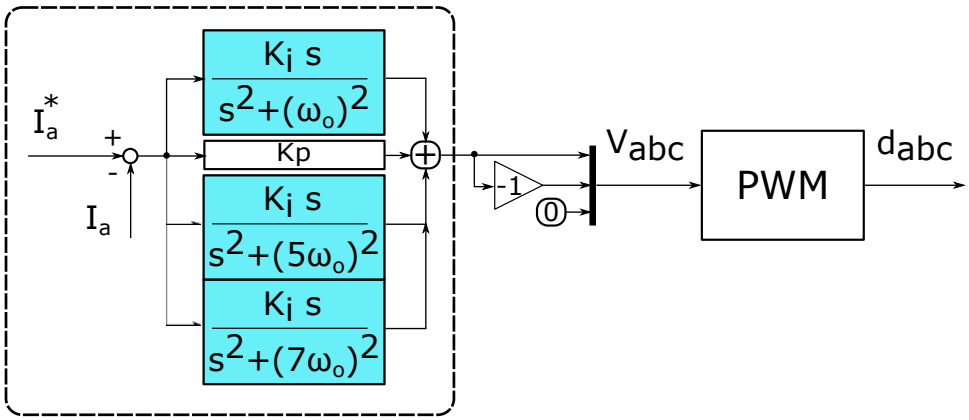


Figure 6.5: single-phase open fault mode control structure

$$T_{3ph} = \frac{3(N-1)}{2}\frac{p}{2}\left(\lambda_m I sin(\phi) - \frac{3(N-1)}{2}L_B I^2 sin(2\phi) - \frac{\sqrt{3}}{2}L_B K_{S2} I^2 sin(2\phi)\right) \tag{6.17a}$$

$$T_{sph} = \frac{\sqrt{3}}{2}\frac{p}{2}\left(\lambda_m K_{S2} I sin(\phi) - \frac{3(N-1)}{2}L_B K_{S2} I^2 sin(2\phi) - \frac{\sqrt{3}}{2}L_B K_{S2}^2 I^2 sin(2\phi)\right) \tag{6.17b}$$

$$T_{4ph} = T_{3ph} + T_{sph} \tag{6.18}$$

Dual single open phase fault

A more severe fault condition is when one phase in each winding set suffers from open faults. The machine effectively reduces to a dual winding set machine. The winding set distribution including fictitious single-phase systems is shown in Fig. 6.6.

$$\theta_{a1-b1} = \theta_{S1} = -\frac{\pi}{6} \tag{6.19a}$$

$$\theta_{a2-b2} = \theta_{S2} = 0 \tag{6.19b}$$

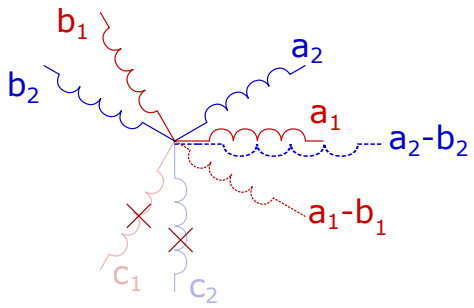


Figure 6.6: Double fault mode machine

The machine stator voltages can be derived as before starting with Eq. (6.8).

$$\begin{aligned} V_{a_1b_1} =& 2r_s{\cdot}i_{a1} + p\Big(2L_{ls} + 3L_A\Big)i_{a1} \\ &+p\Big(3L_A\Big)i_{a2}cos(\theta_{a2} - \theta_{a1}) \\ &+p\Big(3L_Bi_{a1}cos(2\omega t - 2\theta_{a1} - \frac{2\pi}{3})\Big) \\ &+p\Big(3L_Bi_{a2}cos(2\omega t - \theta_{a1} - \theta_{a2} - \frac{2\pi}{3})\Big) \\ &-\sqrt{3}\omega\lambda_m sin(\omega t - \theta_{a1} + \frac{\pi}{6}) \end{aligned} \tag{6.20}$$

In the case of dual single-phase fault, rotating MMF is not present from the healthy winding set. Hence the single-phase currents must generate a rotating MMF to develop torque in the machine. A rotating MMF condition is satisfied by the presence of orthogonal current/flux components given by Eq. (6.21).

$$\begin{aligned} Icos(\omega t) =& -i_{a1}sin(\theta_{S1}) - i_{a2}sin(\theta_{S2}) \\ -Isin(\omega t) =& i_{a1}cos(\theta_{S1}) + i_{a2}cos(\theta_{S2}) \end{aligned} \tag{6.21}$$

The above equations are derived by fixing the rotating stator flux at an angle 90°with respect to the rotor without accounting for reluctance torque. The graphical visualization is shown in Fig. 6.7.

The general equation in Eq. (6.21) can be solved for the particular situation at hand

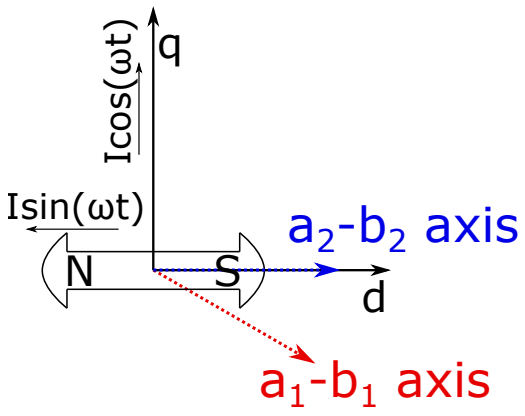


Figure 6.7: Rotating flux generated with two single-phase windings

by applying the restrictions from Eq. (6.19).

$$\begin{aligned} I_{a1} &= 2 \cdot I \\ \phi_{S1} &= -\pi \\ I_{a2} &= 2 \cdot I \\ \phi_{S2} &= \frac{\pi}{6} \end{aligned} \tag{6.22}$$

The torque contribution from each single-phase set can be calculated as shown in Eq. (6.23).

$$\begin{aligned} T_{S1} &= \frac{\sqrt{3}}{2}\frac{p}{2}\left(\lambda_m I_{a1} sin(\frac{\pi}{6})\right) \\ T_{S2} &= \frac{\sqrt{3}}{2}\frac{p}{2}\left(\lambda_m I_{a1} sin(\frac{\pi}{6})\right) \end{aligned} \tag{6.23}$$

The controller structure is identical to the single open phase fault condition as shown in Fig. 6.5. Both winding sets are operated as single-phase winding sets with the current phase angles derived in Eq. (6.22). A comparison is made to the fault mode control proposed in [106]. The above referred method requires a controller reconfiguration while not able to provide a single-phase fault mode operation. The machine control is directly

transitioned to the presented dual phase fault operation. The potential for higher torque is lost by operating in dual phase fault mode. Another key advantage for the proposed method in comparison to the literature method is lack of controller modification which is required in the latter.

6.4 Simulations of dual three phase drive

A simulation model for a dual three phase machine was developed using PLECS blockset in Simulink to verify the current controller performance of the 3L-NPC converters.

6.4.1 Tuning of the current controller

The machine model is simplified to a RL load with a back emf term to tune the PR controller. The discrete plant transfer function including the effect of Zero order hold and computational delay is given by Eq. (6.24)

$$G_{PL}(z) = \frac{z^{-2}}{R}\frac{1-\rho^{-1}}{1-z^{-1}\rho^{-1}} \tag{6.24}$$

where $\rho = e^{R \cdot T_s/L}$

The ideal PR controller structure is shown in Fig.6.3. A damping term is added to the resonant term for practical implementation. In the case of drives, the resonant terms do not provide high gain at zero speed. Hence an integrator is added to the controller to improve start-up performance. The full control structure in s-domain is given by Eq. (6.25)

$$\begin{aligned} G_{PIR}(s) =& K_P + \frac{K_I}{s} \\ &+ K_R \sum_{h=1}^{h_{max}} \frac{k_{damp}(h\omega)s}{s^2 + k_{damp}(h\omega)s + (h\omega)^2} \end{aligned} \tag{6.25}$$

The integrator term is discretized using the tustin method while the resonant term

is implemented using the SOGI method [110]. The SOGI consists of two integrators and the method for their discretization influences the frequency response. The forward integrator is discretised using forward Euler method and the feedback integrator using backward Euler method according to [111]. Tuning of the PR controller is performed to achieve a crossover frequency of 1kHz for the current controller. K_R is chosen to get a high gain at the frequencies to track. The tuning procedure is as described in [112]. The PR parameters are summarized in Tab. 6.1.

The open loop bode plot of the Plant and the PIR controller is plotted in Fig. 6.8. It should be noted that the margins obtained for the controller accounts for the discretization effects.

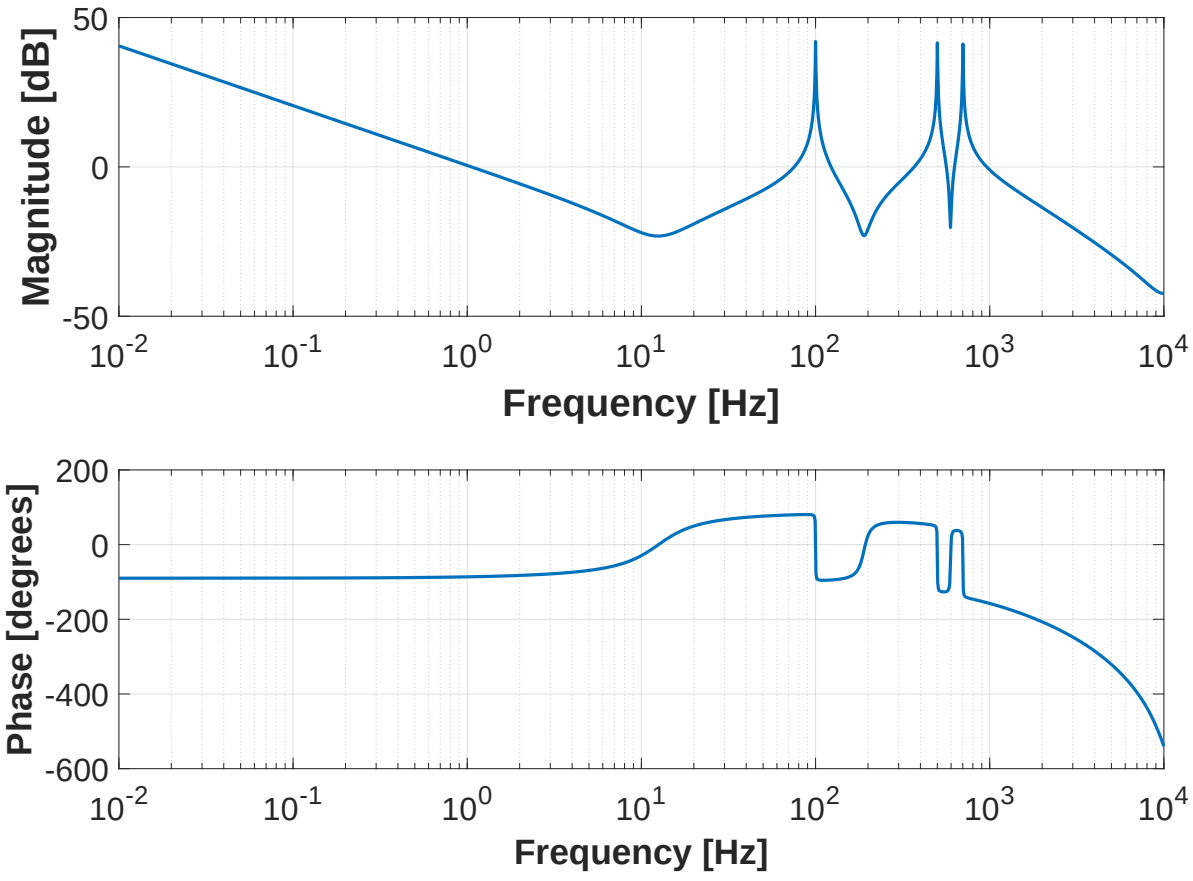
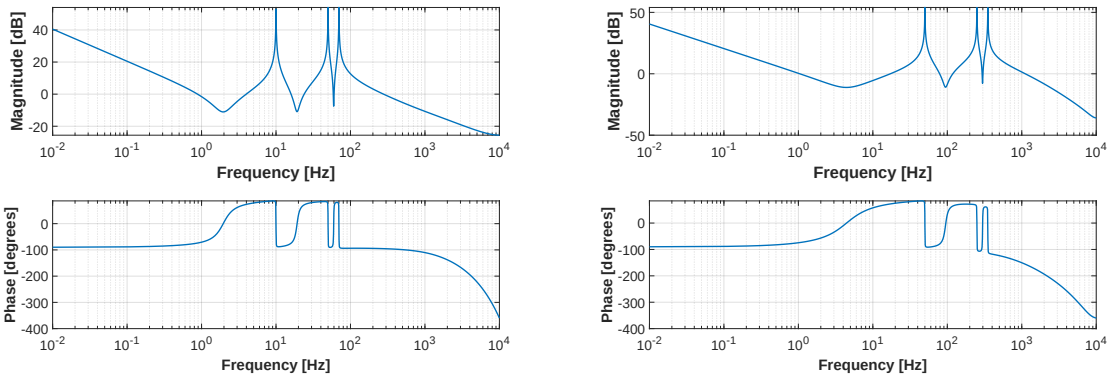


Figure 6.8: Bode plot of PIR controller tuned at fundamental frequency - 100Hz

The bode plots for PIR controllers with fundamentral tuned to 10Hz and 50Hz are shown for reference in 6.9.



(a) Bode plot of PIR controller tuned at fundamental frequency - 10Hz

(b) Bode plot of PIR controller tuned at fundamental frequency - 50Hz

Figure 6.9: Bode plot of PIR controller tuned at 10 Hz and 50 Hz fundamental frequencies

DC link balancing of NPC converters

DC link balancing is essential for NPC operation. A modified balancing method is implemented based as outlined in chapter 5. During fault operation, the converters are operated in single-phase mode and the zero sequence injection is not available for balancing.

6.4.2 Simulated responses of the drive system

The modelled controller performance in the healthy case is validated by applying a 10A step load in the current setpoint. The controller performance is showin in 6.10.

The simulated fault responses of the drive system are of main interest. The transition to single-phase fault as well as dual phase fault are simulated. In simulation, fault injection is achieved by switching in a high value series resistance. In experiments, the fault injection is achieved by turning gate signals off for one of the phases. The fault recovery behaviour in experiments is to trip and restart even though a seamless transfer is possible. The trip restart is chosen as the phase reference would be sub-optimal for maximizing torque and it could potentially lead to controller instability as the remaining phase controllers are in contention to regulate the phase current. Minimal disruption is still achieved as demonstrated by the transient response of the faulty current controllers. A fault detection time of 5ms is simulated. The controllers seamlessly transition to

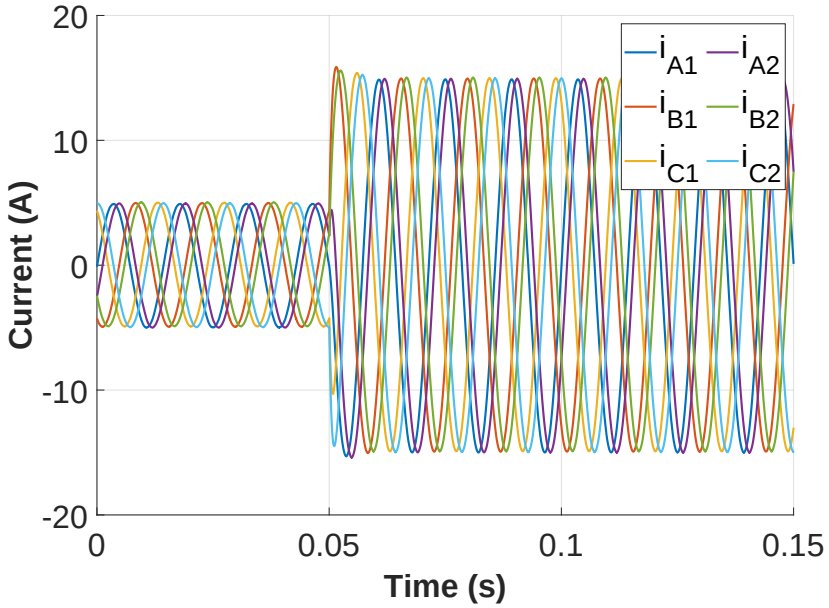
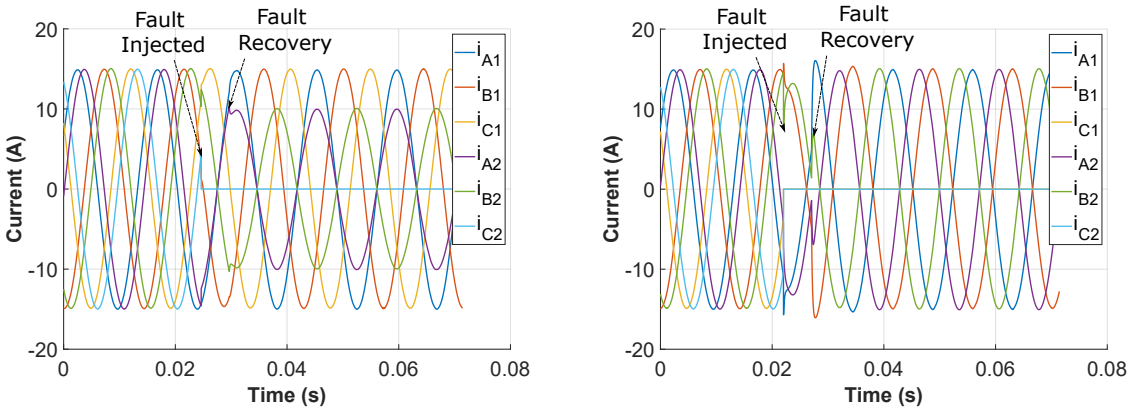


Figure 6.10: Simulated step response of current controllers

the fault mode operation. In practical implementation, the fault transient may trip the converters. The recovery from fault state is shown in the experimental results. The fault responses shown in Fig. 6.11 are simulated at the same conditions as the experimental setup as summarized in Tab. 6.1



(a) Simulated phase currents with phase C2 open

(b) Simulated phase currents with phases C1 and C2 open

Figure 6.11: Simulated phase faults

6.5 Firmware architecture

The software architecture for a three level neutral point clamped (3L-NPC) converter is presented in this section. The software is built in an object oriented manner, for instance measurements, controller outputs etc. are grouped together in "C" structures, lending itself capable of easy addition of control loops to be executed in parallel. The control board is built around a C2000 (F28377D) MCU and an Intel Max V Field Programmable Gate Array (FPGA). FPGA is added to expand the PWM pinout as the MCU is limited to 24 native PWM output pins.

6.5.1 C2000 architecture

F28377D has two CPU cores along with 2 control law accelerator (CLA) cores. C2000 could be clocked at frequencies up to 200 MHz ensuring sufficient bandwidth to support parallel execution of multiple control loops. Reference would be made to Technical Reference Manual (TRM) of F28377D [113] where appropriate to describe functionality of the controller code. F28377D has 24 Pulse Width Modulation (PWM) outputs which can be independently controlled by counter compare registers. As each 3L-NPC converter requires 12 PWM signals, it is possible to control two 3L-NPC converters without pin expansion of F28377D. For measurement purposes, 20 Analog to Digital Converter (ADC) input channels are available in F28377D split over 4 individual ADC modules.

6.5.2 Control platform for multi-phase machine

In order to control more than two 3L-NPC converters, pin expansion is achieved by incorporating a FPGA module on the control board. FPGA module is interfaced with F28377D device via the External Memory Interface (EMIF) bus, which is a TI specific interface for inter-processor communication. An external Serial Peripheral Interface (SPI) interfacedADC module is included on control board to measure analog signals from additional converters. F28377D is able to execute at least 4 independent converter control loops within the execution time limits at 20kHz switching frequency. Key software and

hardware components of the control platform is showin in 6.12.

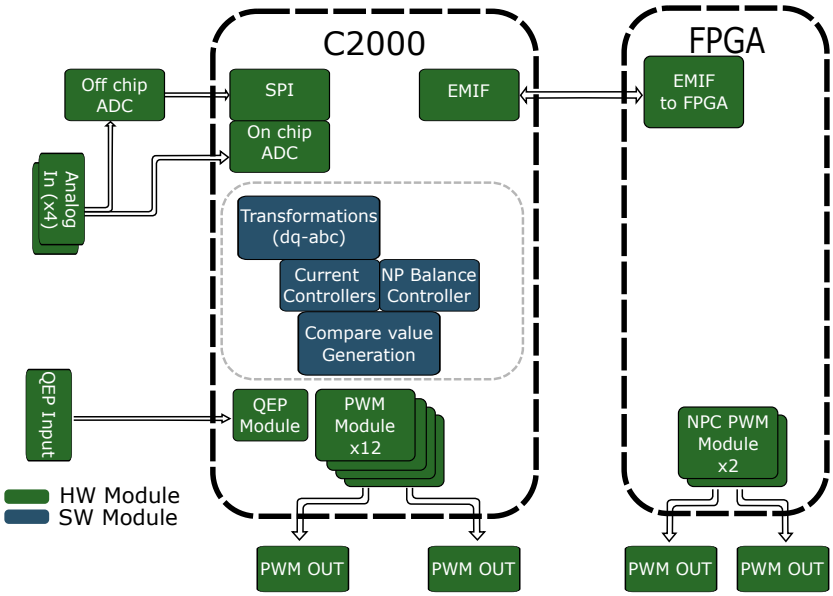


Figure 6.12: Multi converter controller platform

The C2000 firmware is written in the foreground-background architecture. The background process, which is the infinite loop, initializes the MCU setting up the various peripherals, calibrating the ADC channels and hands over control to the state-machine in the infinite loop. The state-machine handles events such as fault injection, data logging and communication with a host computer via serial port. The foreground process which is the Interrupt Service Routine (ISR) is shown in 6.13. The foreground process is triggered by the End of Conversion (EOC) interrupt from the ADC modules.

The control platform is controlled via serial port to send commands. The state-machine triggers a data-logger in the ISR and the data is transferred back to the host via the serial interface.

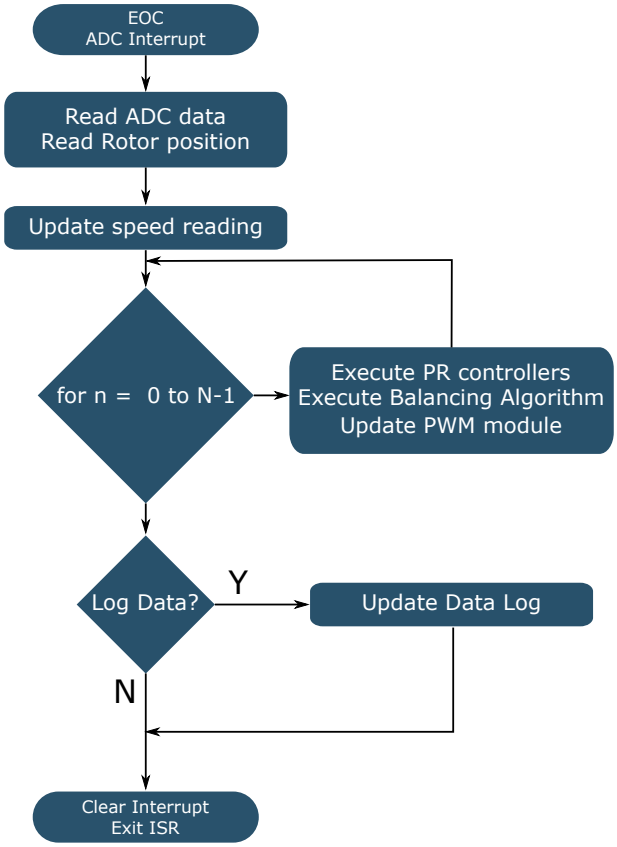


Figure 6.13: Control Loop execution for multiple converters

6.6 Experimental setup

The experimental validation is carried out on a dual neutral 6 phase IPM machine. 3L-NPC converter prototypes developed based on "FS3L30R07W2H3F_B11" power module from Infineon rated at 650V and 30A are used as the drive converters. The control code is run on the controller platform described above. The controller for each three-phase set is run independent from each other. The experimental setup is shown in Fig. 6.14.

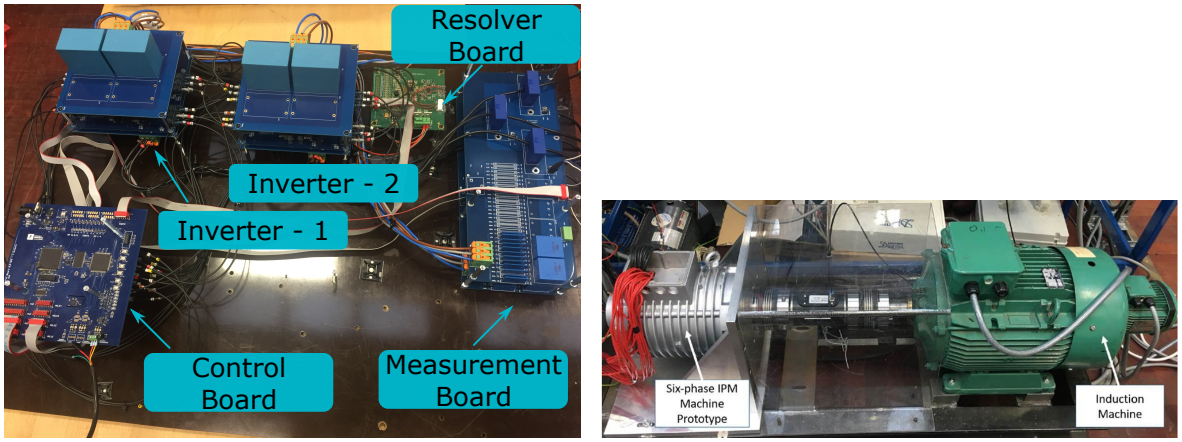
Key parameters of interest of the experimental setup are summarized in Tab. 6.1.

Step response of the drive system in healthy condition is measured to verify controller tuning and is shown in Fig. 6.15

The back EMF voltage waveform is shown in fig. 6.16. The presence of higher order harmonics especially 5th and 7th are evident from the back emf waveform.

The effectiveness of harmonic control is demonstrated in the harmonic spectrum of phase currents as shown in fig.6.17.

The waveforms when phase sets are healthy are not included for brevity. The single-



(a) 3LNPC Drive Prototype (b) IPM Machine Setup

Figure 6.14: NPC based Drive Setup

Table 6.1: Converter/Machine/PIR tuning parameters

DC link Voltage	270V
DC link Capacitance	101.1uF
Machine pole pairs	4
Machine operating speed	1050 rpm
λ_m	0.0923 V/rad/s
Converter Switching Frequency	20 kHz
Datalogger Sampling Frequency	10 kHz
Torque Datalogger Sampling Frequency	100 Hz
K_P	0.42
K_R	750
K_I	10
K_{damp}	0.05

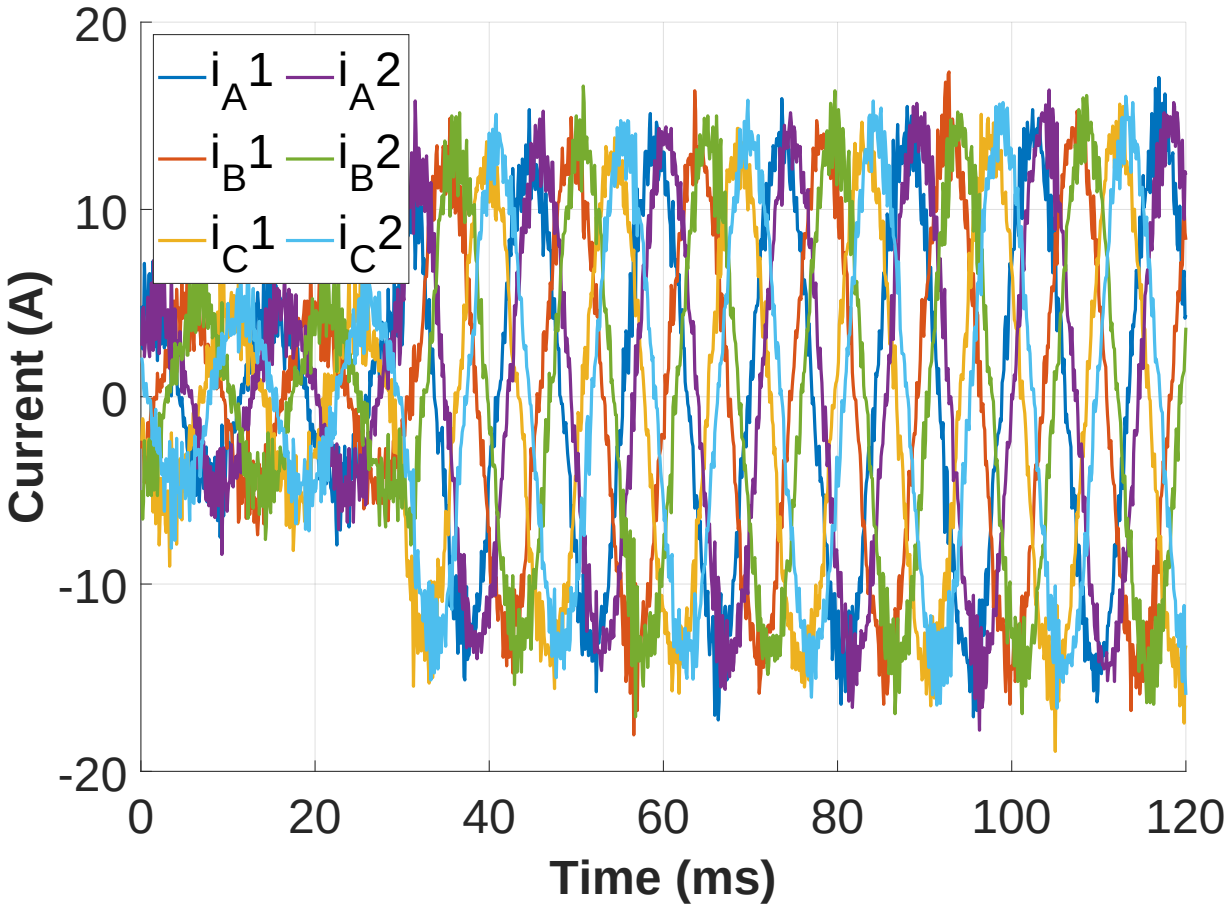


Figure 6.15: Transient response of healthy drive system

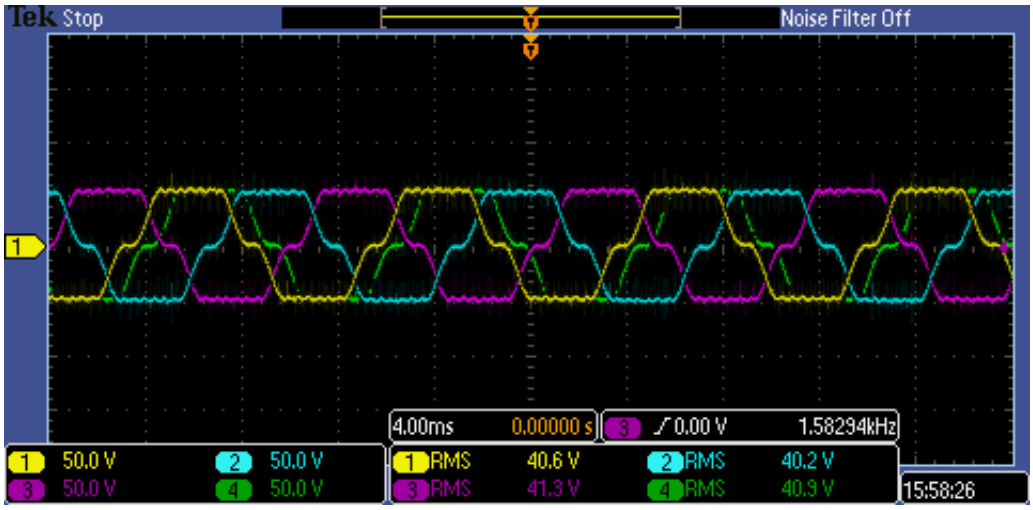


Figure 6.16: Machine terminal back emf. Unloaded voltages of phases A1, B1, C1 and A2 windings are shown

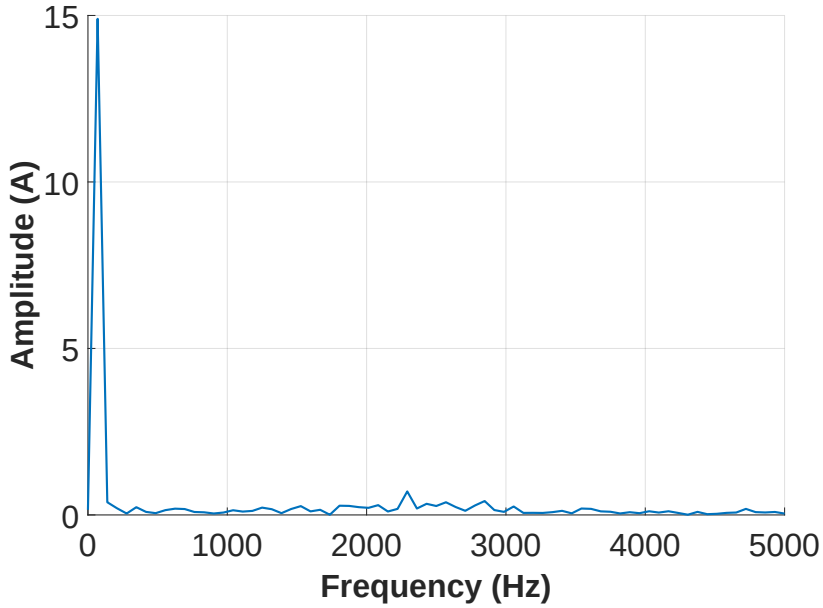
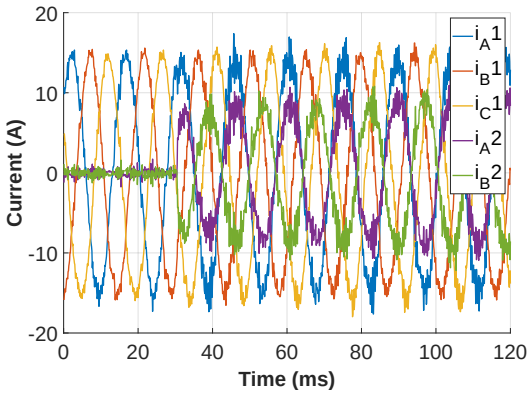


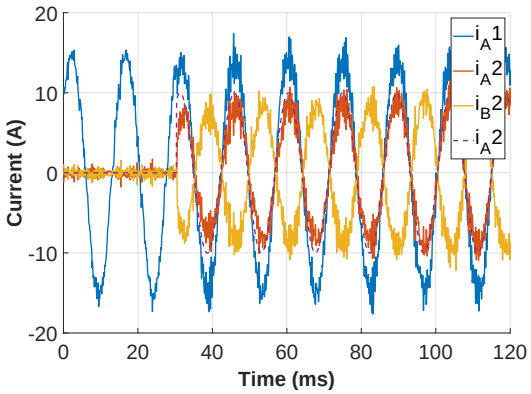
Figure 6.17: Harmonic spectrum of experimentally measured phase currents

phase open fault is considered first. As the fault develops, one phase set goes offline. The healthy winding set continues to operate and provides half the torque to the machine. The reconfiguration in control code for the faulty winding set is straightforward as shown in Fig. 6.5.

The current waveforms as well as the reference tracking is shown in Fig. 6.18. The healthy winding set current reference is set to 15A while the single-phase set is programmed with a current reference of 10A.



(a) Phase currents with phase C2 open

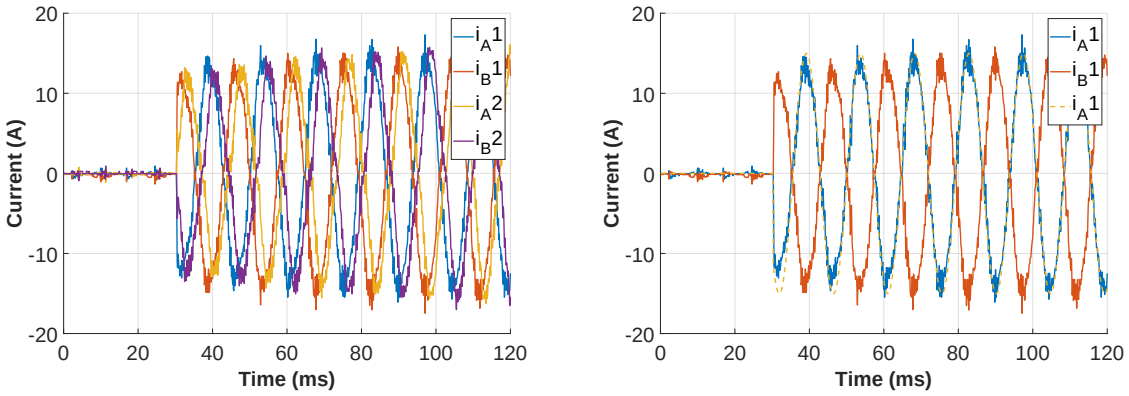


(b) Reference tracking in single-phase fault

Figure 6.18: single-phase open fault mode current control

Dual phase fault where phase C1 and phase C2 suffers open phase fault is shown in

Fig. 6.19. The current reference for each single-phase set is set to 15A.



(a) Phase currents with phases C1 and C2 open (b) Reference tracking in dual phase fault

Figure 6.19: Dual phase open fault mode control

A comparison of torque developed in the healthy, single-phase fault and dual phase fault is shown in Fig. 6.20. As the sampling frequency of the torque meter is only 100 Hz, the double harmonic component in the torque is not visible on the plot. The low frequency torque ripple (approximately 0.1 Hz frequency) in the case of dual phase fault is due to weak mechanical coupling in the test setup at low torque values. Theoretically predicted torque values based on the reference currents following Eqs. (6.12), (6.18) and (6.23) are listed in Tab. 6.2.

Table 6.2: Torque comparison

Operating mode	**Predicted Torque**	**Measured Torque**
Healthy - I_{Ph} - 15A	16.61 Nm	16.3 Nm
single-phase fault Healthy I_{Ph} - 15A single-phase set I_{Ph} - 10A	11.5 Nm	10.48 Nm
Dual phase fault I_{Ph} - 15A	4.8 Nm	3.5 Nm

Transient conditions - speed or load changes are not considered. This work focussed on the current control loops. Speed and load disturbances result in a setpoint change to the current controller. In fault modes, the system gain for the outer speed loop changes as effective torque is lower. This would have implications on achieving speed setpoints.

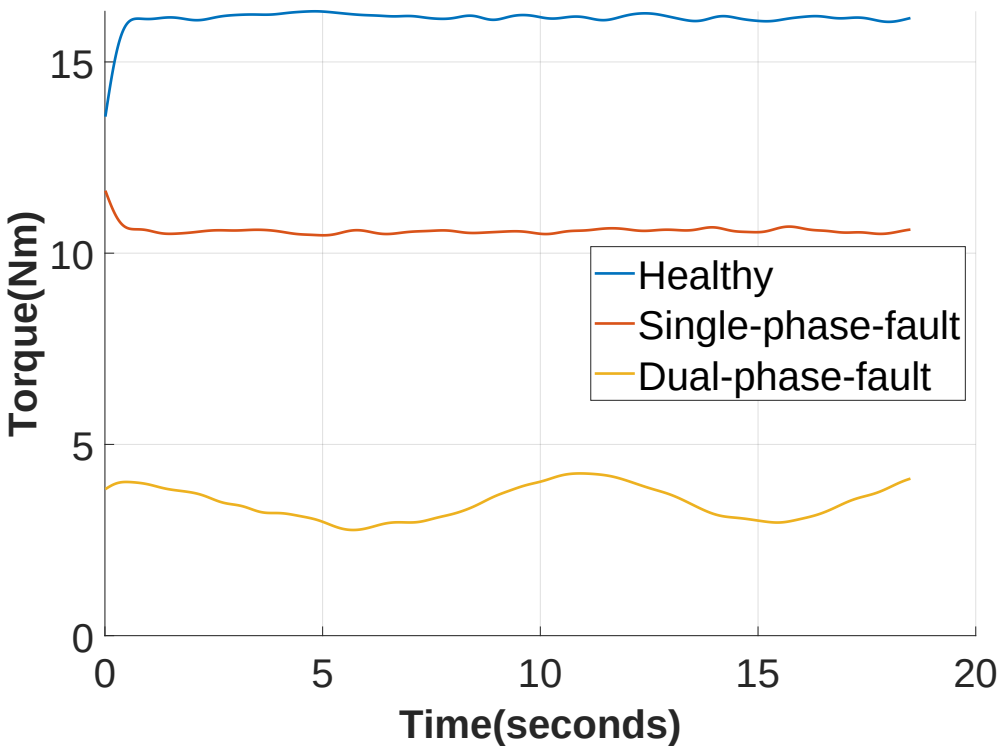


Figure 6.20: Torque comparison across modes

However, within the current limits of the drive converters, the current loop will track the reference and the dynamic performance is demonstrated with the step responses.

6.7 Summary

Two fault mode control schemes to enable limp home functionality for multi three phase machines are presented. The machine model in ABC domain accounting for inter-winding coupling is used to develop current control scheme capable of fault mode operation. The inter-winding coupling can be accounted for by knowledge of current setpoints, however the transient performance would be affected during step or load changes. Control structure using PIR controllers are presented. Using the fault mode machine model, it is shown that fault mode controller reconfiguration can be performed with no modifications to controller structure. Only tuning modification to account for system gain variation is required for fault mode operation. PIR controllers enable harmonic cancellation similar to VSD control while providing independent controllers per phase. The suitability of PIR controllers for fault modes with single and double open phase fault operation is validated with 3L-NPC inverters.

Chapter 7

Conclusions

In this doctoral thesis, design of aerospace power converters was approached from a reliability and availability standpoint. The motivation was to propose design guidelines for power converters based on the aerospace operating requirements. Further to reliability, availability was also included as a key design target. The goal was to identify topologies suited for high power high voltage drive converters to realize future aircraft architectures.

With respect to availability the target was to propose fault tolerant operation such that excessive redundancy in design can be avoided. A limp home feature would provide useful operation even after a fault and improve system availability.

7.1 Conclusions

The aim of this thesis was to investigate reliability bottlenecks for aerospace power converters and generate design guidelines for converter designers to meet the reliability and availability requirements of aviation.

The case study on aerospace reliability brought out the need to account for random failures in reliability assessment. Suitability of SiC modules for future designs were also demonstrated. It can be concluded that for future high voltage designs to enable MEA and AEA SiC devices would be utilized. The study on availability involved investigating fault reconfiguration options available in multi three phase machines. A control scheme was developed to achieve a limp-home functionality under fault scenario. It can be

concluded from the ABC domain controller implementation that the developed control scheme enables fault operation with trivial changes to the controller which would help in meeting the certification requirements for firmware.

7.1.1 Key results from the work

1. Topology and device selection guidelines for aircraft converters.

   A case study was carried out to understand the reliability performance of 2L and 3L-NPC topologies at various DC distribution system voltage levels. The case study considered both wear-out and cosmic ray induced failures to generate reliability figures.

   The case study results show that cosmic ray failures will dominate high voltage aerospace converters unless significant voltage derating is included in the case of silicon power semiconductors. As expected, wear-out reliability performance is better at higher system voltages. In the case of high voltage converters, WBG devices are a natural choice due to their increased robustness against cosmic ray failures. If silicon devices are to be utilized at high system voltages, multi-level topologies are necessary to mitigate the impact of cosmic ray failures.

   (a) Mitigation controls against CR failures

   Mitigation against CR failures is considered by both voltage and thermal control options and it is demonstrated that dynamic voltage control is the appropriate mitigation measure against CR failures.

2. ABC domain control of multi-phase machines enabling fault tolerance,

   Multi-level topologies was identified in the case study as a potential solution for high power aerospace drives. Cosmic ray failure mode highlighted the necessity for design for availability especially in safety critical application. One of the design pathways for availability is to utilize multi phase and in particular multi three phase machines. An ABC domain control for multi three phase machine was implemented to utilize fault tolerance capability of multi-level topologies.

The control development accounts for inter winding flux coupling and it relies on the knowledge of current setpoint for each winding sets to arrive at controller tuning. Two fault mode operations are simulated and experimentally validated. In order to operate the 3L-NPC converter in fault mode, a balancing scheme was developed which can seamlessly transition to fault mode operation. Machine equivalent models for single phase open and double phase open fault cases are developed and torque generation in both fault cases are theoretically predicted and experimentally validated.

7.2 Suggested Future works

There are many topics to be explored further in the reliability domain. The fundamental aspects of PoF based reliability prediction have been fairly well established.

The following are suggestions for future research topics to address the needs for relaibility assessment for aerospace power electronics :

1. Standard aerospace mission profile

   In line with drive profile for road vehicles, flight patterns for aerospace reliability/-efficiency assessment is necessary for design of aerospace systems. Standardization efforts in this direction is suggested as a research topic. A difference between road vehicles and aerospace design is the reliability and availability requirements which forces designers to consider worst case operational requirements for standard design.

2. Assesment of suitability of SiC devices for aerospace applications

   SiC devices are increasingly adopted in power electronics. However, reliability models for SiC devices are not well established and should be explored to bring about standard lifetime models. Another area to study is the effect of thermal dependence on cosmic ray failures of SiC devices with particle beams to establish thermal controllers for SiC based converters.

3. Fault tolerance using multi three phase multi level converters

   This work has shown the advantages of multi three phase systems. The usage of

multi level topologies, in particular three level topologies to make use of redundant switch states to achieve fault tolerant performance is an area to study further. Combination of fault prediction using reliability models and application of thermal controllers to prolong system lifetime is another topic to consider.

(a) Control of multi three phase machines

In the case of multi-phase machines, research is ongoing to improve torque performance by possibly utilizing harmonics of the fundamental. A research effort in that direction was also supported using the experimental setup developed for this thesis [114]. The harmonic performance under fault conditions were not considered beyond implementing PR controllers in this work. It is a possible research area to improve the torque performance further under fault conditions. Finally Model predictive controllers which can handle healthy and fault mode operation of multi three phase systems would be useful to complement the results from this work.

PR controller tuning is an important aspect for enabling fault tolerant control scheme proposed in this work. Robust and simplified tuning methods for PR controllers, following Nyquist stability criteria is an important area to explore further.

Appendix A

Component Sizing

Table A.1: DC link capacitance for 2L topology

DC Link Voltage	Estimated Capacitance	Manufacturer Part number	Device Rating	Number of Caps
270V	684 uF	B32778J4487K000	480 uF, 450V	2
540V	171 uF	B32778G8107000	100 uF, 800V	2
810V	76 uF	B32778J0207K000	200 uF, 1100V	1

Table A.2: Semiconducor selection for 2L topology

DC Link Voltage	Manufacturer Part number	Device Rating	Die Area
270V	SKM400GB07E3	650V-400A	$1.99cm^2$
540V	SKM200GB12V	1200V-200A	$1.93cm^2$
810V	SKM150GB12T4	1200V-150A	$1.42cm^2$
810V	CAS120M12BM2	1200V-120A	-

Table A.3: DC link capacitance for 3L-NPC topology

DC Link Voltage	Estimated Capacitance	Manufacturer Part number	Device Rating	Number of Caps
270V	684 uF	B32778J4487K000	480 uF, 450V	6
540V	171 uF	B32778J4487K000	480 uF, 450V	2
810V	76 uF	B32778J5117K000	110 uF, 540V	4

Table A.4: Semiconducor selection for 3L topology

DC Link Voltage	**Manufacturer Part number**	**Device Rating**	**Die Area**
270V	SEMiX405MLI07E4	650V-400A	$1.99cm^2$
540V	SEMiX205MLI07E4	650V-200A	$0.99cm^2$
810V	SEMiX155MLI07E4	650V-150A	$0.76cm^2$

Appendix B

NPC Balancing Algorithms

B.1 Per phase based NPC balancing - proposed

```
inline void neutralpoint_current_calculation(INV_MEASUREMENTS *inv_meas
    ){
     Uint16 phase_num;
     inv_meas->Io = inv_meas->C*inv_meas->Fsw*(inv_meas->Vdc[
    DCLINK_LOWER] - inv_meas->Vdc[DCLINK_UPPER]);
     inv_meas->Io_error = inv_meas->Io;
     inv_meas->Io_actual = 0.0;
     for (phase_num=PHASE_A;phase_num<Num_Phases;phase_num++){
              // CRITICAL STEP - Saturate Modulation signals to be in
    range [-1,1]
         //inv_meas->Mod[phase_num] = _IQsat(inv_meas->Mod[phase_num],
    inv_meas->UmaxP,inv_meas->UminN);
              // Vmod is positive
         if (inv_meas->Mod[phase_num] > 0){
              inv_meas->vip[phase_num] = inv_meas->Mod[phase_num];
              inv_meas->vin[phase_num] = 1;
              inv_meas->duty_np[phase_num] = 1- inv_meas->vip[phase_num];
         }
                  // Vmod is negative
         else{
              inv_meas->vip[phase_num] = 0; // keep a small value as per
```

Algorithm 1 Offset Generation for Balancing

for $x = a, b, c$ **do**
  $m_{xoff} \leftarrow 0$
  {/* Only run algorithm if NP duty cycle is more than a threshold*/}
  if $d_{xNP} > 0.5$ **then**
    {/* If NP current error is positive →
    more positive NP current/less negative NP current is required
    NP positive current cannot be increased (neutral point dutycycle can only be reduced)
    Only solution is to reduce negative current flow
    Opposite action when NP current error is negative*/}
    if $i_{o-err} > 0$ **then**
      {/* Minimal balancing effect provided/unbalance caused by low currents*/ }
      if $i_x < (-0.5)$ **then**
        $m_{xoff} \leftarrow 0.0 - \frac{i_{o-err}}{i_x}$
      else
        {/* No Correction possible*/}
      end if
    else
      if $i_x > (0.5)$ **then**
        $m_{xoff} \leftarrow 0.0 - \frac{i_{o-err}}{i_x}$
      else
        {/* No Correction possible*/}
      end if
    end if
    if $m_{xoff} > m_{xoff-max}$ **then**
      {/* Saturate the offset to meet duty cycle limits*/ }
      $m_{xoff} \leftarrow m_{xoff-max}$
    end if
    $i_{o-err} \leftarrow i_{o-err} + (i_x \cdot m_{xoff})$ {/* i_{o-err} is updated for next phase*/ }
    $m_{xoff} \leftarrow (0.5 \cdot m_{xoff})$ {/* Offset applied equally to m_{xP} and m_{xN} - Eq. (5.9)*/ }
    $m_{xP} \leftarrow m_{xP} + m_{xoff}$
    $m_{xN} \leftarrow m_{xN} - m_{xoff}$
  end if
end for

```
  TI TRM
18            inv_meas->vin[phase_num] = (1+inv_meas->Mod[phase_num]);
19            inv_meas->duty_np[phase_num] = inv_meas->vin[phase_num];
20          }
21          inv_meas->vipoff[phase_num] = inv_meas->vip[phase_num];
22          inv_meas->vinoff[phase_num] = inv_meas->vin[phase_num];
23          inv_meas->Io_actual += (inv_meas->Iph[phase_num] * inv_meas->
  duty_np[phase_num]);
```

```
24      }
25      inv_meas->Io_error -= inv_meas->Io_actual;
26  }
```

Listing B.1: Helper Function for pre-calculation of NP current

```
1   inline void neutralpoint_balancing_offset_calculation(INV_MEASUREMENTS
        *inv_meas, Uint16 active_phases){
2       Uint16 phase_num;
3       _iq duty_offset = 0.0;
4       _iq duty_offset_max = 0.0;
5       for (phase_num = PHASE_A;phase_num < active_phases;phase_num++){
6           duty_offset = 0.0;
7           if (inv_meas->duty_np[phase_num] > 0.5){
8               duty_offset_max = 0.5 - 0.04;
9               /*
        ************************************************************************

10              * If error is positive => more positive current or less
        negative current
11              * More positive current is not possible (Cannot increase
        neutral duty)#
12              * Only solution is to reduce negative current flow
13              * Opposite case when error is negative
14
        ************************************************************************
        */
15              if (inv_meas->Io_error > 0){
16                  if (inv_meas->Iph[phase_num] < -0.5){
17                      duty_offset = 0.0 - (inv_meas->Io_error/inv_meas->
        Iph[phase_num]);
18                  }
19                  else{
20                  } // No correction possible as duty at NP must increase
21              }
22              else{ // Ioerror < 0
```

```
23                 if (inv_meas->Iph[phase_num] > 0.5){
24                     duty_offset = 0.0 - (inv_meas->Io_error/inv_meas->
   Iph[phase_num]);
25                 }
26                 else{
27                 }// No correction possible as duty at NP must increase
28             }
29             if (duty_offset > duty_offset_max){
30                 duty_offset = duty_offset_max;
31             }
32         }
33         inv_meas->Io_error += (duty_offset * inv_meas->Iph[phase_num]);
34         duty_offset = 0.5*duty_offset;
35         inv_meas->vipoff[phase_num] += duty_offset;
36         inv_meas->vinoff[phase_num] -= duty_offset;
37     }
38 }
```

Listing B.2: Per phase balancing offset generation

```
1 inline void modulation_balancing_proposed(INV_MEASUREMENTS *inv_meas,
   INV_PORTS *inv, Uint16 period, Uint16 deadband, Uint16 active_phases
   ){
2     neutralpoint_current_calculation(inv_meas);
3     neutralpoint_balancing_offset_calculation(inv_meas, active_phases);
4     NPC_DSPWM_Modulation(inv_meas, inv, period, deadband);
5 }
```

Listing B.3: Proposed balancing wrapper function

B.2 Literature NPC balancing [1]

```
1 inline void neutralpoint_balance_modulation_precalculation(
   INV_MEASUREMENTS *inv_meas, Uint16 phase_num){
2
3         /* Vip and Vin computation and saturate to limits*/
```

```
4     inv_meas->vip[phase_num] = _IQsat((_IQdiv2(inv_meas->Mod[phase_num]
      - inv_meas->vmin)),inv_meas->UmaxP,inv_meas->UminP);
5     inv_meas->vin[phase_num] = _IQsat((_IQdiv2(inv_meas->Mod[phase_num]
      - inv_meas->vmax)),inv_meas->UmaxN,inv_meas->UminN);
6
7         /* da computation*/
8     inv_meas->d[phase_num]       = fabs(inv_meas->vin[phase_num] -
     inv_meas->vip[phase_num] + 1);
9         /* pre computation of variables used in offset*/
10    inv_meas->dmpyIph[phase_num] = 0.00 - (inv_meas->d[phase_num] *
     inv_meas->Iph[phase_num]);
11    inv_meas->dmpyIo[phase_num]  = _IQmpy(inv_meas->d[phase_num],
     inv_meas->Io);
12    inv_meas->signoff[phase_num] = ((_IQmpy(inv_meas->Io,inv_meas->Iph[
     phase_num])) > 0) ? -1 : 1; // TO BE CHECKED WITH RESPECT TO PHASE
     CURRENT MEASUREMENT
13 }
```

Listing B.4: Helper Function for pre-calculation

```
1  inline void neutralpoint_balance_modulation_offset_generation(
      INV_MEASUREMENTS *inv_meas, Uint16 phasei, Uint16 phasej, Uint16
      phasek){
2
3     volatile float tmp = 0.00000;
4  /* Check if either vip or vin is clamped*/
5     if ((inv_meas->vip[phasei]==0)||(inv_meas->vin[phasei]==0)){
6         inv_meas->vipoff[phasei] = _IQsat(inv_meas->vip[phasei],
      inv_meas->UmaxP, inv_meas->UminP);
7             // CAREFUL - Vin is shifted from [-1,0] to [0,1]. SHIFT the
      limits too accordingly
8         inv_meas->vinoff[phasei] = _IQsat((1+inv_meas->vin[phasei]),(1+
     inv_meas->UmaxN), (1+inv_meas->UminN));
9     }
10    else{
11        tmp = inv_meas->dmpyIph[phasej] + inv_meas->dmpyIph[phasek];
```

```
12          if (fabs(tmp) < 0.00001){
13              tmp = 0.00001;
14          }
15              /* Voff and sign computation*/
16          inv_meas->off[phasei] = fabs(_IQdiv2(_IQdiv(inv_meas->dmpyIo[
    phasei],tmp)));
17          inv_meas->off[phasei] = (inv_meas->signoff[phasei] * inv_meas->
    off[phasei]); // (inv_meas->signoff[phasei] >= 0) ? inv_meas->off[
    phasei] : (_iq)(0.0-inv_meas->off[phasei])
18              /* Voff magnitude check against conditions*/
19              /* 0<= Vap <= 1 -1 <= Van <= 0 and Van + 1 >= Vap*/
20          if (inv_meas->signoff[phasei] > 0){
21              inv_meas->offmax[phasei] = _IQdiv2(inv_meas->vin[phasei] -
    inv_meas->vip[phasei] + 1);
22              inv_meas->off[phasei] = (inv_meas->off[phasei] <= inv_meas
    ->offmax[phasei])? inv_meas->off[phasei] : inv_meas->offmax[phasei];
23          }
24          inv_meas->off[phasei] = _IQsat((inv_meas->vip[phasei]+inv_meas
    ->off[phasei]), inv_meas->UmaxP, inv_meas->UminP) - inv_meas->vip[
    phasei];
25          inv_meas->off[phasei] = inv_meas->vin[phasei] - _IQsat((
    inv_meas->vin[phasei]-inv_meas->off[phasei]), inv_meas->UmaxN,
    inv_meas->UminN);
26
27          inv_meas->vipoff[phasei] = _IQsat((inv_meas->vip[phasei] +
    inv_meas->off[phasei]),inv_meas->UmaxP, inv_meas->UminP);
28              // CAREFUL - Vin is shifted from [-1,0] to [0,1]. SHIFT the
     limits too accordingly
29          inv_meas->vinoff[phasei] = _IQsat((1 + inv_meas->vin[phasei] -
    inv_meas->off[phasei]),(1+inv_meas->UmaxN), (1+inv_meas->UminN));
30      }
31  }
```

Listing B.5: Helper Function to generate offsets for each phase

```
1 inline void NPC_DSPWM_Modulation(INV_MEASUREMENTS *inv_meas, INV_PORTS
```

```
*inv, Uint16 period, Uint16 deadband){
 Uint16 phase_num;
 for (phase_num = PHASE_A; phase_num < Num_Phases; phase_num++){

     /* CRITICAL STEP - Saturate Modulation signals to be in range [0,Max] for pos [Min,1] for Neg {Negative modulation is shifted by 1}*/
     inv_meas->vipoff[phase_num] = _IQsat((inv_meas->vipoff[phase_num]),inv_meas->UmaxP, inv_meas->UminP);
     inv_meas->vinoff[phase_num] = _IQsat((inv_meas->vinoff[phase_num]),(1+inv_meas->UmaxN), (1+inv_meas->UminN));

         // An error can be reported if the below check is executed
     if (inv_meas->vinoff[phase_num] < inv_meas->vipoff[phase_num]){
         inv_meas->vinoff[phase_num] = inv_meas->vipoff[phase_num];
     }
         /* Translate to fraction of time period */
     inv_meas->vipoff[phase_num] *= period;
     inv_meas->vinoff[phase_num] *= period;

     if(inv_meas->vipoff[phase_num] < (deadband+1)){

Epwm_ActionQualifier_OutA_Software_Force_Low_continuous_Activate(inv->pwm_cmp_info[phase_num][IGBTs_S1_S3].pwm_num); // S1 turned off, S3 turned on
     }
     else{

Epwm_ActionQualifier_OutA_Software_Force_continuous_Deactivate(inv->pwm_cmp_info[phase_num][IGBTs_S1_S3].pwm_num);
     }
     if(inv_meas->vinoff[phase_num] > (period - deadband-1)){
             // Inner switch turned on fully, outer switch turned off

```

```
    Epwm_ActionQualifier_OutA_Software_Force_High_continuous_Activate(
    inv->pwm_cmp_info[phase_num][IGBTs_S2_S4].pwm_num); // S2 turned on,
     S4 turned off
26          }
27          else{
28
    Epwm_ActionQualifier_OutA_Software_Force_continuous_Deactivate(inv->
    pwm_cmp_info[phase_num][IGBTs_S2_S4].pwm_num);
29          }
30
31          Epwm_CMPA_Update(inv->pwm_cmp_info[phase_num][IGBTs_S1_S3].
    pwm_num, inv_meas->vipoff[phase_num]);
32          Epwm_CMPA_Update(inv->pwm_cmp_info[phase_num][IGBTs_S2_S4].
    pwm_num, inv_meas->vinoff[phase_num]);
33
34      }
35  }
```

Listing B.6: Hardware Interfacing Function to apply signals to PWM module

```
1  inline void modulation_balancing_lit(INV_MEASUREMENTS *inv_meas,
    INV_PORTS *inv, Uint16 period, Uint16 deadband){
2      Uint16 phase_num;
3      modulation_max_min_dc_midpoint_current_calculator(inv_meas);
4          // pre-calculation must be finished for all phases
5          // before execution of remaining calculations
6      for (phase_num = PHASE_A; phase_num < Num_Phases; phase_num++){
7          neutralpoint_balance_modulation_precalculation(inv_meas,
    phase_num); // calculates the variables for the balancing (duty *
    Iphase)
8      }
9          // Neutral point current is impacted by all three phases
10         // precalc values from all phases in winding set required in
    final offset calculation
11     for (phase_num = PHASE_A; phase_num < Num_Phases; phase_num++){
12         Uint16 next_phase[2];
```

```
13          next_phase[0] = ((phase_num + 1) > 2) ? ((phase_num + 1) -3) :
    (phase_num + 1);
14          next_phase[1] = ((phase_num + 2) > 2) ? ((phase_num + 2) -3) :
    (phase_num + 2);
15          neutralpoint_balance_modulation_offset_generation(inv_meas,
    phase_num,next_phase[0],next_phase[1]);
16      }
17      NPC_DSPWM_Modulation(inv_meas, inv,period, deadband);
18  }
```

Listing B.7: Literature balancing wrapper function

Bibliography

[1] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen, and M. Corbalan, "Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 305–314, 2009.

[2] *Global Market Forecast: Global Networks, Global Citizens 2018–2037*, https://www.airbus.com/en/products-services/commercial-aircraft/market/global-market-forecast, Airbus, 2018, [Online] Accessed: November 30 2020.

[3] V. Madonna, P. Giangrande, and M. Galea, "Electrical power generation in aircraft: Review, challenges, and opportunities," *IEEE Transactions on Transportation Electrification*, vol. 4, no. 3, pp. 646–659, Sep. 2018.

[4] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-board microgrids for the more electric aircraft—technology review," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5588–5599, July 2019.

[5] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application Manual Power Semiconductors*, SEMIKRON International GmbH, 2015.

[6] K. Ma, N. He, M. Liserre, and F. Blaabjerg, "Frequency-domain thermal modeling and characterization of power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7183–7193, Oct 2016.

[7] M. Ikonen, "Power cycling lifetime estimation of igbt power modules based on chip temperature modeling," Ph.D. dissertation, Lappeenranta University of Technology, 2012.

[8] M. Liserre, G. Buticchi, J. I. Leon, A. Marquez Alcaide, V. Raveendran, Y. Ko, M. Andresen, V. G. Monopoli, and L. Franquelo, "Power routing: A new paradigm for maintenance scheduling," *IEEE Industrial Electronics Magazine*, vol. 14, no. 3, pp. 33–45, 2020.

[9] M. Andresen, M. Liserre, and G. Buticchi, "Review of active thermal and lifetime control techniques for power electronic modules," in *2014 16th European Conference on Power Electronics and Applications*, 2014, pp. 1–10.

[10] "Air Transport Action Group - Facts and Figures," https://www.atag.org/facts-figures.html, September 2020, [Online] Accessed: November 30 2020.

[11] *European Aviation Environmental Report*, https://www.eurocontrol.int/sites/default/files/2019-06/eaer-2019_0.pdf, European environment agency, 2019, [Online] Accessed: November 30 2020.

[12] *Jet Fuel Price Monitor*, https://www.iata.org/en/publications/economics/fuel-monitor/, IATA, 2021, [Online] Accessed: December 5 2021.

[13] *IATA TECHNOLOGY ROADMAP 2013*, International Air Transport Association, 2013.

[14] M. Lukic, P. Giangrande, A. Hebala, S. Nuzzo, and M. Galea, "Review, challenges and future developments of electric taxiing systems," *IEEE Transactions on Transportation Electrification*, pp. 1–1, 2019.

[15] B. Sarlioglu and C. T. Morris, "More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 1, pp. 54–64, 2015.

[16] "10,000 meters above sea level – Motor running," https://drive.tech/en/stream-content/electric-motors-in-passenger-aircrafts, 2022, [Online] Accessed: February 10 2022.

[17] H. Chung, H. Wang, F. Blaabjerg, and M. Pecht, *Reliability of Power Electronic Converter Systems*, ser. Energy Engineering. Institution of Engineering and Technology, 2015. [Online]. Available: https://books.google.co.uk/books?id=Ix4WrgEACAAJ

[18] E. E. Lewis, *Introduction to reliability engineering*, 2nd ed. New York :: J. Wiley,, c1996. [Online]. Available: http://www.loc.gov/catdir/description/wiley033/95013533.html

[19] C. Hillman, "The End is Near for MIL-HDBK-217 and Other Outdated Handbooks," https://www.designnews.com/electronics-test/end-near-mil-hdbk-217-and-other-outdated-handbooks, 2018, [Online] Accessed: December 5 2021.

[20] M. Galea, P. Giangrande, V. Madonna, and G. Buticchi, "Reliability-oriented design of electrical machines: The design process for machines' insulation systems must evolve," *IEEE Industrial Electronics Magazine*, vol. 14, no. 1, pp. 20–28, 2020.

[21] X. Perpiñà, J. Serviere, L. Navarro, M. Mermet-Guyennet, M. Vellvehi, and X. Jordà, *Reliability and Lifetime Prediction for IGBT Modules in Railway Traction Chains*. INTECH Open Access Publisher, 2012. [Online]. Available: https://books.google.co.uk/books?id=LkLYoAEACAAJ

[22] D. Hirschmann, D. Tissen, S. Schroder, and R. W. D. Doncker, "Reliability prediction for inverters in hybrid electrical vehicles," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2511–2517, Nov 2007.

[23] K. Ma, M. Liserre, F. Blaabjerg, and T. Kerekes, "Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 590–602, Feb 2015.

[24] M. H. M. Sathik, S. Prasanth, F. Sasongko, and J. Pou, "Lifetime estimation of off-the-shelf aerospace power converters," *IEEE Aerospace and Electronic Systems Magazine*, vol. 33, no. 12, pp. 26–38, Dec 2018.

[25] D. Zhou, H. Wang, and F. Blaabjerg, "Mission profile based system-level reliability analysis of dc/dc converters for a backup power application," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 8030–8039, Sept 2018.

[26] J. Due and A. J. Robinson, "Reliability of thermal interface materials: A review," *Applied Thermal Engineering*, vol. 50, no. 1, pp. 455–463, 2013. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S1359431112004346

[27] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of igbt modules - various factors influencing lifetime," in *5th International Conference on Integrated Power Electronics Systems*, March 2008, pp. 1–6.

[28] B. Hu, J. Ortiz Gonzalez, L. Ran, H. Ren, Z. Zeng, W. Lai, B. Gao, O. Alatise, H. Lu, C. Bailey, and P. Mawby, "Failure and reliability analysis of a sic power module based on stress comparison to a si device," *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 4, pp. 727–737, 2017.

[29] *Process management for avionics — Atmospheric radiation effects*, International Electrotechnical Commission, 2017.

[30] J. F. Ziegler, "Terrestrial cosmic rays," *IBM Journal of Research and Development*, vol. 40, no. 1, pp. 19–39, Jan 1996.

[31] G. Soelkner, "Ensuring the reliability of power electronic devices with regard to terrestrial cosmic radiation," *Microelectronics Reliability*, vol. 58, pp. 39 – 50, 2016, reliability Issues in Power Electronics. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0026271415302663

[32] U. Scheuermann and U. Schilling, "Impact of device technology on cosmic ray failures in power modules," *IET Power Electronics*, 05 2016.

[33] D. U. Schilling, *Cosmic Ray Failures in Power Electronics*, Semikron Gmbh, 2017.

[34] N. Kaminski, *Failure Rates of HiPak Modules Due to Cosmic Rays Application Note 5SYA 2042-02*, ABB Switzerland Ltd, 2004.

[35] R. Edwards, C. Dyer, and E. Normand, "Technical standard for atmospheric radiation single event effects, (see) on avionics electronics," in *2004 IEEE Radiation Effects Data Workshop (IEEE Cat. No.04TH8774)*, July 2004, pp. 1–5.

[36] G. Consentino, M. Laudani, G. Privitera, C. Pace, C. Giordano, J. Hernandez, and M. Mazzeo, "Effects on power transistors of terrestrial cosmic rays: Study, experimental results and analysis," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, March 2014, pp. 2582–2587.

[37] C. Felgemacher, S. V. Araújo, P. Zacharias, K. Nesemann, and A. Gruber, "Cosmic radiation ruggedness of si and sic power semiconductors," in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, June 2016, pp. 51–54.

[38] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters 2014;an overview," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569–3578, Sept 2014.

[39] H. Wang and H. Wang, "Capacitive dc links in power electronic systems-reliability and circuit design," *Chinese Journal of Electrical Engineering*, vol. 4, no. 3, pp. 29–36, September 2018.

[40] R. Gallay, "Metallized film capacitor lifetime evaluation and failure mode analysis," in *CAS-CERN Accelerator School: Power Converters*, 05 2014.

[41] A. Hammoud and E. Overton, "Low temperature characterization of ceramic and film power capacitors," in *Proceedings of Conference on Electrical Insulation and Dielectric Phenomena - CEIDP '96*, vol. 2, 1996, pp. 701–704 vol.2.

[42] *Electric components — Reliability — Reference conditions for failure rates and stress models for conversion*, International Electrotechnical Commission, 2017.

[43] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 3151–3157.

[44] P. D. Reigosa, H. Wang, Y. Yang, and F. Blaabjerg, "Prediction of bond wire fatigue of igbts in a pv inverter under a long-term operation," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7171–7182, Oct 2016.

[45] J. M. Warmuth, "Mission Profiles," https://semiengineering.com/mission-profiles/, 2018, [Online] Accessed: December 5 2021.

[46] *Mission Profile Format*, http://www.mpfo.org/mpfo-0.7/mpfo_ch_introduction.html, MPFO Project, [Online] Accessed: December 5 2021.

[47] O. S. corporation, *Basic Thermal Properties of Semiconductors*, On Semiconductor corporation, 2009.

[48] "Standard Practices for Cycle Counting in Fatigue Analysis," ASTM International, West Conshohocken, PA, Tech. Rep., Oct. 2011.

[49] K. Mainka, M. Thoben, and O. Schilling, "Lifetime calculation for power modules, application and theory of models and counting methods," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, Aug 2011, pp. 1–8.

[50] C. Souto, J. Correia, A. De Jesus, and R. Calçada, "Fatigue damage tool (fdt) - a tool for fatigue damage assessment according to design codes," vol. 22, 01 2019, pp. 376–385.

[51] *Monte Carlo Simulation*, https://www.ibm.com/nl-en/cloud/learn/monte-carlo-simulation, IBM Cloud Education, [Online] Accessed: December 5 2021.

[52] D. C. Loder, A. Bollman, and M. J. Armstrong, "Turbo-electric distributed aircraft propulsion: Microgrid architecture and evaluation for eco-150," in *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, June 2018, pp. 550–557.

[53] U. Scheuermann and M. Junghaenel, "Limitation of power module lifetime derived from active power cycling tests," in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, March 2018, pp. 1–10.

[54] S. Bozhko, T. Yang, J. Le Peuvedic, P. Arumugam, M. Degano, A. La Rocca, Z. Xu, M. Rashed, W. Fernando, C. I. Hill, C. Eastwick, S. Pickering, C. Gerada, and P. Wheeler, "Development of aircraft electric starter–generator system based on active rectification technology," *IEEE Transactions on Transportation Electrification*, vol. 4, no. 4, pp. 985–996, Dec 2018.

[55] F. Gao, S. Bozhko, Y. Seang Shen, and G. Asher, "Control design for pmm starter-generator operated in flux-weakening mode," in *2013 48th International Universities' Power Engineering Conference (UPEC)*, Sep. 2013, pp. 1–6.

[56] "Raising European Students Awareness in Aeronautical Research," https://www.fp7-restarts.eu/index.php/home/root/state-of-the-art/objectives/2012-02-15-11-58-37/71-book-video/parti-principles-of-flight/126-4-phases-of-a-flight.html, 2017, [Online] Accessed: February 10 2021.

[57] "Flight Aware Flight Tracker," https://uk.flightaware.com, 2021, [Online] Accessed: February 10 2021.

[58] N. Oceanic and A. Administration, *U.S. Standard Atmosphere, 1976*, National Oceanic and Atmospheric Administration, 1976.

[59] E. Kalnay, M. Kanamitsu, R. Kistler, W. Collins, D. Deaven, L. Gandin, M. Iredell, S. Saha, G. White, J. Woollen, Y. Zhu, M. Chelliah, W. Ebisuzaki, W. Higgins, J. Janowiak, K. C. Mo, C. Ropelewski, J. Wang, A. Leetmaa, R. Reynolds, R. Jenne, and D. Joseph, "The ncep/ncar 40-year reanalysis project," *Bulletin of the American Meteorological Society*, vol. 77, no. 3, pp. 437–472, 1996. [Online]. Available: https://doi.org/10.1175/1520-0477(1996)077⟨0437:TNYRP⟩2.0.CO;2

[60] D. A. Wintrich, *ECPE Tutorial Thermal Engineering of Power Electronics Systems 1 - First steps of a converter design*, SEMIKRON Elektronik GMBH, 2018.

[61] J. W. Kolar and S. D. Round, "Analytical calculation of the rms current stress on the dc-link capacitor of voltage-pwm converter systems," *IEE Proceedings - Electric Power Applications*, vol. 153, no. 4, pp. 535–543, July 2006.

[62] K. GOPALAKRISHNAN, S. JANAKIRAMAN, S. Das, and G. Narayanan, "Analytical evaluation of dc capacitor rms current and voltage ripple in neutral-point clamped inverters," *Sadhana - Academy Proceedings in Engineering Sciences*, vol. 42, pp. 1–13, 05 2017.

[63] InfineonTechnologiesAG, *PC and TC Diagrams - Use of Power Cycling Curves for IGBT4*, Infineon Technologies AG.

[64] E. Özkol and S. Hartmann, *Load-Cycle Capability of HiPak IGBT Modules Application Note 5SYA 2043-04*, ABB Switzerland Ltd, 2014.

[65] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97–114, March 2014.

[66] H. Wang, P. Davari, H. Wang, D. Kumar, F. Zare, and F. Blaabjerg, "Lifetime estimation of dc-link capacitors in adjustable speed drives under grid voltage unbalances," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.

[67] K. Ma, U. Choi, and F. Blaabjerg, "Prediction and validation of wear-out reliability metrics for power semiconductor devices with mission profiles in motor drive application," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9843–9853, Nov 2018.

[68] J. McPherson, *Reliability Physics and Engineering: Time-To-Failure Modeling*. Springer US, 2010. [Online]. Available: https://books.google.co.uk/books?id=pXKZFEOZkWcC

[69] B. Smet, "An empiric approach to establishing mosfet failure rate induced by single-event burnout," in *2008 13th International Power Electronics and Motion Control Conference*, 2008, pp. 102–107.

[70] J. Guo, G. Buticchi, and C. Gerada, "Space weather prediction to enhance the reliability of the more electric aircraft," in *2018 IEEE 27th International Symposium on Industrial Electronics (ISIE)*, 2018, pp. 445–450.

[71] M. Andresen, J. Kuprat, V. Raveendran, J. Falck, and M. Liserre, "Active thermal control for delaying maintenance of power electronics converters," *Chinese Journal of Electrical Engineering*, vol. 4, no. 3, pp. 13–20, September 2018.

[72] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, and M. Liserre, "Junction temperature control for more reliable power electronics," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 765–776, Jan 2018.

[73] T. Sato, "Analytical model for estimating terrestrial cosmic ray fluxes nearly anytime and anywhere in the world: Extension of parma/expacs," *PloS one*, vol. 10, no. 12, p. e0144679, 2015. [Online]. Available: http://europepmc.org/articles/PMC4682948

[74] H.Wade Patterson, W. N. Hess, B. J. Mayer, and R. W. Wallace, "The flux and spectrum of cosmic-ray-produced neutrons as a function of altitude," 1959.

[75] E. Normand and T. J. Baker, "Altitude and latitude variations in avionics seu and atmospheric neutron flux," *IEEE Transactions on Nuclear Science*, vol. 40, no. 6, pp. 1484–1490, Dec 1993.

[76] I. Vernica, K. Ma, and F. Blaabjerg, "Optimal derating strategy of power electronics converter for maximum wind energy production with lifetime information of power devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 267–276, March 2018.

[77] N. R. Baker, "An electrical method for junction temperature measurement of power semiconductor switches," Ph.D. dissertation, Aalborg Universitet, 2016.

[78] M. Andresen, M. Schloh, G. Buticchi, and M. Liserre, "Computational light junction temperature estimator for active thermal control," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7.

[79] V. Sundaramoorthy, E. Bianda, R. Bloch, I. Nistor, G. Knapp, and A. Heinemann, "Online estimation of igbt junction temperature (tj) using gate-emitter voltage (vge) at turn-off," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10.

[80] U. Choi, F. Blaabjerg, and S. Jørgensen, "Power cycling test methods for reliability assessment of power device modules in respect to temperature stress," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2531–2551, March 2018.

[81] R. Edwards, "Technical specification foratntospheric radiation single event effects (see) on avionics electronics," Goodrich, 2005.

[82] A. Akturk, J. M. McGarrity, N. Goldsman, D. J. Lichtenwalner, B. Hull, D. Grider, and R. Wilkins, "Predicting cosmic ray-induced failures in silicon carbide power devices," *IEEE Transactions on Nuclear Science*, vol. 66, no. 7, pp. 1828–1832, 2019.

[83] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2219–2230, 2010.

[84] I. Staudt, *Application Note AN-11001 3L NPC & TNPC Topology*, SEMIKRON International GmbH, 2015.

[85] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source pwm inverters," in *Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting*, 1993, pp. 965–970 vol.2.

[86] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: theory, design and operational limitations," in *IAS '97. Conference Record of the 1997 IEEE Industry Applications Conference Thirty-Second IAS Annual Meeting*, vol. 2, 1997, pp. 1336–1343 vol.2.

[87] R. M. Tallam, R. Naik, and T. A. Nondahl, "A carrier-based pwm scheme for neutral-point voltage balancing in three-level inverters," *IEEE Transactions on Industry Applications*, vol. 41, no. 6, pp. 1734–1743, 2005.

[88] J. Pou, J. Zaragoza, P. Rodriguez, S. Ceballos, V. M. Sala, R. P. Burgos, and D. Boroyevich, "Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 4, pp. 2288–2294, 2007.

[89] C. Wang and Y. Li, "Analysis and calculation of zero-sequence voltage considering neutral-point potential balancing in three-level npc converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2262–2271, 2010.

[90] A. H. Bhat and N. Langer, "Capacitor voltage balancing of three-phase neutral-point-clamped rectifier using modified reference vector," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 561–568, 2014.

[91] U. Choi, J. Lee, and K. Lee, "New modulation strategy to balance the neutral-point voltage for three-level neutral-clamped inverter systems," *IEEE Transactions on Energy Conversion*, vol. 29, no. 1, pp. 91–100, 2014.

[92] J. I. Leon, S. Vazquez, J. A. Sanchez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and E. Dominguez, "Conventional space-vector modulation techniques versus the single-phase modulator for multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2473–2482, 2010.

[93] C. Müller, *Opportunities and Challenges of Electric Aircraft Propulsion*, Siemens A.G, 2017.

[94] E. Levi, R. Bojoi, F. Profumo, H. A. Toliyat, and S. Williamson, "Multiphase induction motor drives - a technology status review," *IET Electric Power Applications*, vol. 1, no. 4, pp. 489–516, 2007.

[95] F. Barrero and M. J. Duran, "Recent advances in the design, modeling, and control of multiphase machines—part i," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 449–458, 2016.

[96] M. J. Duran and F. Barrero, "Recent advances in the design, modeling, and control of multiphase machines—part ii," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 459–468, 2016.

[97] R. H. Nelson and P. C. Krause, "Induction machine analysis for arbitrary displacement between multiple winding sets," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-93, no. 3, pp. 841–848, 1974.

[98] R. Bojoi, M. Lazzari, F. Profumo, and A. Tenconi, "Digital field-oriented control for dual three-phase induction motor drives," *IEEE Transactions on Industry Applications*, vol. 39, no. 3, pp. 752–760, 2003.

[99] Yifan Zhao and T. A. Lipo, "Space vector pwm control of dual three-phase induction machine using vector space decomposition," *IEEE Transactions on Industry Applications*, vol. 31, no. 5, pp. 1100–1109, 1995.

[100] I. Zoric, M. Jones, and E. Levi, "Arbitrary power sharing among three-phase winding sets of multiphase machines," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1128–1139, 2018.

[101] J. Karttunen, S. Kallio, P. Peltoniemi, P. Silventoinen, and O. Pyrhönen, "Dual three-phase permanent magnet synchronous machine supplied by two independent voltage source inverters," in *International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion*, 2012, pp. 741–747.

[102] Y. Hu, Z. Q. Zhu, and M. Odavic, "Comparison of two-individual current control and vector space decomposition control for dual three-phase pmsm," *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4483–4492, 2017.

[103] E. Jung, H. Yoo, S. Sul, H. Choi, and Y. Choi, "A nine-phase permanent-magnet motor drive system for an ultrahigh-speed elevator," *IEEE Transactions on Industry Applications*, vol. 48, no. 3, pp. 987–995, 2012.

[104] A. Galassini, "Distributed speed control for multi-three-phase motors with enhanced power sharing capabilities," Ph.D. dissertation, University of Nottingham, 2018.

[105] Jen-Ren Fu and T. A. Lipo, "Disturbance-free operation of a multiphase current-regulated motor drive with an opened phase," *IEEE Transactions on Industry Applications*, vol. 30, no. 5, pp. 1267–1274, 1994.

[106] H. S. Che, M. J. Duran, E. Levi, M. Jones, W. Hew, and N. A. Rahim, "Postfault operation of an asymmetrical six-phase induction machine with single and two isolated neutral points," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5406–5416, 2014.

[107] R. R. Errabelli and P. Mutschler, "Fault-tolerant voltage source inverter for permanent magnet drives," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 500–508, 2012.

[108] B. Li, S. Shi, B. Wang, G. Wang, W. Wang, and D. Xu, "Fault diagnosis and tolerant control of single igbt open-circuit failure in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3165–3176, 2016.

[109] B. . Lin and T. . Wei, "Three-phase high power factor rectifier with two npc legs," *IEE Proceedings - Electric Power Applications*, vol. 150, no. 6, pp. 639–646, 2003.

[110] X. Yuan, W. Merk, H. Stemmler, and J. Allmeling, "Stationary-frame generalized integrators for current control of active power filters with zero steady-state error for current harmonics of concern under unbalanced and distorted operating conditions," *IEEE Transactions on Industry Applications*, vol. 38, no. 2, pp. 523–532, 2002.

[111] F. Rodriguez, E. Bueno, M. Aredes, L. Rolim, F. Neves, and M. Cavalcanti, "Discrete-time implementation of second order generalized integrators for grid converters," in *2008 34th Annual Conference of IEEE Industrial Electronics*, 2008, pp. 176–181.

[112] A. G. Yepes, "Digital resonant current controllers for voltage source converters," Ph.D. dissertation, University of Vigo, 2011.

[113] *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*, Texas Instruments, 9 2019.

[114] D. De Gaetano, J. Harikumaran, G. Sala, M. Degano, G. Buticchi, and C. Gerada, "On torque improvement by current harmonic injection in isotropic and anisotropic multi-phase machines," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, pp. 1–1, 2021.