Modeling and control of a voltage-lift cell split-source inverter with MPPT for photovoltaic systems

Iotfy, M. W.; Dabour, S. M.; Mostafa, R. M.; Almakhles, D. J.; Elmorshedy, M. F.

Published in:
IEEE Access

DOI:
10.1109/ACCESS.2023.3280602

Publication date:
2023

Document Version
Publisher's PDF, also known as Version of record

IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2022.Doi Number

Modeling and Control of a Voltage-Lift Cell Split-Source Inverter with MPPT for Photovoltaic Systems

Mostafa Wageh Iotfy[1], Sherif M. Dabour[2], Ramadan Mahmoud Mostafa[1], Dhafer J. Almakhles[3], and Mahmoud F. Elmorshedy[2,3,*]

[1]Department of Process Control Technology, Faculty of Technology and Education, Beni-Suef University, Beni-Suef, Egypt
[2]Department. of Electrical Power and Machines Engineering, Tanta University, Tanta 31733, Egypt
[4]Renewable Energy Lab., College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia
Corresponding author, Mahmoud F. Elmorshedy (mahmoud.elmorshedy@f-eng.tanta.edu.eg)

Abstract—In this study, a new single-stage inverter with improved boosting performance was proposed to enhance the recently developed split-source inverter (SSI) topology. The study introduced new SSI configurations with high voltage gain. The proposed design features a voltage-lift cell made of capacitors, inductors, and diodes, which increases the boosting capability. The decoupled control technique, where The DC input current is controlled by the AC modulation signals,allows for independent adjustment of both the DC input and AC output current. The research also employed a modified space vector modulation approach to manage the inverter switches and reduce current ripple. The combination of the proposed topology and the modified SVPWM scheme significantly improves the DC-boosting capabilities. the validity of the proposed solution was confirmed through simulation using three-phase SSI models in MATLAB/SIMULINK®. Finally, The validity of the simulation and experimental investigation of the analysis and performance of the topologies provided.

INDEX TERMS Decoupled control; Grid connection; Photovoltaic systems, Three-phase split-source inverter (SSI); Voltage-lift cell SSI.

I. INTRODUCTION

Renewable energy sources, including photovoltaic panels and fuel cells, have garnered a lot of interest [1], [2]. Despite this, the DC voltage produced by these sources is quite low. Hence, The utilization of a DC-DC boost converter is imperative before the DC-AC inverter step to raise the voltage to an acceptable level, in order to transmit the generated power to either the grid or isolated loads [3], [4], [5]. Primary DC–DC boost converters are the traditional options for boosting inverter output voltages, Nevertheless, The instability is caused by their duty ratio, which is relatively high and limits switching frequency [6]. Grid-connected PV systems can benefit from low/high-frequency transformers [7]-[35]. Two-stage or single-stage transformerless power converter topologies are available for renewable energy systems [8], [9]. However, the two-stage method is more expensive and inefficient. One of the recently established single-stage topologies is the split-source inverter (SSI), which has a basic construction, as presented in Fig. 1(a). Because of its benefits, such as continuous input current, reduced capacitor voltage stress, higher efficiency, low cost, and simpler design, it has demonstrated good features [10], [11].

The quasi Z-source inverter (qZSI) is a three-phase inverter that adds an impedance network between the input DC source and the conventional B6-bridge. This impedance network comprised 2 inductors, 2 capacitors, and a fast recovery diode. In order to obtain the boosting action in the qZSI, additional switching states called shoot-through (ST) states are used in addition to the standard eight. The ST switching states can be achieved by using seven different combinations of B6-bridge.

The literature has reported several indepth reviews of various ZSI topologies and modulation approaches [12]-[18]. Because of its straightforward construction and continuous input current, the qZSI topology is more appropriate for the PV, FC applications, multiport topologies, electric vehicles, and electric drive applications [18]-[20]. However, despite this appealing ZSI/qZSI utilization in many applications, it has several common flaws which should be taken into consideration before presenting these inverters in the market. These flaws are summarized as follows [12], [13]: The ST intervals cause a decrease in the modulation area, The low quality of voltage and the underutilization of the DC bus are causing subpar performance.the DC voltage fluctuates rapidly with high dv = dt. To achieve high gain, ZSIs require

prolonged ST intervals, making it challenging to maintain good output voltage quality. In addition, the parasitic effects of the impedance network become more prominent in this situation, which significantly decreases the gain, For attaining a high voltage gain with a brief ST time, the use of additional passive components in constructing a more extensive impedance source network is necessary.

Recently, a newly emerged topology which is called the SSI, presented in Fig. 1(a), has been introduced. This architecture boasts a reduced amount of passive components in comparison to the qZSI and possesses numerous benefits over the ZSI. It features a stable input current, a standardized modulation technique utilizing the same eight states as a conventional VSI, This design incorporates a DC-boost converter into the conventional three-phase VSI by connecting the boost inductor to the AC output terminals of the inverter legs using diodes, resulting in a consistent inverter DC voltage with a low-frequency element. The integration of the boost converter into DC-AC power conversion was initially studied in [14] and [15], where [15] looked into the potential of utilizing two boost converters to generate a sinusoidal output voltage.In [11], a new (SSI) topology was devised by Abdelhakim and his team. This architecture was established by combining a DC-boost converter with a conventional three-phase voltage source inverter (VSI), Figure 1(a) illustrates the connection of the boost inductor to the AC output terminals of the inverter legs (a, b, c) using diodes (Da, Db, Dc) to achieve a conventional three-phase voltage source inverter (VSI).

The continuous conduction mode analysis of the SSI has been investigated in [21] and [22].A new SSI topology is being created in order to improve the boosting capability. In attaining the requisite boosting characteristics and bridging this gap, a novel inverter topology is proposed by combining the basic SSI topology with a voltage-lift method. This combination leads to a significant improvement in the input voltage of the inverter, making it more suitable for uses in the renewable energy sector. The voltage-lift cell is employed to attain a high gain factor, thereby enhancing its efficiency. The suggested design enhances the voltage gain and decreases the ripple in the input current, compared to the SSI discussed in reference [13], several modified space vector modulation (MSVM) techniques have been put forward in studies [12], [13], and [24] to improve the suggested SSI's efficiency. The significance of the boost converter in DC-AC power conversion was initially investigated in studies [14]-[17].

In this article, the DC side of the SSI is modeled, and a control strategy for the grid-connected mode is presented. The strategy involves separating the control of the DC and AC sides of the SSI by using a modified modulation scheme in combination with the synchronous reference frame control method. By utilizing the common-mode component of the AC modulation signals, the DC side can be controlled, resulting in additional flexibility similar to that of a two-stage design. In recent times, there has been a growing interest in the analysis and study of control systems in grid-connected mode for various applications. For example, in [18], the control of three-phase multilevel qZSIs for photovoltaic systems in grid-connected mode was explored. Meanwhile, [19] and [20] An energy storage system has been established that utilizes qZSIs and incorporates several passive components, such as resistors, capacitors, and inductors, without compromising its flexibility in control. This results in a system that is both efficient and reliable, yet still offers the necessary adjustability to meet changing requirements and operate optimally,The potential application scenario for this topology is in renewable energy systems, such as solar photovoltaic and wind energy conversion systems.

The following summarizes the major differences between these topologies and previous boost inverters:

1) The fundamental split-source design remains intact,
2) Both buck and boost operations can be performed,
3) the voltage and boosting gains are increased, and
4) it uses the typical SSI modulation methods.

It corresponds to this flaw: uneven switch current sharing, which was similar to the basic SSI. This study focuses on creating a controller for a grid-connected voltage-lift cell SSI with the aim of improving the power quality of the distribution system. The study also examines its control through the use of the maximum boost method. The paper is structured as follows: Section II provides an overview of the operating principle of the voltage-lift cell, The study begins with an introduction and is followed by a discussion of the decoupled control method for the grid-connected voltage-lift cell SSI in Section III. This section also covers the modification made to its conventional modulation approach. The results of the simulation, performed using a MATLAB/Simulink model, are displayed in Section IV. Finally, the experimental results and conclusions are presented in the last section.

II. DIFFERENT TOPOLOGIES OF THE PROPOSED SSI AND COMPARATIVE ASSESSMENT

A. Topologies of the proposed SSI

A power circuit design for a voltage-lift cell SSI (as specified in [23]) is illustrated in Figure 1(b). The newly introduced SSI topology has two modes of operation: charging mode and discharge mode. The circuit is comprised of three key components: The system includes the three-phase section input section, the high-gain SSI cell section, and the input section section.There are four diodes (D_1, D_2, D_3,and D_4), three inductors (L_1, L_2, L_3), and three capacitors (C_1, C_2,and C_3), with L_1 and L_2 which have the same value, as well as six switches (S_{au}, S_{bu}, S_{cu}, S_{al}, S_{bl}, S_{cl}) and three diodes (D_a, D_b, D_c). This unique topology can result in significantly better voltage conversion than that of the standard SSI. Efficient reduction of input current ripple is achieved when the voltage conversion is equalized.

- ***Charging Mode***

In this configuration, It is necessary to activate at least one of the lower switches (S_{al}, S_{bl}, S_{cl}) is engaged, as indicated in Fig. 1(c).This results in diodes D_2 and D_4 being on and diodes D_1 and D_3 being off. During the switching-charging state operation, the inductor currents i_{L1}, $i_{L2,}$ and i_{L3} increase linearly as the DC input voltage (E) provides energy to inductor L_1, and the stored energy from capacitors C_2 and C_3 is transferred to inductors L_2 and L_3. As a result, the inductor currents i_{L1}, $i_{L2,}$ and i_{L3} increase linearly, and the voltage equations, among others, can be derived from the analysis. and current equations.

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = E \\ L_2 \dfrac{di_{L2}}{dt} = V_{C2} + V_{C3} \\ L_3 \dfrac{di_{L3}}{dt} = V_{C2} \end{cases} \tag{1}$$

and current equations.

$$\begin{cases} C_1 \dfrac{dv_{C1}}{dt} = -i_{L1} \\ C_2 \dfrac{dv_{C2}}{dt} = -i_{L2} - i_{L3} \\ C_3 \dfrac{dv_{C3}}{dt} = -i_{L2} \end{cases} \tag{2}$$

- ***Discharging Mode***

When all the higher switches (S_{au}, S_{bu}, S_{cu}) are closed, this mode is activated (ON). Correspondingly, diodes D_1 and D_2 are ON, as presented in Fig. 1(d). Meanwhile, the D_2 and D_4 diodes are turned off.As a result, the DC input voltage (E) and inductor L_1 supply energy to C_2, the stored energy from inductor L_3 is transferred to C_3, and the energy stored in inductors L_2 and $L_3$is delivered to C_2. This results in a gradual decline in the inductor currents i_{L1}, i_{L2}, and i_{L3} during the discharging mode, as described by the following equations.

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = E - V_{C2} \\ L_2 \dfrac{di_{L2}}{dt} = -V_{C2} + V_{C3} \\ L_3 \dfrac{di_{L3}}{dt} = -V_{C2} \end{cases} \tag{3}$$

and current equations.

$$\begin{cases} C_1 \dfrac{dv_{C1}}{dt} = i_{L2} \\ C_2 \dfrac{dv_{C2}}{dt} = -i_{L1} \\ C_3 \dfrac{dv_{C3}}{dt} = i_{L3} - i_{L2} \end{cases} \tag{4}$$

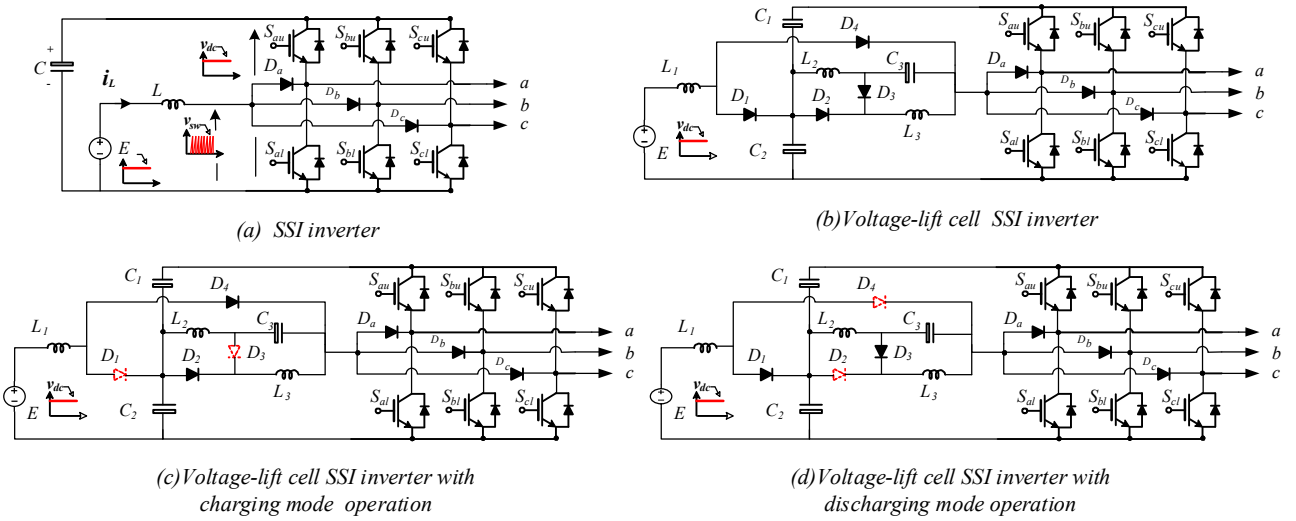


FIGURE 1. A voltage-lift cell SSI inverter that operates in two modes.

B. Comparative Assessment

The comparison of the inverter topologies, including the qZSI, SSI, and proposed VLSSI, is thoroughly discussed in this section. The assessment is based on the following factors: the simplicity of the modulation, steady-state analysis, the stress on current and voltage, and the required specifications for passive components. The comparison results for the evaluated topologies are presented in Table 3, This involves assessing the duty cycles, boosting factors, voltage stress on capacitors and semiconductors, as well as the AC-voltage gain of each topology.

- ***Implementations***

In comparing various topologies, it requires taking into consideration some key factors, one of which is the implementation process for modulation methods which was used in power converters. After considering different factors such as the quantity of duty cycles and the potential use of advanced PWM (ePWM) modules found in modern DSPs,

the complexity of the modulation technique can be determined. In Table I, the various topologies are compared based on the number of active switches needed and the level of intricacy involved in their implementation using ePWM modules. The proposed VLSSI and basic SSI modulation are simpler than the qZSI, whose complexity necessitates high specifications for DSP controllers and higher duty cycle requirements, Implementing a fast modulation scheme, such as space vector pulse width modulation (SVPWM), which can generate the gating signals very quickly based on the control commands. This can partially compensate for the slower inductor dynamics. Proper tuning of the modulation scheme and PLL/inner control loops is needed to optimize dynamic performance.

- ***Voltage Gains***

The investigated topologies are compared in terms of more glaring steady-state contrasts in Table 1. The voltage gain range is chosen as G <= 5, which takes into consideration the restrictions brought on by parasitic factors. Correspondingly, it is possible to draw the following conclusions about the relationships between the charging duty cycles and the boosting factor:

1) In SSI and VLCSSI, the charging duty cycle (D_{ch}) has a wider range with $D_{ah} < 1$, while the boosting action of qZSI is applicable for $D_{ah} < 0.5$.

2) The SSI and suggested VLCSSI topologies can achieve higher voltage gains as compared to qZSI.

3) For the exact charging duty cycle, the VLCSSI's boosting capacity is much higher than that of the ordinary SSI. The DC-boost factor's squaring feature is responsible for this.

4) Low-modulation indices are necessary in achieving significant voltage gains in the qZSI. Thus, the distorted output voltage in the qZSI is anticipated more than that of the other topologies.

Table 1 Comparisons of the proposed voltage-lift cell split-source inverter (VLCSSI) with the conventional full-bridge qZSI and the SSI.

Inverter features	q-ZSI	SSI [6]	VLC SSI
Number of active switches	6	6	6
Number of diodes	1	3	7
Number of inductors	2	1	3
Number of capacitors	2	1	3
THD	Low at low-voltage gains	Low at high-voltage gains	Low at high-voltage gains
Charging duty cycle, Dch	1-M	M	M
Reliability	High	Low	Low
PWM Complexity	Complex	Simple	Simple
Input current waveform	continual	continual	continual
DC- voltage	pulsed	continual	continual
Boosting factor	$1/(1-2D_{sh})$	$1/(1-2D_{sh})$	$1/(1-2D_{sh})^3$
Voltage gain	$M/\left(\sqrt{3}(1-M)\right)$	$M/\left(\sqrt{3}(1-M)\right)$	$M/\left(\sqrt{3}(1-M)^3\right)$
Voltage stresses	Highest	Low	High
Voltage gain control	Complex	Moderate	Moderate

- ***Component Stress Factor (CSF)***

The CSF is an essential parameter in assessing the stress on the components of an inverter. Lower CSF values indicate reduced stress on the components, leading to increased reliability and lifespan. Table 2 shows the specific values of the CSF between the proposed voltage-lift cell split-source inverter (VLCSSI), the conventional full-bridge qZSI, and the SSI.

Table 2 CSF comparison between the proposed voltage-lift cell split-source inverter (VLCSSI), the conventional full-bridge qZSI, and the SSI.

Inverter features	q-ZSI	SSI [6]	VLC SSI
CSF	2.3	1.9	1.8

As demonstrated in table 2, the proposed topology yields a lower CSF than the other inverters, resulting in reduced stress on the components and improved reliability.

- ***Switching Device Power (SDP)***

SDP is a critical indicator of the efficiency of an inverter. Lower SDP values signify higher efficiency and reduced power losses. Table 3 shows the specific values of the SDP between the proposed voltage-lift cell split-source inverter (VLCSSI), the conventional full-bridge qZSI, and the SSI.

Table 3 SDP comparison between the proposed voltage-lift cell split-source inverter (VLCSSI), the conventional full-bridge qZSI, and the SSI.

Inverter features	q-ZSI	SSI [6]	VLC SSI
SDP (W)	65	55	50

The table above demonstrates that the proposed topology has the lowest SDP among all the compared inverters, indicating higher efficiency and minimized power losses.

In conclusion, the proposed topology outperforms the other latest methods (QZS inverter, two-stage inverter, and SSI) in terms of both Component Stress Factor (CSF) and Switching Device Power (SDP), high boosting factor, and higher voltage gain leading to enhanced reliability and efficiency.

III. MODULATION TECHNIQUEs

Based on their approach in attaining the charging and discharging modes, The available modulation methods for the three-phase voltage-boosting cell SSI are categorized in Figure 2, as previously mentioned in [25]. Pulse Width Modulation (PWM) using Space Vector Modulation (SVM)

is employed. This method generates a reference voltage through controlling current in a rotating reference frame. As previously discussed, a VLSSI has eight possible operating conditions, including two zero states and six active states. While all PWM techniques that are used for the conventional VSI can be utilized to control the switches of the proposed voltage-lifting cell split-source inverter (VLCSSI) for boosting and inverting purposes, These are some possible techniques that be applied to the proposed inverter to realize soft-switching operation and improve its performance.

1-Using switch topologies that have inherent soft-switching characteristics. For example, a MOSFET/IGBT with an anti-parallel diode can achieve ZVS operation. When one switch turns off, the body diode of the other switch conducts the current and allows the voltage to rise/fall smoothly, thereby achieving ZVS.

2-Modifying the pulse width modulation (PWM) pattern to achieve soft switching. For example, a degree of dead time can be added between the on/off transitions of the complementary switches. During this dead time, the anti-parallel diodes conduct and allow the voltage/current to change slowly, achieving soft switching.

The standard modulation approach for all extended-boost-based SSIs is considered to be the modified unregulated and regulated SVPWM methods, which were proposed in [10] and [26]. This is because they offer several advantages, such as:

1) It ensures smooth, continuous charging and discharging of the inductors with a duty cycle. This reduces input current ripple and voltage stress.

2) It can be utilized in achieving a performance comparable to that of the two-stage topology. Equations (5) and (6) are used in a carrier-based system implementation to generate gating pulses for the B6 switches by matching the per-phase duty cycles (da, db, dc) with a high-frequency triangular carrier wave.

$$\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - \min\left(d_a, d_b, d_c\right) + \left(1-\gamma\right) \tag{1}$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{M_{ac}}{\sqrt{3}} \begin{bmatrix} \cos\left(2\pi ft\right) \\ \cos\left(2\pi ft - 2\pi/3\right) \\ \cos\left(2\pi ft + 2\pi/3\right) \end{bmatrix} \tag{2}$$

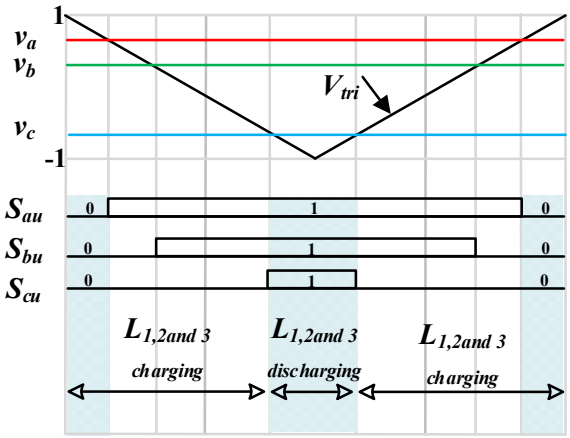


FIGURE 2. Pulse Width Modulation method for proposed topology

The last term in equation (5) represents a constantly increasing upward-shifting factor for the boosting duty cycles. The value of "in" in (5) for the MSVM scheme is "Mac" [6]. Correspondingly, the same control variable, Mac, is used in regulating both the output voltage gains and the DC-boosting factor, By substituting Mdc with equation (5) in the RMSVM technique, an extra control parameter is introduced on the DC side, as explained in reference [26]. This results in a clear differentiation between the control of the AC and DC sides, which is crucial for regulating the frequency (V/f) of motor drives and for applications that are connected to the power grid.

A. Space Vector PWM (SVPWM) Technique

The standard VSI's eight switching states can be synthesized by synthesizing the space-vector for each state.

$$\vec{V} = \frac{2}{3}\left(v_{an} + v_{bn}e^{j2\pi/3} + v_{bn}e^{j4\pi/3}\right) \tag{3}$$

When the space vector is applied to the inverter phase voltages, it results in eight possible voltage vectors, six of which are active and two are zero vectors. Figure 4 illustrates these vectors along with their corresponding instantaneous common-mode voltage magnitudes for each switching vector. In the conventional three-phase VSI SVPWM, two neighboring active space vectors in each sector are used along with the zero vectors to synthesize the reference voltage vector ($\vec{V} = Me^{j\theta}$), as shown in Figure 5. For example, if $\vec{V}$ the vector is in sector A1, the vectors $\vec{V}_1$ and $\vec{V}_2$ are used. The reference vector for each sample interval Ts is calculated using the volt-second balance principle.

$$T_s\vec{V} = T_1\vec{V}_1 + T_2\vec{V}_2 + T_3\vec{V}_3$$

where T_1, T_2, and T_z are the time of application of the active and zero vectors V_1, V_2, and V_z, respectively, which are calculated by:

$$T_1 = T_s M \sin\left(\pi/3 - \theta\right) \tag{4}$$

$$T_2 = T_s M \sin\left(\theta\right) \tag{5}$$

$$T_z = T_s - T_1 - T_2 \tag{6}$$

In the traditional SVPWM approach, the time duration T_z is evenly distributed between the zero vectors V_0 and V_7, with T_0 and T_7 representing this division.

$$T_0 = T_7 = 0.5T_z = 1 - M\sin\left(\pi/3 - \theta\right) \tag{7}$$

The validity of equation (17) extends throughout the entire linear region within its range $0 \le M \le 1$.

B. Modified SVPWM (MSVPWM) Technique for SSI

By using the MSVM method, the low-frequency component present in both the current flowing through the inductor and the voltage of the inverter can be effectively removed. This is achieved by fixing the duty cycle, which is calculated as the ratio of the active-state equivalent times (T_a and T_b) to the total switching time (T_s). The zero-state equivalent time (T_z) can be reallocated without impacting the active-state times by recalling the switching pattern of the SVPWM scheme as depicted in Fig. 7 (a). The key to this process is to redistribute the zero-state equivalent time without affecting the active-state times. Equation (19) represents the minimum value of the zero-state equivalent time, T_{zm}, which has been shown in references [25] and [33] to be equal to the time it takes for the inductor L to discharge, T_x.

$$T_x = T_{zm} = T_s\left(1 - 2M\sin\left(\pi/6\right)\right) \tag{8}$$

In Fig. 7(b), you can see that the extra time left in the zero state is given to another zero-state in that area. By adjusting Tx to Tzm, the same biasing discussed earlier is applied, as shown in Fig. 6. With this modification, you can see that the reference signals remain constant at the lower virtual envelope, and the duty cycle D is fixed at M. Using this information, one can determine the normalized peak phase voltages of the inverter and output fundamental by performing calculations. which are outlined in [34].

$$\frac{V_{inv}}{V_{dc}} = \frac{1}{1 - M} \tag{9}$$

$$\frac{V_{\varphi}}{V_{dc}} = \frac{1}{\sqrt{3}\left(1 - M\right)} \tag{10}$$

C. RMSV Modulation Scheme

In this section, the regulated RMSV modulation technique is introduced as depicted in Fig. 3, In this technique, a single control parameter, the modulation index (M), is used to govern both the AC and DC sides simultaneously, while the maximum peak value of (v_a^*, v_b^*, v_c^*) is fixed at one end. The approach employs space vector modulation technique to generate a reference voltage and regulate current in a rotating reference frame. As mentioned earlier, the three-phase SSI generates eight states, comprising of six active states and two zero states.

The vectors make up a hexagonal shape, as illustrated in Figure 4, comprised of six segments with a 60-degree angle each. The SVPWM technique is employed to produce a reference vector for three-phase sinusoidal voltage by alternating between the active-state and zero-state vectors [16].

IV. CONTROL OF THE VOLTAGE-LIFT CELL TECHNIQUEs

In this section, a high-performance, single-stage DC-to-AC inverter is presented. The suggested inverter architecture relies on a split-source inverter, which has been augmented with a voltage-lift cell to improve its boosting capacity. The voltage-lift cell is composed of three capacitors, two inductors, and four diodes. The control of the AC modulation signals is managed through a decoupled control method that utilizes a common-mode term for the voltage-lift cell split-source inverter.

The authors have put forward a high-boost, single-stage DC-to-AC inverter topology that is based on the split-source inverter. This topology incorporates a voltage-lift cell that consists of two inductors, four diodes, and three capacitors, which enhances its boosting capability. To control the DC input current, the inverter uses a decoupled control technique that separates the AC and DC modulation signals and utilizes the common-mode term. The authors then analyze this control scheme for the grid-connected mode of operation, the SSI is examined to determine whether the synchronous reference frame control technique can also be applied to a conventional two-stage architecture (consisting of a three-phase inverter). The section begins by explaining the SSI modulation scheme and how it adds two control parameters that allow independent regulation of the AC and DC sides. The authors then create a decoupled closed-loop control method for the grid-connected VLCSSI by integrating the regulated MSV modulation approach, the technique of synchronous reference frame control, which is widely used, is employed in this process.This control scheme has two sections: the input power control section and the grid-side control section. The modulation index M_{ac} regulates the grid-side, while the regulation index M_{dc} controls the DC side.

The Figure 8 depicts the grid-connected SSI decoupled control method's architecture in the rotating dq reference frame, which is then elaborated on in the following sections. To begin with, a Lf filter interface inductance links the grid to the SSI. The technique for implementing RMSV modulation is depicted in Fig. 5. The procedure involves converting the reference signals obtained from the synchronous reference frame controller into modulating signals that are expressed as space vectors. which are then subjected to saturation. After saturation, the resulting modulating signals are further transformed into Root Mean Square (RMS) equivalent modulating signals, with the minimum of the negative envelope, represented by min (v_a^*, v_b^*, v_c^*), set to zero (i.e. M_{ac} =1). Subsequently, the input current controller fine-tunes the negative envelope by altering the value of Mac in accordance with the input current reference. By using the input DC voltage (v_{inv}), one can determine the average DC-link voltage and the peak phase voltage of the output

fundamental ($v_{\varphi 1}$). These variables are interconnected and can be expressed mathematically. based on Equations (7) and (8) in reference [26], respectively.

$$v_{inv} = \frac{1}{1 - M_{dc}} \times v_{inv} \tag{11}$$

$$v_{\varphi 1} = \frac{M_{ac}}{\sqrt{3}} \times v_{inv} \tag{12}$$

A. MPPT Controller

The operating point of a photovoltaic (PV) system is managed through the VLCSSI duty cycle, M_{dc}, to maintain the PV voltage at the level corresponding to V_{mp}, denotes the voltage level at which the highest amount of power is accessible for a given temperature and radiation condition.

V_{mp} can be determined using any maximum power point tracking technique. Fig. 8 illustrates how cascaded controllers regulate the PV voltage.In order to obtain the current reference, the PV voltage (V_{pv}) is compared to V_{mp}, and any resulting error is fed into a PI controller. This reference is then compared to the actual input current of the VLCSSI and the error is fed into another PI controller to generate the M_{dc} required by RMSVM. To guarantee stability and fast dynamic response, proper tuning of the PI gains is necessary. Thus, a block diagram must be developed for each controller.

B. Input Current Controller

For the purpose of simplicity, by assuming a constant DC-link voltage, The transfer function G_{iL}(s), which corresponds to the regulation index, is obtained by simplifying the small-signal input current through equation (9).

$$G_{iL}(s) = \frac{i_L(s)}{d(s)} = \frac{v_{inv}}{r_L + Ls} \tag{13}$$

In The time-varying regulatory index, mdc(s), is represented by d(s) in equation (9). Fig. 8 illustrates the input current control loop in block diagram format, and it's important to mention that the input current reference, I_L^*, must be obtained through a Maximum Power Point Tracking (MPPT) block. Various MPPT techniques are discussed in [27]. To reduce the impact of the triangular nature of the input current on M_{dc}, To mitigate the impact of high-frequency components, a capacitor is typically connected in parallel to the DC source, acting as a low-pass filter. Additionally, it's noteworthy that instead of regulating the PV source current, a PV system can regulate the PV source voltage. Furthermore, the small-signal input voltage to the regulation index transfer function can be calculated similarly by deriving the state-space representation of the SSI DC side. The digital implementation of the control scheme has proven to be efficient in achieving these objectives.

C. Output Current Controllers

To calculate the grid currents in the rotating dq reference frame (i_{dq}), we need to perform a Park transformation on the measured grid angle (θ_g) and observed grid currents (i_{abc}).This allows us to describe the grid-connected inverter, as depicted in Figure 4, in the rotating dq reference frame using equations (10) and (11).

$$v_{di} = v_{dg} + L_f \frac{di_d}{dt} + r_f i_d - \omega_g L_f i_q \tag{14}$$

$$v_{qi} = v_{qg} + L_f \frac{di_q}{dt} + r_f i_q - \omega_g L_f i_d \tag{15}$$

The output voltage of the inverter, in the rotating dq reference frame, is denoted by vdqi, The interfacing inductor's internal resistance is denoted by "r_f," while the grid's angular frequency, ω_g, is simply the product of $2\pi f_g$, where fg represents the grid frequency measured in Hz. The transfer function can be expressed as equations (12) and (13).

$$G_{id}(s) = \frac{i_d(s)}{v_{di}(s)} = \frac{1}{r_f + L_f s} \tag{16}$$

$$G_{iq}(s) = \frac{i_q(s)}{v_{qi}(s)} = \frac{1}{r_f + L_f s} \tag{17}$$

This model is similar to the models presented in [28], [29], and [30].

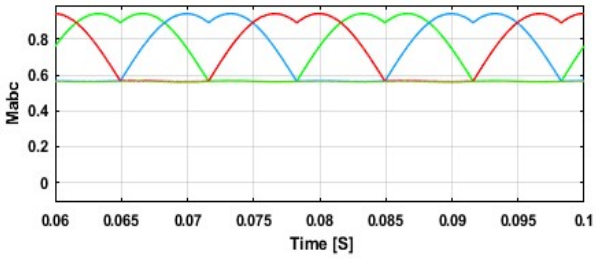


FIGURE 3. Modulating signals.

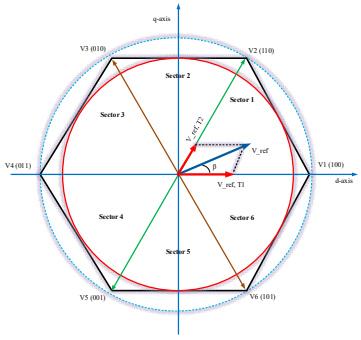


FIGURE 4. Generation of switching vectors for the three-phase voltage-lift cell split-source inverter (VLCSSI).

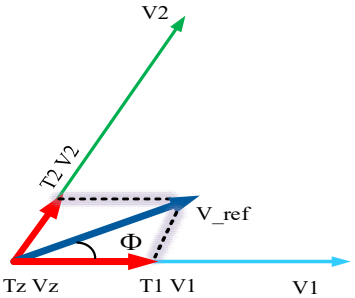


FIGURE 5. The creation of the reference vector for the traditional SVPWM.

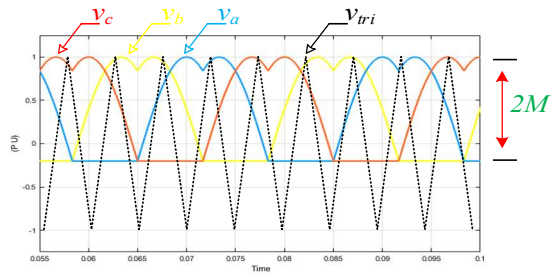


FIGURE 6. References signals that are of the same level as the MSVPWM scheme.

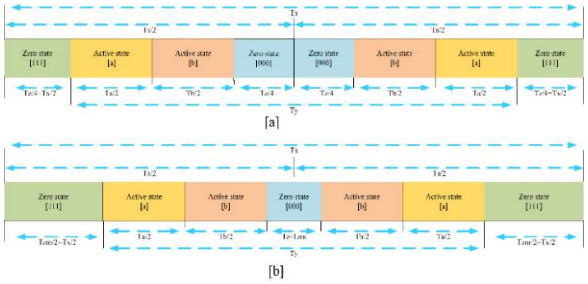


FIGURE 7. Switching behavior during any sector, with time durations between the conventional SVPWM method (a) and the MSVPWM method (b). The duration of the inductor discharge, T_x, and the charge, T_y,

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results and Analysis

The RMSVM approach was used to create a closed-loop configuration with both grid-side control and input power control being part of the strategy. The duty ratio D_0, which controls the DC input power, and the modulation index M, which controls the AC input power, are independent control variables. The MPPT is regulated by an input current controller that manages the duty ratio D_0, as shown in the simulation model in Figure 9. Figure 10 displays simulation results of the voltage, current, and close-up views of 1 millisecond across waveforms of D_1, D_2, C_2, C_3, L_2, and L_3. A 50 V rated voltage ideal voltage source was used to represent the DC input source, while the grid voltage was scaled to 110 Vrms using a grid simulator. The system specifications are listed in Table 3 and the PV array consisted of ten parallel strings, with each string being made up of four connected modules in series. The specifications for each module are outlined in Table 2.

Figure 11 illustrates the agreement between the PV module's I-V characteristics under varying conditions. Specifically, Fig. 11(a) represents different temperatures under a constant irradiance of 1000 W/m2, while Fig. 11(b) shows different irradiance and temperature of 25°C. On the other hand, Fig. 12 displays the simulation results of the grid voltage and current waveforms, which demonstrates the proper control of both the grid currents and input DC current throughout the transient time. These topologies were simulated using MATLAB/SIMULINK® with the parameters provided in Table 3. The DC-link voltage control loop, as demonstrated in Fig. 13, maintains a constant injected active power by adjusting the q-axis current reference.

Table 2. PV modul parameters

Parameters	Values	Parameters	Values
Power (W)	213.15 W	Rsh (ohms)	7.8649
V_{oc} (V)	36.3 V	Rs (ohms)	.39383
Cells per module (N_{cell})	60	Diode ideality factor	.98117
I_{sc} (A)	7.84 A	Voltage at MPP Vmp (V)	29 V
I_L (A)	7.8649 A	Maximum Power Point Current (Imp) in Amperes	7.35 A

Table 3. Lists the parameters used in simulating the studied topologies.

Parameters	Values
Grid phase voltage (*Vn*)	110 Vrms
Grid frequency (*fgrid*)	50 Hz
Dc input voltage (*VDC*)	100 V
input power (P_{in})	8 kW
Switching frequency (*fsw*)	10 kHz

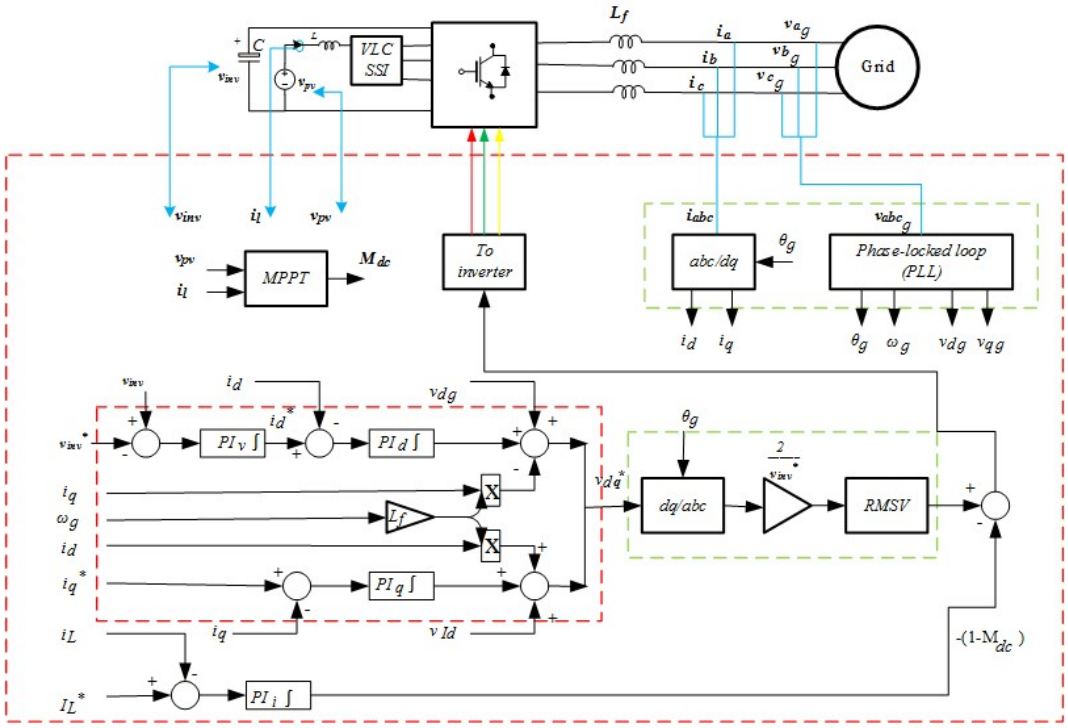


FIGURE 8. The proposed grid-connected split-source inverter employs a decoupled control strategy.

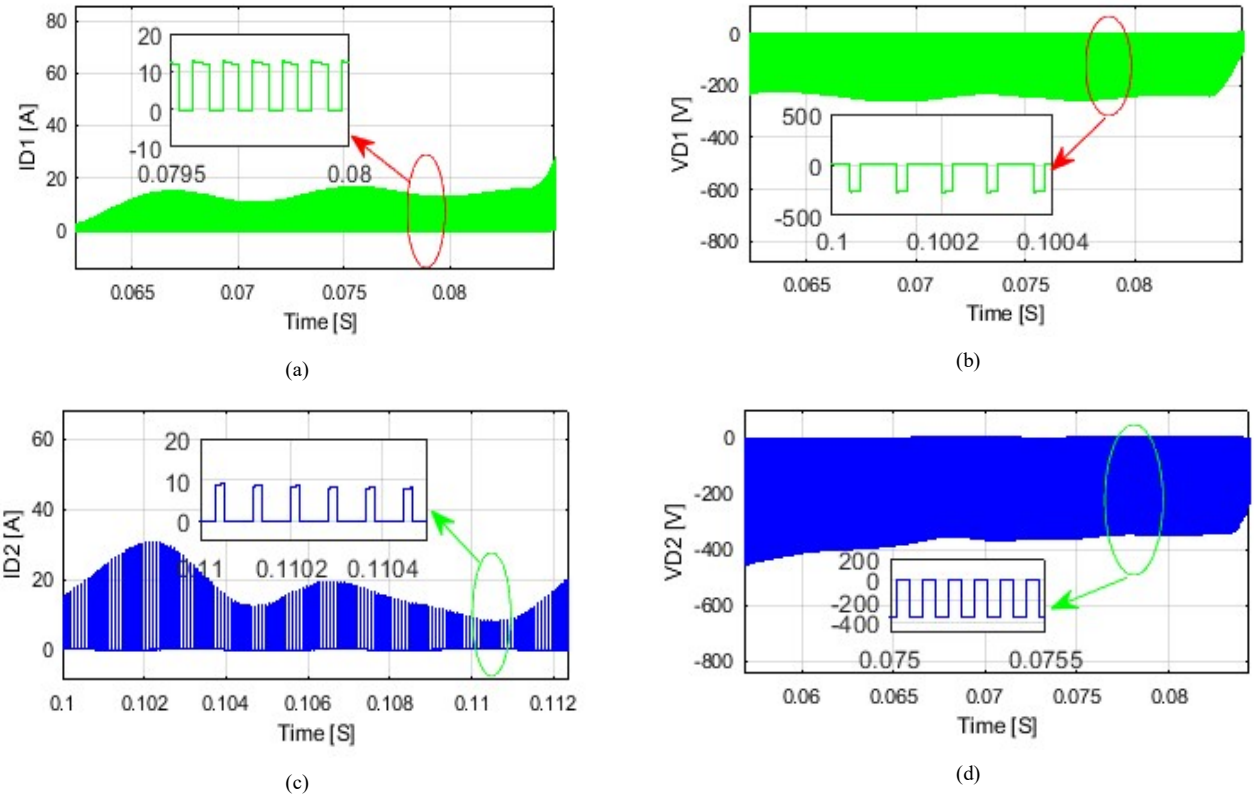


FIGURE 9. The simulation results showed the voltage and current outputs, as well as an in-depth 1 millisecond view of the waveforms across diodes D_1 and D_2. (a) voltage across D_1, (b) current through D_1, (c) voltage across D_2, (d) current through D_2.

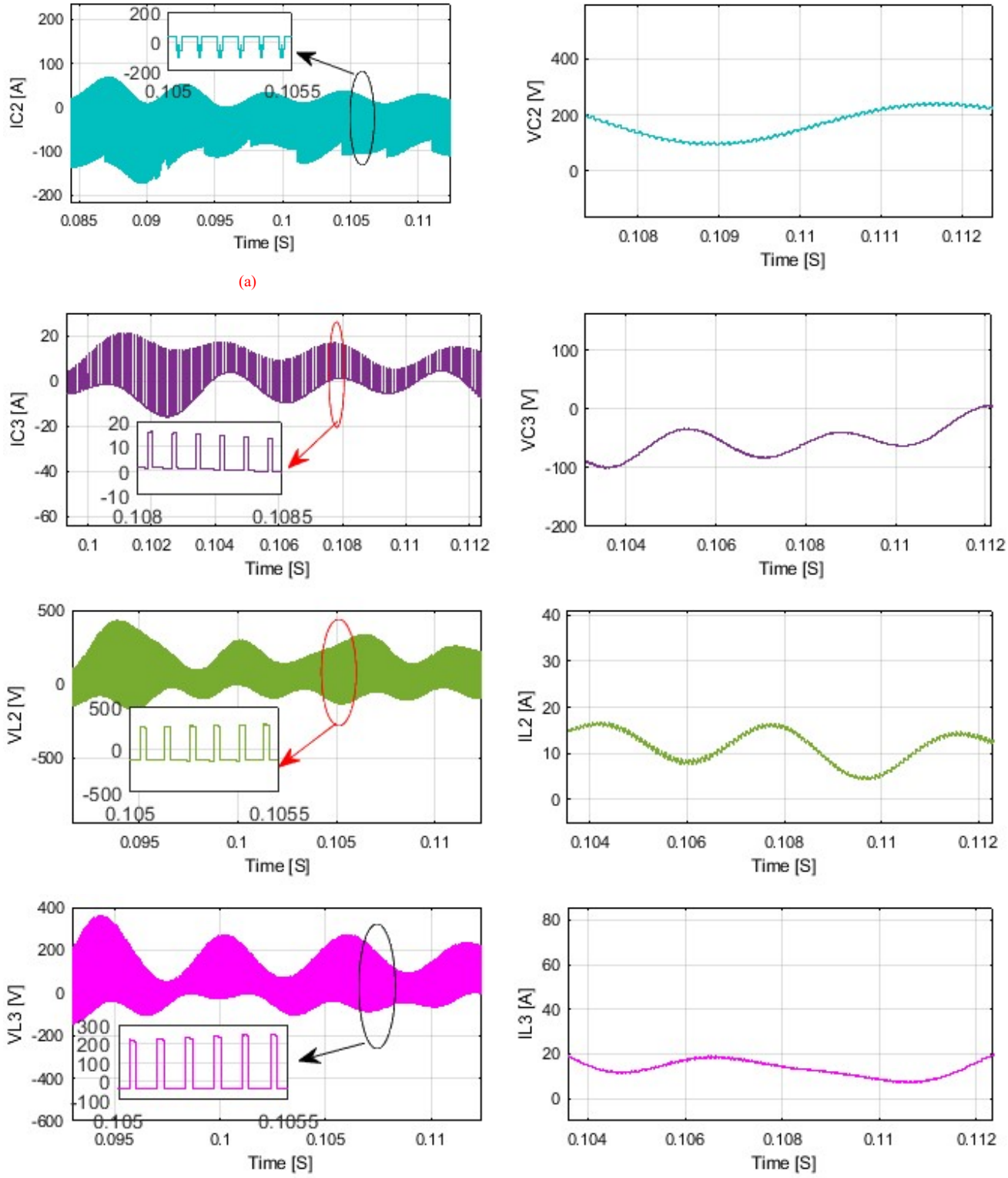


FIGURE 10. simulation results included the voltage and current outputs, as well as detailed 1 millisecond views of the waveforms across capacitors C_2, C_3, and inductors L_2, and L_3.

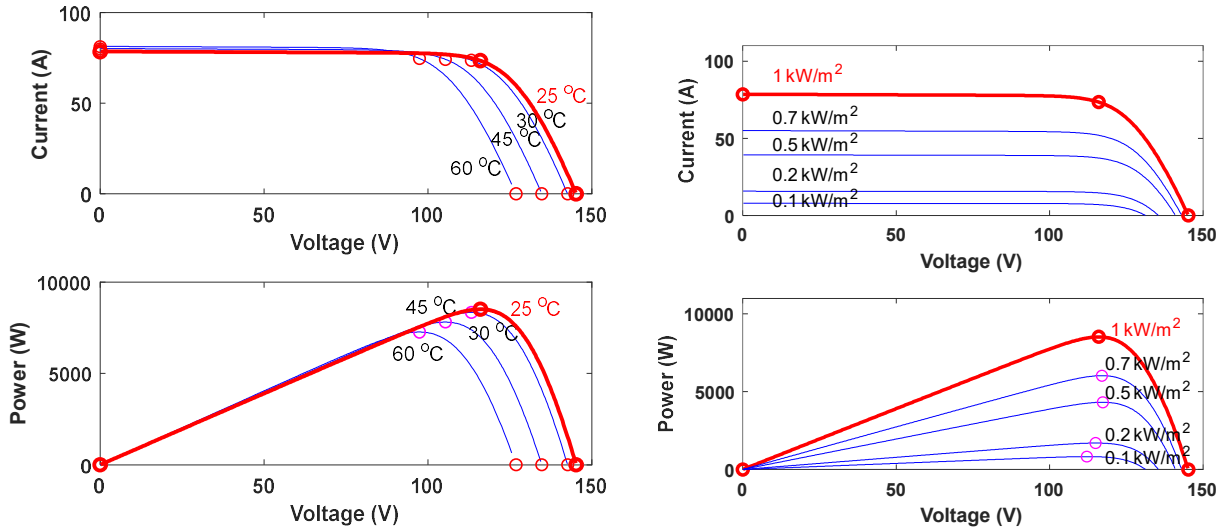


FIGURE 11. The module's I-V characteristics were measured using parameter estimation methods with varying irradiance and a temperature of 25°C. The same I-V characteristics were also measured with a constant irradiance of 1000 W/m^2 and at different temperatures.

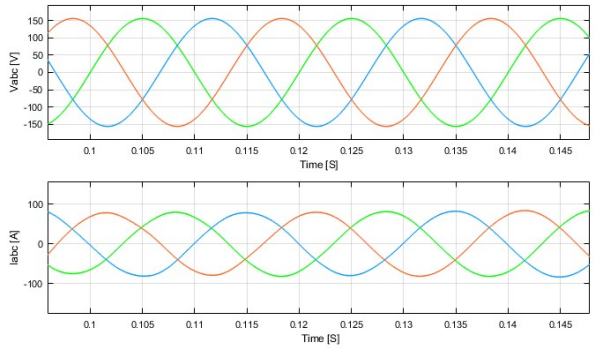


FIGURE 12. Grid voltage and current waveforms.

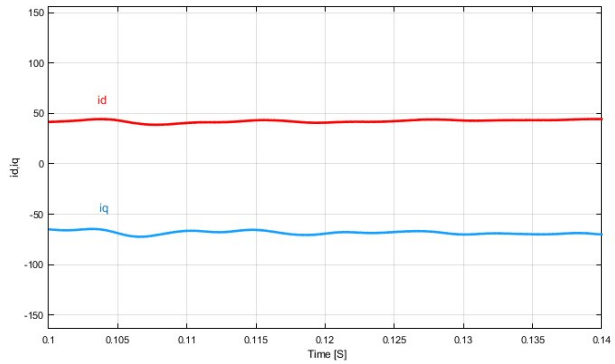


FIGURE 13. Grid current components in the rotating *dq* frame.

B. Experimental Results

To evaluate the performance of the analyzed topologies, a small-scale prototype was created in the lab using the parameters listed in Table 4. The SSI was implemented using the Texas Instruments Launch-Pad LAUNCHXL-F28379D DSP board, which was used for generating the MSVM gating pulses and dead-time generation (1 µs).

The proposed inverter topology improves the basic three-phase SSI by incorporating a voltage-lift cell made up of three capacitors (C_1, C_2, C_3), two inductors (L_2, L_3), and four diodes (D_1, D_2, D_3, D_4) to increase boosting capability. By combining these features, It is possible to attain a high voltage DC-DC boosting factor and lower input DC current ripple, which ultimately results in a significant increase in voltage gain at the AC output terminals.The experimental setup for the VLCSSI is shown in Figure 14.

Figure 15 shows the input current and three-phase load current (i_{abc}) waveforms, and Figs. 16 and 17 present the capacitor C_2 voltage and C_3 current waveform with zoomed-in views of 1 millisecond of the capacitor. Meanwhile, Figs. 18–20 show the inductor voltage and inductor current, L_1, L_2, and L_3 waveforms, respectively, which include zoomed-in views of 1 millisecond.

Table 4. Experimental parameters for the VLCSSI

Parameter	Value	Parameter	Value
Switching Frequency	20 kHz	DSP	TI-F28379D
Dead time	1 µs	IGBT	HGTG20N60B3D
Load	11 Ω & 5 mH	M	.5

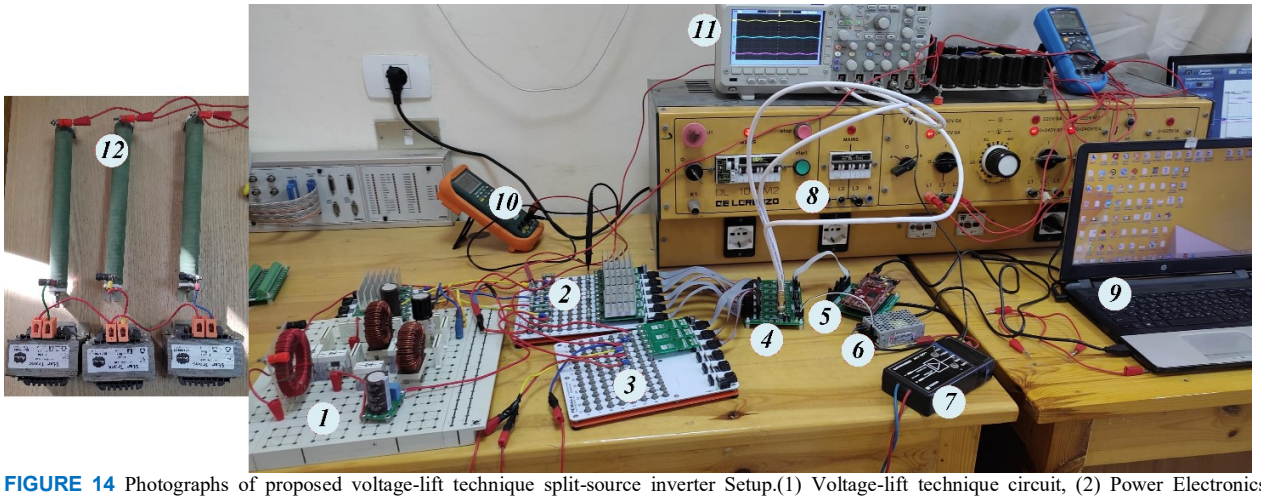


FIGURE 14 Photographs of proposed voltage-lift technique split-source inverter Setup.(1) Voltage-lift technique circuit, (2) Power Electronics Breadboard connected with six IGBT modules,(3) three current sensors,(4) Six Modules Signal Collector Board, (5) F28379D Launchpad Kit Card™, (6) dc supply, (7) Voltage probe, (8) Power supply, (9) lab top, (10) digital multimeter, (11) the oscilloscope and (12) RL-loads.

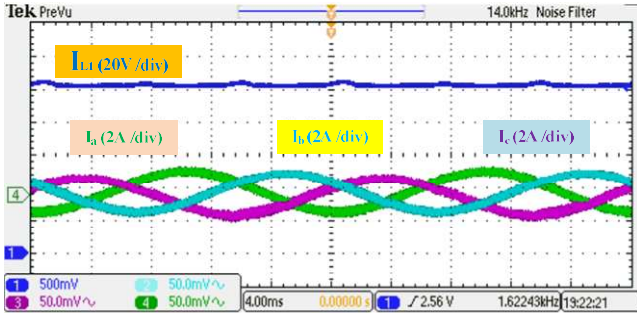


FIGURE 15 Experimental results of input current and three-phase load current ($iabc$) waveforms.

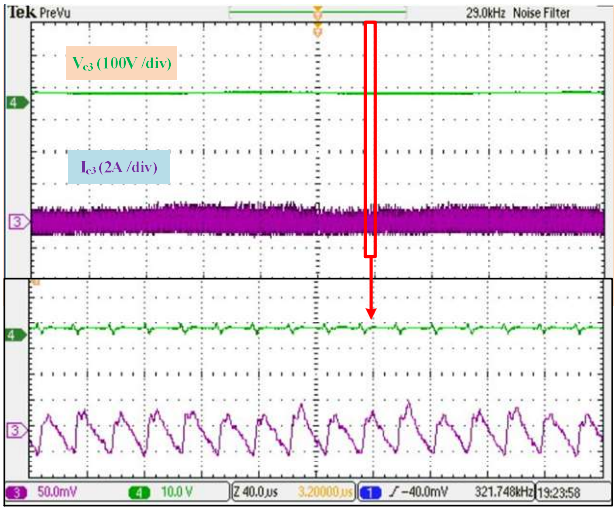


FIGURE 16 Experimental results of capacitor C_3 voltage and current waveforms and zoomed-in views of 1 millisecond across.

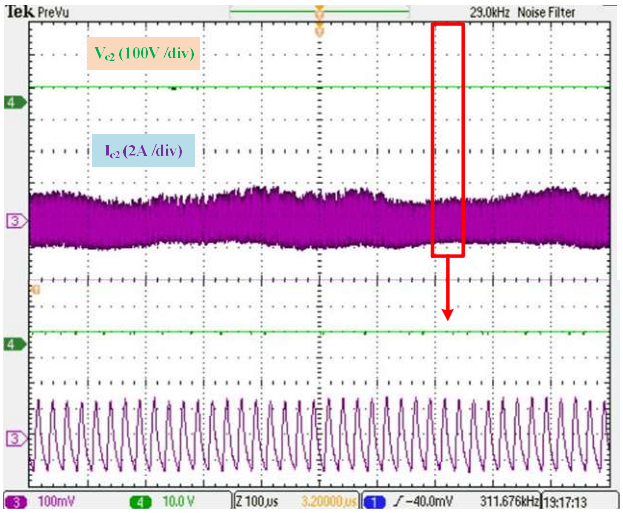


Fig. 17 Experimental results of capacitor C_2 voltage and current waveforms and zoomed-in views of 1 millisecond across.

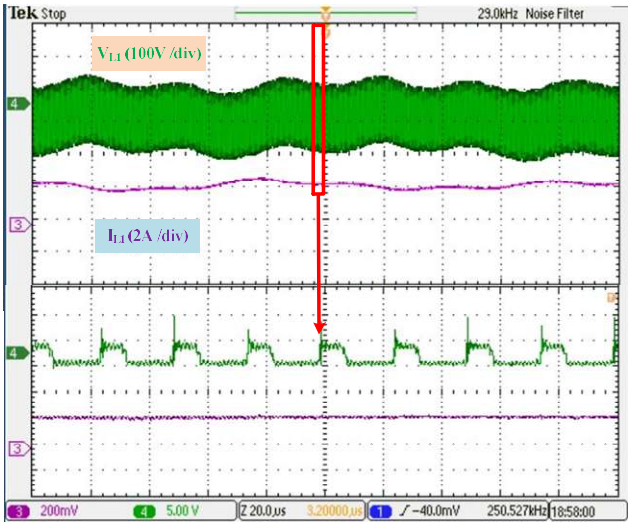


FIGURE 18 Experimental results of inductor L_1 voltage and current waveforms and zoomed-in views of 1 millisecond across.

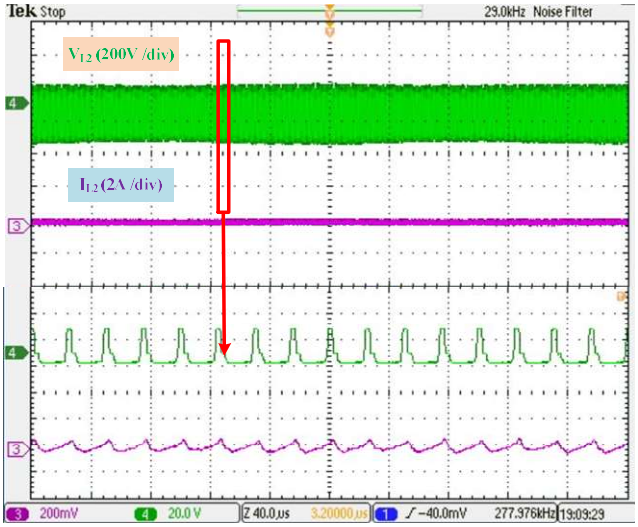


FIGURE 19 Experimental results of inductor L_2 voltage and current waveforms and zoomed-in views of 1 millisecond across.

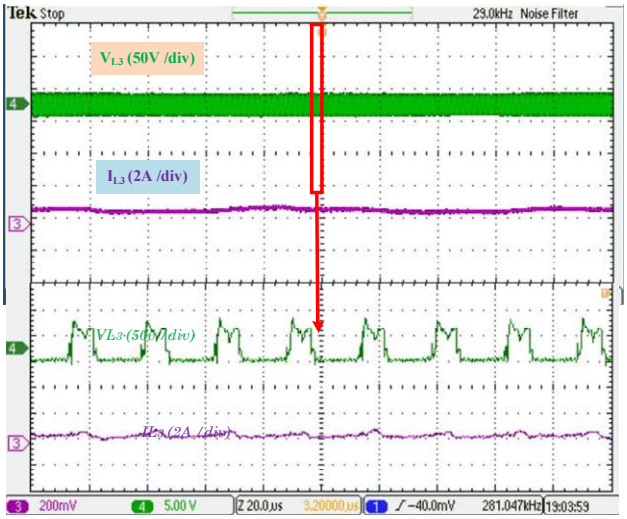


FIGURE 20 Experimental results of inductor L_3 voltage and current waveforms and zoomed-in views of one millisecond across.

VI. CONCLUSIONS

In This paper presents novel SSI topologies with improved high-voltage gain capabilities. By incorporating auxiliary components such as inductors, capacitors, and diodes, these topologies enhance the performance of basic SSI. Additionally, a proposed control strategy has been developed to allow for separate control of the DC and AC sides of the SSI for enhanced applications. The voltage-lift cell technique is utilized for grid-linked control of the split-source inverter. The RMSVM scheme is applied to improve switching characteristics. The conventional boosting inverter topologies that employ a single stage, such as SSI and qZSI, can be mentioned, were compared with the proposed topologies to highlight their benefits. The results indicate that the proposed topology is better suited for renewable energy systems that require a high voltage gain from a low input voltage, and it can be applied to PV and FC systems in a broad range of settings. Both simulation and experimentation demonstrate the feasibility of the proposed topology.

ACKNOWLEDGMENT

The authors would like to thank the support of Prince Sultan University for paying the Article Processing Charges (APC) of this publication and the authors gratefully acknowledge the financial support from Beni-suef University, the university performance development centre, Support and Project Finance office, project ID # YR4-BSU2125.

REFERENCES

[1] W. Li and X. He, "Review of nonisolated high-step-up DC/DCconverters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, 2011, doi:10.1109/TIE.2010.2049715.

[2] Pachagade, Ruchi, AU - Maroti, Pandav Kiran, AU - Bhaskar, M. S."Reduced Auxiliary Circuit Switch Nine-Level Inverter for Renewable Energy Applications" IETE Journal of Research, 2022, doi: 10.1080/03772063.2021.2014364

[3] F. Pereira et al., "Design of a DC-DC converter with high voltage gain for photovoltaic-based microgeneration" in *Proc. 40th Annu.* Conf. IEEE Ind. Electron. Soc. (IECON 2014), Oct. 2014, pp. 1404–1409, doi:10.1109/IECON.2014.7048685.

[4] E. G. Shehata et al., "Design and analysis of a quasi y-source impedance network dc-dc converter" in Nineteenth International Middle East. Power Syst. Conference (MEPCON), vol. 2017. IEEE, 2017, Dec., pp. 235–241, doi:10.1109/MEPCON.2017.8301189.

[5] Jayachandran Divya Navamani , Sathik Jagabar , Padhi Tanmay , Kumari Aditi,"A Comprehensive Review of the Quadratic High Gain DC-DC Converter for Fuel Cell Application" INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2022, VOL. 68, NO. 2, PP. 299-306, DOI 10.24425/ijet.2022.139882

[6] Y.-P. Hsieh et al., "A novel high step-up DC-DC converter for a microgrid system,", *IEEE Trans. Power Electron.*, IEEE, Trans., vol. 26, no. 4, pp. 1127–1136, Apr. 2011, doi:10.1109/TPEL.2010.2096826.

[7] R. Teodorescu et al., *Grid Converters for Photovoltaic and Wind Power Systems*. Hoboken, USA: Wiley, 2011.

[8] I. Jamal, M. F. Elmorshedy, S. M. Dabour, E. M. Rashad, W. Xu and D. J. Almakhles, "A Comprehensive Review of Grid-Connected PV Systems Based on Impedance Source Inverter," in IEEE Access, vol. 10, pp. 89101-89123, 2022, doi: 10.1109/ACCESS.2022.3200681.

[9] Divya Navamani, J., Lavanya, A., Sathik, J., Bhaskar, M.S. and Vijayakumar, K. (2022). Dynamic Analysis and Reduced- Order Modeling Techniques for Power Converters in DC Microgrid. In DC Microgrids (eds N. Gupta, M.S. Bhaskar, S. Padmanaban and D. Almakhles). https://doi.org/10.1002/9781119777618.ch8

[10] A. Abdelhakim et al., "Three-phase split-source inverter (SSI): Analysis and modulation," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7451–7461, Nov. 2016, doi:10.1109/TPEL.2015.2513204.

[11] M. F. Elmorshedy, M. M. Ali, S. M. Dabour, D. Almakhles, I. A. Gowaid and M. E. Farrag, "Improved Responses of Grid Connected Quadratic Boost Inverter Based on Super-Twisting Sliding Mode Control," IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 2022, pp. 1-6, doi: 10.1109/IECON49645.2022.9968560.

[12] A. Abdelhakim et al., "Modulation schemes of the three-phase impedance source inverters-Part I: Classification and review," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, Aug., 6309–6320, 2018, doi:10.1109/TIE.2018.2793255.

[13] A. Abdelhakim et al., "Modulation schemes of the three-phase impedance source inverters-Part II: Comparative assessment," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, Aug., 6321–6332, 2018, doi:10.1109/TIE.2018.2793205.

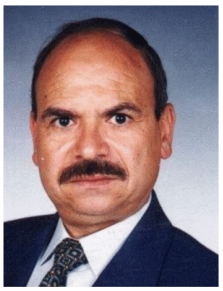
[14] A. Abdelhakim et al., "An improved modulation strategy for the three-phase Z-source inverters (ZSIs)" in *IEEE Energy Conv. Congr. Expo. (ECCE)*, 4237–4243, 2017, doi:10.1109/ECCE.2017.8096733.

[15] R. O. Caceres and I. Barbi, "A boost dc–ac converter: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134-141, Jan. 1999, doi:10.1109/63.737601.

[16] M. Wageh et al., "Space vector PWM of three-phase inverter with MPPT for photovoltaic system," *Aust. J. Electr. Electron. Eng.*, vol. 18, no. 4, p. 310–318, 2021, doi:10.1080/1448837X.2021.1982445.
[17] S. M. Dabour et al., "An optimal PWM technique for dual-output nine-switch boost inverters with minimum passive component count" in *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 1065–1079, Jan. 2021, doi:10.1109/TPEL.2020.3001372.
[18] Y. Liu et al., "An effective control method for three-phase quasi-z-source cascaded multilevel inverter based grid-tie photovoltaic power system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6794–6802, Dec. 2014, doi:10.1109/TIE.2014.2316256.
[19] B. Ge et al., "An energy-stored quasi-z-source inverter for application to photovoltaic power system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4468–4481, Oct. 2013, doi:10.1109/TIE.2012.2217711.
[20] Y. Liu et al., "Control system design of battery-assisted quasi-Z-source inverter for grid-tie photovoltaic power generation," *IEEE Trans. Sustain. Energy*, vol. 4, no. 4, pp. 994–1001, Oct. 2013, doi:10.1109/TSTE.2013.2263202.
[21] N. El-Hendawy et al., "Common-mode voltage analysis of three-phase quasi-Z source inverters for transformerless photovoltaic systems," IEEE Conference on Power Electronics and Renewable Energy (CPERE), 2019, pp. 355–360, doi:10.1109/CPERE45374.2019.8980256.
[22] C. Hou et al., "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, Apr. 2013, doi:10.1109/TPEL.2012.2196712.
[23] M. Wageh et al., "A high gain split-source inverter with reduced input current ripple," 22nd International Middle East. Power Syst. Conference (MEPCON), vol. 2021, *2021*, pp. 383–388, doi:10.1109/MEPCON50283.2021.9686237.
[24] T. T. Thentral et al., "A new space vector pulse width modulated transformerless single-phase unified power quality conditioner," *Mater. Today Proc.*, vol. 45, pp. 1750–1756, 2021.
[25] M. H. Rashid, *Power Electronics Handbook*, 4th ed. Butterworth-Heinemann, 2018.
[26] A. Abdelhakim, et al., "Decoupled control scheme of grid-connected split-source inverters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6202–6211, 2017, doi:10.1109/TIE.2017.2677343.
[27] B. Subudhi and R. Pradhan, "A comparative study on maximum power point tracking techniques for photovoltaic power systems," *IEEE Trans. Sustain. Energy*, vol. 4, no. 1, pp. 89–98, Jan. 2013, doi:10.1109/TSTE.2012.2202294.
[28] R. Teodorescu et al., *Grid Converters for Photovoltaic and Wind Power Systems*. New York, NY, USA: Wiley, 2011.
[29] V. Blasko and V. Kaura, "Anew mathematical model and control of a three phase AC-DC voltage source converter," *IEEE Trans. Power Electron.*, vol. 12, no. 1, pp. 116–123, Jan. 1997, doi:10.1109/63.554176.
[30] Y. Zhang and C. Qu, "Model predictive direct power control of PWM rectifiers under unbalanced network conditions," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4011–4022, Jul. 2015, doi:10.1109/TIE.2014.2387796.
[31] Z. B. Mahmoud et al., "Space vector modulation of multilevel inverters: A simple and fast method of two-level hexagon's selection," *Int. J. Power Electron.*, vol. 8, no. 2, pp. 107–123, 2017, doi:10.1504/IJPELEC.2017.082932.
[32] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters-Principle and Practice*. Wiley-IEEE Press, 2003.
[33] S. Vashishtha and K. R. A. Rekha, "A Survey: Space Vector PWM (SVPWM) in 3φ Voltage Source Inverter (VSI),", *IJECE*, vol. 8, no. 1, pp. 11–18, 2018, doi:10.11591/ijece.v8i1.pp11-18.
[34] S. M. Dabour and E. M. Rashad, "Analysis and implementation of space-vector-modulated three-phase matrix converter," *IET Power Electron.*, vol. 5, no. 8, pp. 1374–1378, 2012, doi:10.1049/iet-pel.2012.0014.
[35] Ali, M., Usman, F., & Yousaf, A. (2017, March). Design and Simulation of Power Electronic Controller for Grid Connected PV Array with maximum power point tracking (MPPT). In 2017 8th International Renewable Energy Congress (IREC) (pp. 1-4). IEEE..

Mostafa Waheb Lotfy was born in Al-Sharkia, Egypt in 1989. He received B.Sc.,M.Sc.,and PhD (Electrical Power and Machines) Degrees in 2012 , 2018 and 2022 respectively, from the Process control technology Department, Faculty of Technology and Education, Beni-Suef University, Egypt, . He is currently working as an Assistant Professor (On academic leave) with the Department of Process control technology, Faculty of Technology and Education, Beni-Suef University, and His research interests include PWM techniques, power converters, electric drives, power electronics, and renewable energy conversion systems.

Sherif M. Dabour (Senior Member, IEEE) received the B.Sc. degree in electrical engineering from Zagazig University, Egypt, in 2002, and the M.Sc. and Ph.D. degrees in electrical power engineering from Tanta University, Egypt, in 2012 and 2015, respectively.,He has extensive experience in research and academic teaching in electrical power and industrial electronics. From 2003 to 2009, he worked as a Lecturer and a Certified Trainer at Technical and Vocational Training Corporation, Riyadh, Saudi Arabia. Since 2009, he has been joining Tanta University, where he is currently an Associate Professor (On academic leave). He was involved in many projects funded by the Egyptian Academy of Scientific Research and Technology and the Qatar National Research Foundation. He is also a Researcher-1A at Glasgow Caledonian University, U.K., where he is participating in research funded by the British Council and the Academy of Engineering and European Commission Projects. He has supervised ten M.Sc. students and three Ph.D. students. To date, he has published 49 articles in international journals and conferences in the field of his expertise. His research interests include analysis, modeling, and application of power electronics converters. In addition, he studies wind turbines, PV systems, storage systems, microgrids, electric vehicle chargers, and energy storage integration. He served as a Treasurer of the IEEE Power Electronics Society (PELS) Egypt Chapter, from 2017 to 2020. Additionally, he is a Reviewer of several journals, including IEEE Transactions on Power Electronics and Industrial Electronics, IET.



Professor R. M. Mostafa has received his B.Sc. & M. Sc. Degrees in Electrical engineering, Aircraft Electric & Special Equipment branch in June, 1972 & Feb. 1978, from Military Technical College, Cairo, Egypt. He has received DEA. & PhD. in Electrical engineering, Juny 1980 & Jan. 1983; Universite/Pierre et Marie Curie, Paris, France. He worked as Lecture & Assistant Professor; Department of Aircraft Electrical & Special Equipment; Military Technical College; Cairo; He worked as Professor at Faculty of Industrial Education, Beni Suef University; June. 2002- July 2015; Dean of the Faculty & Head of Process Control Department, September 2005-August 2009. He worked as Dean of Egyptian Academy for Engineering and Advanced Technology; August 2015 – September 2016.

Dhafer J. Almakhles (Senior Member, IEEE) received the B.E. degree in electrical engineering from the King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, in 2006, and the master's (Hons.) and Ph.D. degrees from The University of Auckland, New Zealand, in 2011 and 2016, respectively. Since 2016, he has been with Prince Sultan University, Saudi Arabia, where he is currently the Chairperson of the Communications and Networks Engineering

Department and the Director of the Science and Technology Unit. He is also the Leader of the Renewable Energy Research Team and the Laboratory at Prince Sultan University. His research interests include the hardware implementation of control theory, signal processing, networked control systems, and sliding mode.

Mahmoud F. Elmorshedy (Member, IEEE) was born in Gharbeya, Egypt, in 1989. He received the B.Sc. and M.Sc. degrees in electrical engineering from Tanta University, Egypt, in 2012 and 2016, respectively, and the Ph.D. degree in electrical engineering from the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, China, in 2020. He started working as a Teaching Assistant with the Department of Electrical Power and Machines Engineering, Faculty of Engineering, Tanta University, in 2013, where he was promoted to an Assistant Lecturer, in June 2016. He is currently working as an Assistant Professor (On academic leave) with the Department of Electrical Power and Machines Engineering, Faculty of Engineering, Tanta University. His current job is a Postdoctoral Fellow with the Renewable Energy Laboratory, College of Engineering, Prince Sultan University, Riyadh, Saudi Arabia. His research interests include linear induction motor, predictive control, power electronics, and renewable energy.