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# An Analysis of Combining dc Circuit Breaker and Hybrid MMC with Reduced Number of FBSM for HVdc System Protection

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# An analysis of combining dc circuit breaker and hybrid MMC with reduced number of FBSM for HVdc system protection

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***Abstract*—Abstract: The hybrid modular multilevel converter (HMMC) is employing half-bridge submodules (HBSMs) and full-bridge submodules (FBSMs), combining the advantages of both. Aiming to reduce the manufacture cost and power losses of such solution, this paper proposes an HMMC in combination with dc circuit breaker (CB) for MMC-based high-voltage direct current (HVdc) systems. Under such conditions, the characteristics of pole-to-pole permanent dc fault is analyzed. Simulation results considering a 150 MW/150 kV symmetrical monopole point-to-point MMC-based HVdc system demonstrate the effectiveness and feasibility of the proposed approach. In this way, the number of FBSM is reduced by about 60 % compared to typical HMMC solutions in the literature. Additionally, considering HMMC with dc CB solution, the peak value of dc fault current and the breaker voltage can be decreased by around 38 % and 50 %, respectively.**

***Index Terms*—Hybrid MMC, dc circuit breaker, HVdc system, full-bridge SM, half-bridge SM**

## I. Introduction

Modular multilevel converter (MMC) has been wide adoption in the high-voltage direct current (HVdc) industry mainly due to its modularity, scalability and inherent fault tolerance [1]. In addition, MMC presents important advantages for multi-terminal HVdc (MTdc) systems when compared with the line commutated converter (LCC), since the dc power flow can be reversed by changing current direction instead of voltage polarity [2]. Nowadays, all leading companies in HVDC market offer solutions based on MMC, and commercial projects for MMC-based MTdc are increasingly common (e.g., Zhangbei four-terminal project, Zhoushan five-terminal project, etc.) [2], [3]. However, dc fault clearance is still one of the major challenge for MMC-based MTdc systems [2].

The state of the art for protection and isolation in dc cable transmission is to use the ac-side circuit breakers (CB) to interrupt dc fault current. This method requires a long time to resume the active power transmission, besides the fact that reactive power support by the converter is lost during the cable isolation sequence [2]. Aiming to provide a faster fault recovery, a dc fault blocking capability can be embedded in the converter station, replacing the traditional half-bridge submodules (HBSM) by submodules capable of producing reverse biased voltage during the dc fault [4]. Some works present a design of hybrid MMC minimizing the number of full-bridge submodules (FBSM) required to ensure a dc fault blocking capability. However, in such cases, the amount of FBSM is still higher than 43% of the total amount of SMs in the HMMC, resulting in increased costs and power losses compared to the HB-MMC [4]. One of the mainstream dc fault handling methods for MMC-based MTdc systems is the hybrid high-voltage dc CB [2]. This technology enables a selective protection scheme for the HVdc system, which minimizes the power outage area and ensures fast fault recovery. Despite advances in the maturity of such technology, the high manufacture cost is a drawback when the number of dc CBs increases due to the complexity of the dc grid [2].

In view of the aforementioned points, this work provides a dc fault blocking approach employing combination of both HMMC and dc CB solutions. Under such conditions, the minimum number of FBSM can be reduced when compared to other HMMC solutions presented in the literature. In addition, a reduction in the dc CB requirements is reached when compared to the traditional dc CB applications with HB-MMC.

This work is outlined as follows. Section II presents the features of the dc CB and an analytical analysis of the HMMC. The case study and the parameters employed in the simulations are presented in Section III. Section IV provides the results obtained and the comparison regarding dynamic behavior for three different solutions. Finally, the conclusions are stated in Section V.

## II. MMC-based HVdc systems

A symmetrical monopole point-to-point MMC-based HVdc system is shown in Fig. 1(a). In contrast to ac grids, the HVdc grid offers low line impedance, which leads to high dc fault currents with fast transients. In addition, an artificial zero crossing to interrupt the fault current safely and to avoid large arc should be created. Under such conditions, the dc circuit breaker or the converter with dc fault blocking capability can be employed, as illustrated in Fig. 1(b) and (c), respectively [5]. The next sections present the features of each method, in addition to explore the use of both methods, simultaneously.

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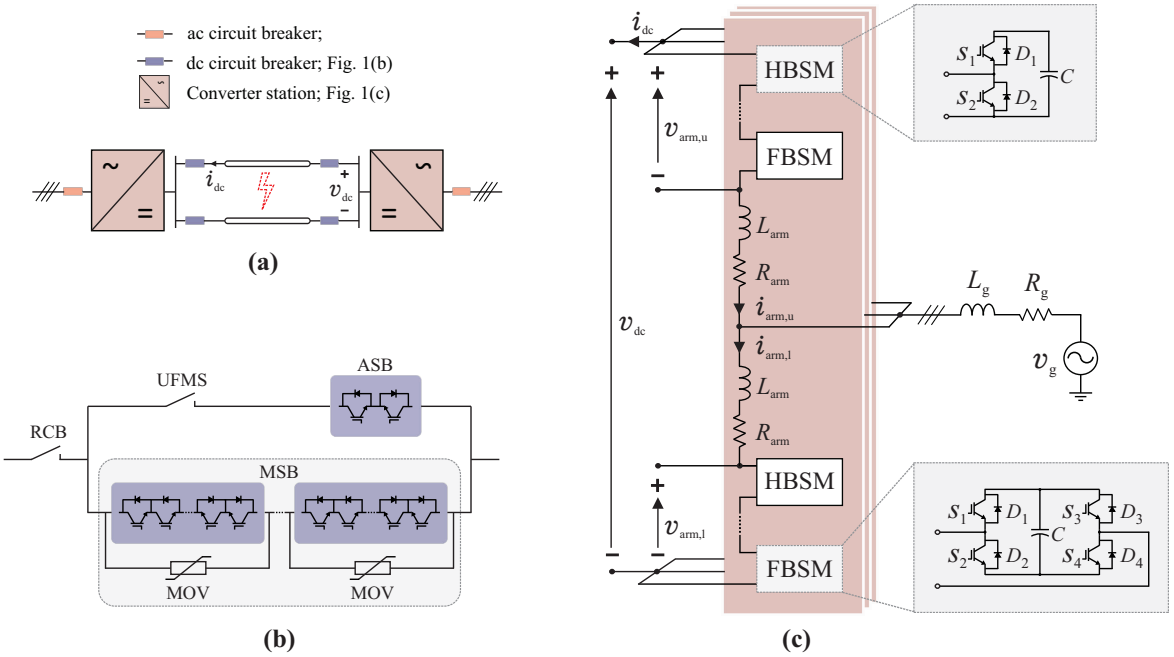


Fig. 1. MMC-based HVdc systems. (a) design schematic of a symmetrical monopole point-to-point HVdc system; (b) hybrid dc CB; (c) three-phase topology of HMMC.

### A. Dc circuit breaker

The basic requirement of dc CB is the capability to create a local current zero at the rated fault current without a re-strike of the mechanical interrupters or thermal overload of power electronic components. After the first announcement of the hybrid dc CB by ABB in 2012 [5], such device has become the most promising dc CB technology for future high-voltage dc grids due to minimum on-state losses and minimum interruption time. As shown in Fig. 1(b), there are three branches to guarantee zero-current switching and to avoid arc creation: a low impedance main current branch with ultra-fast mechanical switch (UFMS) in series with a bidirectional auxiliary semiconductor breaker (ASB), a commutation path with main semiconductor breaker (MSB) and an energy absorption path with metal oxide varistor (MOV). An additional mechanical residual current breaker (RCB) is connected in series with the main dc CB to interrupt the residual current and to isolate the faulted system from HVdc grid, if the fault is identified to be permanent.

The most important dc CB design parameters are the voltage stress after fault current interruption, the energy stress, the interruption time, the rated short circuit current and maximum current derivative [6]. Defining such parameters is a challenge, given the many involved variables and all the possible fault cases in the grid. For such purpose, an interesting approach is to simulate all the possible fault conditions and then evaluate the worst case scenario [7].

### B. Hybrid modular multilevel converter

The schematic of the three-phase HMMC is presented in Fig. 1(c). The converter is composed of three legs, each one containing an upper and a lower arm. Each HMMC arm is composed of an arm inductor $L_{arm}$, an arm inductor resistance $R_{arm}$, $N_{HB}$ HBSMs and $N_{FB}$ FBSMs. Thus, the total number of SMs per arm is $N = N_{HB}+N_{FB}$. All HBSMs consist of two IGBTs $S_1$ and $S_2$, two antiparallel connected diodes $D_1$ and $D_2$, and a capacitor $C$. Regarding FBSMs, there are two more IGBTs $S_3$ and $S_4$, and two more diodes $D_3$ and $D_4$, as shown in Fig. 1(c). In addition, the converter is connected to the grid through a grid inductance $L_g$ and inductor resistance $R_g$.

The fault operation sequence of the HMMC is investigated based on the analytical model developed in [8]. When a dc-side fault occurs, the dc-line current rapidly increases until reaching a pre-defined threshold (e.g. 2-3 times the nominal current). Therefore, all IGBTs in the SMs are switched OFF and the MMC starts the blocked state in a diode rectifier mode. During the diode rectifier mode, the lower arm current related to the phase with highest value, and the upper arm current related to the phase with lowest value, become zero first. Under such conditions, the converter can experience five different stages from six-diode rectifier mode to two-diode rectifier mode [8].

During the two-diode rectifier mode, the smallest number of FBSMs inserted in the fault current path is expected. In this way, such stage is analyzed aiming to evaluate the minimum number of FBSM required to successfully block a dc fault. The two-diode rectifier mode is illustrated in Fig. 2 considering $v_{bn}(t_0) < v_{cn}(t_0) < v_{an}(t_0)$ at the blocking instant $t = t_0$.

Assuming that the forward voltage drop across the free-wheeling diodes in the blocked SM is neglected and the capacitor voltage across all SMs are balanced at $V_c$, the following differential equation can be obtained from Fig. 2:

$$2N_{FB}V_c = v_{ll} - (2L_{arm} + 2L_g + L_{sc})\frac{di_{dc}}{dt} - (2R_{arm} + 2R_g + R_{sc})\, i_{dc}, \quad (1)$$

where $v_{ll}$ is the line-to-line ac voltage ($v_{ll} = v_{ab}$ from Fig. 2), $L_{sc}$ and $R_{sc}$ are the short circuit inductance and resistance, respectively. Aiming to achieve the converter dc fault blocking capability, the HMMC should be capable to handle with dc fault only using the reverse biased voltage generated by FBSMs. Under such conditions, the blocking voltage formed by two series arm voltages on the left side of (1) should be greater or equal than the expression on the right side of (1). For the sake of simplicity, the resistive voltage drop across the resistances and the voltage across the inductors can be neglected. Moreover, assuming that the peak line-to-line ac voltage $\hat{V}_{ll}$ is the worst-case condition for the converter dc fault blocking capability, the following relation can be obtained from (1):

$$2N_{FB}V_c \geq \hat{V}_{ll}. \quad (2)$$

As noted, the HMMC dc fault blocking capability is strictly related to the number of FBSMs and the SM capacitor voltage. In this way, considering that the $-V_c$ state of the FBSMs is not allowed to be generated, the range of the generated total arm voltage is from 0 to $NV_c$. Thus, for a maximum modulation index, the dc and peak ac phase voltages can be described by [4]:

$$V_{dc} = NV_c, \quad \widehat{V}_{an} = \frac{1}{2}V_{dc}. \quad (3)$$

On the other hand, if $N'_{FB}$ FBSMs are allowed to generate the $-V_c$ state in each arm, the arm voltage range is extended from $-N'_{FB}V_c$ to $NV_c$. Therefore, the dc and peak ac phase voltages are given by [4]:

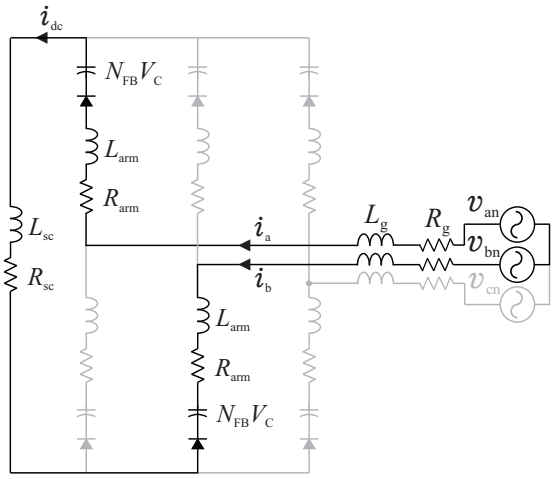


Fig. 2. Equivalent circuit model of an HMMC in blocking mode: Two-diode rectifier, when $v_{bn}(t_0) < v_{cn}(t_0) < v_{an}(t_0)$. Adapted from [9].

$$V_{dc} = (N - N'_{FB})V_c, \quad \widehat{V}_{an} = \frac{N + N'_{FB}}{2(N - N'_{FB})}V_{dc}. \quad (4)$$

To achieve the dc fault blocking capability, the blocking voltage formed by two series arm voltages, each at different phases, should be greater than the peak line-to-line ac voltage, as given $2N_{FB}V_c \geq \sqrt{3}\widehat{V}_{an}$.

$$N_{FB} \geq \frac{\sqrt{3}}{4}(N + N'_{FB}). \quad (5)$$

Moreover, aiming to ensure sufficient charging and discharging times for the HBSMs to balance their capacitor voltages within each fundamental period, $0 \leq N'_{FB} \leq 1/3N$ is required [4]. Therefore, considering that no FBSM generates $-V_c$ (i.e. $N'_{FB} = 0$), the number of FBSMs per HMMC arm must be greater than 43 % through (5). In addition, if the maximum number of FBSM generating $-V_c$ is allowed (i.e. $N'_{FB} = 1/3N$), more than 58 % of the total N should be FBSMs. As noted, the maximum number of FBSMs allowed to generate $-V_c$ is 33 % of the total N, while the minimum requirement of FBSMs needed to ensure the HMMC dc fault blocking capability is 58 %, in this condition. Therefore, the next sections illustrate the combination of HMMC with dc CB aiming to reduce the minimum number of $N_{FB}$ required for secure dc fault blocking.

## III. Case Study

Aiming to evaluate the combination of dc CB with HMMC, a 150 MW/150 kV point-to-point MMC-based HVdc system is employed in this case study, as shown in Fig. 1(a). This configuration has two converter stations, and each converter station is composed of one HMMC or MMC. For this analysis, $N'_{FB} = 0$, i.e. the $-V_c$ state of the FBSMs is neglected. The hybrid dc CB breaker is designed to provide the same response time to clear the dc fault current for all solutions. Moreover, the number of series main breaker modules with parallel connected MOV is defined by each dc CB design that is analyzed in the next sections.

A pole-to-pole permanent dc fault is performed through simulations using the PLECS software. Under such conditions, only the rectifier MMC station is modeled at switch level. In addition, the short circuit path is modeled by an inductance $L_{sc} = 10$ mH in series with a resistance $R_{sc} = 0.1\ \Omega$, which represents an ideal short circuit conditions in an overhead transmission line close to the rectifier MMC station. Moreover, no additional dc fault current limiting inductance is considered. In order to increase the simulation speed, the number of SM per arm is limited to $N = 10$. The main parameters of the system under study are presented in Tab. I. For such purpose, three different cases are studied:

- Case 1: MMC composed only of HBSMs. Moreover, dc CB is considered.
- Case 2: HMMC with 80 % of HBSM and 20 % of FBSM. Moreover, dc CB is considered.

- Case 3: HMMC with 50 % of HBSM and 50 % of FBSM. Moreover, dc CB is neglected;

TABLE I
MAIN PARAMETERS OF THE POINT-TO-POINT MMC-BASED HVDC SYSTEM.

| Parameters | Values |
|---|---|
| Rated power | 150 MW |
| dc-link voltage ($V_{dc}$) | 150 kV |
| Peak phase voltage ($\widehat{V}_{an}$) | 66 kV |
| Nominal dc line current | 1 kA |
| Total number of submodules ($N$) | 10 per arm |
| Nominal MMC SM voltage ($V_{SM}$) | 15 kV |
| Submodule switching frequency | 225 Hz |
| Submodule capacitance ($C$) | 1 mF |
| Arm inductance ($L_{arm}$) | 20 mH |
| Arm inductor resistance ($R_{arm}$) | 0.1 Ω |
| Short circuit inductance ($L_{sc}$) | 10 mH |
| Short circuit resistance ($R_{sc}$) | 0.1 Ω |

## IV. RESULTS

Figure 3 shows the dc fault response for the Case 1, which considers an HB-MMC with dc CB solution. In this way, a pole-to-pole permanent dc fault is performed at t = 0.1s. As observed in detail, this solution can interrupt the fault current in about 2.8 ms, which can be divided in three stages. The dc current is flowing by the ASB during the first stage. When the dc fault is detected ($\approx$ 200 $\mu$s), the dc fault current is commutated to the MSB reaching a dc current peak value of around 3.7 per unit (pu). Therefore, the energy is absorbed through the MOV path by around 1.6 ms. Moreover, the breaker voltage can reach 2 pu during the dc fault, as illustrated in Fig. 3 (b). In addition, the SM capacitor voltages present a maximum overvoltage of less than 9 % during the dc fault, due to the fast blocking state of the converter after fault detection, as illustrated in Figs. 3 (c) and (d),.

The dc fault response employing an HMMC with dc CB is illustrated in Fig. 4. In this way, the Case 2 is analyzed, which considers 20 % of FBSMs per MMC arm. The dc CB is design aiming to provide the same response time in about 2.8 ms to clear the dc fault current. Under such conditions, a reduction of about 38 % in the dc peak current is observed when compared to the Case 1. In addition, the breaker voltage is reduced by around 53 %. The maximum SM capacitor overvoltage is less than 27 %. It is important to remark that the SM capacitor overvoltage is one the most important constraints in the design phase of the HMMC with dc CB. In this way, the maximum SM capacitor overvoltage below 30 % is considered an acceptable margins for SM capacitors and power semiconductors.

Figure 5 shows dynamic behavior of Case 3 during dc fault. Such solution can interrupt the dc fault current in around 2 ms reaching a dc current peak value of around 2 per unit (pu). It is important to mention that such HMMC solution presents 50 % of FBSM, which can be considered suitable in comparison to the minimum number of 43 % obtained in (5). However, the SM capacitor voltages still present a maximum

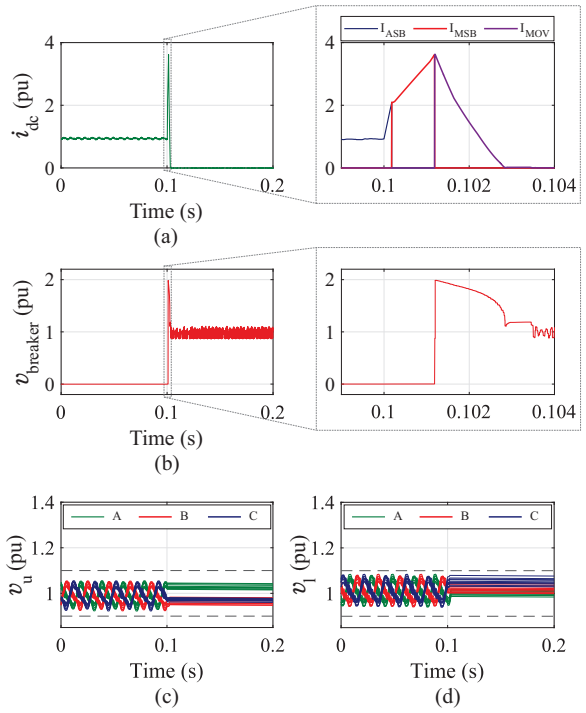


Fig. 3. Dynamic behavior of HB-MMC with dc CB during dc fault (Case 1): (a) dc current; (b) breaker voltage; (c) upper arm SM capacitor voltages; (d) lower arm SM capacitor voltages. *Remark:* $I_b = 1kA, V_b = 150kV$ are base values and $V^*_{SM} = V_b/N$.

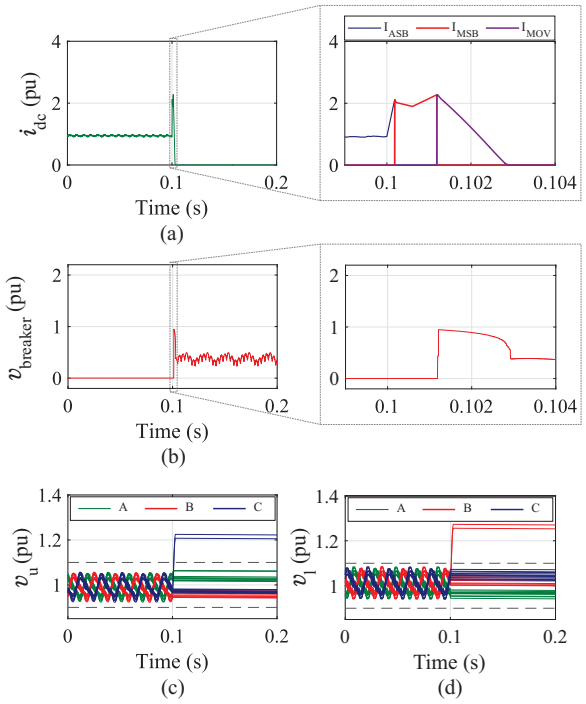


Fig. 4. Dynamic behavior of HMMC with dc CB during dc fault (Case 2): (a) dc current; (b) breaker voltage; (c) upper arm SM capacitor voltages; (d) lower arm SM capacitor voltages. *Remark:* $I_b = 1kA, V_b = 150kV$ are base values and $V^*_{SM} = V_b/N$.

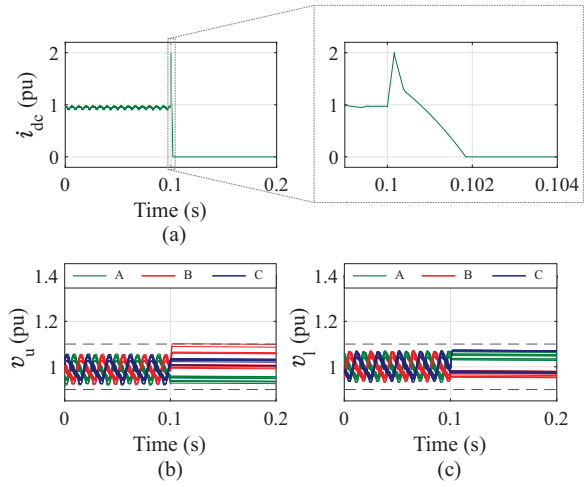


Fig. 5. Dynamic behavior of HMMC without dc CB during dc fault (Case 3): (a) dc current; (b) upper arm SM capacitor voltages; (c) lower arm SM capacitor voltages. *Remark:* $I_b = 1kA$ is the base value and $V^*_{SM} = V_b/N$.

overvoltage by around 10 % during the dc fault, as shown in Figs. 5 (b) and (c). Such feature is observed considering that the analytical analysis performed in (5) neglects the energy stored in the arm and short circuit inductances. Nevertheless, the maximum SM capacitor overvoltage by around 10 % is considered an acceptable margins for SM capacitors and power semiconductors.

The comparison among the three solutions is summarized in Tab II, which the best performances are highlighted. Assuming the dc CB power module is the same as the MMC, the number of power modules per dc CB can be obtained based on the maximum breaker voltage in Fig. 3 (b) and Fig. 4 (b). In this way, Case 1 presents a maximum breaker voltage in about $2V_{dc}$, which is equivalent to the number of power modules of two arms in the MMC (33 % of the amount used in the converter). Similar analysis is performed for Case 2, which needs half the number of power modules of Case 1. Therefore, Case 3 employs the largest total number of power modules, which is about 13 % more than Case 1.

## V. Conclusion

This work provides a dc fault blocking approach employing both HMMC and dc CB able to extinguish the dc fault in an MMC-based HVdc system. The simulation results show that for this combination the number of FBSM can be reduced by about 60 % compared to typical HMMC solutions, while the total number of power modules used in the HMMC with the dc CB can be reduced by around 9 %. Moreover, the peak value of dc fault current and the breaker voltage can be decreased by around 38 % and 50 %, respectively, when HMMC with dc CB solution is employed.

The FBSM reduction has a significant impact on reducing capital expenditure and operating expenses of HMMCs. Moreover, the use of the dc CB is important to enable the selective protection schemes, which is a key to the maturity of MVdc grids. In this way, it is important to mention that the methodology proposed in this work can be extended to find the best HMMC with dc CB design considering other factors such as, type of dc failure, effect of long short-circuit impedance, device overvoltage and overcurrent limits.

TABLE II
Comparison among three different rectifier station solutions for a point-to-point MMC-based HVdc system.

| Parameters | Case 1 | Case 2 | Case 3 |
|---|---|---|---|
| Number of power modules per MMC station (*) | 1 | 1.2 | 1.5 |
| Number of power modules per dc circuit breaker (*) | 0.33 | 0.17 | N/A |
| Total number of power modules (*) | 1.33 | 1.37 | 1.5 |
| Time to extinguish the dc fault (ms) | 2.8 | 2.8 | 2 |
| Peak value of the dc fault current (pu) | 3.7 | 2.3 | 2 |
| Peak value of breaker voltage during the dc fault (pu) | 2 | 1 | N/A |
| SM capacitor overvoltage during the dc fault (%) | 8 | 27 | 10 |
| Enables the selective protection scheme | Yes | Yes | No |

*Base value: number of power modules per MMC station in Case 1.


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