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Partial power processing DC/DC MPPT Converters in Solar PV applications: Overview of Architectures

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***Abstract*— This paper presents an overview of partial power processing (PPP) DC/DC converter architectures in PV applications which has maximum power point tracking (MPPT) capability. The main objectives of PPP in PV applications target to increase the power density and efficiency while reducing overall cost. The converters applied to the PPP is called partial power converter (PPC) and there are three most actively explored topologies in the solar industrial fields: differential power converter (DPC), fractional power converter (FRPC), and partial power converter (PPC). Some previous studies analyze and compare several PPCs in a highly qualitative manner. In this work, PPP topologies are classified in a comprehensive manner, and their power processing capabilities are analyzed with the volt-ampere (VA) area modeling. Moreover, quantitative comparison of PPP topologies by means of utilization factor (UF) is presented and compared for a utility scale solar park scenario. Finally, overview of PPP architectures are compared and organized with the table.**

Keywords— Partial power processing, MPPT converter, Novel PV architecture

I. INTRODUCTION

Partial power processing (PPP) DC/DC architectures for large Solar PV parks have been an interesting proposition for PV industries since the PPPs offers many possibilities to improve the efficiency, power density (PD) and reduce cost of the MPPT DC/DC converters [1]–[3].

The most actively researched PPP architectures in literature are: differential power converter (DPC), fractional power converter (FRPC), and partial power converter (PPC). These converters are categorized based on the power processing features of converter. DPC [4]–[18] processes the differential power of PV cells. In DPC it is possible to connect many numbers of converters in series or parallel manner to the input PV string. The main function of DPC is compensating the power imbalance between series or parallel connected sub-converters.

Another PPP architecture is FRPC [19]–[22]. In FRPC, an auxiliary power source is adapted to decrease the voltage stresses to the converter and make it possible to processes the partial power (PP). Owing to the low voltage stresses on the converter components, therefore, converter has the possibilities to have high power density structure.

The third PPP scheme is PPC [23]–[30]. PPC achieves partial power flow by the current or voltage feedback path in the converter. The PPC MPPT converter designed to process partial power of PV which is targeted to track MPP of PV string. With the processing of partial current and voltage of PPC, it is possible to reduce the processed power between switching devices which yields the increase of power density of power converter. PPC is again categorized into input series output parallel (ISOP) and input parallel output series (IPOS) PPC. Furthermore, IPOS is also divide into two groups based on the number of input/output ports: 2P-IPOS and 3P-IPOS. Fig. 1, shows the categorization of PPP architectures.

There are many previous studies where the PPC topologies are analyzed and characterized with qualitative manner. The application of different PPCs and mentioning of the converter topologies are also discussed in previous studies. However, it is difficult to find the comparison of the PPC topologies in quantitative terms.

This paper presents the overview of the different PPP architectures in PV application with quantitative comparison. The differences of each architectures are highlighted not only with the description of architectural differences and power processing flow of each PPP architectures but also by means of comparing utilization factor (UF) which is the quantitative indicator of assessment for the expensive active semiconductors and passives. Finally, overview of all PPP architectures is organized and compared in a table that highlights the main features of each concept.

II. CONCEPT OF PARTIAL POWER PROCESSING ARCHITECTURES

Partial power processing is the concept that the converter processes only a part of the total input power in order to generate necessary output. In this concept, most of the input power is directly bypassing through the converter elements as shown in Fig. 2. (a). The converter is only processing partial power (PP) of the input power and convert it to the demanded output. In Fig. 2. (b), power delivery process with VA area model of PPC are described. VA area model is one of the

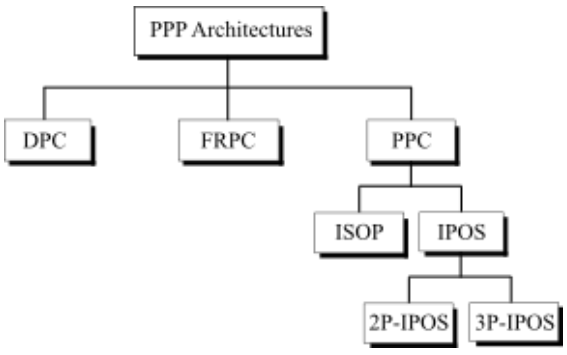


Fig. 1. Categorization of partial power processing architectures.

technique that visualizes the amount of processed power and bypassing power [1]. The VA area model shows that the converter only processes partial power and the rest of the power which is call direct power (P_{direct}) is bypassing trough the converter elements without power processing. As shown in the VA area model, input and output of the converter is processing either "full current and partial voltage" or "partial current and full voltage".

It is possible to see in the VA area model that the partial power in PV application is achieved by processing the targeted voltage or current of input and output which is optimally selected for MPPT. The decrement of input and output current/voltage makes the less current/voltage stresses to the PPC switches and eventually yields lower losses on the semiconductor devices.

In Fig. 3, the architectural concept and power flowing process of differential power converter (DPC) with the VA area model are plotted. DPC is one of the PPP concept for maximum power point tracking (MPPT) converters that processes differential power ($P_{diff,n}$) of PV cells. PV string is comprising with many numbers of PV cells connected in parallel and series. The power on each PV cells are possible to have different powers since the solar irradiation on the each PV cells can be different owing to the position of sun, clouds, and the gradient of PV string. The power difference between PV cells inducing $P_{diff,n}$. DPC processes the power by compensating current unbalances between each PV cells that induced by the $P_{diff,n}$. The voltage stress between $P_{diff,n}$ is as much as cell voltage and current flowing through DPC is the current imbalance between cells which is small value compare to the full current of the PV string. Therefore, the power processing with the full voltage-partial current, DPC is possible to achieve PPP. Even though DPPs are possible to achieve PPP architecture, high number of converters should be connected in series between each PV cells to flow partial current also to achieve MPPT. This makes the high number of counting of switching devices that yields the higher cost. The high cost of the architecture and the incapability of per string MPPT are the biggest limit of the DPC.

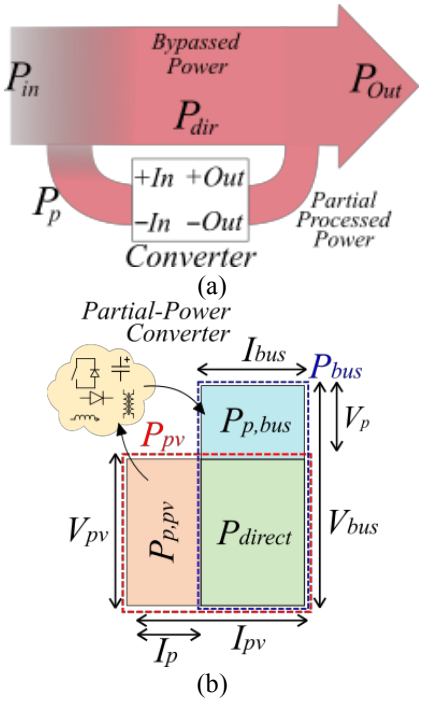


Fig. 2. Concept of partial power converter (a) power flow diagram (b) VA area model.

The second PPP concept is fractional power converter (FRPC) which is shown in Fig. 4. The key point of the FRPC is that the converter adapts auxiliary DC voltage source to achieve PP. As shown in the VA area model, the converter has less voltage stresses compare to the PV voltage since input FRPC is sharing low voltage of auxiliary DC source (V_{aux}). Hence, the converter is processing full current of the PV string but the processed voltage is lower voltage compare to the PV string which is full current-partial voltage PPP characteristics. Moreover, the converter is conducting MPPT per string with the auxiliary DC source unlike the DPC that was not possible to conduct individual MPPT per PV string. Nonetheless of the PPP and per string MPPT capabilities, FRPC needs one auxiliary DC source per one converter. This means that the redundant DC source of FRPC is still the factor that limits the cost of the architecture.

Partial power converter (PPC) is the other PPP concept for the MPPT converter. In order to build the PPC, to have the current feedback path between PV and bus is the most important factor. This feedback connection makes energy conservation of system possible and also makes partial voltage.

$$V_p = V_{bus} - V_{pv}, \tag{1}$$

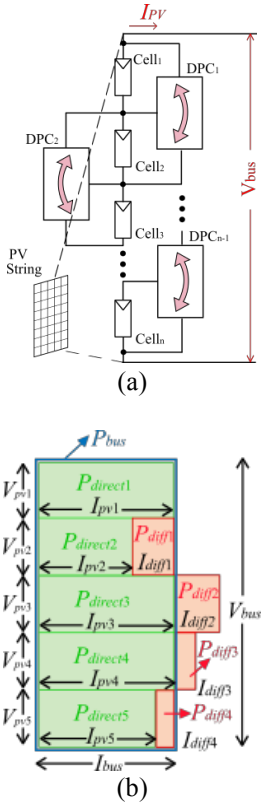
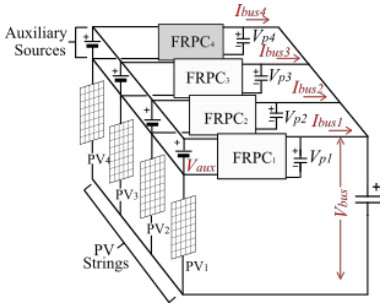
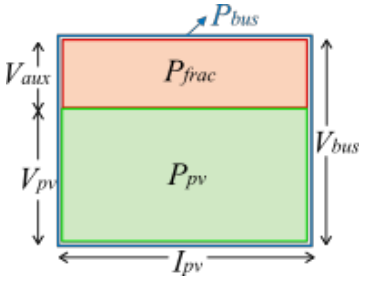


Fig. 3. Concept of DPC (a) architecture (b) VA area model.

where V_p is partial voltage and V_{bus} is bus voltage, and V_{pv} is PV voltage.



(a)



(b)

Fig. 4. Concept of FRPC (a) architecture (b) VA area model.

Moreover, PPC demands an isolation to prevent short circuit between PV and bus which generated from the current feedback path [1]–[3].

Based on the voltage rate on PV and bus, PPC can be categorized in two cases: input parallel output series (IPOS) and input series output parallel (ISOP) architectures.

Fig. 5 (a) shows the block diagram of IPOS PPC for MPPT converter. The voltage of PV applied to the input of IPOS and the current of PV divided by the parallel node on input of IPOS. The positive output port of IPOS is connecting to the bus and the negative output port of IPOS is connecting to the positive input port and generating feedback path. Partial current ($I_{p,n}$) is compensating the PV current and makes the partial current processing possible on the PV side, and the partial voltage (V_p) is compensating bus voltage and allows the partial voltage processing possible on the bus side. IPOS is only processing partial power owing to the partial current and voltage processing of the PV and bus sides, and the rest of the power is bypassing through the common ground of the converter.

Another PPC category is shown in Fig. 5. (b), (c), which is called ISOP. There are two different types of input series output parallel PPCs: 2P-ISOP and 3P-ISOP.

2P-ISOP which is plotted in Fig. 5. (b), has opposite structure compare to the IPOS which the input is connected in series to the PV and the parallel connection exists on bus side. $I_{p,n}$ is compensating the bus current and makes the partial current processing on the bus side and V_p is compensating the PV voltage and makes the partial voltage processing on the PV side possible. Like the IPOS, the partial power is processed from the 2P-ISOP and the rest of the power is flowing through the common ground of the converter.

3P-ISOP is comprising with one isolated converter and auxiliary converter that conducts MPPT. The isolated converter makes the current feedback loop for the PPPs and managing the partial voltage of the converter. The MPPT converter stage of 3P-PPC is controlling the PV current and tracking the MPP. MPPT converter port is conducting partial voltage processing and isolated converter stage is conducting partial current processing.

VA area model also shows the characteristics of each PPC topologies and shows the clear power rate of each part of the converter elements. The partial power generation and delivery processes of PPCs are possible to be known in VA area model in Fig. 6.

Fig. 6. (a), shows the VA area model of IPOS. In order to make the IPOS structure, bus voltage should be higher than the PV voltage which also implies that IPOS is appropriate topology for step-up applications. PV side and bus side partial power can be calculated as following:

$$P_{p,pv} = V_{pv} I_p \,, \tag{2}$$

$$P_{p,bus} = V_p I_{bus}, \tag{3}$$

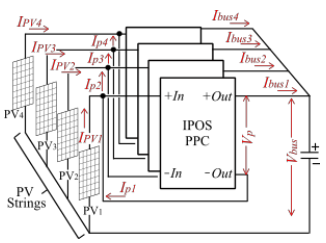
where V_{pv} is PV voltage, I_p is partial current, V_{bus} is bus side voltage, V_p is partial voltage.

As discussed before, partial current is processed from the PV side and partial voltage is processed from the output side. The partial powers of $P_{p,pv}$ and $P_{p,bus}$ are processed by IPOS and the common bypassing power which is

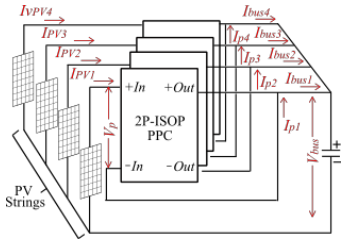
$$P_{direct} = V_{pv} I_{bus}, \tag{4}$$

is flowing through the ground of converter.

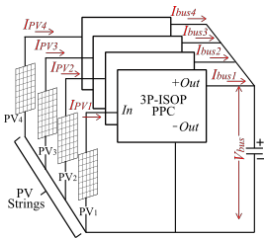
VA area model of 2P-ISOP is plotted in Fig. 6. (b). VA area model of the converter has opposite characteristics compare to the IPOS PPC as the description with the block diagram. The higher PV voltage appears to build 2P-ISOP and



(a)



(b)



(c)

Fig. 5. Concept of PPC architectures (a) IPOS (b) 2P-ISOP (c) 3P-ISOP.

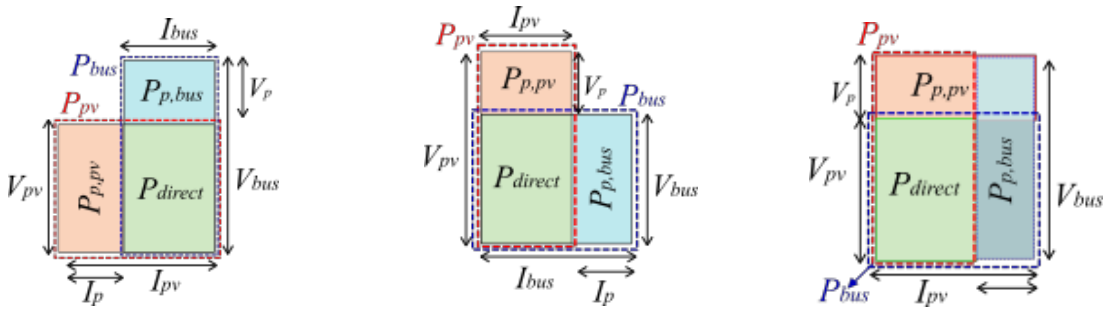


Fig. 6. VA are models of (a) IPOS (b) 2P-ISOP (c) 3P-ISOP.

this implies that the converter is appropriate solution for the step-down applications. The partial power on the PV and bus side can be calculated as following:

$$P_{p,pv} = V_p I_{pv}, \tag{5}$$

$$P_{p,bus} = V_{bus} I_p, \tag{6}$$

The VA area clearly shows that the partial voltage is processed on the input side and the partial current is processed from the bus side of 2P-ISOP. The rest of the bypassing power which is

$$P_{direct} = V_{bus} I_{pv}, \tag{7}$$

is flowing through the ground of converter.

In Fig. 6. (c), VA area model of 3P-PPC is described. VA area model of 3P-PPC has different structure compare to the IPOS and 2P-ISOP. Unlike previous two PPCs, partial voltage of 3P-ISOP is manipulated by the isolated converter and the partial power through the primary and secondary sides of isolated converter are calculated the same as (5) and (6).

It is possible to see from the diagram and the partial power equations that the MPPT current is flowing through the PV side converter stage with partial voltage processing and the isolated converter is circulating power with the partial current. 3P-ISOP is possible to apply to both step-up and step-down solutions since the isolated converter is flowing partial power in a bidirectional way. The bidirectional power flow is possible to compensating partial power from both PV and bus.

III. Overview of Partial Power Processing Architectures

In this section overall comparison of PPP architectures are compared. In order to analyze and compare each of PPC topologies quantitatively, a common condition is required which written in table I. The condition is assuming utility condition of PV application.

TABLE I - COMPARISON CONDITION

Paramters	***Symbol***	***Value***
Maximum power voltage	$V_{pv,MPP}$	1 kV
Battery voltage (FRPC)	V_{aux}	200 V
Panel voltage	$V_{pv,p}$	12 V
Bus voltage	V_{bus}	1.2 kV
PV current	I_{pv}	10 A
Nominal Power	P_{sys}	10 kW

In order to compare the PPP architectures, there needs a quantitative standard to see the characteristics of each PPP topologies more clearly. Utilization factor (UF) is one of the factor that can compare the PPP architecture in quantitative manner [1],[31]. UF shows how much total power of system is utilized by the devices. Lower UF implies that the higher power customer can utilize from the PVs and higher power density converter can achieve. The equation of UF can be written as following:

$$UF = P_{PV} / \sum_{i=1}^{n} V_{Qi} I_{Qi,rms}, \tag{8}$$

where V_{Qi}, I_{Qi} are the voltage and current on the semiconductor devices.

The processed power ratio (K_{pr}) is another quantitative factor which shows the ratio of the PV power and processed partial power. Hence, the lower K_{pr} means PPC can process lower power through it. K_{pr} is expressed as following:

$$K_{pr} = \frac{P_p}{P_{pv}} = \frac{V_p I_p}{V_{pv} I_{pv}}, \tag{9}$$

where P_p is processed power, P_{pv} is PV power, V_p is partial voltage, I_p is processed current, V_{pv} is PV voltage, and I_{PV} is PV current.

Fig. 7 shows the utilization factor of PPCs with increasing number of PV strings. DPC has the lowest UF among all the cases and this concept only can conduct MPPT per cell. Hence, the possibilities of applying DPP to the PV system is lower than the other topologies. On the other hand, FRPP has the highest UF in all the cases. However, FRPP needs higher counting of DC source as increasing of PV string counting

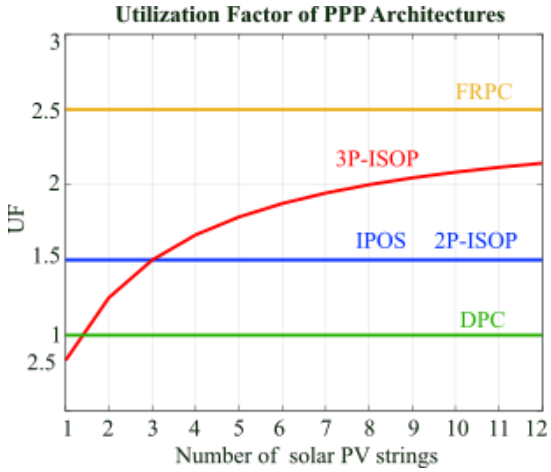


Fig. 7. Utilization factors of PPPAs

TABLE II - OVERVIW OF PPP ARCHITECTURES

PPP		*MPPT per string*	*Auxilary Source*	*Transformers*	*Cost*	K_{pr}	*Overall Rate*
DPC		X	X	Based on Purpose	+	2	+
FRPC		O	O	X	-	5	++
PPC	IPOS	O	X	O	+++	6	+++
	2P-ISOP	O	X	O	+++	6	+++
	3P-ISOP	O	X	O	+++	5	+++

which induces the decrease of PD. The higher counting of auxiliary source impact on the increasing of costs. In the case of single PV string application, IPOS and 2P-ISOP has the highest UF among the topologies that does not demand auxiliary source. However, if the number of PV strings are increasing, 3P-ISOP has more chances to have higher power density than IPOS and 2P-ISOP. The overview of all topologies are organized in the table II. The overview implies that PPCs is the most advantageous topology with comparing it to the others. As discussed before, the auxiliary voltage source limits in terms of the cost efficiency and PD, even if FRPC has the highest UF. DPC has the lowest advantage owing to the incapability of per string MPPT and the low cost efficiency.

IV. CONCLUSION

An overview of possible PPP architectures for DC/DC MPPT converters for solar PV application is presented. There are three big categories of PPP architectures: DPC, FRPC and PPC. Owing to the low UF and incapability of per string MPPT, DPC is not a perfect solution for PV applications. On the other hand FRPC and PPCs have high UF potential for per string MPPT. FRPC has the highest UF compare to the other PPCs. On the other hands, the converter requires redundant DC sources for each MPPT converters to achieve PPP. IPOS and 2P-ISOP has higher UF than 3P-ISOP in single PV string application. However, the increasing number of PV strings counting, 3P-ISOP has more advantage in terms of UF.

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