Digital Object Identifier 10.1109/PEDG54999.2022.9923237

2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)

Networking Aspects based on the Talkative Power Concept for DC Microgrid Systems

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***Abstract*—The talkative power concept is a simultaneous power-line communication and energy transfer technique which integrates data modulation into a power converter. The information sequence is deterministically represented by the ripple, which superimposes the output voltage. With a few exceptions, so far emphasis has been on scenarios where only a single node is actively transmitting data in a certain time slot in simplex mode. In microgrid applications, however, multiple active power sources are of interest as well. Examples include battery management systems, smart metering, electricity trading systems, and smart grids with several power sources, energy storage devices, and data receivers. In this contribution, bus networking aspects based on the talkative power concept are presented for scenarios with several active nodes and for full-duplex communication. The paper addresses potential multiple access techniques as well as duplexing schemes for connected power converters supporting bidirectional power and information flow. In numerical results, a spread spectrum scheme based on orthogonal variable spreading factor codes in conjunction with frequency shift keying (FSK) is presented for four simultaneously active buck converters with a sum data rate of 500 kbps at a switching frequency of 1 MHz. In general, with 2-ary FSK, the maximum achievable sum data rate is half of the switching frequency in a synchronous setup.**

***Index Terms*—DC microgrids, simultaneous information and power transfer, power-line communication, pulse width modulation converters, spread spectrum communication.**

I. Introduction

Since the mid 1960s, pulse width modulation (PWM) became the mainstream waveform to control switched-mode power converters. For about four decades emphasis has been on power conversion only. This situation has changed by the observation that small duty-cycle perturbations can be exploited for simultaneous data transmission, as proposed in [1]. Already in this original paper, a network of distributed DC-DC converters sharing the same bus voltage has been proposed. Subsequently, more effort has been spent on different modulation schemes, suitable power converter topologies, and on applications like visible light communication. Recently, in a Nature publication the concept has been dubbed *talkative power* [2]. Subsequently, we adopt this term, although a variety of other names have been suggested.

The *talkative power* concept is a simultaneous power-line communication and energy transfer technique which integrates data modulation into the switching signal of a power converter. In this paper, DC-DC power conversion is assumed. Fig. 1 depicts a block diagram of the *talkative power* concept for the example of a synchronous buck converter. The buck converter can be implemented as a half bridge with switches S_1 and S_2, followed by a low-pass filter. Given a fixed DC input voltage $v_1(t) = V_1$ and assuming PWM with duty cycle δ, $0 < \delta < 1$, the half bridge outputs a rectangular signal with constant amplitude. The low-pass filter, frequently a second-order LC filter, provides a smoothed output voltage $v_2(t) = V_2 + v_{\text{rip}}(t)$. The DC component of the output voltage is known to be $V_2 = \delta V_1$ in continuous conduction mode (CCM), while the ripple voltage $v_{\text{rip}}(t)$ is a deterministic function of the switching pattern. **The core idea of the *talkative power* concept is to replace the classically-used continuous PWM switching signal with an information-carrying switching signal $s(t) \in [\text{on}, \text{off}]$. In this way, the ripple contains the data stream to be transmitted.** For instance, the information can be represented by duty-cycle-dependent and data-dependent

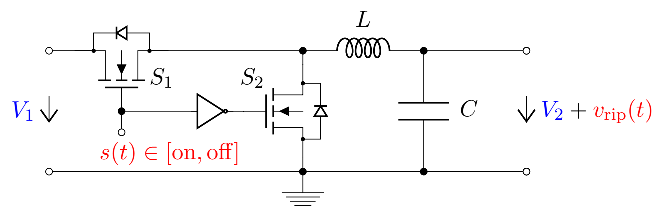

Fig. 1. *Talkative power* system concept explained for the example of a synchronous buck converter. The ripple voltage $v_{\text{rip}}(t)$ is a function of the information-carrying switching signal $s(t)$. DC voltages are in blue color, COM signals in red color.

- pulse widths
  (variable pulse width modulation, VPWM)
- pulse positions
  (variable pulse position modulation, VPPM)
- phase shifts
  (variable phase shift keying, VPSK), or
- frequency shifts
  (variable frequency shift keying, VFSK),

see [4], [5].

It is important to mention that, from a power electronics (PE) point of view, the ripple voltage should be within tolerable ripple limits to comply with power quality and

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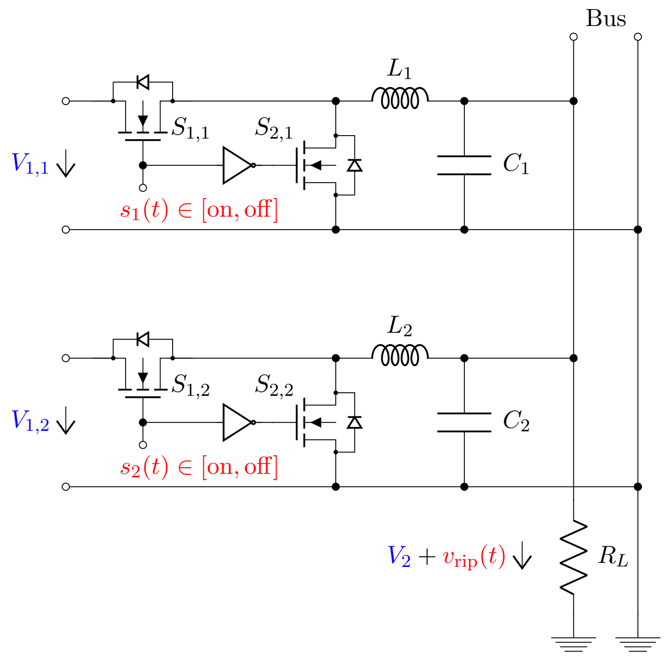


Fig. 2. Networked *talkative power* system concept. Several nodes can be connected to the same bus, for illustrative purposes two nodes are shown in this figure. Source nodes are equipped with a power converter, here a buck converter. Sink nodes (i.e., data recovery units) with high input impedance can be connected to the bus without power converter – sink nodes are not shown here.

electromagnetic interference (EMI) standards. Vice versa, from a digital communications (COM) point of view, the ripple is the useful signal. Besides distortions by noise, co-channel interference arises if two or more active power converters share the bus at the same time. Reliable data recovery is only possible if the signal-to-interference-plus-noise ratio (SINR) is sufficiently large. This trade-off between PE and COM requirements can be mitigated by spreading and channel coding techniques [3], [4] as well as an advanced fully-digital receiver design [4]. Among the advantages of the *talkative power* concept compared to coupler-based power-line communication technologies are simplicity and low hardware cost, short latency, and the possibility of reduced EMI in conjunction with random coding and/or filtering.

In this paper, we address networking aspects, also referred to as multiuser aspects. We assume that several power generators, storage devices, and data recovery units (hereafter referred to as source nodes, storage nodes, and sink nodes) are connected to the same DC bus, see Fig. 2. Each source node is equipped with its own power converter. The power converters are the energy and data transmitters. The maximum number of source nodes is limited in practice. In contrast, any number of receiving units can be connected to the bus if their input impedance is high. A receiving unit may consist of an anti-aliasing filter, an analog-to-digital converter, and a microcontroller. These sink nodes are not capable of transmitting data, but can optionally be joined with a power converter to enable bidirectional data transmission. In the latter case, the microcontroller can be shared between transmitter and receiver.

In the prior art, most work assumes that only one node transmits data in a given time slot to avoid co-channel interference. Exceptions include [6], where direct-sequence code-division multiple access (DS-CDMA) is applied for harmonic reduction and communication. DS-CDMA is a spread-spectrum technique. Due to spreading, several nodes can transmit simultaneously. Two active nodes are reported in the experimental results of [6] applying maximum length spreading sequences. Furthermore, according to the state-of-the-art, unidirectional power and information flow is assumed in most papers between dedicated transmitters and receivers. In microgrids and networked energy storage systems, however, bidirectional power flow is fundamental. In many applications, bidirectional information exchange is important as well. **The challenge is to design switching waveforms that enable reliable, bidirectional data transmission as well as energy flow between all nodes connected to the same bus. At the same time, the maximum ripple voltage should be kept below a certain threshold.** The concept studied is not tied to a specific power level and can be used in a wide range from power electronics to low-power applications. Along the same lines, the proposed concept is not tied to a specific range of switching frequencies. Current research on wide-bandgap semiconductor (GaN, SiC) switches supports our work.

Among the novel contributions of this paper are:

- Principles of multi-user communication established in the field of digital communication are transferred to the concept of *talkative power*.
- Full-duplex communication is considered for the first time in the field of *talkative power*.
- Orthogonal variable spreading factor codes are proposed for the case that all power converters are synchronized.

II. Multiple Access Techniques, Duplexing, and System Modeling

Multiple access (MA) is a family of techniques that allows multiple nodes to share a common channel [7]. In the *talkative power* concept the power is continuously distributed to all nodes without additional action. Therefore, emphasis now is on the data transfer.

- Time-division multiple access: In TDMA, the data is transmitted in allocated time slots. Only a single node is active. This scenario is assumed in most papers since [1].
- Frequency-division multiple access: In FDMA, different frequency bins are allocated to different nodes. FDMA can be realized by FSK, preferably with orthogonal subcarriers (OFDMA). The number of channels is limited though. Also, the lower subcarriers experience a larger ripple and their data rate is limited.
- Code-division multiple access: The most popular CDMA technique is DS-CDMA [6]. In DS-CDMA, each user is assigned a different spreading code. A single pulse of the

spreading code is called a chip. The ratio between chip rate and bit rate is called spreading factor.

An alternative to DS-CDMA is interleave-division multiple access (IDMA). In IDMA, each user is assigned a different interleaver together with a fixed channel encoder. IDMA is more powerful, however, at the cost of increased computational complexity particularly at the receiver side.

Other options are frequency hopping and time hopping.

- Carrier-sense multiple access: In CSMA with collision avoidance (CSMA/CA), channel sensing is performed. Transmission is initiated only if no traffic is monitored. The time slots known from TDMA are avoided, which has a positive effect on latency.
- Non-orthogonal multiple access (NOMA): All MA schemes reported so far are based on orthogonal or quasi-orthogonal signals. In the *talkative power* concept, still cross talk (i.e., co-channel interference) might occur. Therefore, NOMA schemes like superposition modulation (SM) and IDMA are worth to investigate.

Regarding *talkative power*, just one-way (i.e., simplex) communication has been considered so far. In a duplex communication system, nodes can communicate with one another in both directions. Time-division duplexing (TDD), frequency-division duplexing (FDD), and code-division duplexing (CDD) are all applicable.

Given a single active node, a discrete-time model for the ripple voltage at the output of a buck converter was calculated in [4] for arbitrary switching signals and for a constant or a time-varying input voltage. This derivation can be generalized for the case where several power converters are connected to the same bus. It can be shown that the ripple voltage is *not* equal to a linear superposition of the individual ripple voltages. The coil currents are additive, but the total current is split between the capacitors and the load resistor. The current-splitting is data-dependent. Details are dropped here for conciseness, still the results of the derivation (in the form of analytically computed voltage ripples) are reported in Sections IV and V.

III. System Design

In simulation and experimental results, the following setup is assumed and evaluated:

- Power converters: In each node a synchronous buck converter is used, because this topology supports bidirectional energy and data flows and is well analyzed. In the numerical results, the input voltage is 24 V, the bus voltage is 12 V (correspondingly, $\delta = 0.5$), and the maximum switching frequency is 1 MHz (i.e., the minimum on- and off-times are 0.5 μs).
- Modulation: The switching signals are chosen to be 2-ary FSK modulated with two amplitude levels (on and off), because this modulation scheme is simple, robust with respect to load variations [4], and robust regarding different transmission line impedances. If $\delta = 0.5$, the on and off levels are uniformly distributed for any possible data sequence, even without line coding. To maintain orthogonality, the ratio between mark and space frequencies is selected to be equal to two. In the numerical results, the chip duration is 2 μs; mark and space frequencies are 1 MHz (2 periods per chip duration) and 500 kHz (1 period per chip duration), respectively. The classical continuous PWM switching signal is replaced by the data-carrying signal. The modulation unit is fully digital, analogue hardware like a comparator is obsolete as independently proposed in [3], [4]. Previously, the data was modulated onto a carrier using an analog circuit.
- Multiple access and duplexing: In asynchronous setups, CSMA/CA is our preferred MA option due to the lack of time slots. In this paper, however, emphasis is on a synchronized setup. Therefore, DS-CDMA based on orthogonal variable spreading factor (OVSF) codes are used [7]. This code family, known from the UMTS cellular radio system, supports variable data rate, still maintaining orthogonality. In the numerical results, a spreading factor of four is chosen, i.e., up to four converters might be actively transmitting independent data streams at 125 kbps each. Accordingly, the sum data rate is 500 kbps. Alternatively, two nodes can use 125 kbps each, and one node 250 kbps. For larger spreading factors, there are many more options, i.e., data rates are widely adjustable. For instance, with a spreading factor of 32 the range is from 15.625 to 250 kbps at 1 MHz switching frequency. To avoid co-channel interference, passive transmitters are proposed to use the all-ones sequence at the input of the spreader, corresponding to the mark frequency.

  In time-critical applications with short latency, FDD and CDD are the favorable duplexing schemes. We use CDD, since CDD is matched to orthogonal spreading codes.
- Frame structure: The frame design is almost arbitrary. For example, the frame design of the CAN bus or other popular bus systems can be adopted for compatibility reasons. For the data field, we use chunks of pseudo-random binary sequences (PRBS). These chunks are repeated periodically.
- Receiver design: First, intersymbol interference is compensated by an analogue equalizer. Then, Nyquist sampling with 2-times oversampling (i.e., 4 MSa/s) is performed, which can be replaced by bandpass sampling. Afterwards, despreading and demodulation is done by a decorrelator, implemented by means of a matched filter bank. Finally, threshold detection is performed.
- Power control: Power control and communication are decoupled [3], [4]. Since power control is beyond the scope of this paper, we have used the same input DC voltage V_1 on all converters in the following simulation and experimental results. In this way, power control is not required as long as the duty cycles of all converters are the same, and large signal ripple voltage is not a function of precise DC average current share.

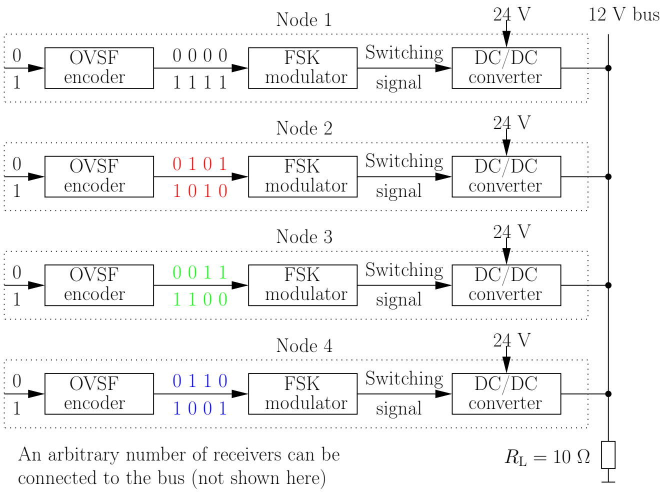


Fig. 3. Block diagram of the proposed system.

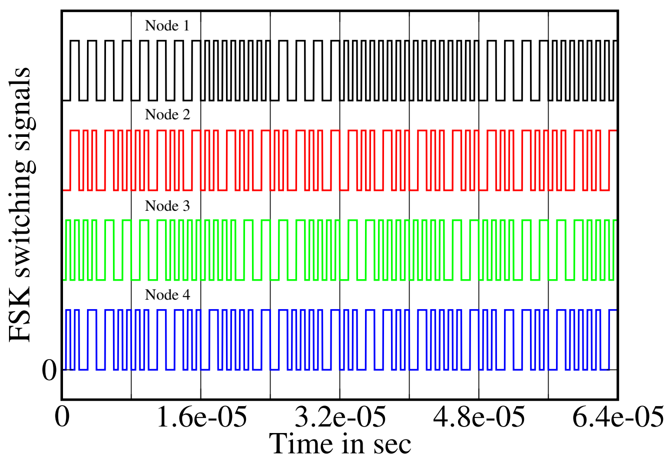


Fig. 4. Switching signals used in simulations and experiments. The vertical lines correspond to one bit duration, i.e., to four chip durations.

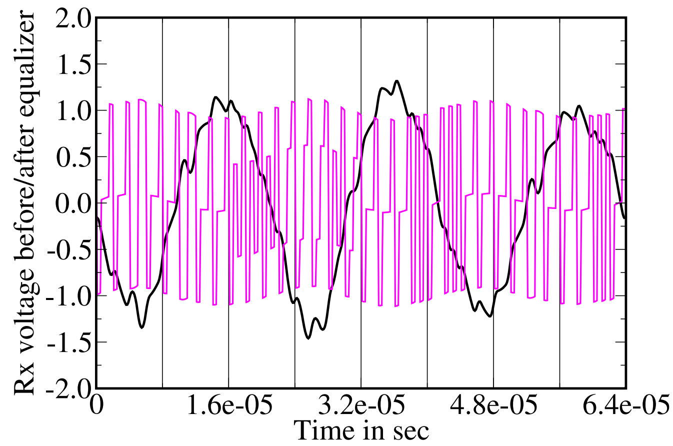


Fig. 5. Received ripple voltage before the equalizer (black color) and after the equalizer (magenta color). The DC bias is removed in this figure. The received ripple voltage is measured in Volts, the equalizer output signal is normalized.

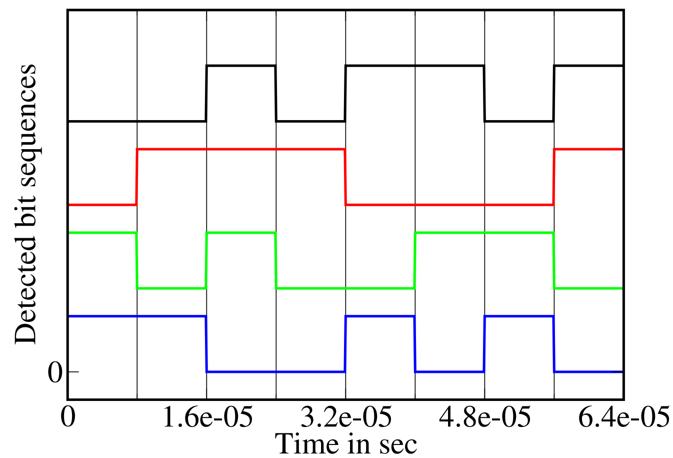


Fig. 6. Detected bit sequences.

IV. Simulation Results

A detailed block diagram of the communication units of the CDMA system under investigation is depicted in Fig. 3. Four simultaneously active nodes are connected to the 12 V bus. Their data rate is chosen to be the same. The selected OVSF code words are [0000], [0101], [0011], and [0110]. If the info bit is zero, the original OVSF codeword is selected, otherwise the inverted codeword. The chip sequence is FSK modulated. If a chip is zero, the lower (space) frequency is sent, otherwise the higher (mark) frequency. The two-level switching signals are equal to the FSK-modulated signals. Hence, the COM unit is implemented fully digital. An Ohmic load R_L is assumed.

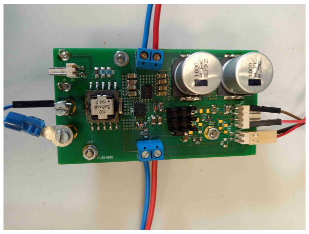
The FSK-modulated switching signals of the four power converters are shown in Fig. 4. The mark and space frequencies are clearly visible. Each signal corresponds to eight random info bits, which are repeated periodically. One period has a length of $8 \cdot 4 \cdot 2\ \mu s = 64\ \mu s$ (i.e., 8 info bits per period, 4 chips per bit, 2 μs per chip duration). The repetition facilitates frame synchronization at the receiver side.

The received ripple voltage before the equalizer (in Volts) and after the equalizer (dimensionless and arbitrarily scaled) is plotted in Fig. 5 for the steady state. Before the equalizer, i.e. on the bus, the peak ripple is about ± 1.4 V at 12 V DC bus voltage. The ripple voltage can be changed by adjusting the switching frequency and/or the cutoff frequency of the LC low-pass filter.

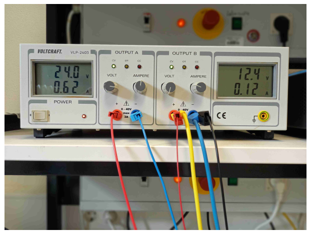
The four detected bit sequences are shown in Fig. 6. Detection has been done offline, hence delays are not displayable. Due to matched filtering, the minimum delay is one bit duration (here: 8 μs). For short lines, the transmission was error-free for all four nodes.

V. Experimental Results

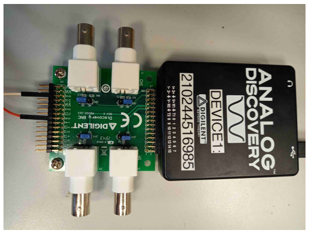
In order to validate the analytical results, an experimental testbed was developed. Four buck converters, each consisting of a half-bridge (Fig. 7 (a)) and an LC low-pass filter, form the central element of the prototype. The half bridges are custom made. The maximum switching frequency is about 2 MHz at 24 V DC input voltage. The LC low-pass filter



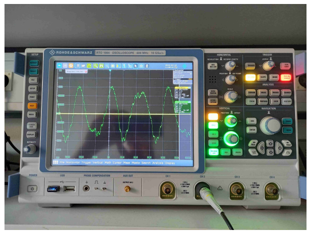
(a) Half bridge



(b) DC power supply

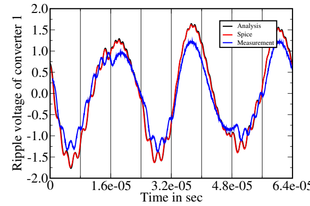


(c) A/D and D/A converter

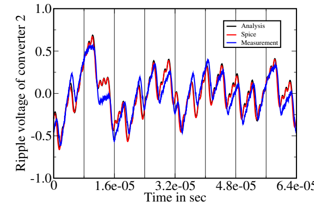


(d) Sampling oscilloscope

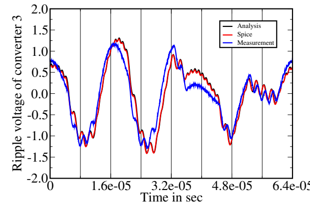
Fig. 7. Hardware components used in the experimental validation.



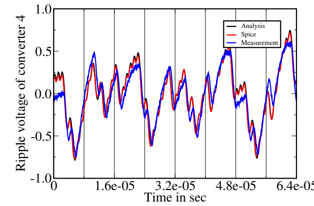
(a) Node 1



(b) Node 2



(c) Node 3



(d) Node 4

Fig. 8. Ripple voltage (measured in Volts) for the case when only one power converter is connected to the bus. The analytical results (black) and Spice simulations (red) are hardly distinguishable.

is based on a 10 μH ± 10 % muRata 1400 inductor (13 A Idc, max SRF 20.7 MHz, 7 mΩ Rdc) and a 1 μF ± 10 % WIMA plastic film capacitor (MKS2, 63 V). As an Ohmic load, a 10 Ω ± 5 % Arcol HS50 resistor (50 W) was used. The buck converters were driven by a Voltcraft VLP-2403 2-channel regulated DC power supply (Fig. 7 (b)). The DC input voltage of the buck converter was selected to be 24 V and the DC output voltage (i.e. the bus voltage) was 12 V. The four FSK-modulated DC-CDMA chip sequences according to Fig. 4 were generated by an Analog Discovery (Digilent Inc.) digital-to-analog converter (Fig. 7 (c)). Signals were sampled and recorded by an R&S RTO 1004 oscilloscope (max 600 MHz, 10 GSa/s) shown in Fig. 7 (d), together with a differential probe (Testec TT-Si 9110, 100 MHz, 1:100). DC voltages were measured by a Fluke 175 true RMS multimeter.

In Fig. 8, the ripple voltages are plotted for the case when only one power converter is connected to the bus. Like in the previous section, the modulated signal is transmitted periodically and only the steady state is observed. The measured signals fit very well with analytical results as well as with Spice simulations. Notice that the ripple voltage is fairly large, because for a single power converter the capacitance is C, whereas for M identically constructed converters connected to the same bus the effective capacitance if $M\,C$. This effect has an impact on the cutoff frequency of the low-pass filter and hence on the ripple. However, it is easy to change the parameters.

In Fig. 9, the buck converters 1 and 4 are connected to the bus. All curves match quite well.

Finally, in Fig. 10 all four buck converters are connected to the bus. We observe that (i) the hook-up is possible if all DC voltages are the same and that (ii) the ripple voltage is not noticeable larger than for a single power converter.

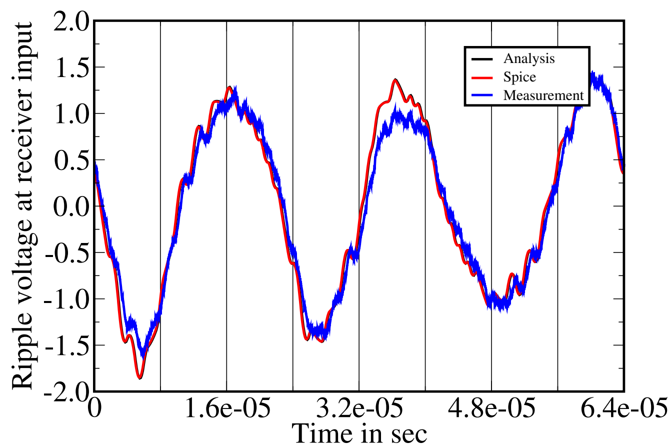


Fig. 9. Ripple voltage (measured in Volts) for the case when power converters 1 and 4 are connected to the bus. The analytical results (black) and Spice simulations (red) are hardly distinguishable. The measurement results agree very well with the analysis and the Spice simulation.

VI. Conclusion

The core idea of the *talkative power* concept is to replace the conventional switching signal of a power electronic converter by an information-carrying switching signal. The original switching signal is modified, e.g. in the form of data-dependent pulse widths, pulse positions, phase shifts or frequency shifts, in order to enable simultaneous energy as well as data transfer. The data sequence is embedded in the output voltage ripple.

In this paper, a DC microgrid is considered which may consist of multiple power generation units, energy storage units, and receiving units. All nodes are connected to the same bus. In the system setup under investigation, power flow and data flow are optionally bidirectional. Bidirectional power flow is, for instance, important for battery charging/discharging. The power is distributed between all nodes connected to the common DC bus. Also, the information is shared among all

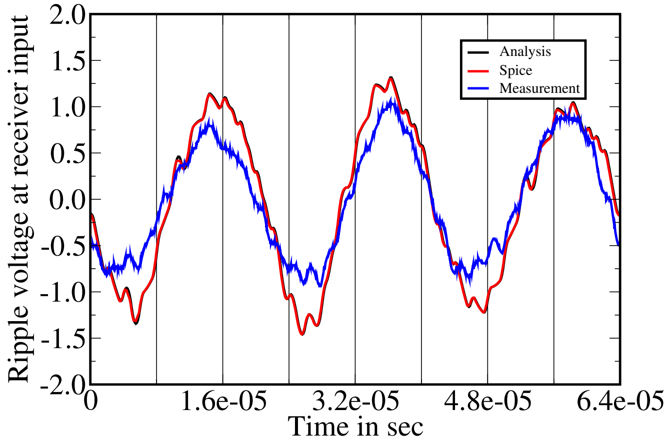


Fig. 10. Ripple voltage (measured in Volts) for the case when all four power converters are connected to the bus. Again, the analytical results (black) and Spice simulations (red) are hardly distinguishable. The measurement error is larger than for two power converters.

power converters and perhaps additional receivers connected to the common DC bus. Information exchange is important for control purposes, but can also include battery state-of-charge and other sensor data, the amount of energy generated by renewable energy sources, or electricity consumption in the context of a smart metering system, just to mention a few examples.

Simultaneous PLC and energy transfer is proposed to be based on the *talkative power* concept. Data bits are sent from multiple nodes simultaneously and optionally in opposite directions. We focus on synchronized nodes and suggest orthogonal spread-spectrum codes with an adjustable spreading factor for this case. In conjunction with 2-ary FSK, a bit error rate degradation caused by multiuser interference is avoided. The data rate is adjustable over a wide range and can be selected differently for each node. If the data rate is chosen to be the same for each node, the maximum achievable sum data rate (in bps) is half of the switching frequency (in Hz), in our case 500 kbps at a switching frequency of 1 MHz. Simulation results are validated by experimental results for two and four simultaneously active nodes.

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