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Active Neutral Point-Clamped Five-Level Inverter With Single-Stage Dynamic Voltage Boosting Capability

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***Abstract*—The circuit performance of conventional active neutral point-clamped (ANPC) inverter is widely accepted in many renewable energy-based applications like photovoltaic (PV) or electric vehicle grid-connected systems. This is mainly because of its excellent characteristics in terms of voltage/current stress profile of the switches, bidirectional power flow capability, and efficient operation. Nonetheless, due to its half-dc link voltage utilization in the output voltage, another power processing stage with additional active and passive elements is required to make its output voltage compatible with the grid when low and wide varying input dc source is available. In this paper, a novel ANPC-based five-level (ANPC5L) inverter with a single-stage boost-integrated circuit design is presented. The proposed topology is able to make the peak output voltage of the conventional ANPC5L inverter followed by a front-end bidirectional boost converter double using the same number of power switches but with less total standing voltage across semiconductors. The working principles of the proposed topology is discussed. Experimental results obtained from 1.3 kW laboratory-built prototype under the grid-connected condition are also given to support the discussion.**

***Index Terms*—active-neutral point-clamped inverter, Grid-connected systems, Multilevel inverters, single-stage boost-integrated design**

I. Introduction

HIGHLY efficient dc-to-ac power electronics converters have grabbed ever-increasing attentions during the latest decade in many newly-developed applications like grid-connected photovoltaic (PV) systems, motor drives and electric vehicles (EV). [1]–[3]. Multilevel inverters (MLIs) with additional front-end dc-dc boost converter are a popular choice in this context to convert the power from low available dc voltage sources like PV string arrays to the ac/grid side. This is mainly because of better output power quality of the resultant system, reduced electro-magnetic interference (EMI) noises, and reduced voltage stress across the switches.

In such two-stage power conversion systems, utilization of the front-end dc-dc boost or buck-boost converter is imperative since it can facilitate the maximum power point tracking operation even with a wide variation in the available dc link voltage of the PV string modules [2]. Conventional mid-point-clamped-based MLIs with active neutral point-clamped (ANPC), T-Type and/or flying capacitor (FC) concepts [3] are able to offer a relatively constant common-mode voltage (CMV) with a reduced leakage current propagation issue [4], which are of interest for grid-tied PV systems. However, ANPC/T-Type-based MLIs suffers from full dc-link voltage utilization, which impose their front-end dc-dc boost converter to work in higher range of dc duty cycle to meet the amplitude of the grid voltage [4]. This can significantly deteriorate the overall conversion efficiency of the entire two-stage system since dc-dc boost converters hardly can possess high efficiency in higher rate of voltage conversion gain.

The aim of this paper is to present a novel single-stage ANPC-based 5L inverter with an integrated switched-boost (SB) concept. The proposed topology requires two boost inductors, four dc-link capacitors, and 10 power switches, and is named as dual-boost (DB)-ANPC-5L inverter in the rest of the article. Owing to the utilization of the inductors with a SB technique, the overall voltage conversion gain of the proposed converter is flexible and two times larger than a standard two-stage system including a dc-dc bidirectional boost converter followed by a back-end ANPC-5L inverter. Moreover, with the same number of required power switches compared to the above-mentioned two-stage converter, the overall total standing voltage (TSV) index of the proposed DB-

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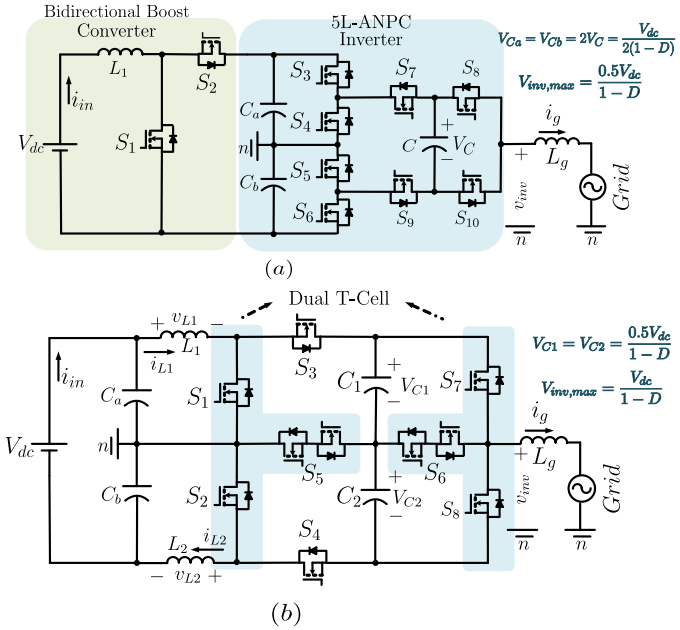


Fig. 1: Grid-connected system based on (a) conventional two-stage platform with front-end dc-dc boost converter and a back-end ANPC-5L inverter (Fig. 1 in [4]), and (b) the proposed single-stage DB-ANPC-5L inverter.

ANPC-5L inverter is lower. Further, a bidirectional power flow performance can also be possible making its application more broaden even for EV systems with vehicle-to-grid (V2G) and grid-to-vehicle (G2V) operations. Continuous input current waveform, reduced size of required passive elements and three-phase circuit extension capability with a reduced switch-count design are other important features of the proposed DB-ANPC-5L inverter. The working principle of the proposed topology is discussed in Section II followed by a comparative study and several experimental results taken from a 1.3kW laboratory-built grid-connected prototype in Section III and IV.

II. Proposed DB-ANPC-5L Inverter

As opposed to two-stage conventional ANPC followed by a front-end boost converter shown in Fig. 1(a), the proposed DB-ANPC-5L inverter requires a single-stage circuit design as shown in Fig. 1(b). Herein, the same number of power switches has been employed with a two standard T-Type switching modules and two discrete power switches. Two boost inductors, L_1 and L_2 in the upper and lower sides of the dc-link capacitors are also used. Herein, both the switches S_1 and S_2 are operating within a flexible dc duty cycle of D, which can be adjusted based on the availability of the input dc voltage and the peak of the grid voltage. Hence, both switches S_1 and S_2 require the same gate switching pulses. Concerning V_{C1} and V_{C_2} as the boosted voltages across C_1 and C_2, respectively, five distinctive output voltage levels e.g., zero, V_{C1}, $-V_{C2}$, $V_{C1}+V_{C2}$, and $-V_{C1}-V_{C2}$ are generated at the output of the proposed inverter.

Different current flowing paths of the proposed DB-ANPC-5L inverter per each output voltage level are depicted in Fig. 2(a)-(h). Herein, the charging paths of the inductors and capacitors are shown with a blue color, while the grid current flowing path is highlighted in a red color. As can be seen, except the top positive [see Fig. 2(g)] and the top negative [see Fig. 2(h)] output voltage levels, the remaining output voltage levels are generated based on two operating sub-modes per switching time interval. Both the inductors are charged to the voltage across the dc-link capacitors of C_a or C_b through two independent power loops of C_a, L_1, S_1 and C_b, L_2, S_2 in one of these sub-modes. Consequently, in the other operating sub-mode, the capacitors C_1 and C_2 are being charged to the voltage across L_1, and L_2 and the voltage across C_a and C_b through two others independent power loops e.g., C_a, L_1, S_3, S_5, C_1, and C_b, L_2, S_4, S_5, C_2. As is clear from Fig. 2(a) to (f), during the output voltage generation in zero and the first positive/negative levels, these power loops act as two integrated boost circuits (dual boost circuits). To succeed the desired zero and the first positive/negative output voltage levels, the four-quadrant switch S_5 is always ON, while the pair switches of S_1/S_2, and S_3/S_4 are switching within a complementary dc duty cycle of D. Therefore, considering these sub-modes switching operation as dual boost circuits over each switching frequency, the following relationship for the involved capacitors voltages can be expressed as $V_{C_1} = V_{C_2} = \frac{0.5V_{dc}}{1-D}$ and $V_{C_a} = V_{C_b} = 0.5V_{dc}$.

Conversely, taking Fig. 2(g) and (h) into account, the charging operation of the capacitors C_1 and C_2 is not possible during the top positive/negative output voltage levels generation. This is because of the fact that the switches S_1 and S_2 must be always ON to provide the grid current flowing path. From Fig. 2(g) and (h), it can be taken that both switches S_3, and S_4 require an ac duty cycle during these time intervals of the operation. In this case, in order to maintain the charging operation of the boost inductors, both switches S_1, and S_2 still are being switched under the dc duty cycle D. It is also worth mentioning that similar to any T-Type network, the role of switches S_6, S_7, and S_8 is for polarity inverting purpose. Hence, all these switches are driven based on the line switching frequency.Considering the value of the inverter output voltage in the top positive/negative levels, which are made by the summation of the voltages across C_1, and C_2, the maximum voltage of the proposed DB-ANPC-5L inverter is equal to $\frac{V_{dc}}{1-D}$. One can be seen is that this value is two times

TABLE I: Voltage stress across the switches for the proposed single-stage DB-ANPC-5L inverter and its two-stage counterpart

Switches	Proposed Topology	Conventional Topology (Fig. 1 in [4])
S_1, S_2	$\frac{0.5V_{dc}}{1-D}$	$\frac{V_{dc}}{1-D}$
S_3, S_4	$\frac{V_{dc}}{1-D}$	$\frac{0.5V_{dc}}{1-D}$
S_5, S_6	$\frac{\pm 0.5V_{dc}}{1-D}$	$\frac{0.5V_{dc}}{1-D}$
S_7, S_8	$\frac{V_{dc}}{1-D}$	$\frac{0.25V_{dc}}{1-D}$
S_9, S_{10}	NA	$\frac{0.25V_{dc}}{1-D}$

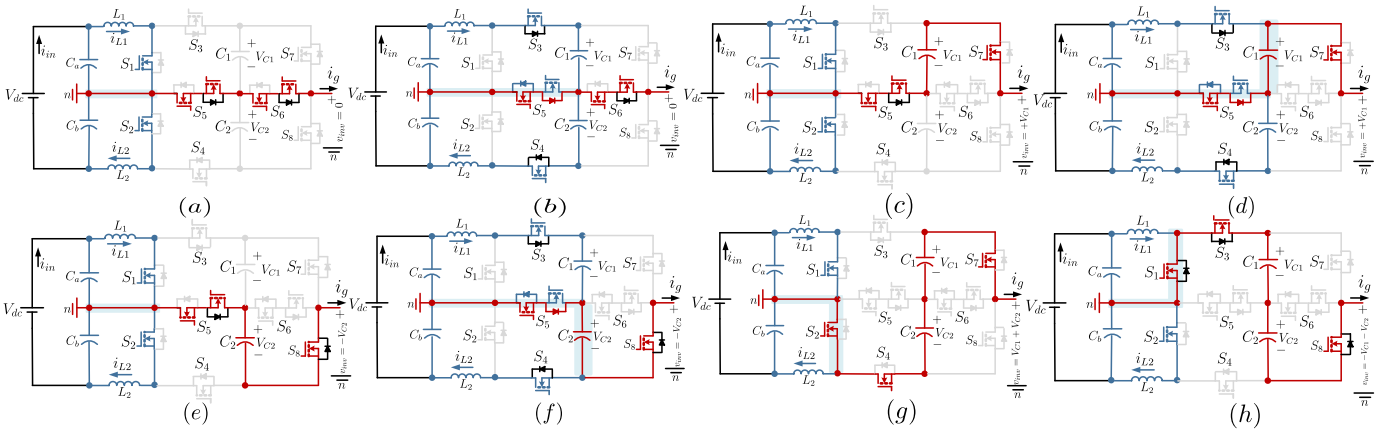


Fig. 2: Different current flowing paths of the proposed DB-ANPC-5L inverter.

TABLE II: ON switching states of the proposed DB-ANPC-5L inverter modulated with a PS-PWM technique.

$d(t)$ Sign	PS-PWM Condition	ON State Switches	v_{inv}
P	$\|d(t)\| \geq A_a, A_b$, D$\geq A_b$	S_1, S_2, S_4, S_7	$V_{C1}+V_{C2}$
	$A_a \leq \|d(t)\| < A_b, D \geq A_b$	S_1, S_2, S_5, S_7	V_{C1}
	$A_b \leq \|d(t)\| < A_a, D \geq A_b$	S_1, S_2, S_5, S_7	V_{C1}
	$A_a \leq \|d(t)\| < A_b, D < A_b$	S_3, S_4, S_5, S_7	V_{C1}
	$A_b \leq \|d(t)\| < A_a, D < A_b$	S_3, S_4, S_5, S_7	V_{C1}
N	$\|d(t)\| \geq A_a, A_b$, D$\geq A_b$	S_1, S_2, S_3, S_8	$-(V_{C1}+V_{C2})$
	$A_a \leq \|d(t)\| < A_b, D \geq A_b$	S_1, S_2, S_5, S_8	$-V_{C2}$
	$A_b \leq \|d(t)\| < A_a, D \geq A_b$	S_1, S_2, S_5, S_8	$-V_{C2}$
	$A_a \leq \|d(t)\| < A_b, D < A_b$	S_3, S_4, S_5, S_8	$-V_{C2}$
	$A_b \leq \|d(t)\| < A_a, D < A_b$	S_3, S_4, S_5, S_8	$-V_{C2}$
-	$\|d(t)\| \leq A_a, A_b D \geq A_b$	S_1, S_2, S_5, S_6	0
	$\|d(t)\| \leq A_a, A_b D < A_b$	S_3, S_4, S_5, S_6	0

larger than its counterpart for the two-stage topology shown in Fig. 1(a). The voltage stress across different switches of the proposed single-stage DB-ANPC-5L inverter and its two-stage counterpart [Fig. 1.(a)] have been tabulated in Table I.

The proposed topology can be driven based on either the phase-shifted (PS)-or level-shifted (LS)-PWM principles. Owing to better output harmonic profile of the PS-PWM, which can reflect two times of effective switching frequency in the output, this type of modulator is selected to generate the required gate switching pulses. Details of this PS-PWM technique are described in Table II, while the ultimate gate switching pulses of the proposed DB-ANPC-5L inverter is illustrated in Fig. 4. The terms of P and N in Table II devote the positive and negative half cycle of this controlled ac reference, respectively. Herein, A_a, and A_b are two 180 degrees PS carriers. The required dc duty cycle of the SB-cell switches is made by comparing the dc reference, D, and the high frequency carrier A_b. As it can be realized from Fig. 3, switches S_3, and S_4 require a dc duty cycle during the zero and the first positive/negative output voltage levels, which is in complementary fashion in respect to S_1, and S_2. Also, they require both this dc and ac duty cycles during the top positive/negative output voltage levels. It can also

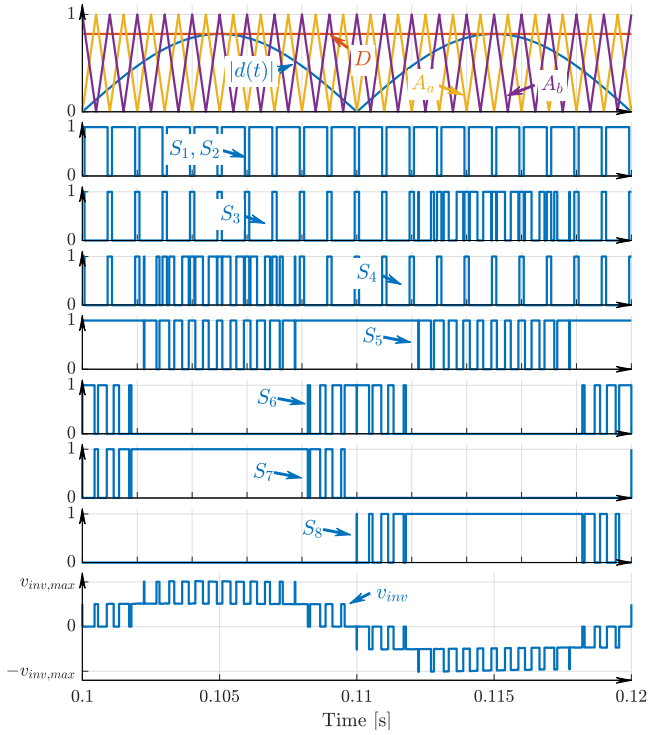


Fig. 3: Modulation and gate pulses of the proposed DB-ANPC-5L inverter.

be discerned that at each level of the output voltage, only half number of the involved switches are ON. This confirms an acceptable overall conduction losses of the proposed DB-ANPC-5L inverter.

III. Comparative Study

To further assess the main features of the proposed DB-ANPC-5L inveter over the other 5L-SB-based inverters with voltage boosting feature, a brief comparative study is presented in this section. The comparative items are the number of required components i.e., switches (S), diodes (D), capacitors

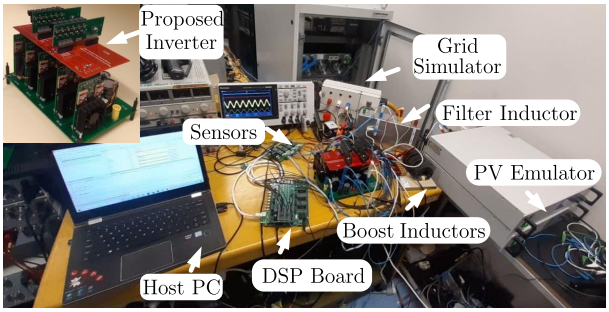


Fig. 4: Proposed DB-ANPC-5L inverter prototype with the measurement setup.

(C), and the inductors (L), the type of output voltage gain, the maximum voltage stress (MVS) across the switches and the TSV index in perunit scale, the nature of input current waveform, bidirectional and self voltage balancing of the capacitors, leakage current value, possibility of applying PS-PWM for the modulation, and the reported maximum efficiency at the rated power. In this case, the leakage current profile of topologies is assumed "Low" if a mid-point-clamped technique is to be used, while it is considered to be "Zero" as long as the circuit configuration is based on common-ground (CG)-based. In other cases rather than the above-mentioned circuit designs, the leakage current is expected to be "High".

As can be found from Table III, the type of output voltage gain of the selected topologies are either static (fixed), or dynamic (flexible). As earlier discussed, in case of having a static voltage conversion gain, the peak of the inverter output voltage cannot be controlled over a wide variation of the input dc voltage unless adopting another front-end dc-dc boost/buck-boost converter, which causes a lower overall efficiency. This can affect the input current nature, as well i.e., being continuous, discontinuous, or semi-continuous depending on the type of the input boost circuit. Among the topologies with a dynamic voltage conversion gain, only the proposed structure is based on the mid-point-clamped technique with a mitigated leakage current propagation issue. Even though the proposed topology needs 10 power switches, its TSV index in perunit scale is only five. Moreover, similar to the most of the reported topologies in Table III, the involved capacitors of the proposed DB-ANPC-5L inverter are self-balanced. This is as opposed to other topologies since their involved capacitors voltages are balanced at the lower rated voltage. This can significantly diminished their losses as well as their dimension area for the fabrication purpose. Having the ability of applying PS-PWM technique is also a notable merit of the proposed topology since it can increase the output frequency of the inverter leading to higher overall power density.

IV. Experimental Results

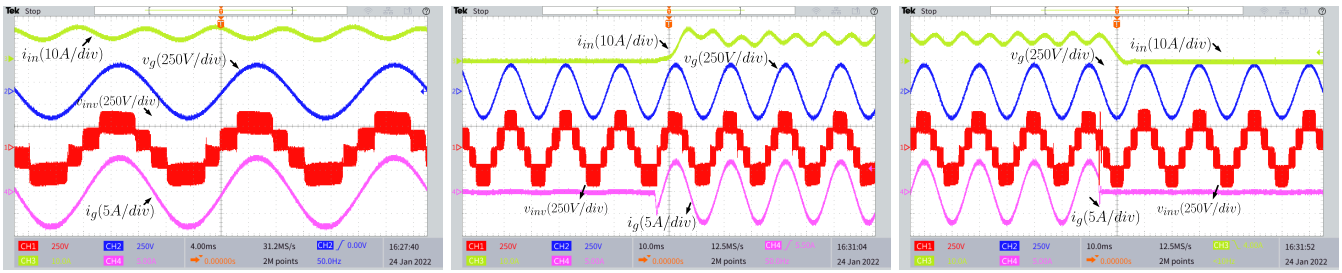
To confirm the feasibility and correctness of the proposed DB-ANPC-5L inverter under the transfomerless grid-connected condition, several laboratory-based experimental results are presented in this section. The laboratory-built prototype with the measurement setup is shown in Fig. 4, while the main parameters used in the experimental tests are summarized in Table IV. The passive elements are selected based on the design guidelines principles discussed in Section IV, while an Elektro-Automatik PV emulator (model EA-PSI-9750-12) is used as an adjustable dc laboratory power supply to electrically feed the proposed inverter. An 50-Hz electrical utility grid is emulated in Regatron TC30.528.43 ACS to interface and test the proposed converter with the grid. Here, the grid peak voltage is adjusted to be 320 V throughout the experiments. To connect the proposed inverter to the grid, an L-type filter with values of $L_g = 5.8$mH and $r_g = 0.33\blacksquare$ is utilized. As for the closed-loop control implementation, a proportional-resonant (PR) controller synchronized with a grid voltage observer technique is used to govern the converter. The modulator used in the experiment is based on the described PS-PWM technique, which has been implemented in a DSP to provide the required gate switching pulses of the proposed DB-ANPC-5L inverter.

Regarding the above-mentioned circuit specifications, and taking the flexible voltage boosting property of the proposed inverter into account, a fixed input dc voltage of 100 V is considered throughout the experiment. Thus, to meet the grid voltage peak amplitude, the dc duty cycle, D, is set at 75% . Fig. 5(a) indicates the input current, i_{in}, the grid voltage, v_g, the 5L inverter output voltage, v_{inv} and the injected grid current, i_g, from top to bottom, respectively, while the peak of the reference current is set at 8 A, which results in 1.3 kW injected power to the grid. As can be confirmed, the input current is continuous with 100-Hz double-line frequency without propagating any large pulsating inrush spikes, while all the 5L output voltage waveform of the inverter with the peak voltage of 400 V and a quality injected grid current are generated. To show the appropriate performance of the controller from the dynamic response view point, the reference active power is changed from zero to 1 kW and vice versa. The respective experimental results of these dynamic tests have been shown in Fig. 5(b), and (c), respectively.

Conversely, the reactive power handling capability of the proposed DB-ANPC-5L inverter is verified through Fig. 6(a) and (b), whilst the value of $P^\star$ is set at 800 W and the amount of $Q^\star$ is chosen at -800 VAR and +800 VAR for the lagging and leading power factor condition, respectively. In both these cases, the proposed inverter is fed through 100 V input dc voltage, and it shows a correct grid-connected performance under the reactive power support mode. Alternatively, Fig. 6(c) attests the bidirectional power flow operation of the proposed DB-ANPC-5L inverter, whereas a resistive load is parallelized with the PV emulator to absorb the reverse power imposed from the grid to the dc side. In this case, the value of $P^\star$ is dynamically changed from -500 W to + 500 W, while there is no distortion in the 5L inverter output voltage. Regarding these conducted experimental results, the peak measured efficiency of the proposed DB-ANPC-5L inverter was at 880 W with the value of 97.5%, while the overall efficiency at the rated power of 1.3 kW was around 96.8%.

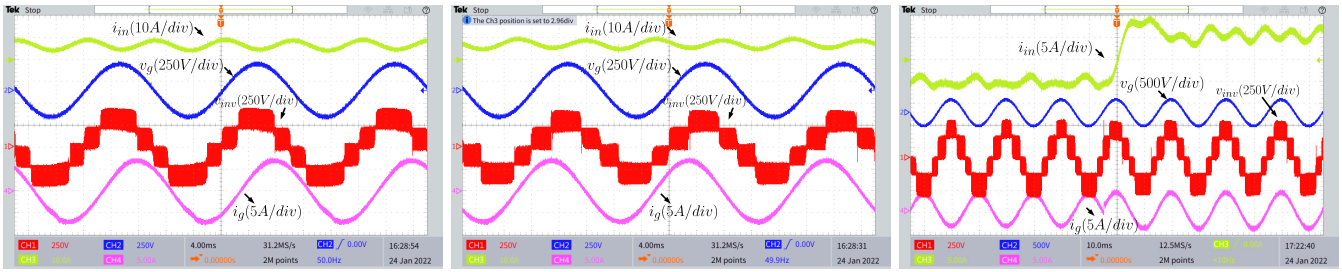
TABLE III: A comparison between the proposed DB-ANPC-5L inverter and the other single-source 5L-SB-based inverters.

Type of Converter	No. of Components				Type of Voltage Gain	MVS (pu) /TSV (pu)	Nature of Input Current	Bidirectional/ Caps Self Balancing	Leakage Current /PS-PWM?	Reported Efficiency
	S	D	C	L						
CG-Based [4]	7	0	2	1	Dynamic	1/6	Continuous	Yes/No	Zero/No	94.9%@1kW
ANPC-Based [5]	12	0	4	2	Static	1.5/11	Continuous	Yes/Yes	Low/No	97.5%@160W
Cascaded-Based [6]	10	0	2	2	Dynamic	0.5/5	Continuous	Yes/Yes	High/Yes	97.3%@1kW
CG-Based [7]	9	0	2	1	Dynamic	1/6.5	Continuous	Yes/Yes	Zero/No	97.3%@1.5kW
Proposed DB-ANPC	10	0	4	2	Dynamic	1/5	Continuous	Yes/Yes	Low/Yes	97.5%@880W



(a) (b) (c)

Fig. 5: Experimental results showing from up to bottom: the input current, the grid voltage, the inverter output voltage, and the injected grid current, (a) at 1.3 kW injected power, (b) under a dynamic test from zero to 1 kW power injection, (c) under a dynamic test from 1 kW to zero power injection.



(a) (b) (c)

Fig. 6: Experimental results showing (a) lagging power factor ($P^\star$= 800 W, $Q^\star$= -800 VAR) (b) leading power factor ($P^\star$= 800 W, $Q^\star$= 800 VAR) (c) bidirectional operation ($P^\star$= -500 W to $P^\star$= +500 W).

TABLE IV: Main parameters used for the experimental prototype

Element	Type and Description
Power Switches	UJ4C075018K4S
Microprocessor	DSP-TMS320F28379D
Switching Frequency	20 kHz
C_1, C_2 and L_1, L_2	$0.47 \times (2)$mF & 0.3 mH
Gate Drivers	UCC21520DW
Isolated dc/dc Converters	MGJ1D051505MPC
Current Sensor	AMC 1200
Voltage Sensor	ISO224B

V. Conclusion

A novel single-stage boost integrated ANBC5L inverter is presented in this paper. Main features of the proposed topology are large dynamic voltage conversion gain, reduced voltage stress across the switches, continuous and spike-free input current and bidirectional operation. Detailed working principle of the proposed converter with a comparative study were discussed. The effectiveness and feasibility of the proposed topology have also been verified through presenting several experimental results from a 1.3 kW grid-connected laboratory-built prototype.

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