Digital Object Identifier 10.1109/IECON49645.2022.9968956

IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society

# dv/dt filter design incorporating machine impedance and voltage slew rate for WBG-based electric drives

Karthik Debbadi

Yoann Pascal

Marco Liserre

## Suggested Citation

K. Debbadi, Y. Pascal and M. Liserre, "dv/dt filter design incorporating machine impedance and voltage slew rate for WBG-based electric drives," IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 2022, pp. 1-6, doi: 10.1109/IECON49645.2022.9968956.

# dv/dt filter design incorporating machine impedance and voltage slew rate for WBG-based electric drives

Karthik Debbadi
*Chair of Power Electronics*
*Kiel University*
Kiel, Germany
kde@tf.uni-kiel.de

Yoann Pascal
*Fraunhofer Institute*
*for Silicon Technology ISIT*
Itzehoe, Germany
yoann.pascal@isit.fraunhofer.de

Marco Liserre
*Chair of Power Electronics*
*Kiel University*
Kiel, Germany
ml@tf.uni-kiel.de

***Abstract*—The trend towards high power density and high reliability of electric drive systems in mobility applications pushes the use of high-speed machine in combination with Wide Band Gap (WBG) power semiconductor technology. Replacement of Si power technology with WBG without mitigating high voltage slew rates $dv/dt$ degrades machine winding insulation. Of the different mitigation techniques employed, especially the passive LCR filter at the output of the inverter cannot be optimally designed without consideration of the inherent low impedance of the high speed machines. This paper presents the analytical techniques used for LCR filter design for motor drives and introduces the technique to incorporate machine impedance $Z_{dm}$ for optimal design of the parameters to achieve high efficiency. An analytical technique based optimization algorithm is introduced for the reduction of filter inductor volume to achieve high power density in these applications. The proposed design methodology is evaluated in simulations and experiments with Gallium Nitride (GaN) based inverter technology.**

***Index Terms*—$dv/dt$ filter, voltage slewrate, Wide Band Gap (WBG) Devices, LCR filter, Inductor optimization, fast analytical techniques, high speed machine drives**

## I. Introduction

Wide band gap-based (WBG) active devices, such as SiC MOSFETs and GaN HEMTs, play a key part in the energy transition and the electrification of society, thanks to their improved performances compared to their conventional silicon-based counterparts. As a matter of fact, WBG components exhibit lower conduction and switching losses, and switching speeds increased by at least a tenfold. This leads to efficiency increase, as well as power density improvements, enabled in particular by the reduction in volume of filters and cooling systems [1].

The WBG devices have many advantages in motor drive applications especially with high-speed machine technology which is gaining interest in mobility applications [2]. However, studies have shown the strong dependency of winding insulation lifetime with voltage slew rate ($dv/dt$) [3]–[5] for insulation in the stator windings of electric machines. Resonances and reflection furthermore lead to voltage overshoots stressing the cables and the windings. Direct replacement of silicon IGBTs by WBG transistors in electric drives would then result in a significant reduction of the machine winding lifetime [5].

Full wave filters deliver high power quality, which minimize iron loss in the machine, but they are bulky and themselves lossy. On the other hand, $dv/dt$ filter have cut-off frequencies significantly greater than the switching frequency and use machine inductance to filter the current. Depending upon their design, they can furthermore notably increase the drive's power loss. Many studies have tackled this issue, of which a review was done in [6]–[8]. The mitigation concepts can be classified in active, passive and hybrid [6]. The active concepts utilize the advanced gate driving techniques either in open/closed loop for switching of the power device [9] thereby avoid generating spectral components stressful for machine windings. Although this method is favorable in terms of EMI, it intrinsically induces increased switching loss. The hybrid concepts utilize modified modulation patterns along with undamped LC-filter to achieve a resonant transition without overshoot. The passive concepts can be classified as LCR-filter and LC with DRC-filter at the output of the inverter as a mitigation method.

This paper proposes a $dv/dt$ filter design technique to minimize the filter's loss and volume, by taking into account the machine impedance and the inverter switching speed. The approach is most beneficial in the case of a high-speed machine, with low impedance. The focus is on LCR filter connected between the phase output and the midpoint $N$ of the inverter as shown in Fig. 1 for effective reduction of both differential mode (DM) and common mode (CM) $dv/dt$ at the motor terminals [10].

In Section II, the values of the components of the $dv/dt$ filter are calculated using the proposed approach taking into account the machine impedance in DM mode as $Z_{dm}$, as well as using the conventional approach assuming $Z_{dm} = \infty$. In section III, an optimization routine is implemented. Section IV describes results validating the approach. Last, Section V concludes the paper.

## II. Design Approach

The machine is characterized by DM and CM impedance [11]. This paper assumes that the machine impedances are balanced. This allows to neglect mode transfer and to reduce the 3-phase circuit to its equivalent model. Under DM configuration, the phase A is connected to the positive DC

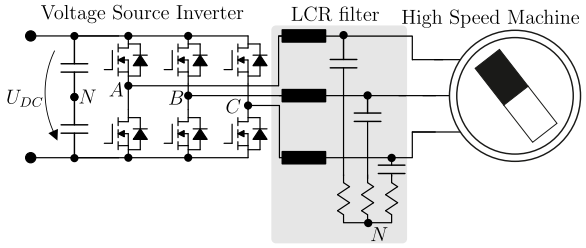



Fig. 1: Motor drive architecture

rail and the phase B, C are connected to negative DC rail and this leads to the filter configuration as shown in Fig. 2b during the 3-phase switching action in the inverter with an overall differential voltage of $U_{DC}$ applied across the DM circuit. With filter inductor ($L_o$), capacitor ($C_o$) and resistor ($R_o$), the filter impedance can be split into $Z_1 = j\omega L_o$ (filter inductor impedance), $Z_2 = R_o + 1/(j\omega C_o)$ (impedance of filter capacitor and resistor in series) as seen in Fig. 2a. For the 3-ph impedance connections shown in Fig. 2b to the right, the point x and y are equipotential points and can be virtually connected together for simplified circuit analysis as seen to the left. The 3-ph machine impedance is simplified into $Z_{dm} = \frac{3}{2}Z_{ph}$ which leads to a simple circuit to be evaluated for the filter design. This will be the case for any other modes in the 3-ph modulation scheme applied to inverter.

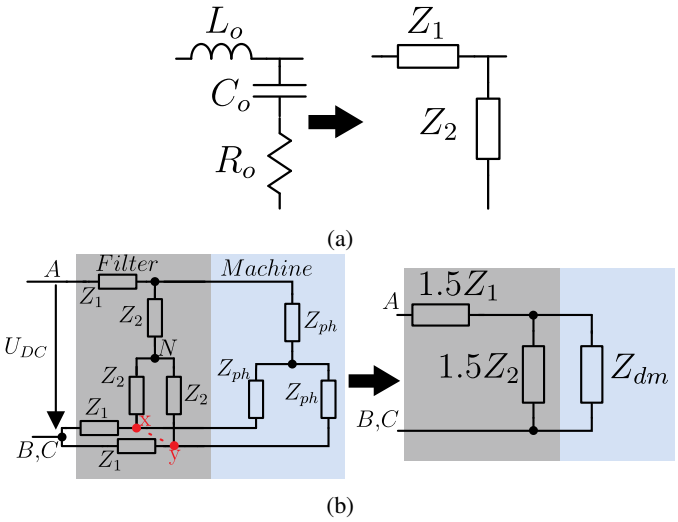



Fig. 2: Simplified equivalent circuit used for filter design. (a) LCR filter impedance. (b) System Impedance in DM configuration with filter and machine

In the following subsections, ($L_o$,$C_o$,$R_o$) are first selected using two conventional design techniques and then following the proposed approach.

### *A. Filter design neglecting the effect of the machine impedance - conventional approach*

*1) Design Space Approach:* $dv/dt$ filter design usually neglects the impact of the machine impedance. For instance, in [12], an analytical methodology for calculation of LCR filter and LC filter with DRC (clamping diodes) is proposed. The same methodology can be extended to a design space based on the changes in the inductor ripple current ($\Delta I_L$) and voltage slew rate $dv/dt$ as in [6]. The design space can be visualized as in Fig. 3a for multiple combinations of $L_o$ and $C_o$ filter values. As the $dv/dt$ required is relaxed from 2 V/ns to 6 V/ns, the filter size decreases for a given $\Delta I_L$. It can be inferred that as and when the future insulation materials can support higher $dv/dt$, the passive filter can be reduced in size for a given specification. Similarly, if for the design the $\Delta I_L$ is relaxed to be higher, in turn filter inductor size can be reduced.

Thereby, the standard design approach for a passive LCR filter for the $dv/dt$ reduction is based on the $2^{nd}$ order filter design formulae (1).

$$\omega_o = \frac{1}{\sqrt{L_o C_o}} \qquad Q = \frac{1}{R_o} \cdot \sqrt{\frac{L_o}{C_o}} \tag{1}$$

where $\omega_o$,$Q$ are the self-resonant angular frequency and the quality factor of the filter.

The cut-off frequency $f_o = \omega_o/(2\pi)$ can be chosen a decade higher than the switching frequency $f_{sw}$ of the inverter while maintaining a $Q = 0.5$ will still respect the National Electrical Manufacturers Association (NEMA) standard; typically NEMA standard is used for various industrial electrical equipment grade; for $U_{dc} \leq 600$V and still keep the resonance damped for the filter [13]. The rise time $t_r$ at the filter output and the here-defined effective impedance $Z_{eff}$ can be computed given the $U_{dc}$ and desired inductor current ripple $\Delta I_L$ and the voltage slewrate $dV/dt$ with (2).

$$t_r = \frac{0.8U_{dc}}{\frac{dV}{dt}} \qquad Z_{eff} = \frac{U_{dc}}{\Delta I_L} \tag{2}$$

The filter characteristic parameters can then be calculated using the scaling constants $\Omega = 1.05$ and $\gamma = 0.71$ (values for $Q = 0.5$), as suggested in [6]:

$$\omega_o = \Omega \cdot \frac{1}{t_r} \qquad Z_o = \gamma \cdot Z_{eff} \tag{3}$$

With the computed $\omega_o$ and $Z_o$, the filter parameters $L_o$, $C_o$ and $R_o$ can be evaluated with (4).

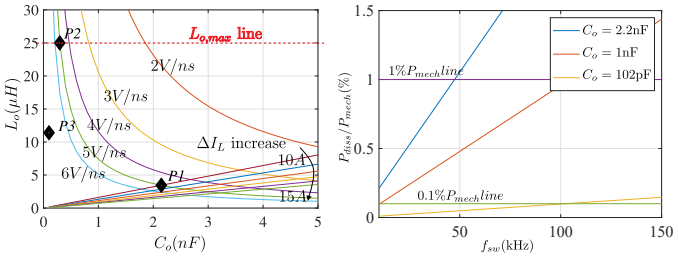
$$C_o = \frac{1}{Z_o \cdot \omega_o} \qquad L_o = \frac{Z_o}{\omega_o} \qquad R_o = Q \cdot Z_o \tag{4}$$

With this design approach for the specifications given in Tab. I, the filter parameters found are shown for P1 in Tab. III.

The power dissipation in the filter resistance (per phase) can be given by the relationship in (5) [6].

$$P_{diss} = f_{sw} U^2{}_{dc} C_o \tag{5}$$

Fig. 3b shows the power dissipated in the filter, normalized by the processed power, as a function of the $f_{sw}$ and for various $C_o$ values. It shows in particular that for the value




(a) (b)

Fig. 3: (a) Design Space of filter parameters : $L_o$,$C_o$. (b) Normalized power dissipation due to filter capacitor for $U_{dc} = 565$ V for a range of $f_{sw}$

of filter capacitor obtained with this design approach (P1), more than $1\%$ of the output power is lost in the filter for $f_{sw}$ above 50 kHz. This counteracts the benefits of using WBG technology for the power semiconductor as it limits the maximum switching frequency. Reducing the filter capacitor to 1 nF allows to push the $f_{sw}$ to 100 kHz before reaching $1\%$ of output power loss in the filter. If the filter capacitor can be further reduced to 102 pF, the filter losses due to the capacitor can be kept less than $0.1\%$, thereby keeping high efficiency and fully utilizing the benefits of WBG technology.

TABLE I: Specifications

| Parameter | Value | Unit |
|---|---|---|
| $U_{dc}$ | 565 | V |
| $\Delta I_L$ | 10 | A |
| $f_{sw}$ | 100 | kHz |

TABLE II: Machine

| Parameter | Value | Unit |
|---|---|---|
| Nom. Speed | $20k$ | rpm |
| Nom. Torque | 4.8 | Nm |
| Pole pair | 2 | - |

*2) Max Inductance design technique:* Based on the design space, it is possible to increase the filter inductor and reduce the filter capacitor to achieve the same $dv/dt$ output with a lower ripple current [14]. However, there needs to be an optimization on the size of the filter inductor $L_o$ to achieve high power density. From [14] the filter inductor can be no more than $2\%$ of the base impedance ($Z_{base}$) to avoid higher voltage drop which can be significant when the output fundamental frequency of the inverter is high. This leads to the upper limit on the value of filter inductor that can be used for the filter design as per (6).

$$Z_{Lo} = \omega L_o \leq 2\% \times Z_{base} = (2\%) \times \left( \frac{{U_{base}}^2}{S_{base}} \right) \quad (6)$$

where $U_{base}$ and $S_{base}$ are referred as system base voltage and base apparent power respectively. In this case, the base values are assumed to be the nominal operating values found on the machine nameplate. Using this approach for the filter parameters for a given $U_{base} = 230\ \mathrm{V_{rms}}$, $S_{base} \approx 10$ kW (for high speed PMSM, the power factor is close to 1) operating at a nominal frequency $\omega_o = 2\pi f_o = 2\pi \cdot 667$ Hz leads to $L_{o,max} \approx 25\ \mu$H as shown in the Fig. 3a. With the applicability of same equation set as used in II-A1 the point P2 is derived in Tab. III. Still with this approach $C_o = 300$ pF leads to dissipation losses due to filter capacitor are still higher than the $0.1\%$ line in Fig. 3b above about 30 kHz.

TABLE III: LCR filter parameters for different approaches

| Design | $L_o(\mu\mathrm{H})$ | $C_o$(nF) | $R_o(\Omega)$ |
|---|---|---|---|
| Design Space Approach (P1) | 3.5 | 2.1 | 20 |
| Max Inductance Approach (P2) | 25 | 0.21 | 174 |
| $Z_{dm}$ incorporated Approach (P3) | 11.4 | 0.1 | 170 |

### *B. Filter design incorporating Machine Impedance*

Conventional machines have high impedance, which justifies neglecting them during filter design as the error is smaller in the analysis. However, in the case of high speed machines with low impedance, this assumption leads to an under-optimized design. Therefore, a new design methodology in which the filter transfer function along with the machine $Z_{dm}$ are used in frequency domain to evaluate the design space of the LCR filter. With the requirements of the $dv/dt$ and the voltage overshoot, the optimal filter parameters are arrived within desired low losses in the filter. Such approach opens the opportunity to look at the filter design at a system level design rather than an independent design aspect of the motor drive system. This is also justified as for high power density an integrated design approach leads to better designs.

The first step consists in identifying the machine impedance, which can be achieved by measurement of the CM and DM impedance of the machine as treated in [11]. The measurements obtained on the machine under study (detailed specifications are given in Tab. II) can be seen in Fig. 4. Since the filter is designed for high frequency applications, roughly in the frequency band 100 kHz-5 MHz, it is prudent to arrive at the high frequency model of the PMSM in DM for integration into the design workflow. The high frequency model of the PMSM is done based on modelling approach provided in [11].

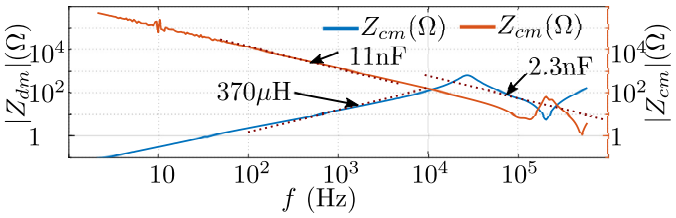
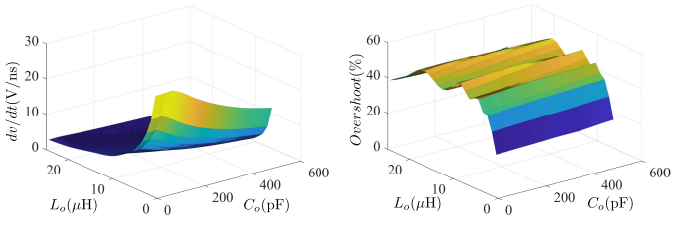



Fig. 4: Impedance measurement of the PMSM with the fitted impedance of some inductance and capacitance.

The filter is then designed as follows: A design set of points ($C_o$, $L_o$) are uniformly sampled in the design space $[0, 600]$ pF $\times$ $[0, 25]$ $\mu$H. $R_o$ is computed for each point using (4). For each of these points, the transfer function of the filter, loaded by the impedance $Z_{DM}$ of the machine, is calculated. Furthermore, the inverter output voltage is modelled as a trapezoidal waveform, the slewrates of which are estimated based on the components' datasheet. The Fast Fourier Transform

(FFT) of this waveform is combined to the filter transfer function, yielding the FFT of output filter voltage. An Inverse Fast Fourier Transform (iFFT) is applied on the voltage across the $Z_{dm}$ of machine. From it are extracted the slewrate ($dv/dt$) (Fig. 5a) and the voltage overshoot (Fig. 5b). It can be seen




(a) (b)

Fig. 5: Design space surface plots. (a) $dv/dt$ for filter design space. (b) Voltage overshoot percentage for design space

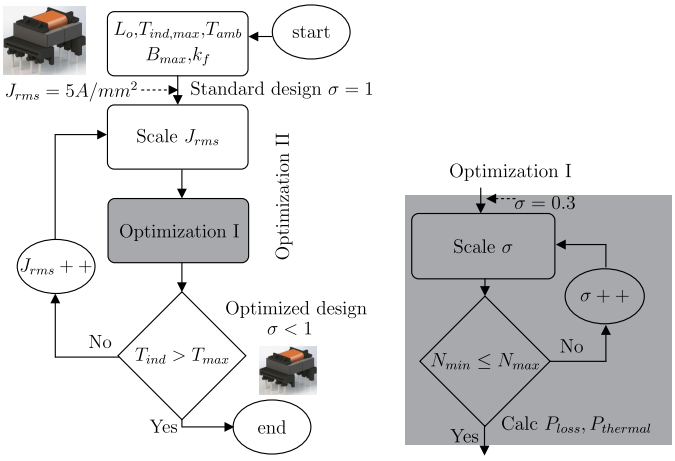
that for most of the design space the overshoot is lower than $50\%$ and for the complete design space lower than $60\%$. This is in agreement with the NEMA norms [13], making slewrate as the criteria for filter parameter evaluation. As discussed in the analytical design, the allowed $dv/dt$ at the output of the filter is limited to $5$ V/ns. Therefore, the slewrate surface is sliced at $5$ V/ns, to arrive at the polynomial fit for the filter parameters $L_o$ and $C_o$ given in (7).

$$\begin{aligned} L_o = (&-5.39 \cdot 10^{-8} \cdot {C_o}^3 + 6.39 \cdot 10^{-5} \cdot {C_o}^2 \\ &- 0.0363 \cdot C_o + 14.48) \\ &(L_o \ in \ \mu H, \ C_o \in [0, 600] \ \ in \ pF) \end{aligned} \tag{7}$$

For instance, for the given filter capacitor of $100$ pF, a filter inductance of $11.4$ $\mu$H is required which can be seen as P3 in Fig. 3a. The power dissipation due to the filter capacitor is less than $0.1\% P_{out}$ and also the filter inductor is smaller ($-54\%$ in inductance) compared to the one obtained analytically without incorporating the machine impedance into the design process of the filter P1.

## III. Loss Analysis and Inductor Optimization

From the section II, the required filter parameters ($L_o$, $C_o$, $R_o$) have been deduced, and this section will focus on the inductor optimization for higher power density and lower power losses, based on an optimal choice of core size (assuming a core homothetic to a standard ETD core, with scaling factor $\sigma$) and current density $J_{rms}$ for optimal number of turns $N$. The approach of using fast analytical methods for optimization is borrowed from [15] and adapted for the optimization as described in Fig. 6. The optimization is composed of two parts. First, the $J_{rms}$ in the winding is set a priori, which enables to calculate the scaling factor $\sigma$ minimizing the core volume whilst meeting the constraints in terms of manufacturability (winding window size) and magnetic saturation. $J_{rms}$ is scaled higher as the second level of optimization to further reduce the volume and improve the utilization of the core. With this approach it is possible to arrive at a reasonable analytical approximation of the volume and temperature rise in inductor without huge database of the materials, geometries for inductor cores and windings allowing for fast analytical method.




(a) (b)

Fig. 6: (a) Inductor optimization algorithm for volume reduction. (b) Optimization I.

### A. Power Losses in Inductors

The main losses in an inductor are the core losses $P_{core}$ and winding losses $P_{wind}$ which can be calculated analytically for a given core material and geometry. The winding losses can be calculated using the equation set in (8) where the skin and proximity losses are accounted based on the strand diameter $d_r$ and skin depth $\delta$ for the operating switching frequency $f_{sw}$ [16].

$$P_{wind} = R_{dc}{I_{dc}}^2 + c_0 R_{dc}{I_{ac}}^2 \qquad R_{dc} = \frac{N l_{avg}}{4 g A_{cond}} \tag{8}$$

where conductor area $A_{cond} = \frac{\pi {d_r}^2 N_s}{4}$ and $c_0 = 1 + \frac{1}{12}\left(\frac{k_f \omega_w d_r}{\delta^2}\right)^2$ for $d_r < 3.17\delta$ and $c_0 = \frac{1}{\delta}\left(\frac{8(k_f \omega_w)^2}{3 d_r}\right)$ for $d_r \geq 3.17\delta$. $R_{dc}$ is the DC resistance of the conductor, $l_{avg}$ is the mean turn length, $g$ is the conductivity of copper, $N, N_s$ are number of turns and number of strands of the winding wire respectively. A litz wire of $100\mu$m is selected for the given $f_{sw}$ in the optimization of the inductor and used for the loss evaluation.

The core losses in the inductor are computed based on the improved Generalized Steinmetz Equation (iGSE) provided by [17]. For a given inductor current ($I_L$) waveform w.r.t time ($t$), the flux density $B$ in the core cross-section is extracted for the given geometry to compute the $P_{core} = V_e \cdot p_v$ using (9) for one fundamental cycle $f_{ac}$, where $V_e$ is the volume of the core.

$$p_v = \frac{k_i \left(\Delta B\right)^{\beta-\alpha}}{T} \sum_m \left|\frac{B_{m+1} - B_m}{t_{m+1} - t_m}\right|^{\alpha} (t_{m+1} - t_m) \tag{9}$$

where $k_i = \frac{k}{2^{\beta}\pi^{\alpha-1}\left(0.2761+\frac{1.7061}{\alpha+1.354}\right)}$

$k$, $\alpha$ and $\beta$ are the conventional Steinmetz parameters, extracted from the datasheet for the operating point. Although, these parameters change as the operating point changes, they are considered as constant in this study. Since the proportion of core losses is minor in the overall losses, the error due to the estimation of these parameters is limited. The core material chosen for this optimization is N87 since it has a good performance factor for the desired frequency of operation.

The allowed thermal losses in an inductor are dependent upon the allowed thermal rise, as well as on the thermal resistance $R_{th}$. For the core under study, $R_{th}$ can be related to the core size using the empirical relation (10) [18].

$$P_{th} = \frac{T_{ind} - T_{amb}}{R_{th}}$$
$$R_{th} = 53\left(V_e\sigma^3\right)^{-0.54} \quad (10)$$

With $R_{th}$ in K/W and core volume $V_e$ in $\mathrm{cm}^3$

### B. Inductor design

The standard design approach of using the area product ($A_p$) method with the inductor parameters as shown in IV leads to optimal turns for which the power loss is 1.5 W with $T_{ind} = 52$ °C ($D_1$ in Tab. V). This leaves a scope for improving the utilization of the inductor to allow for a maximum inductor temperature $T_{ind} = 100$ °C. This is achieved by the optimization approach stated hereafter.

TABLE IV: Input parameters for inductor design

| Parameter | Description | Value | Unit |
|---|---|---|---|
| $L_o$ | Filter Inductance | 11.4 | $\mu$H |
| $T_{ind}$ | Inductor temperature | 100 | °C |
| $T_{amb}$ | Ambient temperature | 25 | °C |
| $B_{max}$ | Maximum flux density | 250 | mT |

The optimization can be split into 2 levels, in first level the current density $J_{rms}$ is set at a constant value of 5 A/mm$^2$ and in the second level this parameter is increasing to reduce the volume but increase the copper loss. The standard design derived above is considered to lead to a maximum core volume, it is assigned to the scaling factor value $\sigma = 1$, as the upper limit for the optimization. The optimization algorithm is based on a complete scan of the universe for scaling factor values $\sigma \in [0.3, 1]$. It runs as follows (see Fig. 6).

1) Initiate system parameters and assign $\sigma = 1$ for standard design using area product method $A_p$.
2) Start from the minimum (arbitrary) $J_{rms}$, $\sigma$-value
3) Calculate the minimum number of turns based on $B_{max}$ and maximum number of turns based on window area $A_w$ using (11).

$$N_{min} = \frac{L_o I_{max}}{B_{max} A_{core}} \qquad N_{max} = \frac{k_{cu} A_w}{a_{litz}} \quad (11)$$

where $I_{max}$ is the peak current, $A_{core}$ is the scaled core cross-sectional area, $k_{cu}$ is the winding filling factor $A_w$ is the window area, and $a_{litz}$ is litz wire area.

4) Check if $N_{min} \leq N_{max}$ to move ahead and compute the total power loss in the inductor for $N_{min}$.
5) In case this condition is not fulfilled, the value of $\sigma$ can be incremented and continue with the optimization.
6) For a satisfactory $\sigma$, calculate inductor temperature $T_{ind}$ using (10). If this temperature is below $T_{max}$, increment the $J_{rms}$ and repeat from step 2 until desired $T_{ind}$ is achieved.

The core losses decrease as the $N$ increases and the winding losses increase with the increase in $N$. The first level of optimization yields to the point $D_2$ in Tab. V, and therefore reduces the volume compared to the standard design $D_1$ around 17%. There is however further margin to reduce size as the inductor is still under utilized: its temperature did not rise much, it remains far below the target. This leads to the next step in the optimization to allow for different current density $J_{rms}$ in the winding to further reduce the volume. With the increase of $J_{rms}$, the $N_{max}$ (maximum possible number of turns in the winding window) is higher for the same core volume, however with an increased $P_{wind}$ in the inductor. The flowchart in Fig. 6, shows that $J_{rms}$ constitute the parameter of a second optimization loop.

This process leads to $D_3$ (Tab. V). The inductor is now operating at the target 100 °C with higher overall losses at around 3.12 W – double the losses from the standard design. On the other hand, the volume is nearly 45% smaller. For the three-phase inverter, the overall filter inductor losses are also less than $0.1\% \cdot P_{out}$. This leads to a high power density and high efficiency design for the filter, without giving up the advantages provided by the use of WBG power devices for the design of the next generation inverters for motor drive applications.

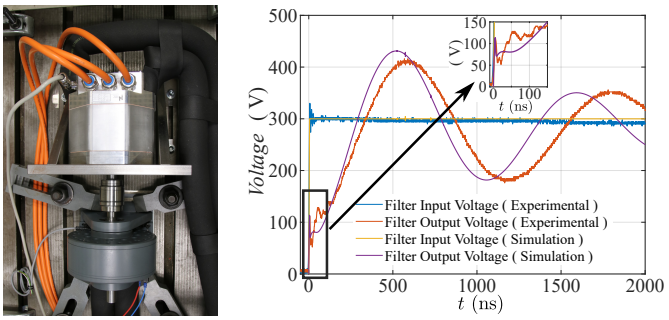
TABLE V: Comparison of standard, optimized level I, optimized level II inductor design w.r.t $V_e$ and $T_{ind}$

| Design | $V_e$ (cm$^3$) | $T_{ind}$ ( °C) | $J_{rms}$ A/mm$^2$ |
|---|---|---|---|
| $D_1$:Standard | 7.63 | 52 | 5 |
| $D_2$:Optimized I | 6.33 | 60 | 5 |
| $D_3$:Optimized II | 4.21 | 100 | 8.6 |

## IV. Simulation and Experimental Results

The lab test bench for experimental validation is shown in Fig. 7a with the PMSM and the load coupled through a shaft, the inverter technology used is based on GaN power devices GS66504B with 650V blocking voltage capability from GaN Systems. The experimental evaluation was performed in single pulse mode in DM configuration as in Fig. 2b with the non-rotating machine. The measurements of the input and output voltages were performed with 200MHz high voltage isolated differential probes (Tektronix TMDP0200) and an 350MHz oscilloscope (Tektronix MDO34). The filter components used are commercial inductor SER2211-123E (Self Resonant Frequency ≈ 18 MHz) and commercial film capacitor (FKP2O100681D00KSSD).

The simulation study was conducted based on the parameter extraction from the measurement of machine $Z_{dm}$ and the filter inductor impedance as outlined in section II-B. Based on the results obtained as seen in Fig. 7b, a good agreement of the simulation and experimental evaluation is found validating the modelling approach and thereby the design approach for the filter components in DM configuration giving by $L_{dm}$, $C_{dm}$ and $R_{dm}$.




(a) (b)

Fig. 7: Test bench and experimental validation of the filter design. (a) High speed PMSM coupled to the Eddy Current Brake (load). (b) Experimental validation: $L_{dm} = 12$ $\mu$H, $C_{dm} = 68$ pF and $R_{dm} = 250$ $\Omega$.

## V. Conclusion

Direct replacement of Si based power semiconductor technology with WBG based technology leads to new challenges for reliability of the machine insulation system due to higher switching frequencies and higher slew rate of the output voltage. Especially with high speed machines as seen in this case are characterized with low impedance lead to either bulky passive filter or less efficiency for the overall inverter with the standard analytical methods without taking into consideration machine impedance. Accounting the machine impedance into the design process reduces the passive LCR filter size by approximately 50% and leads to higher efficiency when the proposed method is used even at higher switching frequencies where full performance of WBG can be exploited. Extra losses due to filter capacitor are reduced with this method but inductor optimization leads to a smaller overall inductor with lower losses. The inductor optimization algorithm leads to a volume reduction of over 45% compared to the standard method. The simulation results agree with the analysis performed respecting the NEMA standards and experimental results provided with the available components.

## Acknowledgment

This work was supported by Interreg Deutschland-Danmark with funds from the European Regional Development Fund via the PE-Region Platform project (ref. 098-1.1-18). Find further information on Interreg Deutschland-Denmark on www.interreg5a.eu

## References

[1] A. Bindra, "Wide-bandgap-based power devices: Reshaping the power electronics landscape," *IEEE Power Electronics Magazine*, vol. 2, no. 1, pp. 42–47, 2015.

[2] A. K. Morya, M. C. Gardner, B. Anvari, L. Liu, A. G. Yepes, J. Doval-Gandoy, and H. A. Toliyat, "Wide bandgap devices in ac electric drives: Opportunities and challenges," *IEEE Transactions on Transportation Electrification*, vol. 5, no. 1, pp. 3–20, 2019.

[3] V. Bolgova, S. Lefebvre, S. Hlioui, N. Boucenna, F. Costa, and A. Leonov, "Development of testing methods for winding turn-to-turn insulation of low voltage motors fed by pwm converters," in *EPE'17 ECCE Europe)*. IEEE, 2017, pp. P–1.

[4] F. Alvarez-Gonzalez, D. Hewitt, A. Griffo, J. Wang, M. Diab, and X. Yuan, "Design of experiments for stator windings insulation degradation under high dv/dt and high switching frequency," in *2020 IEEE Energ. Conv. Congr. and Expo. (ECCE)*. IEEE, 2020, pp. 789–795.

[5] F. Pauli, A. Ruf, and K. Hameyer, "Low voltage winding insulation systems under the influence of high du/dt slew rate inverter voltage," *Archives of EE*, vol. 69, no. 1, 2020.

[6] M. Haider, M. Guacci, D. Bortis, J. W. Kolar, and Y. Ono, "Analysis and evaluation of active/hybrid/passive dv/dt-filter concepts for next generation sic-based variable speed drive inverter systems," in *2020 IEEE EEnerg. Conv. Congr. and Expo. (ECCE)*. IEEE, 2020, pp. 4923–4930.

[7] J. He, G. Y. Sizov, P. Zhang, and N. A. Demerdash, "A review of mitigation methods for overvoltage in long-cable-fed pwm ac drives," in *2011 Energ. Conv. Congr. and Expo.* IEEE, 2011, pp. 2160–2166.

[8] M. Pastura, S. Nuzzo, M. Kohler, and D. Barater, "Dv/dt filtering techniques for electric drives: Review and challenges," in *IECON 2019-45th IEEE Ind. Elec. Soc.*, vol. 1. IEEE, 2019, pp. 7088–7093.

[9] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, and H. A. Mantooth, "A review of switching slew rate control for silicon carbide devices using active gate drivers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4096–4114, 2020.

[10] D. A. Rendusara and P. N. Enjeti, "An improved inverter output filter configuration reduces common and differential modes dv/dt at the motor terminals in pwm drive systems," *IEEE Transactions on Power Electronics*, vol. 13, no. 6, pp. 1135–1143, 1998.

[11] M. A. Gries and B. Mirafzal, "Permanent magnet motor-drive frequency response characterization for transient phenomena and conducted emi analysis," in *2008 Twenty-Third Annual IEEE App. Pow. Elec. Conf. and Expo.* IEEE, 2008, pp. 1767–1775.

[12] H. Kim, B.-H. Kim, and S. Bhattacharya, "An analytical design strategy and implementation of a dv/dt filter for wbg devices based high speed machine drives," in *IECON 2018-44th Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2018, pp. 385–390.

[13] N. E. M. Association *et al.*, *Motors and Generators: NEMA Standards Publication MG-1 2003*. Nat. Elec. Manu. Asso., 2003.

[14] J. He, C. Li, A. Jassal, N. Thiagarajan, Y. Zhang, S. Prabhakaran, C. Feliz, J. E. Graham, and X. Kang, "Multi-domain design optimization of dv/dt filter for sic-based three-phase inverters in high-frequency motor-drive applications," *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 5214–5222, 2019.

[15] A. Connaughton and T. Langbauer, "Fast estimation of best achievable inductor power density in circuit simulation (with dc-bias effects)," in *2021 IEEE Design Methodologies Conference (DMC)*. IEEE, 2021, pp. 1–6.

[16] P. Papamanolis, T. Guillod, F. Krismer, and J. W. Kolar, "Minimum loss operation and optimal design of high-frequency inductors for defined core and litz wire," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 469–487, 2020.

[17] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings.* IEEE, 2002, pp. 36–41.

[18] S. Zurek, "Encyclopedia of electromagnetics. [online].available:https://e-magnetica.pl/doku.php/thermal'resistance'of'ferrite'cores."