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A 129NW Neural Amplifier and Gm-C Filter for EEG Using gm/ID Methodology

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A 129nW NEURAL AMPLIFIER AND G_m-C FILTER

FOR EEG USING g_m/I_D METHODOLOGY

A Thesis

by

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ABSTRACT

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This Thesis presents a low-power analog front-end amplifier and G_m-C filter for biomedical sensing applications, specifically for Electroencephalogram (EEG) use. The proposed neural amplifier uses a supply voltage of 1.8V, it has a mid-band gain of 40.75dB, and consumes a total current of 71.82nA, for a total dissipated power of 129.276nW. Also presented is the design of a 3rd order Butterworth Low Pass G_m-C Filter which makes use of 14.7nS transconductors; the proposed filter has a pass band suitable for EEG recording use (1-100Hz). The amplifier and filter utilize current sources without bias resistances which provide 56nA and (1.154nA x 5) respectively. The proposed neural amplifier occupies a chip area of 0.275mm^2 in a 0.3µm TSMC process. Simulation of the schematic and extracted chip layout is presented, along with a comparison of similar published works. Finally, a projected power consumption calculation for a multichannel system based on this system is offered.

DEDICATION

To my mother who rests in peace; the completion of my studies would not have been possible without the love and support of my family. Thank you for your everlasting love, support, guidance, and patience.

To my best friend and the sunshine in my life. The completion of this manuscript would not have been possible without your encouragement and support. Thank you for always being there for me with the biggest smile.

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I would like to thank Dr. Heinrich Foltz not as my committee member but as an outstanding Electrical Engineering professor; thank you for your patience and for lighting students' candles with your knowledge; thank you for sharing all that experience in a manner that has truly been nourishing.

Finally, I would like to extend my gratitude to my colleagues in the Graduate Lab for their support and good laughs during the completion of this thesis project.

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CHAPTER I

INTRODUCTION

In recent years, research has been done on the miniaturization and development of low power, low noise integrated circuits (ICs) for biosignal sensing applications [1-8] due to their need in the medical field among clinicians and scientists in the field of neuroscience. These circuits need to be capable of amplifying biosignals in the milli Hertz to kilo Hertz range (as seen in Figure 1) while rejecting large DC offsets generated at the electrode-tissue interface [1]. These integrated circuits are being developed for implantable and portable wireless biosensor devices [3], in which multi-electrode neural recordings, for basic neuroscience research, are becoming increasingly common. The knowledge obtained from the studies in this area is beginning to enable clinical and neuroprosthetic applications for paralyzed patients, along with the use of brain controlled computer interfaces, and it is improving the diagnosis and monitoring of patients with epilepsy and sleep disorders.

The purpose of these integrated circuits is to sense biosignals with high fidelity and low power consumption. This is because biophysical signals are, in general, very weak (in the range of a few μV to mV) as can be seen in Figure 1, which leads to noise related concerns. These types of devices are also battery operated which makes low power consumption critical to reduce battery size, extend operating hours and minimize heat dissipation [8]. To address these critical concerns, this thesis project proposes circuits built with transistors operating in weak inversion

(subthreshold) that allow for the implementation of systems working below the microwatt range with low levels of input referred noise [5].

The analog front-end (AFE) amplifier plays a crucial role in biosensor integrated circuits because it usually determines the signal-to-noise ratio (SNR) of the entire neural recording system; therefore it is the most important component to ensure reliable monitoring of neural signals [3].

This thesis presents a low power, analog front-end amplifier and filter for use in neural measuring and recording applications. The proposed integrated circuit is intended for Electroencephalogram (EEG) applications in which, as shown in Figure 1, the biopotential signals vary in magnitude from 1µV to 100µV and in frequency from ~1-100Hz. It should also be noted and taken into account the interference at 60Hz from the power lines, which appear in the middle of the band of interest making it difficult to filter out.

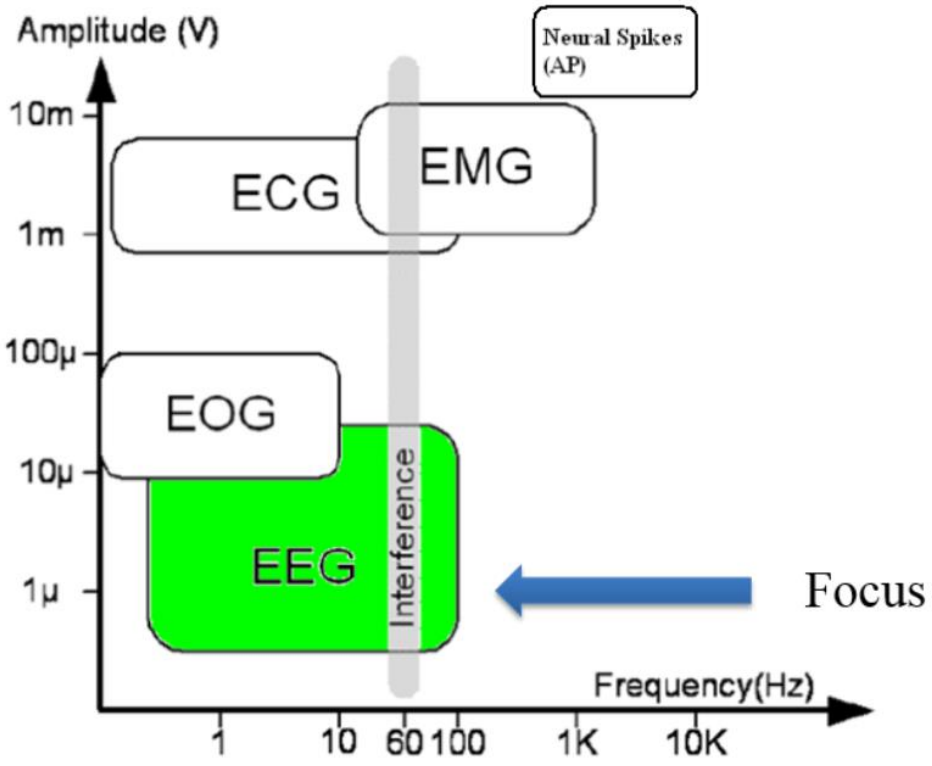


Figure 1. Frequency and amplitude ranges of different biopotential signals [7].

Figure 1 shows the frequency and amplitude ranges of a few biopotential signals that are encountered in common measurements such as the Electrocardiogram (ECG) –which measures cardiac signals; the Electroencephalogram (EEG) –which measures electrical signals from groups of neurons in the brain, right at the scalp; the Electromyogram (EMG) –which measures the electric signals that make muscles contract; and the Electrooculogram (EOG) –which measures electric charge difference between the front and back of the eye and is then correlated with eye movement. One can also observe a higher amplitude type of signal beginning around 1 KHz, called Action Potential (AP) or Neural Spike, this is an undesired signal for the Electroencephalogram measurement and therefore needs to be attenuated and filtered out.

Before diving into the following chapters dealing with the design of the circuits proposed in this thesis, let us first cover brief information on the electroencephalogram measurement, what it is, its uses, and applications; as well as review of the types of circuits used in the system presented in this thesis, such as the operational transconductance amplifier and the G_m-C filter.

Background Information

The Electroencephalogram (EEG)

The electroencephalogram (EEG) reflects the electrical activity of the brain as recorded by placing several electrodes on the scalp. The EEG is widely used for diagnostic evaluation of various brain disorders such as determining the type and location of the activity observed during an epileptic seizure, as well as for the study of sleep disorders such as: insomnia, hypersomnia, circadian rhythm disorders, and parasomnia. The brain activity may also be recorded during surgery by attaching the electrodes directly to the uncovered brain surface; the resulting invasive recording is named an electrocorticogram (ECoG) [14].

Another application for the EEG is of particular interest and is currently the research focus of many neuro scientists —brain-computer interface (BCI). Such an interface enables a subject to communicate with and control the external world without using the brain's normal output through peripheral nerves and muscles [22-24]. This type of interface significantly benefits subjects with severe neuromuscular disorders by allowing them to operate a neuroprothesis [14].

The clinical EEG is commonly recorded using a standardized system for electrode placement, called the International 10/20 system. This particular recording system employs 21 electrodes attached to the surface of the scalp at locations defined by certain anatomical reference points; the numbers 10 and 20 are percentages signifying relative distances between different electrode locations on the skull perimeter. Bipolar as well as unipolar electrodes are used in clinical EEG acquisition. Bipolar electrodes require a reference electrode either distantly or taken as the average of all electrodes [14]. A map of the electrode placement is shown in Figure 2.

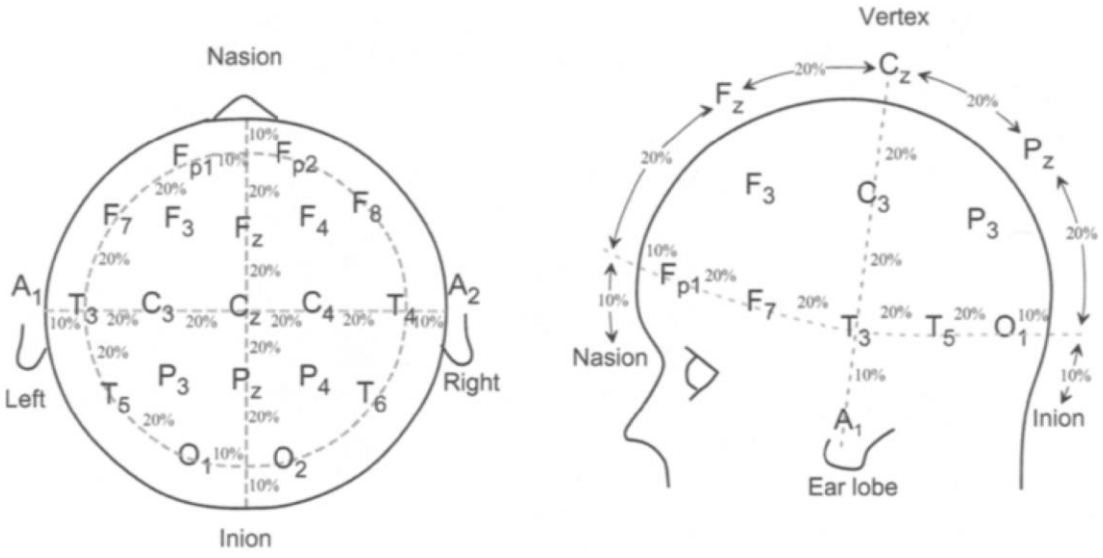


Figure 2. The International 10/20 system for recording of clinical EEGs. The anatomical reference points are defined as the top of the nose (nasion) and the back of the skull (inion). The letters F, P, C, T, O, and A denote frontal, parietal, central, temporal, occipital, and auricle, respectively. Note that odd-numbered electrodes are on the left side, even-numbered electrodes are on the right side, and z (zero) is along the midline [14].

In their book, *Bioelectrical Signal processing in Cardiac and Neurological Applications*, the authors explain that studies have indicated that the total number of electrodes used in the brain mapping applications should be 64 or higher in order to provide sufficient detail [14]. This statement leads to the conclusion that the International System, which consists of 21 electrodes, although minimal for clinical acquisition is not adequate for high quality recordings.

The measured signals at the scalp often exhibit oscillatory, repetitive behavior and may be referred to as rhythms. These brainwave signals, or rhythms, in the EEG range (1–100Hz) can be broken down as shown in Figure 3:

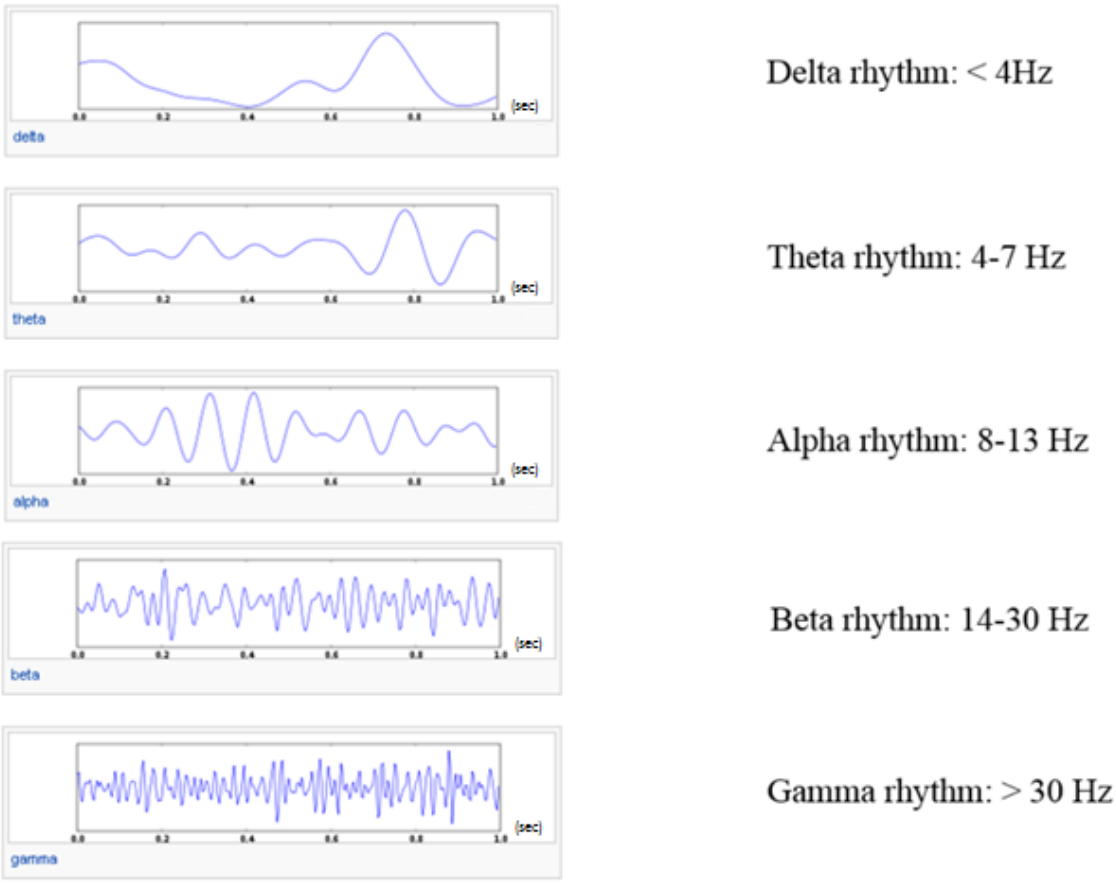


Figure 3. Examples of the different kinds of rhythms observed in an EEG.

Delta rhytm, <4Hz. The delta rhythm is typically seen during deep sleep and it is characteristic of having a large amplitude. It is usually not observed in the awake, normal adult, but is indicative of cerebral damage or brain disease (encephalopathy).

Theta rhythm, 4-7 Hz. The theta rhythm occurs during certain stages of sleep, as well as when a person is drowsy.

Alpha rhythm, 8-13 Hz. The alpha rhythm is most noticeable in normal subjects who are relaxed and awake with their eyes closed; this brain rhythm is suppressed when the eyes are open. The amplitude of the alpha rhythm is largest in the occipital regions.

Beta rhythm, 14-30 Hz. The beta rhythm is fast with and has a low amplitude, it is associated with an activated cortex and it can be observed during certain sleep stages. The beta rhythm is mainly observed in the frontal and central regions of the scalp.

Gamma rhythm, >30 Hz. The gamma rhythm is related to a state of active information processing of the cortex. Using an electrode located over the sensorimotor area and connected using high-sensitivity recording techniques, the gamma rhythm can be observed during finger movements.

The clinical interpretation of the EEG has evolved into a discipline in its own right, where the human interpreter has to draw conclusions based on the frequency, amplitude, morphology, and spatial distribution of the brain waves. The EEG remains a very powerful tool in the diagnosis of many diseases such as epilepsy, sleep disorders, and dementia. It also remains important for real-time monitoring of patients in a coma or with encephalopathy. The technical demands on equipment for recording EEGs are relatively modest and are, for a basic recording setup, restricted to a set of electrodes, a signal amplifier, and a personal computer for data

storage, signal analysis, and graphical presentation [14]. Figure 4 gives an illustration of the typical stages followed for this type of signal acquisition.

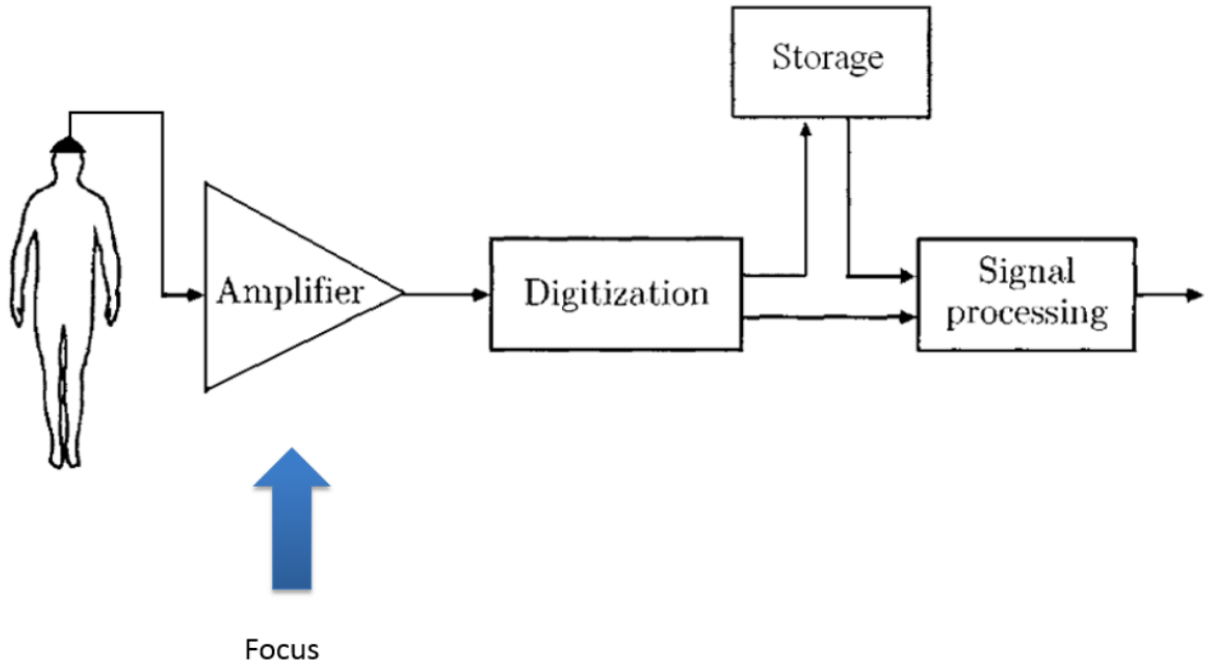


Figure 4. Block diagram describing the main steps in biomedical signal acquisition for analysis. The signal is often processed at the time of acquisition, but may also be stored on a local hard disk or a server on the web for later retrieval and processing [14]. This thesis focuses on the first block of the diagram (acquisition of the EEG).

The Operational Transconductance Amplifier (OTA)

The most important building block of the circuit designed in this project is the Operational Transconductance Amplifier (OTA). This type of amplifier is a device that generates a current as its output, as a function of the difference between two input voltages V_1 and V_2; that difference is called the differential input voltage. This circuit is also called a *differential transconductance amplifier*. An ordinary *conductance* circuit turns a voltage difference across two terminals into a current through the same two terminals. A *transconductance* circuit turns a voltage difference somewhere in the circuit into a current somewhere else in the circuit. In the transconductance amplifier, a voltage difference between two inputs created a current as the output. [25]

The differential transconductance amplifier is used in all the parts of the circuit designed in this project, it is used at the front end as an Operational Transconductance Amplifier with a high open-loop gain, and it is used several times, in a different configuration, in the filter. To understand the operation of such circuits and the neural amplifier as a whole, it is important to understand the idea of how a basic differential transconductor amplifier works.

First, let us discuss the differential pair, shown in Figure 5. This circuit is used as an input stage in which transistor Qb is used as a current source and its current I_b is normally saturated at a value set by the bias voltage V_b. This bias current is then divided between Q1 and Q2 as a function between the difference in the voltages V_1 and V_2 where the input is applied.

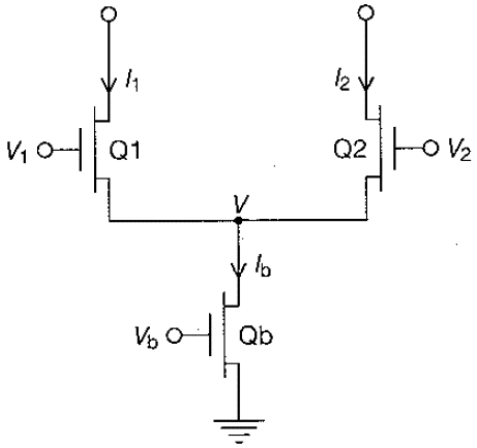


Figure 5. A schematic of the differential pair input stage [25]

The saturated drain current I_{sat} is given by the following equation, where I_0 and κ are constants.

$$I_{\text{sat}} = I_0 e^{\kappa V_g - V_s} \tag{1}$$

If equation (1) is then applied to transistors Q1 and Q2, one obtains

$$I_1 = I_0 e^{\kappa V_1 - V} \qquad \text{and} \qquad I_2 = I_0 e^{\kappa V_2 - V}$$

Applying Kirchoff's current law to node V, yields

$$I_b = I_1 + I_2 = I_0 e^{-V}\left(e^{\kappa V_1} + e^{\kappa V_2}\right)$$

Solving this equation for e^{-V} and substituting it in the equations obtained for I_1 and I_2, yields

$$I_1 = I_b \frac{e^{\kappa V_1}}{e^{\kappa V_1} + e^{\kappa V_2}} \qquad \text{and} \qquad I_2 = I_b \frac{e^{\kappa V_2}}{e^{\kappa V_1} + e^{\kappa V_2}} \tag{2}$$

From these two equations (2) for I_1 and I_2 one can see that if V_1 is more positive than V_2 by many *kT/(qκ)*, transistor Q2 gets turned off, which makes all the current flow through Q1, the current on Q2 is approximately equal to zero and the current I_1 is approximately equal to I_b. The same behavior can be observed on the other side, where if V_2 is more positive tan V1 by many *kT/(qκ)* then transistor Q1 gets turned off, which makes all the current flow through Q2, making the current on Q1 approximately equal to zero and the current I_2 approximately equal to I_b. This behavior can be observed graphically in Figure 6, where, as an example, the currents I_1 and I_2 and plotted as a function of the differential input voltage V_1-V_2.

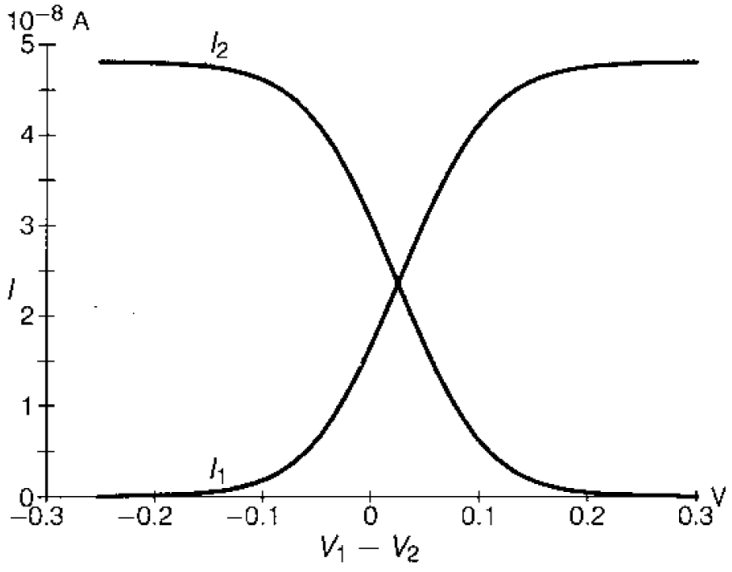


Figure 6. A graphical example of the currents I_1 and I_2 as a function of the input differential voltage V_1-V_2. Note that the curves do not cross at zero differential input voltage due to mismatch between Q1 and Q2 [25].

Furthermore, if one takes the difference of currents I_1 and I_2 as many of the differential transconductance amplifiers do to generate an output current that is proportional to it, we get

$$I_1 - I_2 = I_b \frac{e^{\kappa V_1} - e^{\kappa V_2}}{e^{\kappa V_1} + e^{\kappa V_2}}$$

Then, if one multiplies the numerator and denominator by a factor of $e^{-(V1 + V2)/2}$ the difference equation can be expressed as

$$I_1 - I_2 = I_b \frac{e^{\kappa(V_1 - V_2)/2} - e^{-\kappa(V_1 - V_2)/2}}{e^{\kappa(V_1 - V_2)/2} + e^{-\kappa(V_1 - V_2)/2}}$$

$$= I_b \tanh \frac{\kappa(V_1 - V_2)}{2}$$

The hyperbolic tangent function obtained in equation exhibits the actual real-world behavior of the amplifier output current. The *tanh* function goes through the origin with a slope of one, becomes +1 for large positive numbers and it becomes -1 for large negative numbers. Figure 7 shows a simple transconductance amplifier, which is the basis of many of the circuits presented in this thesis.

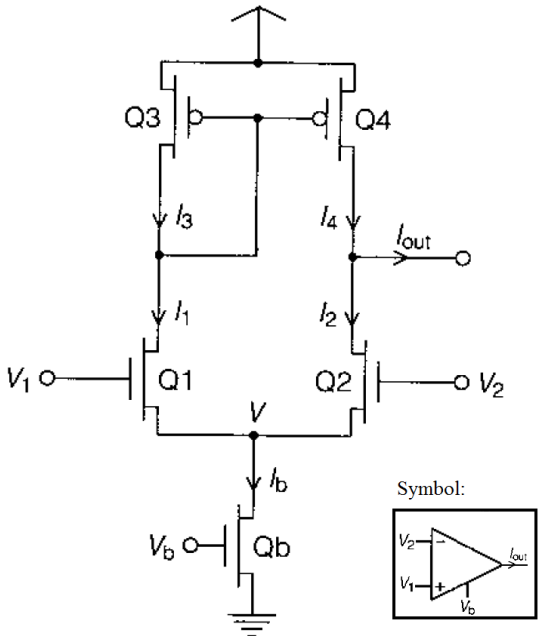


Figure 7. Simple Transconductance Amplifier and its symbol [25]

The circuit of the simple transconductance amplifier in Figure 7 consists of a differential pair just like the one shown in Figure 5 with a current mirror cascoded on top of it. The current mirror is used to subtract the currents of the differential pair I_1 and I_2, it does this by reflecting the current I_1 to Q4, which makes the output current I_{out} equal to I_1-I_2, given by the equation derived previously

$$I_1 - I_2 = I_b \tanh \frac{\kappa(V_1 - V_2)}{2} \qquad (3)$$

To verify this behavior, one can measure the output current of the amplifier as a function of the differential input voltage by keeping the output voltage midway between V_{DD} and ground, as shown in Figure 8.

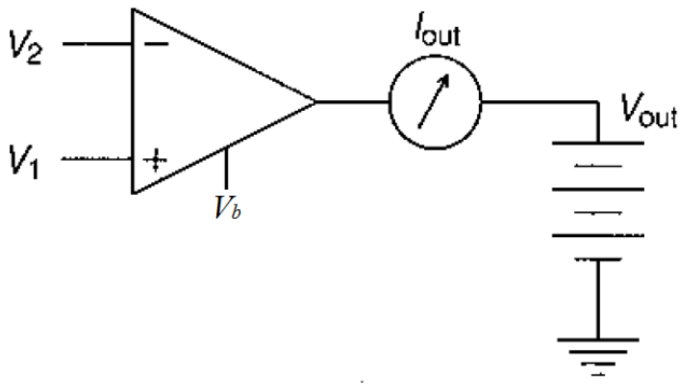


Figure 8. Set up to measure output current as a function of the differential input voltage. The ideal current meter should have zero resistance. V_{out} is held midway between V_{DD} and ground [25]

Figure 9 shows the output current plotted as a function of the differential input voltage. One can observe that the curve closely exhibits the expected behavior of the hyperbolic tangent function. Also, one can determine the effective value of $kT/(q\kappa)$ by extrapolating the slope of the curve at the origin to the two asymptotes. The difference between the positive and negative intercepts should be $4kT/(q\kappa)$ [25].

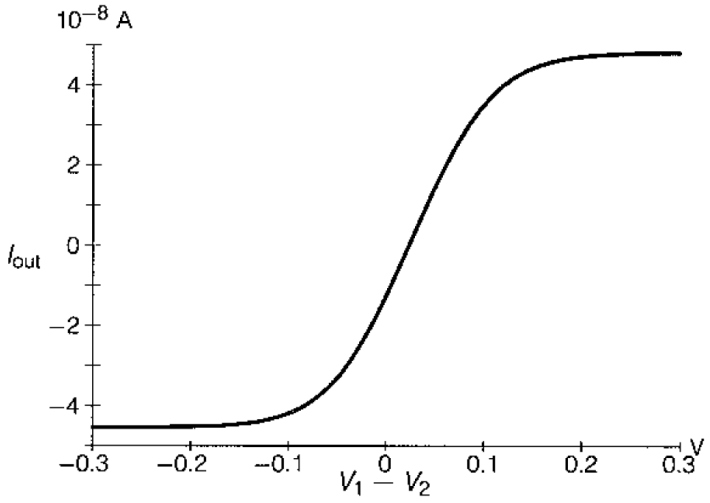


Figure 9. Output current of the transconductance amplifier as a function of the differential input voltage. [25]

For the example curve shown in Figure 9, using the procedure mentioned, one can determine that *kT/(qκ)* for this particular example is approximately 43mV, which gives κ as approximately 0.58. The transconductance, G_m, of the amplifier is defined as the slope of the *tanh* function at the origin in the equation for the output current. From Figure 9, one can determine that G_m is approximately 560nS. The transconductance of the amplifier is defined as the change in the output current divided by the change in the differential input voltage, the equation for G_m is then

$$G_{\mathrm{m}} = \frac{\partial I_{\mathrm{out}}}{\partial V_{\mathrm{in}}} = \frac{I_{\mathrm{b}}}{2kT/(q\kappa)} \tag{4}$$

Now let us consider the case when the output voltage is not held constant as in Figure 8. Let us plot the output current, but this time, as function of the output voltage. This is shown in Figure 10, where one can observe the limitations of this circuit due to transistor mismatches, transistors coming out of saturation, as well as the finite slope of the drain curves in saturation [25].

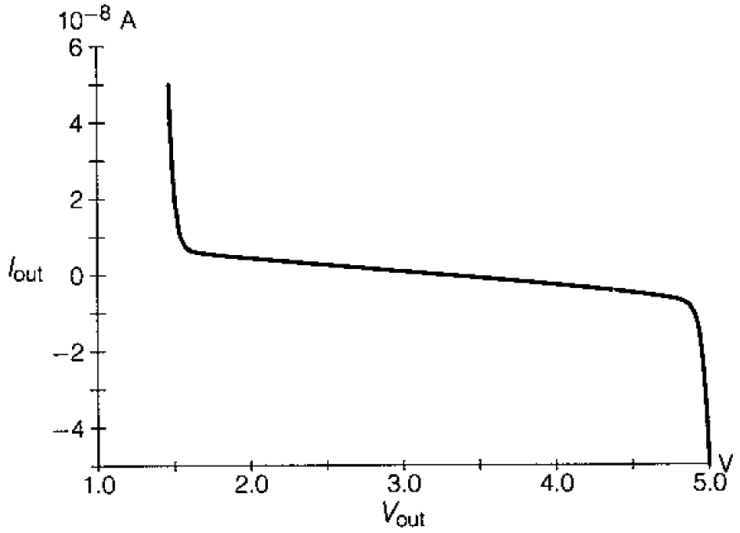


Figure 10. Output current as a function of the output voltage. [25]

Figure 10 shows that the output current decreases as the output voltage increases. The decrease in the output current per change in the output voltage is called the output conductance, G_{out}, of the circuit and is given by equation (5):

$$G_{out} = -\frac{\partial I_{out}}{\partial V_{out}} = \frac{\partial I_2}{\partial V_{out}} - \frac{\partial I_4}{\partial V_{out}} \qquad (5)$$

The output conductance is the inverse of the output resistance of the circuit and it is the negative slope of the middle region of the plot in Figure 10. The output conductance, G_{out}, is approximately 3.6nS from Figure 10. The open-circuit voltage gain of the circuit should be given then by the following equation:

$$A = \frac{G_m}{G_{out}} \quad or \quad A = G_m R_{out} \qquad (6)$$

Using the values we have obtained for G_m and G_{out}, the open-circuit gain of the simple transconductance amplifier example is A = 560nS / 3.6nS = 156.

Finally, let us consider the importance of the Early Voltage and how it affects the amplifier's gain. The slope of the saturated part of the drain curves of a given transistor has a

slope proportional to the current level transistor's drain curve in saturation. In other words, the V_{ds} intercept occurs at a voltage V_0 (the Early Voltage) that is approximately independent of the current level [25].

$$\frac{\partial I_{\text{sat}}}{\partial V_{\text{ds}}} \approx \frac{I_{\text{sat}}}{V_0}$$

As seen previously both G_{out} and G_m are proportional to the bias current, which makes the explicit dependence on the current level to cancel out and makes the voltage gain independent of the bias current. The change in current over the change in voltage can be expressed in terms of the Early Voltage values V_0.

$$\frac{1}{A} = \left(\frac{1}{V_{\text{N}}} + \frac{1}{V_{\text{P}}}\right)\frac{2}{\kappa} \qquad (7)$$

In equation (7), V_N is the Early Voltage for Q2 and V_P is the Early Voltage for Q4, and both are expressed in *kT/q* units. This equation allows one to compute the gain of any output stage composed of complementary n and p channel transistors. Because the Early voltage V_0 of a given transistor is proportional to its length [25], one can make the gain of the amplifier randomly high by increasing the length of the output transistors and sacrificing silicon area in the chip.

Figure 11 shows an improved version of the transconductance amplifier shown in Figure 7. This circuit has current mirrors on both sides of the differential pair, and an extra one on the further leg from the output to achieve the differential output current (I_1-I_2) of the transconductance amplifier. Such circuit is used by Harrison in the neural amplifiers presented in [1] and [2].

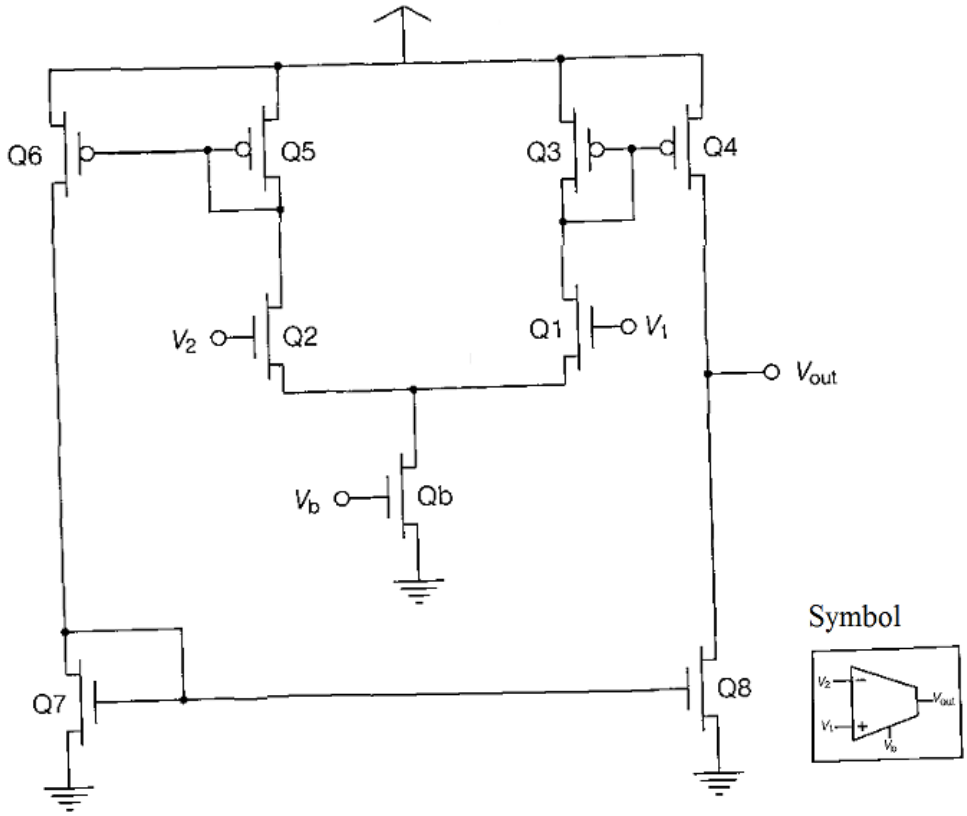


Figure 11. Wide Range Transconductance Amplifier with NMOS differential input pair. [25]

The major advantage of this wide-range amplifier over the simple transconductance amplifier is that it does not have the limitations that the simple one has; in this circuit, both input and output voltages can run almost up to V_{DD} and almost down to ground, without affecting the operation of the circuit [25].

The G_m-C Filter

The filter is a critical building block in any biosignal acquisition system, it is needed not only to enhance the quality of the signal but to add selectability to the system. Signals in biopotential acquisition systems, as mentioned before, are very weak which makes them especially susceptible to noise. The type of filter used in the system presented in this thesis is a G_m-C Filter, meaning it is made up of transconductors and capacitors. This kind of circuit is an

analog continuous-time filter, as well as active—meaning it uses power. G_m-C filters are suitable for applications with frequencies less than 100MHz, which is the case of the system presented here, where the EEG band is 1-100Hz as seen before in Figure 1.

In comparison with discrete-time switched-capacitor filters such as those used in digital systems, continuous-time filters possess the advantage of lower power consumption, since they only drive capacitive loads, as well as not having the switching noise that the switched-capacitor filters inherently have. Among all continuous-time filters, the G_m-C topology appears to be the most reasonable choice for integrated circuits [20], where it is hard to achieve specific inductor values to construct LC passive filters. In G_m-C filters, the cutoff frequency is proportional to the transconductance g_m, which allows a low-power implementation for the acquisition of low frequency biopotential signals. G_m has to be minimized in order to achieve an ultra-low cutoff frequency with a reasonable area and power [20].

To achieve performance on a G_m-C filter it is important for the transconductor to behave as an ideal operational transconductance amplifier, it should have a very high gain, as well as have a very high input and output resistance, ideally infinite, as seen in Figure 12. In essence, the transconductor operates as a voltage-controlled current source, where the output current is:

$$i_o = G_m v_i \tag{8}$$

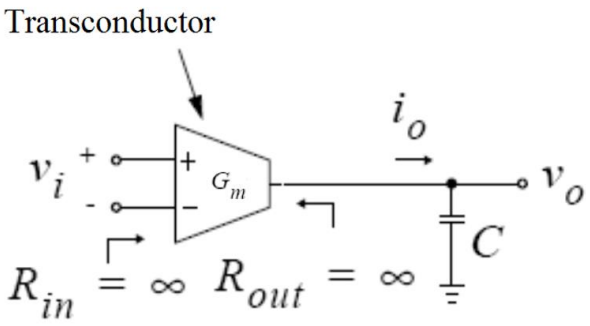


Figure 12. The ideal transconductor in the G_m-C filter

This is important because as explained before, because G_m needs to be low to achieve the low cutoff frequencies needed in these type of applications, the output resistance of the transconductor needs to be very high to achieve a high gain.

Let us take a look at a very simple single pole circuit that behaves as a G_m-C low pass filter, such as the one shown in Figure 13.

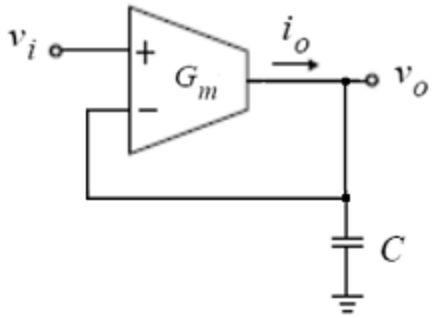


Figure 13. Simple single pole Gm-C low pass filter

To obtain the transfer function of the circuit shown in Figure 13, let us begin by applying Kirchoff's Current Law at the output node v_o, where the impedance of the capacitor is 1/sC:

$$\frac{v_o - 0}{1/_{sC}} - i_o = 0$$

As explained before, the operational transconductor amplifier behaves as a voltage controlled current source, of which the output current is a function of the differential input voltage. This is expressed with the following equation:

$$i_o = G_m(v_i - v_o)$$

Substituting this equation in the previous equation, one gets

$$\frac{v_o - 0}{1/_{sC}} - G_m(v_i - v_o) = 0$$

Solving for the transfer function v_o / v_i yields

$$\frac{v_o}{v_i} = \frac{G_m/C}{s + G_m/C} = \frac{\omega_0}{s + \omega_0}$$

From the obtained transfer function, we can observe that it is the same as a single order system transfer function and that the circuit behaves as a single pole low pass filter, where the cutoff frequency is $\omega_0 = G_m/C$. The gain plot of the frequency response of this circuit is shown in Figure 14.

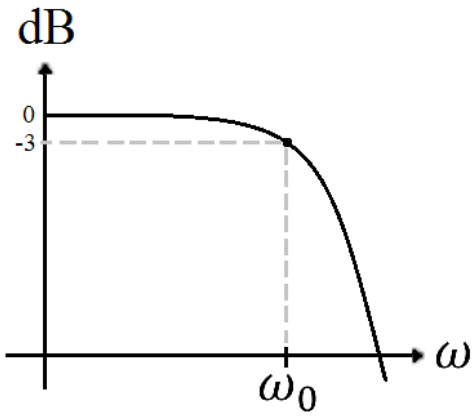


Figure 14. Frequency response dB gain plot of the simple single pole G_m-C low pass filter

In a similar manner Chapter V will present how this theory is applied to the design of a 3rd order Butterworth G_m-C filter that meets the frequency needs of the system.

Thesis Structure

The following chapters of this Thesis are organized as follows, Chapter II presents and reviews relevant published literature on the subject matter related to this Thesis; Chapter III explains the g_m/I_D methodology used in the design of the circuits presented, as well as its importance, application, and relevance to the system; Chapter IV is dedicated to explaining how the methodology described in Chapter II to was used to design the front-end OTA; Chapter V is dedicated to the description of the design of the G_m-C Filter used in the system; Chapter VI

presents the simulation results and comparison of the system to similar published works; and finally, Chapter VII gives a conclusion and provides suggestions and details for future work on this project.

Before we continue to the following chapters, let us take a look at the overall system architecture of the system proposed in this thesis for the neural amplifier. This diagram can be seen in Figure 15 and is composed of the analog front-end Operational Transconductance amplifier (OTA), which will need something at the input to block the DC offsets created at the scalp. It will be connected in a negative feedback configuration for stability and to achieve the desired gain. A 3rd order Butterworth Low Pass G_m-C Filter will follow the operational transconductance at the front end and it will have a proper cutoff frequency for the EEG band that will also be enough to attenuate the Neural Spikes described in Figure 1, which are present beginning at 1 kHz. A capacitive load will be used to simulate the next system in the signal acquisition diagram shown in Figure 4, such as an analog to digital converter.

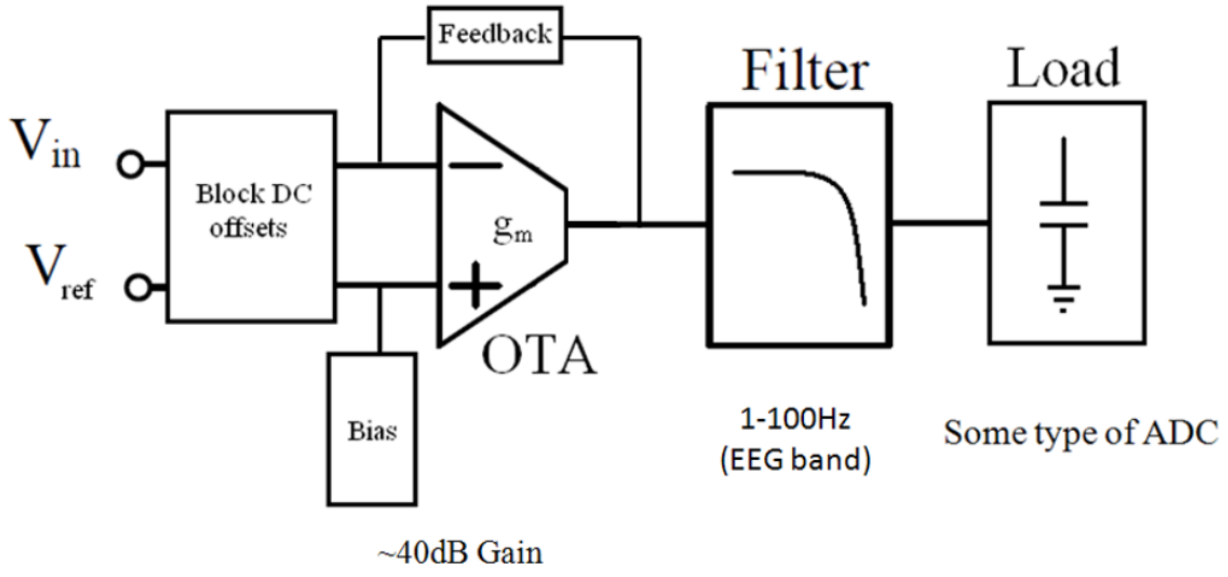


Figure 15. Overall system diagram for the Neural Amplifier analog front-end integrated circuit. The system consists of a unit to block the DC offsets created at the scalp, the OTA with its closed-loop feedback and bias to achieve the desired gain, a filter to capture the signals in the desired band and attenuate Neural Spikes, and finally a load to simulate the next block in the acquisition system such as an analog to digital converter.

CHAPTER II

LITERATURE REVIEW

Increasing interest and advances in neuroscience over the past decade, as mentioned in Chapter I, have led to the need for development, as well as, improvement of circuits to utilize in neural recording applications such as the EEG. This chapter focuses on reviewing a few of the neural amplifiers published in literature in the last decade, especially those scholar publications relevant to this thesis project. A comparison between these published works and the system presented in this manuscript will be presented in Chapter VI.

There have been a significant amount of neural amplifiers published in literature in recent years, most of which aim at low-noise and low power [1-8]. For a better comparison among these published circuits, as well as to aid in the understanding of their efficiency, a figure of merit, called Noise Efficiency Factor (NEF), was introduced in by Steyaert, Sansen, and Zhongyuan in [12]. The NEF compares the power-noise tradeoff among amplifiers and it is widely used to compare neural-amplifier designs. The noise efficiency factor is defined as:

$$\mathrm{NEF} = V_{\mathrm{rms,\,in}}\sqrt{\frac{2\cdot I_{tot}}{\pi\cdot U_T\cdot 4kT\cdot \mathrm{BW}}} \tag{9}$$

where V_{rms} is the total equivalent input noise, I_{tot} is the total current consumed by the system, U_T is the thermal voltage KT/q (≈ 25mV at room temperature), k is Boltzmann's constant, T is the temperature in Kelvin, and BW is the bandwidth of the system.

One of the reasons for choosing to use the Capacitive Feedback Network (shown in Figure 16) for the neural amplifier proposed in this manuscript, comes from a recent publication titled, "*A review of low-noise amplifiers for neural applications*" [9] where the authors present a comparative study of three topologies for neural recording applications: Capacitive Feedback Network (CFN), Miller Integrator Feedback Network (MIFN), and Capacitive Amplifier Feedback Network (CAFN). These configurations are some of the more common topologies presented in literature. In the study made by the authors in [9], these three topologies are analyzed in terms of area, power consumption and noise performance. The authors come to the conclusion that "based upon theoretical developments and transistor-level explorations, [the study] reveals that the [Capacitive Feedback Network] CFN achieves the best performance in terms of area and power consumption for a given input-referred noise specification." [9]

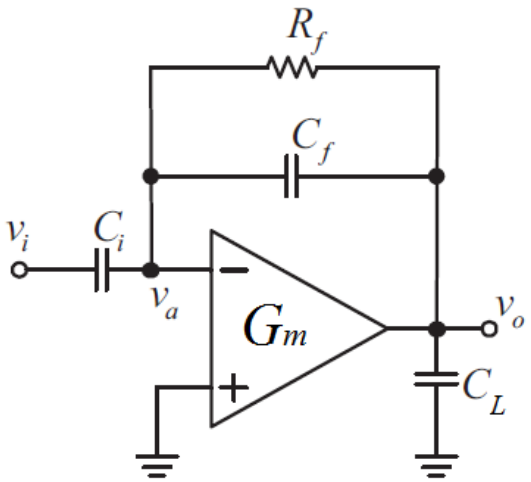


Figure 16. Capacitive Feedback Network for neural amplifier [9]

This simple structure has a bandpass shaped frequency response, on which one can achieve a desired mid-band gain, as well as the desired low and high cutoff frequencies by picking the values of the input capacitor C_i, the feedback capacitor C_f and resistor R_f, and the load capacitor C_L. This behavior is dependent on having an operational transconductance

amplifier with a very high open-loop gain and a very high output resistance, and one where its transconductance is given by the transconductance of one of its input transistors.

A pioneer publication that has been a reference, not only to this project, but that has been cited multiple times by most of the researched papers reviewed during this research project is the "*Low Power Low Noise Amplifier for Neural Recording Applications*" presented by Harrison in 2002 [1] along with a similar follow-up paper that was published a year later in 2003 by Harrison and Charles [2]. The neural amplifier presented by Harrison and Charles utilizes the Capacitive Feedback Network mentioned before; the configuration presented in this research paper is shown in Figure 17. In this neural amplifier, a wide-range current mirror Operational Transconductance Amplifier, such as the one shown in Figure 11, is utilized. This type of circuit is not very power and noise efficient as much of the current that it draws is wasted in the current mirrors. The neural amplifier proposed by Harrison and Charles in [1, 2] has a dual supply voltage of ±2.5 V and consumes 180 nA of current, which yields a 900 nW power consumption. The authors also report that amplifier has a measured gain of 39.8 dB and a bandwidth of 14 mHz - 30 Hz; an input-referred noise of 1.6uVrms was measured on this device, yielding a NEF of 4.8. The amplifier was built in a 1.5um CMOS technology and occupies a chip area of 0.22mm^2.

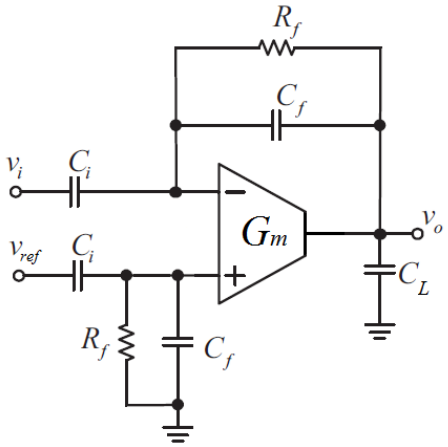


Figure 17. Theoretical Capacitive Feedback Network neural amplifier proposed by Harrison and Charles in [1, 2] on which two series diode-connected pMOS act as the R_f resistors

In [1, 2] the authors use pseudo-resistors made with a couple of MOS-bipolar devices joined as diode-connected pMOS transistors to replace the R_f resistors in Figure 17. Two of this devices as connected in series to reduce distortion for large output signals. The authors mention that "with positive V_{GS}, the parasitic source-well-drain p-n-p bipolar junction transistor (BJT) is activated, and the device acts as a diode-connected BJT" [2]. The authors claim to have measured a resistance greater than 10^{11} Ω for small voltage changes across the pseudo resistors. The proposed neural amplifier with Capacitive Feedback Network and the diode-connected pseudo-resistors is shown in Figure 18.

If one looks at the operational transconductance amplifier used in the neural amplifier proposed in [1, 2], shown in Figure 18, and compares it with the one shown in Figure 11, one can observe that the circuit proposed in [1, 2] uses pMOS transistors instead of nMOS transistors for the differential input pair. This is because a major concern for a low-frequency circuit, whose main purpose is to have low noise, is flicker noise (also called 1/*f* noise). The authors explain that, "flicker noise in pMOS transistors is typically one to two orders of magnitude lower than flicker noise in nMOS transistors as long as $|V_{GS}|$ does not exceed the threshold voltage" [2].

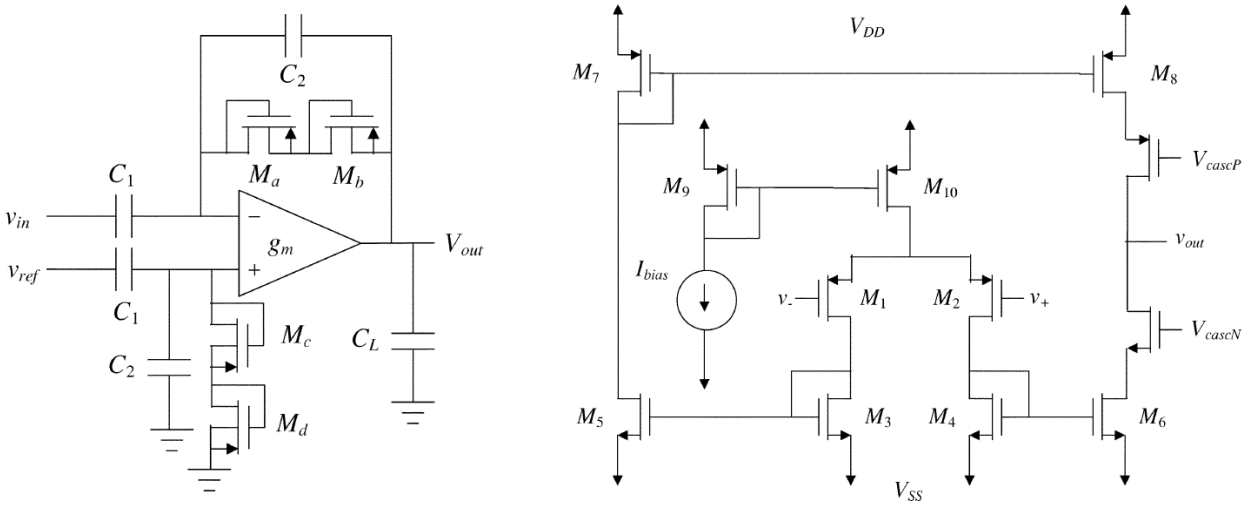


Figure 18. The neural amplifier configuration and the OTA proposed by Harrison and Charles in [1, 2]

A second reference research publication of particular importance to the research project presented in this manuscript is the "*Energy-Efficient Micropower Neural Recording Amplifier*" [6] proposed by Wattanapanitch, Fee, and Sarpeshkar in 2007. In it, the authors propose a novel folded cascode topology for the operational transconductance amplifier, shown in Figure 19, which they claim appears to be the lowest power and most energy-efficient neural recording amplifier reported to date (2007). A modified version of this folded cascode topology for the operational transconductance amplifier was adopted in the research project presented in this manuscript. In the research paper [6] the authors report that their proposed amplifier, when configured to measure Local Field Potentials (EEG range), uses a 2.8 V supply voltage and consumes 743 nA of current, which yields 2.08 µW of total power consumption. They also claim that their proposed amplifier achieves a mid-band gain of 40.9 dB over a bandwidth ranging from 392 mHz to 295 Hz. An input-referred noise of 1.66µ V_{rms} was measured on this device, corresponding to a NEF of 3.21. This energy-efficient micropower neural amplifier was built in AMI's 0.5 µm CMOS process and occupies a chip area of 0.16mm^2.

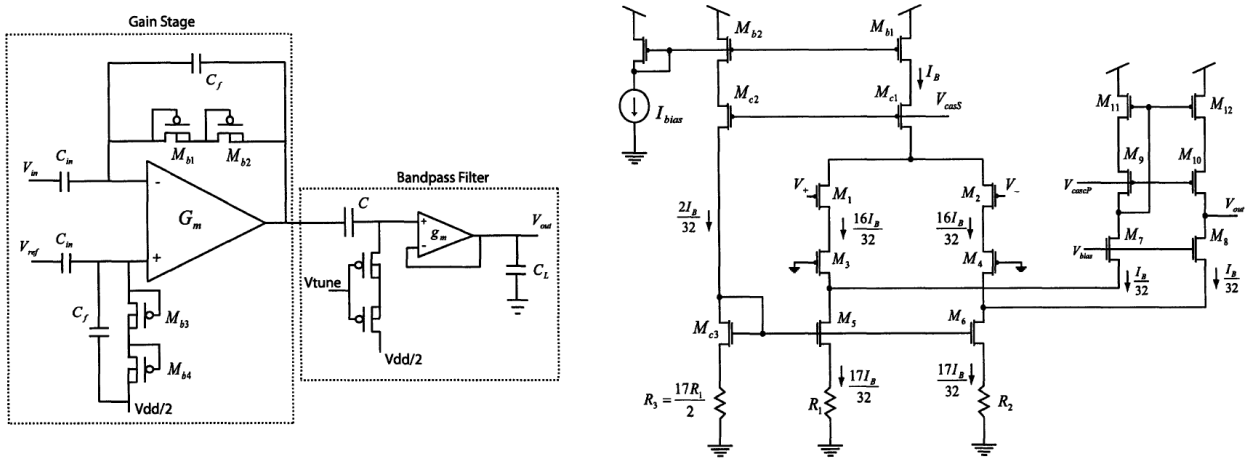


Figure 19. The neural amplifier configuration and the OTA proposed by Wattanapanitch, Fee, and Sarpeshkar in [6]

We can observe from Figure 19 that the authors in [6] also use the Capacitive Feedback Network topology for their neural amplifier. In this design, however, the authors use a band-pass filter after the front-end amplifier, which can be tuned with an external voltage V_{tune}, to adjust the frequency range to measure different type of signals. The reader should note that this band-pass filter is made up of a high-pass filter that uses a capacitor *C* and a pseudo-resistor like the ones presented by Harrison and Charles in [1, 2] followed by a simple G_m-C low pass filter just like the one presented in the example in Chapter I. The folded cascode topology for the operational transconductance amplifier used in the circuit is also shown in Figure 19. In this circuit, the authors use a severe $1/16^{th}$ current scaling as well as 17 source-degenerated current mirrors for the current mirrors made up by transistors M_{c3}, M_5, and resistors R_3 and R_1.

A more recent publication made in 2012 (this thesis project was started in the Fall of 2012) by Liu, Zou, Goh, Ramamoorthy, Dawe, and Je describes an "*800nW neural recording amplifier with enhanced noise efficiency factor*" [3]. This amplifier uses a very low 1 V power supply and consumes a total current of 160 nA, yielding a 160 nW power consumption. This amplifier has a gain of 40 dB similar to the other systems reviewed in this chapter, as well as most of the amplifiers in literature, and a bandwidth of 200 mHz to 430 Hz; an input-referred noise of 5.71 μV_{rms} was measured on this device, corresponding to a very good NEF of 2.59. The amplifier was built in a 0.18µm CMOS technology and occupies a chip area of $0.05mm^2$. The neural amplifier schematic proposed in this research publication, along with the operational transconductance amplifier used, is shown in Figure 20. One can observe in this figure that the authors use a fully differential configuration for the amplifier, as well as a Capacitive Feedback Network similar to the ones in the publications reviewed in this chapter. The fully differential structure helps to reduce the effect of the common mode noise [3]. The front-end amplifier is

then followed by a bandpass filter that provides additional gain; details are not given by the authors on the structure of the filter nor are details given on the bias circuits and currents needed. This last point will become particularly important in Chapter VI where a comparison between the system proposed in this thesis and several of the amplifiers reviewed in this chapter is made. When presenting their results, particularly current consumption, most authors in the publications that were reviewed during this research come to the conclusion that this is not reported because bias circuits can be shared by many parts of the integrated circuit, although this statement is true, it is important to establish how such currents are sourced because it can be done with numerous different types of bias circuits, some of which are more power efficient than others.

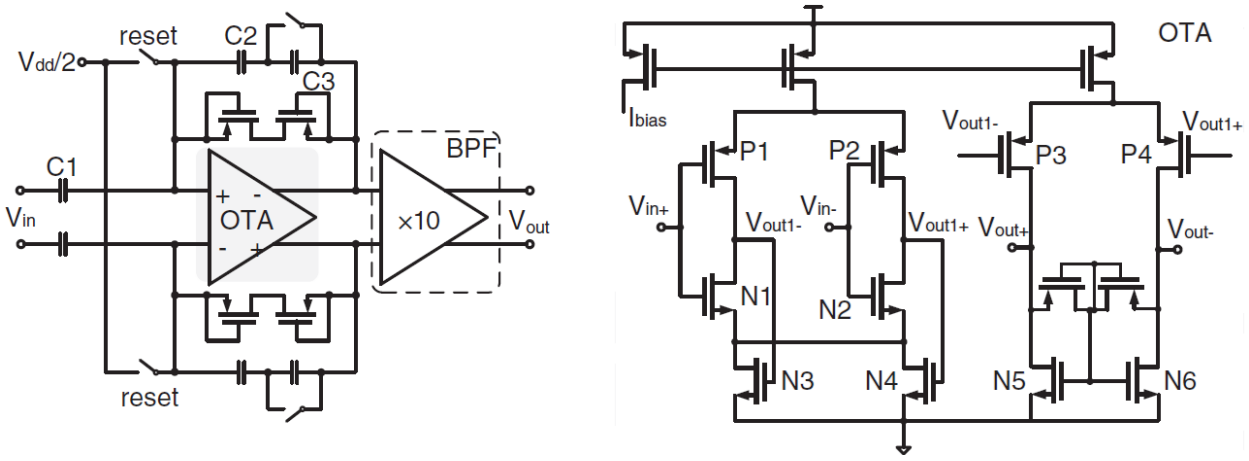


Figure 20. The proposed neural amplifier and OTA [3]

Finally, a comprehensive overview in the topic of neural recording systems is summarized and explained in a recent publication by Gosselin titled "*Recent Advances in Neural Recording Microsystems*" [19]. This research paper describes the most relevant developments made in this area and gives insight to the approaches taken by several researchers to tackle problems in neural recording and acquisition systems. This journal paper examines most of the circuit topologies presented in this chapter and provides a comparison between the most power

and noise efficient operational transconductance amplifier structures that constitute the core of most of the neural amplifiers published to date, discussing their characteristics and advantages. This publication is extensive and particularly useful since it has reviewed 106 research publications related to neural recording microsystems published in the past 30 years.

Now that we have reviewed some of the neural amplifiers in literature, described the techniques used in these circuits, and established a concise figure of merit, in the NEF, to adequately compare these designs. It is time to describe the design of the neural amplifier proposed in this thesis project, beginning with the methodology used in the circuits.

CHAPTER III

THE g_m/I_D METHODOLOGY

As explained in previous chapters, it is imperative for the neural amplifier's circuits to achieve high efficiency and low power. To be able to achieve these criteria, a transistor characterization methodology, known as g_m/I_D, was applied; the theory and application to the circuits in this project is described in this chapter. This methodology's importance to the thesis project presented in this manuscript comes from the fact that it was used as a sizing tool to help determine the sizes of the transistors, making them operate in a desired region that is power efficient, such as the subthreshold region. This design method was originally introduced and explained in detail by Silveira, Flandre, and Jespers in their publication titled, "*A g_m/I_D based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA*" [11].

In this publication, the authors define the g_m/I_D methodology as "a new design methodology that allows a unified synthesis methodology in all regions of operation of the MOS transistor." Furthermore, they explain that their method, "provides an alternative [to traditional analysis methods] taking full advantage of the moderate inversion region to obtain a reasonable speed-power compromise. The method exploits the transconductance over DC drain current ratio *(g_m/I_D)* relationship versus the normalized current [$I_D/(W/L)$]" [11].

Why use the g_m/I_D method? Well, the authors argue that the choice of g_m/I_D is based on its relevance for the following three reasons:

1) It is strongly related to the performances of analog circuits

2) It gives an indication of the device operating region.

3) It provides a tool for calculating the transistors dimensions.

The g_m/I_D ratio is also referred to as the transconductance efficiency and it is a measure of how efficiently a transistor translates current (hence power) into transconductance. This means that the higher the value of this ratio, the higher the transconductance obtained is at a constant value [11]. It is used because for deep submicron processes and subthreshold region of operation, analytical or hand methods for synthesizing analog circuits rely on classic square law model equations that are no longer accurate and useful in describing the behavior of the transistor in all regions of operation and therefore not good for design purposes.

The authors in their journal paper [11] define g_m/I_D as the derivative of the logarithm of the normalized I_D with respect to V_G as shown in equation (10):

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_G} = \frac{\partial(\ln I_D)}{\partial V_G} = \frac{\partial\left\{\ln\left[\dfrac{I_D}{\left(\dfrac{W}{L}\right)}\right]\right\}}{\partial V_G} \qquad (10)$$

Equation (10) will be used to obtain the plots that indicate the transistor's mode of operation. But first, let us consider the dependence of g_m/I_D on the transistor size since one needs to specify transistor sizes to characterize the transistors through simulation. The authors state that the normalized current $I_D/(W/L)$ as well as the g_m/I_D ratio are independent of the transistors size. This means that the relationship between "g_m/I_D and the normalized current is a unique

characteristic for all transistors of the same type (nMOS or pMOS) in a given batch" [11]. In other words, g_m/I_D is a universal characteristic governing all the transistors that belong to the same technology or process.

Obtaining the plot of g_m/I_D vs. $I_D/(W/L)$ for NMOS and PMOS

The g_m/I_D design methodology is based on measuring, or more specifically characterizing the transistor through simulation and using the different plots obtained as lookup tables in the design process to size the transistors in a way that they achieve the desired currents (and therefore the desired power consumption) at the required bias voltages.

Because the system was aimed at low power it was decided that a low voltage process should be used instead of a traditional 5V digital process used in introductory academic VLSI classes. The lowest voltage and smallest process available to me for the implementation of the design was a 2.5 V TSMC process, however since this specification is only a limit, it was decided that 1.8V could be used in that same process. The Spice TSMC 25 models given in Appendix A for both NMOS and PMOS transistors, for the 300nm TSMC process in use, were obtained from wafer test data for a similar process provided by MOSIS (www.mosis.com). Using equation (10) for g_m/I_D and these transistor models, the circuits in Figures 21 and 23 were simulated to characterize the transistors in this technology and obtain the desired plots.

In the test circuit shown in Figure 21, V_{DS} was held at $V_{DD}/2$ since there is not a lot of variation for any changes in V_{DS}; V_{GS} is swept from 0V to V_{DD} (1.8V). This simulation will yield a plot of I_D vs. V_{GS} which one can turn into a plot of g_m/I_D vs. V_{GS} with the help from the trace calculator in PSpice and the equation for g_m/I_D.

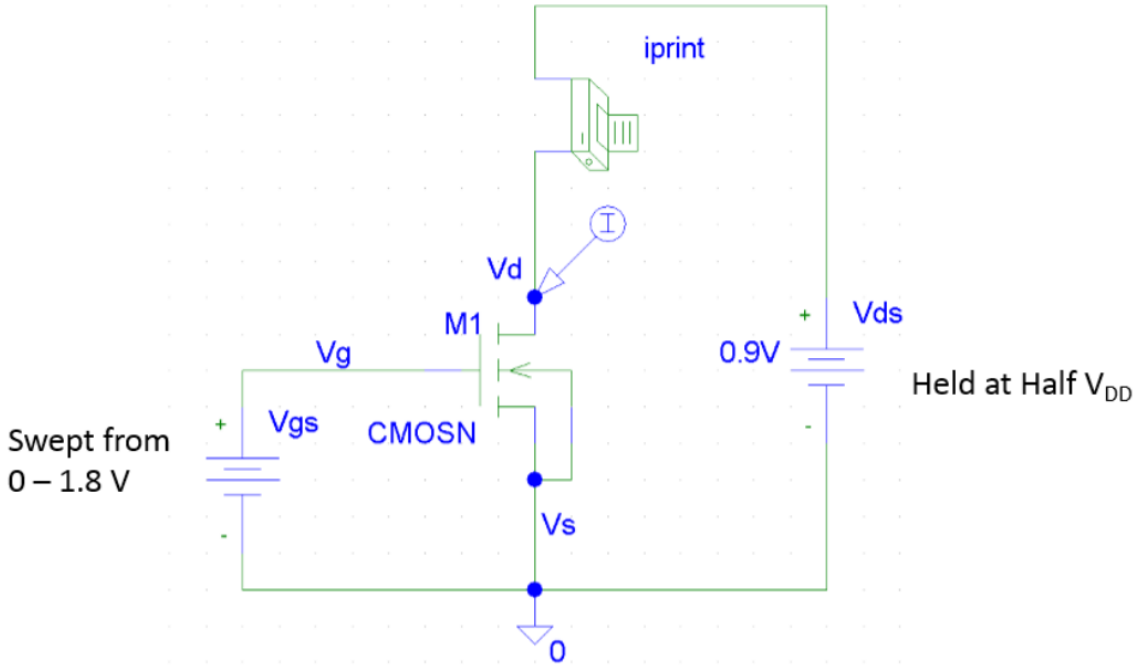


Figure 21. Test circuit to characterize the NMOS transistor in the 300nm TSMC process.

Figure 22 below shows the obtained g_m/I_D vs. V_{GS} plot for the NMOS in the 300nm TSMC process.

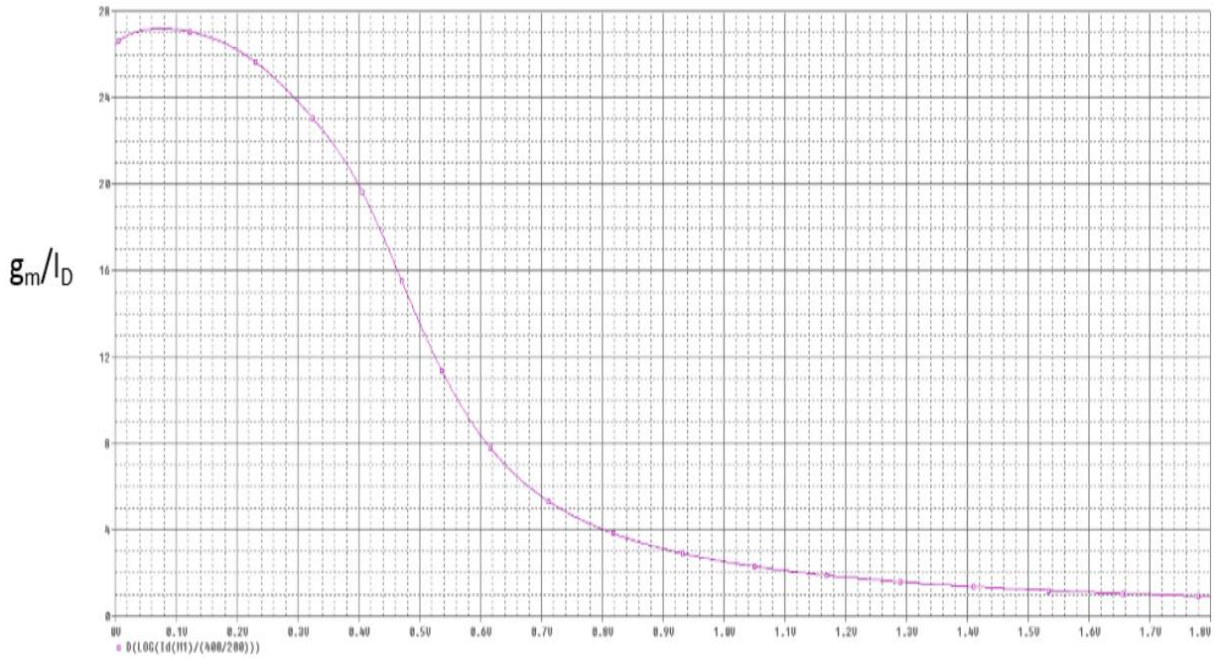


Figure 22. g_m/I_D vs. V_{GS} curve for NMOS with TSMC 25 transistor model

In a similar manner, the PMOS was characterized using the circuit shown in Figure 23. For the PMOS V_{DS} was again held at $V_{DD}/2$ and V_{SG} was swept from 0V to V_{DD} (1.8V). This simulation yielded a plot of I_D vs. V_{GS} which was turned into a plot of g_m/I_D vs. V_{SG}, shown in Figure 24.

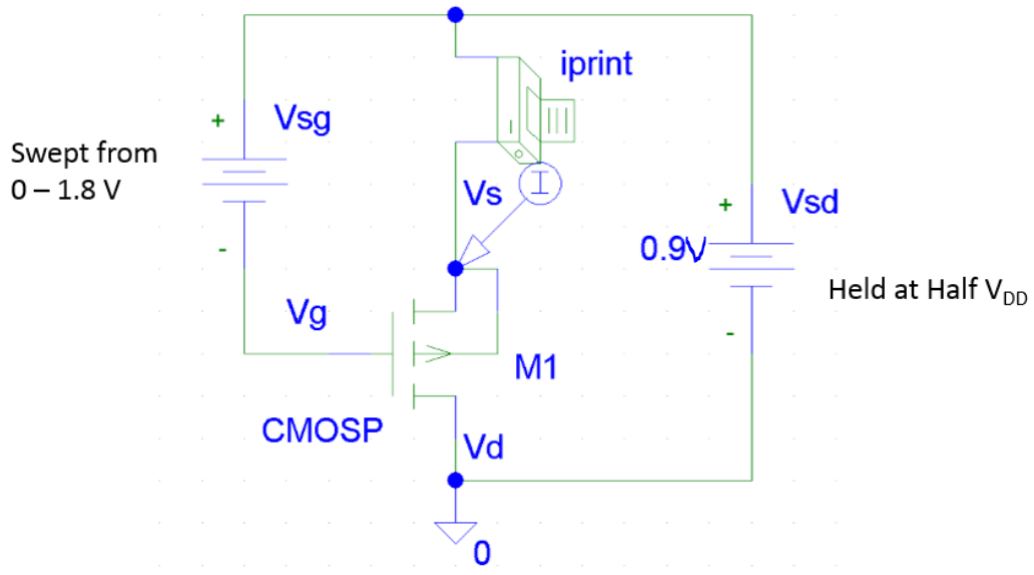


Figure 23. Test circuit to characterize the PMOS transistor in the 300nm TSMC 25 process.

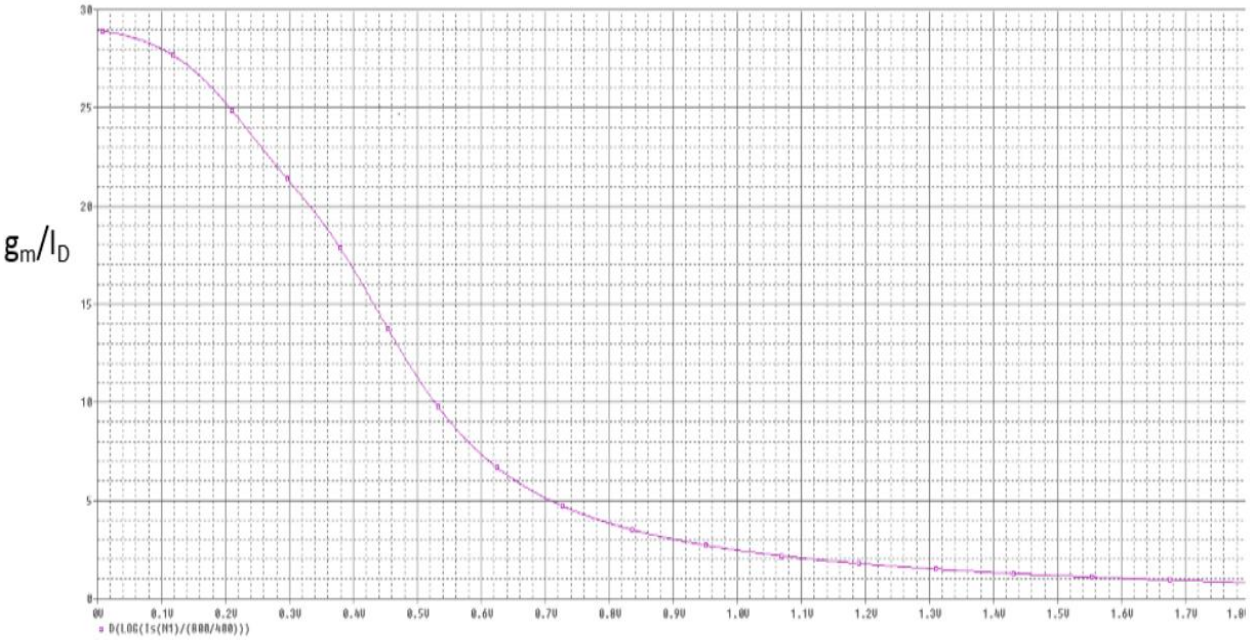


Figure 24. g_m/I_D vs. V_{SG} curve for PMOS with TSMC 25 transistor model

Using the obtained PSpice simulation plots of g_m/I_D vs. V_{GS} and V_{SG} respectively, the next step in the design process was to obtain the plot of g_m/I_D vs. the normalized current $I_D/(W/L)$. Exporting the data of I_D and g_m/I_D from the two plots shown in Figures 22 and 24 to a numerical computation program such as MATLAB, one is able to normalize the current data and obtain the desired of g_m/I_D vs. $I_D/(W/L)$. This plot is shown in Figure 25 below.

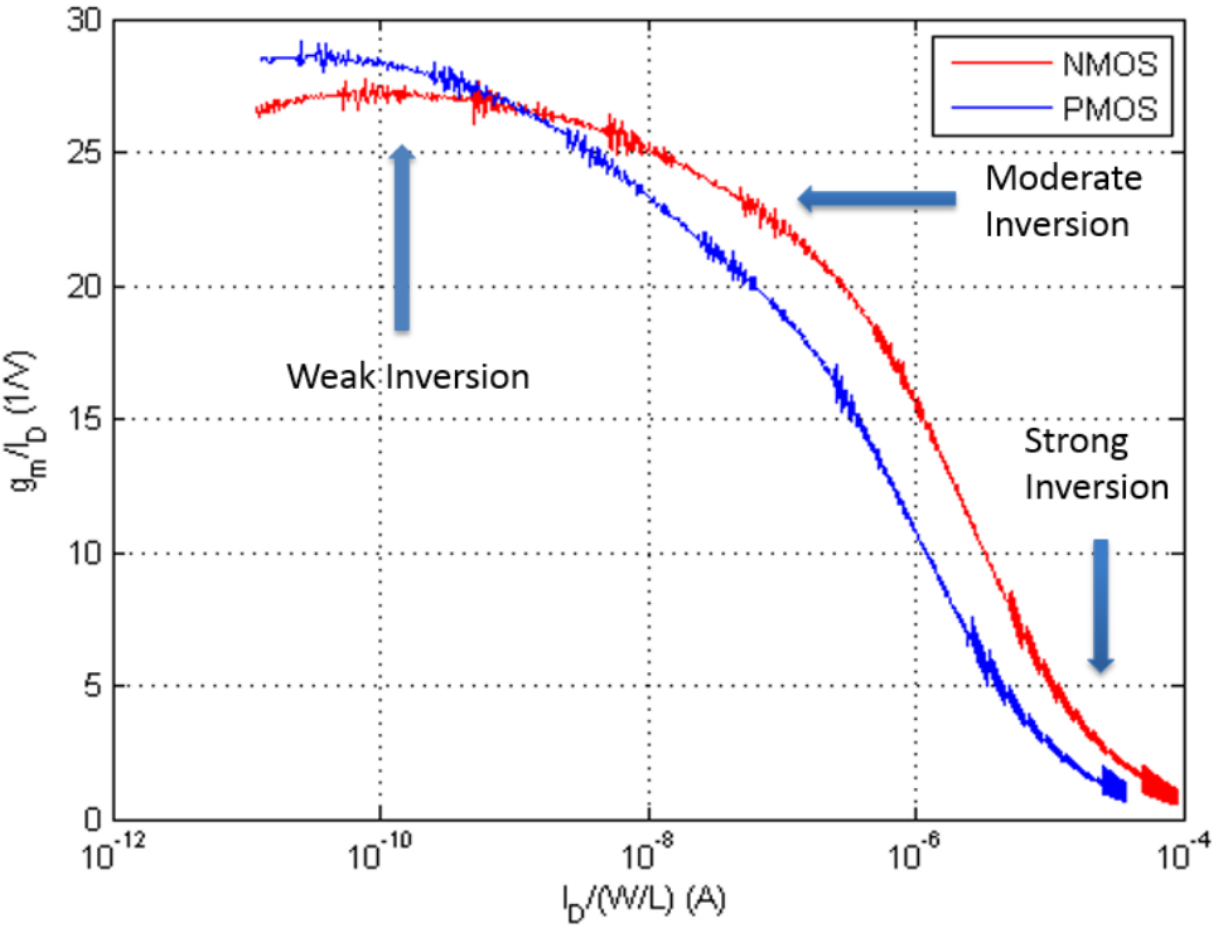


Figure 25. Transconductor efficiency (g_m/I_D) vs. normalized current ($I_D/(W/L)$ curves for NMOS and PMOS in the 300nm TSMC process using the TSMC 25 transistor model.

The significance of the plot shown in Figure 25 comes from the fact that it is also an indicator of the mode of operation of the transistor; one can observe that the derivative of g_m/I_D is maximum in the weak inversion region (subthreshold) where the I_D dependence versus V_G is

exponential while it is quadratic in strong inversion, becoming almost linear deeply in the strong inversion because of the saturation velocity [11].

From this plot determining the sizes of transistors becomes a straightforward exercise, for example, consider the case of an NMOS transistor desired to operate in weak inversion (subthreshold), where, from the plot g_m/I_D = 25 1/V; also let us say that in this hypothetical example, the current through this transistor is needs to be 100nA. Then, by looking at the plot in Figure 25, one can observe that the normalized current value corresponding to g_m/I_D = 25 1/V is $I_D/(W/L) \approx 10^{-8}$ or 10nA. Since the value of I_D needs to be 100nA one can see that

$$10\text{ nA} = \frac{100\text{ nA}}{W/L}$$

Arbitrarily choosing the length L of the transistor to be the minimum for the process L=300nm, for example, yields

$$W = \frac{100\text{ nA}}{10\text{ nA}}(300\ nm) = 300\ \mu m$$

As a conclusion to this chapter, let us state and review the step by step transistor sizing procedure for the g_m/I_D methodology:

1) Determine bias current for the circuit and based on it determine currents on all branches
2) Determine the region of operation desired for a given transistor according to circuit operation: subthreshold (weak inversion); linear (moderate inversion); saturation (strong inversion)
3) Using the obtained g_m/I_D vs. I_D/(W/L) plot, pick a value for g_m/I_D (Based on region of operation), read the corresponding normalized current I_D/(W/L), using this value and the drain current through the transistor, solve for W/L

CHAPTER IV

OPERATIONAL TRANSCONDUCTANCE AMPLIFLIER DESIGN

As we begin describing the components that make up the neural amplifier proposed in this project, this chapter focuses on the design of the operational transconductance amplifier used in the neural amplifier. It is important to remember that for the amplifier to function as an operational transconductance amplifier, its open-loop gain should be ideally infinite, however realistically it should be high enough so that its unity gain bandwidth is wide enough to encompass within it a pass band shaped response of ~40dB mid-band gain with bandwidth of 1-100 Hz as this will be the shape of the neural amplifier's closed-loop frequency response once the capacitive feedback is added.

Initially, a wide-range current mirror operational transconductance amplifier, such as the one presented in Chapter I (Figure 11), was chosen but this circuit was not able to meet the power consumption goals because, as explained in the Chapter II review, this topology is inherently not very power efficient as it wastes a lot of precious current in the two current mirrors that achieve its transconductance operation. Instead, the circuit topology for the operational transconductance amplifier was chosen to be similar to the one presented in [6] (described in Chapter II) because as stated in the review "*Recent advances in neural recording microsystems*" [19] presented in Chapter II, this topology is one of the more power efficient. Furthermore, this structure was modified to achieve a simpler OTA that would operate in a similar manner with a supplied bias current, as seen in Figure 26

Using the plot of g_m/I_D vs. $I_D/(W/L)$ obtained in Chapter III and a modified amplifier circuit topology similar to the one presented for the OTA in [6], the transistor sizes were determined based on the total bias current (chosen to be 56nA) and the individual currents through each transistor that was determined to be drawn from the 1.8V source to meet power consumption constraints. A simplified schematic of the amplifier is shown in Figure 26.

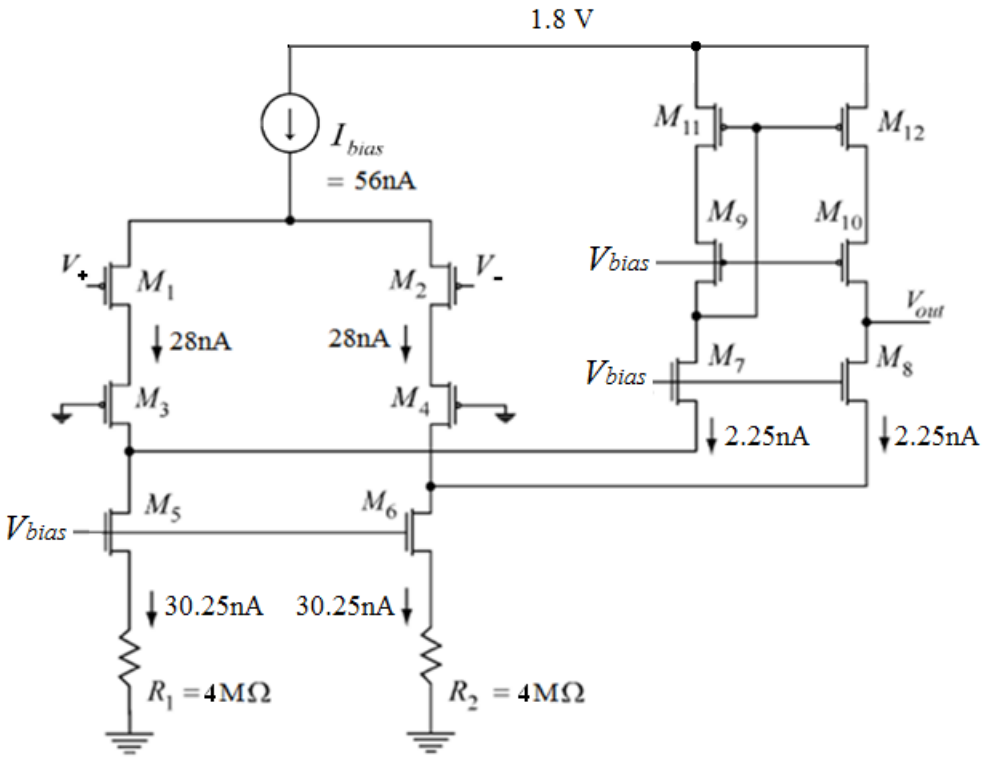


Figure 26. 108.9nW Folded Cascode Operational Transconductance Amplifier

The Bias Circuit for the OTA

The circuit in Figure 26 requires a bias circuit to provide the 56nA of current; to achieve this, a "*CMOS current reference without resistance*" was carefully chosen to be used; this circuit in shown in Figure 27 and was proposed by Oguey and Aebischer in [13]. The authors state that this bias circuit is ideal for sourcing currents from 1nA to 100nA and even though the bias circuit added to the amplifier makes it consume more than the 56nA of current, its power consumption

is not included in the power calculation of the entire system because one of this current sources can be shared by all the channels in a multi-channel neural amplifier system.

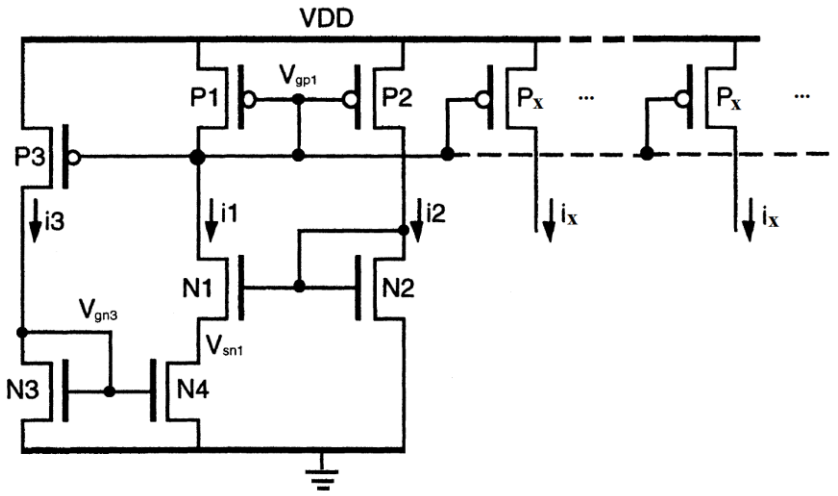


Figure 27. CMOS current reference proposed in [13]

The current is generated as soon as the power supply is turned on in the left part of the circuit in Figure 27 and then mirrored a couple of times. The current can be set by changing the sizes of transistors N1, N2, P1, and P2; and this current reference can be replicated and scaled as many times as needed with transistors, P_x, as shown in Figure 27. The sizes, determined through g_m/I_D methodology, for the OTA and for the current reference are shown in Table I below.

Table 1. OTA and Current Reference Transistor Sizes

Transistor sizes (μm)					
OTA	*W*	*L*	*Current Reference*	*W*	*L*
M_1, M_2	420.075	1.5	N1	75	2.25
M_3, M_4	140.025	1.5	N2	4.05	2.25
M_5, M_6	180.075	3	N3	2.25	241.875
M_7, M_8	3.525	1.5	N4	2.25	363.075
M_9, M_{10}	6	1.5	P1, P2, Px	2.25	112.5
M_{11}, M_{12}	20.025	20.025	P3	6.75	112.5

Figure 28 shows the completed Cadence schematic of the OTA, including the bias circuit. Notice that the resistors shown in the schematic in Figure 26 are broken into four 1MΩ in series.

This was done for physical layout design purposes, more specifically so that the Layout vs Schematic (LVS) check passed.

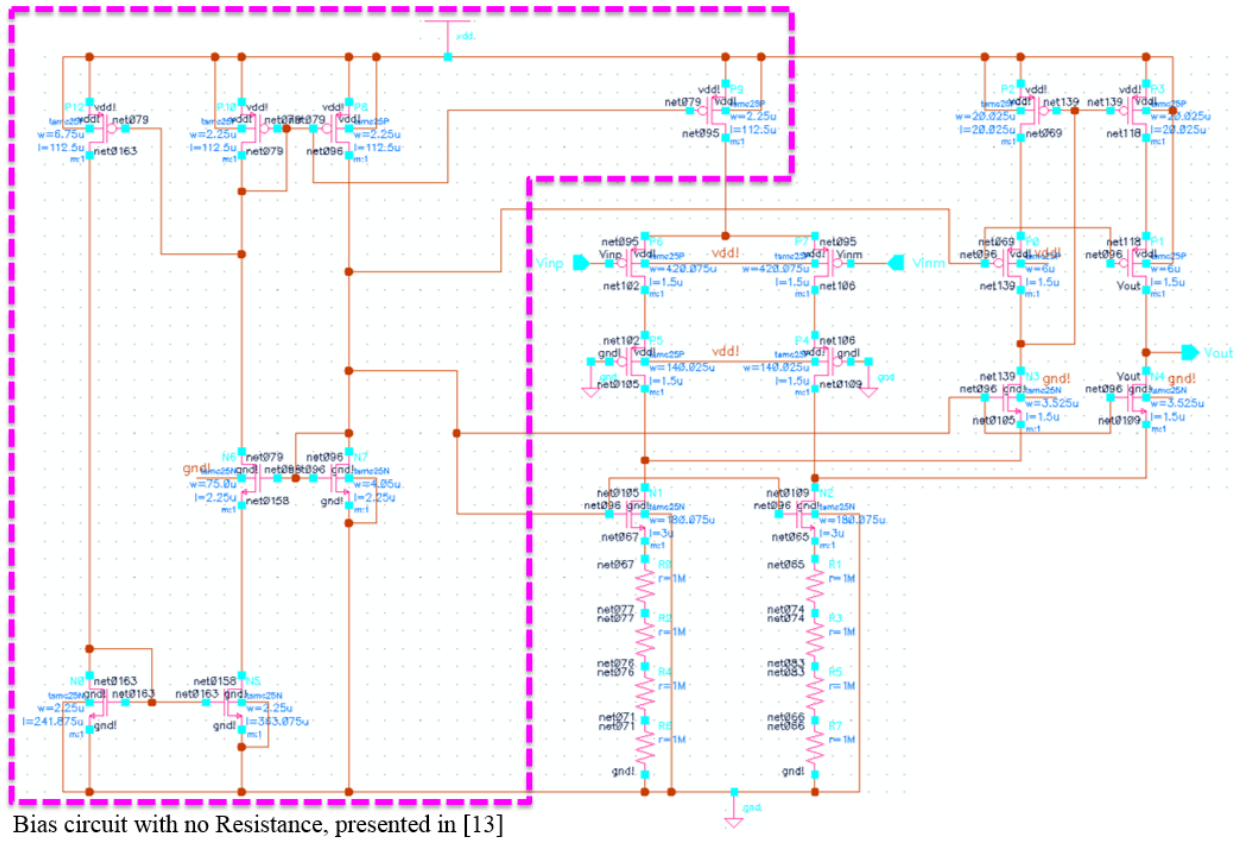


Figure 28. The OTA with its 56nA current reference circuit.

Design of the Amplifier's Physical Layout

The amplifier's physical layout was designed in the 300nm TSMC process as shown in Figure 29 below, it occupies an area of 474.75µm x 184.2µm. This layout also includes the bias circuit for the amplifier, which can be seen in the far left of Figure 29. It is important to note that in a multi-channel system where several amplifiers are needed, as is the common use for this type of circuits, only one bias circuit would be needed. This will be explained further in Chapter VI.

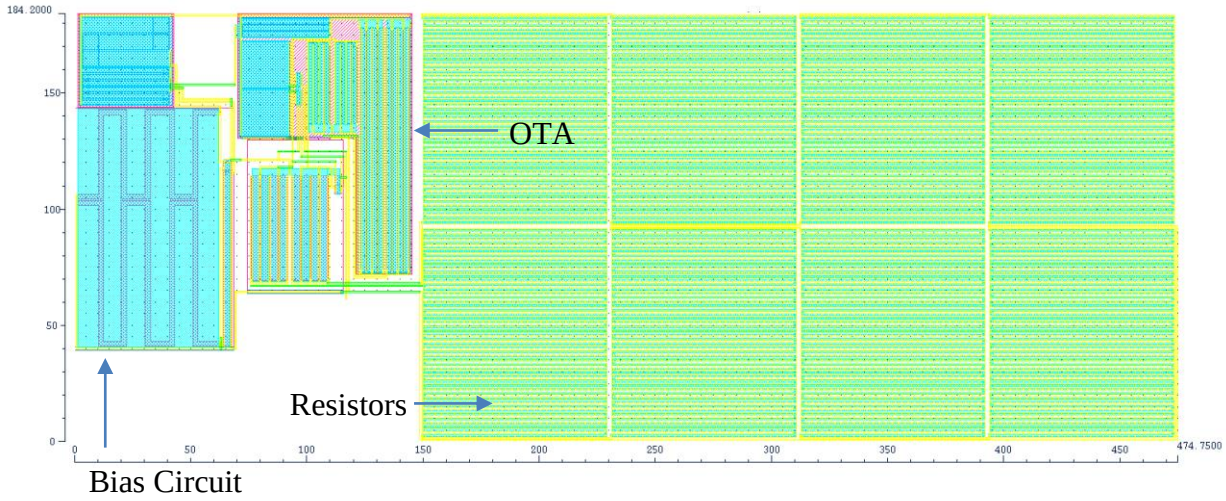


Figure 29. Amplifier Layout (including bias circuit) with an area of 474.75µm x 184.2µm

Circuits in this kind of applications and with this power consumption constraints consume currents that are several orders of magnitude smaller than other circuits. Having such small currents require bias resistors that are extremely large, which is impractical in an integrated circuit where area is a precious resource. Therefore, it is a much better approach to achieve the required small bias currents using only transistors, as these can be physically implemented very easily in the integrated circuit and also save a significant amount of chip area.

Resistors were made with polysilicon and silicide block due to the lack of a higher resistivity per square material in the TSMC 25 process. The 4Ω resistors shown in Figure 26 were broken up and a unit 1MΩ resistor layout was made, then four of these were placed in series to achieve the 4MΩ resistance shown in the schematic (Figure 28). The physical layout of the eight unit resistors that make up the two 4MΩ resistors that are part of the amplifier circuit can be seen in the far right of the amplifier layout (Figure 29).

The layout for a single channel amplifier without the bias circuit would only occupy an area of approximately 354µm x 184µm.

Simulation of the OTA

This section presents the simulated open-loop frequency response for both the schematic and layout of the operational transconductance amplifier designed in this chapter. Figure 30 shows the simulation results for the schematic (shown in Figure 28).

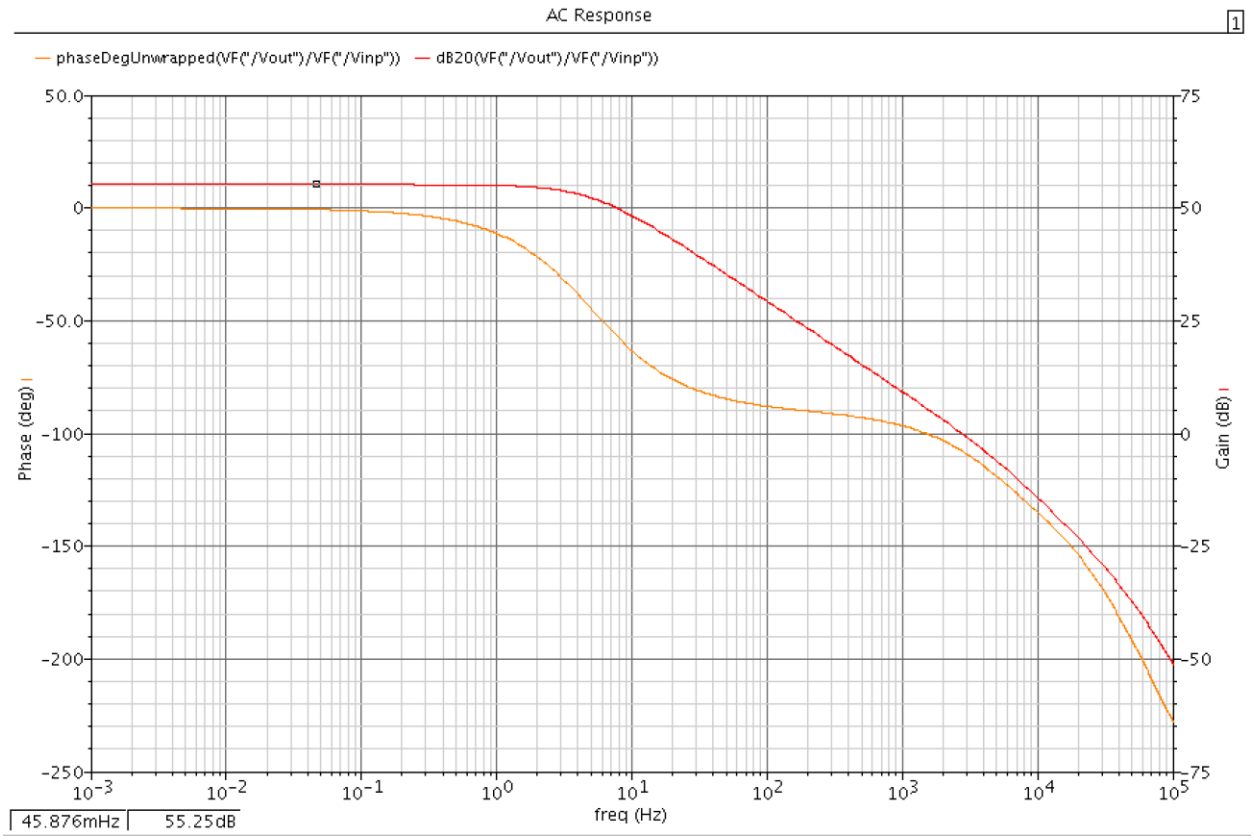


Figure 30. Open-loop frequency response of the OTA's schematic

After the physical layout was designed and it was confirmed that the Device Rule Check (DRC) passed, the extracted physical layout, including parasitic capacitances was generated. This cell is a more realistic representation of how the actual manufactured integrated circuit will behave. This extracted layout was cross-referenced and checked with the schematic circuit in a Layout vs. Schematic (LVS) check, and as can be confirmed in Appendix B, the netlists for both cells matched. Figure 31 shows the extracted layout's frequency response simulation.

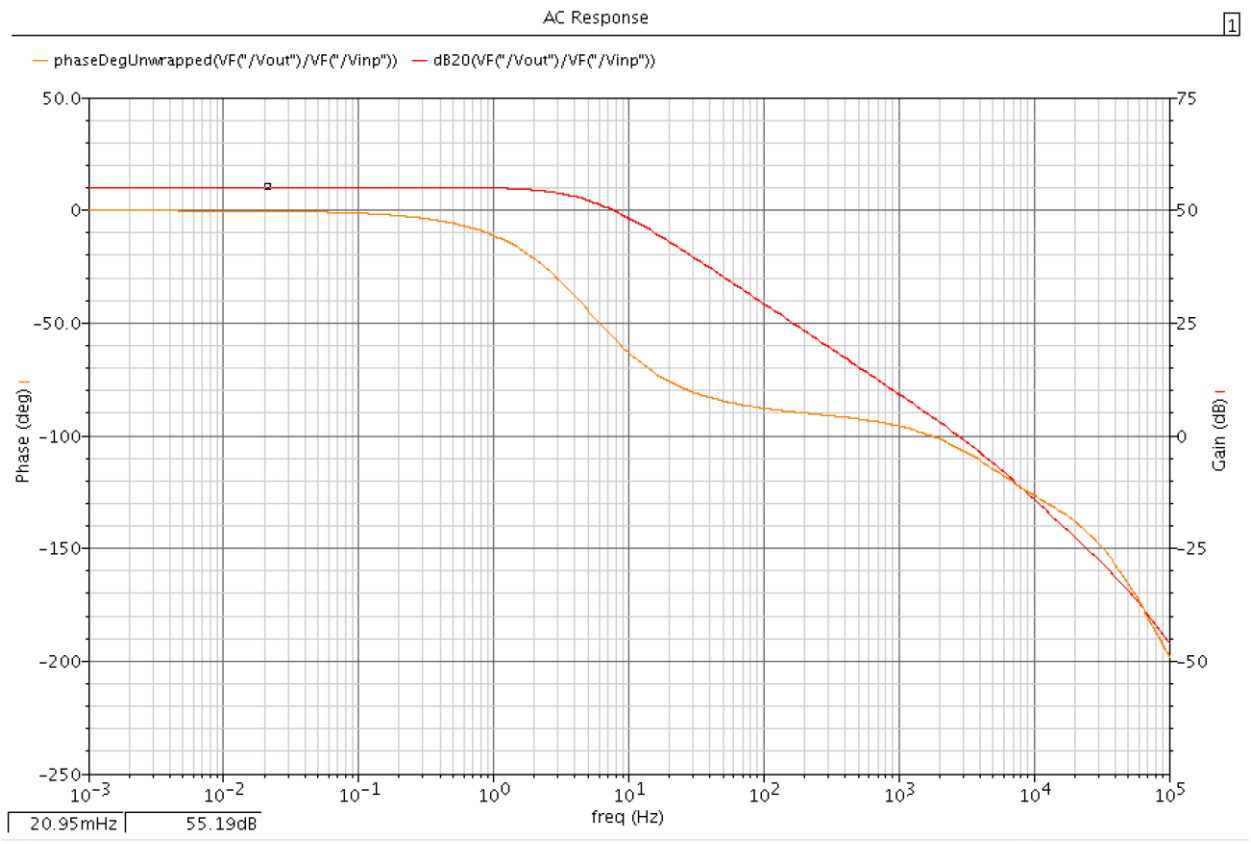


Figure 31. Open-loop frequency response of the OTA's extracted layout

One can observe in this figure that the OTA meets the requirements to be used as an operational transconductance amplifier by having a high open-loop gain (55.12dB = 575), an excellent phase margin (~80°) and a unity gain frequency of ~3 kHz, which is enough to encompass a closed-loop bandpass shaped response from 1 Hz to 100 Hz and a mid-band gain of ~40dB. The OTA was simulated with a load of 12pF.

CHAPTER V

G_m-C FILTER DESIGN

The next component that makes up the neural amplifier proposed in this thesis project is a filter that will follow up the front-end amplifier describe in Chapter IV. The design of a 3rd order Butterworth G_m-C low pass filter in presented in this chapter.

Remember that the neural amplifier is intended for recording of EEG, where the Local Field Potentials range from 1-100Hz. The Capacitive Feedback Network introduced by Harrison in [1, 2] shapes the frequency response as a pass-band, however the high frequency cutoff of this pass-band may not decrease fast enough to attenuate noise at higher frequencies. Therefore to be able to attenuate the neural spikes described in Chapter I (Figure 1) beginning at around 1 kHz, the circuit proposed in this chapter uses 14.7nS transconductors and a sharper roll-off after a cutoff frequency of 150Hz that attenuate undesired noise signals by a greater amount than with only the CFN described in Chapter II. The 3rd order filter is comprised, as can be observed, from equation (11) of a single order stage, of which the circuit is shown in Figure 32, followed by a second order stage, of which circuit is shown in Figure 33. The transfer functions of these two stages are then matched to their counterparts made from a 3rd order Butterworth polynomial. Remember that $\omega_c=2\pi f_c$, where f_c was chosen to be 150 Hz.

$$\frac{\omega_c}{(s+\omega_c)}\cdot\frac{G_0\omega_c^2}{(s^2+\omega_c s+\omega_c^2)}=\frac{300\pi}{(s+300\pi)}\cdot\frac{(300\pi)^2}{(s^2+300\pi\, s+(300\pi)^2)} \qquad (11)$$

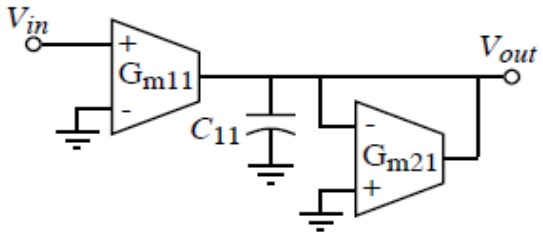


Figure 32. First order G_m-C Stage

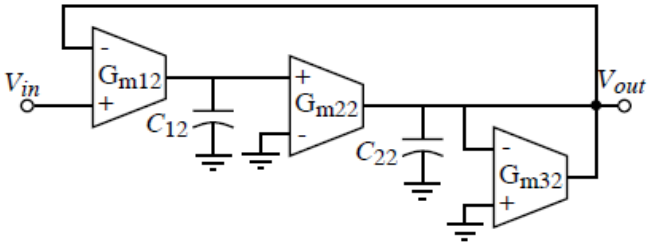


Figure 33. Second order G_m-C stage

One can derive the transfer functions for each of these stages following the same procedure described in the example in Chapter I, these transfer functions are shown in terms of their circuit components in the right hand side of equations (12) and (13). The transfer function of the first order stage and the design method to match it to the corresponding product in the Butterworth third order equation (11) is shown in equation (12)

$$\frac{\omega_c}{(s+\omega_c)} = \frac{300\pi}{(s+300\pi)} = \frac{\frac{G_{m11}}{C_{11}}}{\left(s+\frac{G_{m11}}{C_{11}}\right)} \tag{12}$$

The transfer function of the second order stage and the design method followed to match it to its corresponding product in the Butterworth third order equation (11) is shown in equation (13).

$$\frac{G_0\omega_c^2}{(s^2+\omega_c s+\omega_c^2)} = \frac{(300\pi)^2}{(s^2+300\pi\, s+(300\pi)^2)} = \frac{\frac{G_{m12}G_{m22}}{C_{12}C_{22}}}{\left(s^2+\frac{G_{m32}}{C_{22}}s+\frac{G_{m12}G_{m22}}{C_{12}C_{22}}\right)} \tag{13}$$

Notice from the circuits shown in Figures 32 and 33 that several transconductors make up filter's circuit. To be able to construct one single physical layout for a transconductor and use it for all the transconductors in the G_m-C filter, the value of G_m for all transconductors was chosen to be the same, 14.7nS. Then matching equations (12) and (13) with this know value for G_m, the values for the rest of the capacitors are easily obtained.

A simple current mirror transconductance amplifier like the one described in Chapter I was used to achieve the required transconductance. This cell, shown in Figure 34, was cascoded to increase its output resistance and therefore to increase the gain (refer to Chapter I), enabling the transconductors to be used as OTAs in the circuit. Figure 35 shows the Cadence schematic of the 14.7nS NMOS differential pair transconductor used in the G_m-C filter, along with the procedure to calculate the bias current needed. Table 2 shows the sizes of the transistors in the filter's OTA.

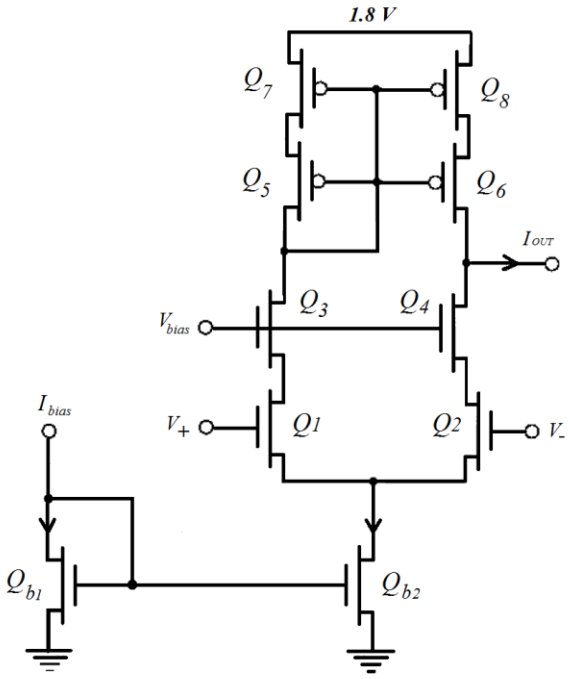
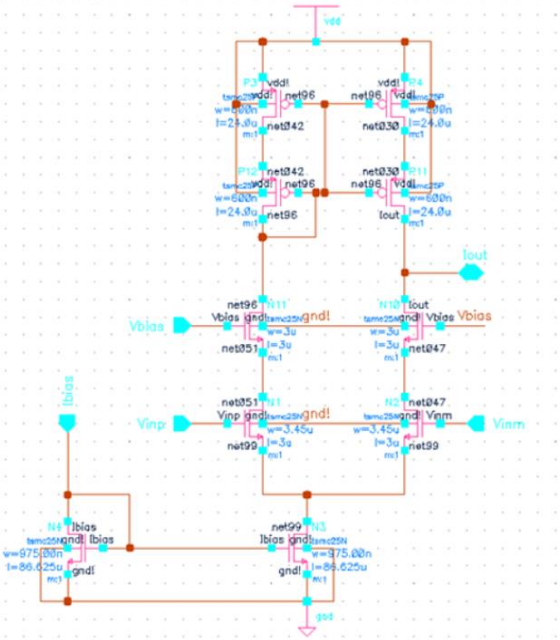


Figure 34.Telescopic cascoded amplifier used as the OTA for the G_m-C filter

Transistor sizes (µm)		
Filter OTA	*W*	*L*
Q_1, Q_2	3.45	3
Q_3, Q_4	3	3
Q_5, Q_6	0.6	24
Q_7, Q_8	0.6	24
Q_{b1}, Q_{b2}	0.975	86.625

Table 2. G_m-C filter OTA transistor sizes



Picked:

$G_m = 14.7nS$

$$g_m = \frac{I_{bias}}{nU_T}$$

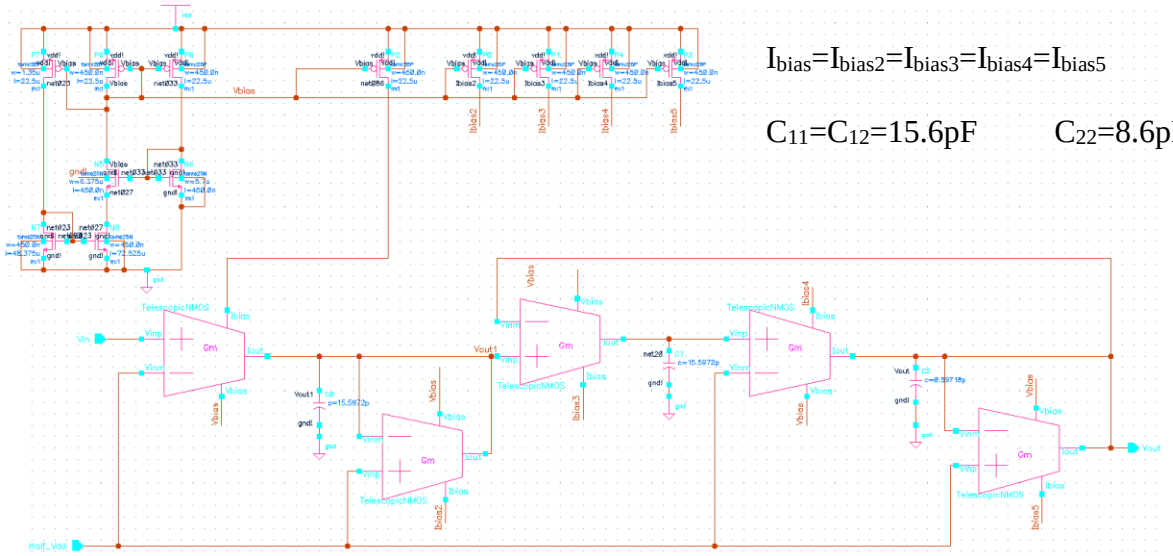
$n \approx 1.5$
$U_T \approx 25mV$ (at 300 K)

then bias current needed,

$I_{bias} = 1.154nA$

Figure 35. 14.7nS NMOS cascoded differential pair transconductor used in the G_m-C filter

The complete schematic of the 3rd order G_m-C low pass filter, including the bias circuit that provides the five identical bias currents for the transconductors, is shown in Figure 36 below. The bias circuit used to source the five transconductors is similar to the one used for the OTA in Chapter IV, except this time it was designed to output five 1.154nA currents instead of a single 56nA current.



$I_{bias}=I_{bias2}=I_{bias3}=I_{bias4}=I_{bias5}$

$C_{11}=C_{12}=15.6pF$ $C_{22}=8.6pF$

Figure 36. 3rd order G_m-C low pass filter schematic with its bias circuit

The G_m-C Filter consumes 17.637nA, corresponding to 31.75nW of power, including the bias circuit. However, remember that one bias circuit is enough for an entire multichannel system, so a more important figure is the power consumption per channel (without the bias circuit). That being the case, the G_m-C filter consumes 6.092nA, corresponding to 10.966nW of power per channel.

Design of the G_m-C Filter's Physical Layout

The designed layout for the filter in the 300nm TSMC process is shown in Figure 37 below, it occupies an area of 346.95µm x 184.95µm. Since only one bias circuit is needed to implement a multichannel system the total area occupied by the filters can be reduced in a multichannel system. The capacitors were built as MIM (Metal-Insulator-Metal) capacitors due to the lack of polysilicon layers in the TSMC process used. These type of capacitors have a lower capacitance per area (1fF/µm^2) than polysilicon ones which increases the area they use.

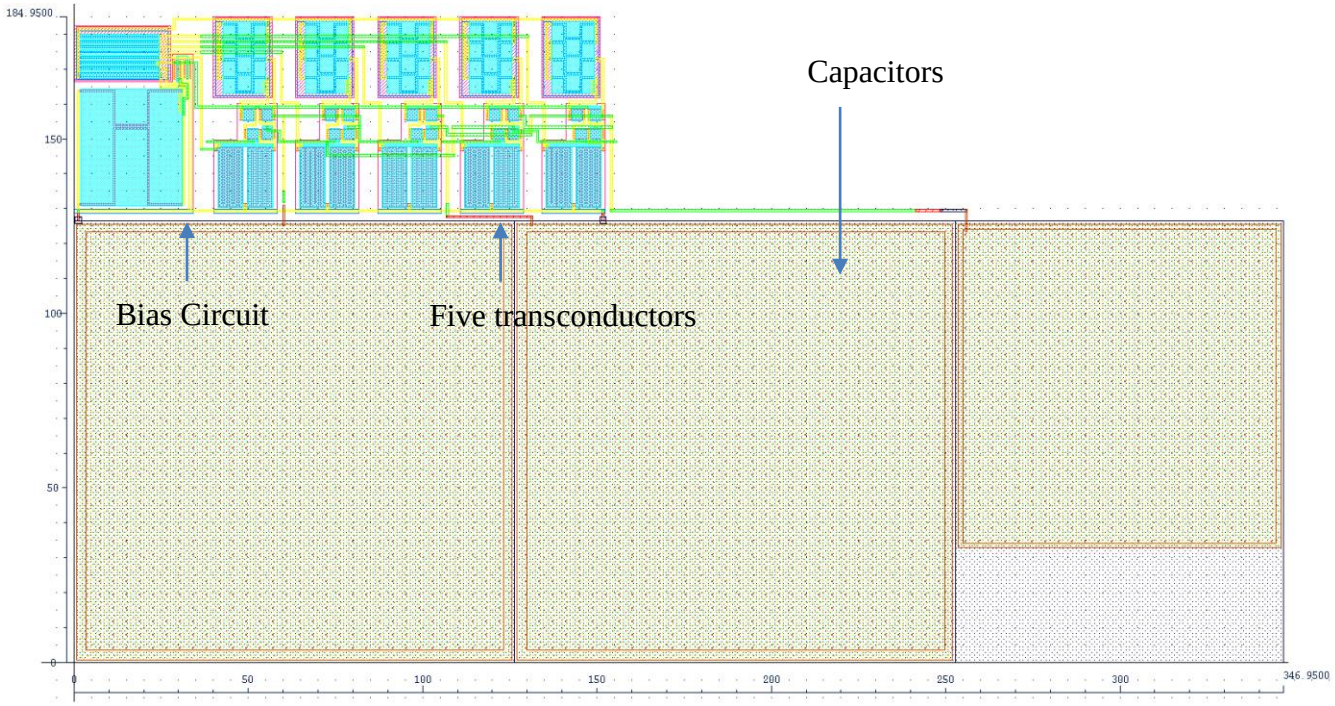


Figure 37. G_m-C Filter Layout in the 300nm TSMC process

Simulation of the G_m-C Filter

This section presents the simulated frequency response for both the schematic and layout of the 3rd order G_m-C low pass filter designed in this chapter. Figure 38 below shows the simulation results for the schematic (shown in Figure 36).

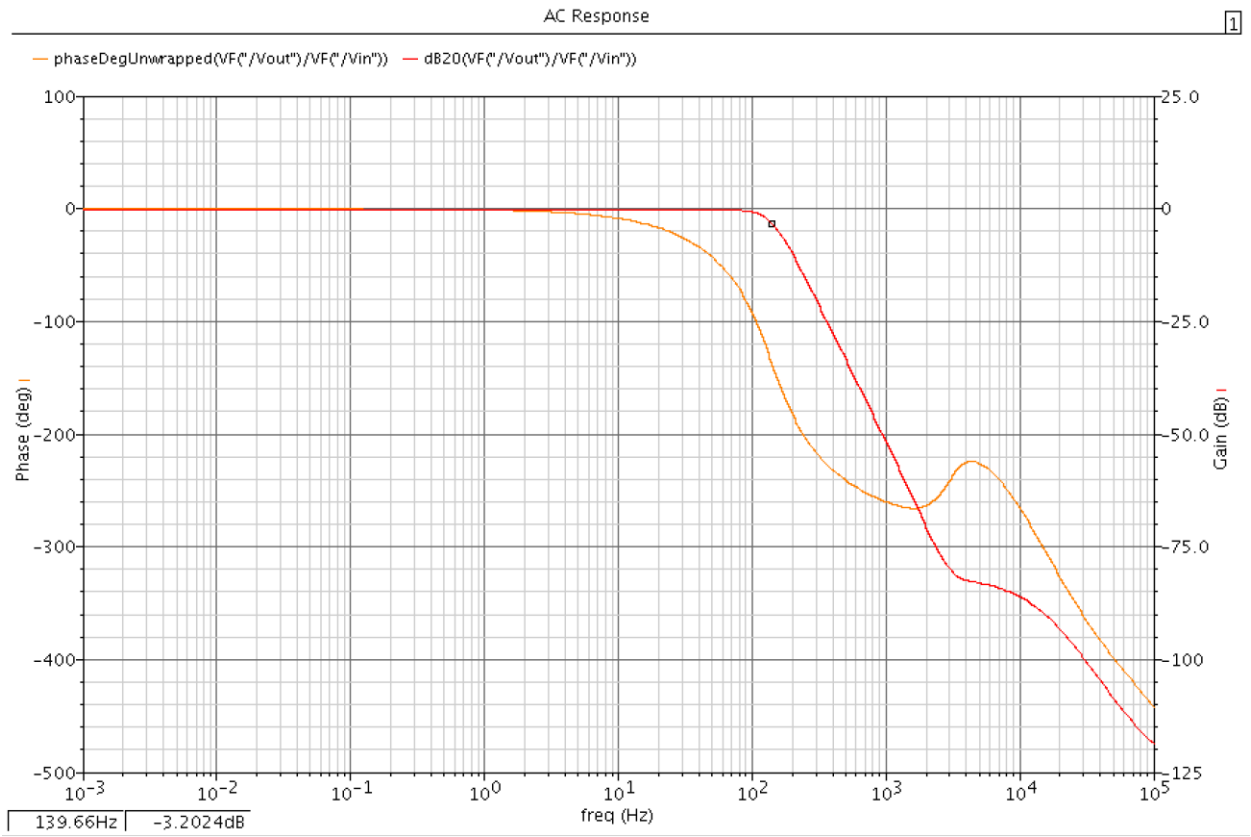


Figure 38. Frequency response of the G_m-C filter's schematic

After the physical layout was designed and it was confirmed that the Device Rule Check (DRC) passed, the extracted physical layout, including parasitic capacitances was generated. As explained in Chapter IV, this cell is a more realistic representation of how the actual manufactured integrated circuit will behave. This extracted layout was cross-referenced and checked with the schematic circuit in a Layout vs. Schematic (LVS) check, and as can be

confirmed in Appendix B, the netlists for both cells matched. Figure 39 below shows the extracted layout's frequency response simulation.

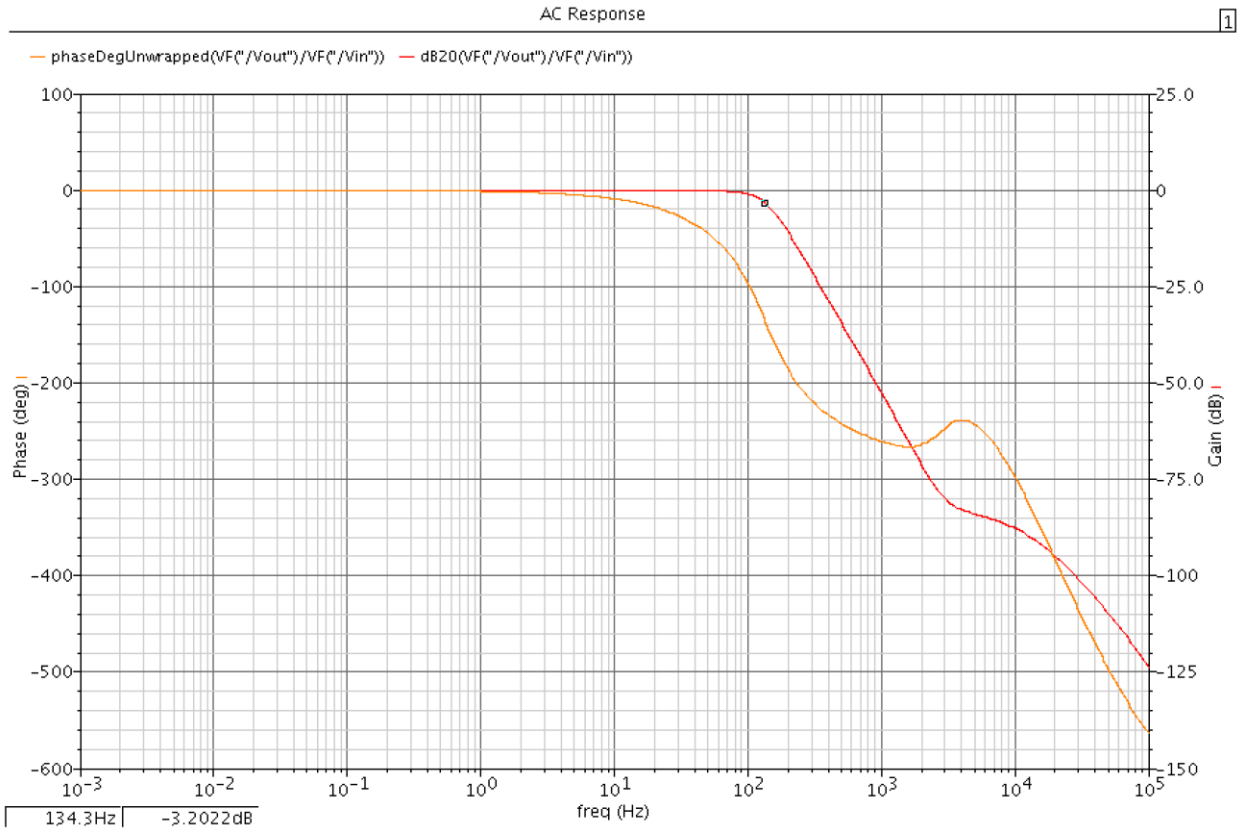


Figure 39. Frequency response of the G_m-C filter's extracted layout

As can be seen in Figure 39 the filter layout behaves as intended in the design, it has the sharper falling edge of a 3rd order filter and a cutoff frequency of ~140 Hz. Comparing figures 38 and 39, it can be observed that the extracted layout response closely matches the schematic response. Any discrepancies in the accuracy of the cutoff frequency are attributed to parasitic capacitances in the extracted layout, which affect the designed values of the capacitors, therefore affecting the cutoff frequency.

CHAPTER VI

THE NEURAL AMPLIFIER

Now that we have presented all the components of the neural amplifier, this chapter will focus on describing how these components are put together to realize the entire system. The full 3rd order filter, as well as the neural amplifier are shown in Figure 40. The Capacitive Feedback configuration for the gain stage was presented in [1] and explained in Chapter II; the mid-band gain A_M is set by C_{in}/C_f, and the bandwidth is $g_m/(A_M C_L)$, where g_m is the transconductance of the operational transconductance amplifier (OTA). The input capacitors C_{in} get rid of the DC offset generated at the electrode-tissue interface and the transistors in the feedback loop are used as pseudo-resistors to deliver a bias voltage to the input transistors of the amplifier, as well as set the low frequency cutoff of the amplifier's frequency response.

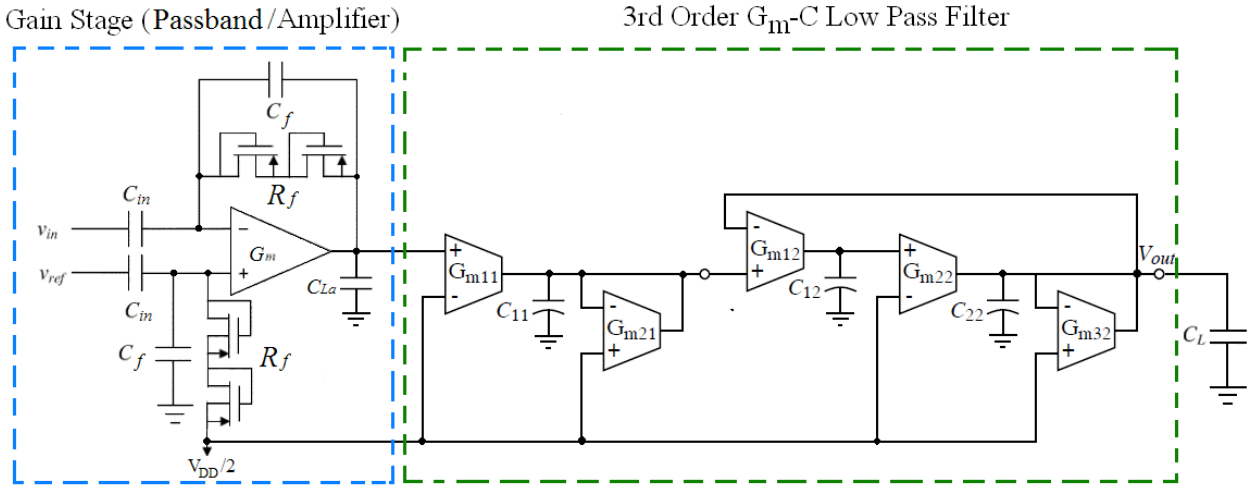


Figure 40. The proposed neural amplifier

Using nodal analysis and the procedure described in Chapter I, the transfer functions of the gain stage, as well as that of the entire system were derived. Equation 14 below shows the derived transfer function of the gain stage OTA with its Capacitive Feedback Network.

$$\frac{V_{out}}{V_{in}} = \frac{s^2 C_{in} C_f R_f + s\left(C_{in} - C_{in} G_m R_f\right)}{s^2\left(C_{La} C_f R_f + C_{La} C_{in} R_f + C_f C_{in} R_f\right) + s\left(C_{La} + C_{in} + C_f G_m R_f\right) + G_m} \tag{14}$$

The transfer function of the 3rd order G_m-C filter is given by the product equations 12 and 13 (Chapter V). Figure 41 below shows the theoretical bode plots obtained for each stage of the system (the OTA with CFN and the G_m-C filter), as well as the entire neural amplifier.

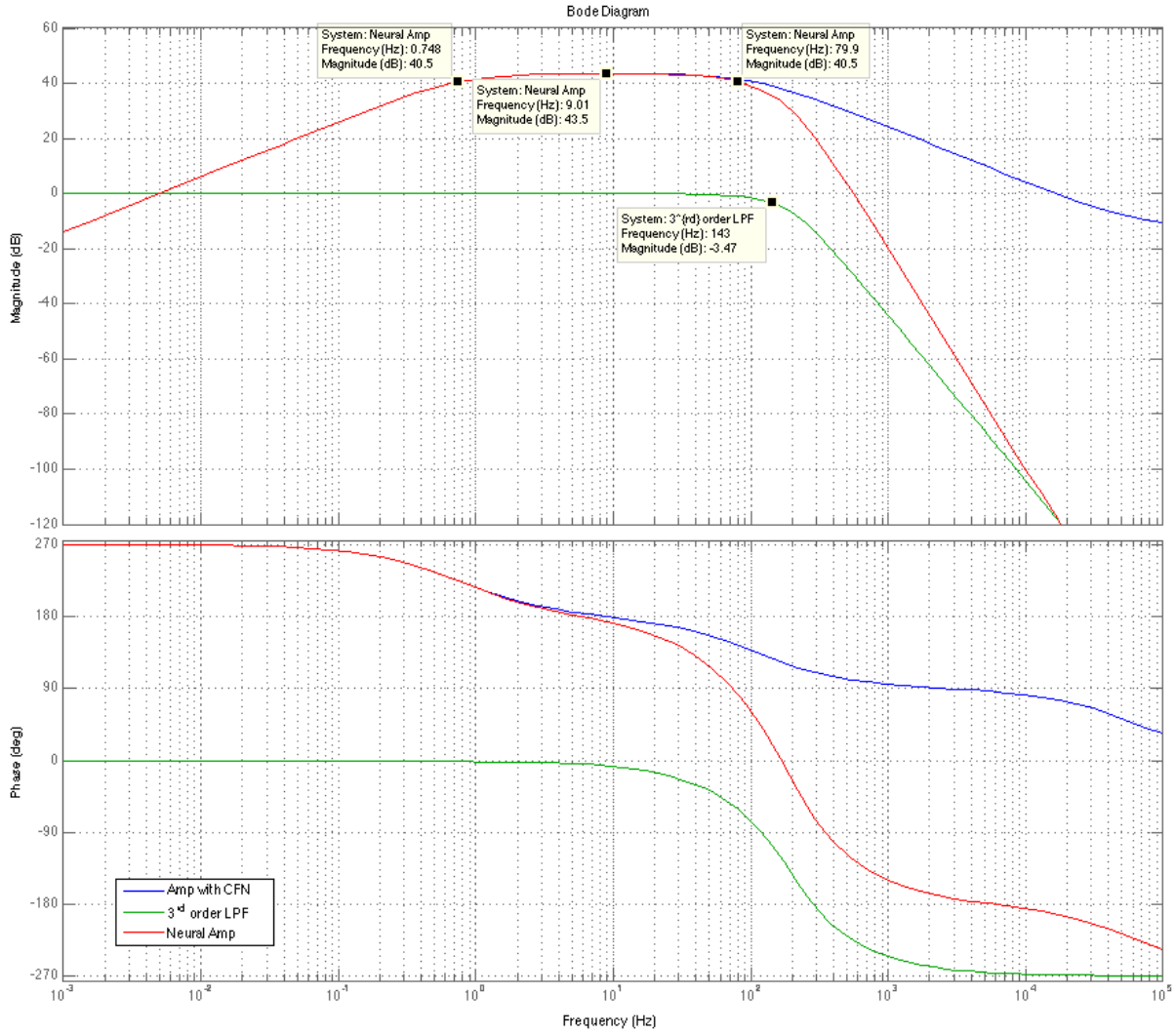


Figure 41. MATLAB Bode plots for all stages of the neural amplifier

To verify the theoretical response, the completed neural amplifier was simulated in Cadence; its schematic is shown in Figure 42 below.

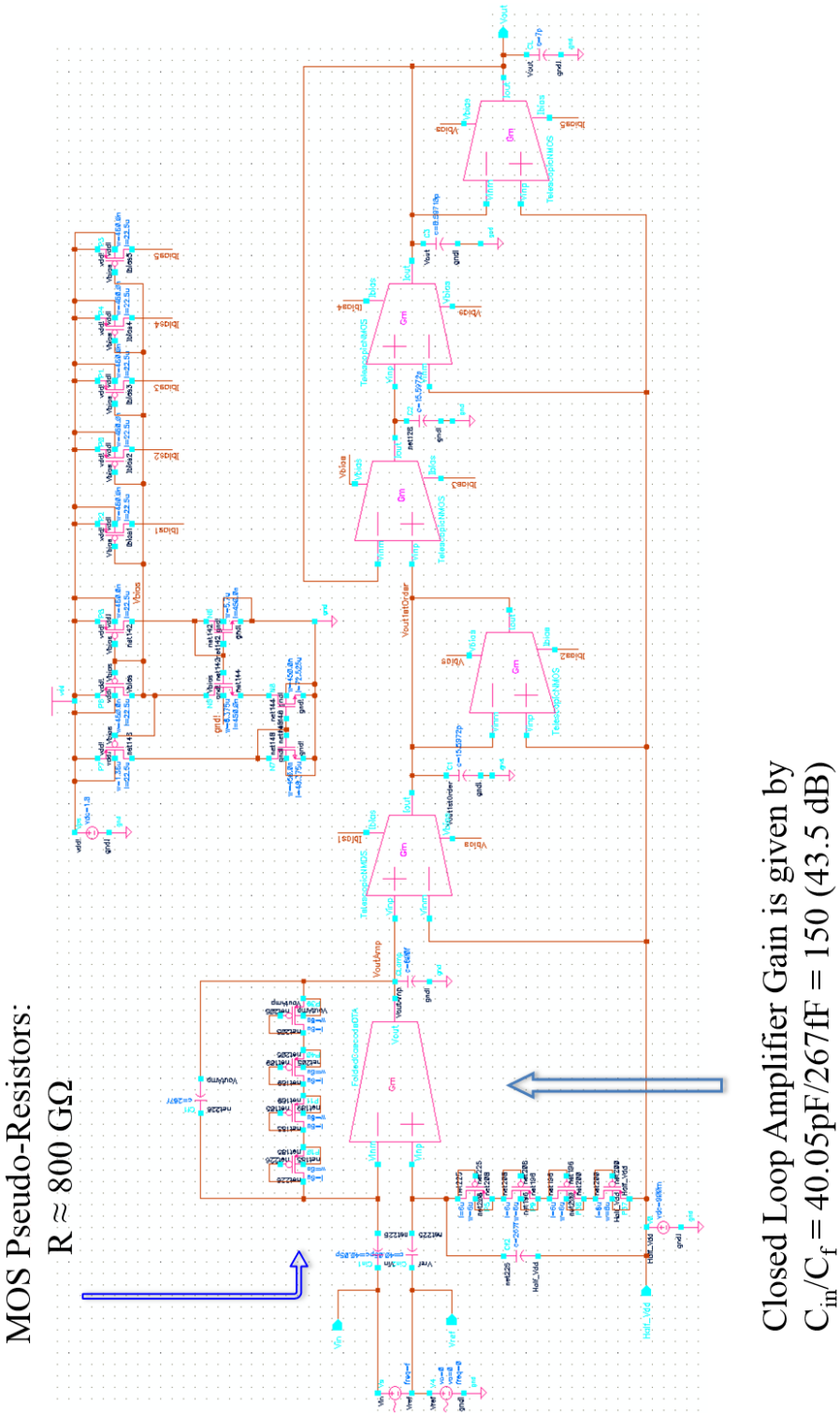


Figure 42. Complete schematic of the neural amplifier

The transistors in the feedback loop were measured to have a resistance of ~800GΩ to small changes in the voltage across them; their *W/L* ratio was set to 6µm/6µm. This high resistance is needed to achieve a low frequency cutoff in the milliHertz range. The closed-loop gain was set to be 150 (43.5dB) as shown in Figure 42.

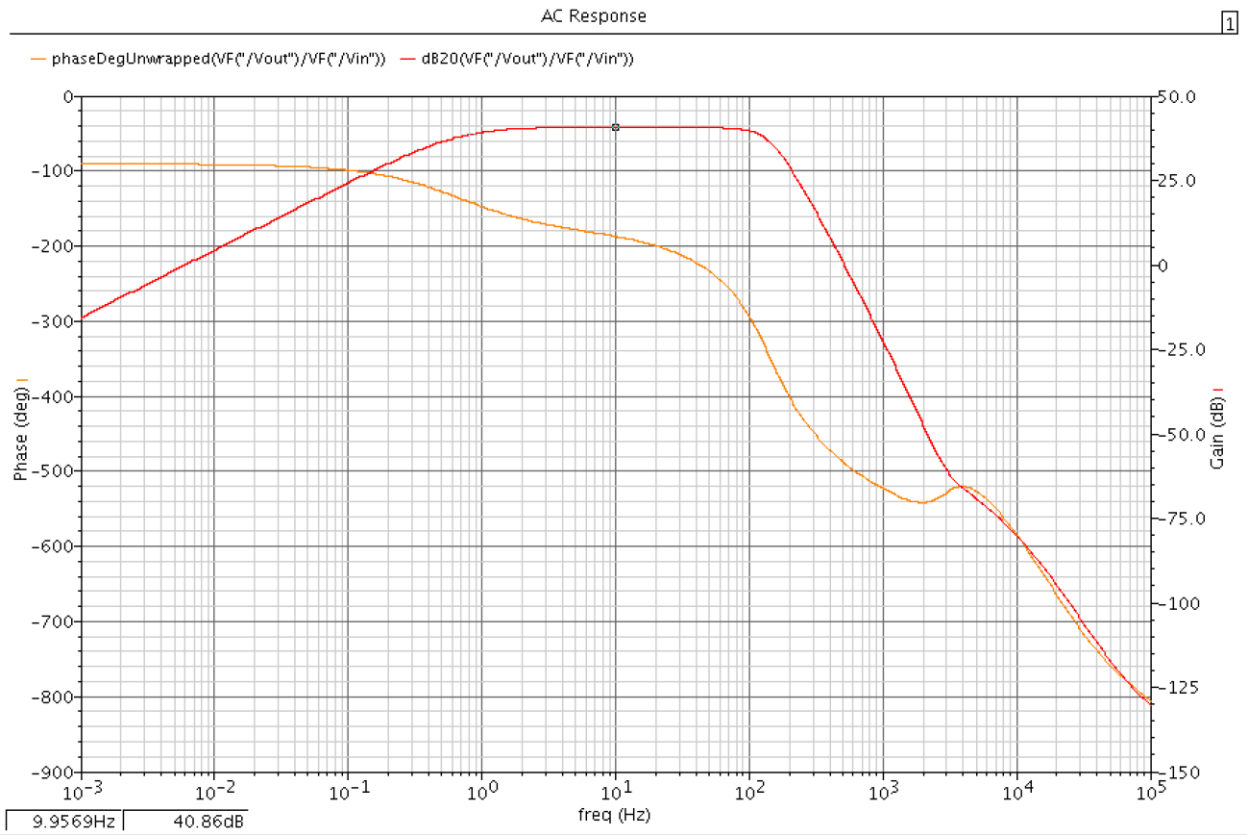


Figure 43. Frequency response of the Neural Amplifier's schematic.

The circuit's schematic frequency response (Figure 43) shows agreement with the theoretical plots in Figure 41.

Design of the Neural Amplifier's Physical Layout

Having the designed physical layout cells for the front-end OTA and the G_m-C filter (presented in Chapters IV and V), the physical layout of the entire system was realized paying close attention to floor-planning to be able to achieve a minimal size area in the chip. Then, after

it was confirmed that the Device Rule Check (DRC) for the entire integrated circuit passed, the extracted physical layout, including parasitic capacitances was generated. As explained in Chapter IV, this cell is a more realistic representation of how the actual manufactured integrated circuit will behave. This extracted layout was cross-referenced and checked with the schematic circuit in a Layout vs. Schematic (LVS) check, and as can be confirmed in Appendix B, the netlists for both cells matched. Figure 44 shows the designed layout of the neural amplifier system and Figure 45 shows the extracted layout's frequency response simulation.

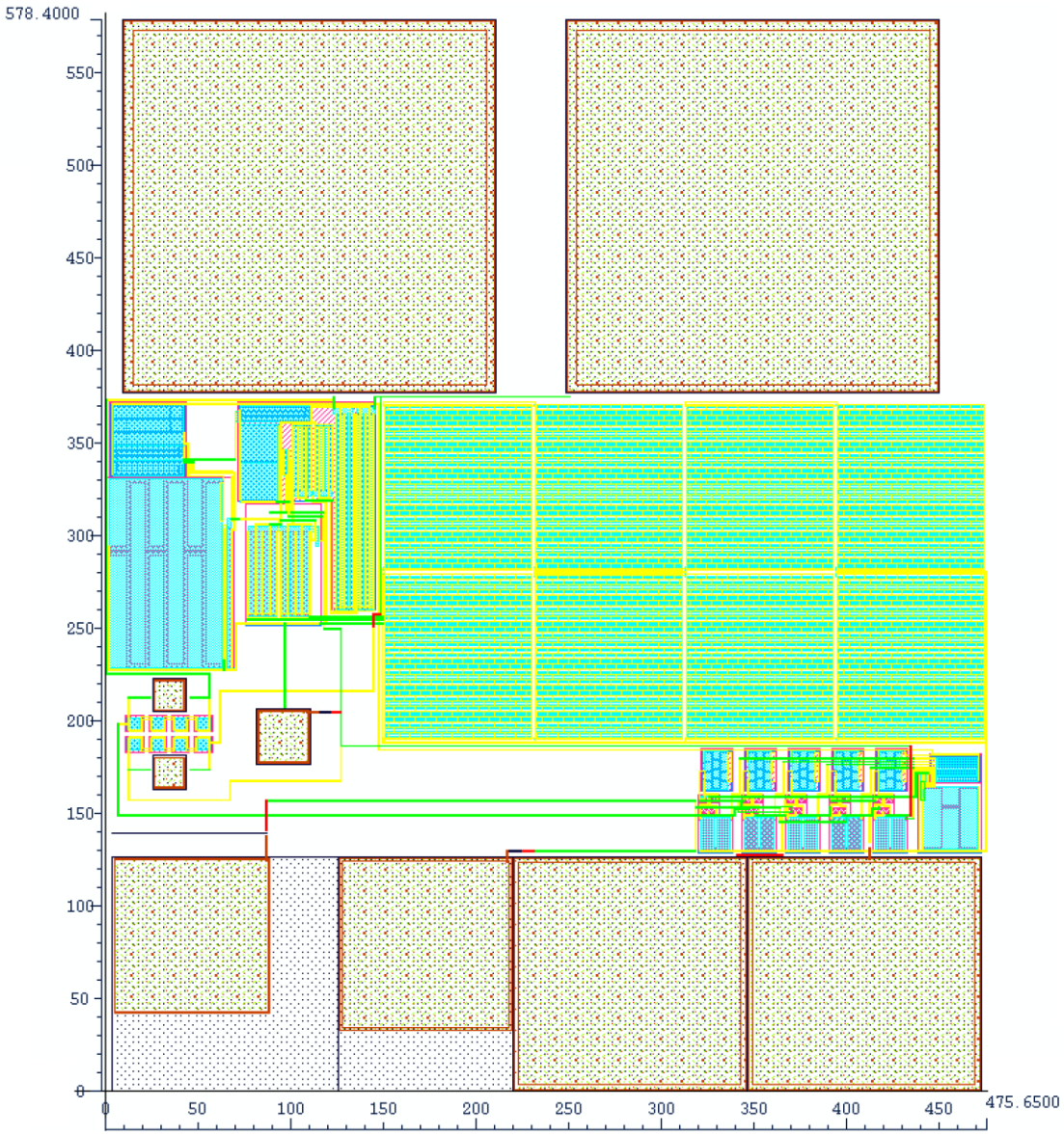


Figure 44. The Neural Amplifier's IC Layout. It occupies an area of 475.65µm x 578.4µm (0.275mm^2)

Simulation of the Neural Amplifier

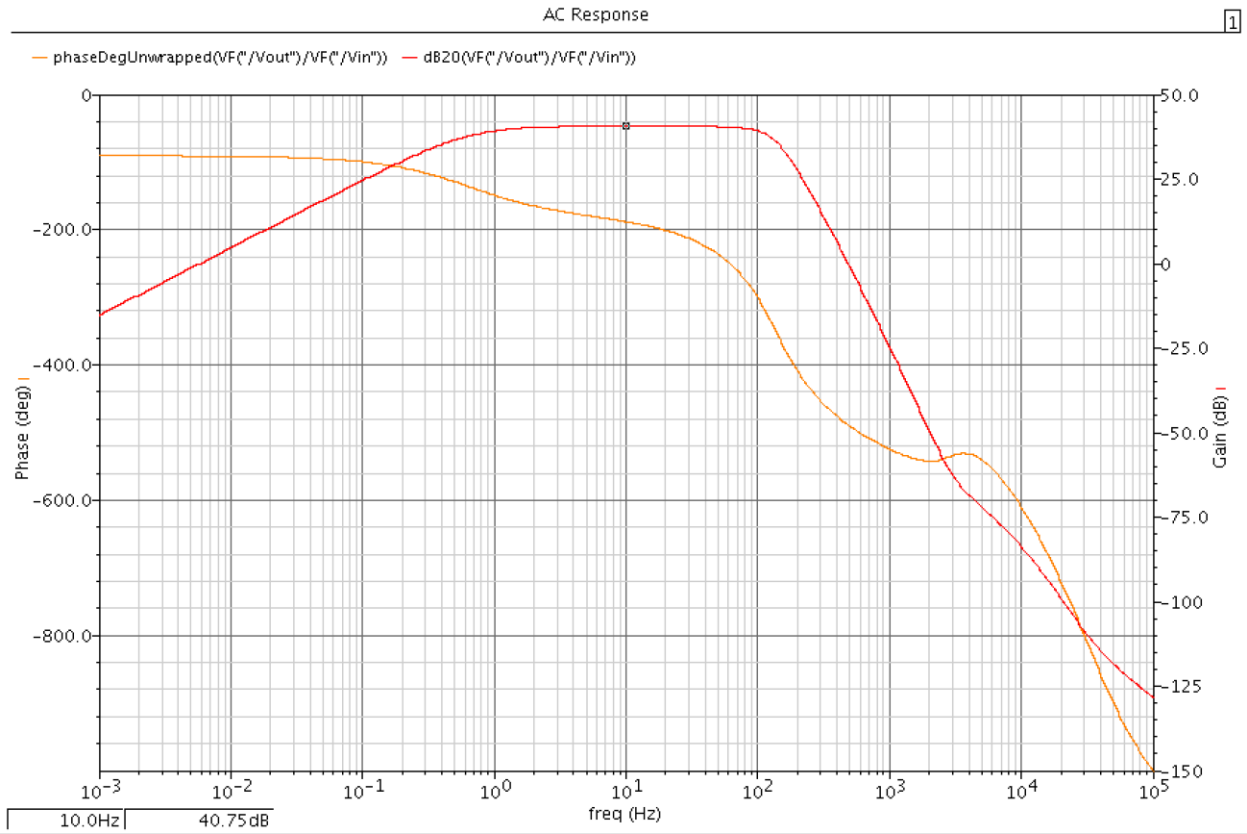


Figure 45. Frequency response of the Neural Amplifier's extracted layout.

As seen in Figure 45, the system's response is in agreement with the response obtained theoretically using the derived transfer functions, as well as those of the schematic, shown in Figures 41 and 43. Any minimal discrepancies are attributed to the parasitic capacitances of the extracted layout, which affect the values of the design's capacitors and therefore shift the cutoff frequencies of the two stages.

Figure 46, next, shows the squared output noise of the system from 0.1 Hz to 1 kHz. This noise curve was integrated over the range shown and referred back to the input by dividing it by the gain of the amplifier to calculate the system's input-referred noise, which corresponded to $3.77\mu V_{rms}$.

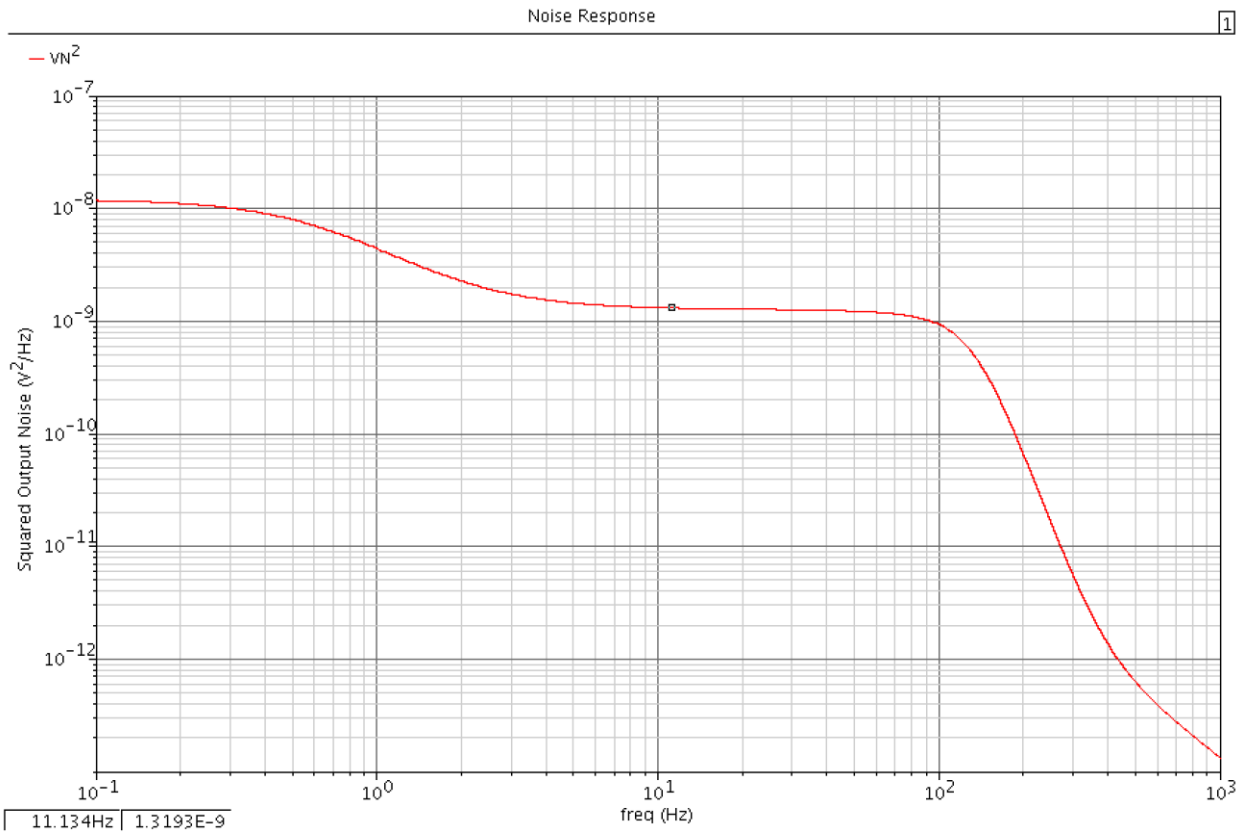


Figure 46. Squared output noise of the neural amplifier's extracted layout

Using the NEF equation described in Chapter II, the noise efficiency factor of the system was calculated to be 3.54, which is comparable with other published works as will be seen in Table 3.

Furthermore, a transient simulation was conducted on the neural amplifier to verify the response of the system to a small noisy input signal. The simulation was made with a $10\mu V_{pk}$, 30 Hz signal affected by $2\mu V_{pk}$ 1 kHz noise, such as the case will be in an EEG recording measurement affected by neural spikes. As can be observed in Figure 47, the output signal shows no common 1 kHz noise and its amplitude was measured to be ~$1.084mV_{pk}$ showing a gain of ~108.35 V/V (40.696 dB). This simulation is in agreement with the frequency response of the system shown in Figure 45.

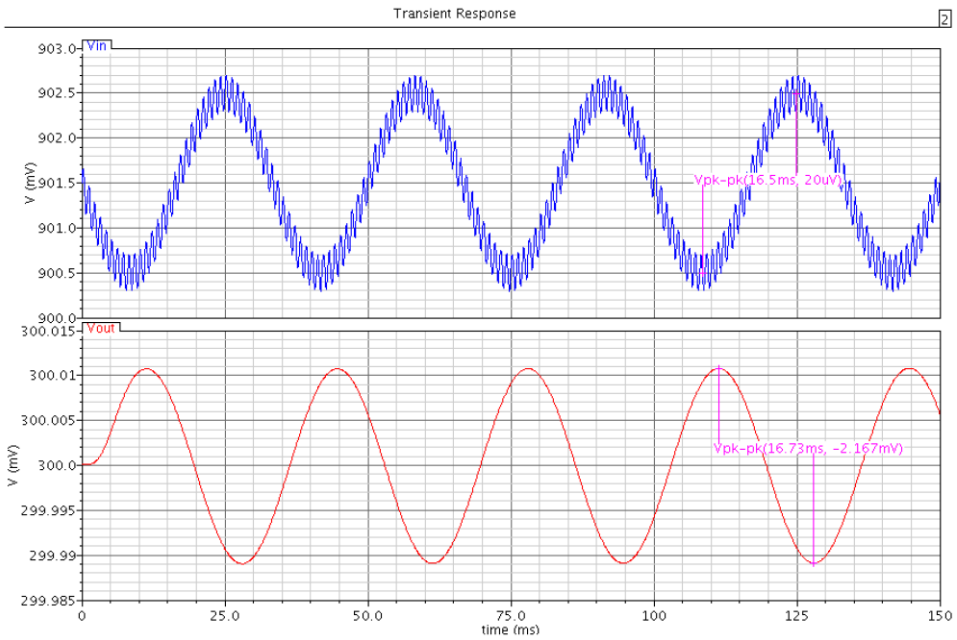


Figure 47. Transient simulation of the system to a noise affected input signal

Now let us present how this amplifier compares to other published works in literature. Figure 48 below shows a graph of *NEF* vs. I_{total} on which a few relevant reviewed published neural amplifiers in literature are placed along with this work. For low-noise and low power systems, one can see that the ideal case is to get as close as possible to the lower left corner, *i.e.* having a circuit with low noise that consumes minimal power as well.

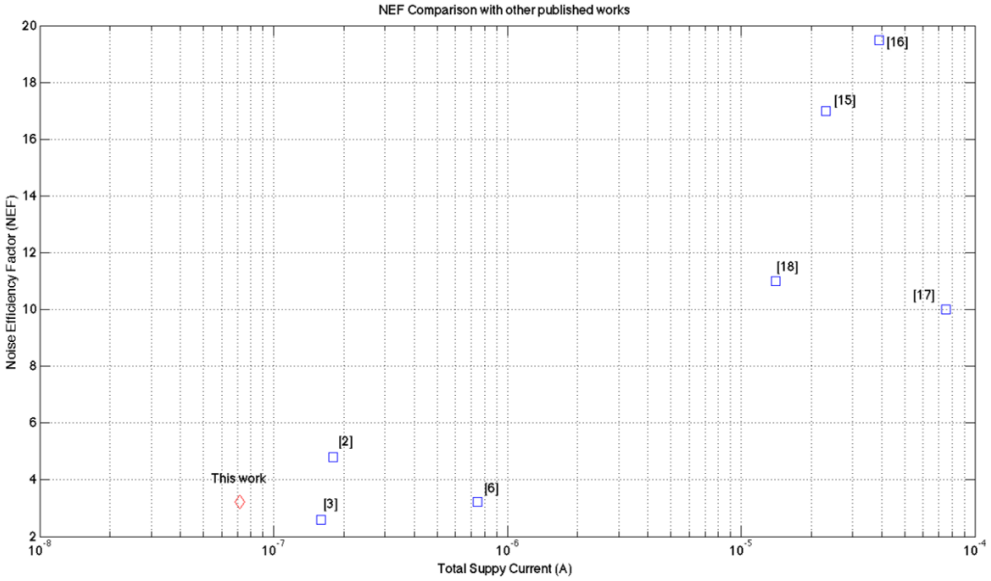


Figure 48. NEF vs. Total Supply Current comparison

Table 3. Neural Amplifier Simulation Results Comparison with Published Works

	This work 2012-2014		2007	2003	2012
Parameter	**Schematic**	**Extracted**	**[6] (Measured)**	**[2] (Measured)**	**[3] (Measured)**
Supply Voltage	1.8 V	1.8 V	2.8 V	± 2.5 V	1 V
Total Current	71.9nA	71.82nA	743nA	180nA	160nA
Power Consumption	129.42nW	129.276nW	2.08µW	900nW	160nW
Gain	40.86 dB	40.75 dB	40.9 dB	39.8 dB	40 dB
Bandwidth	633mHz – 129 Hz	620mHz - 121 Hz	392mHz - 295 Hz	14mHz - 30 Hz	200mHz - 430 Hz
Input-referred Noise	$3.83\mu V_{rms}$	$3.77\mu V_{rms}$	$1.66\mu V_{rms}$	$1.6\mu V_{rms}$	$5.71\mu V_{rms}$
Noise Efficiency Factor (NEF)	3.49	3.54	3.21	4.8	2.59
PSRR	57 dB	56 dB	75 dB	>80dB	>70 dB
CMRR	76 dB	72 dB	66 dB	>86 dB	>60 dB
Load Capacitance (C_L)	7pF	6.993pF	9pF	50pF	N/A
Area	-	$0.275mm^2$ (in 0.3µm TSMC)	$0.16\ mm^2$ (in 0.5µm CMOS)	$0.22\ mm^2$ (in 1.5µm CMOS)	$0.05\ mm^2$ (in 0.18µm CMOS)

As seen in Table 3, compared to other published works in literature, the proposed neural amplifier shows a significant improvement on power consumption with comparable noise performance, which as mentioned before benefits greatly the battery powered devices for which this type of system is used. The amplifier consumes 71.82nA from the 1.8 V power supply, which corresponds to 129.276nW of power consumed. The neural amplifier has a gain of 40.75dB in the EEG target pass-band.

As mentioned before, all the total currents in published works do not include the power consumption of bias circuits since one can be shared by a multichannel system. In Table 3, quantities are reported for a single channel only. With this in mind, the following section is aimed at calculating the power consumption of a multichannel system based on the proposed neural amplifier in this project.

Projected Multi-Channel Amplifier for EEG

As explained in Chapter I, current EEG systems utilize multi-channel electrode arrays placed at specific points in the human scalp. These multichannel electrode systems consist of 21 (minimum) to 64 channels and even up to 100+ channels. In this section, a projection of such a system is presented using the proposed neural amplifier described in this thesis project.

A 21 channel system (minimum) such as the 10/20 international standard for clinical EEG described in Chapter I would need:

-1 Amplifier Bias circuit (285.8nA)

-21 Amplifiers (21 x 60.355nA = 1.26746μA)

-1 Filter Bias Circuit (6.092nA)

-21 Filters (21 x 11.545.nA = 242.445nA)

From this calculation, it can be observed why the bias circuits are not included in the power consumption comparison in Table 3. One such system consisting of 21 channels would require only one bias circuit for all the amplifiers and one for all the filters. The 21 channel neural amplifier would consume a total current of 1.802μA, which corresponds to a total power consumption of 3.243μW. The bias circuits would only constitute 16% of the multichannel system and this number would only get lower as more channels are added, as is the case of better, more accurate multichannel systems. A projected estimate for a minimal 21 channel integrated circuit's physical dimensions, is that it would occupy a total chip area of approximately 5.775mm^2.

CHAPTER VII

CONCLUSION

A 129.276nW analog front-end amplifier and a 3rd order Butterworth Gm-C filter for Electroencephalogram (EEG) use has been proposed. Simulation of the extracted physical layouts with parasitic capacitances has been presented; the entire system has a gain of 40.75dB and rejects DC offset voltages present at the scalp at the input. The neural amplifier system has a bandwidth from 633mHz to 129 Hz, attenuating neural spikes present at 1 kHz by -25dB. Power consumption per channel has been reduced significantly while maintaining comparable noise performance with other neural amplifiers published in literature. The proposed system shows comparable input-referred noise, NEF, CMRR, and PSRR; and occupies an area of 0.275mm^2 in 0.3μm TSMC process.

Future Work

This section is aimed to interested readers wishing to follow up on this project, or confirm its operation experimentally, or simply improve it. Because this project only presents simulation results, future work includes sending the designed layout for IC fabrication and verifying its operation in the laboratory. To do this, one should acquire IC pads for the TSMC process being used and create the pad frame layout in Cadence, inside of which the entire system can fit in and where all pins can be connected to the pad frame. Then, it can be sent to MOSIS (www.mosis.com) for fabrication and the chip's performance can be verified experimentally in the laboratory.

One would require to take certain measures when testing the neural amplifier experimentally, such as, shielded electrodes which would need to be acquired; a live test subject would need to be selected, many of the published amplifiers reviewed and referenced in this manuscript test their systems with anesthetized animals such as rats or small birds; finally, a capable oscilloscope to observe and record any desired EEG signals, would also be needed.

Among the improvements that can be made to the amplifier, if lower power than what has been proposed in this project is desired, one can try redesigning the front end amplifier using the Telescopic topology, as this is the most power efficient of the topologies described in [19]. Different kinds of filter (band pass, tunable) can also be designed according to the site interference and specific signal needs of a completed multichannel IC to be used for neural recording. Regarding the physical design of the integrated circuit and taking into consideration that a multichannel system will need to be created for a fully useful EEG Neural Recording Amplifier, a much better layout of the system can be designed. This would help with noise, parasitic capacitances, leakage, and possibly reduce the chip area of a fully integrated multichannel system. Refer to "The Art of Analog Layout" by A. Hastings for a description and examples of the techniques used to make a better layout. After all this has been done, one can implement a multichannel (21, 64 or 100+) integrated circuit such as the ones described in Chapter I, send it for fabrication, and test its performance in the laboratory by measuring a complete Electroencephalogram of all the different areas of the brain for diagnostic.

Finally, to complete the system shown in Figure 15, an Analog to Digital Converter (ADC) can be designed, implemented and added to a fully implemented integrated circuit. Then a fully recording system can be set up and EEGs can be stored for further digital signal processing.

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APPENDIX A

APPENDIX A

TSMC 25 SPICE NMOS AND PMOS TRANSISTOR MODELS

```
.MODEL CMOSN NMOS (
LEVEL   = 7              TNOM    = 27             TOX     = 5.8E-9
XJ      = 1E-7           NCH     = 2.3549E17      VTH0    = 0.3551677
K1      = 0.4881677      K2      = -1.465714E-6   K3      = 1E-3
K3B     = 3.2222493      W0      = 1E-7           NLX     = 1.927361E-7
DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
DVT0    = 0.5751286      DVT1    = 0.5660833      DVT2    = -0.3026132
U0      = 305.8066794    UA      = -1.152667E-9   UB      = 2.42808E-18
UC      = 4.12734E-11    VSAT    = 1.287591E5     A0      = 1.7957675
AGS     = 0.359392       B0      = 1.272642E-10   B1      = 4.171173E-9
KETA    = -9.762332E-3   A1      = 4.569146E-4    A2      = 0.531924
RDSW    = 175            PRWG    = 0.15           PRWB    = -0.1243425
WR      = 1              WINT    = 0              LINT    = 2.8E-9
XL      = 0              XW      = -4E-8          DWG     = -1.5E-8
DWB     = 2.37129E-9     VOFF    = -0.1090174     NFACTOR = 1.5319983
CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
CDSCB   = 0              ETA0    = 6.182294E-3    ETAB    = 2.692579E-4
DSUB    = 0.0454551      PCLM    = 1.6205616      PDIBLC1 = 0.9594821
PDIBLC2 = 2.748496E-3    PDIBLCB = -0.0220856     DROUT   = 1
PSCBE1  = 6.837438E8     PSCBE2  = 2.319772E-4    PVAG    = 9.53415E-3
DELTA   = 0.01           RSH     = 3.8            MOBMOD  = 1
PRT     = 0              UTE     = -1.5           KT1     = -0.11
KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
WL      = 0              WLN     = 1              WW      = 0
WWN     = 1              WWL     = 0              LL      = 0
LLN     = 1              LW      = 0              LWN     = 1
LWL     = 0              CAPMOD  = 2              XPART   = 0.5
CGDO    = 4.57E-10       CGSO    = 4.57E-10       CGBO    = 1E-12
CJ      = 1.556442E-3    PB      = 0.99           MJ      = 0.4227041
CJSW    = 4.217952E-10   PBSW    = 0.9814315      MJSW    = 0.1974203
CJSWG   = 3.29E-10       PBSWG   = 0.8515942      MJSWG   = 0.2684911
CF      = 0              PVTH0   = -6.690647E-3   PRDSW   = -8.4
PK2     = 1.959318E-3    WKETA   = 3.50257E-3     LKETA   = 8.792764E-4     )
*
```

```
.MODEL CMOSP PMOS (
LEVEL   = 7              TNOM    = 27             TOX     = 5.8E-9
XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.5478816
K1      = 0.6458081      K2      = -1.621568E-3   K3      = 0.0963219
K3B     = 5.9878549      W0      = 1E-6           NLX     = 1.468974E-8
DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
DVT0    = 2.726151       DVT1    = 0.7470899      DVT2    = -0.1147141
U0      = 100            UA      = 8.754904E-10   UB      = 1E-21
UC      = -1E-10         VSAT    = 1.292519E5     A0      = 0.9039776
AGS     = 0.0844426      B0      = 1.473225E-6    B1      = 5E-6
ETA    = 7.2918E-3      A1      = 0.03521        A2      = 0.3
RDSW    = 839.1660575    PRWG    = 0.2331634      PRWB    = -0.0514751
WR      = 1              WINT    = 0              LINT    = 3.349079E-8
XL      = 0              XW      = -4E-8          DWG     = -4.722775E-8
DWB     = -1.6212E-8     VOFF    = -0.1292636     NFACTOR = 0.9361946
CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
CDSCB   = 0              ETA0    = 0.243084       ETAB    = -0.0204632
DSUB    = 0.9978554      PCLM    = 1.3975173      PDIBLC1 = 4.013259E-3
PDIBLC2 = 5.534487E-6    PDIBLCB = -1E-3          DROUT   = 0.0591126
PSCBE1  = 5.132455E9     PSCBE2  = 1.189024E-9    PVAG    = 0
DELTA   = 0.01           RSH     = 2.9            MOBMOD  = 1
PRT     = 0              UTE     = -1.5           KT1     = -0.11
KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
WL      = 0              WLN     = 1              WW      = 0
WWN     = 1              WWL     = 0              LL      = 0
LLN     = 1              LW      = 0              LWN     = 1
LWL     = 0              CAPMOD  = 2              XPART   = 0.5
CGDO    = 5.59E-10       CGSO    = 5.59E-10       CGBO    = 1E-12
CJ      = 1.87036E-3     PB      = 0.9616687      MJ      = 0.4756791
CJSW    = 3.115985E-10   PBSW    = 0.8            MJSW    = 0.2684522
CJSWG   = 2.5E-10        PBSWG   = 0.8            MJSWG   = 0.2786992
CF      = 0              PVTH0   = 6.913576E-3    PRDSW   = 10.4939271
PK2     = 1.392595E-3    WKETA   = 1.2571E-3      LKETA   = -3.261413E-3    )
*
```

APPENDIX B

APPENDIX B

NEURAL AMPLIFIER LVS LOG FILE

```
@(#)$CDS: LVS.exe version 5.1.0 06/20/2007 02:10 (cicln03) $

Command line: /programs/cadence/IC5141/tools.lnx86/dfII/bin/32bit/LVS.exe -
dir /home/sagallegos/cadence/LVS_FinalAmp_and_Filter -l -s -t
/home/sagallegos/cadence/LVS_FinalAmp_and_Filter/layout
/home/sagallegos/cadence/LVS_FinalAmp_and_Filter/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for
/home/sagallegos/cadence/LVS_FinalAmp_and_Filter/layout/netlist
       count
      76          nets
      6           terminals
      8           res
      9           cap
      60          pmos
      48          nmos

    Net-list summary for
/home/sagallegos/cadence/LVS_FinalAmp_and_Filter/schematic/netlist
       count
      76          nets
      6           terminals
      8           res
      9           cap
      48          pmos
      42          nmos

    Terminal correspondence points
    N2        N4        Half_Vdd
    N45       N15       Vin
    N33       N24       Vout
    N71       N19       Vref
    N12       N1        gnd!
    N0        N0        vdd!

Devices in the netlist but not in the rules:    pcapacitor res
Devices in the rules but not in the netlist:    nfet pfet nmos4 pmos4

1 net-list ambiguity was resolved by random selection.
```

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	125	107
total	125	107
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	76	76
total	76	76
	terminals	
un-matched	0	0
matched but different type	0	0
total	6	6

Probe files from /home/sagallegos/cadence/LVS_FinalAmp_and_Filter/schematic

devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

Probe files from /home/sagallegos/cadence/LVS_FinalAmp_and_Filter/layout

devbad.out:
netbad.out:
mergenet.out:
termbad.out:
prunenet.out:
prunedev.out:
audit.out:

APPENDIX C

APPENDIX C

NEURAL AMPLIFIER SIMULATION INPUT FILES

Schematic Input File

```
// Generated for: spectre
// Generated on: Dec 1 20:27:25 2014
// Design library name: ThesisNeuralAmpFinal
// Design cell name: FinalAmp_and_Filter
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
parameters f=30
include "/programs/cadence/ncsu-cdk-1.5.1/models/spectre/standalone/tsmc25N.m"
include "/programs/cadence/ncsu-cdk-1.5.1/models/spectre/standalone/tsmc25P.m"

// Library name: tsmc25Test
// Cell name: Transconductor
// View name: schematic
subckt Transconductor Ibias Iout Vinm Vinp Vbias
    P12 (net96 net96 net042 vdd!) tsmc25P w=600n l=24.0u as=4.5e-13 \
        ad=4.5e-13 ps=2.7u pd=2.7u m=1 region=sat
    P11 (Iout net96 net030 vdd!) tsmc25P w=600n l=24.0u as=4.5e-13 \
        ad=4.5e-13 ps=2.7u pd=2.7u m=1 region=sat
    P4 (net030 net96 vdd! vdd!) tsmc25P w=600n l=24.0u as=4.5e-13 \
        ad=4.5e-13 ps=2.7u pd=2.7u m=1 region=sat
    P3 (net042 net96 vdd! vdd!) tsmc25P w=600n l=24.0u as=4.5e-13 \
        ad=4.5e-13 ps=2.7u pd=2.7u m=1 region=sat
    N10 (Iout Vbias net047 0) tsmc25N w=3u l=3u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=1 region=sat
    N11 (net96 Vbias net051 0) tsmc25N w=3u l=3u as=2.25e-12 ad=2.25e-12 \
        ps=7.5u pd=7.5u m=1 region=sat
    N2 (net047 Vinm net99 0) tsmc25N w=3.45u l=3u as=2.5875e-12 \
        ad=2.5875e-12 ps=8.4u pd=8.4u m=1 region=sat
    N1 (net051 Vinp net99 0) tsmc25N w=3.45u l=3u as=2.5875e-12 \
        ad=2.5875e-12 ps=8.4u pd=8.4u m=1 region=sat
    N4 (Ibias Ibias 0 0) tsmc25N w=975.00n l=86.625u as=7.3125e-13 \
        ad=7.3125e-13 ps=3.45u pd=3.45u m=1 region=sat
    N3 (net99 Ibias 0 0) tsmc25N w=975.00n l=86.625u as=7.3125e-13 \
        ad=7.3125e-13 ps=3.45u pd=3.45u m=1 region=sat
ends Transconductor
// End of subcircuit definition.

// Library name: tsmc25Test
// Cell name: Amp_CurrentSource_No_R
// View name: schematic
subckt Amp_CurrentSource_No_R Vinm Vinp Vout
```

```
    R0 (net067 net077) resistor r=1M m=1
    R1 (net065 net074) resistor r=1M m=1
    R7 (net066 0) resistor r=1M m=1
    R2 (net077 net076) resistor r=1M m=1
    R6 (net071 0) resistor r=1M m=1
    R3 (net074 net083) resistor r=1M m=1
    R4 (net076 net071) resistor r=1M m=1
    R5 (net083 net066) resistor r=1M m=1
    P12 (net0163 net079 vdd! vdd!) tsmc25P w=6.75u l=112.5u as=5.0625e-12 \
        ad=5.0625e-12 ps=15.0u pd=15.0u m=1 region=sat
    P10 (net079 net079 vdd! vdd!) tsmc25P w=2.25u l=112.5u as=1.6875e-12 \
        ad=1.6875e-12 ps=6u pd=6u m=1 region=sat
    P9 (net095 net079 vdd! vdd!) tsmc25P w=2.25u l=112.5u as=1.6875e-12 \
        ad=1.6875e-12 ps=6u pd=6u m=1 region=sat
    P8 (net096 net079 vdd! vdd!) tsmc25P w=2.25u l=112.5u as=1.6875e-12 \
        ad=1.6875e-12 ps=6u pd=6u m=1 region=sat
    P7 (net106 Vinm net095 vdd!) tsmc25P w=420.075u l=1.5u as=3.15056e-10 \
        ad=3.15056e-10 ps=841.65u pd=841.65u m=1 region=sat
    P6 (net102 Vinp net095 vdd!) tsmc25P w=420.075u l=1.5u as=3.15056e-10 \
        ad=3.15056e-10 ps=841.65u pd=841.65u m=1 region=sat
    P5 (net0105 0 net102 vdd!) tsmc25P w=140.025u l=1.5u as=1.05019e-10 \
        ad=1.05019e-10 ps=281.55u pd=281.55u m=1 region=sat
    P4 (net0109 0 net106 vdd!) tsmc25P w=140.025u l=1.5u as=1.05019e-10 \
        ad=1.05019e-10 ps=281.55u pd=281.55u m=1 region=sat
    P3 (net118 net139 vdd! vdd!) tsmc25P w=20.025u l=20.025u \
        as=1.50188e-11 ad=1.50188e-11 ps=41.55u pd=41.55u m=1 region=sat
    P2 (net069 net139 vdd! vdd!) tsmc25P w=20.025u l=20.025u \
        as=1.50188e-11 ad=1.50188e-11 ps=41.55u pd=41.55u m=1 region=sat
    P1 (Vout net096 net118 vdd!) tsmc25P w=6u l=1.5u as=4.5e-12 ad=4.5e-12 \
        ps=13.5u pd=13.5u m=1 region=sat
    P0 (net139 net096 net069 vdd!) tsmc25P w=6u l=1.5u as=4.5e-12 \
        ad=4.5e-12 ps=13.5u pd=13.5u m=1 region=sat
    N7 (net096 net096 0 0) tsmc25N w=4.05u l=2.25u as=3.0375e-12 \
        ad=3.0375e-12 ps=9.6u pd=9.6u m=1 region=sat
    N6 (net079 net096 net0158 0) tsmc25N w=75.0u l=2.25u as=5.625e-11 \
        ad=5.625e-11 ps=151.5u pd=151.5u m=1 region=sat
    N5 (net0158 net0163 0 0) tsmc25N w=2.25u l=363.075u as=1.6875e-12 \
        ad=1.6875e-12 ps=6u pd=6u m=1 region=sat
    N4 (Vout net096 net0109 0) tsmc25N w=3.525u l=1.5u as=2.64375e-12 \
        ad=2.64375e-12 ps=8.55u pd=8.55u m=1 region=sat
    N3 (net139 net096 net0105 0) tsmc25N w=3.525u l=1.5u as=2.64375e-12 \
        ad=2.64375e-12 ps=8.55u pd=8.55u m=1 region=sat
    N2 (net0109 net096 net065 0) tsmc25N w=180.075u l=3u as=1.35056e-10 \
        ad=1.35056e-10 ps=361.65u pd=361.65u m=1 region=sat
    N1 (net0105 net096 net067 0) tsmc25N w=180.075u l=3u as=1.35056e-10 \
        ad=1.35056e-10 ps=361.65u pd=361.65u m=1 region=sat
    N0 (net0163 net0163 0 0) tsmc25N w=2.25u l=241.875u as=1.6875e-12 \
        ad=1.6875e-12 ps=6u pd=6u m=1 region=sat
ends Amp_CurrentSource_No_R
// End of subcircuit definition.

// Library name: ThesisNeuralAmpFinal
// Cell name: FinalAmp_and_Filter
// View name: schematic
V0 (Half_Vdd 0) vsource type=dc dc=900m
Vps (vdd! 0) vsource type=dc dc=1.8
Vs (Vin Vref) vsource type=sine dc=0 mag=20u phase=0 freq=f
```

```
V4 (Vref 0) vsource type=sine dc=300m mag=0 phase=0 sinedc=0 ampl=0 freq=0
I112 (Ibias5 Vout Vout Half_Vdd Vbias) Transconductor
G3 (Ibias4 Vout Half_Vdd net128 Vbias) Transconductor
G0 (Ibias1 Vout1stOrder Half_Vdd VoutAmp Vbias) Transconductor
G2 (Ibias3 net128 Vout Vout1stOrder Vbias) Transconductor
G1 (Ibias2 Vout1stOrder Vout1stOrder Half_Vdd Vbias) Transconductor
N6 (net142 net142 0 0) tsmc25N w=5.7u l=450.0n as=4.275e-12 ad=4.275e-12 \
        ps=12.9u pd=12.9u m=1 region=sat
N5 (Vbias net142 net144 0) tsmc25N w=6.375u l=450.0n as=4.78125e-12 \
        ad=4.78125e-12 ps=14.25u pd=14.25u m=1 region=sat
N8 (net144 net148 0 0) tsmc25N w=450.0n l=72.525u as=3.375e-13 \
        ad=3.375e-13 ps=2.4u pd=2.4u m=1 region=sat
N7 (net148 net148 0 0) tsmc25N w=450.0n l=48.375u as=3.375e-13 \
        ad=3.375e-13 ps=2.4u pd=2.4u m=1 region=sat
P2 (Ibias1 Vbias vdd! vdd!) tsmc25P w=450.0n l=22.5u as=3.375e-13 \
        ad=3.375e-13 ps=2.4u pd=2.4u m=1 region=sat
P7 (net148 Vbias vdd! vdd!) tsmc25P w=1.35u l=22.5u as=1.0125e-12 \
        ad=1.0125e-12 ps=4.2u pd=4.2u m=1 region=sat
P6 (Vbias Vbias vdd! vdd!) tsmc25P w=450.0n l=22.5u as=3.375e-13 \
        ad=3.375e-13 ps=2.4u pd=2.4u m=1 region=sat
P0 (Ibias2 Vbias vdd! vdd!) tsmc25P w=450.0n l=22.5u as=3.375e-13 \
        ad=3.375e-13 ps=2.4u pd=2.4u m=1 region=sat
P1 (Ibias3 Vbias vdd! vdd!) tsmc25P w=450.0n l=22.5u as=3.375e-13 \
        ad=3.375e-13 ps=2.4u pd=2.4u m=1 region=sat
P8 (net142 Vbias vdd! vdd!) tsmc25P w=450.0n l=22.5u as=3.375e-13 \
        ad=3.375e-13 ps=2.4u pd=2.4u m=1 region=sat
P4 (Ibias4 Vbias vdd! vdd!) tsmc25P w=450.0n l=22.5u as=3.375e-13 \
        ad=3.375e-13 ps=2.4u pd=2.4u m=1 region=sat
P3 (Ibias5 Vbias vdd! vdd!) tsmc25P w=450.0n l=22.5u as=3.375e-13 \
        ad=3.375e-13 ps=2.4u pd=2.4u m=1 region=sat
P10 (net226 net226 net185 net185) tsmc25P w=6u l=6u as=4.5e-12 ad=4.5e-12 \
        ps=13.5u pd=13.5u m=1 region=sat
P11 (net185 net185 net189 net189) tsmc25P w=6u l=6u as=4.5e-12 ad=4.5e-12 \
        ps=13.5u pd=13.5u m=1 region=sat
P5 (net225 net225 net208 net208) tsmc25P w=6u l=6u as=4.5e-12 ad=4.5e-12 \
        ps=13.5u pd=13.5u m=1 region=sat
P38 (net196 net196 net200 net200) tsmc25P w=6u l=6u as=4.5e-12 ad=4.5e-12 \
        ps=13.5u pd=13.5u m=1 region=sat
P37 (net200 net200 Half_Vdd Half_Vdd) tsmc25P w=6u l=6u as=4.5e-12 \
        ad=4.5e-12 ps=13.5u pd=13.5u m=1 region=sat
P40 (net189 net189 net205 net205) tsmc25P w=6u l=6u as=4.5e-12 ad=4.5e-12 \
        ps=13.5u pd=13.5u m=1 region=sat
P9 (net208 net208 net196 net196) tsmc25P w=6u l=6u as=4.5e-12 ad=4.5e-12 \
        ps=13.5u pd=13.5u m=1 region=sat
P39 (net205 net205 VoutAmp VoutAmp) tsmc25P w=6u l=6u as=4.5e-12 \
        ad=4.5e-12 ps=13.5u pd=13.5u m=1 region=sat
CL (Vout 0) capacitor c=7p m=1
C2 (net128 0) capacitor c=15.5972p m=1
C1 (Vout1stOrder 0) capacitor c=15.5972p m=1
C3 (Vout 0) capacitor c=8.59718p m=1
Cf2 (net225 Half_Vdd) capacitor c=267f m=1
Cin1 (Vin net226) capacitor c=40.05p m=1
Cf1 (net226 VoutAmp) capacitor c=267f m=1
CLamp (VoutAmp 0) capacitor c=800f m=1
Cin2 (Vref net225) capacitor c=40.05p m=1
I67 (net226 net225 VoutAmp) Amp_CurrentSource_No_R
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
```

```
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 ckptclock=1800 \
    sensfile="../psf/sens.output" checklimitdest=psf
ac ac start=1m stop=100k dec=101 annotate=status
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000 annotate=status
dcOpInfo info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=allpub
```

Extracted Input File

```
// Generated for: spectre
// Generated on: Dec  2 01:55:40 2014
// Design library name: ThesisNeuralAmpFinal
// Design cell name: FinalAmp_and_Filter
// Design view name: extracted
simulator lang=spectre
global 0
parameters f=30
include "/programs/cadence/ncsu-cdk-1.5.1/models/spectre/standalone/tsmc25N.m"
include "/programs/cadence/ncsu-cdk-1.5.1/models/spectre/standalone/tsmc25P.m"

// Library name: ThesisNeuralAmpFinal
// Cell name: FinalAmp_and_Filter
// View name: extracted
\+429 (0 _74) capacitor c=1.09125e-16 m=1
\+427 (0 _72) capacitor c=1.09125e-16 m=1
\+379 (0 _74) capacitor c=5.72244e-15 m=1
\+378 (0 _73) capacitor c=5.72244e-15 m=1
\+145 (Vout 0) capacitor c=2.70879e-15 m=1
\+438 (_13 _55) capacitor c=6.984e-16 m=1
\+437 (_12 _54) capacitor c=6.984e-16 m=1
\+436 (_11 _13) capacitor c=6.984e-16 m=1
\+435 (_10 _12) capacitor c=6.984e-16 m=1
\+434 (_9 _11) capacitor c=6.984e-16 m=1
\+433 (_8 _10) capacitor c=6.984e-16 m=1
\+432 (_7 _9) capacitor c=6.984e-16 m=1
\+414 (0 _20) capacitor c=5.45625e-17 m=1
\+413 (0 _18) capacitor c=5.45625e-17 m=1
\+408 (Half_Vdd _8) capacitor c=6.984e-16 m=1
\+405 (vdd! _54) capacitor c=3.3174e-15 m=1
\+388 (_13 _55) capacitor c=2.856e-16 m=1
\+387 (_12 _54) capacitor c=2.0988e-16 m=1
\+386 (_11 _13) capacitor c=2.4084e-16 m=1
\+385 (_10 _12) capacitor c=2.4084e-16 m=1
\+384 (_9 _11) capacitor c=2.4084e-16 m=1
\+383 (_8 _10) capacitor c=2.4084e-16 m=1
\+382 (_7 _9) capacitor c=2.4084e-16 m=1
\+377 (0 _72) capacitor c=5.72244e-15 m=1
\+374 (0 _58) capacitor c=1.98904e-15 m=1
```

```
\+373 (0 _55) capacitor c=1.10305e-14 m=1
\+338 (0 _20) capacitor c=3.15276e-15 m=1
\+336 (0 _18) capacitor c=2.98248e-15 m=1
\+333 (0 _15) capacitor c=5.16e-17 m=1
\+331 (0 _13) capacitor c=2.1336e-16 m=1
\+330 (0 _12) capacitor c=2.1336e-16 m=1
\+329 (0 _11) capacitor c=2.1336e-16 m=1
\+328 (0 _10) capacitor c=2.1336e-16 m=1
\+327 (0 _9) capacitor c=2.1336e-16 m=1
\+326 (0 _8) capacitor c=2.1336e-16 m=1
\+324 (Half_Vdd _8) capacitor c=2.4084e-16 m=1
\+312 (vdd! _60) capacitor c=1.31844e-15 m=1
\+225 (_7 _55) capacitor c=1.3812e-16 m=1
\+222 (_7 _20) capacitor c=1.3812e-16 m=1
\+221 (_7 _18) capacitor c=1.3812e-16 m=1
\+218 (0 _54) capacitor c=3.0215e-14 m=1
\+207 (0 _20) capacitor c=4.97692e-15 m=1
\+205 (0 _18) capacitor c=9.4708e-15 m=1
\+202 (0 _15) capacitor c=3.1167e-16 m=1
\+201 (0 _7) capacitor c=5.53026e-14 m=1
\+179 (vdd! _20) capacitor c=1.3812e-16 m=1
\+178 (vdd! _18) capacitor c=1.3812e-16 m=1
\+175 (vdd! _7) capacitor c=1.3812e-16 m=1
\+174 (vdd! 0) capacitor c=1.3812e-16 m=1
\+160 (_20 _55) capacitor c=1.3128e-16 m=1
\+159 (_18 _55) capacitor c=1.3128e-16 m=1
\+153 (0 _55) capacitor c=1.3845e-15 m=1
\+152 (0 _54) capacitor c=3.7269e-16 m=1
\+148 (Half_Vdd 0) capacitor c=3.45735e-16 m=1
\+147 (vdd! _55) capacitor c=9.18e-17 m=1
\+144 (Vout Half_Vdd) capacitor c=1.3128e-16 m=1
\+139 (0 _7) capacitor c=6.27507e-15 m=1
\+138 (Half_Vdd 0) capacitor c=5.74227e-15 m=1
\+137 (Vout 0) capacitor c=8.3088e-15 m=1
\+136 (_7 _55) capacitor c=1.42561e-14 m=1
\+135 (0 _55) capacitor c=4.356e-17 m=1
\+134 (0 _54) capacitor c=4.356e-17 m=1
\+131 (0 _7) capacitor c=3.72205e-14 m=1
\+130 (Half_Vdd _54) capacitor c=1.42561e-14 m=1
\+127 (Vout 0) capacitor c=6.23503e-13 m=1
\+426 (0 _71) capacitor c=1.09125e-16 m=1
\+415 (0 _22) capacitor c=5.82728e-16 m=1
\+412 (0 _17) capacitor c=7.96613e-16 m=1
\+411 (0 _16) capacitor c=1.28986e-14 m=1
\+410 (0 _14) capacitor c=4.70755e-13 m=1
\+406 (vdd! _55) capacitor c=3.3174e-15 m=1
\+398 (vdd! _22) capacitor c=3.49637e-15 m=1
\+397 (vdd! _17) capacitor c=2.36627e-14 m=1
\+396 (vdd! _16) capacitor c=3.38288e-16 m=1
\+395 (vdd! 0) capacitor c=6.6348e-15 m=1
\+393 (_55 _59) capacitor c=1.2348e-15 m=1
\+392 (_54 _59) capacitor c=1.2348e-15 m=1
\+390 (_16 _21) capacitor c=1.8522e-15 m=1
\+389 (_16 _19) capacitor c=1.8522e-15 m=1
\+376 (0 _71) capacitor c=5.72244e-15 m=1
\+375 (0 _60) capacitor c=7.02816e-15 m=1
\+372 (0 _54) capacitor c=9.24e-15 m=1
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\+340 (0 _22) capacitor c=1.57908e-15 m=1
\+339 (0 _21) capacitor c=2.30304e-15 m=1
\+337 (0 _19) capacitor c=1.82676e-15 m=1
\+335 (0 _17) capacitor c=5.83822e-15 m=1
\+334 (0 _16) capacitor c=5.98752e-15 m=1
\+332 (0 _14) capacitor c=2.69184e-15 m=1
\+325 (0 _7) capacitor c=1.66e-14 m=1
\+311 (vdd! _59) capacitor c=2.6934e-15 m=1
\+310 (vdd! _58) capacitor c=5.36937e-15 m=1
\+294 (vdd! _22) capacitor c=1.02e-15 m=1
\+293 (vdd! _21) capacitor c=1.18164e-15 m=1
\+292 (vdd! _19) capacitor c=4.99656e-15 m=1
\+291 (vdd! _17) capacitor c=1.08842e-15 m=1
\+290 (vdd! _16) capacitor c=9.5808e-16 m=1
\+289 (vdd! _14) capacitor c=7.572e-17 m=1
\+288 (vdd! _7) capacitor c=1.59793e-15 m=1
\+284 (_58 _60) capacitor c=1.3812e-16 m=1
\+283 (_54 _59) capacitor c=1.3812e-16 m=1
\+235 (_21 _22) capacitor c=1.3812e-16 m=1
\+234 (_19 _57) capacitor c=1.3812e-16 m=1
\+233 (_19 _56) capacitor c=1.3812e-16 m=1
\+232 (_19 _22) capacitor c=1.3812e-16 m=1
\+231 (_19 _21) capacitor c=1.3812e-16 m=1
\+230 (_16 _22) capacitor c=1.3812e-16 m=1
\+229 (_16 _19) capacitor c=2.7624e-16 m=1
\+228 (_16 _17) capacitor c=4.23825e-16 m=1
\+227 (_14 _17) capacitor c=1.3812e-16 m=1
\+226 (_14 _16) capacitor c=1.3812e-16 m=1
\+224 (_7 _22) capacitor c=1.3812e-16 m=1
\+223 (_7 _21) capacitor c=1.3812e-16 m=1
\+220 (0 _58) capacitor c=1.5705e-16 m=1
\+219 (0 _55) capacitor c=3.12958e-14 m=1
\+208 (0 _22) capacitor c=2.74489e-15 m=1
\+206 (0 _19) capacitor c=2.87766e-15 m=1
\+204 (0 _17) capacitor c=3.30786e-15 m=1
\+203 (0 _16) capacitor c=1.85918e-15 m=1
\+189 (vdd! _58) capacitor c=1.62608e-15 m=1
\+188 (vdd! _57) capacitor c=1.67535e-16 m=1
\+187 (vdd! _56) capacitor c=1.67535e-16 m=1
\+186 (vdd! _55) capacitor c=4.79625e-16 m=1
\+185 (vdd! _54) capacitor c=4.00785e-16 m=1
\+180 (vdd! _22) capacitor c=5.37368e-16 m=1
\+177 (vdd! _17) capacitor c=1.5426e-16 m=1
\+176 (vdd! _16) capacitor c=1.5426e-16 m=1
\+142 (0 _54) capacitor c=3.59435e-13 m=1
\+126 (Vref _54) capacitor c=1.53475e-12 m=1
\+125 (Vref 0) capacitor c=1.134e-16 m=1
\+431 (0 _76) capacitor c=1.09125e-16 m=1
\+428 (0 _73) capacitor c=1.09125e-16 m=1
\+425 (0 _53) capacitor c=4.1904e-15 m=1
\+424 (0 _51) capacitor c=8.89238e-14 m=1
\+423 (0 _50) capacitor c=2.54261e-16 m=1
\+422 (0 _49) capacitor c=9.23634e-15 m=1
\+421 (0 _44) capacitor c=9.23634e-15 m=1
\+420 (0 _40) capacitor c=6.984e-16 m=1
\+419 (0 _38) capacitor c=9.23634e-15 m=1
\+418 (0 _34) capacitor c=3.492e-16 m=1
```

```
\+417 (0 _32) capacitor c=9.23634e-15 m=1
\+416 (0 _27) capacitor c=9.23634e-15 m=1
\+409 (0 _7) capacitor c=3.492e-16 m=1
\+407 (Half_Vdd 0) capacitor c=1.3968e-15 m=1
\+404 (vdd! _53) capacitor c=1.73509e-14 m=1
\+403 (vdd! _48) capacitor c=1.9505e-14 m=1
\+402 (vdd! _43) capacitor c=1.9505e-14 m=1
\+401 (vdd! _37) capacitor c=1.9505e-14 m=1
\+400 (vdd! _31) capacitor c=1.9505e-14 m=1
\+399 (vdd! _26) capacitor c=1.9505e-14 m=1
\+394 (Vout 0) capacitor c=6.984e-16 m=1
\+391 (_49 _50) capacitor c=6.69915e-16 m=1
\+381 (0 _76) capacitor c=5.72244e-15 m=1
\+371 (0 _53) capacitor c=7.572e-17 m=1
\+370 (0 _52) capacitor c=1.78884e-15 m=1
\+369 (0 _51) capacitor c=7.4652e-16 m=1
\+368 (0 _50) capacitor c=5.0916e-16 m=1
\+367 (0 _49) capacitor c=2.32352e-15 m=1
\+366 (0 _48) capacitor c=7.7748e-16 m=1
\+365 (0 _47) capacitor c=3.9216e-16 m=1
\+364 (0 _46) capacitor c=4.7472e-16 m=1
\+363 (0 _45) capacitor c=4.4892e-16 m=1
\+362 (0 _44) capacitor c=2.90172e-15 m=1
\+361 (0 _43) capacitor c=7.7748e-16 m=1
\+360 (0 _42) capacitor c=3.9216e-16 m=1
\+359 (0 _41) capacitor c=4.7472e-16 m=1
\+358 (0 _40) capacitor c=3.65172e-15 m=1
\+357 (0 _39) capacitor c=4.4892e-16 m=1
\+356 (0 _38) capacitor c=2.99976e-15 m=1
\+355 (0 _37) capacitor c=7.7748e-16 m=1
\+354 (0 _36) capacitor c=3.9216e-16 m=1
\+353 (0 _35) capacitor c=4.7472e-16 m=1
\+352 (0 _34) capacitor c=2.92764e-15 m=1
\+351 (0 _33) capacitor c=4.4892e-16 m=1
\+350 (0 _32) capacitor c=3.10296e-15 m=1
\+349 (0 _31) capacitor c=7.7748e-16 m=1
\+348 (0 _30) capacitor c=3.9216e-16 m=1
\+347 (0 _29) capacitor c=4.7472e-16 m=1
\+346 (0 _28) capacitor c=4.4892e-16 m=1
\+345 (0 _27) capacitor c=3.20616e-15 m=1
\+344 (0 _26) capacitor c=7.7748e-16 m=1
\+343 (0 _25) capacitor c=3.9216e-16 m=1
\+342 (0 _24) capacitor c=4.7472e-16 m=1
\+341 (0 _23) capacitor c=4.4892e-16 m=1
\+323 (Half_Vdd 0) capacitor c=1.67724e-15 m=1
\+322 (vdd! _70) capacitor c=3.096e-16 m=1
\+321 (vdd! _69) capacitor c=1.15584e-15 m=1
\+320 (vdd! _68) capacitor c=3.096e-16 m=1
\+319 (vdd! _67) capacitor c=1.15584e-15 m=1
\+318 (vdd! _66) capacitor c=3.096e-16 m=1
\+317 (vdd! _65) capacitor c=1.15584e-15 m=1
\+316 (vdd! _64) capacitor c=3.096e-16 m=1
\+315 (vdd! _63) capacitor c=1.15584e-15 m=1
\+314 (vdd! _62) capacitor c=3.096e-16 m=1
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\+309 (vdd! _53) capacitor c=1.9443e-16 m=1
\+308 (vdd! _51) capacitor c=7.572e-17 m=1
```

```
\+307 (vdd! _50) capacitor c=3.492e-16 m=1
\+306 (vdd! _49) capacitor c=1.7892e-16 m=1
\+305 (vdd! _48) capacitor c=3.522e-16 m=1
\+304 (vdd! _44) capacitor c=1.7892e-16 m=1
\+303 (vdd! _43) capacitor c=3.522e-16 m=1
\+302 (vdd! _40) capacitor c=1.5144e-16 m=1
\+301 (vdd! _38) capacitor c=1.7892e-16 m=1
\+300 (vdd! _37) capacitor c=3.522e-16 m=1
\+299 (vdd! _34) capacitor c=7.572e-17 m=1
\+298 (vdd! _32) capacitor c=1.7892e-16 m=1
\+297 (vdd! _31) capacitor c=3.522e-16 m=1
\+296 (vdd! _27) capacitor c=1.7892e-16 m=1
\+295 (vdd! _26) capacitor c=3.522e-16 m=1
\+287 (vdd! 0) capacitor c=3.05863e-14 m=1
\+286 (Vout 0) capacitor c=4.45848e-15 m=1
\+285 (Vout vdd!) capacitor c=1.5144e-16 m=1
\+282 (_52 _53) capacitor c=1.4172e-16 m=1
\+281 (_50 _53) capacitor c=3.273e-16 m=1
\+280 (_50 _52) capacitor c=2.7957e-16 m=1
\+279 (_49 _53) capacitor c=1.3812e-16 m=1
\+278 (_48 _53) capacitor c=1.3812e-16 m=1
\+277 (_44 _70) capacitor c=1.3812e-16 m=1
\+276 (_44 _69) capacitor c=1.3812e-16 m=1
\+275 (_44 _53) capacitor c=1.3812e-16 m=1
\+274 (_44 _48) capacitor c=1.19493e-15 m=1
\+273 (_43 _53) capacitor c=1.3812e-16 m=1
\+272 (_40 _53) capacitor c=9.4224e-16 m=1
\+271 (_40 _44) capacitor c=1.3812e-16 m=1
\+270 (_40 _43) capacitor c=1.4172e-16 m=1
\+269 (_40 _42) capacitor c=1.4172e-16 m=1
\+268 (_40 _41) capacitor c=2.7984e-16 m=1
\+267 (_38 _70) capacitor c=1.3812e-16 m=1
\+266 (_38 _69) capacitor c=1.3812e-16 m=1
\+265 (_38 _68) capacitor c=1.3812e-16 m=1
\+264 (_38 _67) capacitor c=1.3812e-16 m=1
\+263 (_38 _53) capacitor c=1.3812e-16 m=1
\+262 (_38 _48) capacitor c=1.19493e-15 m=1
\+261 (_38 _43) capacitor c=1.19493e-15 m=1
\+260 (_38 _40) capacitor c=1.3812e-16 m=1
\+259 (_37 _53) capacitor c=1.3812e-16 m=1
\+258 (_34 _53) capacitor c=1.3812e-16 m=1
\+257 (_32 _70) capacitor c=1.31805e-16 m=1
\+256 (_32 _69) capacitor c=1.3812e-16 m=1
\+255 (_32 _68) capacitor c=1.31805e-16 m=1
\+254 (_32 _67) capacitor c=1.3812e-16 m=1
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\+251 (_32 _53) capacitor c=1.3812e-16 m=1
\+250 (_32 _48) capacitor c=1.19493e-15 m=1
\+249 (_32 _43) capacitor c=1.19493e-15 m=1
\+248 (_32 _37) capacitor c=1.19493e-15 m=1
\+247 (_32 _34) capacitor c=1.3812e-16 m=1
\+246 (_31 _53) capacitor c=1.3812e-16 m=1
\+245 (_27 _69) capacitor c=1.3812e-16 m=1
\+244 (_27 _67) capacitor c=1.3812e-16 m=1
\+243 (_27 _65) capacitor c=1.3812e-16 m=1
\+242 (_27 _63) capacitor c=1.3812e-16 m=1
```

```
\+241 (_27 _53) capacitor c=1.3812e-16 m=1
\+240 (_27 _48) capacitor c=1.19493e-15 m=1
\+239 (_27 _43) capacitor c=1.19493e-15 m=1
\+238 (_27 _37) capacitor c=1.19493e-15 m=1
\+237 (_27 _31) capacitor c=1.19493e-15 m=1
\+236 (_26 _53) capacitor c=1.3812e-16 m=1
\+217 (0 _53) capacitor c=1.07063e-14 m=1
\+216 (0 _52) capacitor c=1.47933e-15 m=1
\+215 (0 _49) capacitor c=4.5333e-16 m=1
\+214 (0 _44) capacitor c=8.0127e-16 m=1
\+213 (0 _40) capacitor c=5.02605e-15 m=1
\+212 (0 _38) capacitor c=1.77008e-15 m=1
\+211 (0 _34) capacitor c=2.26338e-15 m=1
\+210 (0 _32) capacitor c=2.72902e-15 m=1
\+209 (0 _27) capacitor c=3.68797e-15 m=1
\+200 (Half_Vdd _46) capacitor c=1.4172e-16 m=1
\+199 (Half_Vdd _44) capacitor c=9.80745e-16 m=1
\+198 (Half_Vdd _40) capacitor c=1.3812e-16 m=1
\+197 (Half_Vdd _38) capacitor c=1.47141e-15 m=1
\+196 (Half_Vdd _34) capacitor c=2.7624e-16 m=1
\+195 (Half_Vdd _32) capacitor c=1.3812e-16 m=1
\+194 (Half_Vdd _30) capacitor c=4.58445e-16 m=1
\+193 (Half_Vdd _29) capacitor c=1.4172e-16 m=1
\+192 (Half_Vdd _27) capacitor c=1.3812e-16 m=1
\+191 (Half_Vdd _23) capacitor c=6.53899e-16 m=1
\+190 (Half_Vdd 0) capacitor c=5.792e-14 m=1
\+184 (vdd! _44) capacitor c=5.2533e-16 m=1
\+183 (vdd! _38) capacitor c=1.05066e-15 m=1
\+182 (vdd! _32) capacitor c=1.74789e-15 m=1
\+181 (vdd! _27) capacitor c=2.6538e-15 m=1
\+173 (Vout _53) capacitor c=8.0412e-16 m=1
\+172 (Vout _35) capacitor c=1.3812e-16 m=1
\+171 (Vout _34) capacitor c=4.7112e-16 m=1
\+170 (Vout _32) capacitor c=1.3812e-16 m=1
\+169 (Vout _30) capacitor c=1.4172e-16 m=1
\+168 (Vout _29) capacitor c=1.4172e-16 m=1
\+167 (Vout _28) capacitor c=1.4532e-16 m=1
\+166 (Vout _27) capacitor c=2.7624e-16 m=1
\+165 (Vout _26) capacitor c=1.4172e-16 m=1
\+164 (Vout _25) capacitor c=6.00165e-16 m=1
\+163 (Vout _24) capacitor c=2.7984e-16 m=1
\+162 (Vout 0) capacitor c=4.88277e-14 m=1
\+161 (Vout Half_Vdd) capacitor c=7.4736e-16 m=1
\+158 (_7 _53) capacitor c=1.3128e-16 m=1
\+157 (_7 _44) capacitor c=1.3128e-16 m=1
\+156 (_7 _38) capacitor c=1.3128e-16 m=1
\+155 (_7 _32) capacitor c=1.3128e-16 m=1
\+154 (_7 _27) capacitor c=1.3128e-16 m=1
\+151 (0 _40) capacitor c=1.0548e-16 m=1
\+150 (0 _34) capacitor c=2.94474e-15 m=1
\+149 (0 _7) capacitor c=4.90113e-15 m=1
\+146 (vdd! _7) capacitor c=9.18e-17 m=1
\+141 (0 _40) capacitor c=8.514e-17 m=1
\+140 (0 _34) capacitor c=7.848e-17 m=1
\+133 (0 _40) capacitor c=6.09797e-13 m=1
\+132 (0 _34) capacitor c=6.09575e-13 m=1
\+430 (0 _75) capacitor c=1.09125e-16 m=1
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\+380 (0 _75) capacitor c=5.72244e-15 m=1
\+143 (0 _55) capacitor c=3.59435e-13 m=1
\+129 (Vin _55) capacitor c=1.53475e-12 m=1
\+128 (Vin 0) capacitor c=1.0944e-16 m=1
\+118 (Vout 0) capacitor c=6.99314e-12 m=1
\+117 (_54 Half_Vdd) capacitor c=2.67322e-13 m=1
\+116 (_55 _7) capacitor c=2.67322e-13 m=1
\+119 (_7 0) capacitor c=7.99476e-13 m=1
\+121 (Vout 0) capacitor c=8.59329e-12 m=1
\+123 (Vin _55) capacitor c=4.007e-11 m=1
\+120 (Vref _54) capacitor c=4.007e-11 m=1
\+124 (_40 0) capacitor c=1.55938e-11 m=1
\+122 (_34 0) capacitor c=1.55938e-11 m=1
\+115 (_75 0) resistor r=999514 m=1
\+114 (0 _76) resistor r=999514 m=1
\+113 (_75 _73) resistor r=999514 m=1
\+112 (_74 _76) resistor r=999514 m=1
\+111 (_71 _73) resistor r=999514 m=1
\+110 (_74 _72) resistor r=999514 m=1
\+109 (_71 _20) resistor r=999514 m=1
\+108 (_18 _72) resistor r=999514 m=1
\+52 (_14 _17 vdd! vdd!) tsmc25P w=6.75e-06 l=0.000112425 as=6.075e-12 \
       ad=6.075e-12 ps=8.55e-06 pd=8.55e-06 m=1 region=sat
\+54 (_16 _17 vdd! vdd!) tsmc25P w=2.25e-06 l=0.000112425 as=2.025e-12 \
       ad=2.025e-12 ps=4.05e-06 pd=4.05e-06 m=1 region=sat
\+58 (_55 _55 _13 _13) tsmc25P w=6e-06 l=6e-06 as=5.4e-12 ad=5.4e-12 \
       ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+57 (_54 _54 _12 _12) tsmc25P w=6e-06 l=6e-06 as=5.4e-12 ad=5.4e-12 \
       ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+56 (_13 _13 _11 _11) tsmc25P w=6e-06 l=6e-06 as=5.4e-12 ad=5.4e-12 \
       ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+55 (_12 _12 _10 _10) tsmc25P w=6e-06 l=6e-06 as=5.4e-12 ad=5.4e-12 \
       ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+51 (_11 _11 _9 _9) tsmc25P w=6e-06 l=6e-06 as=5.4e-12 ad=5.4e-12 \
       ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+50 (_10 _10 _8 _8) tsmc25P w=6e-06 l=6e-06 as=5.4e-12 ad=5.4e-12 \
       ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+49 (_9 _9 _7 _7) tsmc25P w=6e-06 l=6e-06 as=5.4e-12 ad=5.4e-12 \
       ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+48 (_8 _8 Half_Vdd Half_Vdd) tsmc25P w=6e-06 l=6e-06 as=5.4e-12 \
       ad=5.4e-12 ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+67 (_59 _17 vdd! vdd!) tsmc25P w=2.25e-06 l=0.000112425 as=2.025e-12 \
       ad=2.025e-12 ps=4.05e-06 pd=4.05e-06 m=1 region=sat
\+53 (_17 _17 vdd! vdd!) tsmc25P w=2.25e-06 l=0.000112425 as=2.025e-12 \
       ad=2.025e-12 ps=4.05e-06 pd=4.05e-06 m=1 region=sat
\+60 (_57 _22 vdd! vdd!) tsmc25P w=2.0025e-05 l=2.0025e-05 as=1.80225e-11 \
       ad=1.80225e-11 ps=2.1825e-05 pd=2.1825e-05 m=1 region=sat
\+59 (_56 _22 vdd! vdd!) tsmc25P w=2.0025e-05 l=2.0025e-05 as=1.80225e-11 \
       ad=1.80225e-11 ps=2.1825e-05 pd=2.1825e-05 m=1 region=sat
\+62 (_22 _16 _57 vdd!) tsmc25P w=6e-06 l=1.5e-06 as=5.4e-12 ad=5.4e-12 \
       ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+61 (_7 _16 _56 vdd!) tsmc25P w=6e-06 l=1.5e-06 as=5.4e-12 ad=5.4e-12 \
       ps=7.8e-06 pd=7.8e-06 m=1 region=sat
\+71 (_19 0 _60 vdd!) tsmc25P w=3.5025e-05 l=1.5e-06 as=1.57612e-11 \
       ad=2.62687e-11 ps=9e-07 pd=3.6525e-05 m=1 region=sat
\+70 (_60 0 _19 vdd!) tsmc25P w=3.5025e-05 l=1.5e-06 as=1.57612e-11 \
       ad=1.57612e-11 ps=9e-07 pd=9e-07 m=1 region=sat
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\+69 (_19 0 _60 vdd!) tsmc25P w=3.5025e-05 l=1.5e-06 as=1.57612e-11 \
        ad=1.57612e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+68 (_60 0 _19 vdd!) tsmc25P w=3.5025e-05 l=1.5e-06 as=2.62687e-11 \
        ad=1.57612e-11 ps=3.6525e-05 pd=9e-07 m=1 region=sat
\+66 (_21 0 _58 vdd!) tsmc25P w=3.5025e-05 l=1.5e-06 as=1.57612e-11 \
        ad=2.62687e-11 ps=9e-07 pd=3.6525e-05 m=1 region=sat
\+65 (_58 0 _21 vdd!) tsmc25P w=3.5025e-05 l=1.5e-06 as=1.57612e-11 \
        ad=1.57612e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+64 (_21 0 _58 vdd!) tsmc25P w=3.5025e-05 l=1.5e-06 as=1.57612e-11 \
        ad=1.57612e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+63 (_58 0 _21 vdd!) tsmc25P w=3.5025e-05 l=1.5e-06 as=2.62687e-11 \
        ad=1.57612e-11 ps=3.6525e-05 pd=9e-07 m=1 region=sat
\+79 (_60 _55 _59 vdd!) tsmc25P w=0.000105075 l=1.5e-06 as=4.72837e-11 \
        ad=7.88063e-11 ps=9e-07 pd=0.000106575 m=1 region=sat
\+78 (_59 _55 _60 vdd!) tsmc25P w=0.000105075 l=1.5e-06 as=4.72837e-11 \
        ad=4.72837e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+77 (_60 _55 _59 vdd!) tsmc25P w=0.000105075 l=1.5e-06 as=4.72837e-11 \
        ad=4.72837e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+76 (_59 _55 _60 vdd!) tsmc25P w=0.000105075 l=1.5e-06 as=7.88063e-11 \
        ad=4.72837e-11 ps=0.000106575 pd=9e-07 m=1 region=sat
\+75 (_58 _54 _59 vdd!) tsmc25P w=0.000105075 l=1.5e-06 as=4.72837e-11 \
        ad=7.88063e-11 ps=9e-07 pd=0.000106575 m=1 region=sat
\+74 (_59 _54 _58 vdd!) tsmc25P w=0.000105075 l=1.5e-06 as=4.72837e-11 \
        ad=4.72837e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+73 (_58 _54 _59 vdd!) tsmc25P w=0.000105075 l=1.5e-06 as=4.72837e-11 \
        ad=4.72837e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+72 (_59 _54 _58 vdd!) tsmc25P w=0.000105075 l=1.5e-06 as=7.88063e-11 \
        ad=4.72837e-11 ps=0.000106575 pd=9e-07 m=1 region=sat
\+99 (_69 _48 _48 vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+98 (_70 _48 _40 vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+97 (_70 _48 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+96 (_69 _48 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+95 (_68 _43 _40 vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+94 (_68 _43 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+93 (_67 _43 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+92 (_67 _43 _43 vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+91 (_65 _37 _37 vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+90 (_66 _37 _34 vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+89 (_66 _37 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+88 (_65 _37 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+87 (_63 _31 _31 vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+86 (_64 _31 Vout vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+85 (_64 _31 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
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        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+84 (_63 _31 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+83 (_61 _26 _26 vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+82 (_62 _26 Vout vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+81 (_62 _26 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+80 (_61 _26 vdd! vdd!) tsmc25P w=6e-07 l=2.025e-05 as=5.4e-13 ad=5.4e-13 \
        ps=2.4e-06 pd=2.4e-06 m=1 region=sat
\+107 (vdd! _53 _53 vdd!) tsmc25P w=4.5e-07 l=2.25e-05 as=4.95e-13 \
        ad=4.95e-13 ps=2.55e-06 pd=2.55e-06 m=1 region=sat
\+106 (vdd! _53 _49 vdd!) tsmc25P w=4.5e-07 l=2.25e-05 as=4.95e-13 \
        ad=4.95e-13 ps=2.55e-06 pd=2.55e-06 m=1 region=sat
\+105 (vdd! _53 _44 vdd!) tsmc25P w=4.5e-07 l=2.25e-05 as=4.95e-13 \
        ad=4.95e-13 ps=2.55e-06 pd=2.55e-06 m=1 region=sat
\+104 (vdd! _53 _38 vdd!) tsmc25P w=4.5e-07 l=2.25e-05 as=4.95e-13 \
        ad=4.95e-13 ps=2.55e-06 pd=2.55e-06 m=1 region=sat
\+103 (vdd! _53 _32 vdd!) tsmc25P w=4.5e-07 l=2.25e-05 as=4.95e-13 \
        ad=4.95e-13 ps=2.55e-06 pd=2.55e-06 m=1 region=sat
\+102 (vdd! _53 _27 vdd!) tsmc25P w=4.5e-07 l=2.25e-05 as=4.95e-13 \
        ad=4.95e-13 ps=2.55e-06 pd=2.55e-06 m=1 region=sat
\+100 (vdd! _53 _50 vdd!) tsmc25P w=4.5e-07 l=2.25e-05 as=4.95e-13 \
        ad=4.95e-13 ps=2.55e-06 pd=2.55e-06 m=1 region=sat
\+101 (vdd! _53 _51 vdd!) tsmc25P w=1.35e-06 l=2.25e-05 as=1.305e-12 \
        ad=1.305e-12 ps=3.45e-06 pd=3.45e-06 m=1 region=sat
\+0 (_14 _14 0 0) tsmc25N w=2.25e-06 l=0.000242325 as=1.6875e-12 \
        ad=1.6875e-12 ps=3.75e-06 pd=3.75e-06 m=1 region=sat
\+1 (_15 _14 0 0) tsmc25N w=2.25e-06 l=0.000363825 as=1.6875e-12 \
        ad=1.6875e-12 ps=3.75e-06 pd=3.75e-06 m=1 region=sat
\+2 (_16 _16 0 0) tsmc25N w=4.05e-06 l=2.25e-06 as=3.645e-12 ad=3.645e-12 \
        ps=5.85e-06 pd=5.85e-06 m=1 region=sat
\+3 (_17 _16 _15 0) tsmc25N w=7.5e-05 l=2.25e-06 as=6.75e-11 ad=6.75e-11 \
        ps=7.68e-05 pd=7.68e-05 m=1 region=sat
\+11 (_20 _16 _21 0) tsmc25N w=4.5075e-05 l=3e-06 as=2.02838e-11 \
        ad=3.38062e-11 ps=9e-07 pd=4.6575e-05 m=1 region=sat
\+10 (_21 _16 _20 0) tsmc25N w=4.5075e-05 l=3e-06 as=2.02838e-11 \
        ad=2.02838e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+9 (_20 _16 _21 0) tsmc25N w=4.5075e-05 l=3e-06 as=2.02838e-11 \
        ad=2.02838e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+8 (_21 _16 _20 0) tsmc25N w=4.5075e-05 l=3e-06 as=3.38062e-11 \
        ad=2.02838e-11 ps=4.6575e-05 pd=9e-07 m=1 region=sat
\+7 (_18 _16 _19 0) tsmc25N w=4.5075e-05 l=3e-06 as=2.02838e-11 \
        ad=3.38062e-11 ps=9e-07 pd=4.6575e-05 m=1 region=sat
\+6 (_19 _16 _18 0) tsmc25N w=4.5075e-05 l=3e-06 as=2.02838e-11 \
        ad=2.02838e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+5 (_18 _16 _19 0) tsmc25N w=4.5075e-05 l=3e-06 as=2.02838e-11 \
        ad=2.02838e-11 ps=9e-07 pd=9e-07 m=1 region=sat
\+4 (_19 _16 _18 0) tsmc25N w=4.5075e-05 l=3e-06 as=3.38062e-11 \
        ad=2.02838e-11 ps=4.6575e-05 pd=9e-07 m=1 region=sat
\+13 (_22 _16 _21 0) tsmc25N w=3.525e-06 l=1.5e-06 as=3.1725e-12 \
        ad=3.1725e-12 ps=5.325e-06 pd=5.325e-06 m=1 region=sat
\+12 (_7 _16 _19 0) tsmc25N w=3.525e-06 l=1.5e-06 as=3.1725e-12 \
        ad=3.1725e-12 ps=5.325e-06 pd=5.325e-06 m=1 region=sat
\+41 (0 _49 _45 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=8.775e-13 \
        ad=5.85e-13 ps=2.775e-06 pd=1.2e-06 m=1 region=sat
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\+34 (0 _44 _39 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=8.775e-13 \
        ad=5.85e-13 ps=2.775e-06 pd=1.2e-06 m=1 region=sat
\+29 (0 _38 _33 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=8.775e-13 \
        ad=5.85e-13 ps=2.775e-06 pd=1.2e-06 m=1 region=sat
\+22 (0 _32 _28 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=8.775e-13 \
        ad=5.85e-13 ps=2.775e-06 pd=1.2e-06 m=1 region=sat
\+16 (0 _27 _23 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=8.775e-13 \
        ad=5.85e-13 ps=2.775e-06 pd=1.2e-06 m=1 region=sat
\+42 (_48 _53 _47 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+40 (_47 _7 _45 0) tsmc25N w=3e-06 l=3e-06 as=1.8e-12 ad=2.7e-12 \
        ps=1.2e-06 pd=4.8e-06 m=1 region=sat
\+39 (_46 _53 _40 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+38 (_45 Half_Vdd _46 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=1.8e-12 \
        ps=4.8e-06 pd=1.2e-06 m=1 region=sat
\+36 (_43 _53 _42 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+35 (_42 Half_Vdd _39 0) tsmc25N w=3e-06 l=3e-06 as=1.8e-12 ad=2.7e-12 \
        ps=1.2e-06 pd=4.8e-06 m=1 region=sat
\+33 (_39 _40 _41 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=1.8e-12 \
        ps=4.8e-06 pd=1.2e-06 m=1 region=sat
\+32 (_41 _53 _40 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+30 (_37 _53 _36 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+28 (_36 _40 _33 0) tsmc25N w=3e-06 l=3e-06 as=1.8e-12 ad=2.7e-12 \
        ps=1.2e-06 pd=4.8e-06 m=1 region=sat
\+27 (_33 Vout _35 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=1.8e-12 \
        ps=4.8e-06 pd=1.2e-06 m=1 region=sat
\+26 (_35 _53 _34 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+24 (_31 _53 _30 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+23 (_30 _34 _28 0) tsmc25N w=3e-06 l=3e-06 as=1.8e-12 ad=2.7e-12 \
        ps=1.2e-06 pd=4.8e-06 m=1 region=sat
\+21 (_28 Half_Vdd _29 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=1.8e-12 \
        ps=4.8e-06 pd=1.2e-06 m=1 region=sat
\+20 (_29 _53 Vout 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+18 (_26 _53 _25 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+17 (_25 Half_Vdd _23 0) tsmc25N w=3e-06 l=3e-06 as=1.8e-12 ad=2.7e-12 \
        ps=1.2e-06 pd=4.8e-06 m=1 region=sat
\+15 (_23 Vout _24 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=1.8e-12 \
        ps=4.8e-06 pd=1.2e-06 m=1 region=sat
\+14 (_24 _53 Vout 0) tsmc25N w=3e-06 l=3e-06 as=2.7e-12 ad=2.7e-12 \
        ps=4.8e-06 pd=4.8e-06 m=1 region=sat
\+43 (_49 _49 0 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=5.85e-13 \
        ad=8.775e-13 ps=1.2e-06 pd=2.775e-06 m=1 region=sat
\+37 (_44 _44 0 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=5.85e-13 \
        ad=8.775e-13 ps=1.2e-06 pd=2.775e-06 m=1 region=sat
\+31 (_38 _38 0 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=5.85e-13 \
        ad=8.775e-13 ps=1.2e-06 pd=2.775e-06 m=1 region=sat
\+25 (_32 _32 0 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=5.85e-13 \
        ad=8.775e-13 ps=1.2e-06 pd=2.775e-06 m=1 region=sat
\+19 (_27 _27 0 0) tsmc25N w=9.75e-07 l=8.7525e-05 as=5.85e-13 \
```

```
        ad=8.775e-13 ps=1.2e-06 pd=2.775e-06 m=1 region=sat
\+44 (_50 _50 0 0) tsmc25N w=5.7e-06 l=4.5e-07 as=5.13e-12 ad=5.13e-12 \
        ps=7.5e-06 pd=7.5e-06 m=1 region=sat
\+46 (0 _51 _51 0) tsmc25N w=4.5e-07 l=4.845e-05 as=4.95e-13 ad=4.95e-13 \
        ps=2.55e-06 pd=2.55e-06 m=1 region=sat
\+47 (0 _51 _52 0) tsmc25N w=4.5e-07 l=7.26e-05 as=4.95e-13 ad=4.95e-13 \
        ps=2.55e-06 pd=2.55e-06 m=1 region=sat
\+45 (_53 _50 _52 0) tsmc25N w=6.375e-06 l=4.5e-07 as=5.7375e-12 \
        ad=5.7375e-12 ps=8.175e-06 pd=8.175e-06 m=1 region=sat
include
"/home/sagallegos/cadence/simulation/FinalAmp_and_Filter/spectre/extracted/ne
tlist/stimuli/StimulusFile.txt"
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 ckptclock=1800 \
    sensfile="../psf/sens.output" checklimitdest=psf
ac ac start=1m stop=100k dec=101 annotate=status
dcOp dc write="spectre.dc" maxiters=150 maxsteps=10000 annotate=status
dcOpInfo info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts  where=rawfile
saveOptions options save=allpub
```

Stimulus File (Extracted Layout Simulation)

```
simulator lang=spectre

Vps (vdd! 0) vsource type=dc dc=1.8
HalfVdd (Half_Vdd 0) vsource type=dc dc=900m
Vs (Vin Vref) vsource type=sine mag=10u phase=0 ampl=10u freq=f
Vcm (Vref 0) vsource type=sine dc=300m ampl=0 mag=0 phase=0 freq=0
```

BIOGRAPHICAL SKETCH

Samuel A. Gallegos was born in Mexico City, Mexico on June 10th, 1987. He moved to the United States in 2003 where he completed High School and continued to earn his Bachelor of Science degree in Electrical Engineering from The University of Texas Pan-American, he graduated *summa cum laude*, in the Spring of 2011. He was inducted to the Texas Nu Chapter of Tau Beta Pi and is a member of the Engineering Honor Society. He worked as a Graduate Teaching Assistant for the Electrical Engineering Department at The University of Texas Pan American from 2013-2014 while completing his graduate studies. Toward the end of his graduate studies he obtained a cooperative employment position as an integrated circuit Physical Design Engineer at IBM in Austin, TX from May-December 2014. He went on to obtain his Master of Science degree in Electrical Engineering from The University of Texas Pan-American, and graduated in the Fall of 2014.

The abstract of his Master's Thesis, presented in this manuscript, was accepted for a poster session at the International Semiconductor Devices and Research Symposium in Bethesda, MD, which he attended on December 11th - 13th, 2013. He currently works full-time as a Circuit Design Engineer at IBM, and his current mailing address is 1900 Hobby Horse Ct Apt. 1116 Austin, TX 78758.