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The optimization of amplifiers for UWB applications

Kyoung D. Kim
University of Texas-Pan American

THE OPTIMIZATION OF AMPLIFIERS FOR UWB APPLICATIONS

A Thesis

by

Kyoung D. Kim

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Approved as to style and content by:

Foltz, Heinrich Ph.D.
Chair of Committee

Son, Jae Sok Ph.D.
Committee Member

Timmer, Douglas Ph.D.
Committee Member

April 2005

ABSTRACT

Kim, Kyoung D, The Optimization Amplifiers For UWB Applications. Master of Science and Engineering (MSE). April 2006, 174 pp.; 147 figures, 14 tables, references, 16 titles.

Optimizations of 0.18 μm and 0.5 μm MOSFET amplifiers without using inductors for UWB applications are presented. A 3 dB bandwidth from 3.1 GHz to 9.9 GHz with minimum 9.6 dB of transducer gain at 10.6 GHz and approximate 92.8 mWatts of total power consumption are achieved. The source and load impedances were 50 ohms. Also, the number of capacitors and resistors has been minimized. To predict characteristics more precisely, the pad capacitance is added to the output port. In addition, a different feedback topology is presented which gives a lower Noise Figure with maximum 7.73 dB at 10.6 GHz with 300 ohms feedback resistance.

DEDICATION

This thesis is dedicated all the people who supported me.

이 논문을 나의 사랑하는 아내 유미와 항상 웃음을 주는 딸 민아 그리고 한국에 계신 부모님들을 비롯한 모든 가족들에게 바칩니다.

ACKNOLWEDGEMENT

This thesis has been possible with the help of many people. First and foremost, I am deeply thankful for my advisor Dr. Heinrich Foltz, for his continued support and guidance in my research, and his assistance in writing this thesis. It was a great opportunity and I was really excited to work on this research. I would like to thank the other members of committee, Dr. Jae Sok Son, and Dr. Douglas Timmer for the assistance and willingness for my thesis.

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CHAPTER 1

INTRODUCTION

Since UWB technology had been approved for commercialization by FCC, many engineers have been researching to meet its requirements. One of the requirements is the amplifier. It has been a technical challenge because UWB requires Ultra-Wideband as it represents. Therefore, many people have tried to breakthrough it and introduced several different approaches.

In this thesis, cascoded type which is among the approaches will be introduced. Though it gives better performances versus single stages of MOSFET amplifiers, such as Common-Source and Common-Gate, its performances should be enhanced to meet UWB requirements, especially frequency response. In addition, many other performances are needed to be enhanced as well, such as Transducer gain, total power consumption, and Noise Figure, etc. This thesis will show various optimizations of the introduced amplifier for UWB applications include the feedback topologies.

In chapter 2, the UWB technologies and applications will be briefly introduced. In chapter 3, previous approaches to the design of UWB amplifiers will be presented with comparisons. In chapter 4, at first fundamental theories of single MOSFETs' amplifiers will be re-visited and the technical limitations for UWB applications will be shown and then the proposed solution of this thesis which is a cascoded type will be shown with advantages against single MOSFET amplifiers. After this, the simulation of the initial

schematic platform will be shown. As stated previously, the initial platform should be enhanced to satisfy the UWB application, so that multistage approach will be introduced with its effects. In chapter 5, the optimizations of the proposed design will be shown. In this chapter, feedback topologies will be introduced to enhance the gain flatness and 3 dB bandwidth with eliminating passive elements. In chapter 6, the measurements of proposed design will be presented. Finally, in chapter 7, conclusions will be stated.

Additionally, in the appendices, the optimizations with 0.5 μm MOSFETs amplifier will be shown and a different design with a different feedback topology will be shown.

The lastly shown design in appendix with a different feedback topology gives much better Noise Figure which is one of the most important factors in receivers. Unlikely transmitters, receivers require a low noise to amplify the received signal with minimizing the noise. However, the design proposed in this thesis does not really satisfy the desired noise figure.

Though it gives a promising simulation result of noise figure, its research has not been done thoroughly because the new feedback topology has been found in the closing period of my research.

CHAPTER 2

UWB INTRODUCTION

Since the 1980s UWB technology has been researched for military purposes and recently it has shown possibilities of using it in wireless applications. Though it has interference issues with current wireless communications, the FCC (Federal Communications Commission) approved UWB for commercial applications on 2002.

UWB is a wireless communications technology which enables highly reliable communications through high-speed and high-performance wireless networks. In addition, the technology can be used for military purposes which require low interception and detection devices, and anti-collision devices, etc.

2.1 UWB DEFINITION

UWB refers to electromagnetic signal waveforms that have instantaneous fractional bandwidths greater than 0.25 with respect to a center frequency. There are two other classes identified by signal fractional bandwidth: narrowband, where the fractional bandwidth is less than 1%, and wideband, with a fractional bandwidth from 1 to 25%. Therefore, it differs substantially from conventional narrowband radio frequency (RF).

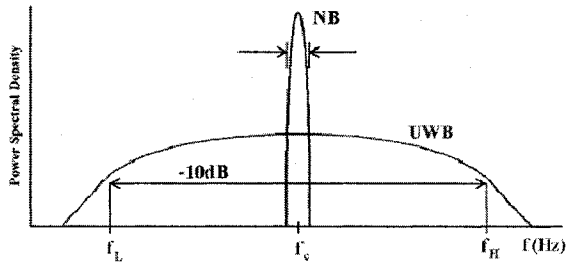

Figure 1 Definition of UWB

Fractional BW: $$\frac{f_H - f_L}{\left(\frac{f_H + f_L}{f_C}\right)} \geq 0.20$$

Where

f_H : Upper 10 dB down point

f_L : Lower 10 dB down point

f_C : Center frequency

2.2 UWB FREQUENCY ALLOCATIONS AND POWER LIMITS

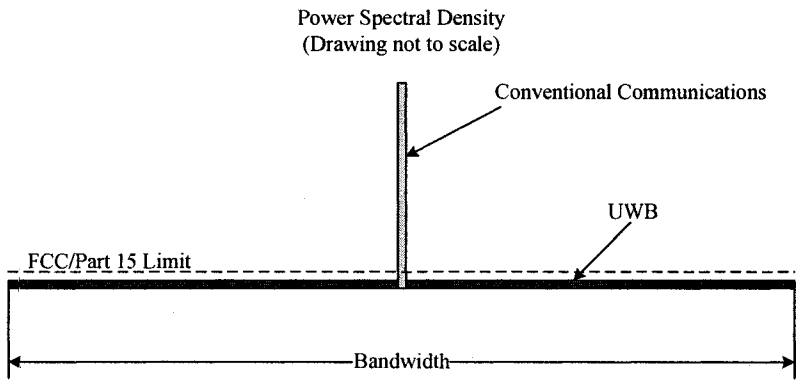

Figure 2 Comparison of conventional NB and UWB signal concept

UWB is a unique and new usage of a recently legalized frequency spectrum. UWB devices can use frequencies from 3.1 GHz to 10.6 GHz – a band more than 7 GHz wide. Each channel can have a bandwidth of more than 500 MHz, depending on its center frequency.

To allow for such a large signal bandwidth, the FCC put in place severe broadcast power restrictions. But by doing so, UWB devices can make use of an extremely wide frequency band while not emitting enough energy to be noticed by narrower band devices nearby, such as 802.11a/r radios.

Strict power limits (Figure 3) mean the devices themselves must be low-power consumers. Because of the low power requirements, it is feasible to develop cost-effective CMOS implementations of UWB devices.

Regulation

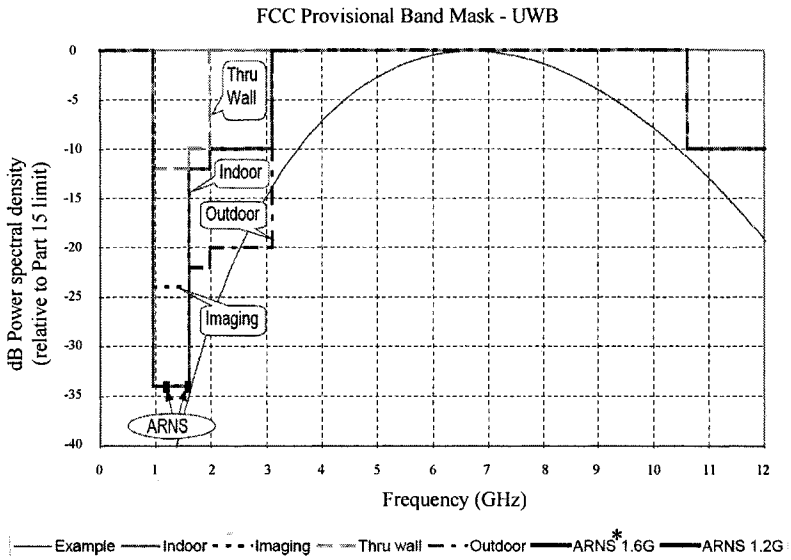

Figure 3[1] FCC UWB Limits

* ARNS: Aeronautical navigation services

2.3 APPLICATIONS

UWB applications can be divided into the military and commercial areas.

2.3.1 MILITARY APPLICATIONS

Fine spatial resolution, low probability of interception, and noninterfering signal waveforms are some of the features that make UWB radar appealing. Therefore, UWB radar offers solutions to defense requirements such as passive target identification, target imaging and discrimination, and signal concealment from electronic warfare equipment and antiradiation missiles.

The UWB radar's fine spatial resolution gives a capability for target imaging and discrimination of targets. Target clutter separation is a major problem in look-down radar

[1] Taken from "UWB Applications and Interference (UWB Colloquium 23rd July 2002)," Presenter: Ewan Frazer

and limits the ability to detect small radar cross section (RCS) low altitude flying targets or surface. In addition, the UWB radar could provide features such as detection surveillance or tracking systems with a low probability of detection by spectral characteristics of the signal.

2.4 COMMERCIAL (WIRELESS) APPLICATIONS

UWB technology offers a solution for the bandwidth, cost, power consumption, and physical size requirements of next-generation consumer electronic devices. UWB enables wireless connectivity with consistent high data rates across multiple devices and PCs within the digital home and the office. This emerging technology provides the high bandwidth that multiple digital video and audio streams require throughput the home[2].

A number of practical usage scenarios are well suited to UWB. In these scenarios system implementations based on UWB Radio Technology could be beneficial and potentially welcomed by industry and service providers alike[3]:

- High-data-rate wireless personal are network (HDR-WPAN)
- Wireless Ethernet interface link (WEIL)
- Intelligent wireless are network (IWAN)
- Outdoor peer-to-peer network (OPPN)

---

[2] Intel White paper, "Ultra-Wideband (UWB) Technology."

[3] Composite Reconfigurable Wireless Networks: The EU R&D Path Towards 4G, "Ultra-Wideband Radio Technology: Potential and Challenges Ahead." By Domencio Porcino, Phillips Research and Walter Hirt, IBM Zurich Research Laboratory

CHAPTER 3

PREVIOUS APPROACHES TO THE DESIGN OF UWB AMPLIFIERS

Since the FCC approved UWB technology for commercialization, various approaches have been made to the design of CMOS-based UWB amplifiers. In this section, the different methods shown below will be shown and compared.

- 3.1 – 10.6 GHz CMOS cascaded two-stage distributed amplifier for ultra-wideband application
- Ultra-wideband CMOS low noise amplifier with active input matching
- Design of CMOS UWB low noise amplifier with cascode feedback
- An ultra-wideband CMOS low noise amplifier for 3 – 5 GHz UWB system

3.1 3.1 ~ 10.6 GHz CMOS CASCADED TWO-STAGE DISTRIBUTED AMPLIFIER FOR ULTRA-WIDEBAND APPLICATION [1]

The work employed a topology in which several gain stages are in parallel and series-inductors are introduced to separate capacitances of the input and output node of adjacent gain stages.

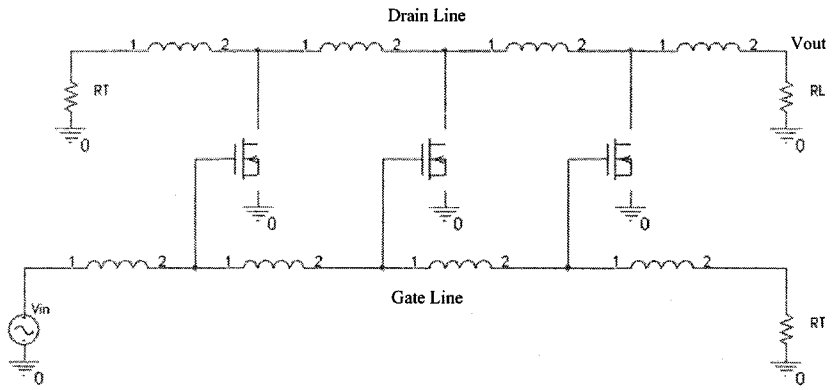

Figure 4[4] Three-stage distributed amplifier

This topology builds two artificial transmission lines, a gate and a drain line as shown in Figure 4. Output current is combined additively by the current flowing from each gain stage.

This topology results in low gain with very wide bandwidth.

A 3.1~10.6 GHz CMOS Cascaded Two-stage Distributed Amplifier for Ultra-Wideband Application has been proposed by Kuan-Hung Chen and Chorng-Kuang Wang in Aug. 4-5, 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits [1].

This paper proposed a cascaded two-stage distributed amplifier (CTDA) as shown in Figure 10 to give higher gain, better input-output isolation, and high output impedance.

[4] Redrawn the Fig. 1 from the reference [1]

The CTDA can achieve a voltage gain of 12~24 dB using less power consumption. In this work, an 18 dB voltage gain CTDA consuming only 54 mW has been presented for UWB application and the noise figure is between 5 dB and 7 dB.

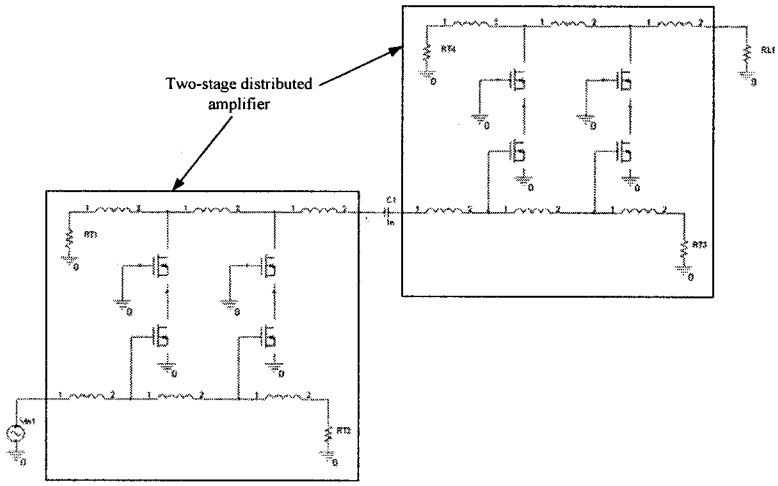

Figure 5[5] Cascaded two-stage distributed amplifier

[5] Redrawn the Fig. 3 from the reference [1]

3.2 ULTRA WIDEBAND CMOS LOW NOISE AMPLIFIER WITH ACTIVE INPUT MATCHING [2]

To improve impedance matching for the full band of frequency of operation, there are three main wideband topologies – resistive termination, shunt series feedback, and common gate.

Though all these three methods provide wideband matching at the price of increase noise, the common gate (CG) topology can be a good candidate for wideband impedance matching.

In [2], the authors propose a new LNA with broadband input matching and excellent gain flatness operating at the frequency range of 3.1 GHz to 4.8 GHz with 0.18 μm CMOS process.

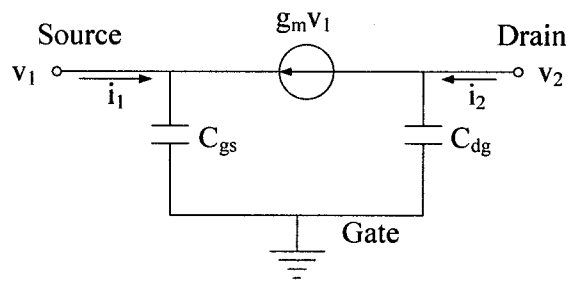

Figure 6[6] Common Gate small signal equivalent circuit

The first step is the selection of transistor size and the bias point of M1 to yield $\mathrm{Re}|Z_{11}| = 1/g_m = 50\Omega$.

[6] Redrawn the Figure 1. (b) from the reference [2]

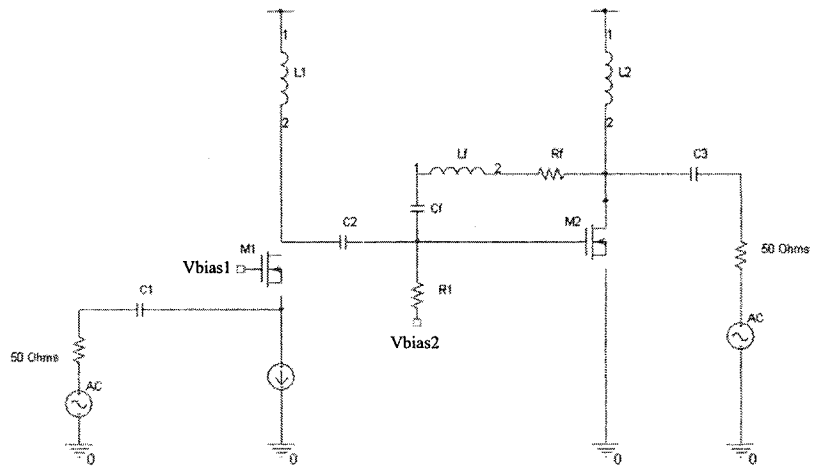

Figure 7[7] LNA circuit schematic

The next step is the selection of optimal bias point of second stage of M2, so that it operates at its maximum f_T.

In addition, this paper uses a shunt resistor feedback configuration to reduce $|S_{12}|$ and noise figure. Also, with adding an inductor L_f in the feedback path, the gain flatness at higher frequencies can be improved.

This paper shows that the proposed design can achieve with 0.18 μm CMOS at the frequency range of 3.1 GHz to 4.8 GHz as follows.

- Noise Figure (dB): 3.95 dB to 4.3 dB
- S_{12}: less than -43 dB
- Power Gain: 16.5 dB

[7] Redrawn the Figure 2 from the reference [2]

3.3 DESIGN OF CMOS UWB LOW NOISE AMPLIFIER WITH CASCODE FEEDBACK [3]

In [3], the authors describe a broadband LNA for UWB applications with 0.18 μm CMOS technology based on cascode feedback topology.

The cascode configuration is being used to reduce the high frequency roll-off of the input devices due to the Miller effect and the negative feedback is to give better stability and bandwidth (Figure 8).

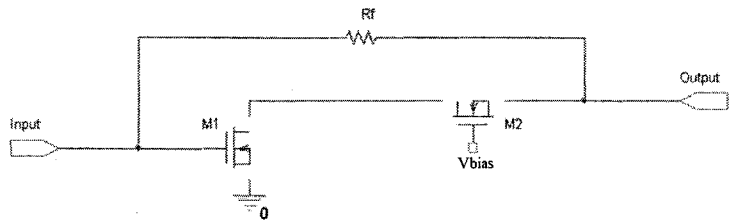

Figure 8[8] Typical schematic of cascode feedback LNA

To achieve a gain of over 15 dB and the NF of less than 2 dB, the feedback resistance was chosen to be between 800 Ω and 1000 Ω (Table 1).

Table 1[9] Effects on feedback resistance (NF_{min} & G_{max})

Feedback Resistance	NF_{min} (dB)	G_{max} (dB)
2000 Ω	1.08	19.16
1000 Ω	1.44	16.22
800 Ω	1.59	15.22

[8] Redrawn the Fig. 1. from the reference [3]

500 Ω	2.01	13.0
300 Ω	5.15	10.37

A broad matching technique with a lossy gain-compensating network such as aresonant circuit [4] provides lower input reflection coefficients and a lower NF because a lossy resonant circuit can imitate the behavior of a negative capacitor or inductor in the resonance frequency range.

The resonant circuit for broadband input matching is shown in Figure 9[9]. The gate inductor (L_g) is applied to form 50 Ω input match as well as increasing gain.

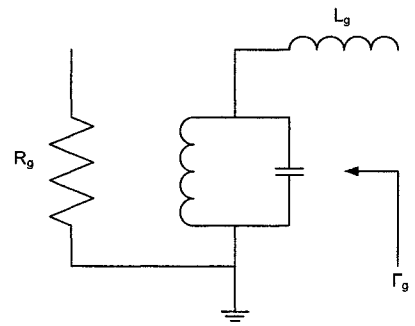

Figure 9 The resonant circuit for broadband input matching

[9] Taken from the reference [3]. (Fig. 3.)

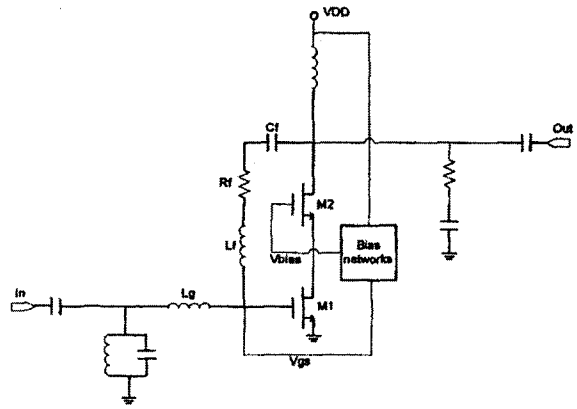

Figure 10[10] The complete schematic of LNA

The designed circuit schematic of the CMOS cascode feedback LNA is shown in Figure 10. In Figure 10, the RC feedback (R_f & C_f) in cascode circuit improves the S_{11}. The inductor (L_f) in the feedback stage is used to broaden bandwidth and to improve gain flatness at the upper band edge.

With this proposed design, a maximum power gain of 15.3 dB at 4 GHz and a minimum power gain of 14.5 dB at 7 GHz were achieved. The flatness of gain within 0.8 dB in the frequency range where achieved. The noise figure was 1.4 dB and 1.9 dB between 3 GHz and 7 GHz.

Simulation results are shown in Table 2.

Table 2[11] Simulation results of broadband LNA

Process	0.18 μm RF CMOS
Supply Voltage	1.8 V

[10] Taken from the reference [3]. (Fig. 6.)

[11] Redrawn the Table II from the reference [3]

Frequency Range	3 ~ 7 GHz
Power Gain (S21)	15 dB
Gain Flatness	< 0.8 dB
Noise Figure (NF)	< 1.9 dB @ 7 GHz
Power Consumption	21 mW with bias network

At the operation voltage of 1.8 V single supply, this amplifier has less than 1.9 dB noise figure, 15 dB gain within flatness 0.8 dB, and less than -10 dB input and output return loss from 3 GHz to 7 GHz with 21 mW power consumption.

3.4 AN ULTRA-WIDEBAND CMOS LOW NOISE AMPLIFIER FOR 3-5 GHz UWB SYSTEM [5]

In this paper, an ultra-wideband (UWB) CMOS low noise amplifier (LNA) topology that combines a narrowband LNA with a resistive shunt-feedback is proposed.

Figure 11[12](a) shows a typical narrowband cascade LNA topology. In Figure 11(a), the inductor L_s is added for simultaneous noise and input matching and L_g for the impedance matching between the source resistance R_s and the input of the LNA [6].

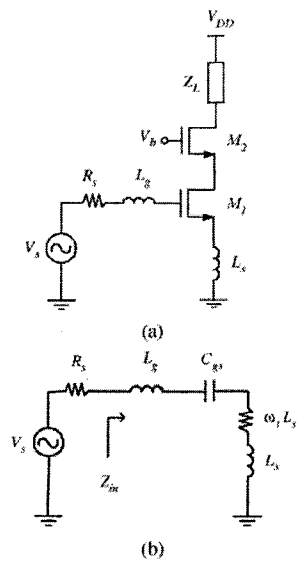

Figure 11 Narrowband LNA topology. (a) Overall schematic. (b) Small-signal equivalent circuit at the input.

Figure 11(b) shows the small –signal equivalent circuit for the input part of the overall LNA, where C_{gs} represents the gate-source capacitance of the input transistor M_1.

The ω_T represents the cutoff frequency of transistor M_1. the equality factor Q of the series resonating input circuit shown in Figure 11(b) can be given by [7]

[12] Copied from the reference [5] (Fig. 1.)

$$Q_{NB} = \frac{1}{(R_s + \omega_T L_s) \cdot \omega_0 \cdot C_{gs}} \tag{3.1}$$

where ω_0 represents the resonant frequency. Since the fractional -3 dB bandwidth of a typical *RLC* series resonant circuit is inversely proportional to its *Q*-factor ($BW_{-3\,dB} = \omega_0/Q_{NB}$), the LNA shown in Figure 12 (a) is unsuitable for wideband application.

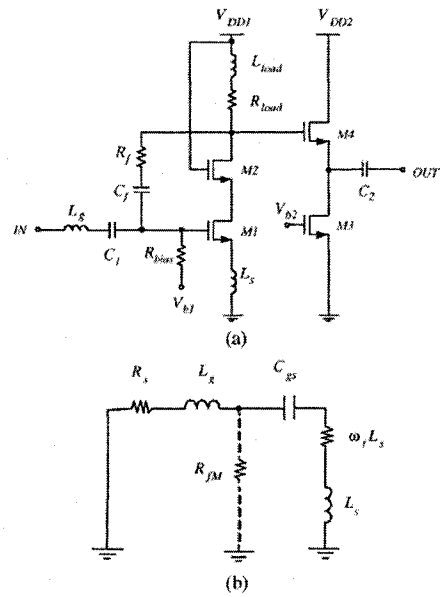

Figure 12[13] UWB LNA topology.

(a) Overall schematic. (b) Small-signal equivalent circuit at the input.

where ω_0 represents the resonant frequency. Since the fractional -3 dB bandwidth of a typical *RLC* series resonant circuit is inversely proportional to its *Q*-factor ($BW_{-3\,dB} = \omega_0/Q_{NB}$), the LNA shown in Figure 8 (a) is unsuitable for wideband application.

[13] Copied from the reference [5] (Fig. 2.)

Figure 12 (a) shows the proposed wideband LNA topology. In Figure 12 (b), the resistor $R_{fM}[= R_f /(1 - A_v)]$ represents the Miller equivalent input resistance of R_f, where Av is the open-loop voltage gain of the LNA.

In Figure 12 (a), R_f is added as a shunt-feedback element, L_{load} is used as a shunt peaking inductor at the output [8], the capacitor C_f is used for ac coupling purpose, the source follower of M_3 and M_4 is added for measurement purpose only, and C_1 and C_2 are ac coupling capacitors.

From the Figure 12 (b), the input impedance is determined by $\omega_T L_s$. Therefore, the feedback resistor R_f plays a main role to reduce the Q-factor of the resonating narrowband LNA input circuit. The Q-factor of the circuit shown in Figure 12 (b) can be approximately given by

$$Q_{WB} \approx \frac{1}{\left[R_s + \omega_T L_s + \frac{(\omega_o L_g)^2}{R_{fM}} \right] \cdot \omega_0 \cdot C_{gs}}. \qquad (3.2)$$

From (1.2), and considering the inversely linear relation between the -3 dB bandwidth and the Q-factor, the narrowband LNA in Figure 12 (a) can be converted into a wideband amplifier by the proper selection of R_f.

This topology is applied for a 3.1-5 GHz UWB amplifier implementation based on 0.18 μm CMOS technology. The measured results show more than 9 dB of input return loss, a higher than 11 dB output return loss, a peak gain of 9.8 dB over the -3 dB bandwidth of 2-4.6 GHz, while dissipating 7 mA from 1.8 V supply. The minimum NF is 2.3 dB at 3 GHz and stays at less than 3 dB up to 4 GHz, but rises up to 5.2 dB at 5 GHz.

3.5 SUMMARY OF DIFFERENT APPROACHES

The following Table 3 shows the summarized simulation result from the referenced papers.

Table 3 Summary of the simulation result of the referenced papers

Table 3. A summary of the simulation result of the referenced papers.

Referenced Paper	Technology	Frequency (GHz)	Gain (dB)	Noise Figure (dB)	Power Consumption (mW)
1. A 3.1 ~ 10.6 GHz CMOS Cascaded Two-stage Distributed Amplifier for Ultra-Wideband Application	TSMC 0.18 μm	3.1 ~ 10.6	18	5 ~ 7	54
2. Ultra Wideband CMOS Low Noise Amplifier with Active Input Matching	TSMC 0.18 μm	3.1 ~ 6.1	15.5 ~ 17	3.9 ~ 4.3	21
3. Design of CMOS UWB Low Noise Amplifier with Cascode Feedback	TSMC 0.18 μm	3 ~ 7	15 dB Min.: 14.5 @7 GHz Max.: 15.3 @4 GHz	< 1.9 @7 GHz	21 (w/bias network) 15 (w/o bias network)
4. An Ultra-Wideband CMOS Low Noise Amplifier for 3-5 GHz UWB System	0.18 μm	2 ~ 4.6	9.8	2.3 (minimum)	12.6 (only core LNA)

Based on the simulation (measured) data, paper 1 covers whole UWB frequency band with highest gain and highest power consumption. Paper 3 shows overall better result than paper 2. Paper 4 adopted a feedback resistor to reduce the Q-factor of the narrowband amplifier input impedance. As a result it shows advantages in overall performance (NF, power gain, power dissipation, chip size, number of external components, etc.), compared to the distributed and conventional shunt-feedback amplifiers for UWB applications.

CHAPTER 4

DESIGNING UWB AMPLIFIER

In this section, the basic theories of MOSFET, common-source single stage and common-gate MOSFET, and cascode topology will be shown and analyzed. By analyzing the high frequency characteristics of single stage MOSFET amplifiers, the need of a new design of, such as cascode topology will be shown.

Though cascoded topology gives better performances against single MOSFET amplifiers, it is required to enhance them to meet UWB requirements. Various considerations in broadband and multistage amplifiers will be shown.

4.1 MOSFET THEORY

In this section, the basic materials for MOSFET will be reviewed. These information have taken from various materials [9] [10] [11] [12] [13] [14] [15] [16].

4.1.1 MOSFET FUNDAMENTALS

In this chapter we are concerned with describing the fundamentals of MOSFET. MOS structures are assumed ideal and the long-channel enhancement-mode MOSFETs are focused.

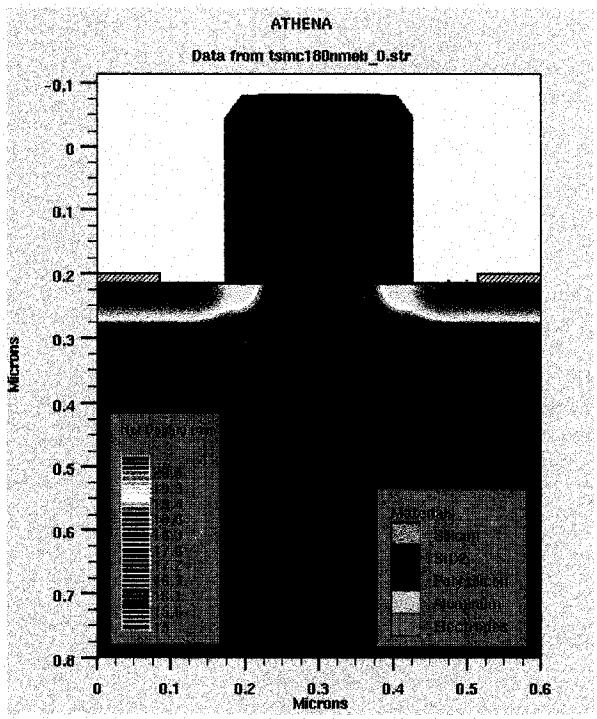

Figure 13[14] MOSFET structure simulation by Silvaco

[14] Project done for ELEE63201 with Edward Banatoski, Ph.D.
Simulated TSMC 180nm MOSFET through Silvaco Athena.

As shown in Figure 13 MOSFET (Metal Oxide Semiconductor Field Effect Transistor) has a structure of source and drain diffusion to the MOS capacitor which has a vertical stacking structure of metal (Gate), oxide, and semiconductor.

The MOSFET has become by far the most widely used electronic device, especially in the design of integrated circuits (ICs), which are circuits fabricated on a single silicon chip.

Compared to BJTs, MOSFETs can be made quite small and their manufacturing process relatively simple. Also, their operation requires comparatively little power. In addition, it is possible to implement digital and analog together.

All of these properties have made it possible to build VLSI circuits such as those for memory and microprocessors.

Therefore, MOSFET-based integrated circuits have become the dominant technology in the semiconductor industry. There are thousands of MOS-transistor circuits in production ranging from rather simple logic gates used in digital-signal processing to custom designs with both logic and memory functions on the same silicon chip.

4.1.2 MOSFET IV CHARACTERISTICS

The next Figure 14 shows the MOSFET with proper bias voltages.

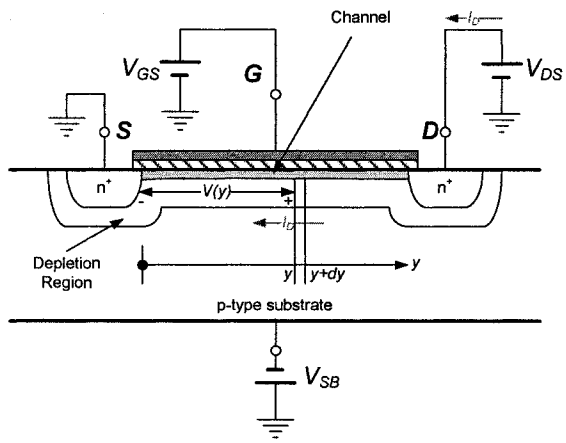

Figure 14 n-MOSFET device with bias voltages

When $V_{GS} < V_T$, the MOSFET is cutoff. If $V_{GS} > V_T$, inversion occurs and a conducting channel establishes. The channel conductivity is determined by the vertical electrical field, which is controlled by the voltage, $V_{GS} > V_T$. Nonzero V_{DS} produces a horizontal electrical field and causes current I_D to flow.

The drain current I_D is

$$I_D = K_n' \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2 \right) \tag{4.1}$$

Where

$$K_n' \triangleq \mu_n C_{OX} = \frac{\mu_n \varepsilon_{OX}}{t_{OX}} \tag{4.2}$$

C_{OX} : The gate oxide capacitance per unit area

$$\left(= \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9 \cdot \varepsilon_o}{t_{ox}} = \frac{3.9 \cdot \left(8.854 \times 10^{-14}\right)}{t_{ox}} \right)$$

In saturation region (4.1) becomes as follows with $(V_{GS} - V_T) = V_{DS}$

$$I_D = \left(\frac{1}{2}\right) K_n' \left(\frac{W}{L}\right) (V_{GS} - V_T)^2 \tag{4.3}$$

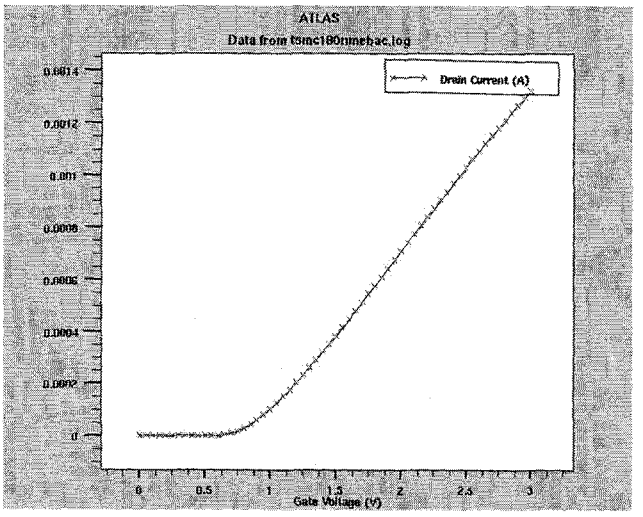

Figure 15[15] MOSFET V_G - I_D Graph by Silvaco simulation

Furthermore, (4.3) becomes as follows with a channel-length modulation

$$I_D = \left(\frac{1}{2}\right) K_n' \left(\frac{W}{L}\right) (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \tag{4.4}$$

Where

$$\lambda : \text{Channel-length modulation factor } \left(= \frac{1}{V_A}\right) \tag{4.5}$$

Figure 15 shows the relation between drain current I_D and gate voltage V_G. The drain current starts flowing when V_G is larger than V_T and gradually increase until a

[15] Project done for ELEE63201 with Edward Banatoski, Ph.D.
Simulated TSMC 180nm MOSFET through Silvaco Athena.

certain level of V_G. Based on the Figure 15, the larger V_G gives the higher I_D. However, V_G cannot be increased above a certain point (refer to the Figure 17) because the transconductance will be decreased.

4.1.3 SMALL-SIGNAL EQUIVALENT CIRCUIT OF MOSFET

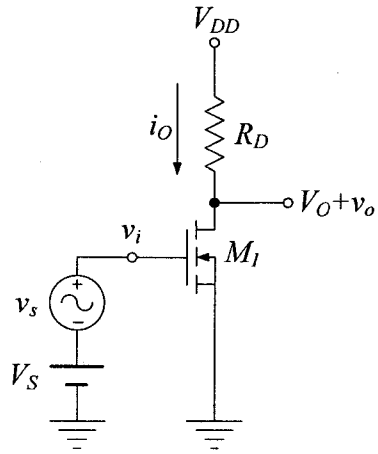

Figure 16 Common-source MOSFET amplifier circuit

4.2 SMALL-SIGNAL ANALYSIS

The total output current (i_O) when MOSFET (M_1) operates in saturation is as follows (neglected channel-length modulation):

$$i_O = \left(\frac{1}{2}\right) K_n' \left(\frac{W}{L}\right)(V_{GS} + v_{gs} - V_T)^2 \tag{4.6}$$

$$i_O = \frac{V_{DD} - (V_O + v_o)}{R_D} \tag{4.7}$$

With (4.6) and (4.7), the output voltage (v_o) is shown below.

$$
\begin{aligned}
v_o &= -R_D K_n' \left(\frac{W}{L}\right)\left\{(V_{GS}-V_T)v_{gs}+\frac{v_{gs}^2}{2}\right\} \\
&= -R_D K_n' \left(\frac{W}{L}\right)(V_{GS}-V_T)v_{gs}\left\{1+\frac{v_{gs}}{2(V_{GS}-V_T)}\right\}
\end{aligned}
\tag{4.8}
$$

The small-signal output current, $i_o = \frac{-v_o}{R_D}$, becomes as follows.

$$
i_o = K_n' \left(\frac{W}{L}\right)(V_{GS}-V_T)v_{gs}\left\{1+\frac{v_{gs}}{2(V_{GS}-V_T)}\right\} \tag{4.9}
$$

From (4.8) distortions occurs when v_{gs} is large. To make the distortion rate less than 10 %, the magnitude of small-signal input voltage ($|v_{gs}|$) should satisfy the following.

$$
|v_{gs}| \le 0.2(V_{GS}-V_T) \tag{4.10}
$$

When (4.10) is valid, the v_{gs}^2 term can be neglected from the equation (4.8) and the small-signal output voltage(v_O) and output current(i_o) can be shown as follows.

$$
v_o = -R_D K_n' \left(\frac{W}{L}\right)(V_{GS}-V_T)v_{gs} \tag{4.11}
$$

$$
i_o = K_n' \left(\frac{W}{L}\right)(V_{GS}-V_T)v_{gs} \tag{4.12}
$$

4.3 TRANSCONDUCTANCE

One of the most important components of a MOSFET ac analysis is find the voltage-to-current ratio (a proportional constant between i_o and v_{gs} in (4.12)). When the MOSFET operates in saturation region, it indicates how well a device converts a voltage to a current. The change in drain current that will result from a change in gate-to-source voltage can be determined using the transconductance factor g_m in the following way [10].

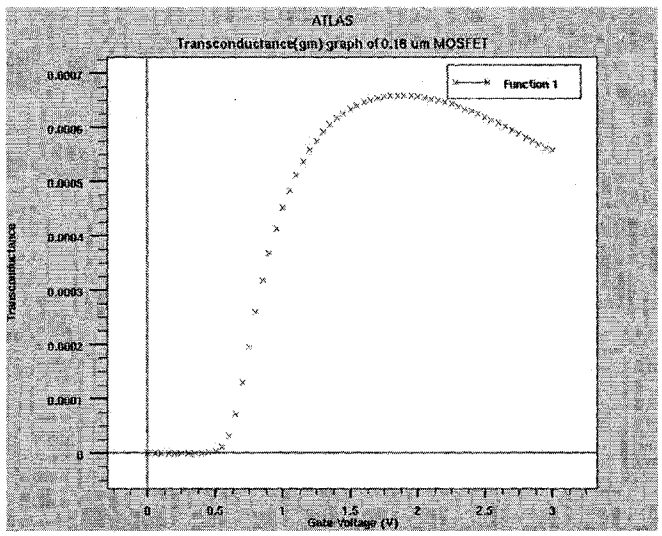

Figure 17[16] Transconductance graph from Silvaco simulation

$$g_m \triangleq \frac{\Delta I_O}{\Delta V_{GS}} = \frac{\partial i_o}{\partial v_{GS}} \tag{4.13}$$

From (4.12), transconductance(g_m) becomes as follows.

[16] Project done for ELEE63201 with Edward Banatoski, Ph.D.
Simulated TSMC 180nm MOSFET through Silvaco Athena.

$$g_m = K_n'\left(\frac{W}{L}\right)(V_{GS} - V_T) = \frac{2I_O}{(V_{GS} - V_T)} \tag{4.14}$$

Transconductance represents the sensitivity of the device: for high g_m, a small changes in V_{GS} results in a large change in I_O.

Figure 17 shows the relations between gate voltage and transconductance. There is a gate voltage which gives the maximum of transconductance. For designing amplifier, the proper gate (bias) voltage should be used.

4.4 OUTPUT RESISTANCE

Increasing drain-source voltage in an n-channel MOSFET increases the width of the depletion region around the Drain and reduces the effective channel length in the saturation region. This effective is called channel-length modulation and causes the Drain current to increase.

$$r_o \triangleq \left\{\left.\frac{\partial i_O}{\partial v_{DS}}\right|_{at\ Q}\right\}^{-1} = \frac{1}{\lambda I_O} \tag{4.15}$$

4.5 SINGLE STAGE MOSFET ANALYSIS

This section will show the analysis of the two different types of MOSFETs' topologies (common-source (CS) and common-gate (CG)) for high-frequency characteristics. The two main characteristics of transducer gain and high frequency response will be discussed though there are many other characteristics.

MOSFETs have internal gate capacitive effect. The gate electrode forms a parallel-plate capacitor with the channel, with the oxide layer serving as the capacitor dielectric.

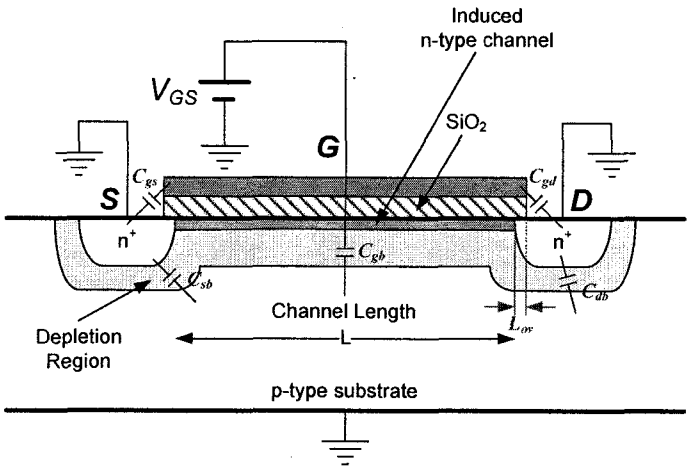

Figure 18 The cross-sectional view of a nMOSFET with various capacitances

As Figure 18 shows five main different capacitances in MOSFET. Gate capacitances are C_{gs}, C_{gd}, and C_{gb} and depletion capacitances are C_{sb} and C_{db}.

Based on the Meyer model which is being commonly used in SPICE simulation, each gate capacitances (neglect body effect coefficient γ) can be expressed as follows.

$$C_{gs} = W \cdot CGSO + \frac{2}{3} W \cdot L \cdot C_{OX} \qquad (4.16)$$

$$C_{gd} = W \cdot CGDO \tag{4.17}$$

$$C_{gb} = L \cdot CGBO \tag{4.18}$$

where

$$CGSO = CGDO = L_{ov} \times C_{ox} \tag{4.19}$$

where L_{ov} is the overlap length between the gate-source and gate-drain as shown in Figure 8. The intrinsic value of C_{gd} is zero because the channel is the pinched-off at the drain end. However, the value of C_{gd} has a parasitic value due to the overlap that depends on the layout. As C_{gd} plays an important role in deciding the bandwidth of some amplifiers, its influence cannot be ignored. [11]

Here are the typical values of *CGSO*, *CGDO*, and *CGBO* of TSMC T3CV 0.18 μm MOSFET[17].

$$CGSO = CGDO = 7.9 \times 10^{-10} \tag{4.20}$$

$$CGBO = 1 \times 10^{-12} \tag{4.21}$$

[17] Electrical parameters are shown in Appendix A-1.

4.5.1 COMMON-SOURCE MOSFET HIGH-FREQUENCY MODEL

The common-source amplifier uses the gate as an input ports and drain as an output port as shown in Figure 19 which includes internal capacitances for high frequency analysis.

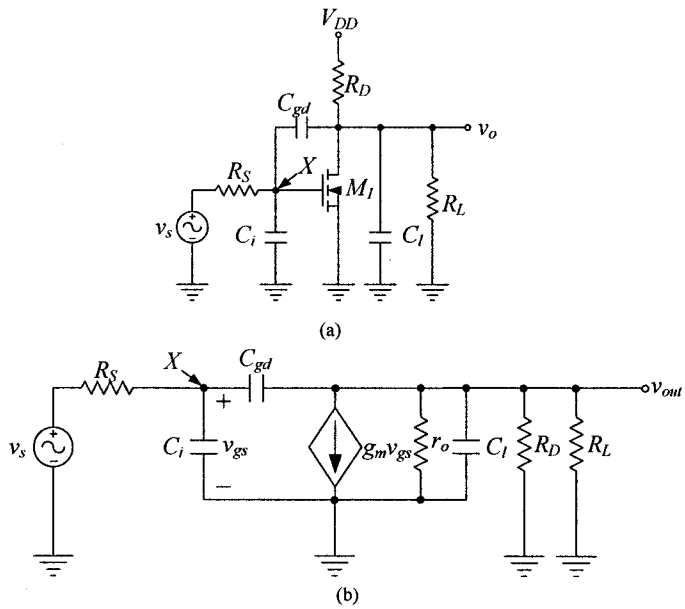

Figure 19 (a) Common-source MOSFET high frequency model (b) its small signal model

Where

$$C_i = C_{gs} + C_{gb} + \text{input wiring capacitances}$$

$$C_l = C_{db} + \text{output wiring capacitances}$$

C_{gd} itself is much smaller than C_{gs} and usually set to zero. However, because of the Miller's effect, it becomes the major factor for frequency response.

4.5.2 TRANSDUCER GAIN (G_T) OF CS MOSFET

The gain that we are interested in RF transistors is the power gain of the device, rather than just the voltage or current gain because voltage and current gains alone no longer mean anything when an impedance level changes in a circuit. [12]

Transducer Power Gain (G_T)

$$G_T = \frac{P_L}{P_{AVS}} = \frac{Power\ delivered\ to\ the\ load}{Power\ available\ from\ the\ source}$$

From Figure 11, the relations between v_{out} and v_x is as follows

$$v_{out} = -g_m v_x (R_L' \| sC_O) = -g_m v_x \frac{R_L'}{1 + R_L' sC_O} \tag{4.22}$$

Where $R_L' = \left(r_o \| R_D \| R_L\right)$ and the relations between v_s and v_x is

$$v_s = \left(1 + sR_S C_I\right) v_x \tag{4.23}$$

Therefore, voltage gain $\left(\frac{v_{out}}{v_s}\right)$ becomes

$$\frac{v_{out}}{v_s} = \frac{-g_m R_L'}{\left(1 + sR_S C_I\right)\left(1 + sR_L' C_O\right)} \tag{4.24}$$

From the definition of (G_T),

$$P_L = |i_L|^2 R_L' = \left|\frac{v_{out}}{R_L'}\right|^2 R_L' = \frac{|v_{out}|^2}{R_L'} \tag{4.25}$$

$$P_{AVS} = \frac{|v_S|^2}{4R_S} \tag{4.26}$$

Transducer gain (G_T) becomes

$$G_T = \frac{P_L}{P_{AVS}} = \frac{\left(\frac{|v_{out}|^2}{R_L'}\right)}{\left(\frac{|v_S|^2}{4R_S}\right)} = 4\frac{R_S|v_{out}|^2}{R_L'|v_S|^2} = 4\left(\frac{R_S}{R_L'}\right)\left|\frac{v_{out}}{v_S}\right|^2 \qquad (4.27)$$

Therefore, by substituting (4.27) with (4.24), transducer gain (G_T) of a single stage CS amplifier becomes

$$G_T(s) = 4\left(\frac{R_S}{R_L'}\right)\left|\frac{g_m R_L'}{(1+sR_L'C_O)(1+sR_SC_I)}\right|^2 \qquad (4.28)$$

4.5.3 FREQUENCY RESPONSE OF CS MOSFET

The frequency of the applied signal can have a very important effect on the response of a single-stage or multistage network. The frequency dependent parameters of the small-signal equivalent circuits and the stray capacitive elements associated with the active device and network will limit the high-frequency response of the system.

In this section the frequency response of CS amplifier in high-frequency will be analyzed to estimate the upper 3 dB frequency.

From (4.24), high frequency gain of the CS amplifier is as follows

$$|A_v(s)| = \left|\frac{v_{out}(s)}{v_s(s)}\right| = \left|\frac{A_M}{(1+sR_SC_I)(1+sR_L'C_O)}\right| \qquad (4.29)$$

Where $A_M \left(= g_m R_L'\right)$ is mid-band gain.

Equation (4.29) can be rearranged as follows

$$A_v(s) = \frac{v_{out}(s)}{v_s(s)} = \frac{A_M}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)} \tag{4.30}$$

From (4.30) the input pole ω_{P1} and the output pole ω_{P2} are as follows

$$\omega_{P1} = \frac{1}{R_S C_I} = \frac{1}{R_S\left(C_{gs} + (1+A_v)C_{gd}\right)} \tag{4.31}$$

$$\begin{aligned} \omega_{P2} &= \frac{1}{R_L' C_O} = \frac{1}{R_L'\left(C_{db} + \left(1+\frac{1}{A_v}\right)C_{gd}\right)} \\ &\cong \frac{1}{R_L'\left(C_{db} + C_{gd}\right)} \qquad \left(\because A_v \gg 1\right) \end{aligned} \tag{4.32}$$

By comparing the (4.31) and (4.32), the ω_{P1} is the dominant pole of the common-source amplifier and becomes

$$\omega_{P1} = \omega_H = \frac{1}{R_S\left(C_{gs} + (1+A_v)C_{gd}\right)} \tag{4.33}$$

Therefore, bandwidth (BW) of CS amplifier is

$$BW \triangleq f_H - f_L \cong f_H = \frac{1}{2\pi \cdot R_S\left(C_{gs} + (1+A_v)C_{gd}\right)} \tag{4.34}$$

The multiplication effect that C_{gd} undergoes comes about because it is connected between two nodes whose voltages are related by a large negative gain $(1+A_v)$. This Miller effect causes the CS amplifier to have a large total input impedance C_I and hence a low ω_H.

4.6 COMMON-GATE MOSFET HIGH-FREQUENCY MODEL

Common-gate amplifier applies DC bias voltage into gate node, input voltage into source node, and uses drain as an output port as shown in Figure 20. This amplifier gives large positive voltage gain with low input resistance and high output resistance.

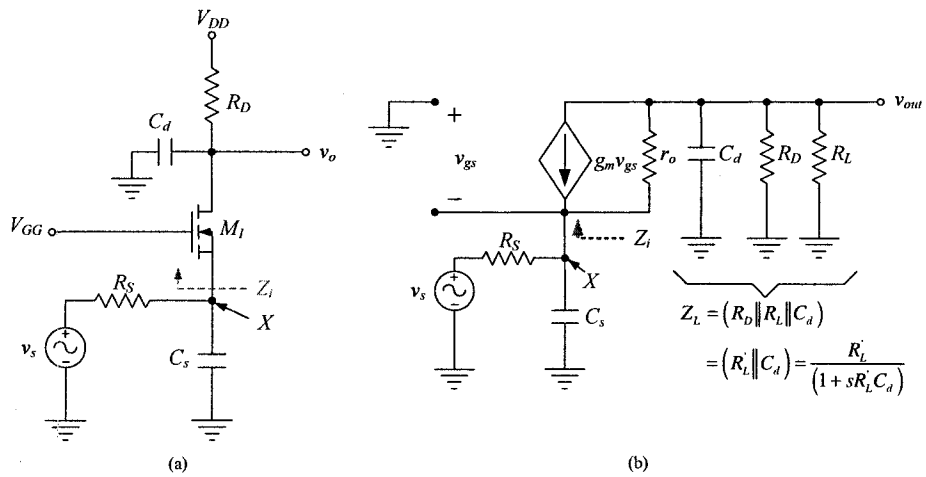

Figure 20 (a) Common-gate MOSFET high frequency model and (b) high-frequency small signal model

4.6.1 TRANSDUCER GAIN (G_T) OF CG MOSFET

To find the transducer gain (G_T), Figure 20 (b) is re-arranged as shown in Figure 21. [13]

By applying KCL at node X, we can find the current (i_s) flows at the resistor (R_S)

$$i_s + i_{ro} = g_m v_x + i_x \tag{4.35}$$

$$i_s = g_m v_x + i_x - i_{ro} = i_x + i_L = sC_i v_x + \frac{v_{out}}{Z_L} \tag{4.36}$$

Noting that the supply voltage must equal voltage across R_S plus v_x as follows

$$\begin{aligned} v_s &= R_S i_S + v_x = \left(sC_i v_x + \frac{v_{out}}{Z_L} \right) R_S + v_x \\ &= \left(sR_S C_i + 1\right) v_x + \left(\frac{R_S}{Z_L} \right) v_{out} \end{aligned} \tag{4.37}$$

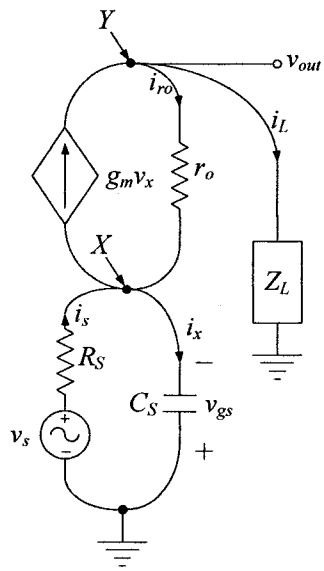

Figure 21 Re-arranged CG MOSFET high frequency small signal model

From (4.37), v_x can be expressed as follows

$$v_x = \frac{\left(v_s - \left(\frac{R_S}{Z_L} \right) v_{out} \right)}{\left(1 + sR_S C_i\right)} \tag{4.38}$$

Also the voltage v_{out} must equal v_x plus the voltage across r_o

$$
\begin{aligned}
v_{out} &= v_{r_o} + v_x = r_o\left(g_m v_x - i_L\right) + v_x \\
&= \left(1 + g_m r_o\right)v_x - r_o i_L = \left(1 + g_m r_o\right)v_x - \left(\frac{r_o}{Z_L}\right)v_{out}
\end{aligned}
\tag{4.39}
$$

With applying (4.39), we can have the relations between v_{out} and v_s as follows.

$$
\begin{aligned}
v_{out} &= \left(1 + g_m r_o\right)\frac{\left(v_s - \left(\frac{R_S}{Z_L}\right)v_{out}\right)}{\left(1 + sR_S C_i\right)} - \left(\frac{r_o}{Z_L}\right)v_{out} \\
&= \frac{\left(1 + g_m r_o\right)}{\left(1 + sR_S C_i\right)}v_s - \left(\frac{\left(1 + g_m r_o\right)R_S + r_o\left(1 + sR_S C_i\right)}{Z_L\left(1 + sR_S C_i\right)}\right)v_{out}
\end{aligned}
\tag{4.40}
$$

From (4.40) $\left(\frac{v_{out}}{v_S}\right)$ can be find as follows.

$$
\begin{aligned}
\left(\frac{v_{out}}{v_s}\right) &= \left(\frac{\frac{\left(1 + g_m r_o\right)}{\left(1 + sR_S C_i\right)}}{1 + \left(\frac{\left(1 + g_m r_o\right)R_S + r_o\left(1 + sR_S C_i\right)}{Z_L\left(1 + sR_S C_i\right)}\right)}\right) \\
&= \left(\frac{\left(1 + g_m r_o\right)}{\left(1 + sR_S C_i\right)\left(1 + \frac{r_o}{Z_L}\right) + \left(1 + g_m r_o\right)\left(\frac{R_S}{Z_L}\right)}\right)
\end{aligned}
\tag{4.41}
$$

Where,

$$
Z_L = \left(R_D \| R_L \| C_d\right) = \left(R_L^{'} \| C_d\right) = \frac{R_L^{'}}{\left(1 + sR_L^{'} C_d\right)}
\tag{4.42}
$$

Therefore, $\left(\frac{v_{out}}{v_S}\right)$ becomes as follows

$$\frac{(1+g_m r_o)R_L'}{\left((R_L'+r_o+(1+g_m r_o)R_S\right)+s\left(R_S(R_L'+r_o)C_i+r_o R_L' C_d+R_S R_L'(1+g_m r_o)C_d\right)+s^2 r_o R_S R_L' C_i C_d\right)} \tag{4.43}$$

The transducer gain (G_T) of a single stage CG amplifier becomes

$$G_T(s)=4\left(\frac{R_S}{R_L}\right)\times \left|\frac{(1+g_m r_o)R_L'}{\left((R_L'+r_o+(1+g_m r_o)R_S\right)+s\left(R_S(R_L'+r_o)C_i+r_o R_L' C_d+R_S R_L'(1+g_m r_o)C_d\right)+s^2 r_o R_S R_L' C_i C_d\right)}\right|^2 \tag{4.44}$$

4.6.2 FREQUENCY RESPONSE OF CG MOSFET

Finding the input impedance of CG amplifier make it easier to find the frequency response of the CG MOSFET.

To find the input impedance (Z_{in}) of CG amplifier, we need an input impedance circuit shown in Figure 22.

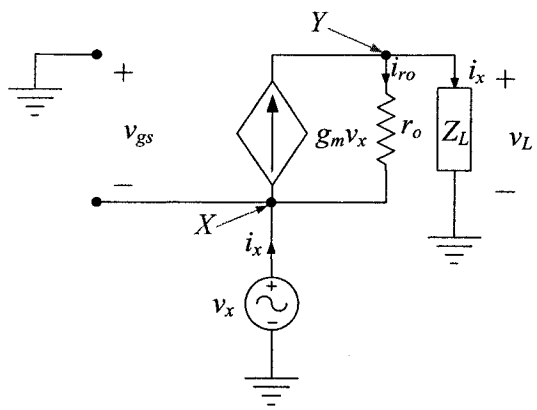

Figure 22 Re-arranged CG MOSFET for input impedance, Z_{in}

By KCL at node X of Figure 14 is

$$i_x = g_m v_x - i_{r_O} = g_m v_x - \frac{Z_L i_x - v_x}{r_O} \tag{4.45}$$

Therefore, the input impedance $\left(Z_{in} = \frac{v_x}{i_x}\right)$ is

$$Z_{in} = \frac{r_o + Z_L}{1 + g_m r_o} \tag{4.46}$$

From Figure 13 (b),

$$C_s = C_{gs} + C_{bs} \tag{4.47}$$

$$C_d = C_{gd} + C_{bd} \tag{4.48}$$

Where C_{bs} is the junction capacitance between bulk and source and C_{bd} is the junction capacitance between bulk and drain and omitted for simplification.

Dominant pole ω_p becomes

$$\omega_P = \omega_H = \frac{1}{\left(R_S \| Z_{in}\right) \cdot C_i} \tag{4.49}$$

The input impedance $Z_{in} = \frac{r_o + Z_L}{1 + g_m r_o}$ varies depends on the Z_{in} as

$$Z_{in,MIN.}\Big|_{at\ Z_L=0} \cong \frac{1}{g_m} \tag{4.50}$$

$$Z_{in,MAX.}\Big|_{at\ Z_L=\infty} = \infty \tag{4.51}$$

Therefore, the dominant pole exists between

$$\frac{1}{R_S \cdot C_i} \le \omega_H \le \frac{1}{\left(R_S \| \frac{1}{g_m}\right) \cdot C_i} \tag{4.52}$$

As a result, the minimum of ω_H can be expressed as follows.

$$\frac{1}{R_S \cdot C_i} = \frac{1}{R_S \cdot \left\{ W \cdot CGSO + \frac{2}{3} W \cdot L \cdot C_{OX} \right\}} \tag{4.53}$$

The dominant pole of CS MOSFET amplifier which is given by (4.33) can be restated as follows to be compared with CG MOSFET amplifier.

$$\frac{1}{R_S \cdot \left\{ W \cdot CGSO + \frac{2}{3} W \cdot L \cdot C_{OX} + W \cdot CGDO\left(1 + g_m R_D\right) \right\}} \tag{4.54}$$

If we compare the $\omega_{H,CS}$ (4.53) and $\omega_{H,CG}$ (4.53), frequency response of CG amplifier is much higher than CS amplifier.

4.7 CASCODE AMPLIFIER TOPOLOGY

In the previous sections Common-Source and Common-Gate MOSFET configurations were presented. For conventional and narrowband purpose, the CS amplifier can be used. However, it cannot be used for UWB application because of the Miller Effect which drastically decrease the frequency response, ω_{-3dB}. One of the possible ways of minimizing Miller effect is using a cascode topology which is shown in Figure 23.

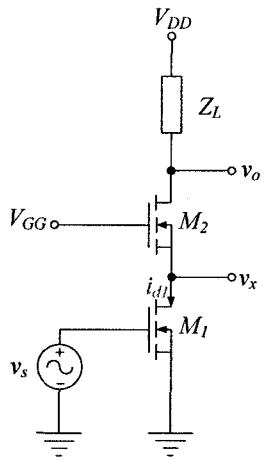

Figure 23 Basic cascode amplifier configuration

The Drain current, i_{d1} of M1 is given as follows

$$i_{dM1} = g_{mM1} v_s \tag{4.55}$$

Therefore, v_x is given as follows

$$\begin{aligned} v_x &= -i_{dM1} \cdot \left(r_{oM1} \| Z_{iM2} \right) \cong -i_{dM1} \cdot \left(r_{oM1} \| \frac{1}{g_{mM2}} \right) \\ &\cong -i_{dM1} \cdot \frac{1}{g_{mM2}} = -\left(\frac{g_{mM1}}{g_{mM2}} \right) v_s \end{aligned} \tag{4.56}$$

Where $Z_{iM2} \cong \dfrac{1}{g_{mM2}}$ from (4.50)

From (4.14)

$$\begin{aligned} g_{mM1} &= K_n' \left(\frac{W}{L} \right)_{M1} (V_{GS} - V_T) \\ g_{mM2} &= K_n' \left(\frac{W}{L} \right)_{M2} (V_{GS} - V_T) \end{aligned} \tag{4.57}$$

Therefore,

$$v_x = -\left(\frac{g_{mM1}}{g_{mM2}}\right)v_s = -\left(\frac{\left(\frac{W}{L}\right)_{M1}}{\left(\frac{W}{L}\right)_{M2}}\right)v_s \qquad (4.58)$$

From (4.58) it is clear that v_x is proportional to the ratio of the widths and lengths of *M1* and *M2*. If *M1* and *M2* have same physical dimensions, the small signal gain $\left(\frac{v_x}{v_s}\right)$ becomes -1.

As a result, the Miller effect becomes 2 (Miller constant). Therefore this cascode topology will have a better frequency response than single MOSFET CS transistors.

4.7.1 SMALL SIGNAL ANALYSIS OF CASCODE AMPLIFIER

The CASCODE is a very useful two-transistor stage that provides the performance of a CS stage with a much small Miller effect and much larger output resistance. Therefore, it gives better high-frequency performance and higher output resistance.

4.8 OUTPUT RESISTANCE OF CASCODE

From Figure 23 output resistance R_{out} can be found as follows.

$$g_{roM2}(v_o - v_2) = i_o + g_{mM2}v_2 \tag{4.59}$$

$$g_{roM2}(v_o - v_2) = (g_{roM1} + g_{mM2})v_2 \tag{4.60}$$

Therefore,

$$R_{out} = \frac{(g_{roM1} + g_{roM2} + g_{mM2})}{g_{roM1}g_{roM2}} \cong \frac{g_{mM2}}{g_{roM1}g_{roM2}} = g_{mM2}r_{oM2}r_{oM1} \tag{4.61}$$

From (4.61) it is evident that the output resistance of CASCODE is much larger than r_{oM1}.

4.9 HIGH-FREQUENCY RESPONSE OF CASCODE AMPLIFIER [16]

Figure 24 is shown as a high frequency equivalent circuit. Only C_{gs} and C_{gd} will be considered for simplifications.

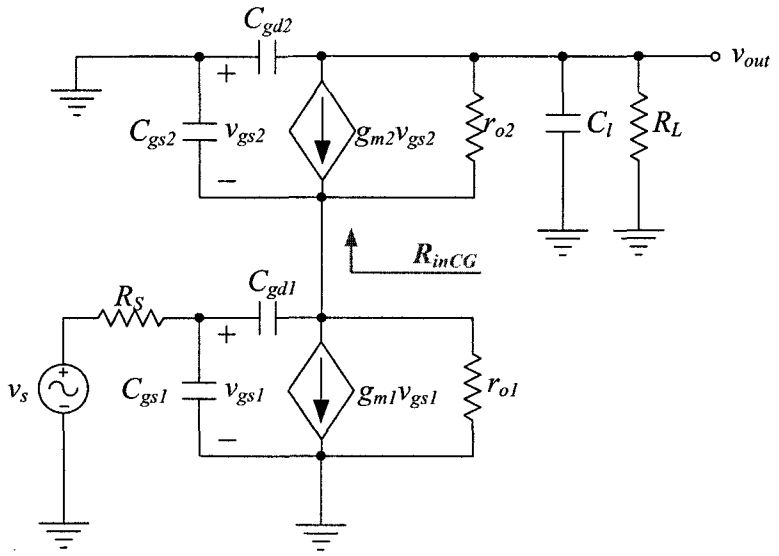

Figure 24 CASCODE small signal circuit for frequency response

With the open-circuit time constants, the frequency response can be estimated as follows

$$\tau_{gs1} = C_{gs1}R_S \tag{4.62}$$

For τ_{gd1}, at first the resistance R_{gd1} that is seen by the capacitor C_{gd1} must be found.

4.9.1.1 RE-VISIT CS AMPLIFIER

Figure 24 can be re-drawn to find the R_{gd1}.

The relation between i_x and v_x is given

$$\left(1+g_m R_S\right) i_x = -\frac{1}{\left(r_o \| R_L\right)}\left(R_S i_x - v_x\right) \tag{4.63}$$

Therefore, the resistance seen by the capacitor C_{gd1} is

$$\begin{aligned} R_x = R_{gd1} &= \left(r_o \| R_L\right) + R_S\left(1+g_m\left(r_o \| R_L\right)\right) \\ &= \left(r_o \| R_L\right) + R_S\left(1+\left|A_v\right|\right) \end{aligned} \tag{4.64}$$

Notice that the term $R_S\left(1+\left|A_v\right|\right)$ gives the largest contribution.

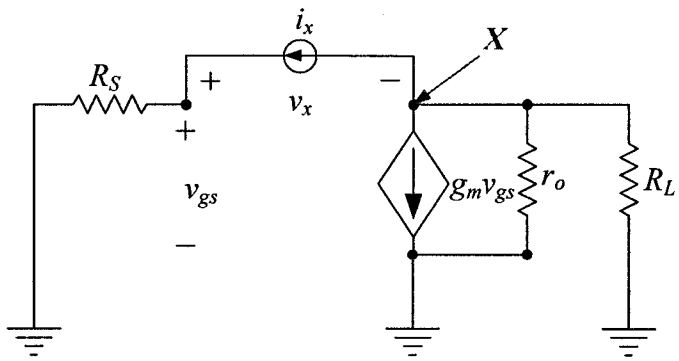

Figure 25 Circuit to find R_{gd1}

Therefore, τ_{gd1} is as follows

$$\tau_{gd1} = R_{gd1} C_{gd1} \tag{4.65}$$

From the calculation of time constants it has been shown that the largest time constant is associated with the drain-gate capacitance, C_{gd1}, even though hat capacitance is numerically the smallest one. The effect of this capacitance is multiplied by the gain $\left(1+\left|A_v\right|\right)$. As it has been explained previously, this is called Miller effect. This effect arises from connecting a capacitance across two nodes that have inverting voltage gain between them. One of the possible solutions of this problem is to isolate this capacitor so that it no longer appears across a gain stage. [11]

The CASCODE amplifier of Figure 16 shows the elimination Miller effect by performing this isolation. The output is at the drain of *M2*, while the input is at the gate of *M1*, and there is no capacitance directly across these two nodes.

4.10 TIME-CONSTANT OF A CASCODE AMPLIFIER

At first, the input resistance of CG stage is already given in (4.46).

$$R_{inCG}=\frac{r_{oM2}+R_L}{1+g_{mM2}r_{oM2}}\cong\frac{1}{g_{mM2}}\left(1+\frac{R_L}{r_{oM2}}\right) \tag{4.66}$$

The R_{gd1} from (4.64) becomes with R_{inCG} as follows

$$R_{gd1}=\left(r_{oM1}\left\|R_{inCG}\right.\right)+R_S\left(1+g_{mM1}\left(r_{oM1}\left\|R_{inCG}\right.\right)\right) \tag{4.67}$$

Therefore, the time constant τ_{gd1} is given

$$\tau_{gd1}=R_{gd1}C_{gd1}=C_{gd1}\left\{\left(r_{oM1}\left\|R_{inCG}\right.\right)+R_S\left(1+g_{mM1}\left(r_{oM1}\left\|R_{inCG}\right.\right)\right)\right\} \tag{4.68}$$

For the amplifier *M2*, time constants are

$$\tau_{gs2} = C_{gs2}\left(r_{oM2} \| R_{inCG}\right) \tag{4.69}$$

$$\tau_{gs2} \cong C_{gs2} R_L \tag{4.70}$$

and, finally,

$$\tau_L \cong C_l R_L \tag{4.71}$$

As a result, the bandwidth estimation is

$$BW \cong \frac{1}{\tau_{total}} = \frac{1}{\tau_{gs1} + \tau_{gd1} + \tau_{gs2} + \tau_{gd2}} \tag{4.72}$$

$$= \frac{1}{\left\{C_{gs1} R_S + \left(r_{oM1} \| R_{inCG}\right) + R_S\left(1 + g_{mM1}\left(r_{oM1} \| R_{inCG}\right)\right) + C_{gs2} R_L + C_l R_L\right\}}$$

4.11 BROADBAND AND MULTISTAGE AMPLIFIERS

So far, CASCODE amplifier has been shown a possible topology for UWB applications. Though it gives better performances against single stage topologies, it needs enhancements of gains and bandwidths. In this section various methods will be introduced and analyzed.

4.11.1 CHANNEL LENGTH

Other than that, the simulation result shown below gives the role of MOSFET channel length. One of the ways to have better bandwidth is using short channel length. This section will explain the relations between channel length and frequency bandwidth.

4.11.1.1 UNITY-GAIN FREQUENCY (ω_T)

The unity-gain is defined as the frequency at which the short-circuit current-gain of the common-source configuration become unity. This measurement assumes the steady state operation with sinusoidal excitation. A current source i_{in} is applied to the gate of the device, and the output current i_d is measured in the short-circuited drain circuit.

As previously shown in (4.3) and (4.14) the drain current I_D and the transconductance g_m is given by

$$I_D = \left(\frac{1}{2}\right) K_n' \left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \tag{4.73}$$

$$g_m = K_n' \left(\frac{W}{L}\right)(V_{GS} - V_T) \tag{4.74}$$

Therefore, the current gain $A_i(j\omega)$ is

$$A_i(j\omega) = \frac{i_d}{i_{in}} = \frac{g_m}{j\omega\left(C_{gs} + C_{gd}\right)} \cong \frac{g_m}{j\omega C_{gs}} \tag{4.75}$$

The unity-gain frequency is determined as the frequency where the absolute value of the current gain becomes equal to unity. If

$$\left|A_i(j\omega)\right| = 1 \tag{4.76}$$

Then

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{K_n'\left(\frac{W}{L}\right)(V_{GS} - V_T)}{\left(\frac{2}{3}\right)WLC_{ox}} \tag{4.77}$$

The result (4.77) shows that $\omega_T \propto \frac{1}{L^2}$, i.e. that for high-frequency operation the device should be short and that $\omega_T \propto (V_{GS} - V_T)$. The second proportionality means that to amplify high frequencies the device has to carry a heavy current. However, increasing power is not always possible especially for the mobile communications, etc. Therefore, using short channel transistors are much better solution [14].

4.11.2 SHUNT-PEAKING METHOD TO ENHANCE BANDWIDTH

If a transistor is an ideal, then the only elements that control the bandwidth are ***R***, ***L***, and ***C***. It can be represented as in Figure 26. [7]

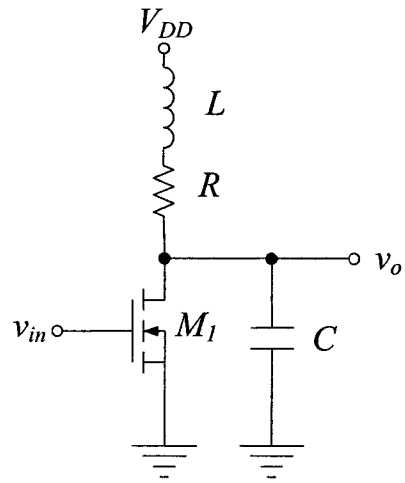

Figure 26 Shunt-peaked amplifier

As previously shown the gain of the amplifier is proportional to $g_m R_L$. The addition of an inductance in series with the load resistor introduces a zero. Therefore the impedance of the ***RLC*** network can be written as

$$Z(s) = (sL + R) \| \frac{1}{sC} = \frac{R\left(s\left(\frac{L}{R}\right) + 1\right)}{s^2 LC + sRC + 1} \tag{4.78}$$

Therefore, the magnitude of Z(s) can be expressed in frequency as follows

$$|Z(j\omega)| = R\sqrt{\frac{\left(\left(\frac{\omega L}{R}\right)^2 + 1\right)}{\left(1 - \omega^2 LC\right)^2 + (\omega RC)^2}} \tag{4.79}$$

It shows that the numerator has a term that increases with increasing frequency. In addition, the $1-\omega^2 LC$ term in the denominator contributes to an increase in $|Z(j\omega)|$ for frequencies below the LC resonance as well.

Initially the inductor(s) will be used. However, inductors have some deficiencies of a low Q-factor and occupy a lot of chip area. Therefore, if it is possible, it is preferable not to use those. The solution with trade-offs will be shown later.

4.11.3 CASCADING TOPOLOGY

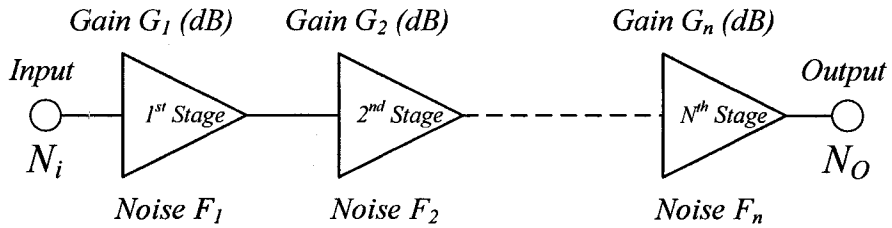

Figure 27 CASCADE topology

As shown in Figure 27 n^{th} transistor stage connected directly to the output of a $(n-1)^{th}$ stage. Therefore, there will be several major elements to be considered for designing amplifiers with CASCADE topology as follows.

- Change of overall power (voltage) gain
- Change of overall Noise Figure
- Change of IP3
- Change of overall frequency response

For convenient, only dual-stage performance parameters will be analyzed for the following sub-sections.

4.12 OVERALL GAIN, NOISE FIGURE, AND IP3 EFFECT

4.12.1.1 OVERALL GAIN

At first, to increase power gain, a multistage amplifier circuit such as CASCADE topology should be considered. For cascaded circuit (refer to the Figure 27) the total power gain G_{total} of a dual-stage amplifier under linear operating conditions results in an addition of the individual gains G_1 and G_2

$$G_{total}(dB) = G_1(dB) + G_2(dB) \tag{4.80}$$

4.12.1.2 NOISE FIGURE

Noise is a form of background signal. A major part of the noise signal belongs to the input transducer; but other components within the circuit will each contribute noise.

The comparison between the desired signal and noise background are defined quantitatively by the *signal-to-noise* ratio,

$$\frac{S}{N} = \frac{(Signal\ Power)}{(Noise\ Power)} \tag{4.81}$$

The S/N at the output of an amplifier is weaker than it is at the input, due to the fact that the amplifier has components that add noise. Therefore, for a network with gain G, the output noise is then

$$N_O = G(N_i + N_a) \tag{4.82}$$

as if an additional noise source N_a exists at the input. $G \times N_a$ is the extra noise at the output arising from internal elements within the amplifier, sometimes called the equivalent system-noise input.

The definition of noise factor is the ratio

$$F = \frac{N_O}{GN_i} = \frac{N_i + N_a}{N_i} = 1 + \frac{N_a}{N_i} \tag{4.83}$$

The dB form is called "noise figure" NF.

4.12.1.3 CASCADED STAGES

In cascaded stage, each stage contributes noise and has a noise factor and a gain (or loss). The total noise of the system is an equivalent input noise, N_a, as defined in (4.83).

In the cascaded system shown in Figure 27, the total noise in terms of their noise factors and gains.

For the 1st stage, having noise factor F_1 and power gain G_1, the equivalent input noise, according to (4.83), is

$$N_{a1} = N_i F_1 - N_i = N_i (F_1 - 1) \tag{4.84}$$

Similarly, the equivalent input noise at the 2nd stage is $N_{a2}=N_i(F_2-1)$, and at the input noise of the 3rd stage is $N_{a3}=N_i(F_3-1)$, etc. but noise at the input to the 2nd stage represents an equivalent input noise at the 1st stage of

$$N'_{a2} = \frac{N_{a2}}{G_1} \tag{4.85}$$

Therefore, the entire input noise of the dual stage is

$$N_a = N_i (F_1 - 1) + N_i \frac{(F_2 - 1)}{G_1} \tag{4.86}$$

Since $F-(N_i+N_a)/N_i$, then the overall system noise figure is

$$F_{total}(dB) = F_1(dB) + \frac{(F_2(dB) - 1)}{G_1(dB)} \tag{4.87}$$

Where

F_1 and F_2 denote the noise figure of stage 1 and 2.

This process can be extended to more stages in like manner, for which

$$F_{total}(dB) = F_1(dB) + \frac{(F_2(dB) - 1)}{G_1(dB)} + \frac{(F_3(dB) - 1)}{G_1(dB)G_2(dB)} + \frac{(F_4(dB) - 1)}{G_1(dB)G_2(dB)G_3(dB)} + \ldots . \tag{4.88}$$

From (4.88) the gain of the 1st stage should be high enough to decrease total noise figure of the system.

4.13 3RD ORDER INTERCEPT POINT (IP3)

When active devices driven with a large enough RF signal, they will generate undesirable spurious signals. How much spurious generated by the device is dependent on the linearity of the devices.

There are couple of factors which determine the linearity of RF devices, such as 1 dB compressed point (P1dB), Intermodulation distortion (IMD), and 3rd order intercept point (IP3).

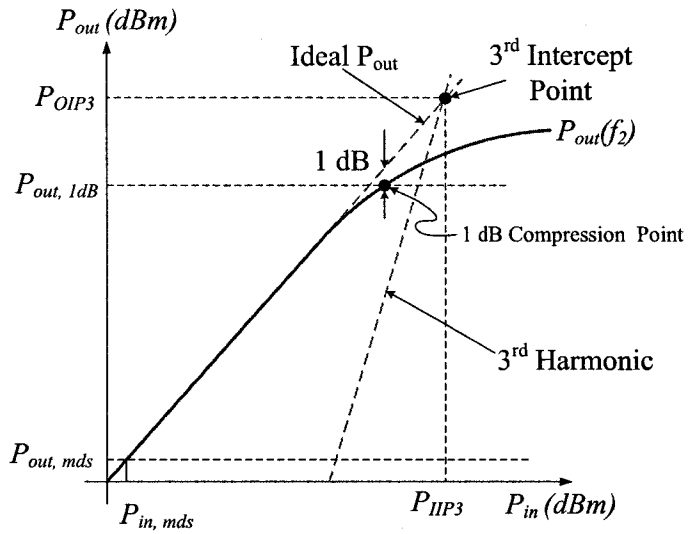

Figure 28 IP3, P1dB, IMD graph

In this section, IP3 will be analyzed how it is being affected by cascading stages as follows.

By definition, IP3 is the point where fundamental power meets IM3 power under the condition that the two power increase without saturating as shown in Figure 28.

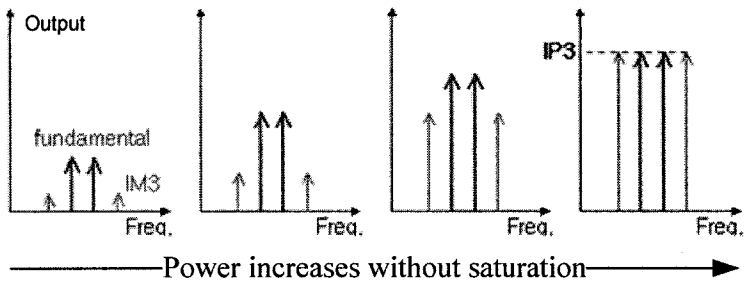

Figure 29 3rd order intercept point (IP3)

In non-linear system, output signal y can be expressed with input signal x as follows

$$y = a + bx + cx^2 + dx^3 + \ldots\ldots \tag{4.89}$$

From (4.89), the IM3 term dx^3 has 3 times slope in dB scale than the fundamental frequency term bx. Therefore, there is an assumed point where they meet each other.

In modern communication systems, the IP3 is a very important criterion to measure the linearity of amplifiers.

From Figure 35, if the minimal detectable signal $P_{in,mds}$ at *3 dB* above thermal noise at the input is given by $P_{in,mds} = kTB+3dB+F_1$, the minimal detectable output power $P_{out,mds}$ becomes [16]

$$P_{out,mds}(dBm) = kTB(dBm) + 3dB + F_{total}(dB) + G_{total}(dB) \tag{4.90}$$

The dynamic properties are also affected. For instance, the third-order intercept point (*IP3*) changes to

$$IP3_{total}(dBm) = \frac{1}{\left(1/IP3_1(dBm)\right) + \left(1/(G_2 IP3_2)(dBm)\right)} \tag{4.91}$$

Where $IP3_1$ and $IP3_2$ are the third order intercept points associated with stage 1 and 2.

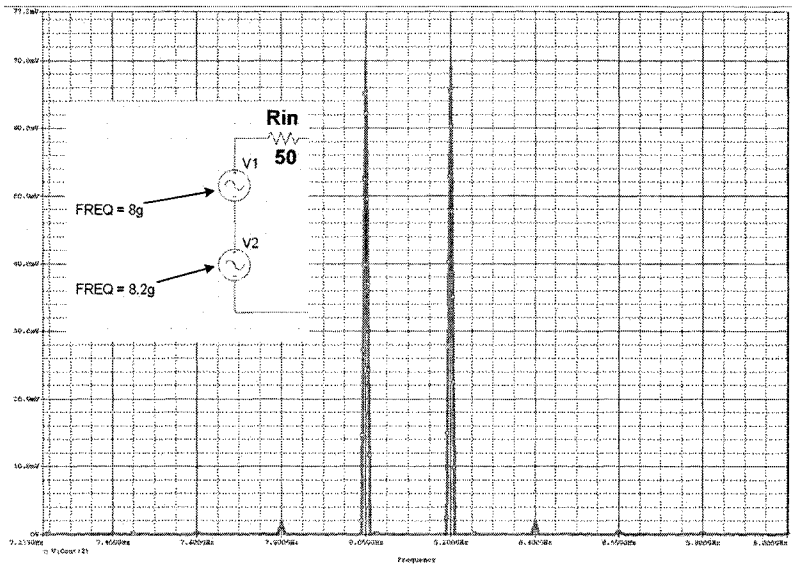

Figure 30 Actual IP3 simulation graph with two different input sources (8 GHz & 8.2 GHz)

4.14 FREQUENCY RESPONSE EFFECTS

Since a $(n+1)^{th}$ stage connected directly to the output of a n^{th} stage, there will be significant change in the overall frequency response mainly because of the capacitances, such as the wiring capacitances, parasitic capacitances, and Miler capacitances, etc.

In case of each stage have a unit DC gain and a single pole of the amplfier's transfer function is then

$$H(S) = \frac{1}{\tau s + 1} \tag{4.92}$$

In a CASCADE that has nth stages have an overall transfer function of

$$A_H(S) = \left(\frac{1}{\tau s + 1}\right)^n \tag{4.93}$$

Solving for -3 dB bandwidth by computing the magnitude of the transfer function is then

$$|A_H(j\omega)| = \left|\left(\frac{1}{\tau s + 1}\right)\right|^n = \frac{1}{\sqrt{2}} \tag{4.94}$$

Therefore, the bandwidth is a as follows

$$\omega = \frac{1}{\tau}\sqrt{\left(2^{(1/n)} - 1\right)} \tag{4.95}$$

Table 4 Bandwidth versus *n*

n	$\sqrt{\left(2^{(1/n)} - 1\right)}$
2	0.64
3	0.51
4	0.43
5	0.39

Therefore, from (4.95) it is necessary to optimize the maximum bandwidth in a cascaded amplifier with a gain requirement.

CHAPTER 5

CONSIDERATIONS OF UWB AMPLIFIER

In this section, standard considerations to meet the main desired quality characteristics shown in Table 5 will be presented.

Table 5 UWB quality characteristics

Target Characteristics	
Frequency Range	3.1 to 10.6 GHz
Minimum Desired Transducer Gain (dB)	10 dB @ 10.6 GHz
Maximum Desired Power Consumption (W)	100 mWatts
Minimum Desired Noise Figure (dB)	< 10 dB
Input/Output resistance	50 ohm

With previous technical considerations, the initial circuit shown in Figure 39 will be used for optimization.

The optimization procedure is as follows.

- Focus on achieving 3 dB bandwidth with a decent Transducer gain
- Eliminate capacitors in the circuit
- Take account the fabrication factor (PAD capacitance in the output port) for Transducer gain

- Eliminate inductors from the circuit

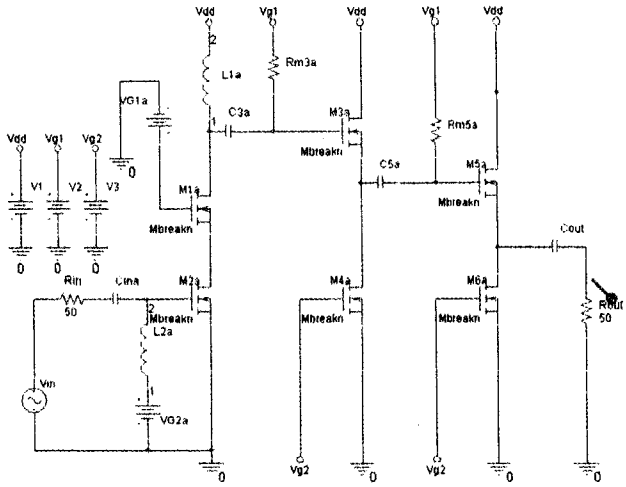

Figure 31 Initial circuit for optimization

With previous technical considerations, such as optimizing the lengths of MOSFETs, bias voltages, and the resistances, the initial circuit shown in Figure 31 has been achieved. The 1st stage is a CASCODE arrangement to provide voltage gain, while the two common drain stages that follow permit driving a 50 ohm load.

5.1 ACHIEVING 3 dB BANDWIDTH THROUGH FEEDBACK TOPOLOGIES

To meet the 3 dB bandwidth criteria, a feedback topology will be used. Negative feedback allows a flat gain response and reduces the input and output VSWR over wide frequency range. An additional advantage of the negative feedback is that it makes the circuit less sensitive to transistor-to-transistor parameter variations. The disadvantage of such circuit is that tend to limit maximum power gain of the transistor and increase its noise figure.

In amplifier design, negative feedback is applied to change gain (desensitize), reduce nonlinear distortion, reduce the effect of noise, control the input and output impedances, and extend the bandwidth with trading off the gain of an amplifier.

For UWB applications, we need to extend bandwidth almost 7 GHz with a decent gain flatness. Therefore, negative feedback will be one of the most important factors.

In this section the properties of negative feedback will be analyzed.

5.2 GAIN DESENSITIZATION

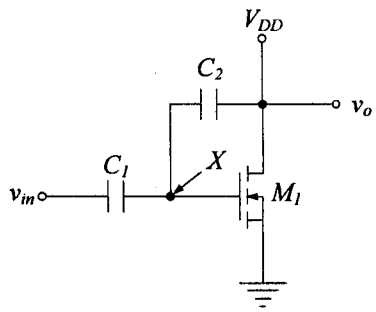

Figure 32 Simple CS amplifier with a feedback

From Figure 32 v_o and v_x are as follows.

$$\frac{v_o}{v_x} = -g_m r_o \tag{5.1}$$

Perform KCL at node X,

$$(v_o - v_x)sC_2 = (v_x - v_{in})sC_1 \tag{5.2}$$

With combining (5.1) and (5.2), we have

$$\frac{v_o}{v_{in}} = -\frac{1}{\left(1 + \frac{1}{g_m r_o}\right)\frac{C_2}{C_1} + \frac{1}{g_m r_o}} \tag{5.3}$$

Since $g_m r_o \gg 1$, (5.3) can be simplified as follows

$$\frac{v_o}{v_{in}} = -\frac{C_1}{C_2} \tag{5.4}$$

From (5.4), it is clear that gain does not depend on g_m and r_o which are variables of process and temperature. Rather, it depends on the ratio of capacitances, which can be avoided of the effects from process and temperature if same materials are used.

5.3 BANDWIDTH EXTENSION

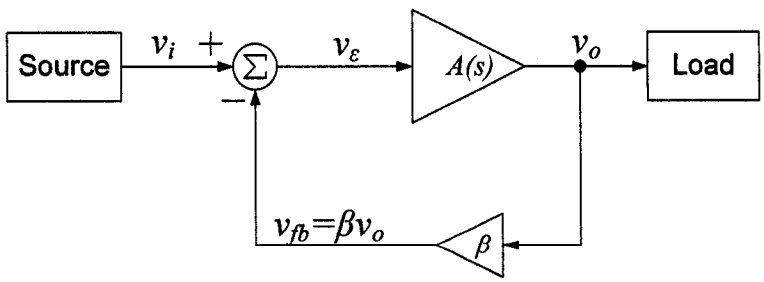

Figure 33 Negative series-shunt feedback amplifier block diagram

From Figure 33, the voltage gain is given by

$$A_f(s) \triangleq \frac{v_o}{v_i} = \frac{A(s)}{1+T(s)} \tag{5.5}$$

Where $T(s)$ is loop gain which is $\beta \cdot A(s)$.

If the amplifier *A(s)* has a single-pole characteristic it can be expressed as follows.

$$A(s) = \frac{A_0}{1-\frac{s}{p_1}} \tag{5.6}$$

Loop gain $T(s)$ is $\beta \cdot A(s)$. Therefore, it can be expressed as follows.

$$T(s) = \frac{\beta \cdot A_0}{1-\frac{s}{p_1}} \tag{5.7}$$

The denominator of (5.5) $(1+T(s))$ is given by

$$1+T(s) = \frac{1-\frac{s}{p_1}}{1-\frac{s}{p_1}} + \frac{\beta \cdot A_0}{1-\frac{s}{p_1}} = \frac{1+\beta \cdot A_0 - \frac{s}{p_1}}{1-\frac{s}{p_1}}$$

$$= (1+\beta \cdot A_0)\left(\frac{1-\frac{s}{p_1(1+\beta \cdot A_0)}}{1-\frac{s}{p_1}} \right) \tag{5.8}$$

Therefore, the denominator $(1+T(s))$ has pole (p_1) and zero $(p_1(1+\beta \cdot A_0))$.

With (5.6) and (5.8), the voltage gain of feedback circuit $(A_f(s))$ is given by

5.4 ELIMINATE CAPACITORS

Cx in Figure 35 represents the parasitic capacitance to ground at the output end of the CASCODE stage. This is a high impedance point so the shunt capacitance is especially critical, and careful layout will be required.

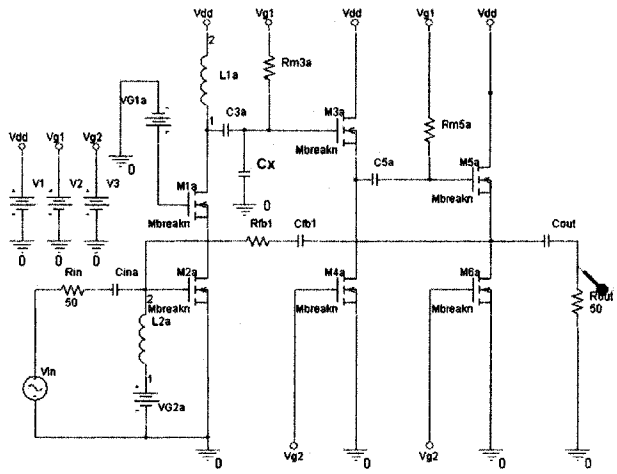

Figure 35 Parasitic capacitance to ground at the output end of the CASCODE stage

The physical implementation of the blocking capacitor (for example, C3a) shown in Figure 35 causes additional Cx which obviously affects the performance of amplifiers. The Figure 36 shows the various transducer gains with different Cx.

The simulation results show that the additional capacitance should be less than 0.001 pF which is not likely to be feasible. Therefore, the blocking capacitors should be removed from the circuit. To remove the capacitors, the initial design has been modified. The modified circuit is shown in the Figure 37.

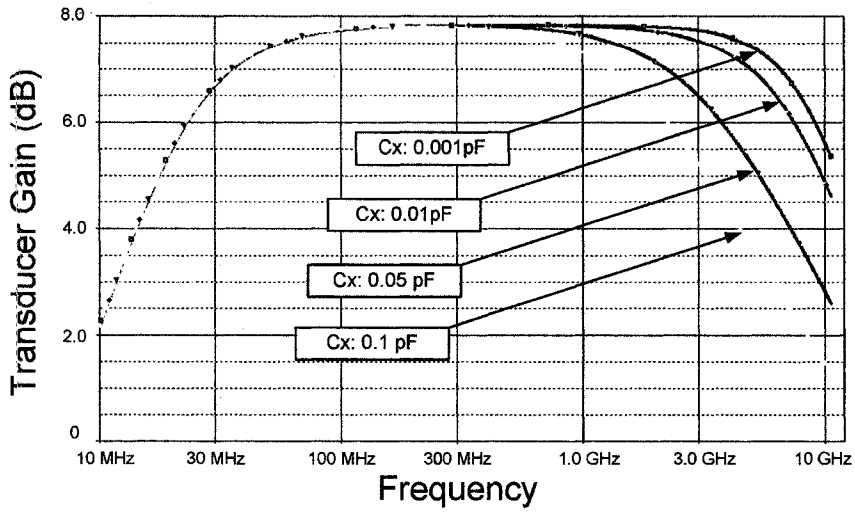

Figure 36 Transducer gain (dB) with different Cx

Two each stage has two more cascaded CASCODE topologies. Though it causes very large power consumption, it is worth while removing the passive elements, such as capacitors.

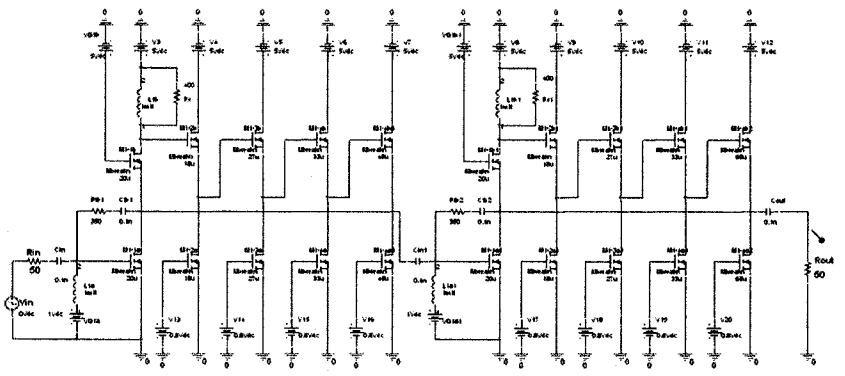

Figure 37 Modified circuit to resolve the capacitor and the Transducer gain issues

Adding more RC negative feedback introduced more poles and zeros which caused the peaking at the high frequency. Though it helps extending frequency bandwidth, the amount of peak should be limited not to exceed certain amount (in this amplifier

design, the limit has been set to +1 dB). To optimize the peaking phenomenon, further study should be done, such as more complicated feedback circuitry, etc.

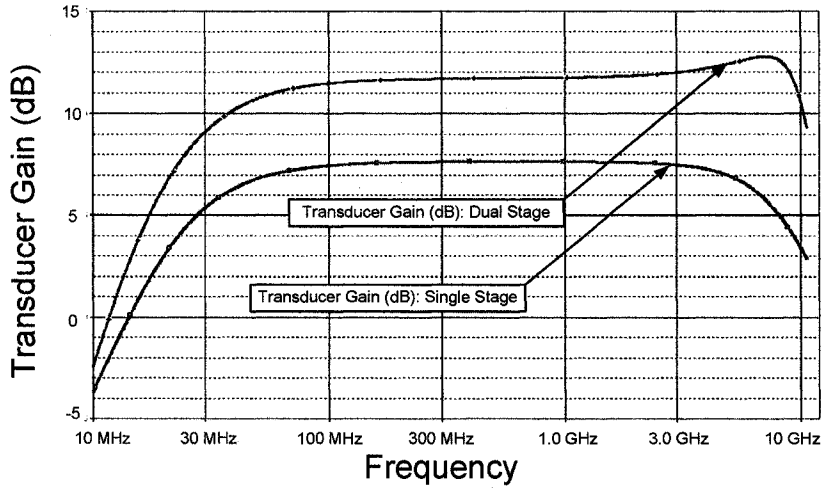

Figure 38 Transducer gain comparison of dual stages and a single stage

5.5 FABRICATION FACTOR (Pad CAPACITANCE)

To meet the desired Transducer gain without the use of blocking capacitors, two more cascades have been added and the whole stage has been extended as shown in Figure 39.

In practice, the pad capacitance is given and cannot be changed. For this reason, it would be better taken account as a factor. Therefore, the Pad capacitance ($C_{pad}(0.4\ pF)$) has been added in the output stage as shown in the Figure 39.

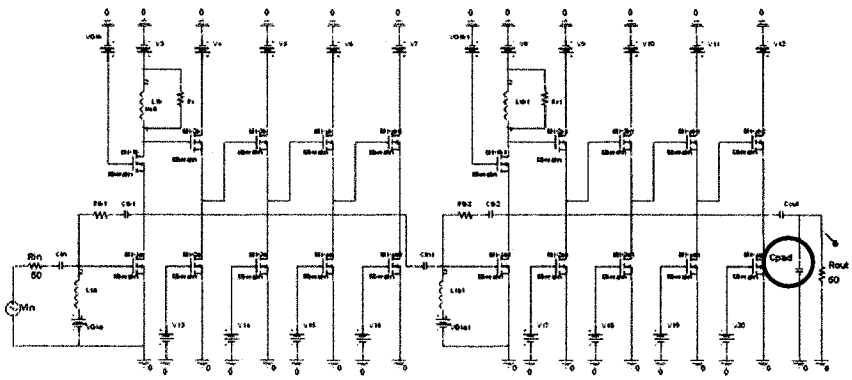

Figure 39 Circuit with a Pad capacitor at the output node

The comparison of the Transducer gains with the Pad capacitance and without Pad capacitance is shown in the Figure 40.

As the Figure 40 shows, the pad capacitance sharply affected the Transducer gain in the higher frequencies. At 10.6 GHz, it made the Transducer gain lower by approximately 1.2 dB which is a great amount in power gain.

Since it degraded the transducer gain mainly in the higher frequencies, it should be taken into account as a known factor for all subsequent simulations.

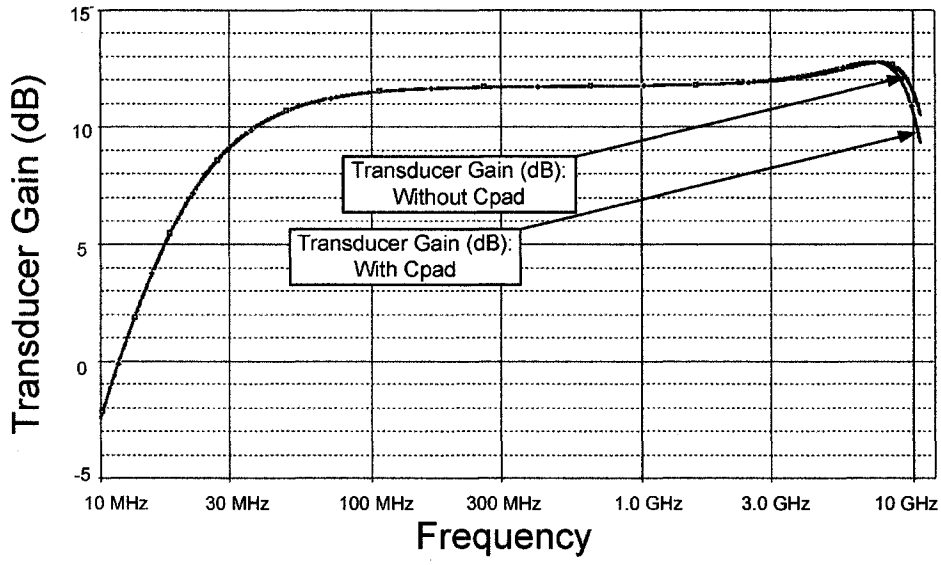

Figure 40 Transducer gain comparison with and without a Pad capacitor

So far, the newly suggested design of the UWB amplifier with minimizing the passive devices, such as resistors and capacitors, proved the achievement of the quality characters shown in the Table 5 (page 72).

5.6 ELIMINATE INDUCTORS

In addition to the passive devices introduces previously, there is one more which plays important role in VLSI.

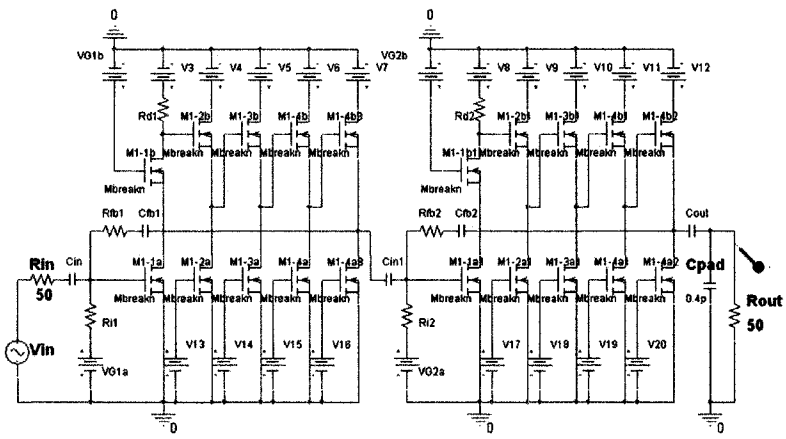

Figure 41 Circuit without inductors

As shown in previous section, inductors help enhancing bandwidth through peaking phenomenon. However, they have a low Q-factor and occupy a lot of chip area. Therefore, in modern VLSI it is highly desirable to limit them.

The Figure 41 shows inductorless circuit and Figure 42 shows the trade-off of the 3 dB bandwidth (3 dB bandwidth achievement: 3.1 GHz to 9.9 GHz), the inductors can be removed successfully.

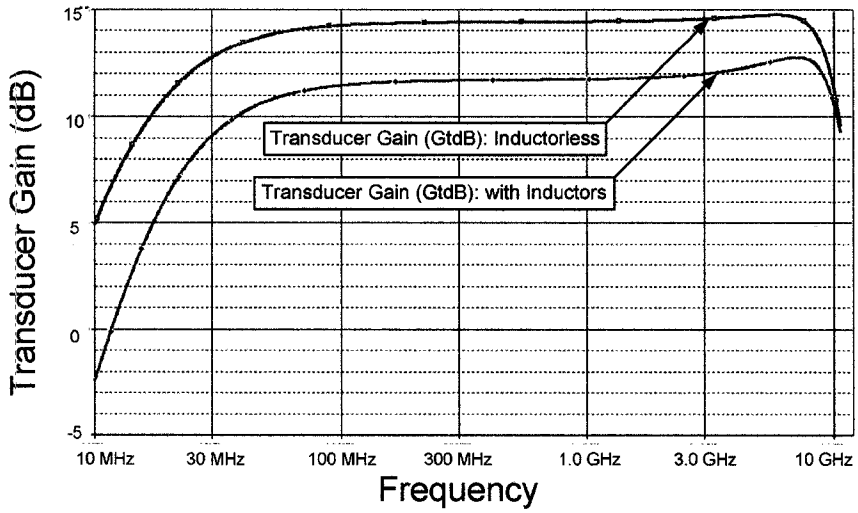

Figure 42 Transducer gain comparison with and without inductors

5.7 FIND THE INPUT IMPEDANCE OF EACH STAGE

In this section, the input impedance of each stage will be analyzed. At first, the impedance of the last stage $\left(Z_{in\_4th}\right)$ with a load resistor R_L in Figure 43 will be calculated. Secondly, the $\left(Z_{in\_1th}\right)$ will be found by generalizing $\left(Z_{in\_4th}\right)$.

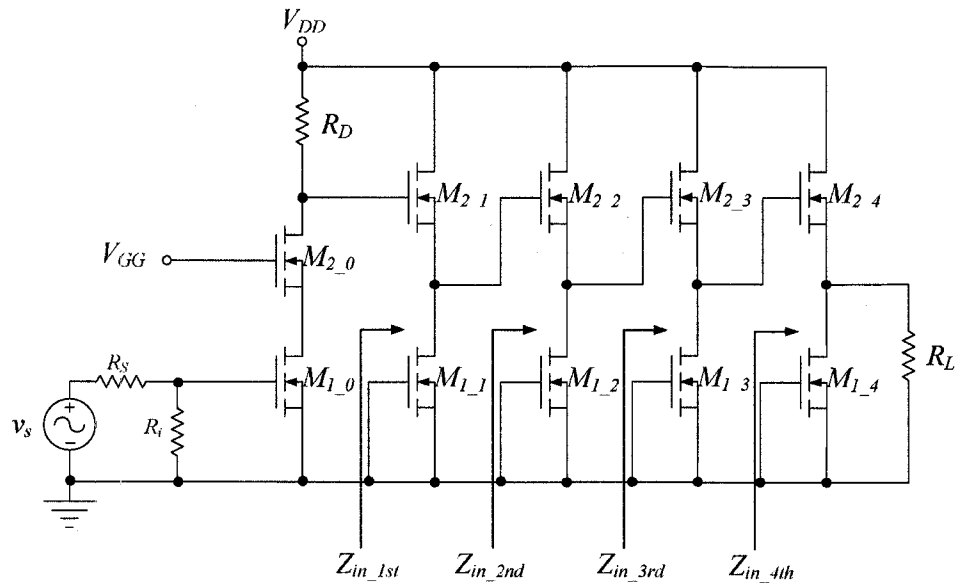

Figure 43 CASCODE total input resistance circuit

5.7.1 FIND Z_{in_nth} with R_L

The 4th circuit for Z_{in_4th} is shown in the Figure 44. For simplification, the output resistors are neglected. There is no current flow in the C_{gsM1_4}. Therefore, the Figure 44 can be simplified as Figure 44.

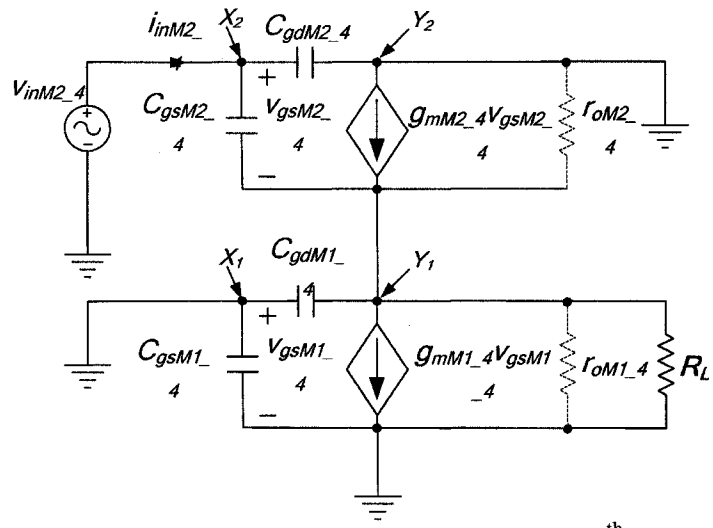

Figure 44 Small signal circuit of the 4th stage

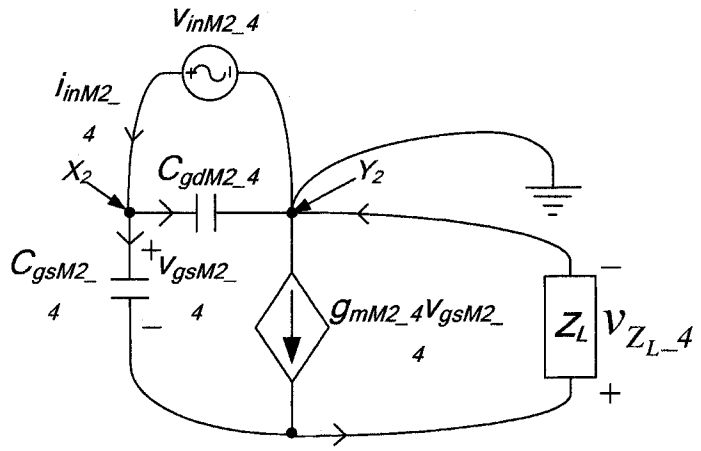

Figure 45 Simplified circuit of Figure 63

Where $Z_L = C_{gdM1\_2} \| R_L$.

At first, the input voltage v_{inM2_4} is as follows.

$$v_{inM2\_4} = v_{gsM2\_4} + v_{Z_L\_4} \tag{5.10}$$

KCL at node X_2 and Y_2 gives as:

$$i_{inM2\_4} = sC_{gdM2\_4} \bullet v_{inM2\_4} + sC_{gsM2\_4} \bullet v_{gsM2\_4} \tag{5.11}$$

$$sC_{gdM2\_4} \bullet v_{inM2\_4} + gZ_L \bullet v_{Z_L\_4} = g_{mM2\_4} \bullet v_{gsM2\_4} \tag{5.12}$$

With applying (5.10) to (5.12) gives as:

$$sC_{gdM2\_4} \bullet v_{inM2\_4} + gZ_L \left(v_{inM2\_4} - v_{gsM2\_4} \right) = g_{mM2\_4} \bullet v_{gsM2\_4}$$

$$\Rightarrow \left(sC_{gdM2\_4} + gZ_L \right) \bullet v_{inM2\_4} = \left(gZ_L + g_{mM2\_4} \right) \bullet v_{gsM2\_4} \qquad (5.13)$$

$$\Rightarrow v_{gsM2\_4} = \frac{\left(sC_{gdM2\_4} + gZ_L \right)}{\left(gZ_L + g_{mM2\_4} \right)} \bullet v_{inM2\_4}$$

With applying (5.13) to (5.11) gives the relationship between the input current and the input voltage of the 4th stage as follows.

$$\begin{aligned} i_{inM2\_4} &= \left(sC_{gdM2\_4} + \frac{sC_{gsM2\_4} \bullet \left(sC_{gdM2\_4} + gZ_L \right)}{\left(gZ_L + g_{mM2\_4} \right)} \right) \bullet v_{inM2\_4} \\ &= \left(\frac{sC_{gdM2\_4} \bullet \left(gZ_L + g_{mM2\_4} \right) + sC_{gsM2\_4} \bullet \left(sC_{gdM2\_4} + gZ_L \right)}{\left(gZ_L + g_{mM2\_4} \right)} \right) \bullet v_{inM2\_4} \\ &= \left(\frac{s\left(gZ_L \bullet \left(C_{gdM2\_4} + C_{gsM2\_4} \right) + C_{gdM2\_4} g_{mM2\_4} \right) + s^2 C_{gsM2\_4} \bullet C_{gdM2\_4}}{\left(gZ_L + g_{mM2\_4} \right)} \right) \bullet v_{inM2\_4} \end{aligned} \qquad (5.14)$$

Therefore, the input impedance of the 4th stage is given as follows.

$$\frac{v_{inM2\_4}}{i_{inM2\_4}} = Z_{in}^{4th} = \frac{1}{\left(\frac{s\left(gZ_L\left(C_{gdM2\_4} + C_{gsM2\_4}\right) + C_{gdM2\_4}g_{mM2\_4}\right) + s^2 C_{gsM2\_4}\bullet C_{gdM2\_4}}{\left(gZ_L + g_{mM2\_4}\right)}\right)}$$

$$= \frac{\left(gZ_L + g_{mM2\_4}\right)}{s\left(gZ_L\left(C_{gdM2\_4} + C_{gsM2\_4}\right) + C_{gdM2\_4}g_{mM2\_4}\right) + s^2 C_{gsM2\_4}\bullet C_{gdM2\_4}}$$

$$= \frac{\left(g_{mM2\_4} + sC_{gdM1\_4} + \frac{1}{R_L}\right)}{s\left(\left(sC_{gdM1\_4} + \frac{1}{R_L}\right)\left(C_{gdM2\_4} + C_{gsM2\_4}\right) + C_{gdM2\_4}g_{mM2\_4}\right) + s^2 C_{gsM2\_4}\bullet C_{gdM2\_4}}$$

$$= \frac{\left(g_{mM2\_4} + sC_{gdM1\_4} + \frac{1}{R_L}\right)}{s\left(sC_{gdM1\_4}\left(C_{gdM2\_4} + C_{gsM2\_4}\right) + \frac{1}{R_L}\left(C_{gdM2\_4} + C_{gsM2\_4}\right) + C_{gdM2\_4}g_{mM2\_4}\right) + s^2 C_{gsM2\_4}\bullet C_{gdM2\_4}} \quad (5.15)$$

$$= \frac{\left(g_{mM2\_4} + sC_{gdM1\_4} + \frac{1}{R_L}\right)}{s\left(C_{gsM2\_4}\bullet\frac{1}{R_L} + C_{gdM2\_4}\left(\frac{1}{R_L} + g_{mM2\_4}\right)\right) + s^2\left(C_{gdM1\_4}\left(C_{gsM2\_4} + C_{gdM2\_4}\right) + C_{gsM2\_4}\bullet C_{gdM2\_4}\right)}$$

Where $gZ_L = sC_{gdM1\_4} + \frac{1}{R_L}$.

From (5.15), it can be extended up to the proposed circuit which has 4th stage as shown below.

$$Z_{in}^{1st} = \frac{\left(g_{mM2\_1} + sC_{gdM1\_1} + \frac{1}{Z_{in}^{2nd}}\right)}{s\left(C_{gsM2\_1}\bullet\frac{1}{Z_{in}^{2nd}} + C_{gdM2\_1}\left(\frac{1}{Z_{in}^{2nd}} + g_{mM2\_1}\right)\right) + s^2\left(C_{gdM1\_1}\left(C_{gsM2\_1} + C_{gdM2\_1}\right) + C_{gsM2\_1}\bullet C_{gdM2\_1}\right)}$$

$$Z_{in}^{2nd} = \frac{\left(g_{mM2\_2} + sC_{gdM1\_2} + \frac{1}{Z_{in}^{3rd}}\right)}{s\left(C_{gsM2\_2}\bullet\frac{1}{Z_{in}^{3rd}} + C_{gdM2\_2}\left(\frac{1}{Z_{in}^{3rd}} + g_{mM2\_2}\right)\right) + s^2\left(C_{gdM1\_2}\left(C_{gsM2\_2} + C_{gdM2\_2}\right) + C_{gsM2\_2}\bullet C_{gdM2\_2}\right)}$$

$$Z_{in}^{3rd} = \frac{\left(g_{mM2\_3} + sC_{gdM1\_3} + \frac{1}{Z_{in}^{4th}}\right)}{s\left(C_{gsM2\_3}\bullet\frac{1}{Z_{in}^{4th}} + C_{gdM2\_3}\left(\frac{1}{Z_{in}^{4th}} + g_{mM2\_3}\right)\right) + s^2\left(C_{gdM1\_3}\left(C_{gsM2\_3} + C_{gdM2\_3}\right) + C_{gsM2\_3}\bullet C_{gdM2\_3}\right)} \quad (5.16)$$

$$Z_{in}^{4th} = \frac{\left(g_{mM2\_4} + sC_{gdM1\_4} + \frac{1}{R_L}\right)}{s\left(C_{gsM2\_4}\bullet\frac{1}{R_L} + C_{gdM2\_4}\left(\frac{1}{R_L} + g_{mM2\_4}\right)\right) + s^2\left(C_{gdM1\_4}\left(C_{gsM2\_4} + C_{gdM2\_4}\right) + C_{gsM2\_4}\bullet C_{gdM2\_4}\right)}$$

When MOSFET operates in saturation region, the capacitances are

$$C_{gs} = W \bullet CGSO + \frac{2}{3} W \bullet L \bullet C_{ox}$$
$$C_{gd} = W \bullet CGDO \tag{5.17}$$

The Z_{in}^{4th} can be simplified as follows.

From (5.17)[18],

$$\begin{aligned} C_{gs} &= W \bullet \left(CGSO + \frac{2}{3} L \bullet C_{ox} \right) \\ &= W \bullet \left(7.9 \times 10^{-10} + \frac{2}{3} \times 0.18 \times 10^{-6} \times 84.2 \times 10^{-6} \right) \\ &= W \bullet \left(7.9 \times 10^{-10} + 10.1 \times 10^{-12} \right) \\ &\cong W \bullet \left(7.9 \times 10^{-10} \right) = W \bullet CGSO \end{aligned} \tag{5.18}$$

Therefore,

$$C_{gs} \cong C_{gd} = \alpha W$$

Where $\alpha = CGSO = CGDO = 7.9 \times 10^{-10}$.

As a result, Z_{in}^{4th} is given

$$Z_{in}^{4th} = \frac{\left(g_{mM2\_4} + s\alpha W_4 + \frac{1}{R_L} \right)}{s\left(\alpha W_4 \bullet \frac{1}{R_L} + \alpha W_4 \left(\frac{1}{R_L} + g_{mM2\_4} \right) \right) + s^2 \left(\alpha W_4 \left(\alpha W_4 + \alpha W_4 \right) + \alpha W_4 \bullet \alpha W_4 \right)} \tag{5.19}$$

$$= \frac{\left(g_{mM2\_4} + s\alpha W_4 + \frac{1}{R_L} \right)}{s\alpha W_4 \left(\frac{2}{R_L} + g_{mM2\_4} \right) + s^2 3a^2 W_4^2} = \frac{\left(s\alpha W_4 + g_{mM2\_4} + 0.02 \right)}{s\alpha W_4 \left(g_{mM2\_4} + 0.04 \right) + s^2 3a^2 W_4^2}$$

Where R_L is 50 ohms.

Therefore, generalized input impedances of each stage given in (5.16) can be rearranged as follows

---

[18] $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\varepsilon_o}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-14}}{4.1 \times 10^{-9}} = 84.2 \times 10^{-6}$

$$Z_{in}^{1st} = \frac{\left(s\alpha W_1 + g_{mM2\_1} + \frac{1}{Z_{in}^{2nd}}\right)}{s^2 3\alpha^2 W_1^2 + s\alpha W_1\left(g_{mM2\_1} + \frac{2}{Z_{in}^{2nd}}\right)}$$

$$Z_{in}^{2nd} = \frac{\left(s\alpha W_2 + g_{mM2\_2} + \frac{1}{Z_{in}^{3rd}}\right)}{s^2 3\alpha^2 W_2^2 + s\alpha W_2\left(g_{mM2\_2} + \frac{2}{Z_{in}^{3rd}}\right)}$$

$$Z_{in}^{3rd} = \frac{\left(s\alpha W_3 + g_{mM2\_3} + \frac{1}{Z_{in}^{4th}}\right)}{s^2 3\alpha^2 W_3^2 + s\alpha W_3\left(g_{mM2\_3} + \frac{2}{Z_{in}^{4th}}\right)}$$

$$Z_{in}^{4th} = \frac{\left(s\alpha W_4 + g_{mM2\_4} + 0.02\right)}{s^2 3\alpha^2 W_4^2 + s\alpha W_4\left(g_{mM2\_4} + 0.04\right)} \qquad (5.20)$$

Where $g_{mM2\_4}\Big|_{M1\_4b8} = 2.24 \times 10^{-2}$, $W_4 = 55\mu m$, and $\alpha = 7.9 \times 10^{-10}$.

With the values, impedance of each stages are shown below.

$$Z_{in}^{1st} = \frac{\left(1.264 \times 10^{-53}\right)s^4 + \left(1.003 \times 10^{-41}\right)s^3 + \left(2.063 \times 10^{-30}\right)s^2 + \left(2.065 \times 10^{-19}\right)s + \left(1.097 \times 10^{-8}\right)}{\left(1.764 \times 10^{-67}\right)s^5 + \left(1.299 \times 10^{-55}\right)s^4 + \left(2.142 \times 10^{-44}\right)s^3 + \left(1.790 \times 10^{-33}\right)s^2 + \left(6.930 \times 10^{-23}\right)s} \qquad (5.21)$$

$$Z_{in}^{2nd} = \frac{\left(4.157 \times 10^{-40}\right)s^3 + \left(3.003 \times 10^{-28}\right)s^2 + \left(4.433 \times 10^{-17}\right)s + \left(3.235 \times 10^{-6}\right)}{\left(1.001 \times 10^{-53}\right)s^4 + \left(6.724 \times 10^{-42}\right)s^3 + \left(7.653 \times 10^{-31}\right)s^2 + \left(3.557 \times 10^{-20}\right)s}$$

$$Z_{in}^{3rd} = \frac{\left(6.693 \times 10^{-27}\right)s^2 + \left(4.272 \times 10^{-15}\right)s + \left(5.427 \times 10^{-4}\right)}{\left(3.417 \times 10^{-40}\right)s^3 + \left(2.131 \times 10^{-28}\right)s^2 + \left(1.286 \times 10^{-17}\right)s}$$

$$Z_{in}^{4th} = \frac{\left(4.345 \times 10^{-14}\right)s + \left(4.240 \times 10^{-2}\right)}{\left(5.664 \times 10^{-27}\right)s^2 + \left(2.711 \times 10^{-15}\right)s}$$

The impedance graphs are shown in Figure 46. It is shown that the input impedance is increased in each stage.

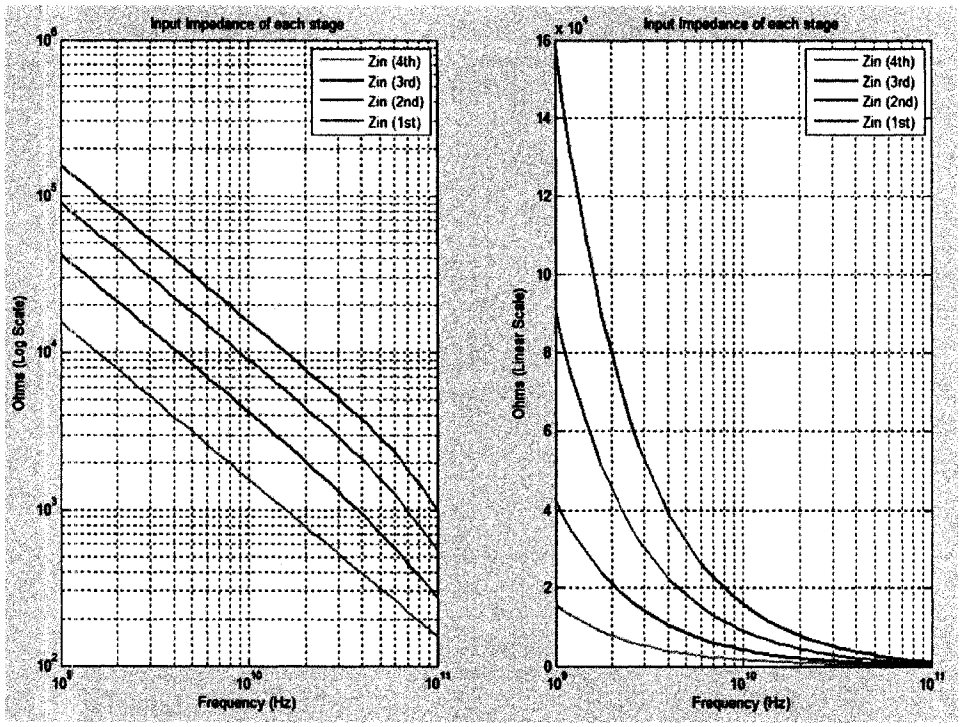

Figure 46 Input Impedance Graphs of each stage

CHAPTER 6

OPTIMIZING UWB AMPLIFIER

In this section, the actual results of optimizing will be represented. At first, optimizing of the initial layout will be shown. Secondly, the 2nd phase with feedback topologies will be shown. Finally, the final inductorless stage will be presented.

6.1 OPTIMIZING INITIAL STAGE

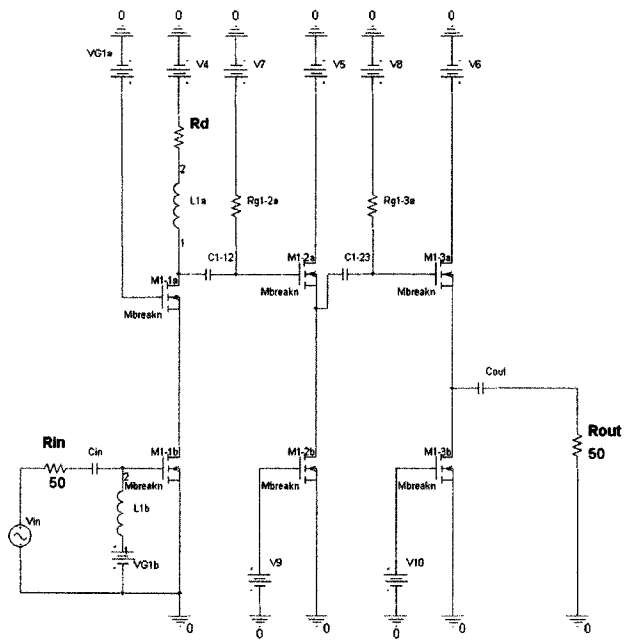

Figure 47 Initial layout

The followings will show the optimization of the initial layout shown in Figure 47. Voltages, width of MOSFETs, and the resistances include the input and output resistance will be represented.

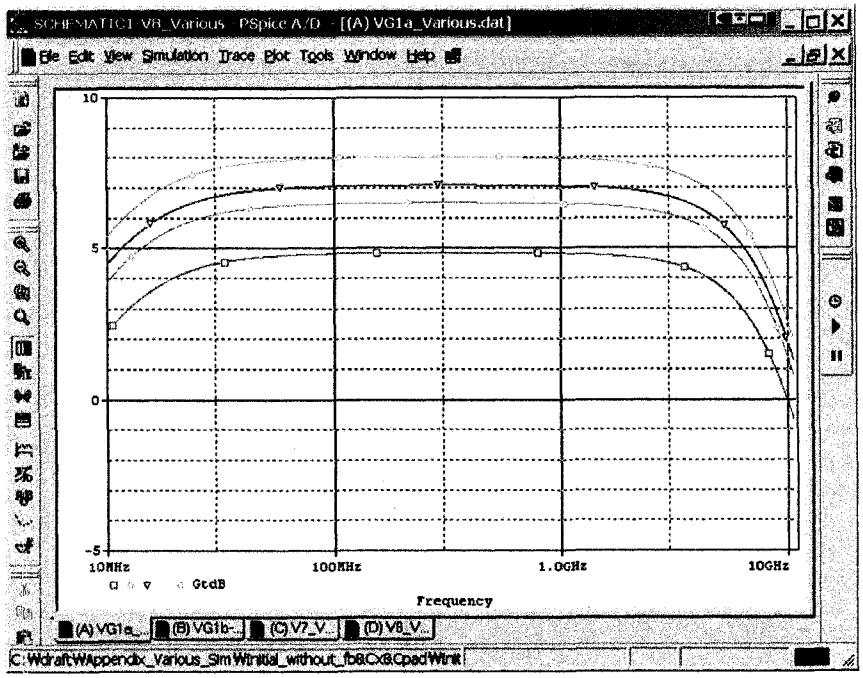

Figure 48 VG1a optimization

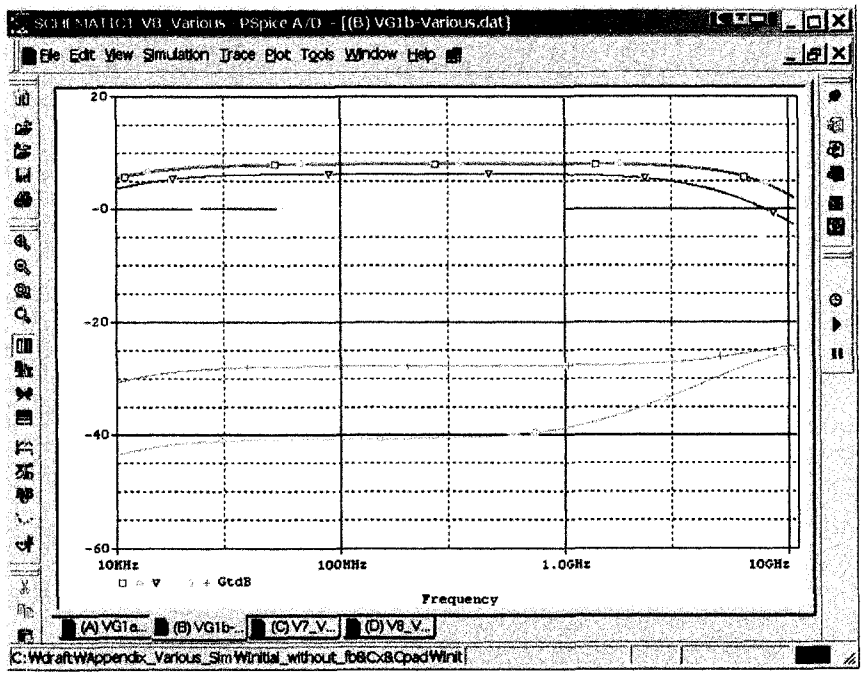

Figure 49 VG1b optimization

From Figure 48, VG1a effects on the overall transducer gain (Gt) of the amplifier.

The highest value is 5 Vdc.

The transducer gain (Gt) is almost same with 0.8 and 1 Vdc. With 1 Vdc, the power consumption is very high. Therefore, 0.8 Vdc is selected.

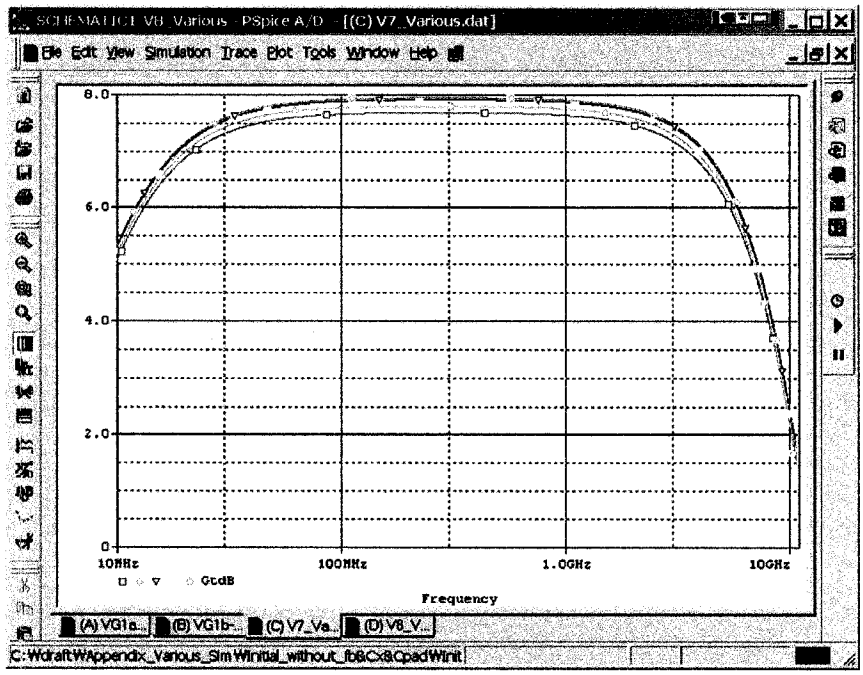

Figure 50 V7 optimization

The transducer gain (Gt) variations are almost same with different V7 and V8 (from 1 Vdc to 5 Vdc). Later, these voltages will be eliminated with blocking capacitors.

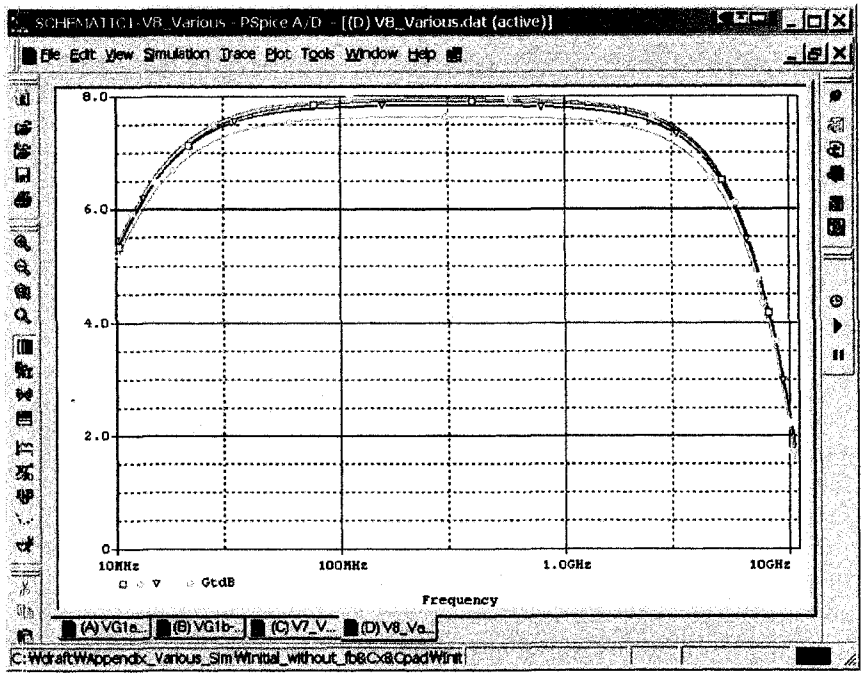

Figure 51 V8 optimization

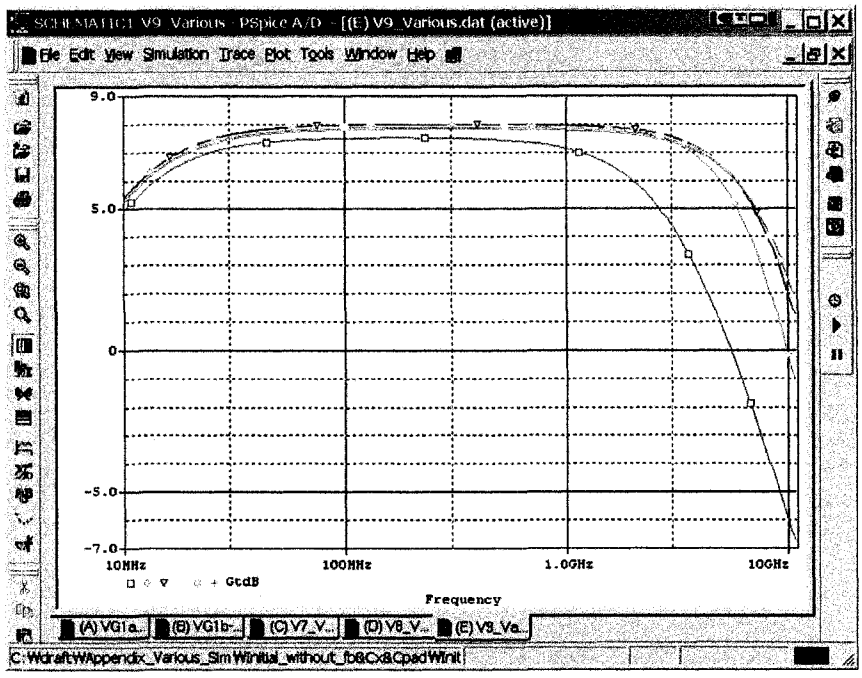

Figure 52 V9 optimization

Unlike previous bias voltages, the V9 shown in Figure 52 affects on the high frequency region very much.

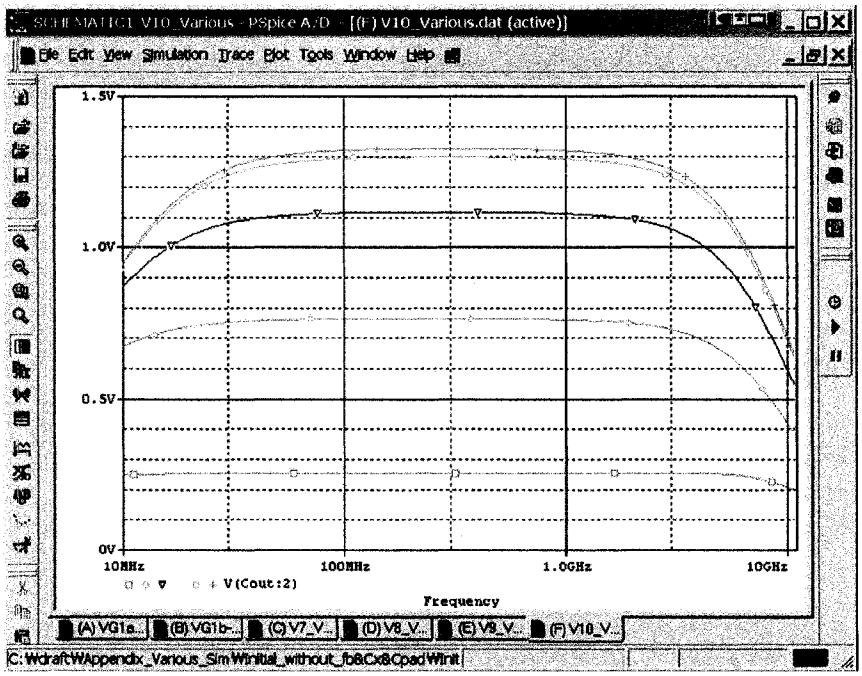

Figure 53 V10 optimization

The bias voltage, V10, affects on the overall the transducer gain.

In addition, these bias voltages remarkably change the drain current.

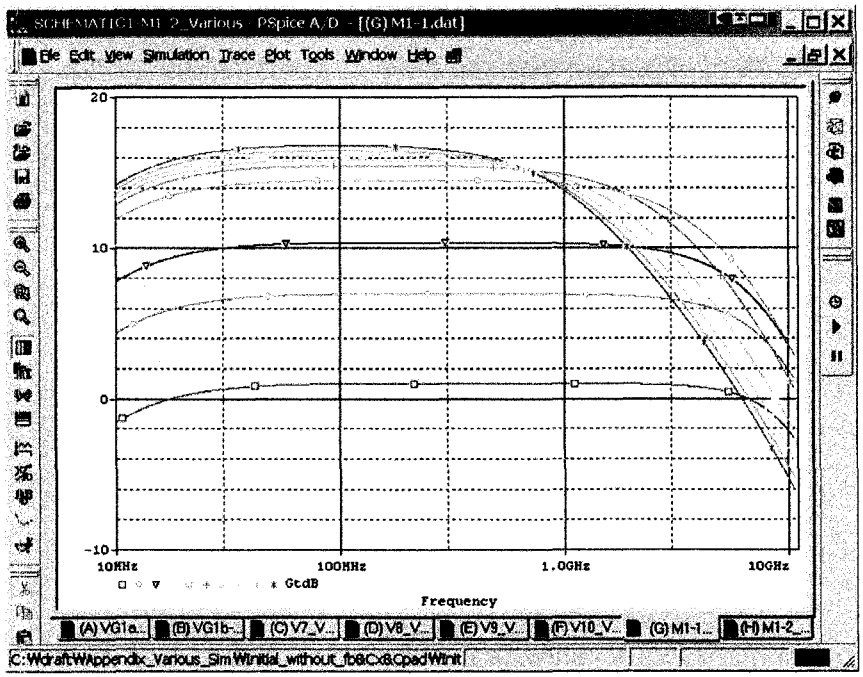

Figure 54 M1-1 width optimization

The width of M1-1 MOSFET affects on the transducer gain (Gt) and the frequency response. An optimized value has been selected with considering the flatness, Gt, power consumption, and the frequency response.

Figure 55 shows that the width of M1-2 affects on the high frequency region frequency response also, the power consumption should be considered for optimization.

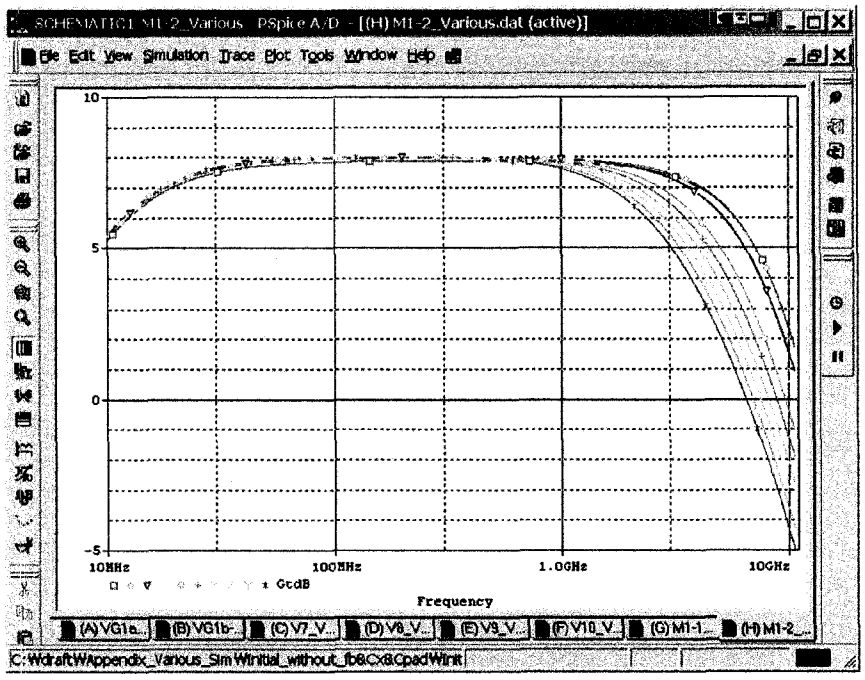

Figure 55 M1-2 width optimization

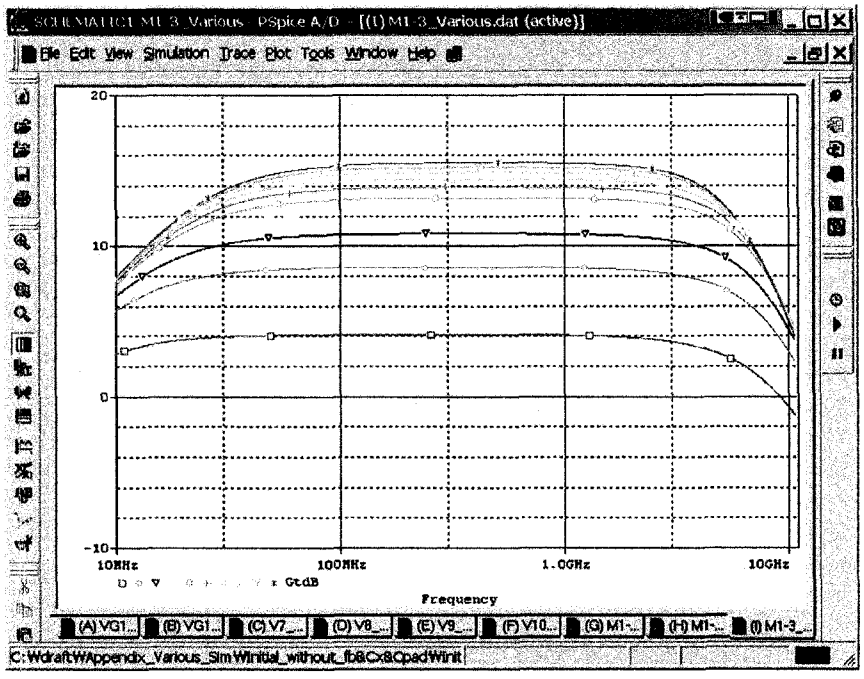

Figure 56 M1-3 width optimization

The width of M1-3 MOSFET affects on the mid-band gain. A best value should be selected with considering the 3 dB bandwidth criteria.

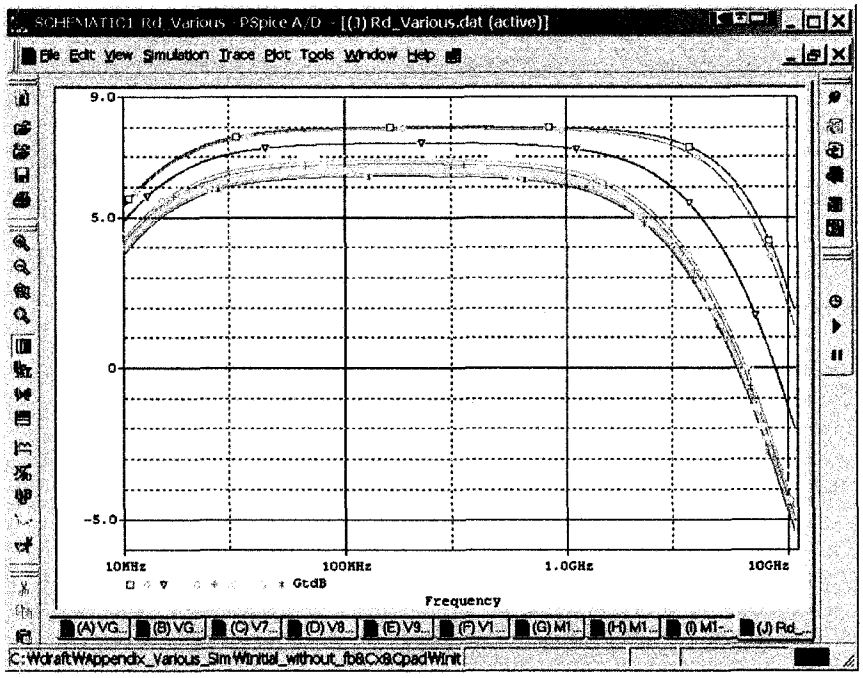

Figure 57 Rd optimization

The Rd affects on the overall transducer gain (Gt) with frequency response. Since it directly affects on the power consumption, proper optimization should be done.

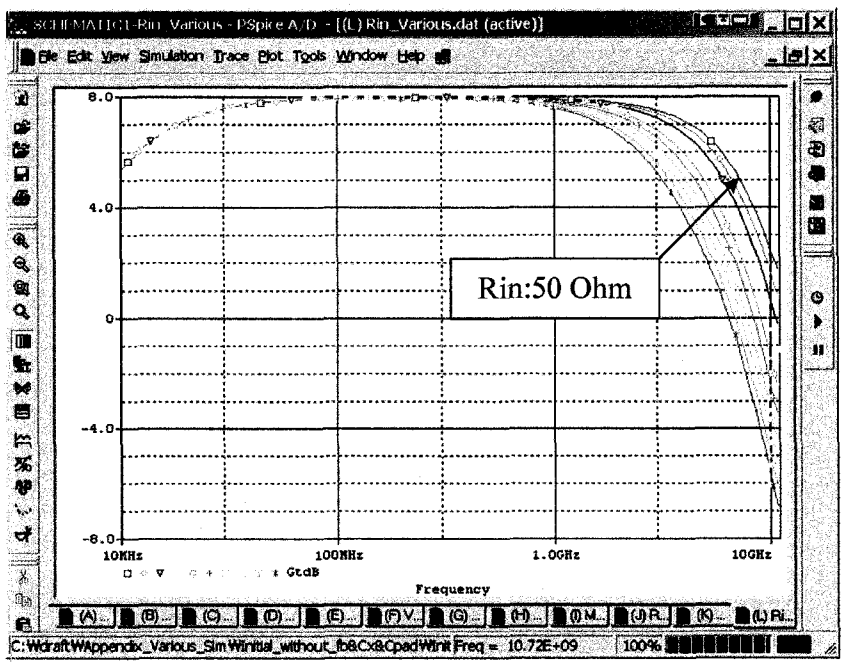

Figure 58 Input resistance

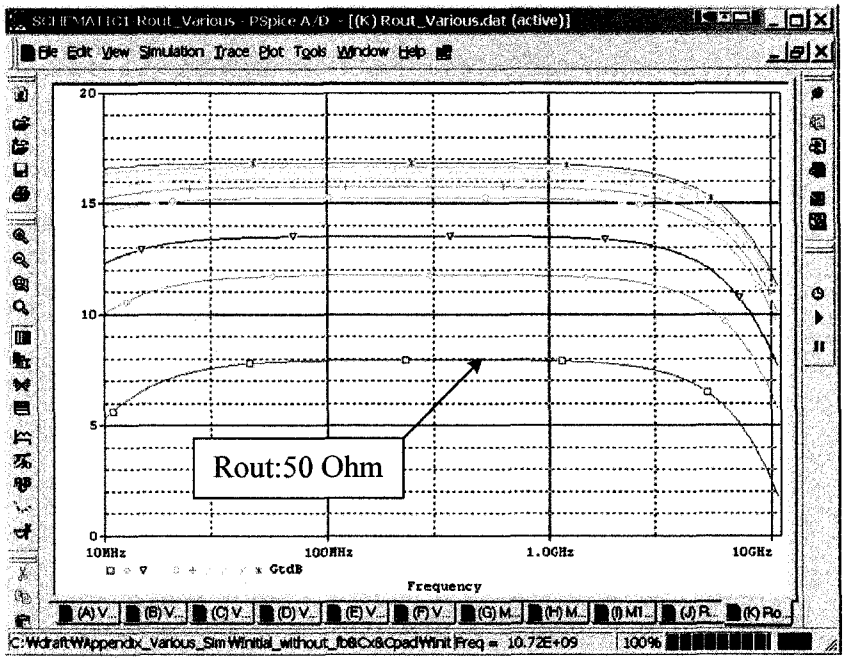

Figure 59 Output resistance

The input resistance shown in Figure 58 mainly affects on the high frequency region frequency response.

Unlikely the input resistance, the output resistance (Figure 59) affects on the overall transducer gain (Gt). This simulation result shows the difficulties to obtain desirable transducer gain (Gt) with 50 ohm output resistance.

6.2 OPTIMIZING 2nd PHASE WITH FEEDBACK TOPOLOGIES

In this section, the optimization with feedback topologies will be shown to achieve 3 dB bandwidth with eliminating blocking capacitors.

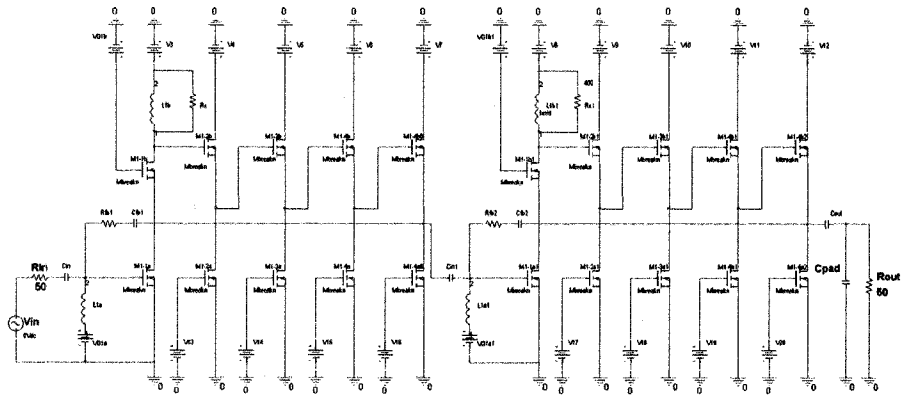

Figure 60 2nd phase layout

Figure 60 shows the 2nd phase layout. This layout shows the elimination of blocking capacitors and feedback topologies to achieve 3 dB bandwidth.

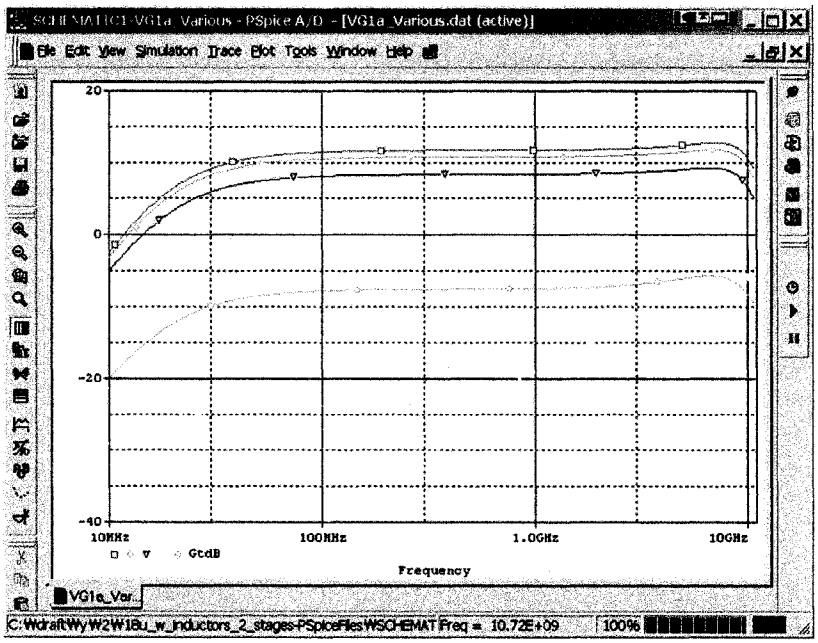

Figure 61 VG1a optimization

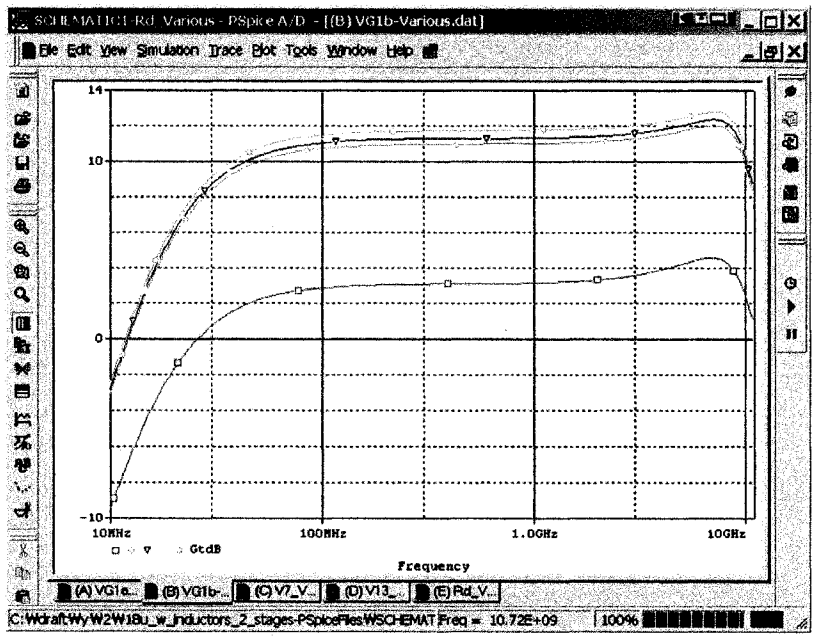

Figure 62 VG1b optimization

VG1a (Figure 61) and VG1b (Figure 62) affect on the overall transducer gain (Gt). Comparing with the VG1a of the initial layout, this graph shows the remarkable improve of frequency response and transducer gain (Gt) with 3 dB bandwidth

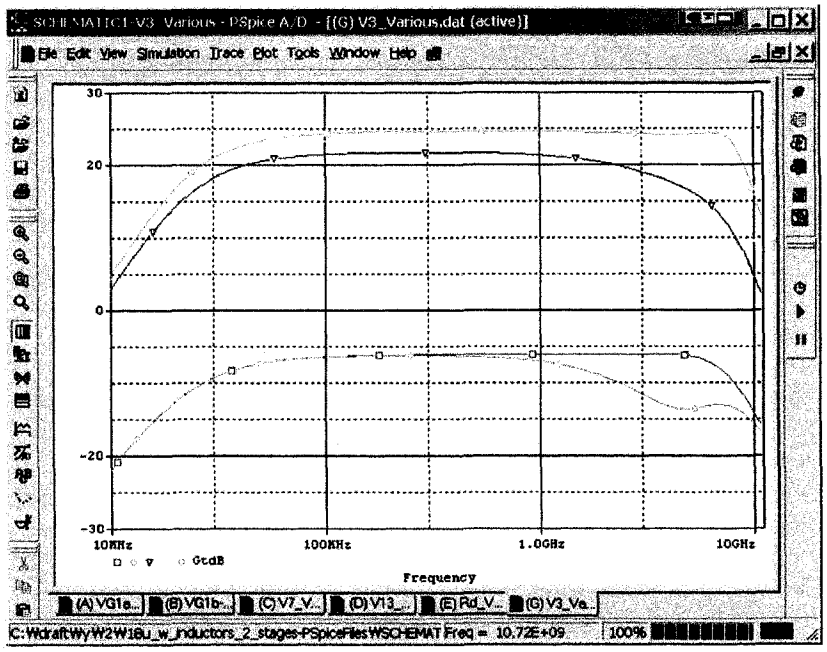

Figure 63 V3 optimization

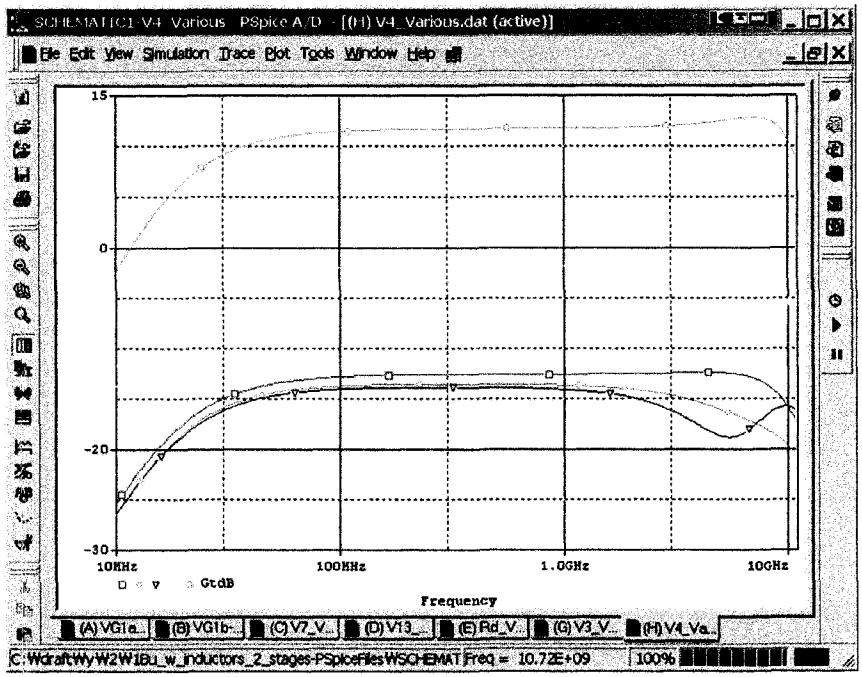

Figure 64 V4 optimization

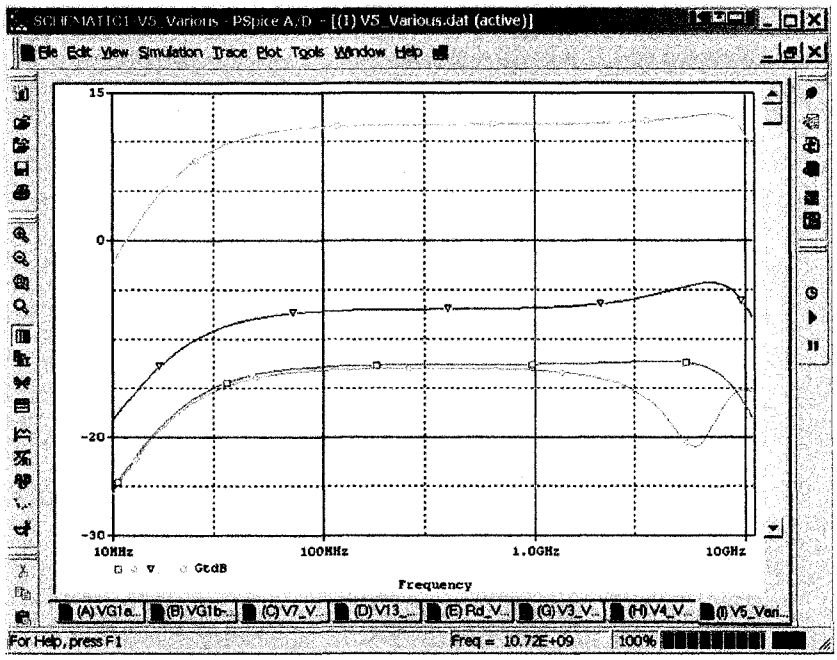

Figure 65 V5 optimization

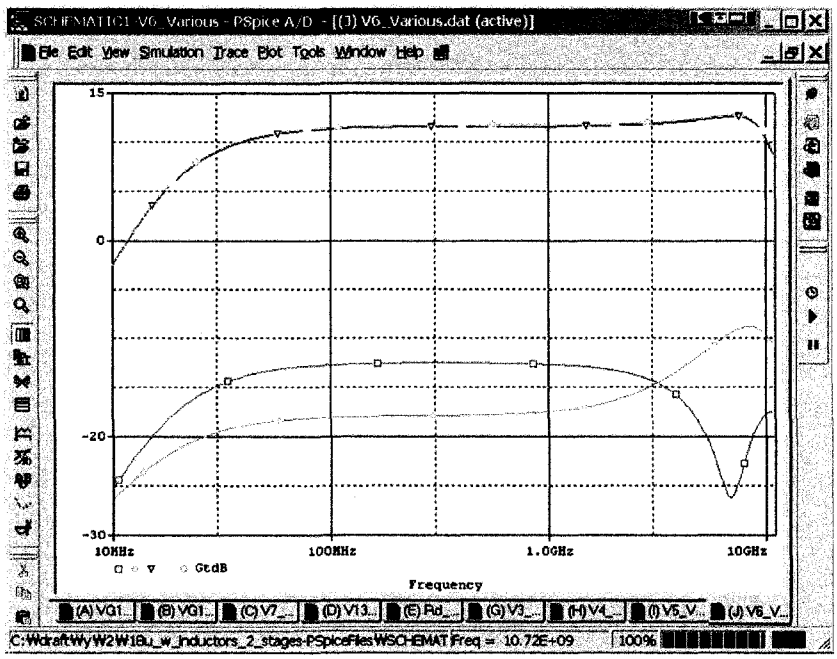

Figure 66 V6 optimization

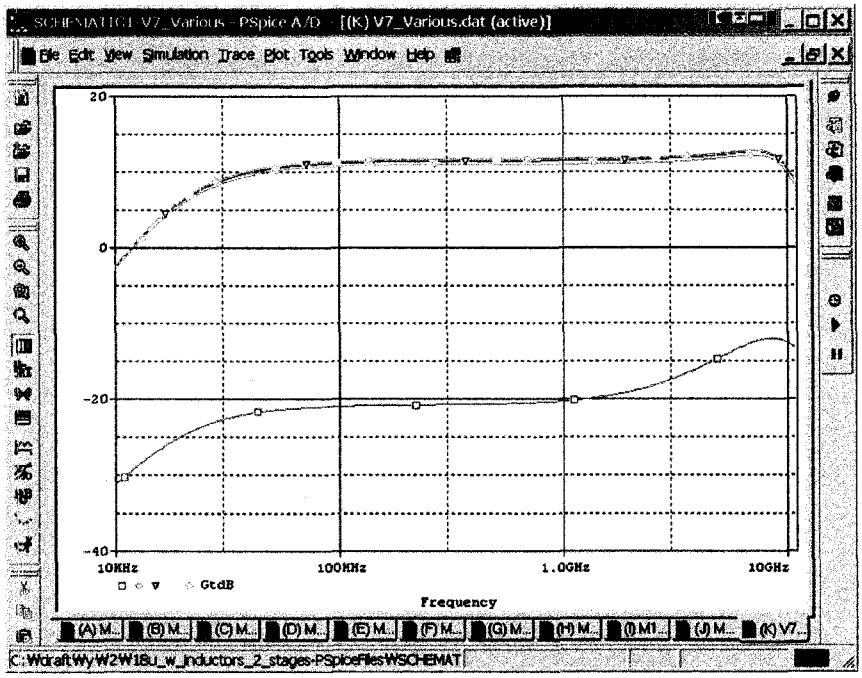

Figure 67 V7 optimization

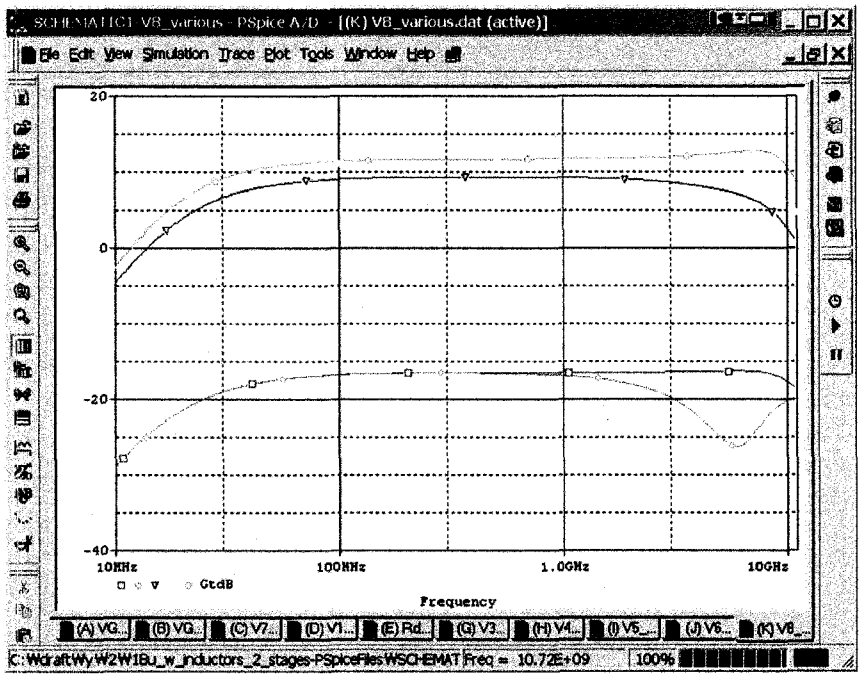

Figure 68 V8 optimization

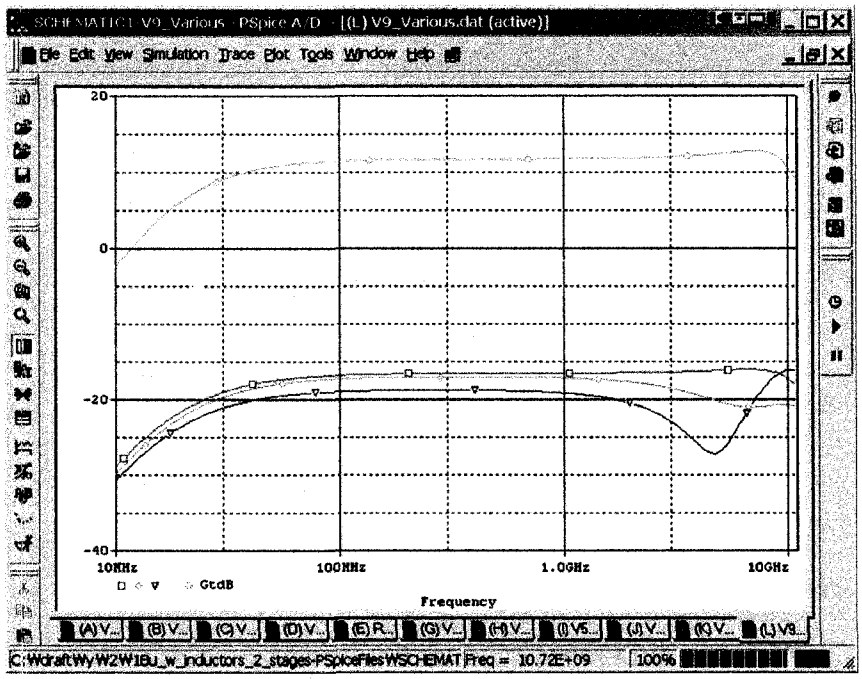

Figure 69 V9 optimization

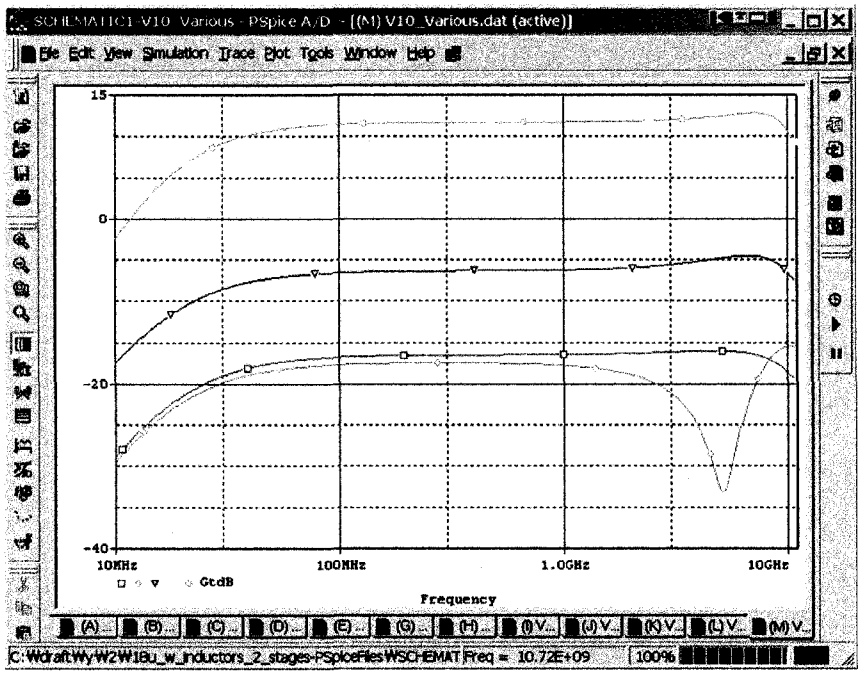

Figure 70 V10 optimization

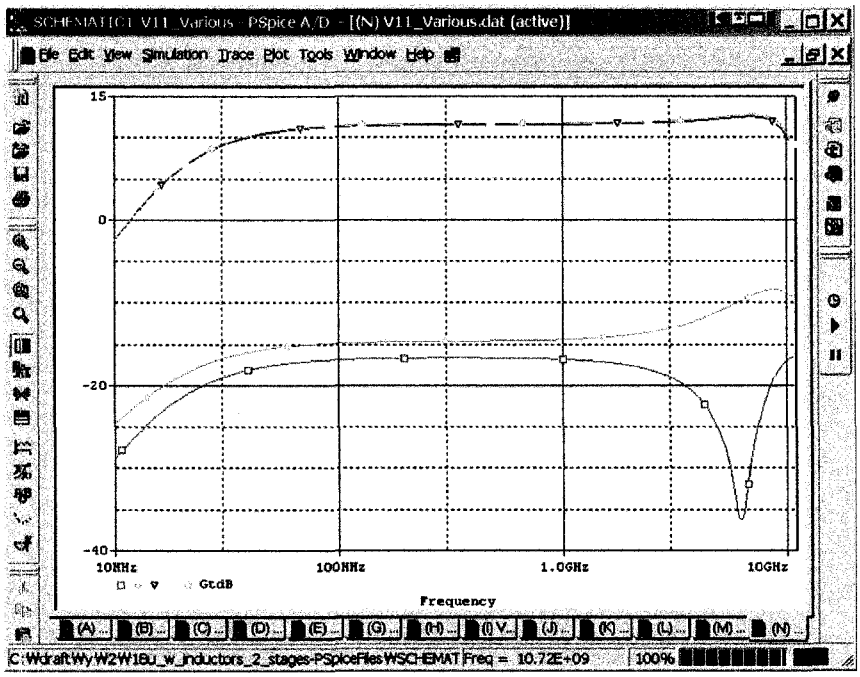

Figure 71 V11 optimization

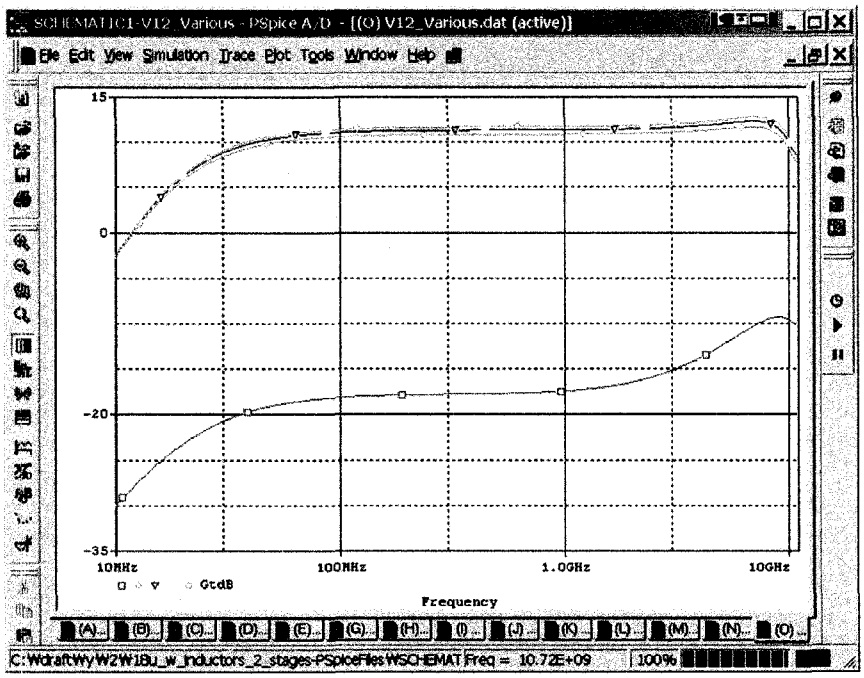

Figure 72 V12 optimization

Table 6 Optimization table of each bias voltage (CG)

Bias Voltage	Effects	Best Values	Remark
V3	Transducer gain (Gt) and frequency response	5 Vdc	
V4			
V5	Transducer gain (Gt)	4 and 5 Vdc	*
V6		3, 4 and 5 Vdc	*
V7		2, 3, 4 and 5 Vdc	*
V8	Transducer gain (Gt) and frequency response	5 Vdc	
V9	Transducer gain (Gt)		
V10		4 and 5 Vdc	*
V11	Transducer gain (Gt)	3, 4 and 5 Vdc	*
V12		2, 3, 4 and 5 Vdc	*

* The lower voltages give lower power consumption. However, using different voltages make the circuit complex. This is a trade-off.

Subsequent graphs show the effect of the bias voltages (from V13 to V20) of the common-source amplifiers of the 2nd phase amplifier.

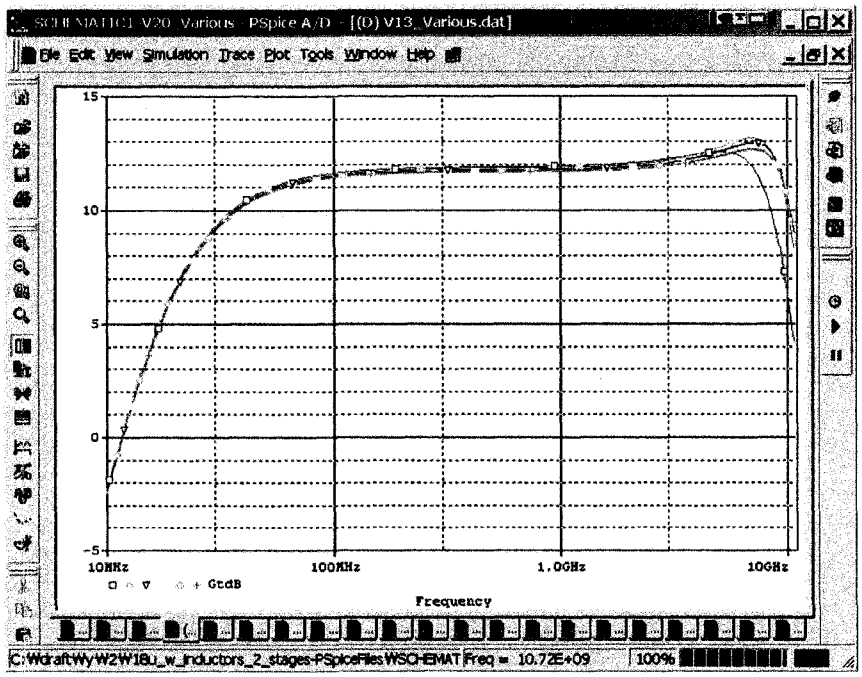

Figure 73 V13 optimization

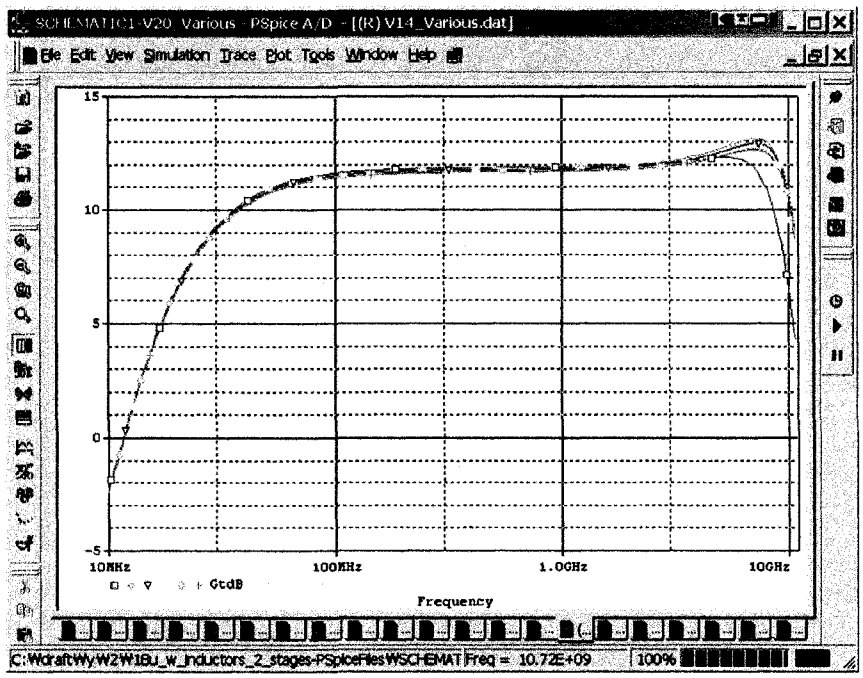

Figure 74 V14 optimization

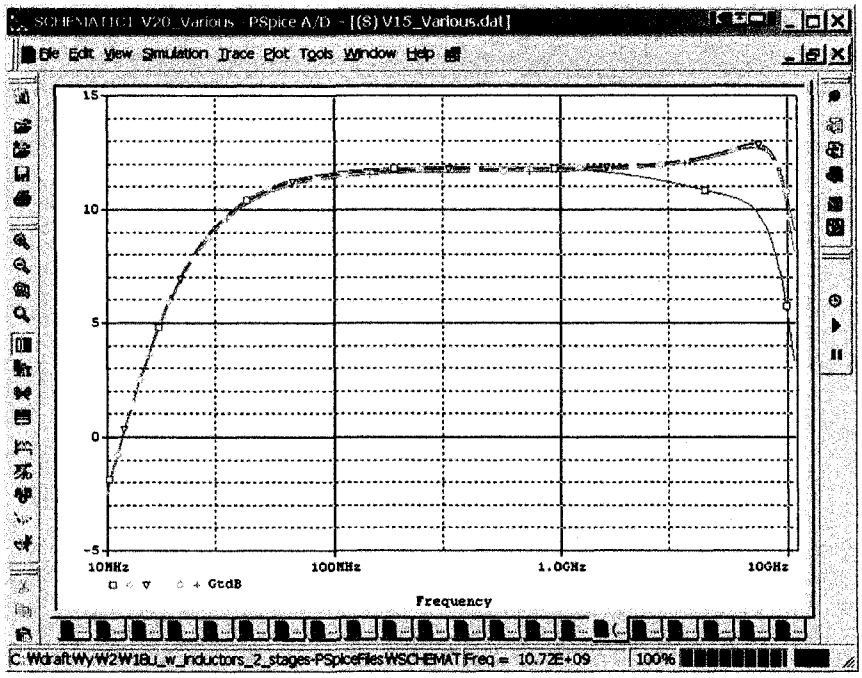

Figure 75 V15 optimization

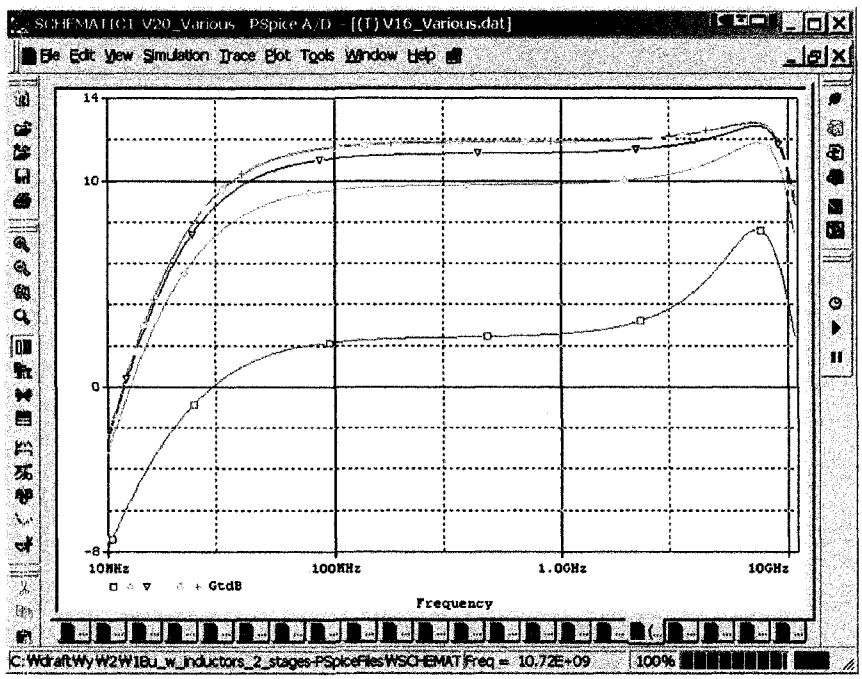

Figure 76 V16 optimization

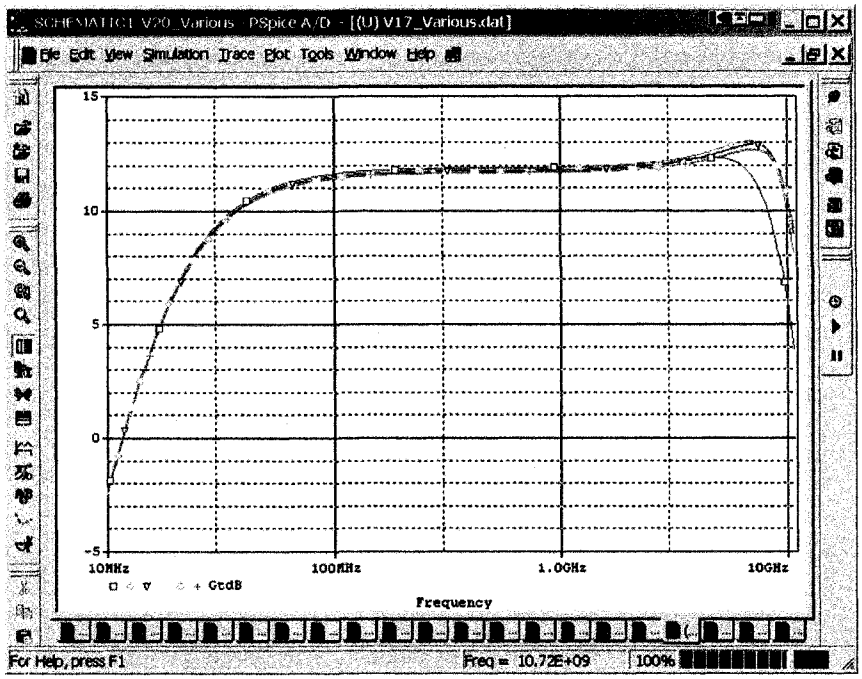

Figure 77 V17 optimization

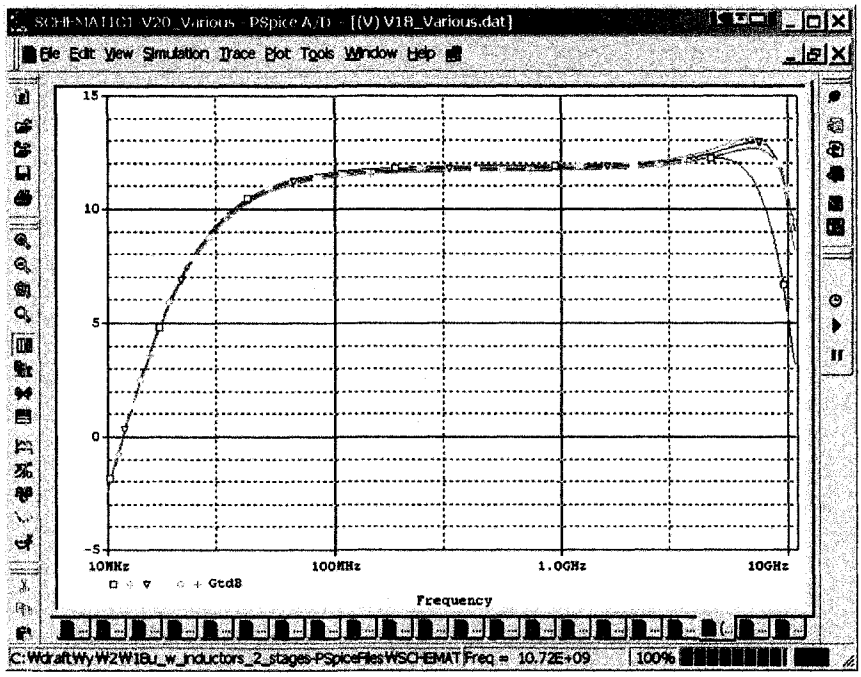

Figure 78 V18 optimization

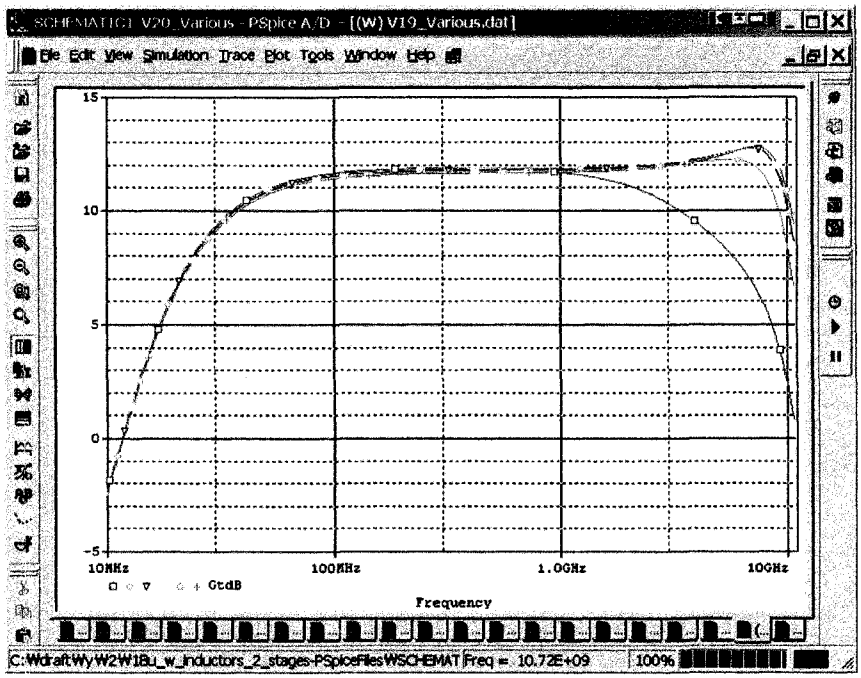

Figure 79 V19 optimization

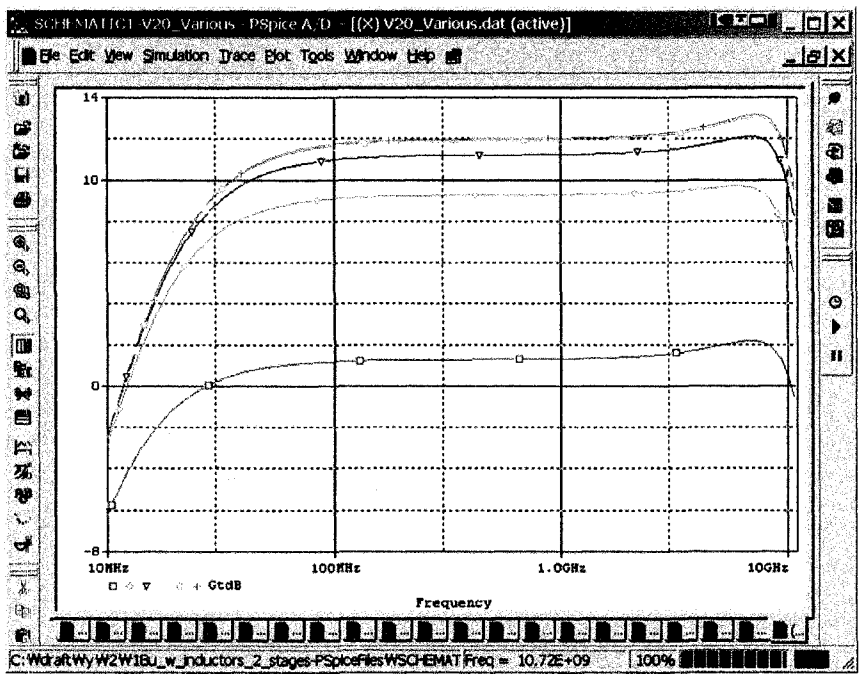

Figure 80 V20 optimization

Table 7 Optimization table of each bias voltage (CS)

Bias Voltage	Effects	Best Values	Remark
V13	Frequency response of high frequency region	0.7 ~ 1.0 Vdc	*
V14		0.6 ~ 1.0 Vdc	*
V15		0.7 ~ 1.0 Vdc	*
V16	Transducer gain (Gt)		*
V17	Frequency response of high frequency region	0.6 ~ 1.0 Vdc	*
V18		0.7 ~ 1.0 Vdc	*
V19		0.8 ~ 1.0 Vdc	*
V20	Transducer gain (Gt)		*

* The lower voltages give lower power consumption. However, using different voltages make the circuit complex. This is a trade-off.

Table 7 shows the effects of each bias voltage of the CS amplifiers of the 2nd phase. Some of them affect on the transducer gain (Gt) and others on the frequency response.

Subsequent graphs show the effect of the MOSFETs width of the 2nd phase amplifier.

The comparisons are shown in the Table 8.

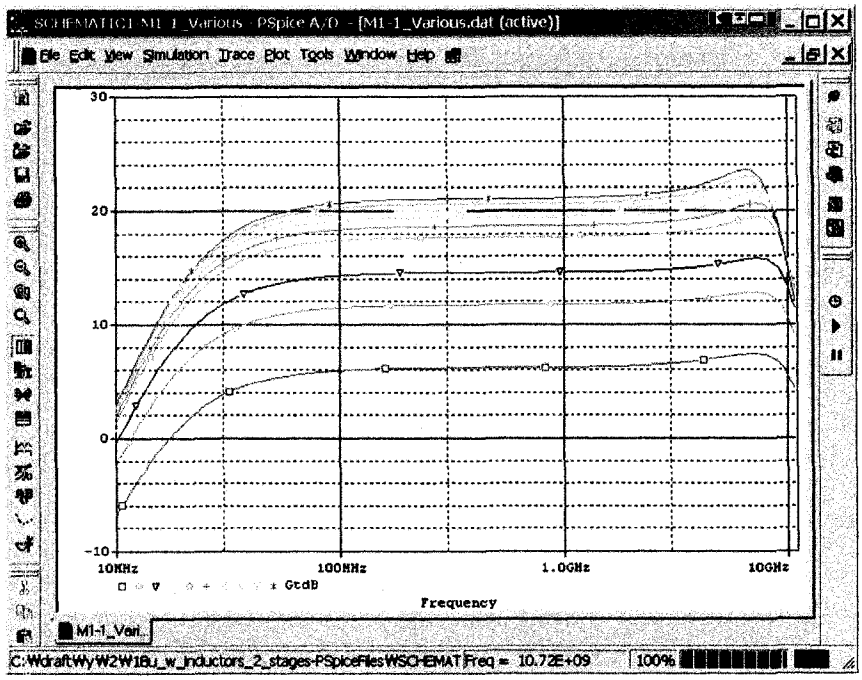

Figure 81 M1-1a & M1-1b MOSFET width optimization

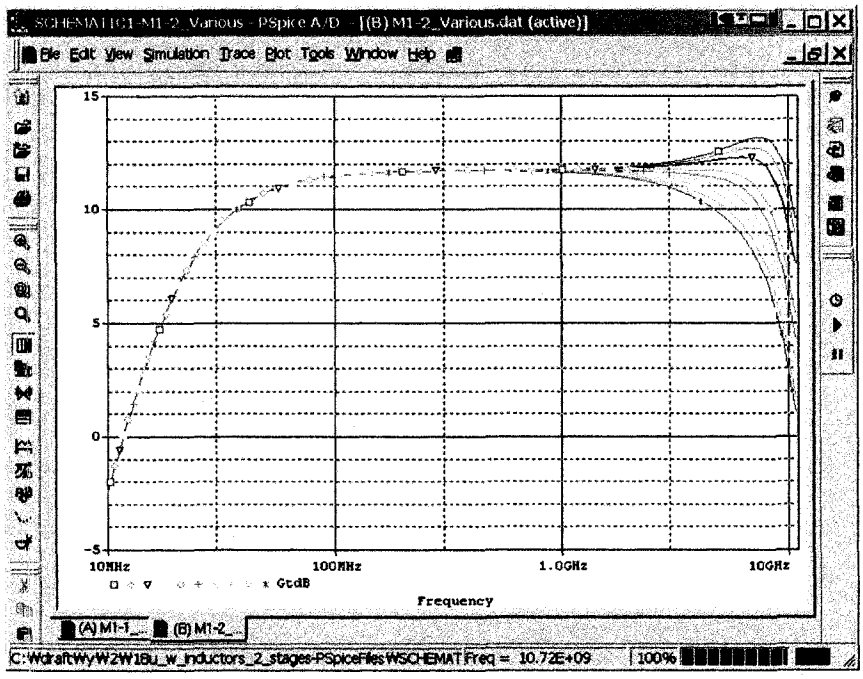

Figure 82 M1-2a and M1-2b MOSFET width optimization

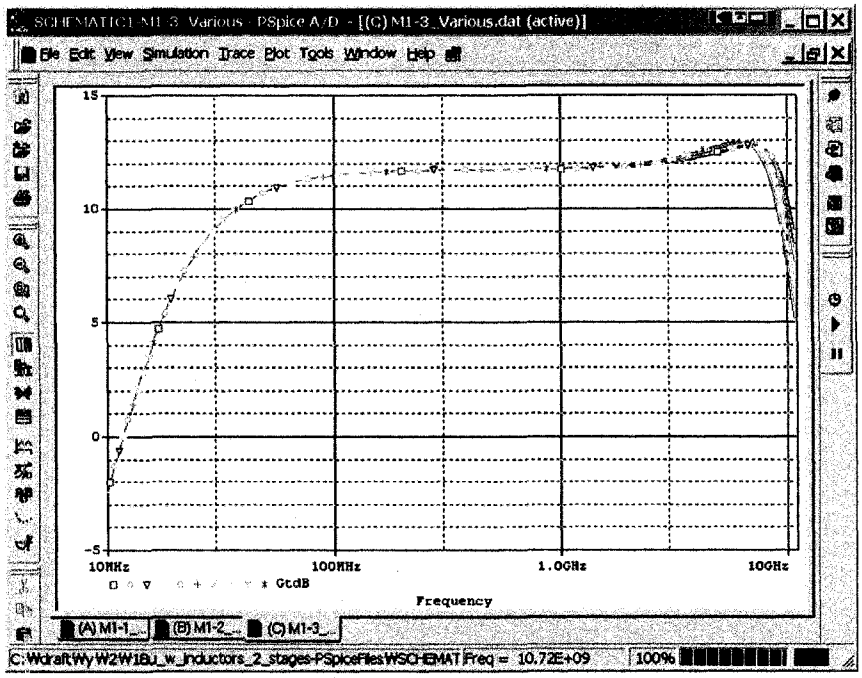

Figure 83 M1-3a and M1-3b MOSFET width optimization

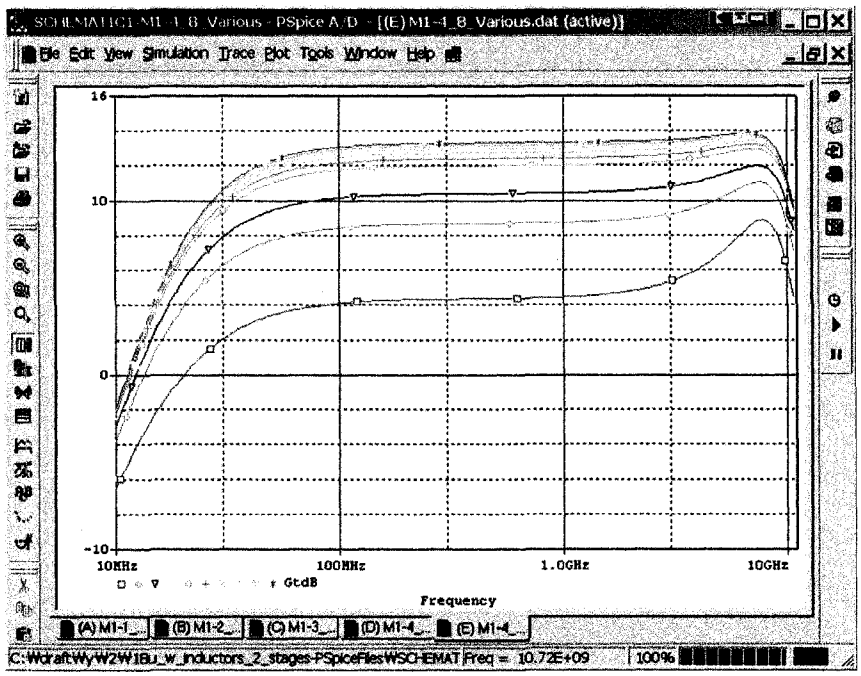

Figure 84 M1-4a8 & M1-4b8 MOSFET width optimization

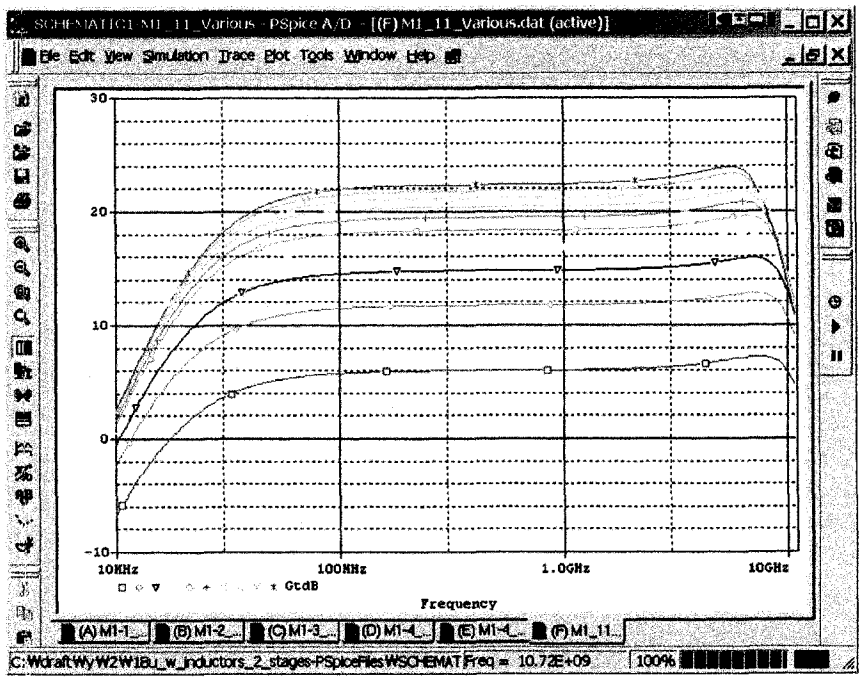

Figure 85 M1-1a1 & M1-1b1 MOSFET width optimization

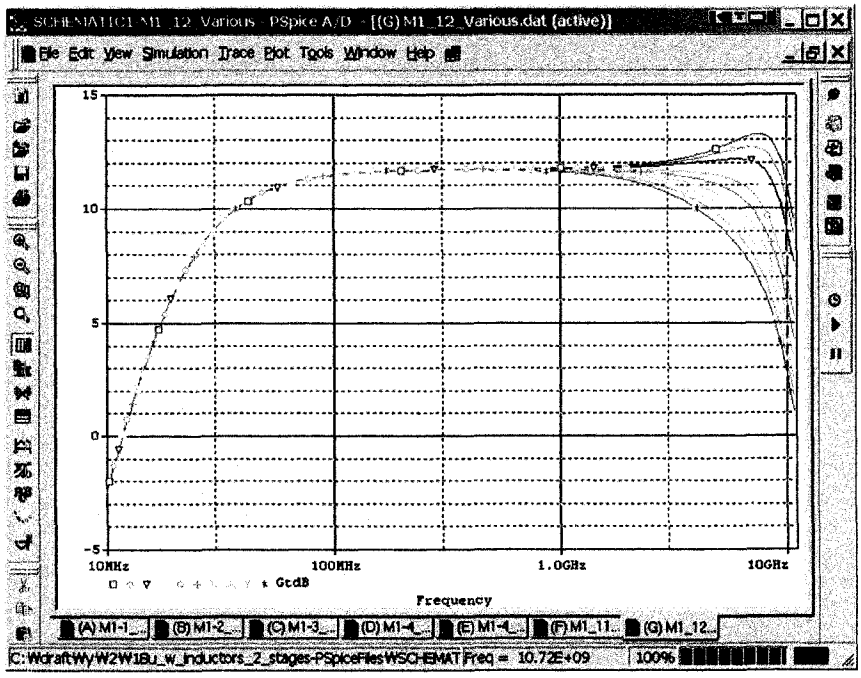

Figure 86 M1-2a1 & M1-2b1 MOSFET width optimization

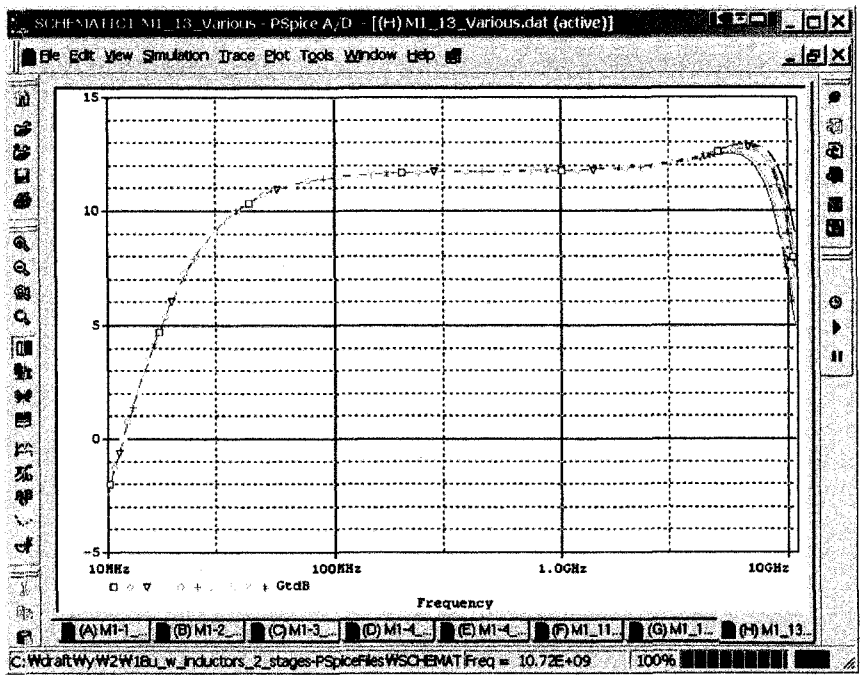

Figure 87 M1-3a1 & M1-3b1 MOSFET width optimization

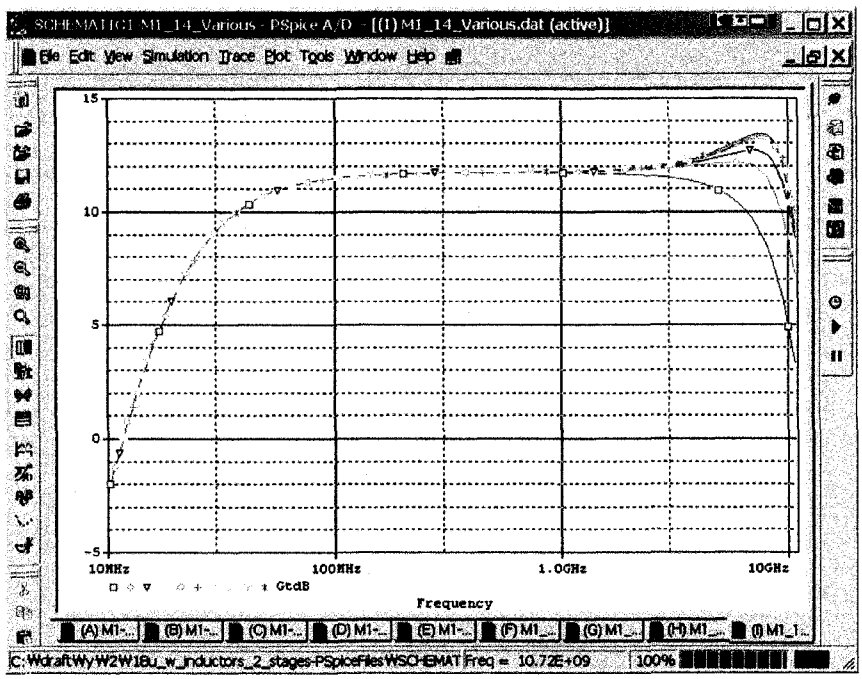

Figure 88 M1-4a1 & M1-4b1 width optimization

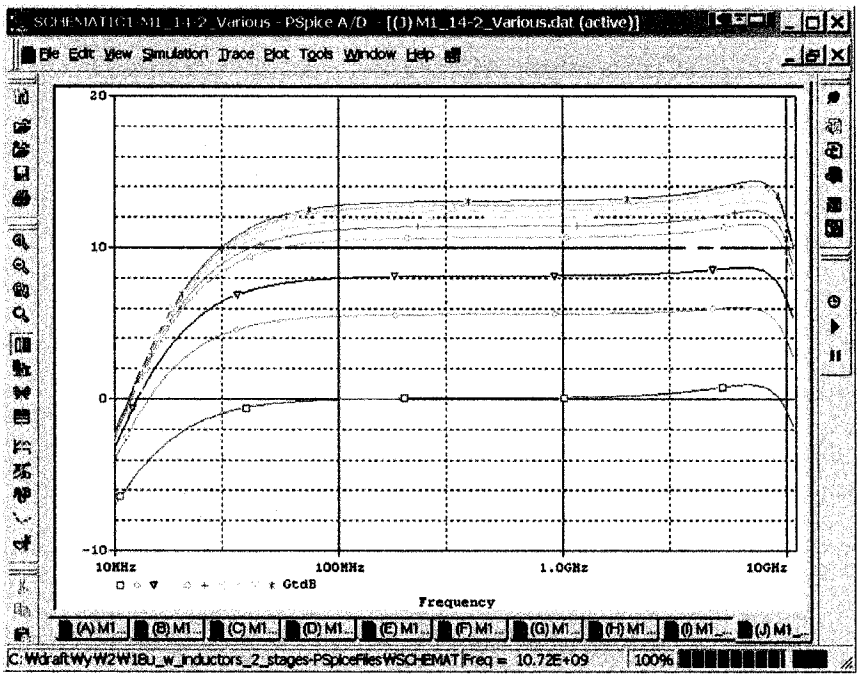

Figure 89 M1-4a2 & M1-4b2 MOSFET width optimization

Table 8 MOSFET width effects comparison table

MOSFET Width	Effects	Remark
M1-1a & M1-1b	Overall transducer gain (Gt). Smaller values give better frequency response.	
M1-2a & M1-2b	Frequency response of high frequency region. Larger value cause peaking.	
M1-3a & M1-3b	Smaller values give better frequency response.	
M1-4a & M1-4b	Some Smaller values give better frequency response at high frequency region.	

M1-4a8 & M1-4b8	Larger values give better transducer gain (Gt) and frequency response. However, power consumption increases.	
M1-1a1 & M1-1b1	Overall transducer gain (Gt). Smaller values give better frequency response.	Similar to M1-1a & M1-1b
M1-2a1 & M1-2b1	Frequency response of high frequency region. Larger value cause peaking.	Similar to M1-2a & M1-2b
M1-3a1 & M1-3b1	Smaller values give better frequency response.	Similar to M1-3a & M1-3b
M1-4a1 & M1-4b1	Some Smaller values give better frequency response at high frequency region.	Similar to M1-4a & M1-4b
M1-4a2 & M1-4b2	Larger values give better transducer gain (Gt) and frequency response. However, power consumption increases.	Similar to M1-4a8 & M1-4b8

Based on the simulation results, wider width does not give better performance always. Sometimes, shorter width gives better performance.

Subsequent graphs will show the effects of Rd, feedback resistances, input, and output resistances.

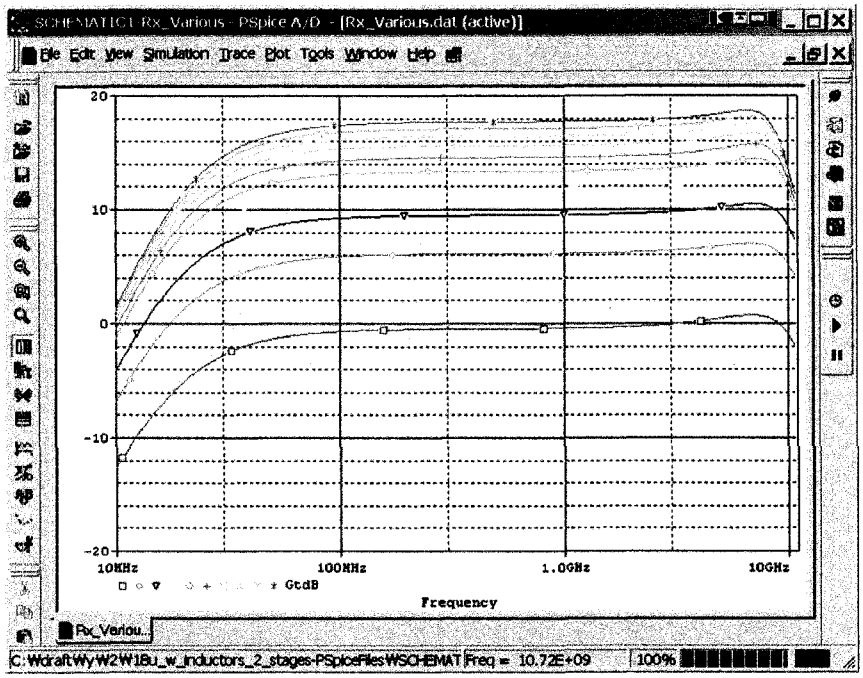

Figure 90 Rx optimization

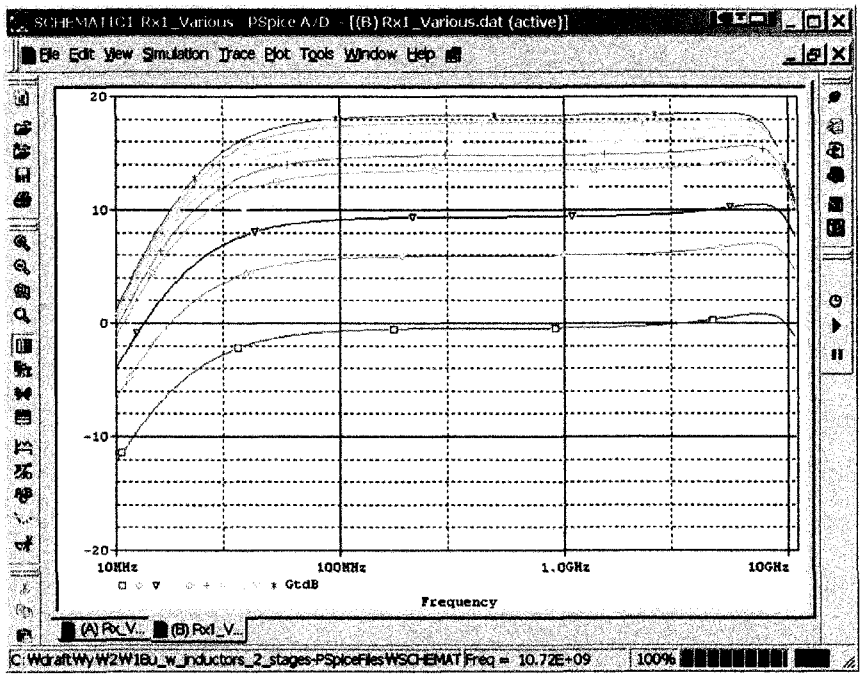

Figure 91 Rx1 optimization

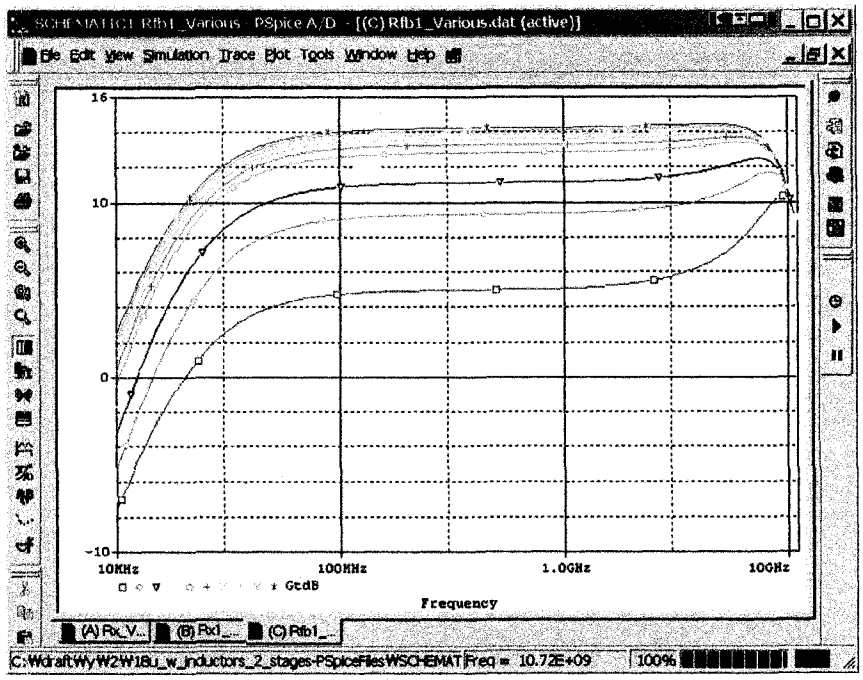

Figure 92 Rfb1 optimization

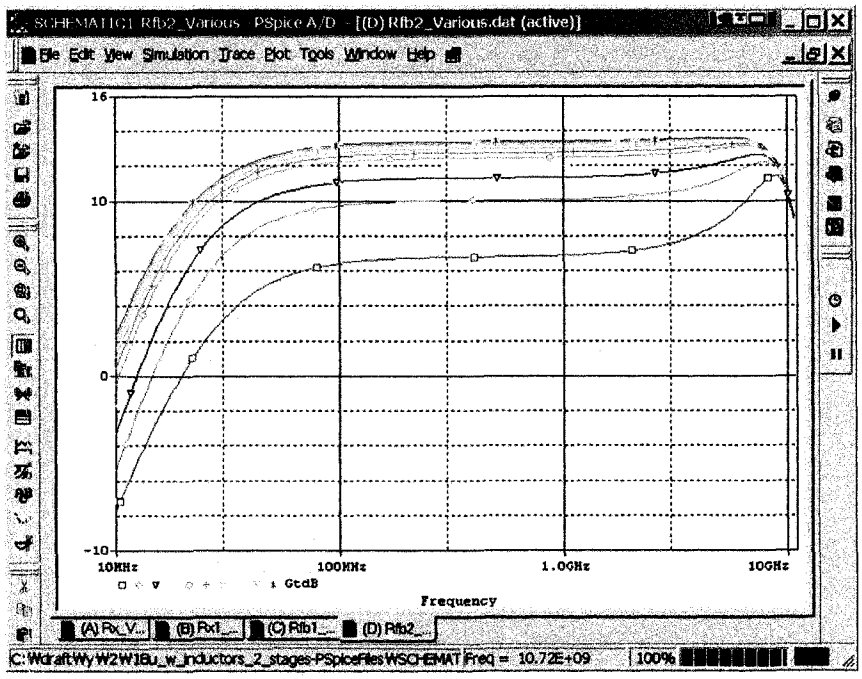

Figure 93 Rfb2 optimization

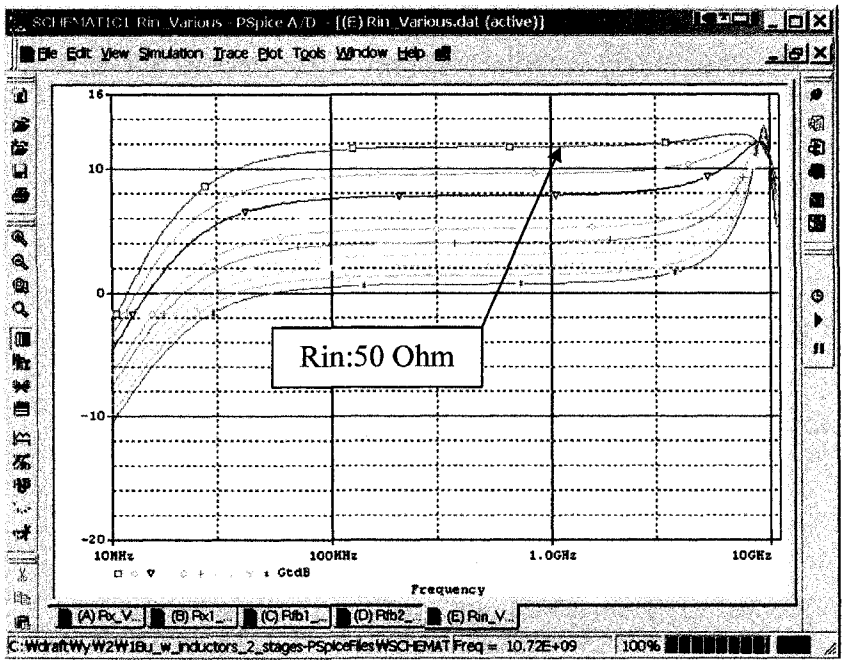

Figure 94 Rin optimization

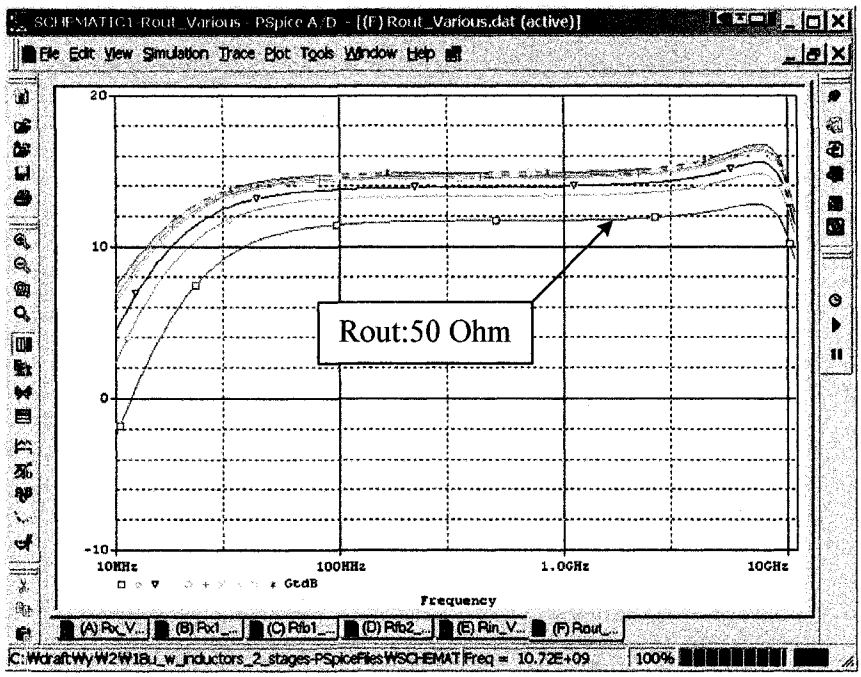

Figure 95 Rout optimization

Table 9 Resistances effect comparison table

Resistances	Effects	Remark
Rx & Rx1	These resistance affect the overall transducer gain (Gt). Lower values give better frequency response.	
Rfb1 & Rfb2	Higher values give better flatness. However, power consumption increases.	
Rin	Lower resistance gives better transducer gain (Gt) and frequency response. Higher resistance causes distortion of the transducer gain (Gt)	
Rout	Unlike the input resistance, the output resistance affects on the overall transducer gain (Gt). This simulation results show the difficulties of achieving high transducer gain with 50 ohm resistance.	

6.3 OPTIMIZING PROPOSED INDUCTORLESS LAYOUT

In this section, optimizations of the proposed inductorless layout will be represented. As shown previously, transducer gain (Gt) and frequency response will be analyzed with different values of each component.

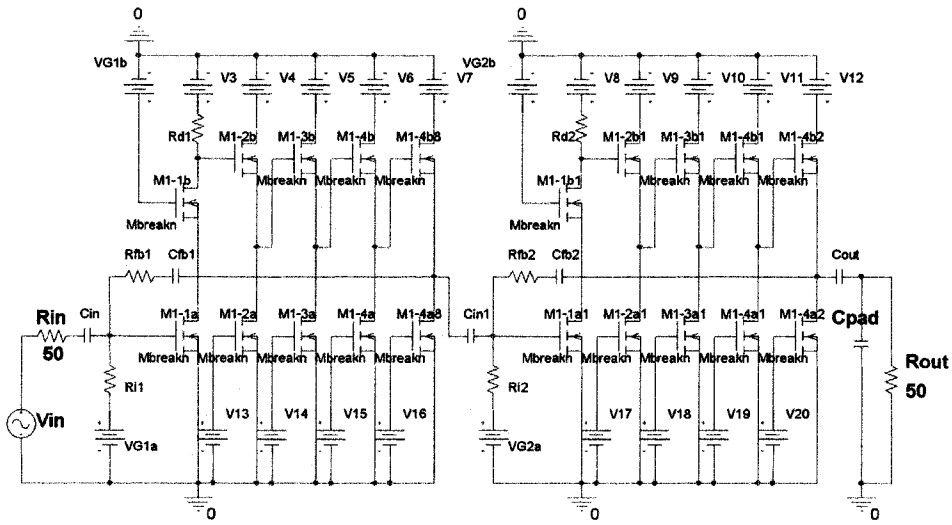

Figure 96 Proposed inductorless layout

Figure 96 shows the proposed inductorless layout. At first, the effects of voltages will be analyzed. Secondly, the effects of each MOSFET's width will be analyzed. Finally, the effects of resistances will be analyzed.

The comparisons will be shown in the Table 10.

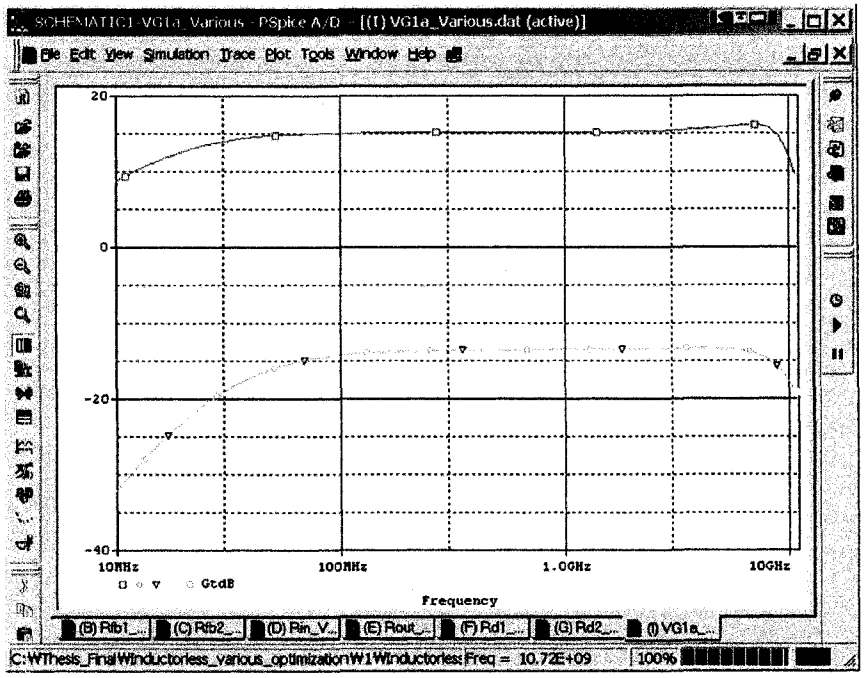

Figure 97 VG1a optimization

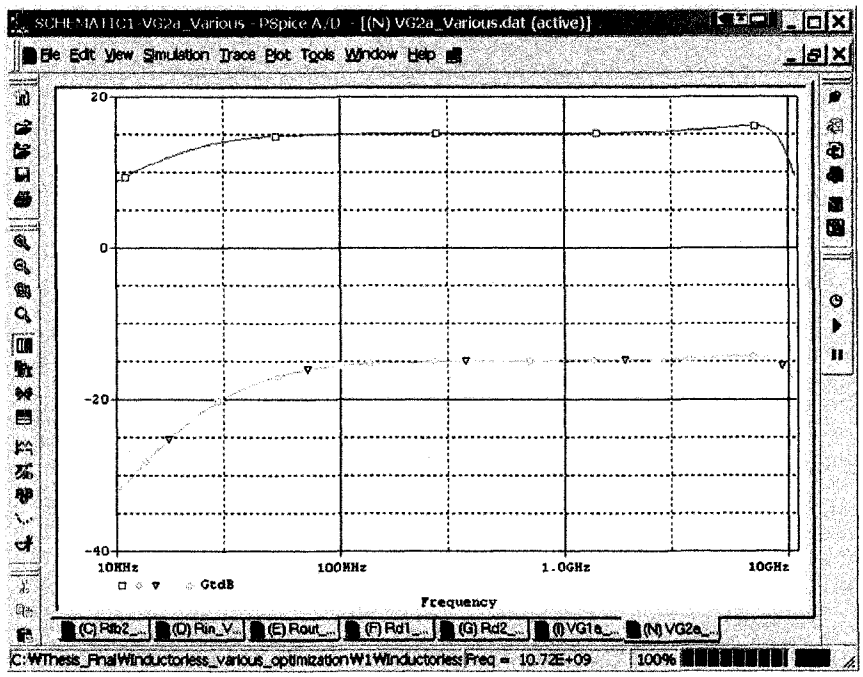

Figure 98 VG2a optimization

Only 1 Vdc of VG1a and VG2a is possible one.

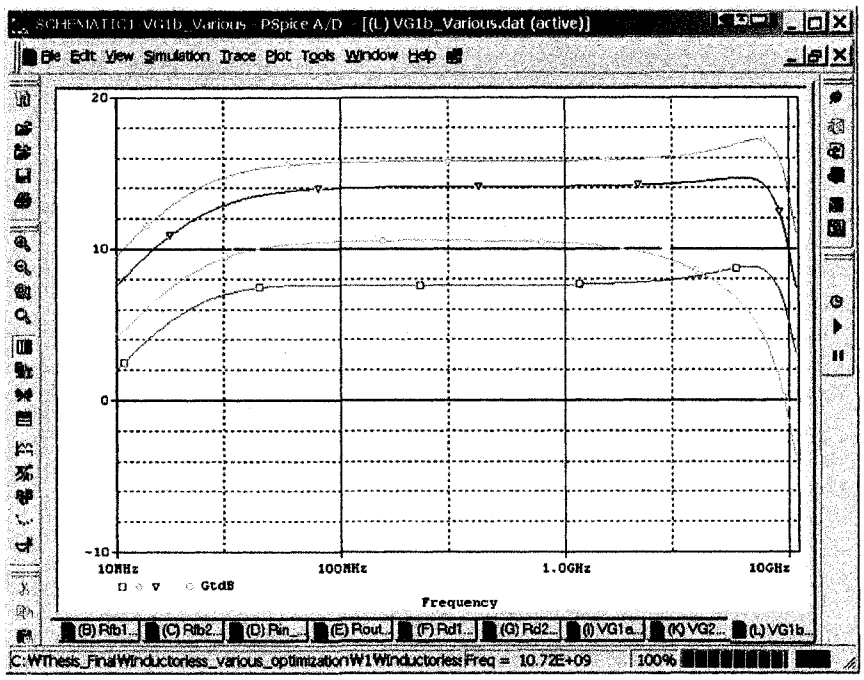

Figure 99 VG1b optimization

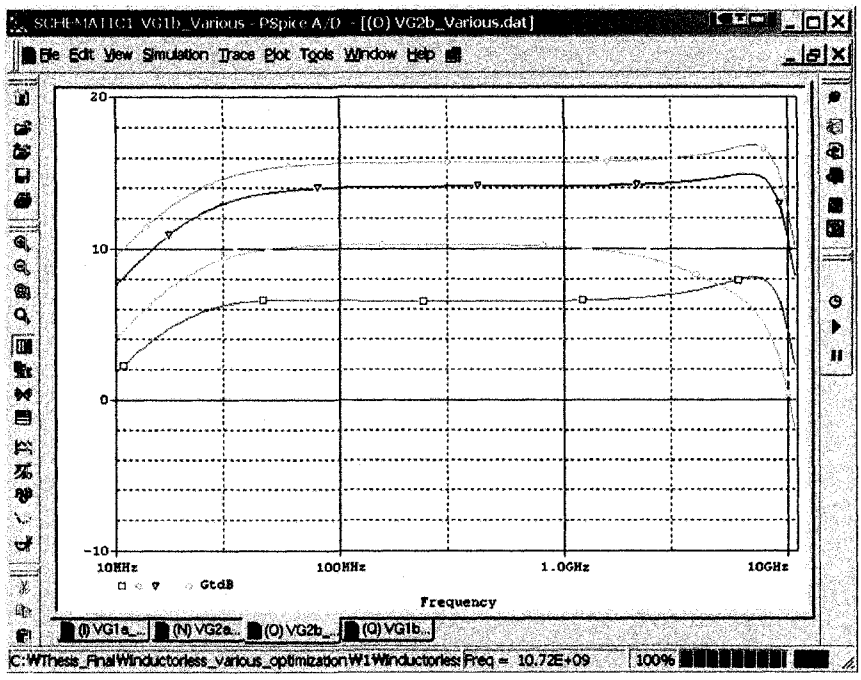

Figure 100 VG2b optimization

Optimum value of VG1b and VG2b will be between 2 Vdc and 3 Vdc.

Table 10 Bias voltage comparison table

Voltages	Effects	Remark
VG1a & VG2a	Only 1 Vdc is working as a bias voltage.	
VG1b & VG2b	Optimum value will be between 2 Vdc and 3 Vdc.	

Based on the simulation results, only 1 Vdc will be working for VG1a and VG2a and the optimum value of VG1b and VG2b is between 2 Vdc and 3 Vdc.

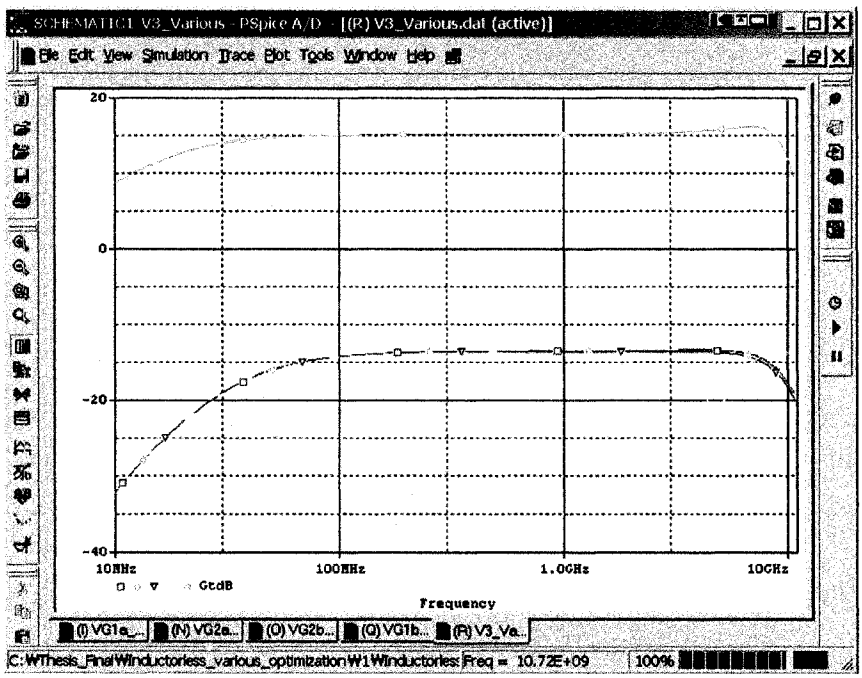

Figure 101 V3 optimization

Only 5 Vdc is working supply voltage of M1-1b.

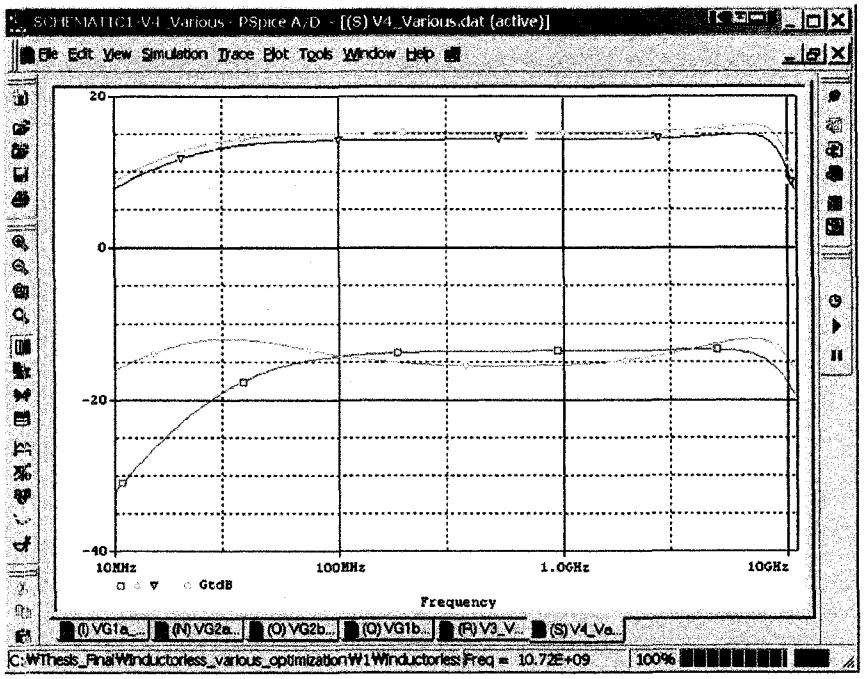

Figure 102 V4 optimization

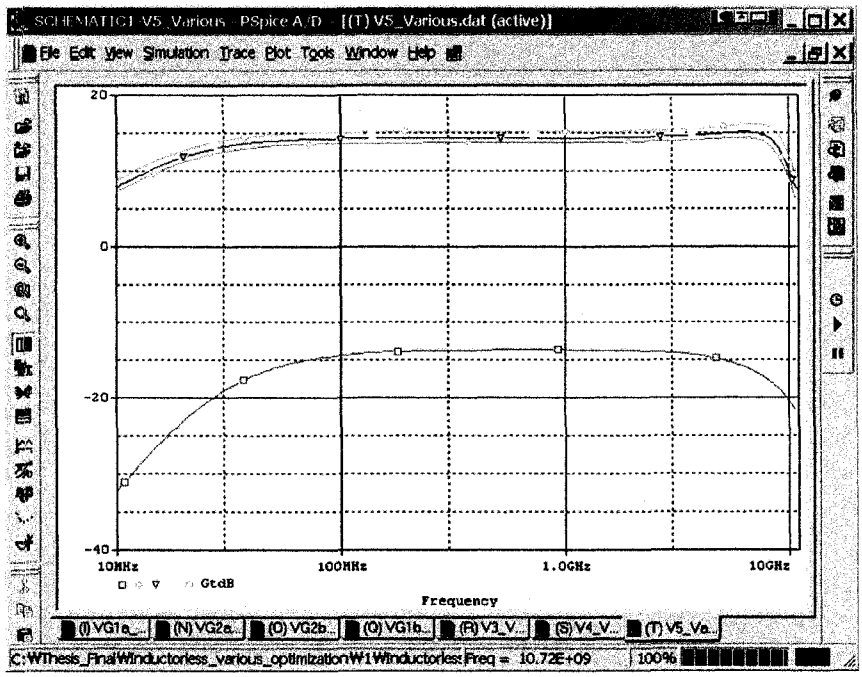

Figure 103 V5 optimization

3, 4, and 5 Vdc will be possible for V4 and 2, 3, 4, and 5 Vdc will be possible for V5.

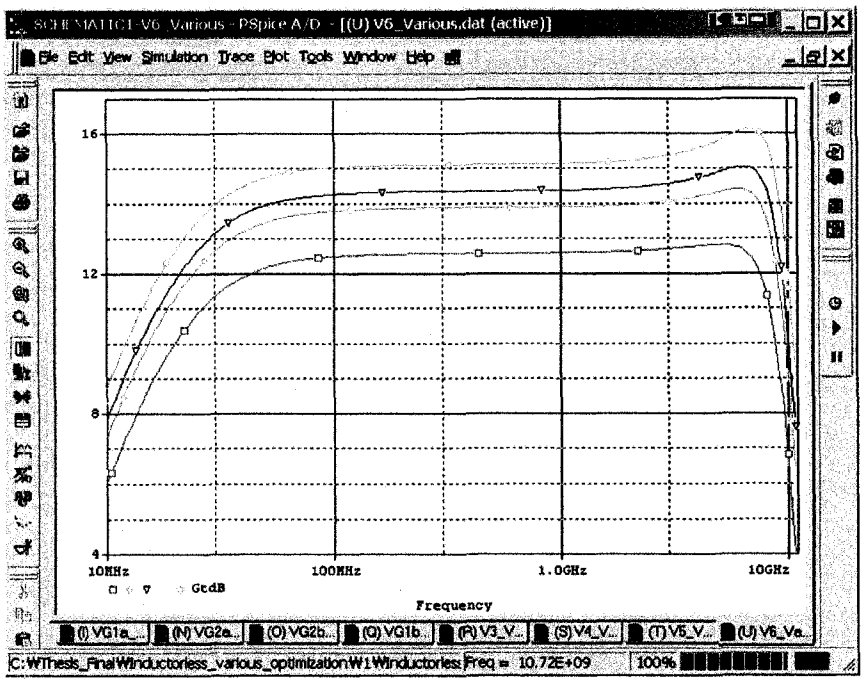

Figure 104 V6 optimization

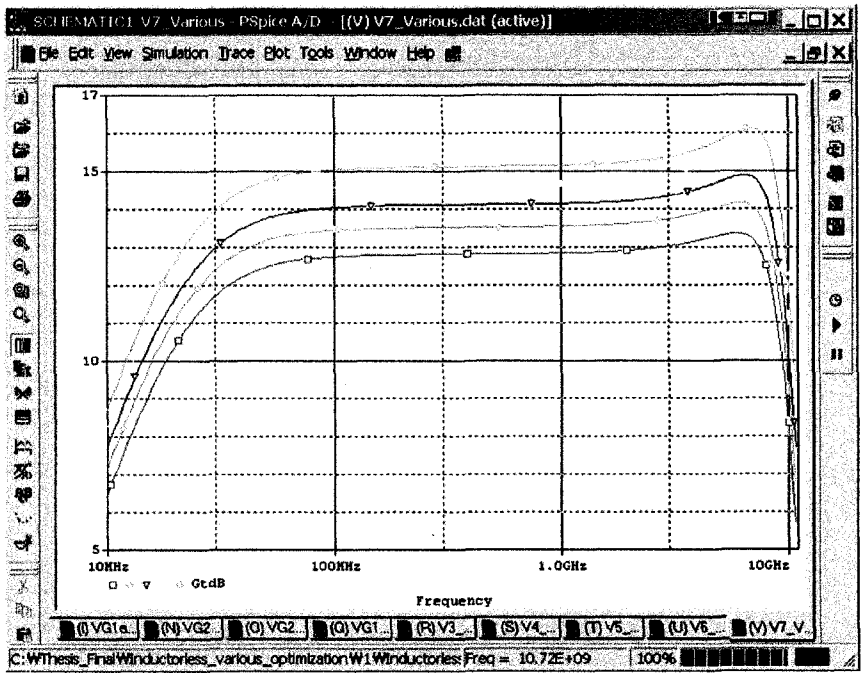

Figure 105 V7 optimization

V6 and V7 affect the transducer gain (Gt). The higher value gives higher transducer gain (Gt).

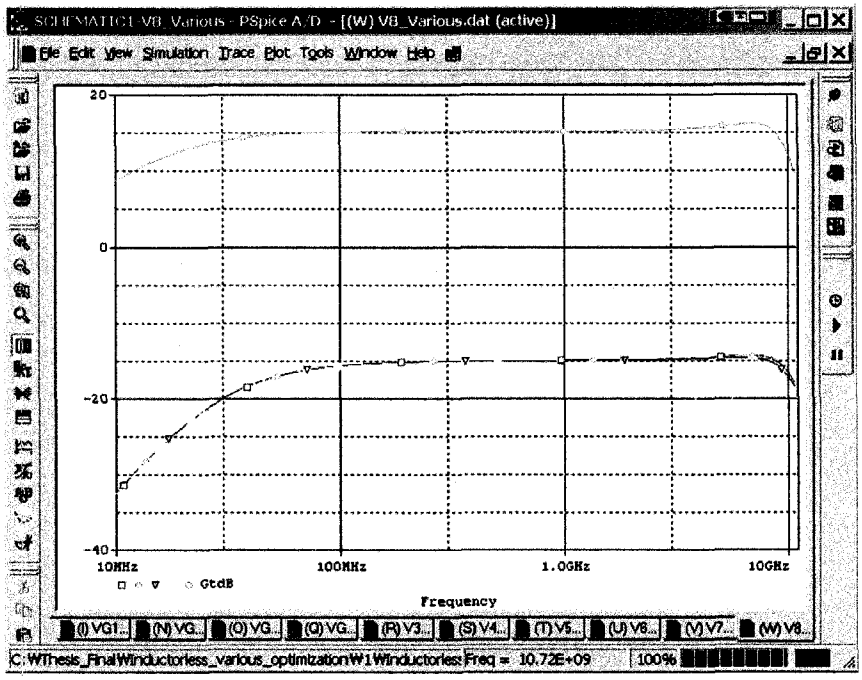

Figure 106 V8 optimization

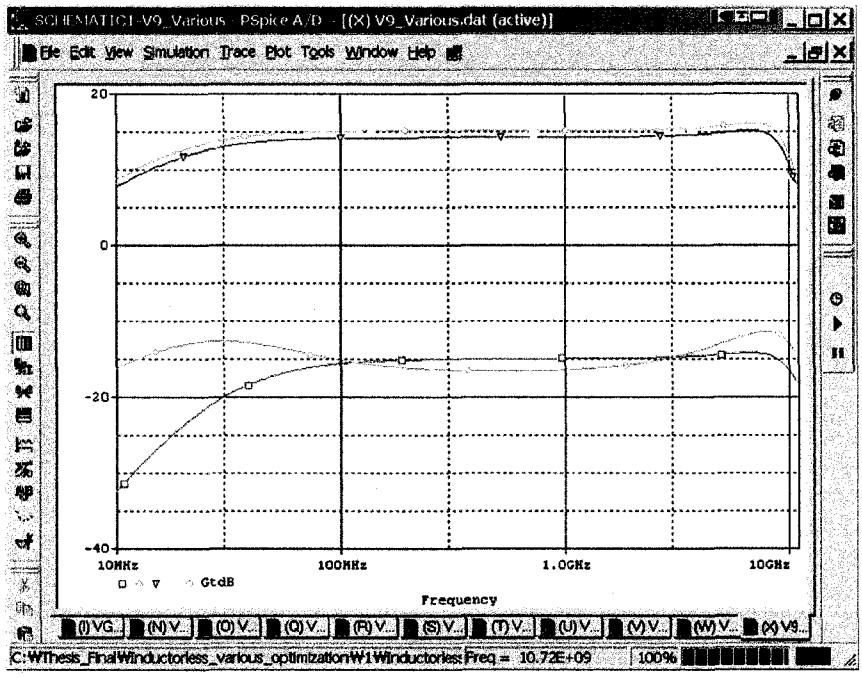

Figure 107 V9 optimization

V8, V9, V10 (Figure 108) affect almost the same as V3, V4, V5 each other.

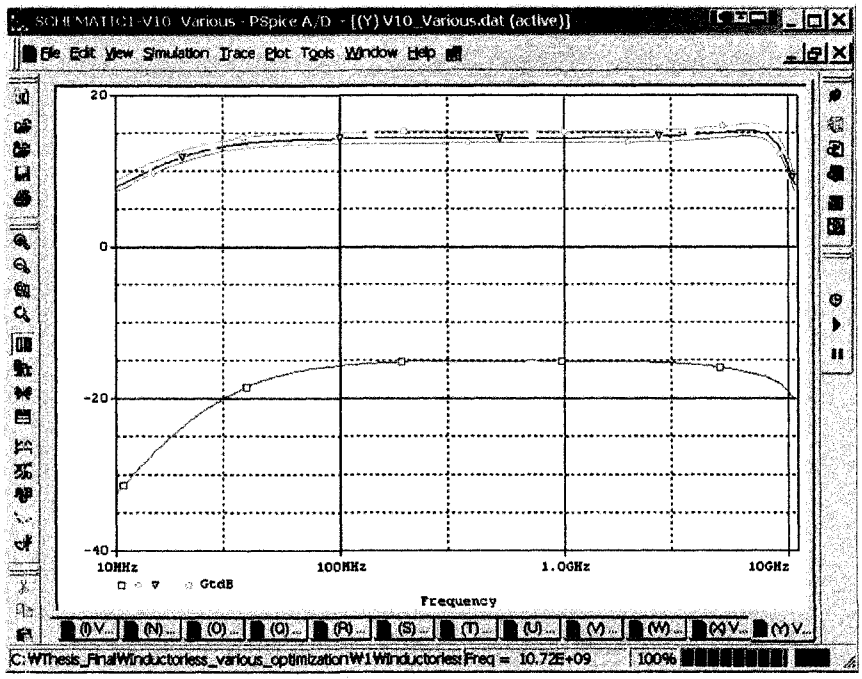

Figure 108 V10 optimization

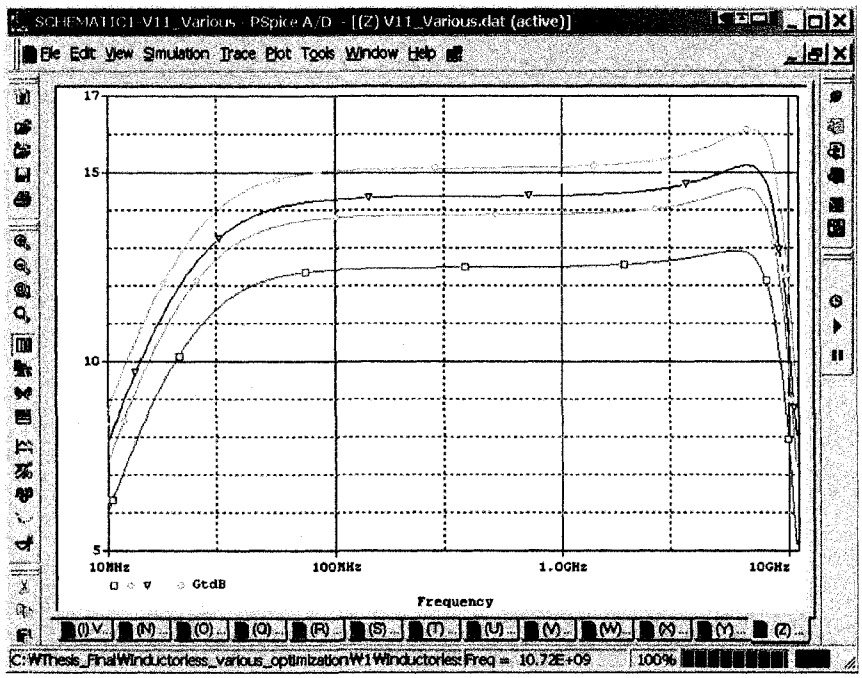

Figure 109 V11 optimization

V11 and V12 (Figure 110) affect the same as V6 and V7. The higher value gives higher transducer gain (Gt).

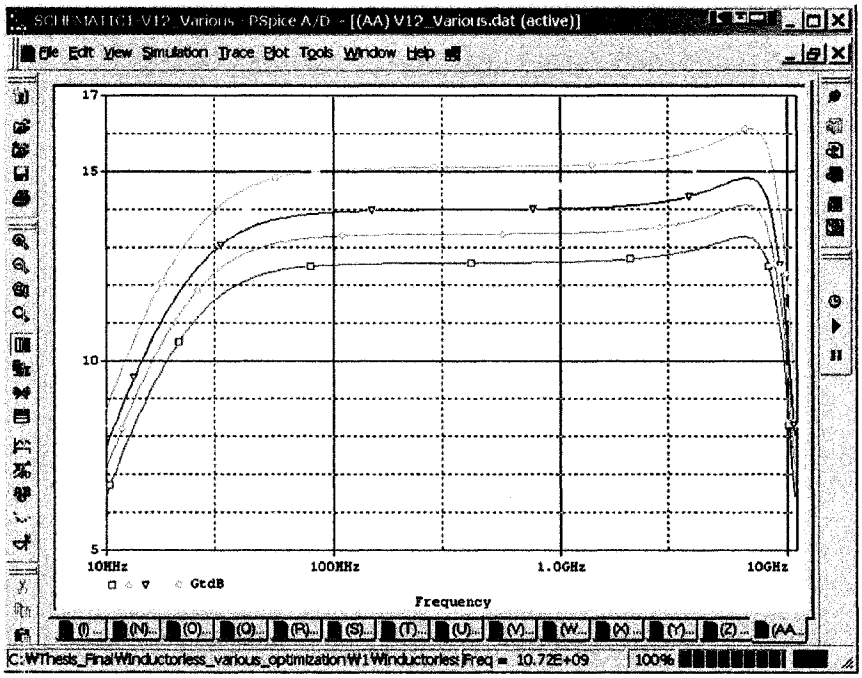

Figure 110 V12 optimization

Table 11 Drain voltage comparison table

Drain Voltage	Effects	Best Values	Remark
V3 & V8	Only 1 Vdc will be working.	1.0 Vdc	
V4 & V9	The transducer gain (Gt) is not really changing with certain values.	3 ~ 5 Vdc	*
V5 & V10	The transducer gain (Gt) is not really changing with certain values.	2 ~ 5 Vdc	*
V6, V7 and V11, V12	Affects the overall transducer gain (Gt). The higher value gives higher transducer gain (Gt).		

* The lower voltages give lower power consumption. However, using different voltages make the circuit complex. This is a trade-off.

Subsequent graphs show the effect of each bias voltage of the CS amplifiers.

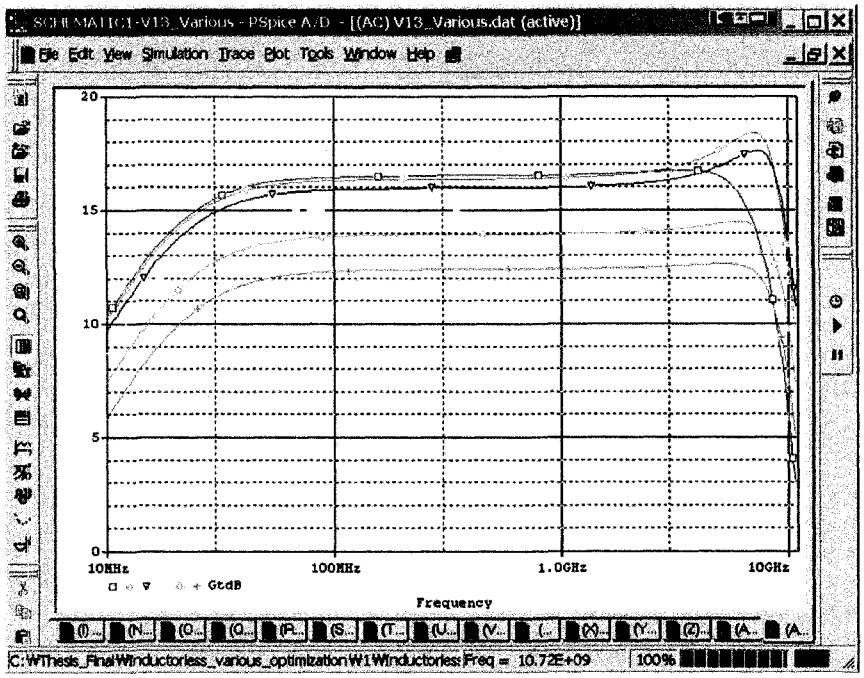

Figure 111 V13 optimization

Higher values of V13, V14 (Figure 112), and V15 (Figure 113) are not working. The optimum values are between 0.6 and 0.8 Vdc.

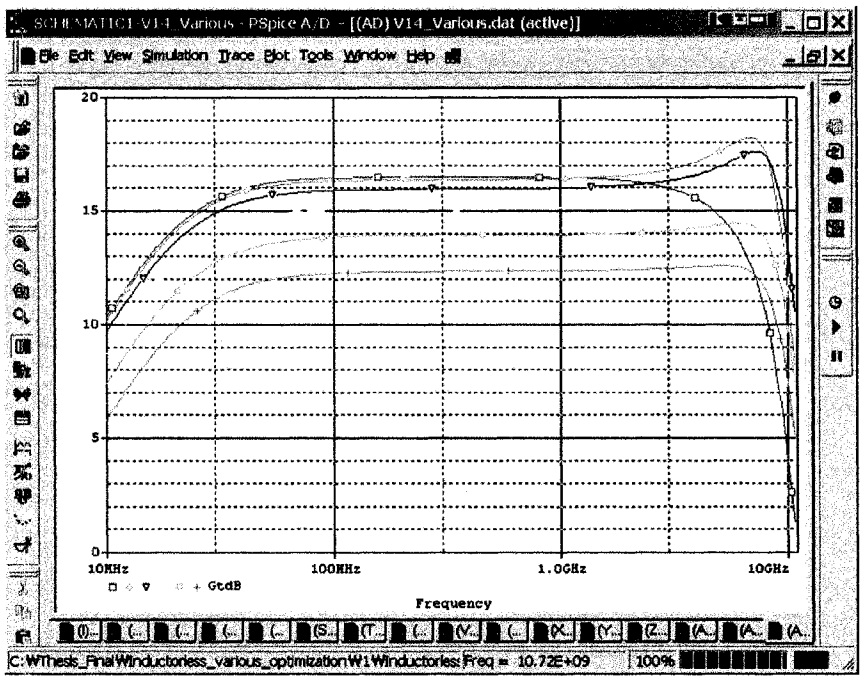

Figure 112 V14 optimization

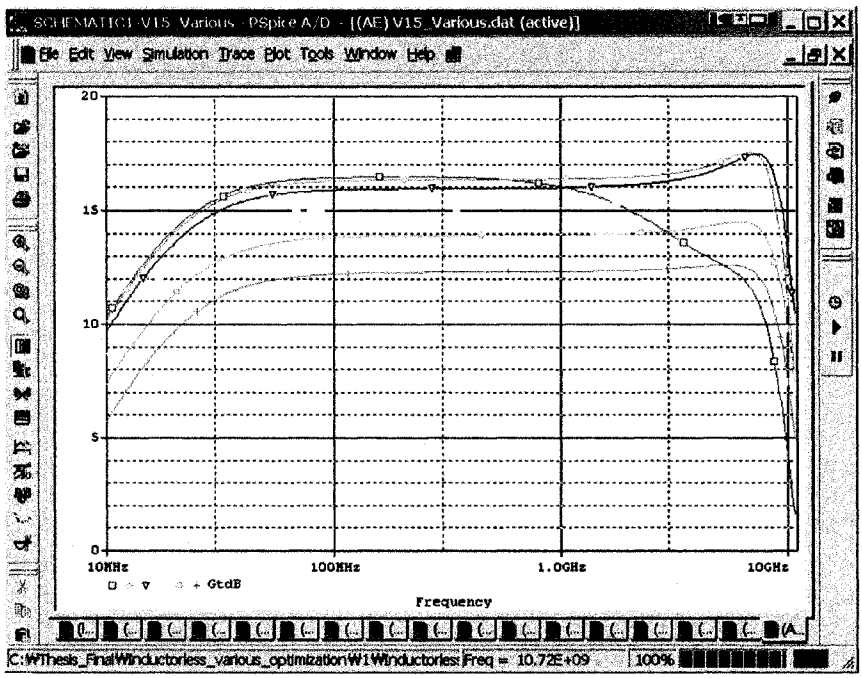

Figure 113 V15 optimization

0.6, 0.7, and 0.8 Vdc are the optimum values of V14 and V15.

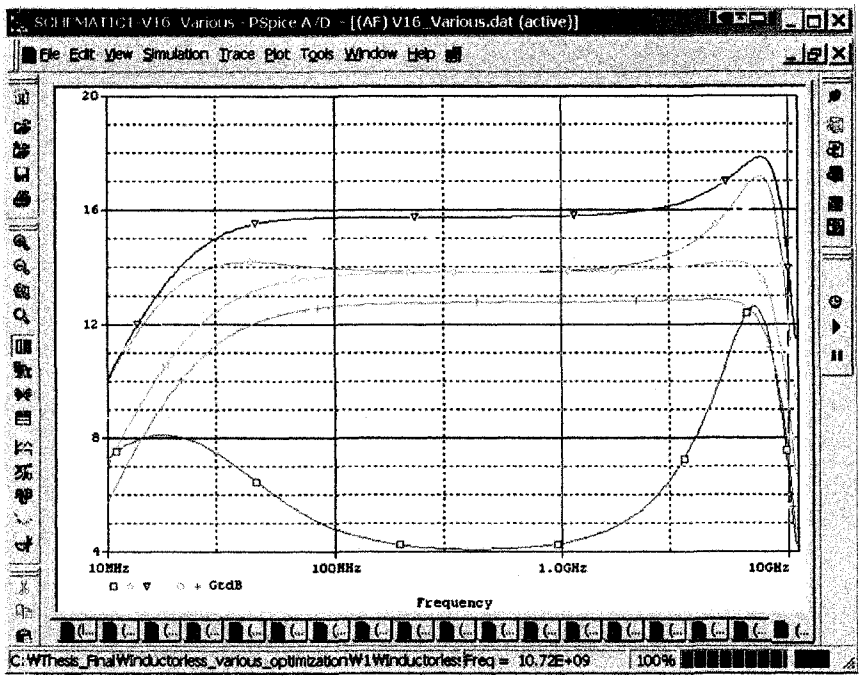

Figure 114 V16 optimization

0.7 and 0.8 Vdc are the optimum voltages of V16.

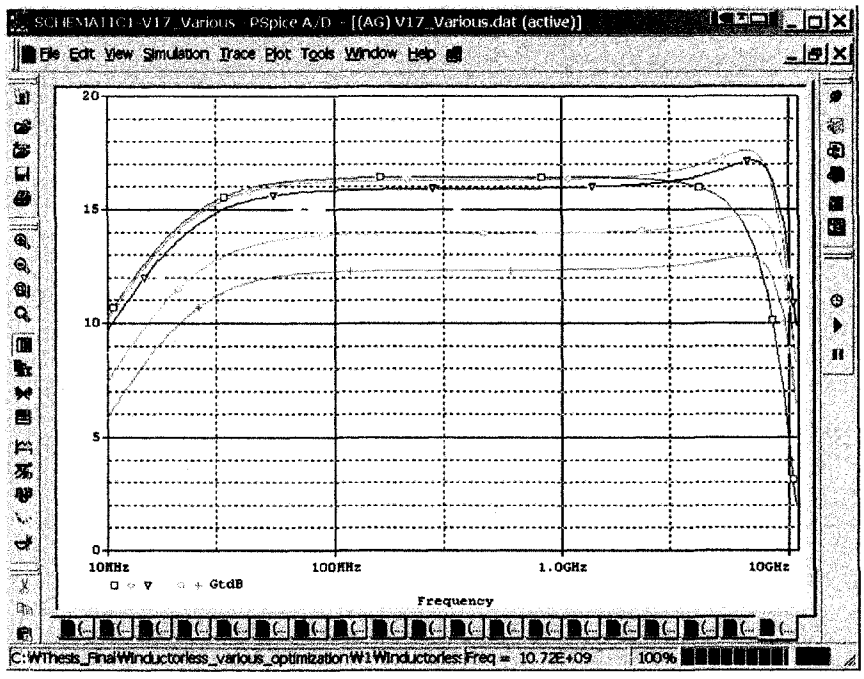

Figure 115 V17 optimization

0.6, 0.7, and 0.8 Vdc are the optimum voltages of V17.

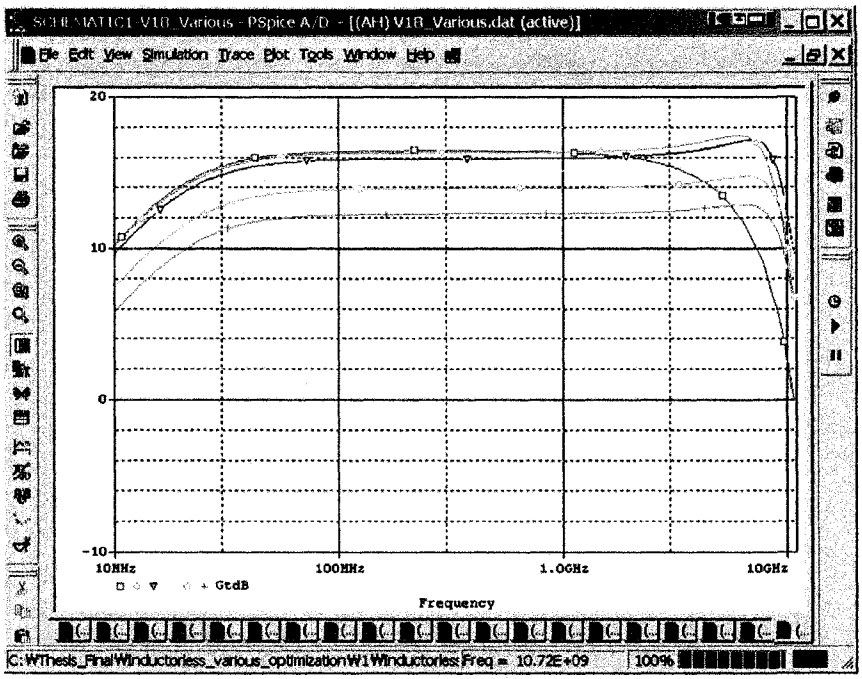

Figure 116 V18 optimization

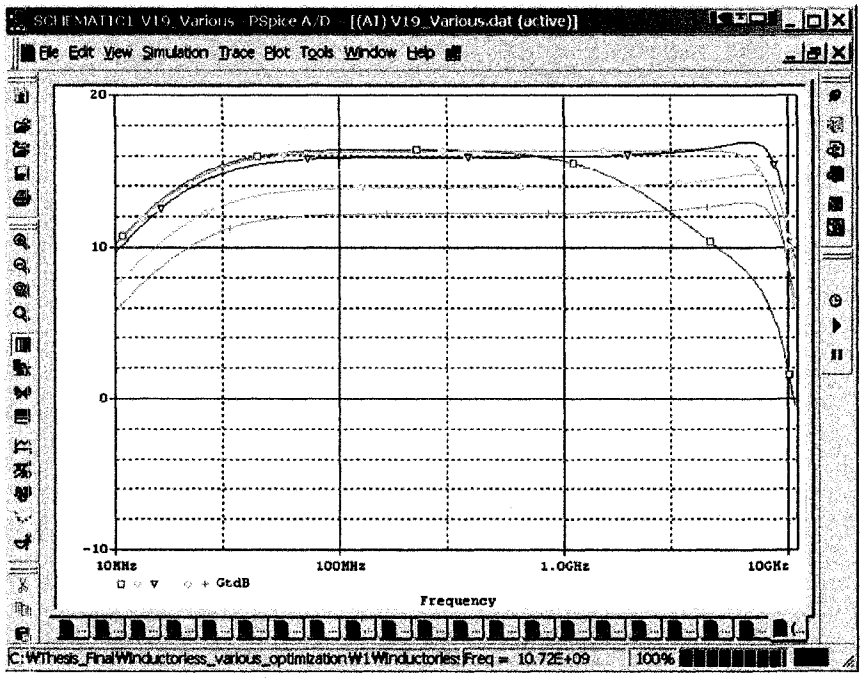

Figure 117 V19 optimization

0.7 and 0.8 Vdc are the best values of V18 and V19.

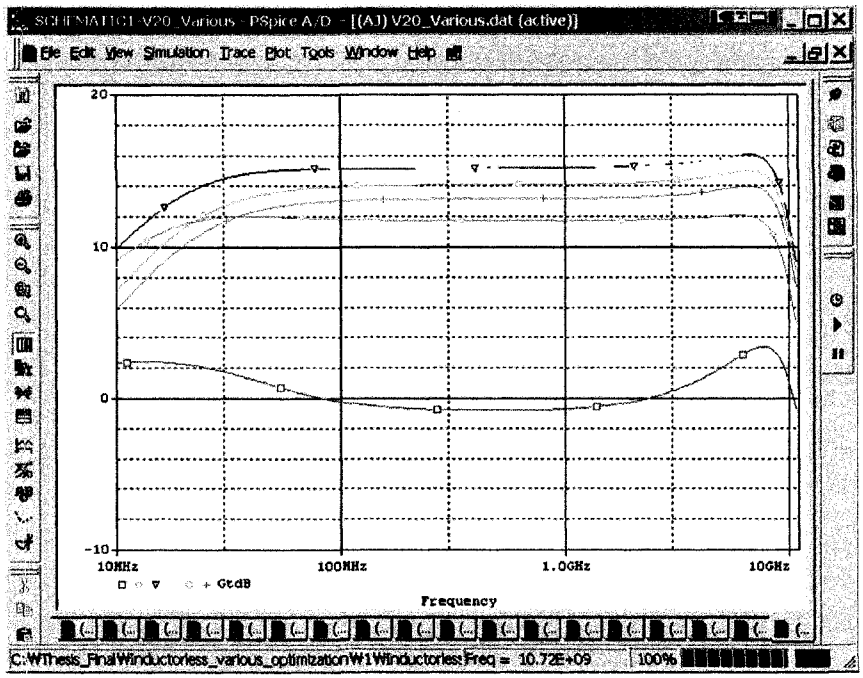

Figure 118 V20 optimization

0.7 and 0.8 Vdc are the best values of V20.

Table 12 Bias voltage of CS comparison table

Bias Voltage	Effects	Best Values	Remark
V13, V14 & V15,V17,V18	Higher values give worse transducer gain (Gt).	0.6 ~ 0.8 Vdc	*
V16	0.7 Vdc gives higher transducer gain (Gt) whereas 0.8 Vdc gives better flatness.	0.7 & 0.8 Vdc	*
V19	0.7 Vdc gives the highest transducer gain (Gt) and frequency response.	0.7 & 0.8 Vdc	*
V20	0.7 Vdc and 0.8 Vdc give almost	0.7 & 0.8 Vdc	*

	the same performance of transducer gain (Gt) and frequency response.		

* The lower voltages give lower power consumption. However, using different voltages make the circuit complex. This is a trade-off.

Subsequent graphs show the effect of width of each MOSFETs.

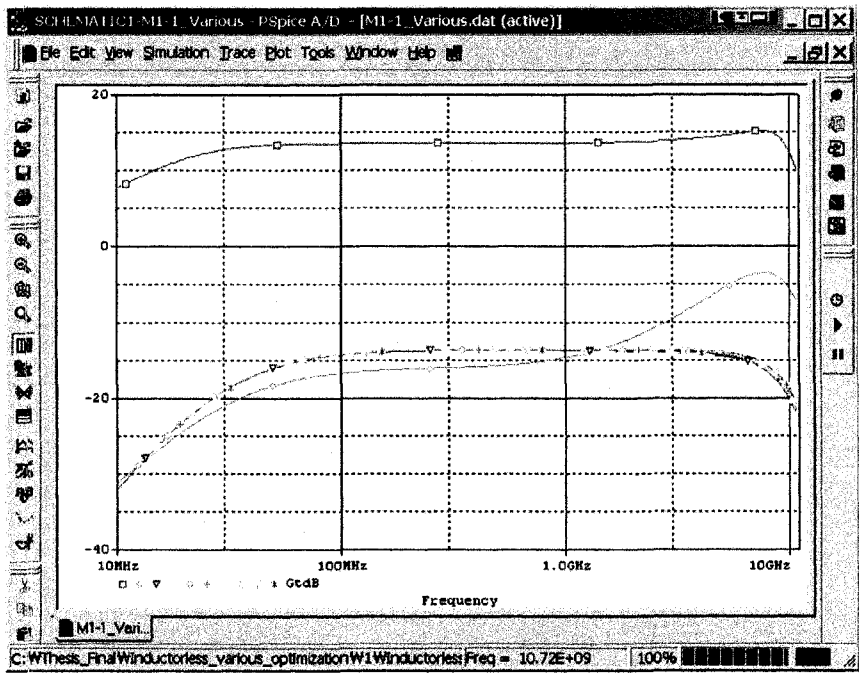

Figure 119 Width of M1-1a & M1-1b MOSFET optimization

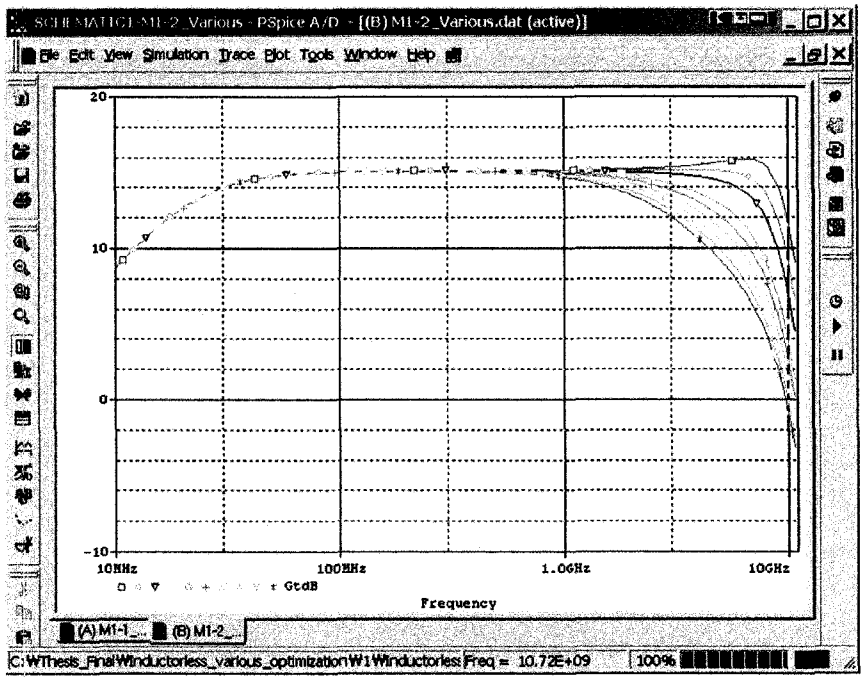

Figure 120 Width of M1-2a & M1-2b MOSFET optimization

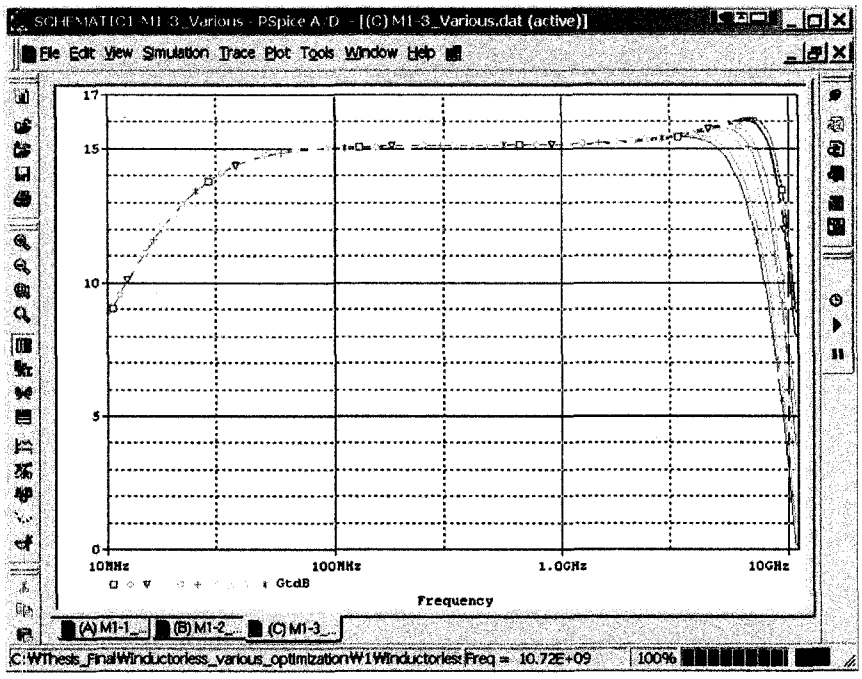

Figure 121 Width of M1-3a & M1-3b MOSFET optimization

Lower width of M1-2a, M1-2b, M1-3a, and M1-3b give better frequency response in high frequency region.

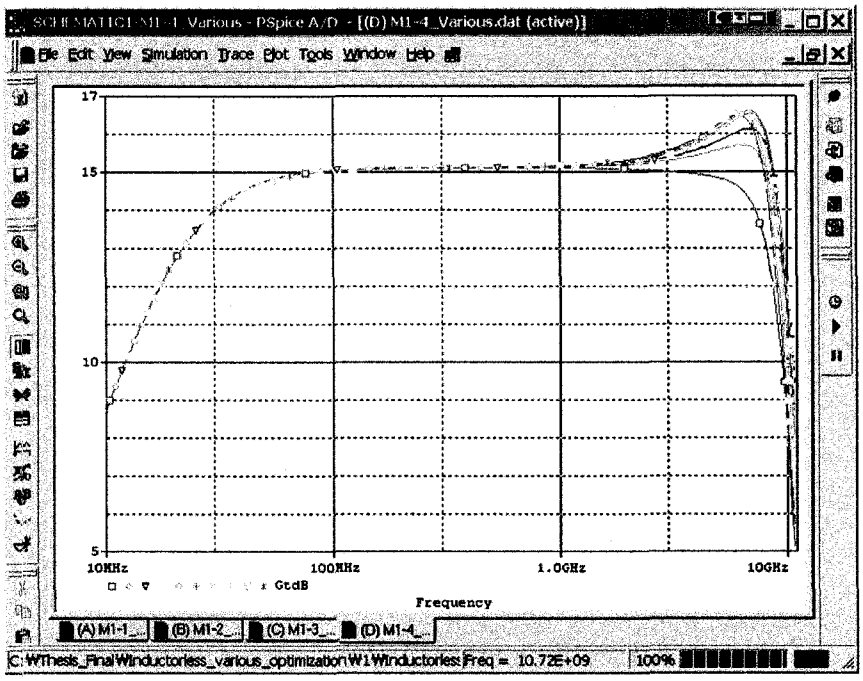

Figure 122 Width of M1-4a & M1-4b MOSFET optimization

Higher width gives better frequency response. However, causes peaking.

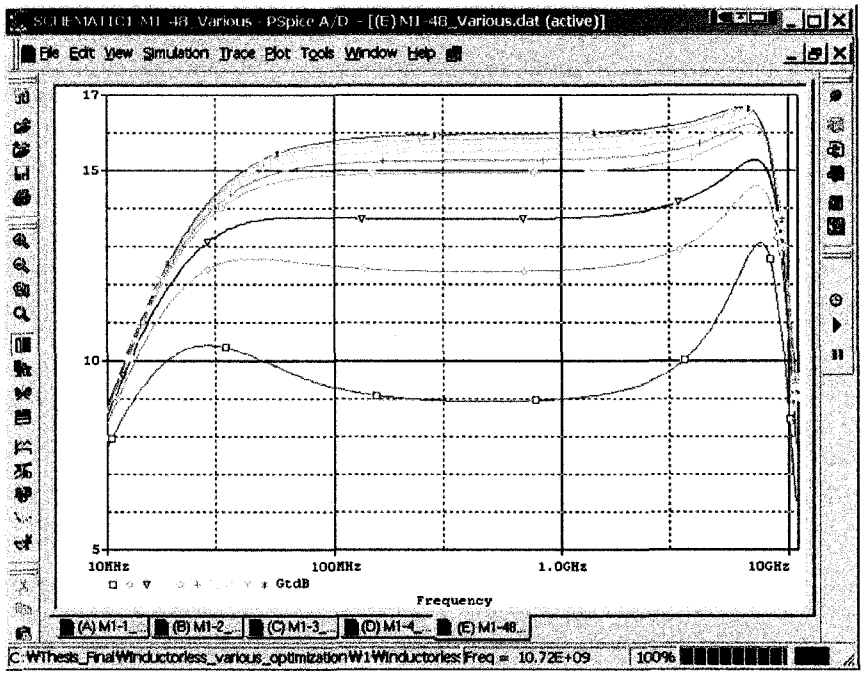

Figure 123 Width of M1-4a8 & M1-4b8 MOSFET optimization

Higher width affects overall transducer gain (Gt) with frequency response.

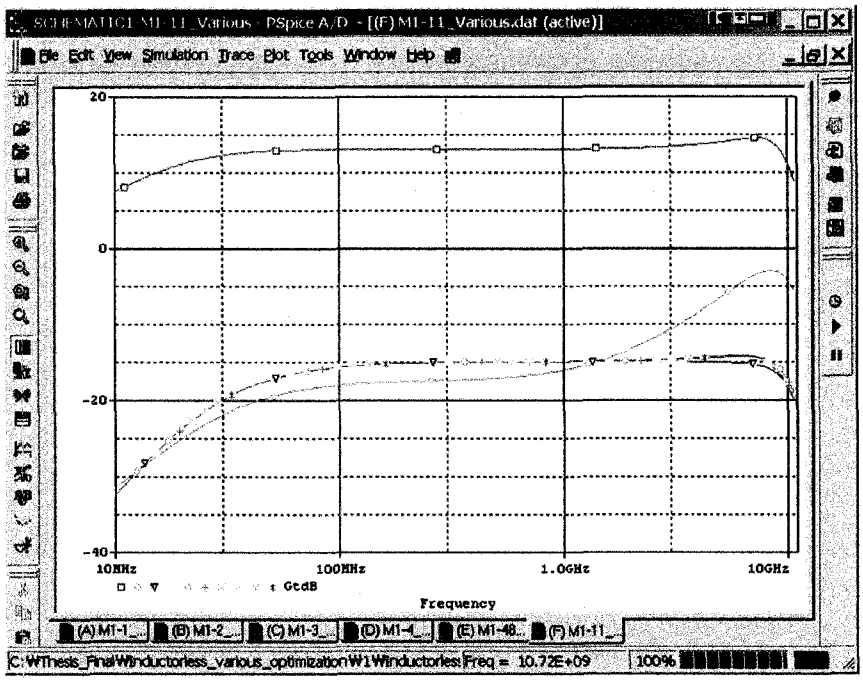

Figure 124 Width of M1-1a1 & M1-1b1 MOSFET optimization

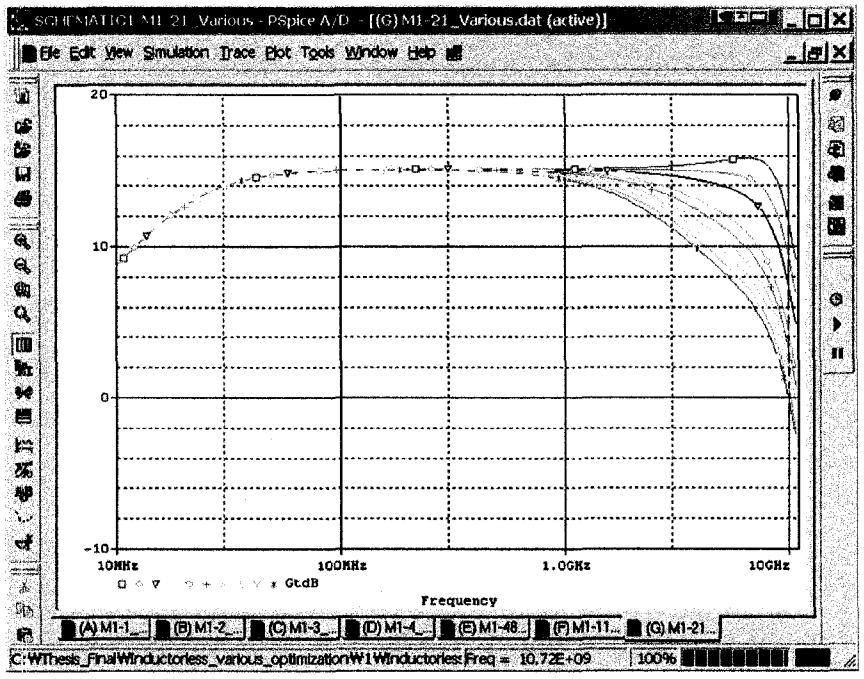

Figure 125 Width of M1-2a1 & M1-2b1 MOSFET optimization

Lower width of M1-2a1, M1-2b1, M1-3a1, and M1-3b1 (Figure 126) give better frequency response in high frequency region.

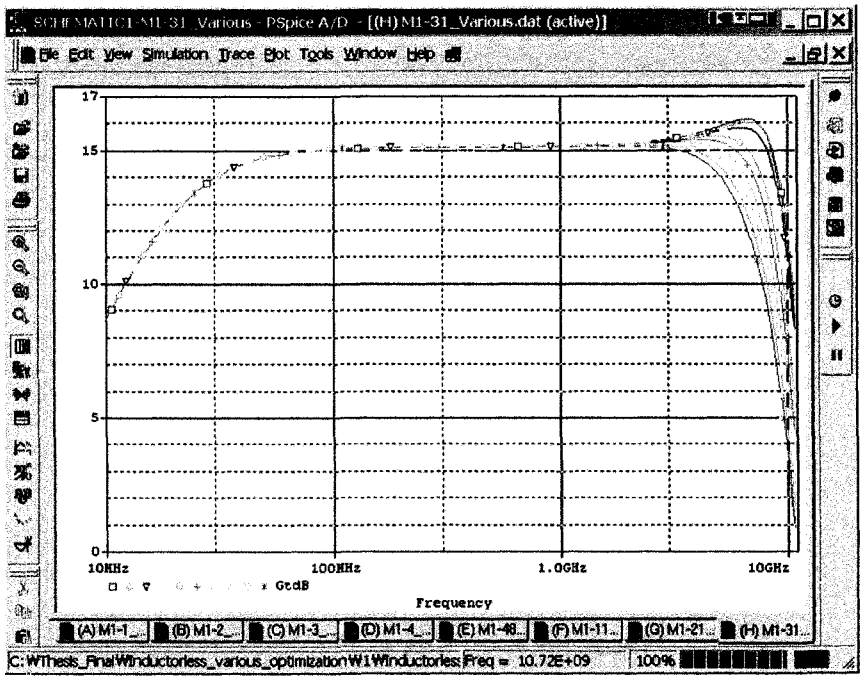

Figure 126 Width of M1-3a1 & M1-3b1 MOSFET optimization

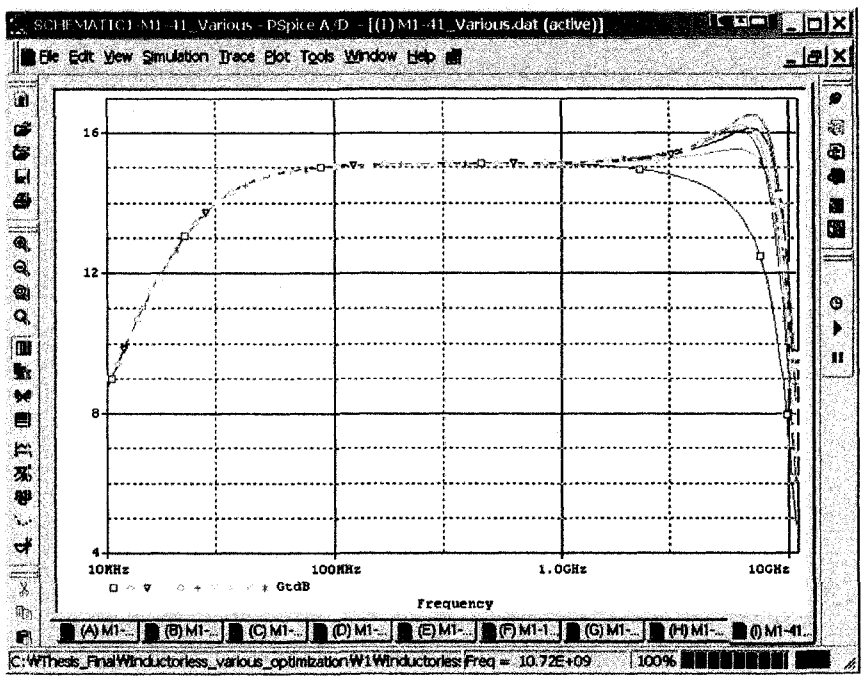

Figure 127 Width of M1-4a1 & M1-4b1 MOSFET optimization

Higher width gives better frequency response. However, causes peaking.

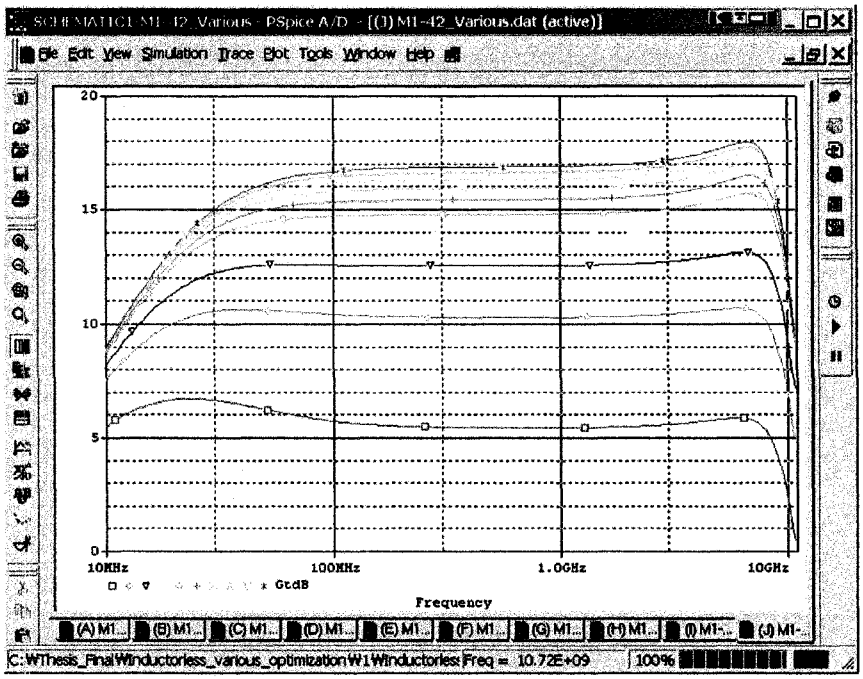

Figure 128 Width of M1-4a2 & M1-4b2 MOSFET optimization

Higher width affects overall transducer gain (Gt) with frequency response.

Table 13 MOSFET width effects comparison table

MOSFET Width	Effects	Remark
M1-1a, M1-1b, M1-1a1, & M1-1b1	Optimized value will be between 10 μm and 20 μm.	
M1-2a, M1-2b, M1-3a, M1-3b, M1-2a1, M1-2b1, M1-3a1, & M1-3b1	Lower width gives better frequency response in high frequency region.	

M1-4a, M1-4b, M1 4a1, & M1-4b1	Higher width gives better frequency response in high frequency region. However, best value has to be selected not too exceed the peaking criteria.	
M1-4a8, M1-4b8, M1-4a2, & M1-4b2	Higher width gives better overall transducer gain (Gt).	

Based on the simulation results, wider width does not give better performance always. Sometimes, shorter width gives better performance.

Subsequent graphs will show the effects of Rd, feedback resistances, input, and output resistances.

Rd1 and Rd2 affect the overall transducer gain (Gt) and optimum values are between 600 ~ 800 ohms.

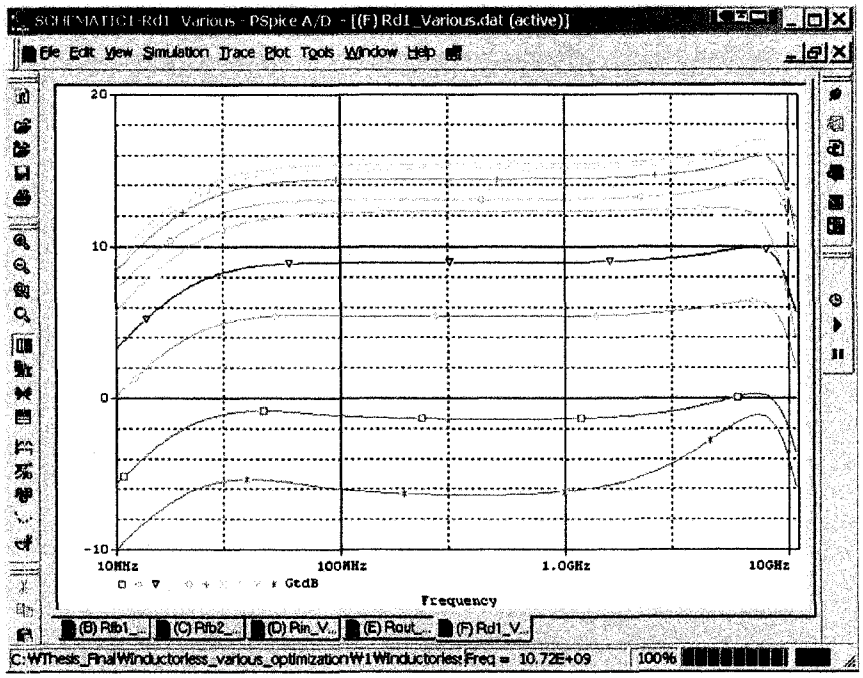

Figure 129 Rd1 optimization

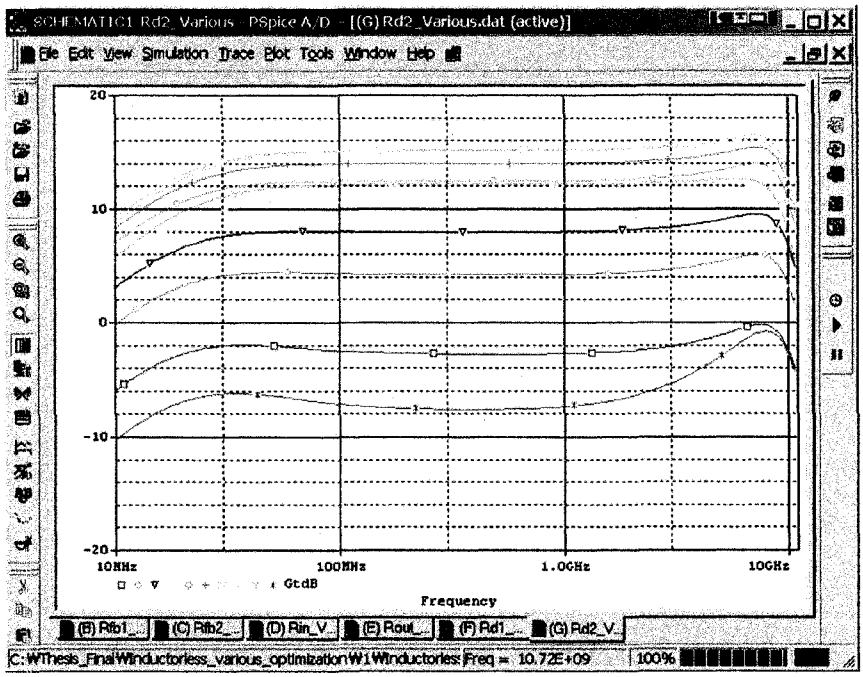

Figure 130 Rd2 optimization

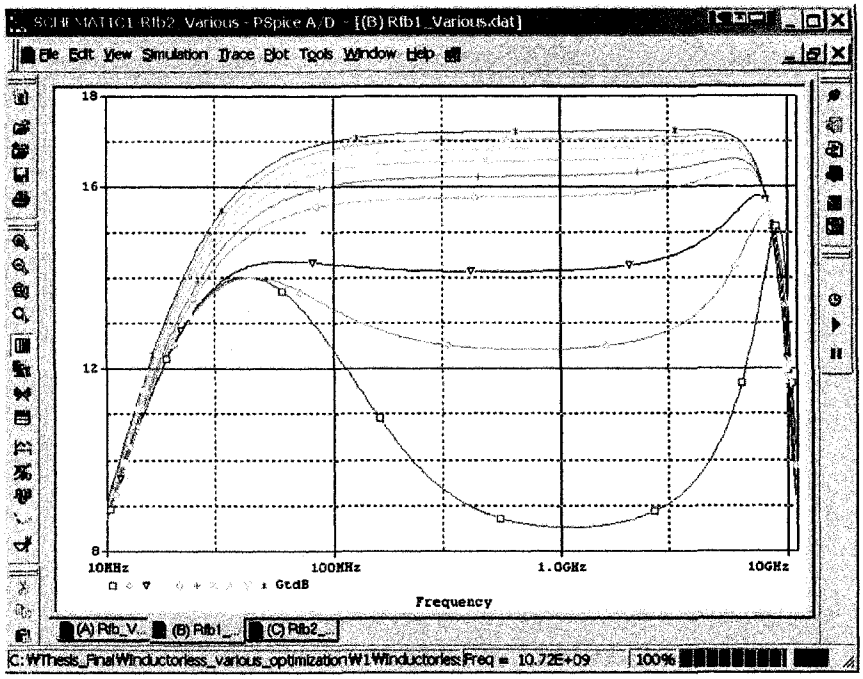

Figure 131 Rfb1 optimization

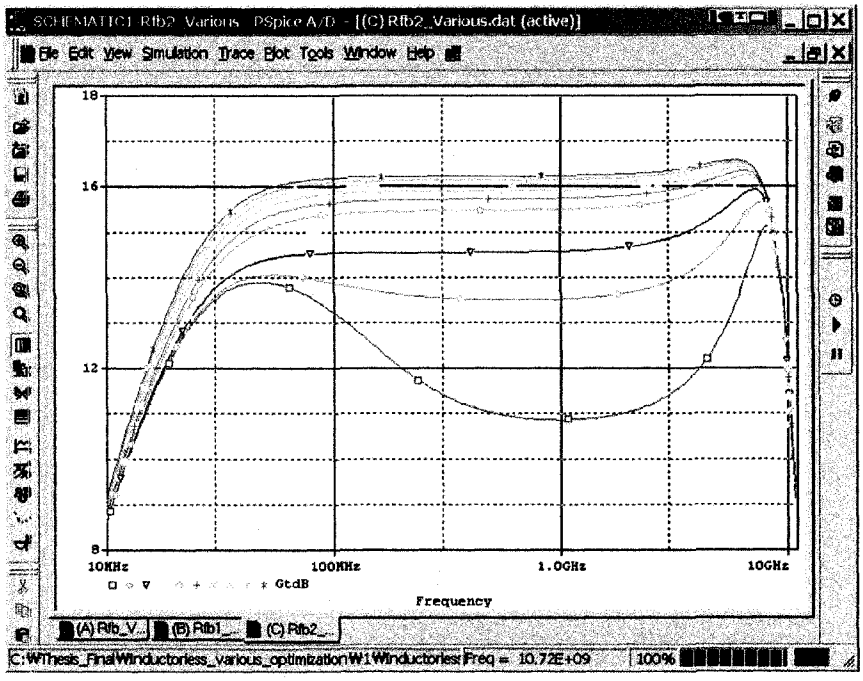

Figure 132 Rfb2 optimization

Higher values give better transducer gain (Gt).

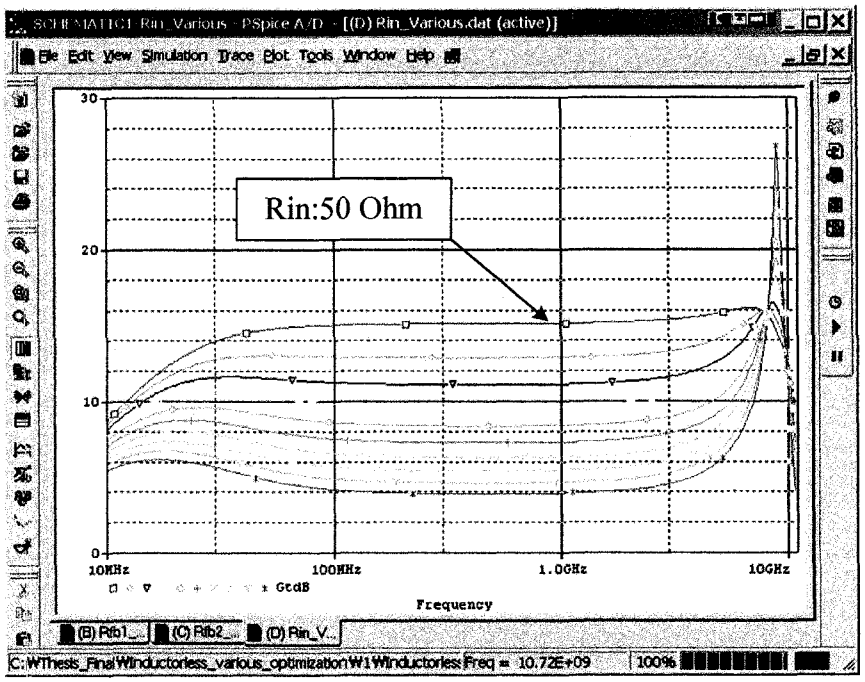

Figure 133 Rin optimization

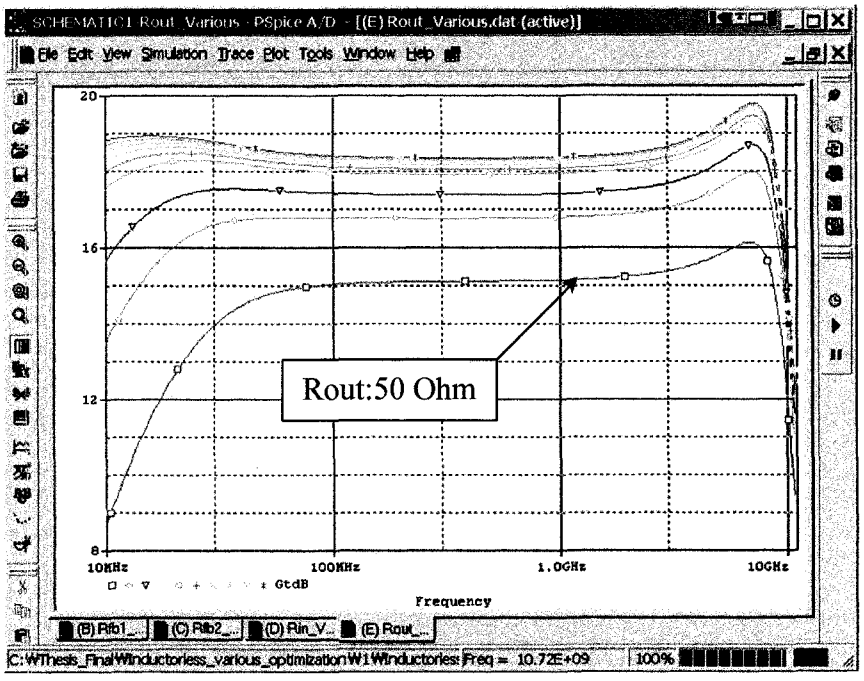

Figure 134 Rout optimization

Lower input resistance (Figure 133) gives better transducer gain (Gt). Higher output resistance give better transducer gain (Gt).

Table 14 Resistances effect comparison table

Resistances	Effects	Remark
Rd1 & Rd2	These resistance affect the overall transducer gain (Gt). Higher values give better transducer gain (Gt).	
Rfb1 & Rfb2	Higher values give better transducer gain (Gt) with better flatness.	
Rin	Lower resistance gives better transducer gain (Gt) and frequency response. Higher resistance causes distortion of the transducer gain (Gt)	
Rout	Unlike the input resistance, the output resistance affects on the overall transducer gain (Gt). This simulation results show the difficulties of achieving high transducer gain with 50 ohm resistance.	

CHAPTER 7

PROPOSED UWB AMPLIFIER QUALITY CHARACTERISTICS MEASUREMENTS

So far the optimizations of the proposed UWB amplifier have been shown. With couple of trade-offs, quite acceptable results are achieved. In this section, the quality characteristics shown below will be measured.

- Transducer Gain (dB) – already shown in section 5.4
- Noise Figure (dB)
- 1 dB Compressed Power (P1dB)
- IP3 Point

7.1 NOISE FIGURE (dB)

Figure 135 shows the Noise Figure (dB) of the two different designs. It shows that the circuit which does have inductors has better Noise Figure (dB); however, the Noise Figure is substantially higher than presented in [2] and [5].

The circuit which has inductors has better Noise Figure (dB) by a margin of 1.6 dB to 2.2 dB.

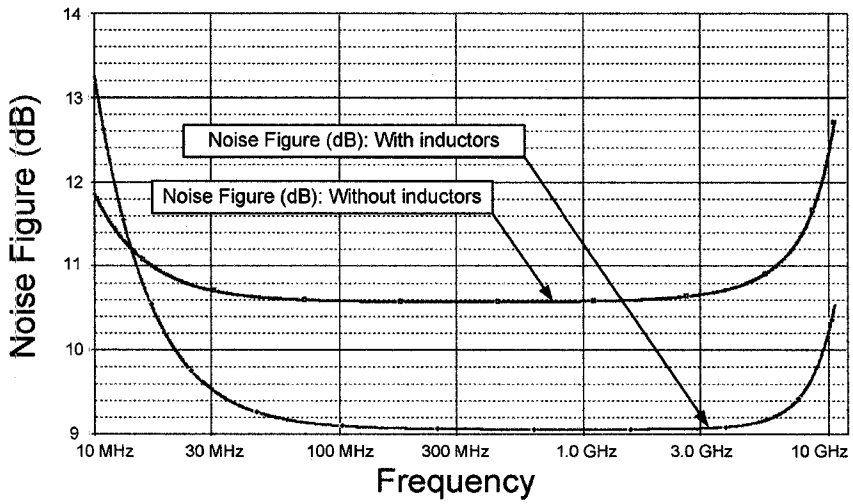

Figure 135 Noise Figure (dB) comparison with and without inductors

7.2 1 dB COMPRESSED POWER POINT (P1dB)

In this section, 1 dB compressed power point which is defined as the input power causes 1 dB drop in a linear gain due to its saturation will be shown.

The 1 dB compressed power comparison graph of the circuits with inductors and without inductors is shown in the Figure 136.

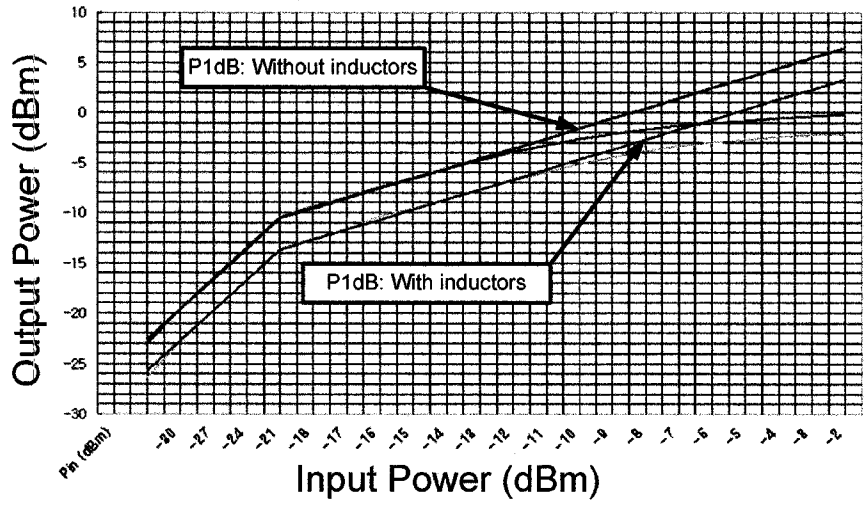

Figure 136 P1 dB comparison with and without inductors

The Figure 136 shows that the amplifier with inductors has higher compressed power with higher Transducer gain (dB).

7.3 IP3 POINT

The next important characteristic of measuring the linearity of amplifiers is the 3rd Intermodulation Product.

The Figure 137 shows the IP3 Point of the amplifier with inductors and without inductors.

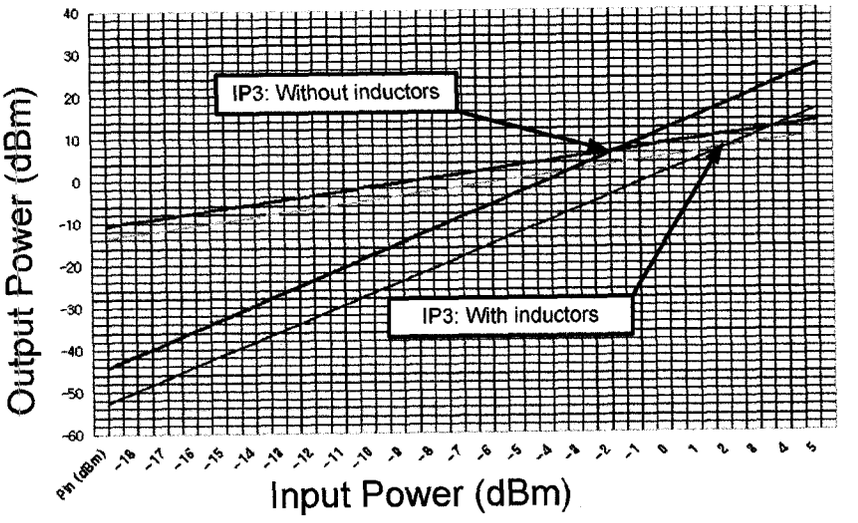

Figure 137 IP3 comparison with and without inductors

CHAPTER 8

CONCLUSIONS

A new design with the TSMC 0.18 μm MOSFET UWB amplifier is proposed and simulated. To satisfy the UWB requirements, multiple cascode stages cascaded with common drain stages has been used with feedback topologies. The Cadence OrCAD Capture simulation tool has been used.

Passive devices (resistors, capacitors, and inductors) play major role in RF circuits with active devices. Particularly, capacitors and inductors are critical components in the amplifiers. A newly proposed design without using inductors has been suggested. There are some trade-offs between the two designs with and without inductors. Also, the parasitic capacitance to ground of the blocking capacitors is a serious issue, and this thesis shown circuits that eliminate these blocking caps.

Though the proposed amplifier without using inductors has some disadvantages versus the other one, in many applications the reduced fabrication complexity ad area may make the trade-off worthwhile.

Different feedback topologies will be shown in Appendix C. Noise Figure has been improved with these new topologies. Though it has disadvantage of the number of supply voltage, it can be the right amplifier for UWB receiver. The next step will be optimizing these new topologies.

[1] Kuan-Hung Chen and Chorng-Kuang Wang, "A 3.1 GHz CMOS Cascaded Two-stage Distrubuted Amplifier for Ultra-Wideband Application," IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, pp. 296-299, 2004.

[2] Vishwakarma, S., Sungyong Jung, Youngjoong Joo, "Ultra Wideband CMOS Low Noise Amplifier with Active Input Matching," Ultra Wideband Systems, 2004. Joint with Conference on Ultrawideband Systems and Technologies. Joint UWBST & IWUWBS. 2004 International Workshop on 18-21 May 2004 pp. 415 - 419

[3] Heechan Doh, Youngkyun Jeong, and Sungyong Jung, "Design of CMOS UWB Low Noise Amplifier with Cascode Feedback," The 47th IEEE International Midwest Symposium on Circuits and Systems, pp. II-641-644.

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[7] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge, U.K.: Cambridge Univ. Press, 1988.

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[9] Gerold W. Neudeck and Robert F. Pierret, "Field Effect Devices," 2nd edition, Addison-Wesley Publishing Company, inc. 1990

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[14] Adel S. Sedra, "Microelectronic Circuits," 5th Edition, Oxford University Press, 2004

[15] Reinhold Ludwig and Pavel Bretchko, "RF Circuit Design Theory and Applications," Prentice Hall, 2000

[16] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits," 4th Edition, Wiley, 2001

APPENDICES

APPENDIX A

MOSFET ELECTRICAL PARAMETERS[19]

A.1 0.18 μm MOSFET

```
SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Feb 19/04
* LOT: T3CV                    WAF: 5097
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1          TNOM    = 27               TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17        VTH0    = 0.3715978
+K1      = 0.5857966    K2      = 3.370488E-3      K3      = 1.142595E-3
+K3B     = 1.31638      W0      = 1E-7             NLX     = 1.800732E-7
+DVT0W   = 0            DVT1W   = 0                DVT2W   = 0
+DVT0    = 1.1791332    DVT1    = 0.357396         DVT2    = 0.0460611
+U0      = 269.6317621  UA      = -1.432404E-9     UB      = 2.452385E-18
+UC      = 6.782724E-11 VSAT    = 1.169395E5       A0      = 2
+AGS     = 0.4555686    B0      = 1.289286E-7      B1      = 5E-6
+KETA    = -0.0121019   A1      = 7.857827E-4      A2      = 0.7688367
+RDSW    = 146.8801646  PRWG    = 0.5              PRWB    = -0.2
+WR      = 1            WINT    = 0                LINT    = 1.348283E-8
+XL      = 0            XW      = -1E-8            DWG     = -3.085532E-9
+DWB     = 2.220704E-9  VOFF    = -0.0950787       NFACTOR = 2.2758058
+CIT     = 0            CDSC    = 2.4E-4           CDSCD   = 0
+CDSCB   = 0            ETA0    = 3.004568E-3      ETAB    = 6.031239E-5
+DSUB    = 0.0117103    PCLM    = 0.9429049        PDIBLC1 = 0.2453788
+PDIBLC2 = 2.239981E-3  PDIBLCB = -0.1             DROUT   = 0.8449584
+PSCBE1  = 1.455122E9   PSCBE2  = 9.343513E-10     PVAG    = 0.2868374
+DELTA   = 0.01         RSH     = 6.7              MOBMOD  = 1
+PRT     = 0            UTE     = -1.5             KT1     = -0.11
+KT1L    = 0            KT2     = 0.022            UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11         AT      = 3.3E4
+WL      = 0            WLN     = 1                WW      = 0
+WWN     = 1            WWL     = 0                LL      = 0
+LLN     = 1            LW      = 0                LWN     = 1
+LWL     = 0            CAPMOD  = 2                XPART   = 0.5
+CGDO    = 8.52E-10     CGSO    = 8.52E-10         CGBO    = 1E-12
+CJ      = 9.52372E-4   PB      = 0.8              MJ      = 0.3773036
+CJSW    = 2.531918E-10 PBSW    = 0.8              MJSW    = 0.1575623
+CJSWG   = 3.3E-10      PBSWG   = 0.8              MJSWG   = 0.1575623
+CF      = 0            PVTH0   = -1.120319E-4     PRDSW   = -3.8025797
+PK2     = -1.177563E-4 WKETA   = -4.321643E-4     LKETA   = -2.994344E-3
+PU0     = 12.4406965   PUA     = 3.528405E-11     PUB     = 0
+PVSAT   = 1.478512E3   PETA0   = 1.003159E-4      PKETA   = 2.775872E-4     )
*
```

[19] From http://www.mosis.org website

A.2 0.5 μm MOSFET

```
SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Apr  9/02
* LOT: T22Y                    WAF: 1102
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                    LEVEL    = 49
+VERSION = 3.1            TNOM    = 27                 TOX      = 1.39E-8
+XJ      = 1.5E-7         NCH     = 1.7E17             VTH0     = 0.6695207
+K1      = 0.8694489      K2      = -0.0917188         K3       = 25.6919711
+K3B     = -7.3653322     W0      = 1E-8               NLX      = 1E-9
+DVT0W   = 0              DVT1W   = 0                  DVT2W    = 0
+DVT0    = 2.7518708      DVT1    = 0.4157316          DVT2     = -0.1405757
+U0      = 459.4342532    UA      = 1E-13              UB       = 1.522944E-18
+UC      = 1.874362E-11   VSAT    = 1.487444E5         A0       = 0.5981684
+AGS     = 0.1306288      B0      = 2.521977E-6        B1       = 5E-6
+KETA    = -4.514909E-3   A1      = 7.33129E-5         A2       = 0.4029659
+RDSW    = 1.564889E3     PRWG    = 0.027362           PRWB     = 0.0392247
+WR      = 1              WINT    = 2.520232E-7        LINT     = 3.653372E-8
+XL      = 0              XW      = 0                  DWG      = -1.17306E-8
+DWB     = 5.311566E-8    VOFF    = -5.688886E-4       NFACTOR  = 1.0780094
+CIT     = 0              CDSC    = 2.4E-4             CDSCD    = 0
+CDSCB   = 0              ETA0    = 0.0213525          ETAB     = -1.275836E-3
+DSUB    = 0.2490912      PCLM    = 2.5868986          PDIBLC1  = -0.2902944
+PDIBLC2 = 2.407506E-3    PDIBLCB = -0.0307296         DROUT    = 0.6175306
+PSCBE1  = 5.55857E8      PSCBE2  = 5.346571E-5        PVAG     = 0
+DELTA   = 0.01           RSH     = 82.4               MOBMOD   = 1
+PRT     = 0              UTE     = -1.5               KT1      = -0.11
+KT1L    = 0              KT2     = 0.022              UA1      = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11           AT       = 3.3E4
+WL      = 0              WLN     = 1                  WW       = 0
+WWN     = 1              WWL     = 0                  LL       = 0
+LLN     = 1              LW      = 0                  LWN      = 1
+LWL     = 0              CAPMOD  = 2                  XPART    = 0.5
+CGDO    = 2.07E-10       CGSO    = 2.07E-10           CGBO     = 1E-9
+CJ      = 4.190399E-4    PB      = 0.99               MJ       = 0.4442523
+CJSW    = 3.25452E-10    PBSW    = 0.1                MJSW     = 0.1159885
+CJSWG   = 1.64E-10       PBSWG   = 0.1                MJSWG    = 0.1159885
+CF      = 0              PVTH0   = 0.0362863          PRDSW    = -50.9170356
+PK2     = -0.0310644     WKETA   = -0.0155136         LKETA    = 2.178067E-3     )
*
```

APPENDIX B

DESIGNING WITH 0.5 μm MOSFETS

Previous work had been done with TSMC 0.18 μm MOSFETs which was the most current technology and shown the promising results for UWB applications.

In this section, the possibility of 0.5 μm MOSFETs for UWB amplifier will be shown. The main characteristics will be compared with 0.18 μm MOSFETs[20].

Initially, the 1st stage of 0.18 μm design was used as a basic platform. It was much harder to have the desired outputs with 0.5 μm MOSFETs.

The design looks the same as 0.18 μm MOSFETs. However, all the values are different to obtain desired outputs.

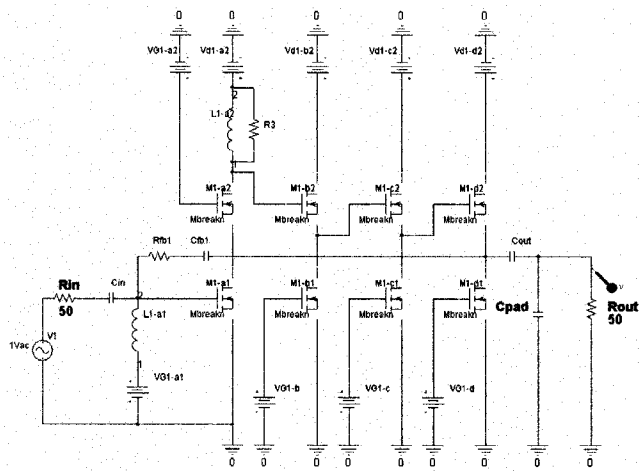

Figure A- 1 Basic circuit with 0.5 μm MOSFETs

[20] The comparison has been done with the 0.18 μm MOSFETs circuit with inductors.

B.1 STAGE EXTENSION

Unlikely 0.18 μm MOSFETs, it requires one more stage which makes it total 3 stages as shown in Figure A-2.

To increase the transducer gain (G_t), additional 3rd stage has been added. The schematic is shown below. The simulation results are shown in section A-2.2.

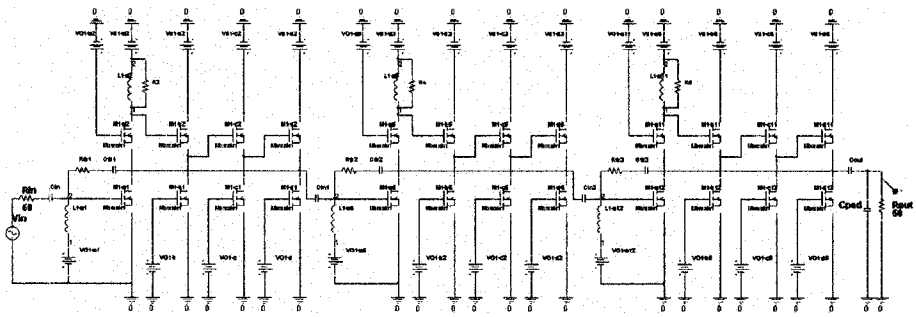

Figure A- 2 UWB amplifier with 0.5 μm MOSFETs

B.2 SIMULATION RESULTS

In this section, the transducer gain (G_t dB), and the noise figure (dB) of 0.18 μm and 0.5 μm will be presented. In addition, the P1 dB will be shown.

B.2.1 TRANSDUCER GAIN (G_t DB)

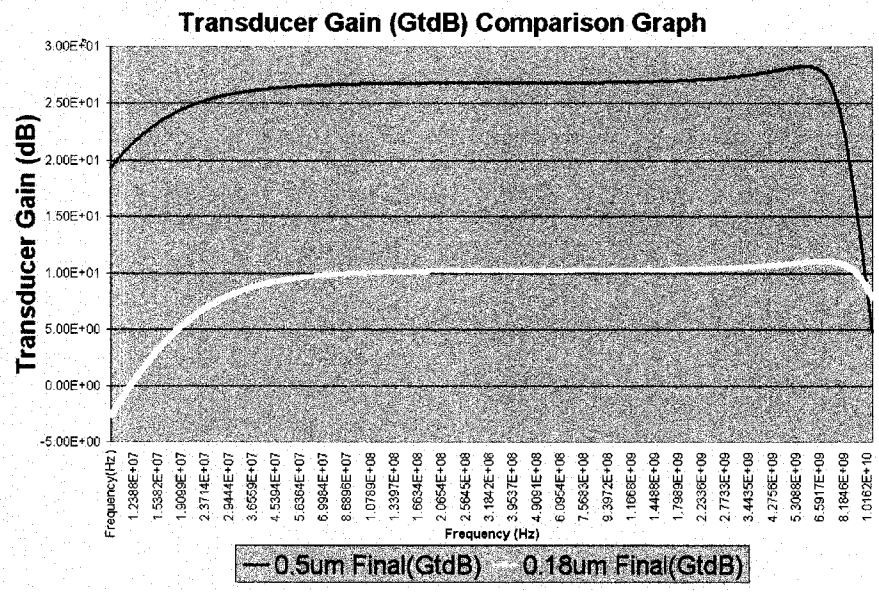

Figure A- 3 Transducer gain comparison graph

0.5 μm MOSFET amplifier gives higher overall transducer gain. However, above 10 GHz, 0.18 μm MOSFET amplifier gives higher gain than 0.5 μm one. Especially in the 10.6 GHz, 0.18 μm MOSFET amplifier gives 7.8 dB whereas 0.5 μm one gives 4.9 dB.

B.2.2 NOISE FIGURE (dB)

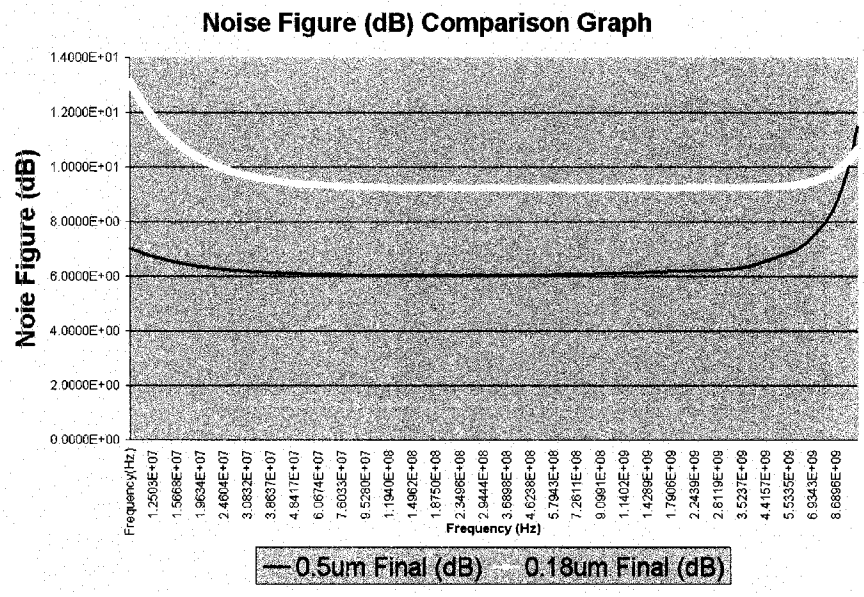

Figure A- 4 Noise Figure (dB) comparison graph

As shown above, 0.5 μm MOSFET amplifier has lower overall Noise figure (dB). However, above 9.954 GHz, 0.18 μm MOSFET amplifier gives lower noise figure than 0.5 μm amplifier. At the 10.6 GHz, 0.18 μm MOSFET amplifier gives 10.62 dB whereas 0.5 μm MOSFET gives 11.49 dB.

B.2.3 1 dB COMPRESSED POWER (P1dB)

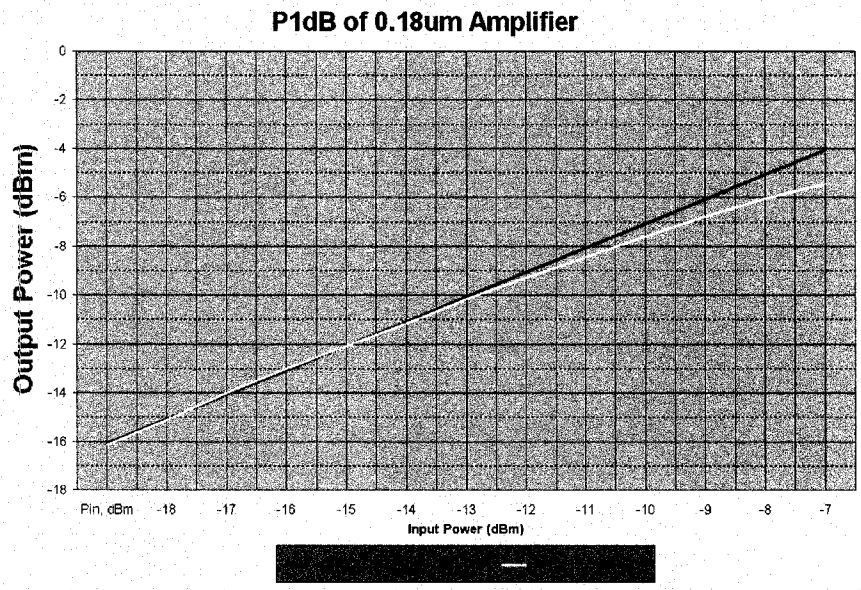

Figure A- 5 P1dB of 0.18 μm MOSFET amplifier

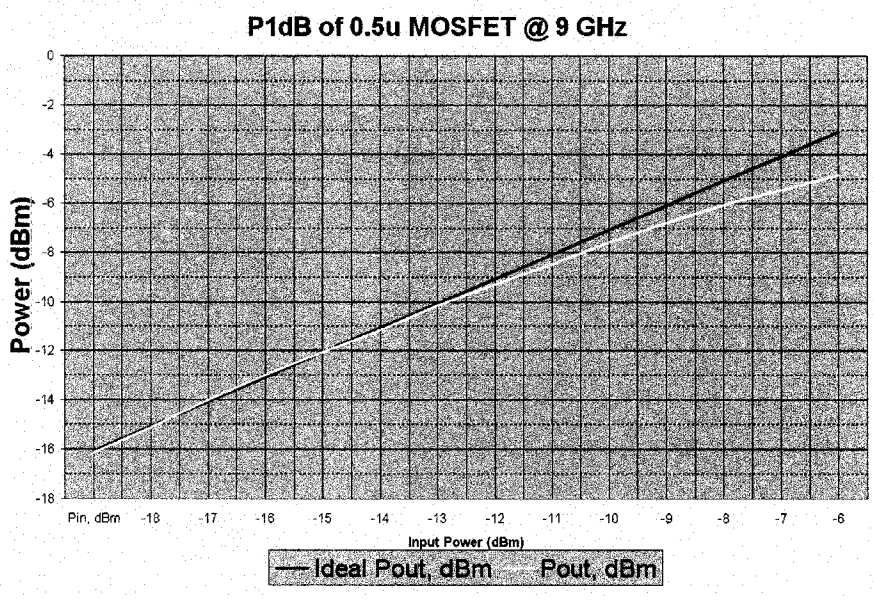

Figure A- 6 P1dB of 0.5 μm MOSFET amplifier

Not like the previous compared results, P1dB are the same between 0.18 μm and 0.5 μm MOSFET amplifiers.

The main purpose of the design with 0.5 μm MOSFETs was checking the possibilities if it was feasible for UWB applications. As the results shown, the overall performances looked fine. However, above 10 GHz, its performances were must worse than 0.18 μm MOSFETs. One of the main reasons was the channel length which was shown in section 3.6.1.1. Other than the test results, the power consumption of the 0.5 μm MOSFET amplifier is approximately 400 mWatts which is not practical for telecommunication applications.

Though it has main degradations above 10 GHz, there are some rooms to enhance its performances mainly through the feedback topologies which will be shown in the next section.

APPENDIX C

OTHER FEEDBACK TOPOLOGIES

In the main sections, the feedback topology with a serial R-C circuit has been used. In this annex, how a different feedback topology makes an effect on the performances will be shown mainly for the Noise figure (dB).

Previously R-C series-connected feedback topology has been utilized. In this section, R-C parallel-connected feedback topology with a little bit different schematics will be used and compared with.

C.1 SCHEMATICS WITH R-C PARALLEL-CONNECTED FEEDBACKS

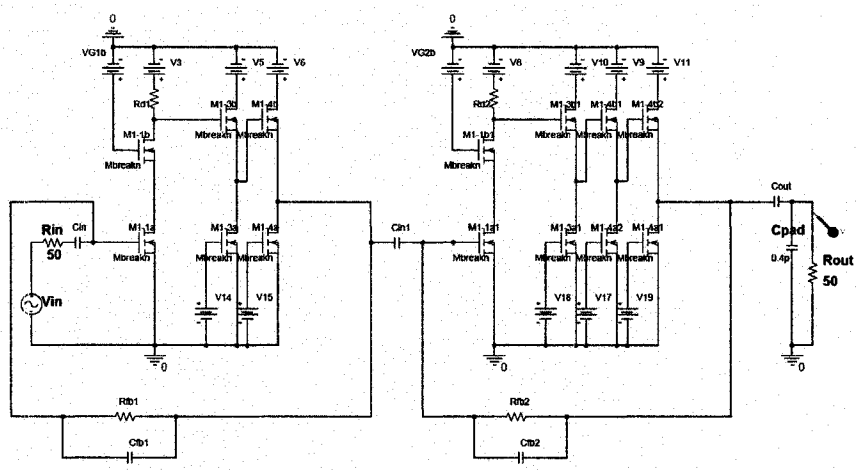

Figure A- 7 Schematic with R-C parallel-connected feedbacks

The major changes of this circuit are the feedback topologies. As shown in Figure A-7, instead of R-C series-connected, R-C parallel-connected topologies are used. By using these topologies, the number of stages can be reduced. The other characteristics will be shown in the latter sections.

C.2 TRANSDUCER GAINS (G_t dB)

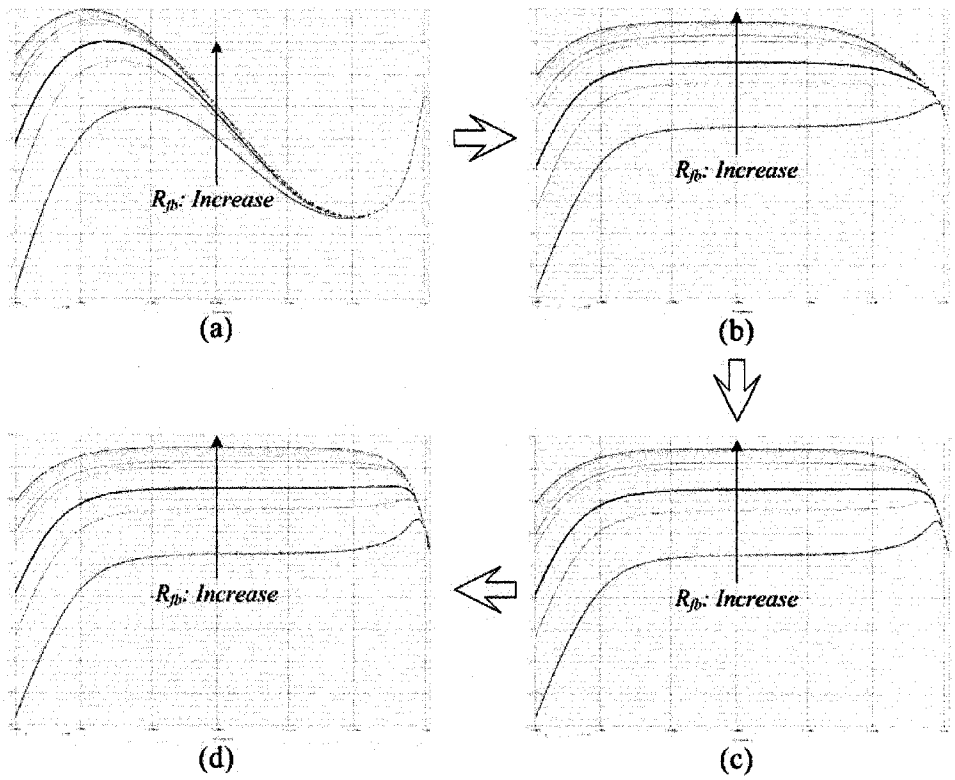

Figure A- 8 Transducer gains (G_t dB) with different feedback resistances and capacitances.

Figure A-8 shows the changes of Transducer gains with different feedback resistances and capacitances. The amplifier does not work until the feedback capacitance is 0.01nF (Figure A-8 (a)). The frequency response is getting better with decreasing the feedback capacitances until 0.001pF (Figure A-8 (d)). The frequency response can be improved a little bit by peaking phenomena with 0.001pF (Figure A-8 (d)) versus 0.01pF (Figure A-8 (c)).

From the simulation result, the optimized feedback resistance is 250 Ohm. With this feedback resistance, Transducer gains with different feedback capacitances will be shown in Figure A-9.

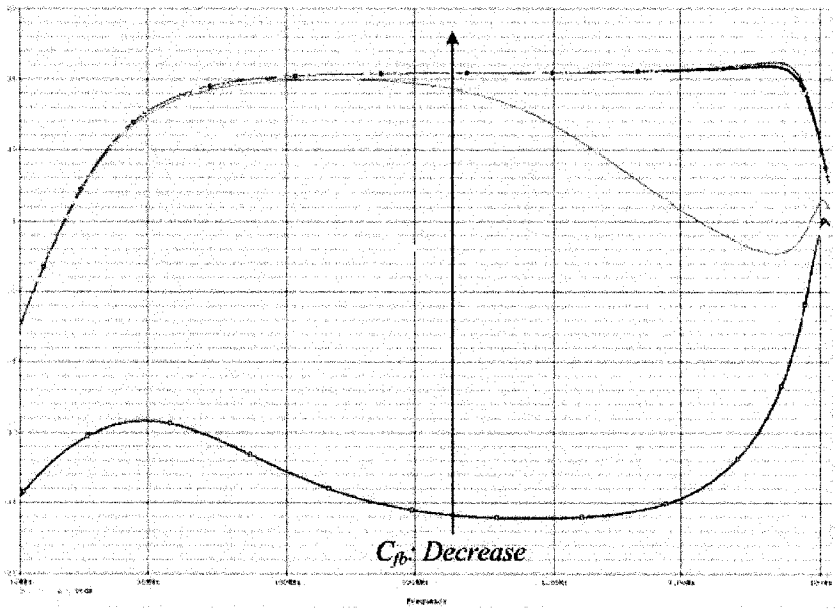

Figure A- 9 Transducer gain (G_t dB) with different feedback capacitances with a fixed feedback resistance (250 Ohm)

Figure A-9 shows the Transducer gains (G_t dB) with different feedback capacitances with a fixed feedback resistance 250 Ohm which is found from previous simulations. The frequency response was the best with 0.001pF.

C.3 NOISE FIGURE (NF dB)

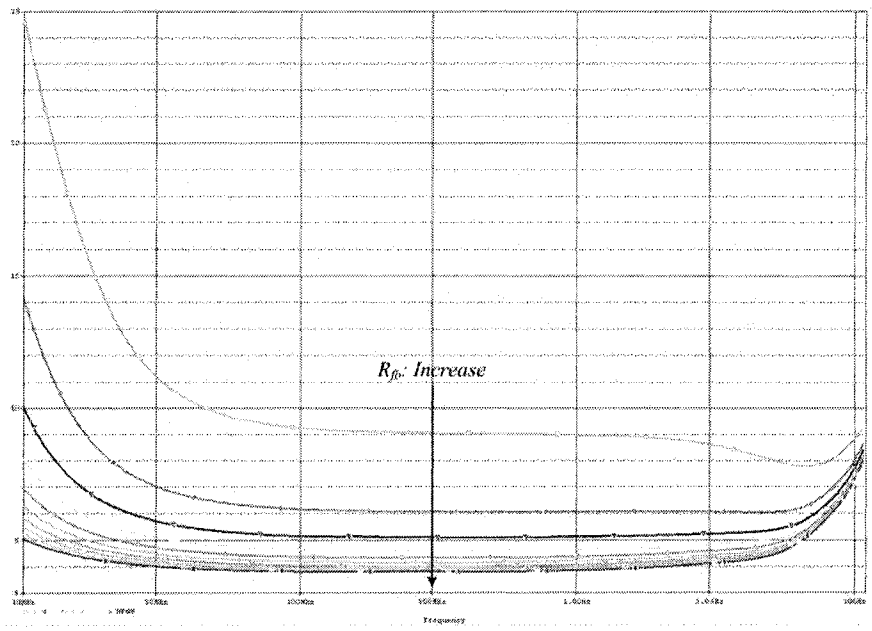

Figure A- 10 Noise figure (dB) variations with different feedback resistances

Figure A -10 shows the Noise figure variations with different feedback resistances from 100 Ohms to 1 kOhms with a fixed feedback capacitance 0.001pF. It shows that the higher feedback resistance, the lower noise figure can be achieved.

With the previous Transducer gain results, the optimized feedback resistance would be 300 Ohms with the capacitance 0.001pF.

APPENDIX D

CONCLUSIONS OF THE ANOTHER FEEDBACK TOPOLOGIES

In this Annex, a different feedback topology has been shown and analyzed. One of the main advantages of this new approach is the lower Noise figure which is the most important factor in a receiver. In addition, another advantage is the number of elements. The numbers of MOSFETs are decreased from 20 MOSFETs to 14 MOSFETs. The approximate power consumption of this new design is 89.8 mWatts which is about the same as the previous design (92.8 mWatts). The disadvantage of this new design is using two different drain voltages of 5 V and 3 V whereas the previous design uses one drain voltage of 5 V.

This new design with R-C parallel-connected topology gives very promising results. In future, more optimizations should be done to have better performances to meet UWB applications.

VITA

Kyoung D. Kim was born in Incheon, Republic of Korea, on March 7, 1967, the sun of Myeong K. Kim and Dong H. Jung. After completing Ajou University in Suwon 1994 he started working as EMC Applications/Systems engineer at Kwang Wha Trading in Republic of Korea. In 1998 he started working as EMC Applications/Systems engineer at TDK RF Solutions (former EMC Automation) in Cedar Park, Texas. He built 9 years of professional career as EMC engineer and started studying at the University of Texas Pan American. He is currently working as a research assistant of the University of Texas Pan American. He will be graduating from the Engineering Master's Program with an electrical major in May 2006.