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Subthreshold 3 Phase Mixers

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SUBTHRESHOLD 3 PHASE MIXER

A Thesis

by

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ABSTRACT

Torres, Jesus A., Subthreshold 3 Phase Mixer. Master of Science (MS), December, 2011, 57 pp., 40 figures, 23 references.

This thesis will discuss subthreshold FET mixers with a focus on conversion loss derivations. To begin understanding the mixers, a look into the FET model is first taken in Chapter II. Then in Chapter III, a single FET device mixer is studied and its conversion loss is found from its small-signal model. The chapter will then include a two FET device mixer and a four device FET mixer. Finally a new type of mixer will be discussed in Chapter IV.

The new type of mixer is a 3 phase mixer with the phase angles being 0°, 120°, and 240°. The theoretical conversion loss is found by treating the FETs as simple switches and a square wave as the RF signal. The resulting conversion loss is shown to be better than the previous mixers mentioned. The thesis will conclude with a discussion of future areas of work for the mixer.

DEDICATION

This thesis is dedicated to my family who has supported and helped me throughout my education. Without them none of this could have been possible.

ACKNOWLEDGEMENTS

I would like to acknowledge my thesis committee for their help throughout the thesis research. They have given me a great deal of knowledge to get through my graduate studies.

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CHAPTER I

INTRODUCTION

1.1 Background of mixers

Many great advances in technology have emerged during the darkest hour of mankind, such as a war, and the mixer is one of those examples. Major Edwin Armstrong is given credit as creating the mixer and is the inventor of the super heterodyne receiver. The mixers of that time used vacuum tubes, instead of semiconductor devices, to convert a radio frequency (RF) into an intermediate frequency (IF) by the help of a local oscillator (LO). It was not until World War II that mixer design really took off.

This was due in part thanks to the Massachusetts Institute of Technology Radiation Laboratories (MIT Rad Lab) for their efforts in creating a radio system to pin point the location of specific targets at a distance. This was later named by the Navy as Radio Detection and Ranging (RADAR). Where a RADAR is essentially a microwave transmitter and receiver that uses a mixer to either upconvert or downcovert a signal. Major Edwin Armstrong's use of vacuum tubes in mixers proved to work quite well, but RADAR systems needed to be more efficient. Throughout the next years diode fabrication improved which lead to higher mixer efficiency. Currently diode based mixers have reached research maturity, and semiconductor devices have expanded to the development of field-effect transistors (FETs). Currently active research in mixers has been to incorporate FETs into mixers.

1.2 Semiconductor devices for mixers

The transition into semiconductor devices is due in part because it has improved mixer conversion loss. Other benefits are that the frequency can be increased far into the gigahertz area and the mixer will also have low-noise, where both tend to coincide almost as a byproduct of each other. The semiconductor devices that have been used before are the point-contact diode and the Schottky diode. Both diodes are somewhat similar in some sense, because they involve a semiconductor piece with metal. The point-contact diode is exactly what the name implies; a conductive piece of metal with a sharp point makes contact with an n-type semiconductor. The Schottky diode has a bigger surface area which makes contact between the metal and the semiconductor. This makes a metal-semiconductor junction and forms a Schottky barrier. With better fabrication process this Schottky barrier could be achieved in metal-semiconductor FETs (MESFETs), which are fabricated from Gallium Arsenide (GaAs). The interest to use these types of FETs with mixers is that conversion gain can be achieved rather than loss due to a transistor's transconductance.

Another key point is that a mixer composed of GaAs MESFETs can be implemented in monolithic microwave integrated circuits (MMICs). Diodes may also be fabricated into MMICs but they have to follow the same template as a transistor and this will cause problems in producing high quality diodes. Necessary balun circuits for diodes are also another problem when fabricating them for MMIC, which requires them to be built separately or in the majority of the cases an RF transformer is used. A FET mixer may use planar baluns that will be easier to implement in MMICs.

Another transistor that has also appeared is the high electron mobility transistor (HEMT) which is made from gallium nitride (GaN). These transistors work in higher frequencies and

handle more power than GaAs MESFETs, although several HEMT devices are also made from GaAs. Both GaAs MESFETs and GaN HEMTs can be incorporated into MMICs either as GaAs MMICs or GaN MMICs.

1.3 Mixer Basics

An RF mixer can essentially be thought of as a multiplier where two signals will be multiplied. In this case the RF signal will be multiplied by the LO signal and one of the outputs is filtered out. The remaining output signal is called the IF signal as in Figure 1.3.1. Normally the LO signal is applied to the gate of a FET device and causes its transconductance or conductance to vary. Thus the LO signal is sometimes called the pump waveform. The output of Figure 1.3.1 is an ideal case generally a non-linear device will exhibit LO harmonics.

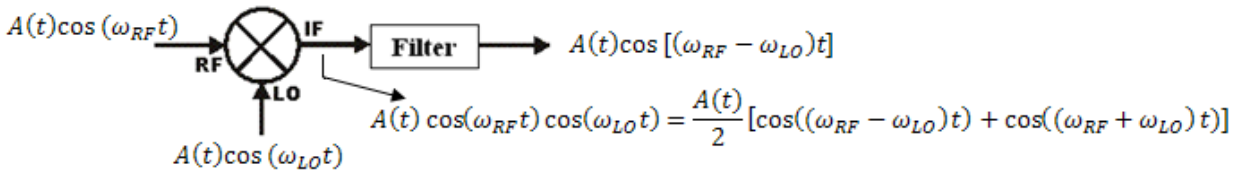

Figure 1.3.1: Ideal RF Mixer

The mixer can be designed as a single FET device shown in Figure 1.3.2, two devices called singly balanced shown in Figure 1.3.3, or four devices called doubly balanced shown in Figure 1.3.4. In some cases the FET device can have a dual gate, but in this thesis dual gate FETs will not be shown. Each mixer has its own advantages and will be discussed further. It is also important to note that no drain bias will be applied making these mixers resistive.

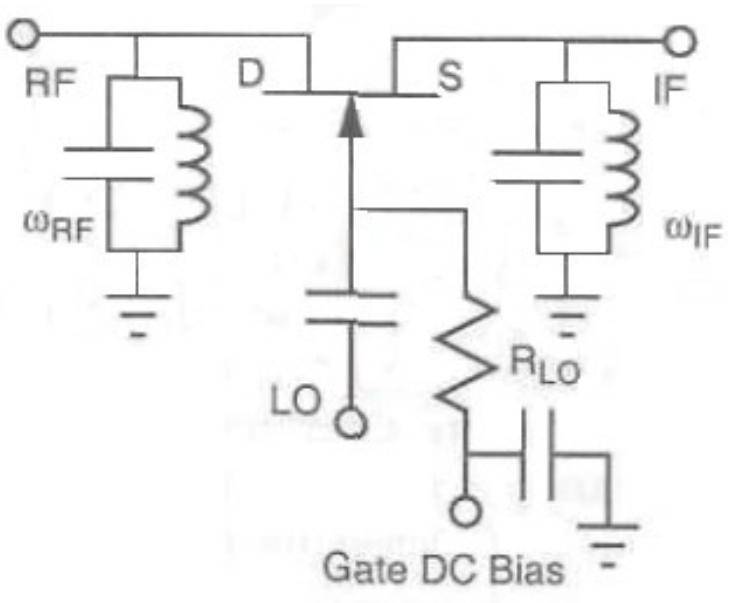

Figure 1.3.2: Single Device Resistive FET Mixer

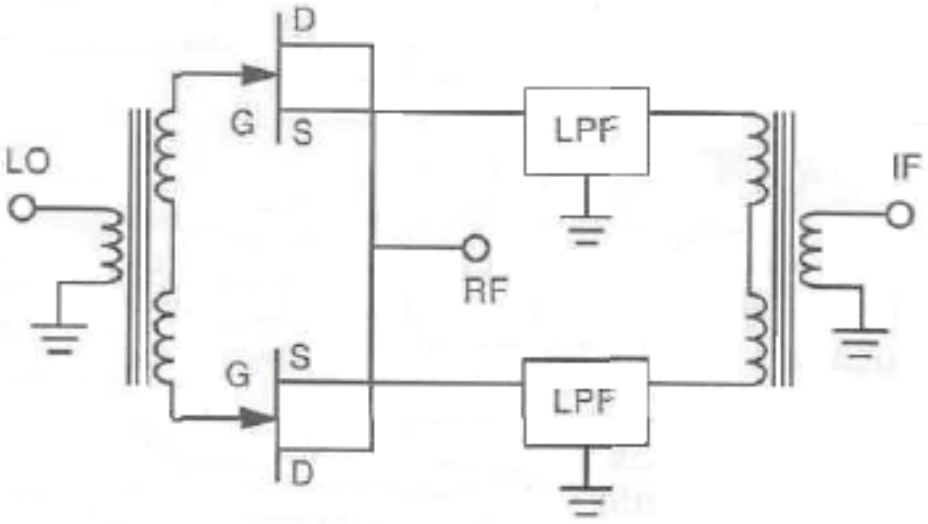

Figure 1.3.3: Singly Balanced Resistive FET Mixer

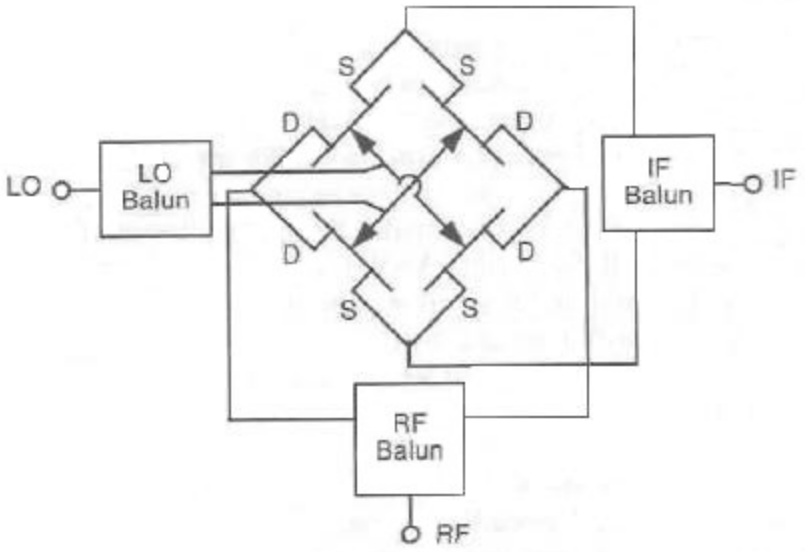

Figure 1.3.4: Doubly Balanced Resistive FET Mixer

1.4 Thesis Proposal

The thesis deals with subthreshold type mixers where the main goal is to improve the conversion loss. A background in existing mixers will be shown to understand how a mixer operates and derivations for conversion loss will be studied. A 3 phase mixer will be introduced in the end as a new type of mixer.

1.5 Thesis Outline

This thesis has been prepared as the following chapters. Chapter II discusses the MESFET transistors used by demonstrating the large signal and small signal models. The chapter will briefly discuss a de-embedding process that was taken to obtain some of its values. Chapter III deals with the mixers that were introduced at the beginning of this chapter. A conversion loss derivation of a single FET mixer will be discussed and show how to implement it with other types of mixers. Chapter IV will carry out the implementation of the mixers and its simulated results. Finally Chapter V will conclude the thesis and will mention steps for future work.

CHAPTER II

FET DEVICES

As mentioned before, the device that was chosen for this thesis was a MESFET device. For subthreshold mixers, the device is biased at a voltage slightly below its threshold voltage and V_d is kept at 0 volts DC. This chapter will discuss the large-signal model, small-signal model and device measurements for modeling. Agilent ADS software was used to perform nonlinear simulations.

2.1 Large-Signal Model

A large-signal model is needed for non-linear devices to characterize the internal elements as non-linear equations. These non-linear equations are then solved to produce an approximation of the device behavior. The large-signal model for a MESFET device is shown in Figure 2.1.1 where V_d is biased higher than zero volts. The elements R_{ds} and C_i are used to model the effects of traps in the channel at bias voltage V_d. The capacitance C_{ds} is a small capacitance and at V_d=0 it will be even smaller. Finally the resistance R_i is a resistance created between the gate and the source that comes from the channel.

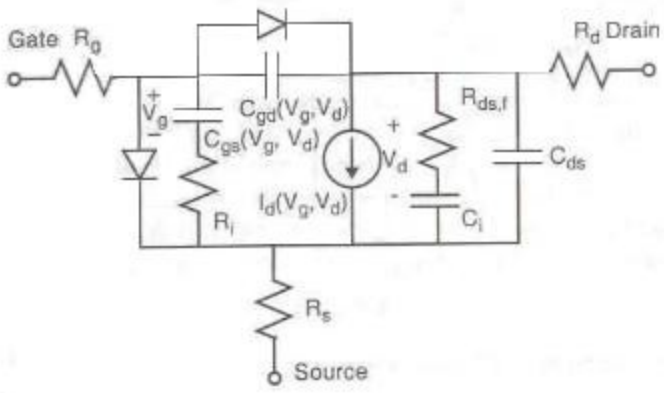

Figure 2.1.1: Large-Signal Model of MESFET - With Drain Bias

The main elements to take into consideration when converting to the resistive model are R_i, C_i, R_{ds}, and C_{ds}. All of these elements can be omitted because for resistive mixer there will be no drain bias and thus those elements will be negligible. The large-signal model is greatly reduced and is shown in Figure 2.1.2.

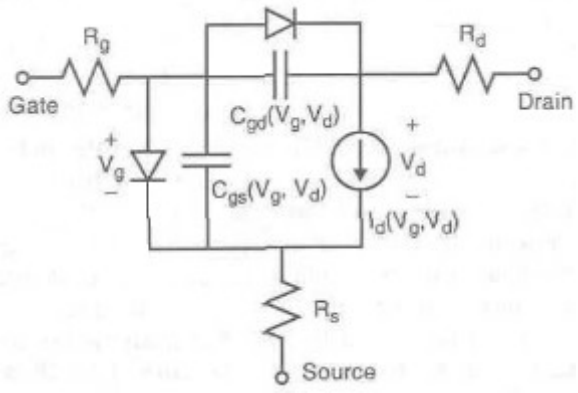

Figure 2.1.2: Large-Signal Model of MESFET - No Drain Bias

For the resistive mixer the gate is kept near its threshold voltage and with no bias at the drain the I_dV_d models have to be adjusted to work for resistive FETs. The problem is that the existing FET I_dV_d models are for active devices as discussed in [1,4,6]. To model low drain voltages the drain current can be modeled as:

$$I(V_g, V_d) = I_1\{3[u^2(V_g, V_d) - u^2(V_g, 0)] - 2[u^3(V_g, V_d) - u^3(V_g, 0)]\}$$

where $u(V_g,V_d)$ is the normalized depletion width:

$$u(V_g, V_d) = \sqrt{(V_d + V_g + \varphi)/V_p}.$$

V_p is the pinchoff voltage, φ is the gate built-in potential, and I_1 is a constant with dimensions of current. The channel conductance is found by differentiating (1) and leaving V_d=0:

$$g(V_g) = 3I_1(1 - u(V_g, 0))/V_p.$$

The capacitance C_{gd} is an ideal Schottky-barrier capacitance and is shown as:

$$C_{gd}(V_g) = C_{gd0}(1 - \frac{V_g}{\varphi})^{-0.5}.$$

The MESFET transistor that was available to use in ADS is from NEC with model number NE71000. The I_dV_d curves were measured in ADS, simulation setup shown in Figure 2.2.1, and are shown in Figure 2.2.2 and Figure 2.2.3.

2.2 Small-Signal Model

With a small-signal model, the idea is to approximate the non-linear devices with linear equations. The small-signal model of a resistive mixer using a MESFET is much simpler as shown in Figure 2.2.4. The main thing to note is the channel conductance in that it is represented as two lumped capacitance, C_{gs} and C_{gd}. When V_{ds}=0, C_{gs}≈C_{gd} and each is half the gate channel conductance. The current I_d is replaced with $g(V_g)$ and will be discussed in the next chapter in further detail.

Figure 2.2.1: ADS FET Curve Tracer Setup

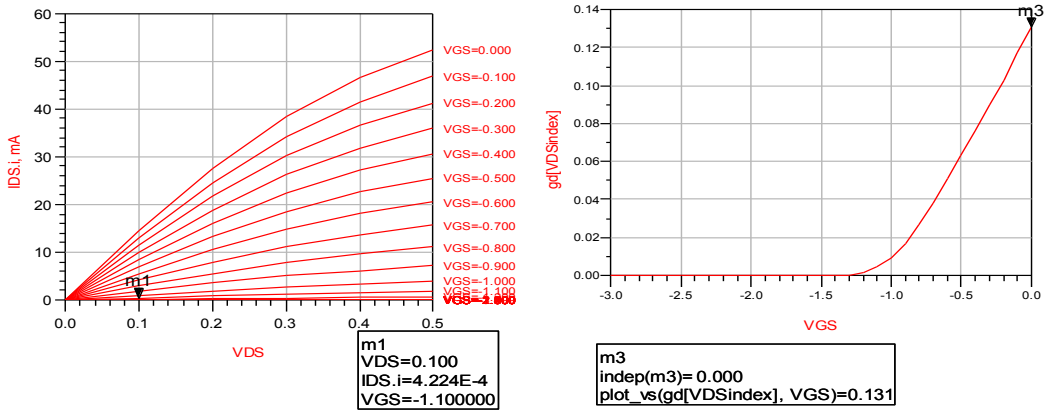

Figure 2.2.2: I-V Curves and Conductance at V_d = 0.1V

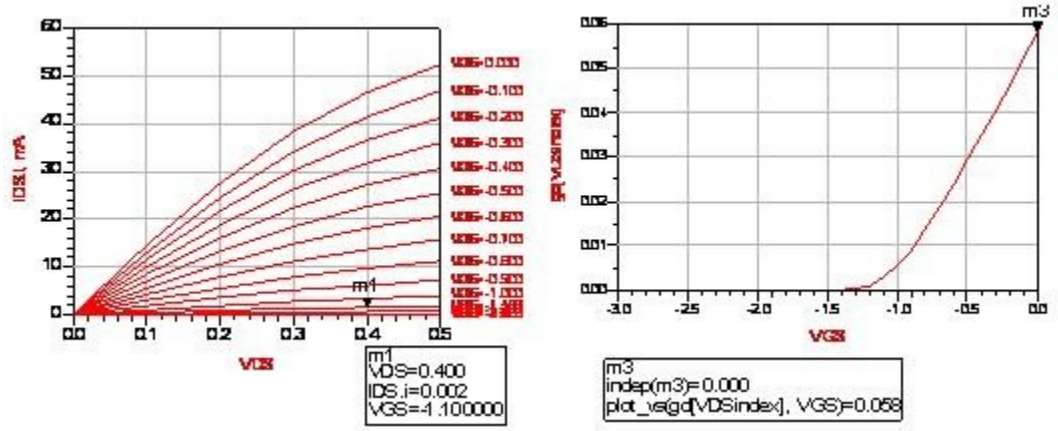

Figure 2.2.3: I-V Curves and Conductance at V_d = 0.4V

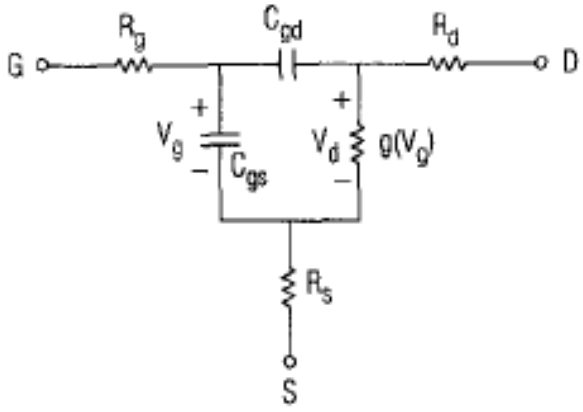

Figure 2.2.4: FET Small-Signal Model - No Drain Bias

2.3 Device Modeling and Parameter Extraction

The resistance and capacitances in the small-signal model can be found by doing a device measurement extraction. The device extraction follows the extraction methods of [17-22] where the extraction is found from using the Cold-FET techniques. The Cold-FET is basically having the device with no drain bias which is very similar to how the FET will be biased. The model for the FET after it has been packaged is shown in Figure 2.3.1 and is similar to Figure 2.2.4. The main concept is to provide a negative bias to pinch of the gate and drain., then measure the Y-parameters from the device and find the package capacitors by using the imaginary portion of the Y-parameters. After finding these capacitances the next step is to bias the gate with a positive voltage and find the Z-parameters. From the Z-parameters the values of the capacitance are subtracted and the parasitic inductances can be found from the imaginary part. The real part of the Z-parameters is used to solve for the parasitic resistances R_g, R_s, and R_d. The device from ADS is a NE71000 MESFET and the setup for the extraction is shown in Figure 2.3.2.

The package capacitors are then found as such:

$$Vd = 0\ V,\ Vs = 0\ V,\ Vg = -1.8V,$$

$$C_{pgd}=Im(-Y_{12})/\omega$$

$$C_{pgs}=Im(Y_{11})/\omega + Im(Y_{12})/\omega$$

$$C_{pds}=IM(Y_{22})/\omega + Im(Y_{12})/\omega$$

where the values are of the capacitances are found from the simulation, shown in Figure 2.3.3:

$$C_{pgd} = 152.5\ fF$$

$$C_{pgs} = 122\ fF$$

$$C_{pds} = 225.8\ fF$$

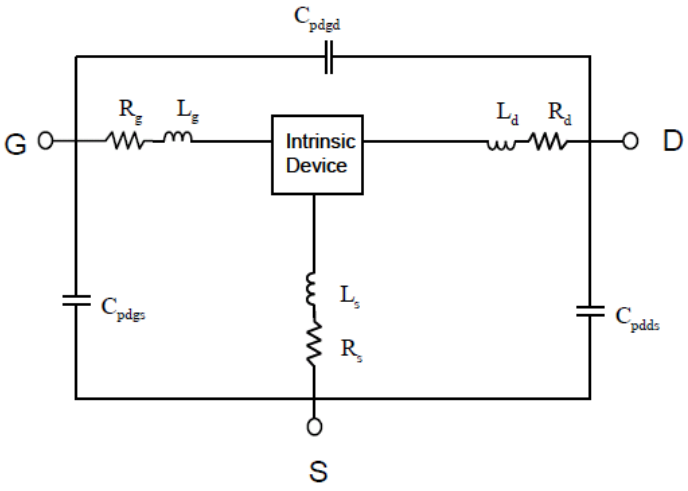

Figure 2.3.1: FET Packaged Model

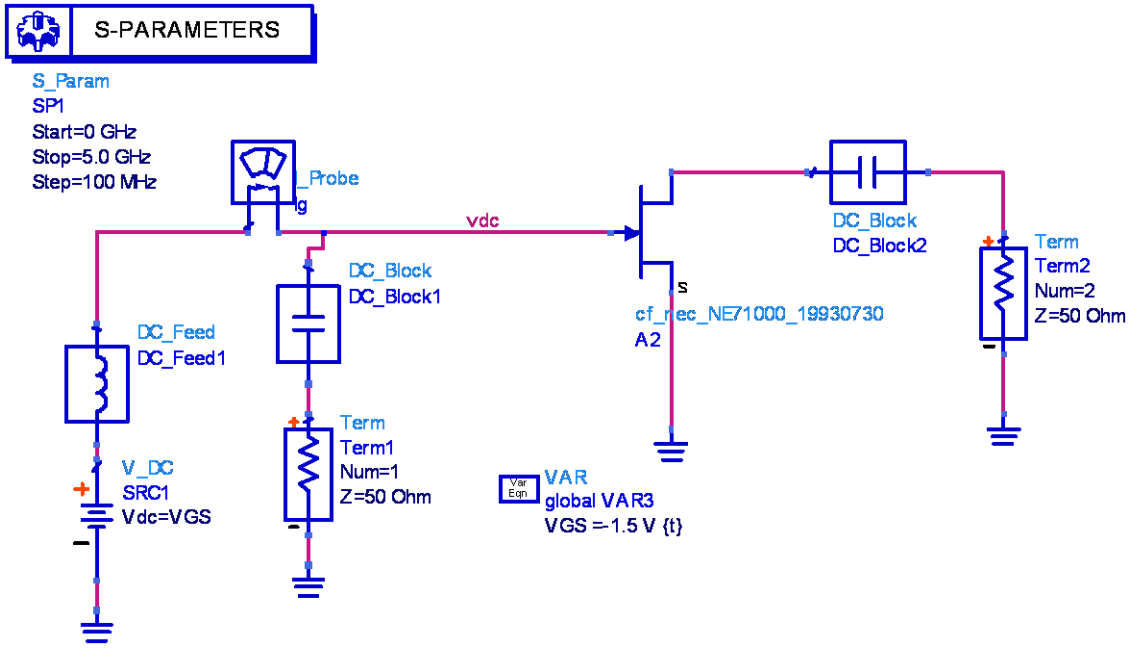

Figure 2.3.2: De-Embed Setup

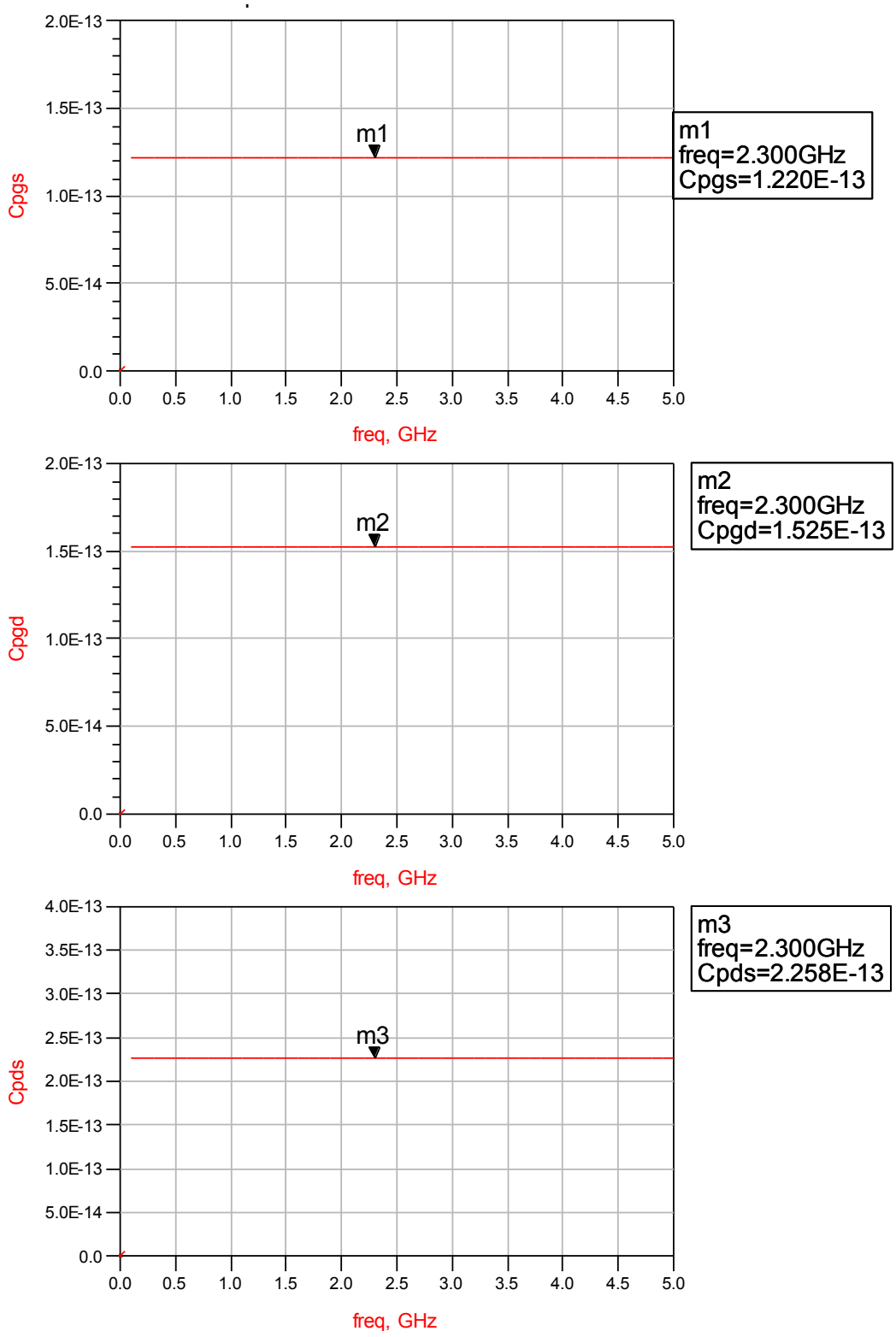

Figure 2.3.3: Package Capacitances

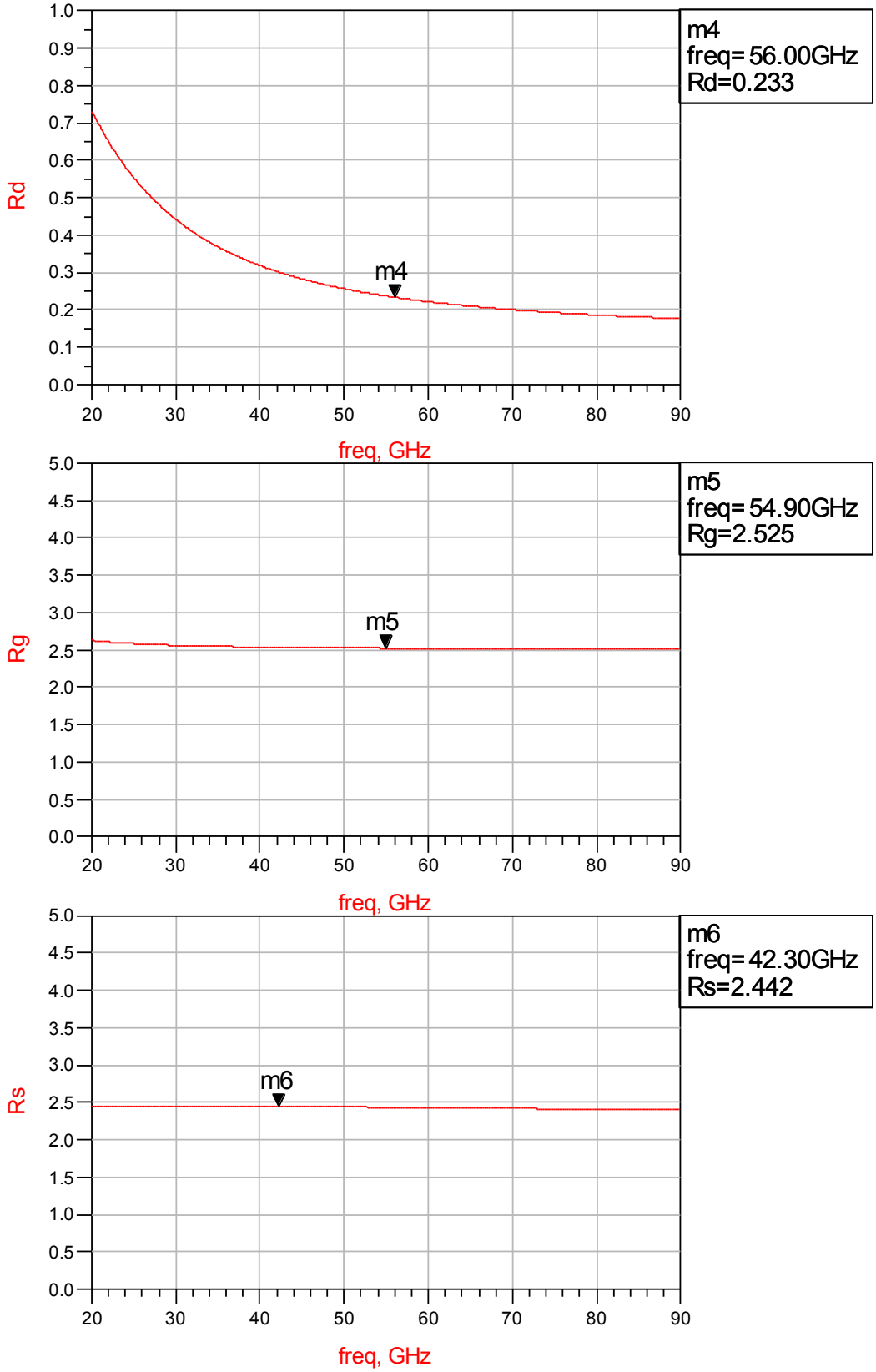

Figure 2.3.4: Extrinsic Resistances

The extrinsic resistances R_d,R_g, and R_s are shown in Figure 2.3.4, where they are found as:

$$Rg = real(Z(1,1)-Z(1,2))$$
$$Rd = real(Z(2,2)-Z(1,2))$$
$$Rs = real(Z(1,2))$$

Vg = 0.5V Frequency: 10 GHz to 90 GHz

Rs = 2.4 ohms

Rg = 2.5 ohms

where R_d appears to be in parallel with a capacitor. MATLAB is used to curve fit and is solved as:

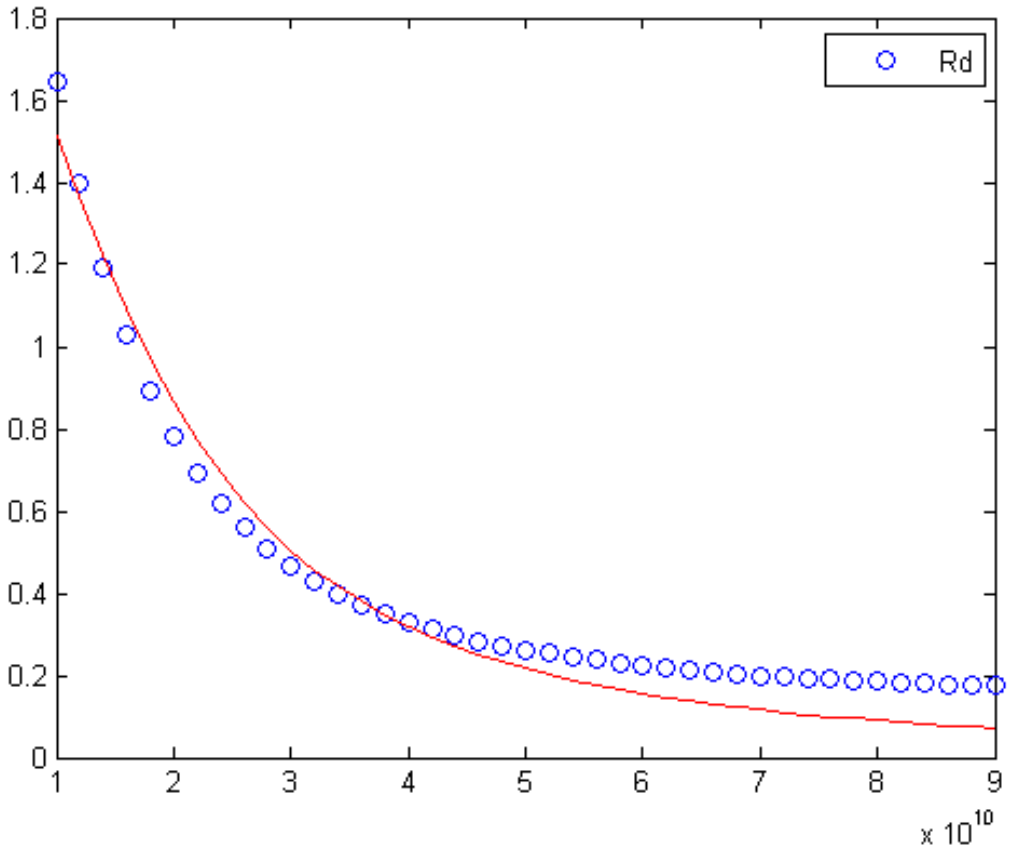

Figure 2.3.5: R_d parallel with a Capacitance

$R_d = 2.02$

Cap_Rd = 4.55 pF

The parameter extraction for the package capacitances and extrinsic resistances were in good accordance with the references. The remainder of the parameters could be found by continuing on the extraction methods. It is important to note that for the device extraction it would be best to run the extraction in a lab with the actual device at hand. The reason being that in ADS the FET NE71000 uses a different transistor model than the models previously discussed. The ADS model for the FET is called EEFET3, shown in Figure 2.3.6. This model is more accurate than the previous model discussed and also would not allow for further parameter extraction since both models are not compatible. In the following chapter the differences between models will be more noticeable from conversion gain simulations.

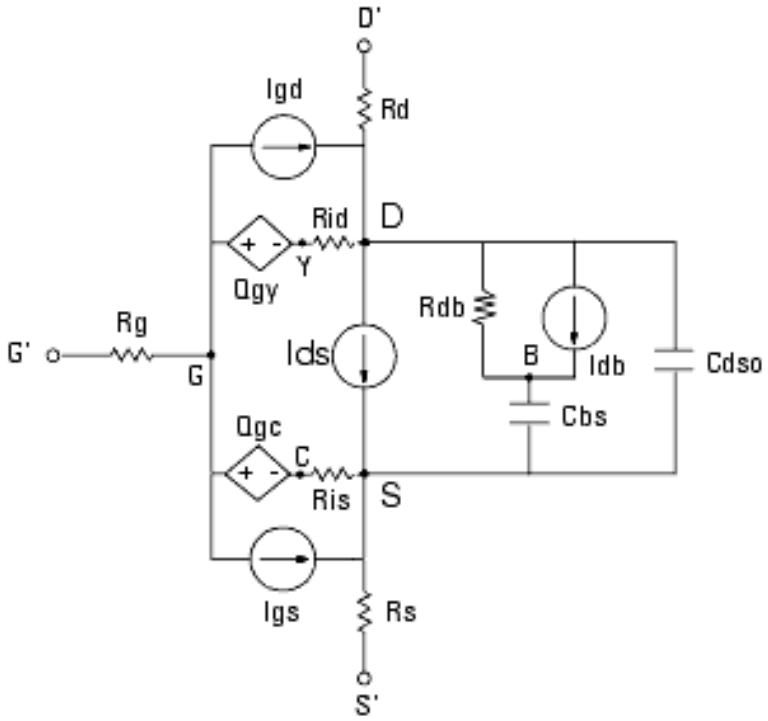

Figure 2.3.6: EEFET3 Model

CHAPTER III

RESISTIVE MIXERS

The purpose of this chapter is to get familiarize with the mixers that are briefly shown in Chapter 1. The conversion gain is solved for a mixer with a single device and then demonstrates how that can be applied to the other types of mixers. The derivations of the single device FET mixer are simulated using MATLAB and compared to ADS Agilent simulations.

3.1 Single Device FET Mixer

The single resistive FET mixer was briefly introduced in chapter 1 and this section will continue with some of its analysis. For a single MESFET mixer, as shown in Figure 3.1.1, the LO is applied to the gate along with a negative dc bias, the RF is applied to the drain, and the IF is filtered from the drain. The RF will use a filter to short-circuit the drain at LO frequency and the LO will also use a filter to short-circuit the RF at the gate. Once again, there must be no DC bias in the drain and the gate bias will be biased at its subthreshold.

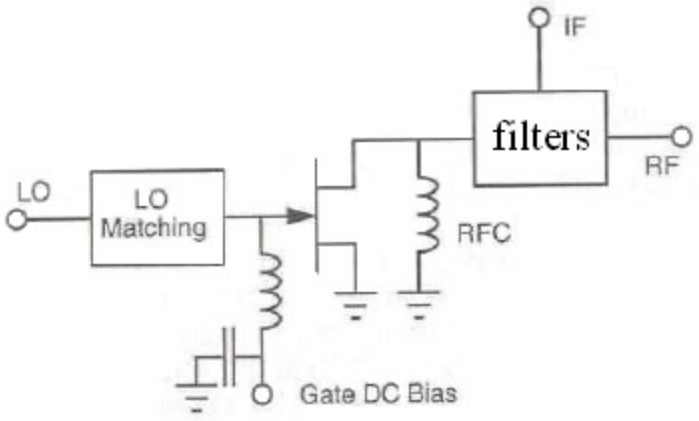

Figure 3.1.1: Resistive FET Mixer Common Source Configuration

If the mixer has taken the appropriate short-circuit design rules mentioned for the RF and LO then some approximations can be taken. The two approximations can be seen in Figure 3.1.2 with part a showing the LO equivalent circuit looking through the gate and the RF equivalent circuit looking through the drain. The conversion gain is then found as follows.

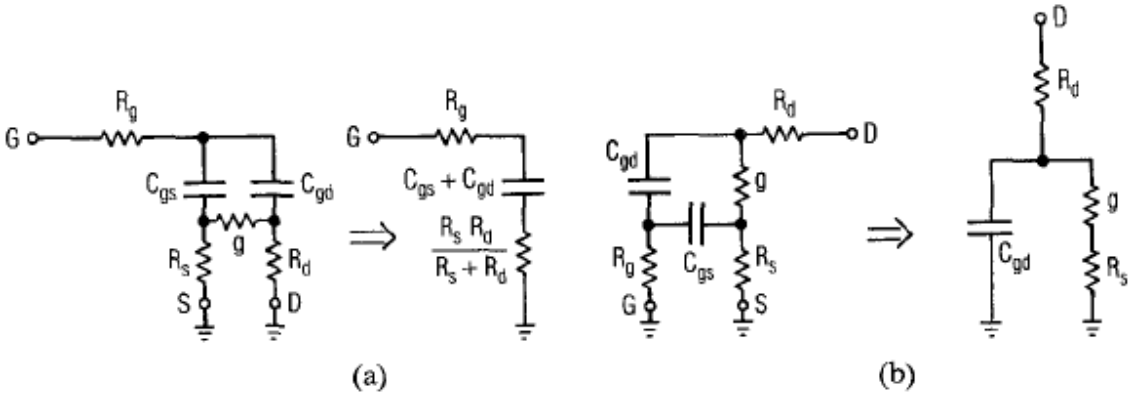

Figure 3.1.2: (a) LO Equivalent Circuit (b) RF Equivalent Circuit

The impedance at the gate is found from Figure 3.1.2 (a) as:

$$Z_{in} = R_g + \frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}.$$

The impedance in the input should be properly matched by the complex conjugate of the input impedance as:

$$Z_g = Z_{in}^* = R_g - \frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}.$$

In time domain $V_s = V_{LO}\cos(\omega_{LO}t)$ and thus in phasor $V_s = V_{LO}\angle 0$, this will be the input signal into the gate. The voltage V_g across the capacitors C_{gs} and C_{gd} is found from Figure 3.1.3 as:

$$V_1 = \frac{\frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}}{Z_g + R_g + \frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}} V_{LO}$$

$$V_2 = \frac{\frac{R_s R_d}{R_s+R_d}}{Z_g + R_g + \frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}} V_{LO}$$

$$V_g = V_1 - V_2 = \frac{\frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}}{Z_g + R_g + \frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}} V_{LO}$$

$$- \frac{\frac{R_s R_d}{R_s+R_d}}{Z_g + R_g + \frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}} V_{LO}$$

$$V_g = \frac{\frac{1}{j\omega_{LO}(C_{gs}+C_{gd})}}{Z_g + R_g + \frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}} V_{LO}$$

$$V_g = \frac{1}{\left(j\omega_{LO}(C_{gs}+C_{gd})\right)\left(Z_g + R_g + \frac{1}{j\omega_{LO}(C_{gs}+C_{gd})} + \frac{R_s R_d}{R_s+R_d}\right)} V_{LO}$$

$$V_g = \frac{V_{LO}}{\left(j\omega_{LO}(C_{gs}+C_{gd})\right)\left(Z_g + R_g + \frac{R_s R_d}{R_s+R_d}\right) + 1}$$

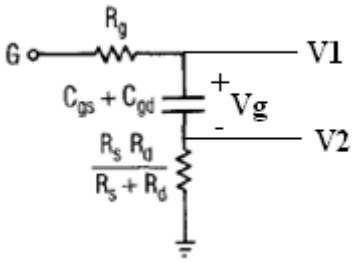

Figure 3.1.3: Finding V_g

This equation is good because it is easier to use in MATLAB were Z_s = 50 ohms would be for unmatched. If Z_s is used to matched then:

$$V_g = \frac{V_{LO}}{2j\omega_{LO}(C_{gs}+C_{gd})(R_g+\frac{R_S R_d}{R_s+R_d})}.$$

The small signal current is found from Figure 3.1.4 where the capacitor is taken out and V_{RF} is left in phasor. Thus V_d is found as:

$$V_x = \frac{\frac{1}{g} + R_s}{R_s + R_d + \frac{1}{g} + Z_d} V_s$$

$$V_2 = \frac{R_s}{\frac{1}{g} + R_s} V_x$$

$$V_2 = \frac{R_s}{(\frac{1}{g} + R_s)} * \frac{(\frac{1}{g} + R_s)}{(R_s + R_d + \frac{1}{g} + Z_d)} V_s$$

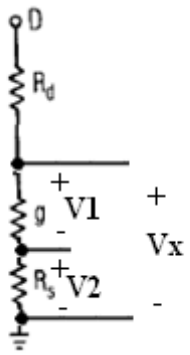

Figure 3.1.4: Simplifying Small-Signal Circuit Looking Through Drain

$$V_2 = \frac{R_s}{R_s + R_d + \frac{1}{g} + Z_d} V_s$$

$$V_d = V_1 = V_x - V_2 = \frac{\frac{1}{g} + R_s}{R_s + R_d + \frac{1}{g} + Z_d} V_s - \frac{R_s}{R_s + R_d + \frac{1}{g} + Z_d} V_s$$

$$V_d = \frac{\frac{1}{g}}{R_s + R_d + \frac{1}{g} + Z_d} V_s$$

$$v_d = \frac{\frac{1}{g}}{R_s + R_d + \frac{1}{g} + Z_d} v_{rf} \cos(\omega_{rf} t)$$

$$i_d = g \frac{\frac{1}{g}}{R_s + R_d + \frac{1}{g} + Z_d} v_{rf} \cos(\omega_{rf} t) = \frac{v_{rf} \cos(\omega_{rf} t)}{R_s + R_d + \frac{1}{g} + Z_d}$$

$$i_d = \frac{g v_{rf} \cos(\omega_{rf} t)}{g(R_s + R_d + Z_d) + 1}$$

Using the conductance and procedure from the paper "A Simplified Method to Predict The Conversion loss of FET Resistive Mixers [5],"

$$G_d = \begin{cases} K(V_g - V_p) & for\ V_g > V_p \\ 0 & for\ V_g \leq V_p \end{cases}$$

Where K is found from the slope of the channel conductance in the on-state, Vg is the internal gate-source voltage, and Vp is the pinch off voltage. Since the device is biased near pinch off the equation is rewritten as:

$$G_d(V_{g,LO}) = \begin{cases} KV_{g,LO}\cos(\omega_{LO}t + \theta) & for \quad -\frac{\pi}{2} \leq \omega_{LO}t + \theta \leq \frac{\pi}{2} \\ 0 & for \quad \frac{\pi}{2} \leq \omega_{LO}t + \theta \leq \frac{3\pi}{2} \end{cases}$$

The equation has $\cos(\omega_{LO}t + \theta)$, which means that there is a phase shift of θ. This comes from the first equation from the phase shift created by the imaginary j on the denominator.

Using Equation 4 and 6:

$$i_d = \frac{KV_{g,LO}\cos(\omega_{LO}t + \theta)\ v_{rf}\cos(\omega_{rf}t)}{KV_{g,LO}\cos(\omega_{LO}t + \theta)\,(R_s + R_d + Z_d) + 1}$$

$$i_d(t) = f(\omega_{LO}t)v_{RF}\cos(\omega_{RF}t)$$

$$f(x) = \frac{KV_{g,LO}\cos(x)}{KV_{g,LO}\cos(x)\,(R_s + R_d + Z_d) + 1}$$

Taking the Fourier transform of Equation 8 to find the fundamental LO frequency component:

$$g_1 = \frac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{KV_{g,LO}\cos(x)}{KV_{g,LO}\cos(x)\,(R_s + R_d + Z_d) + 1}\cos(x)\,dx$$

Equation 7 can now be solved numerically.

Then the current for IF is:

$$i_{d,IF} = \frac{g_1 v_{RF}}{2}\cos((\omega_{LO} - \omega_{RF})t)$$

The IF power is then:

$$P_{IF} = \frac{(g_1 V_{RF})^2}{8}\mathrm{Re}(\mathrm{Z_{D,IF}})$$

The available power is:

$$P_a = \frac{|V_{RF}|^2}{8Re(Z_s)}$$

The conversion gain will be:

$$G_C = \frac{P_L}{P_a} = \frac{\frac{(g_1 v_{RF})^2}{8}\mathrm{Re}(\mathrm{Z_{D,IF}})}{\frac{|V_{RF}|^2}{8Re(Z_s)}}$$

$$G_c = g_1^2 Re\left(Z_{D,IF}\right) Re(Z_s).$$

The derived conversion gain is then compared to the conversion gain from ADS Agilent. The difference in ADS Agilent is that the simulation tool used is called Harmonic Balance. The harmonic balance tool is more accurate in solving nonlinear circuits compared to transient analysis. The circuit setup is shown in Figure 3.1.5 and the mixer is in Figure 3.1.6.

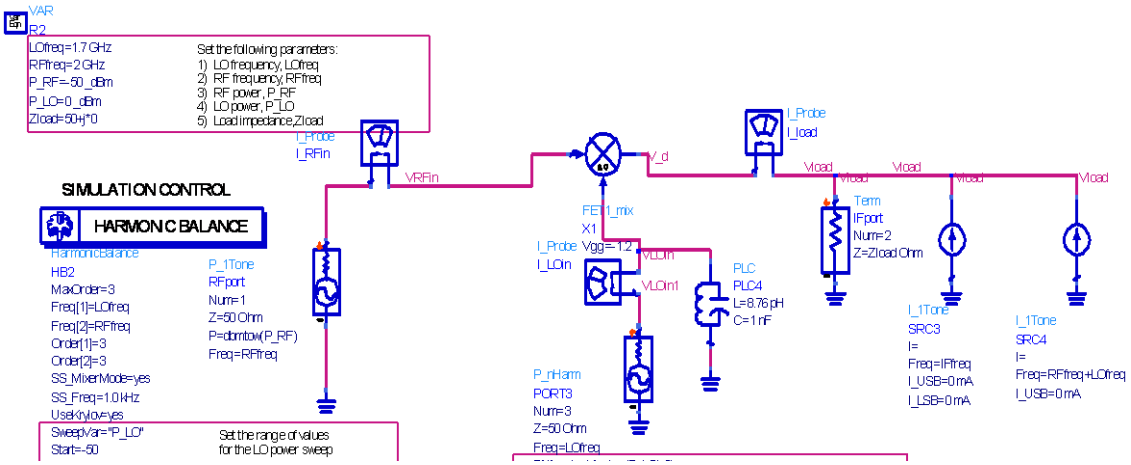

Figure 3.1.5: ADS Agilent Mixer Setup

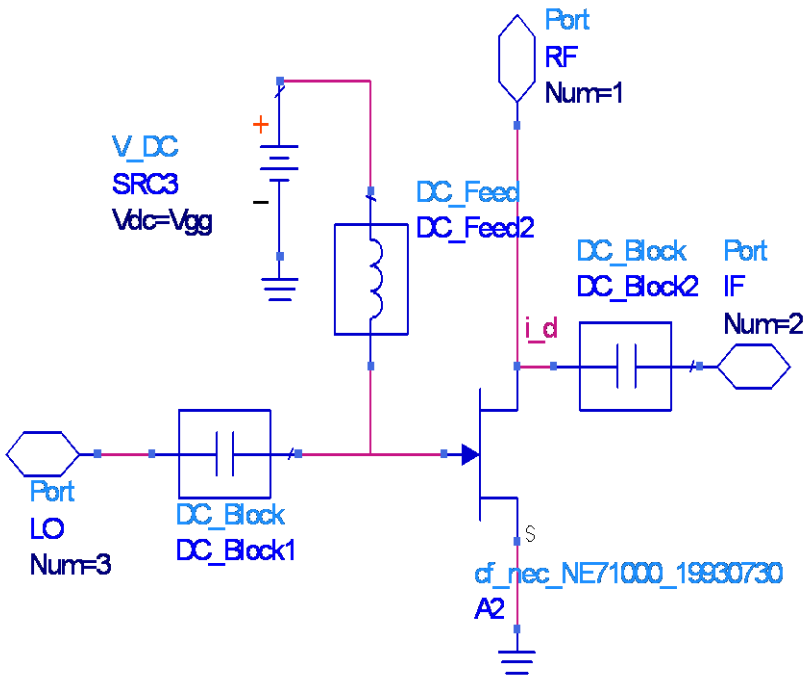

Figure 3.1.6: ADS Agilent Single Device Mixer

Results were obtained from the ADS simulation and compared to the derivations shown throughout Chapter III.1. It should be noted that the simulations are first done with the mixer being unmatched. The reason for this is because from simulations, the impedance looking into the LO and RF gates was roughly about 50-70 ohms with an imaginary component. The mixer was also tested at different frequencies to determine which frequency would give a better conversion loss and it would be tedious to form a matching circuit for each simulation test that was run for each of the frequencies.

The input LO and RF waveforms from ADS are shown in Figure 3.1.7and Figure 3.1.8. Note that the RF waveform is not exactly a sinusoidal waveform and the reason is because of the Harmonic Balance simulation. The waveforms are solved so that they are consistent with the non-linear device. In MATLAB the waveforms are both left as sinusoidal and are shown in Figure 3.1.9 and Figure 3.1.10. The conversion loss is then found from the derivations and ADS,

shown in Figure 3.1.11. The difference in the waveforms could be attributed in that the derivations use a simplified linear model where as in ADS the FET is simulated as non-linear.

The mixer is then changed so that the output IF is extracted through the source as shown in Figure 1.3.2 from Chapter I. The derivation for the conversion loss for this mixer is very similar as before but now there is an impedance connected to the source. The results are showed in Figure 3.1.12 and the ADS waveform appears to have a slight improvement on the conversion loss. The reason of how the waveforms differ this time is due to the source output and the FET is a three terminal device. If the body is tied to the source then the device will tend to be more non-linear. This is commonly done if they do not have a four terminal device because the idea is that the source should be grounded,. The body of the MESFET won't be grounded in this case and will be affected. This effect will also be seen in a singly and doubly balanced mixer if the IF is taken from the source.

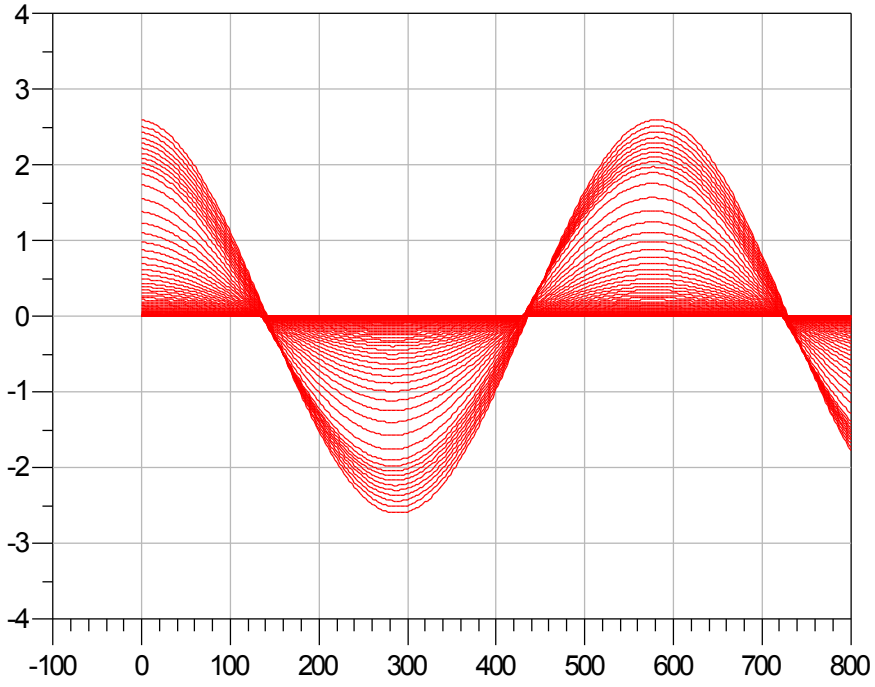

Figure 3.1.7: ADS Agilent LO waveforms

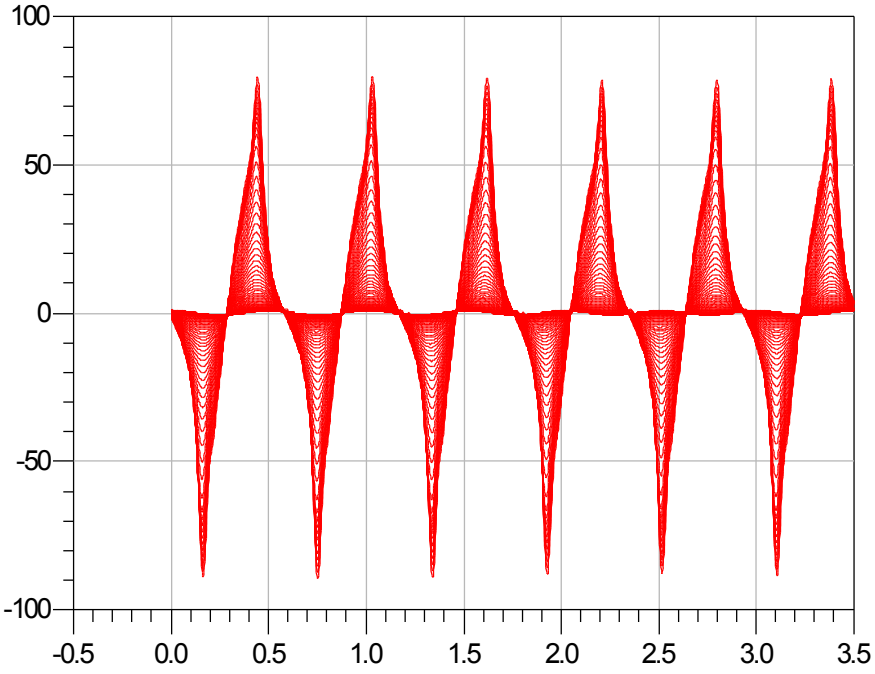

Figure 3.1.8: ADS Agilent RF Waveforms

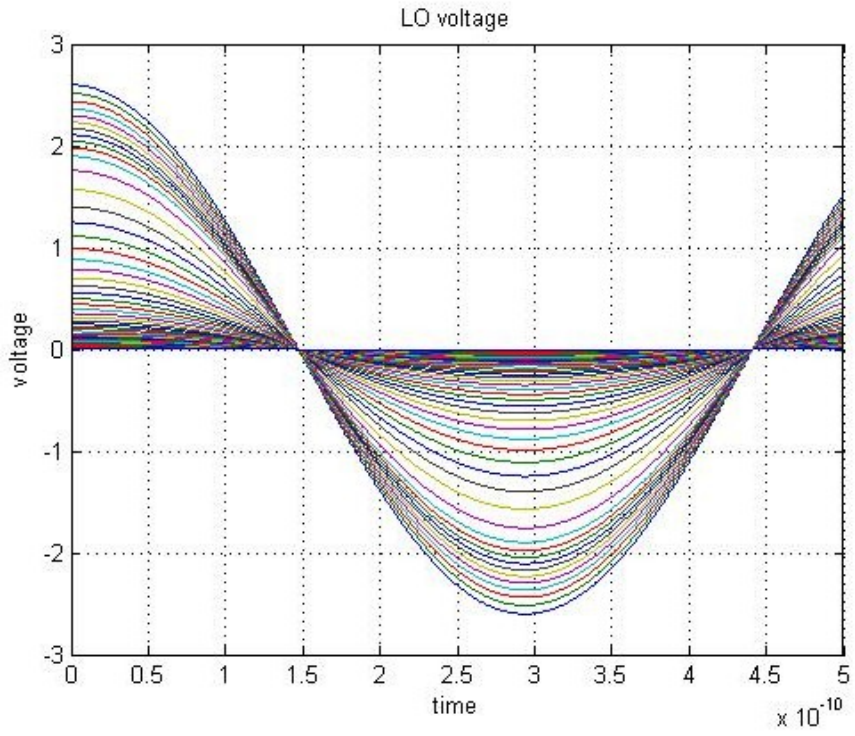

Figure 3.1.9: MATLAB LO Waveforms

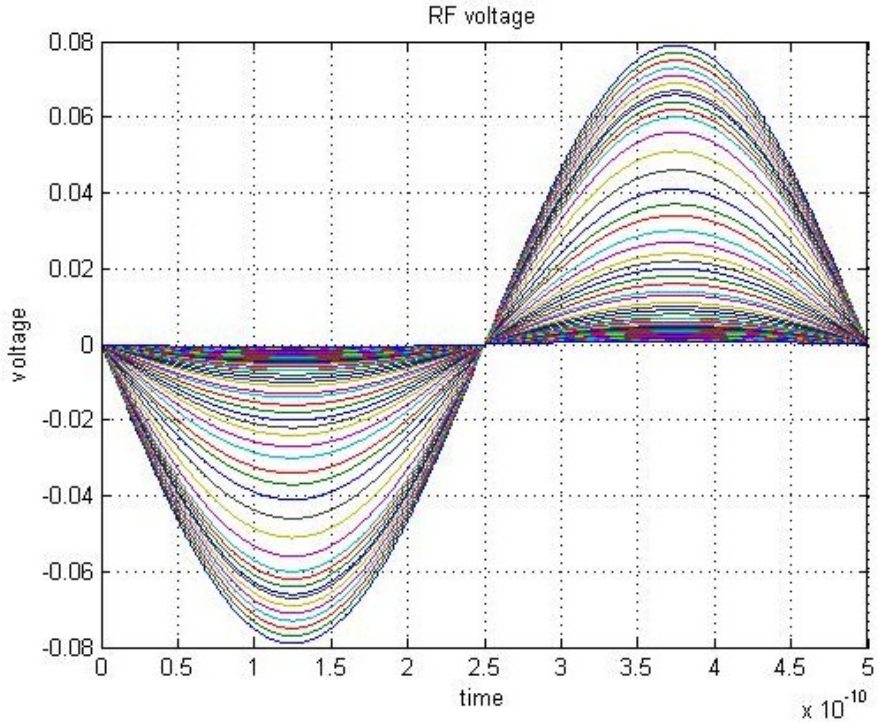

Figure 3.1.10: MATLAB RF Waveforms

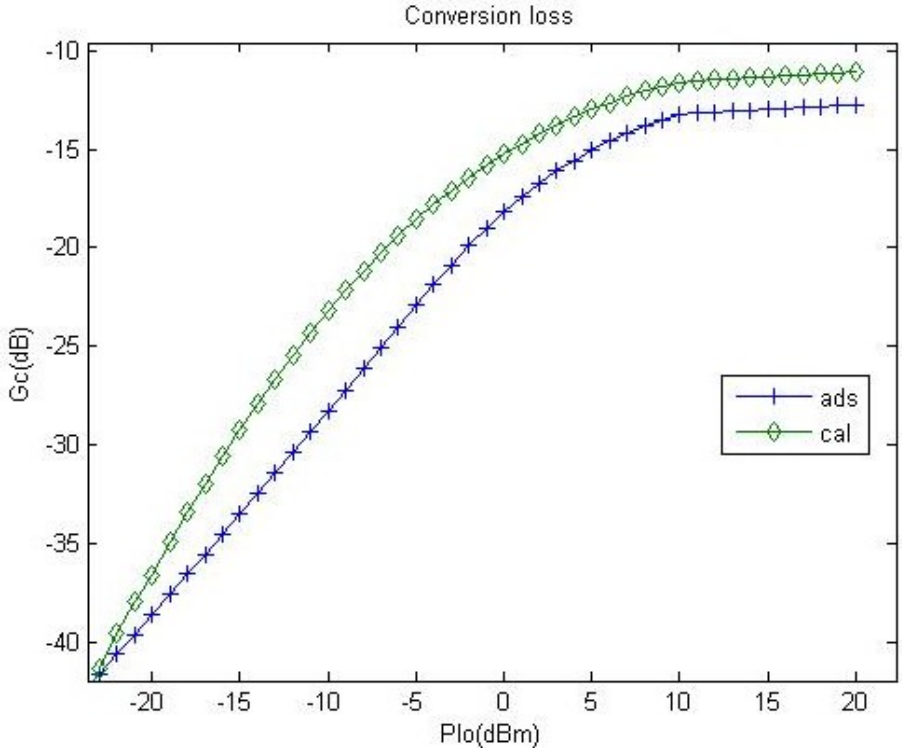

Figure 3.1.11: Conversion Loss of Derivation vs. ADS Single Device using 2 pins

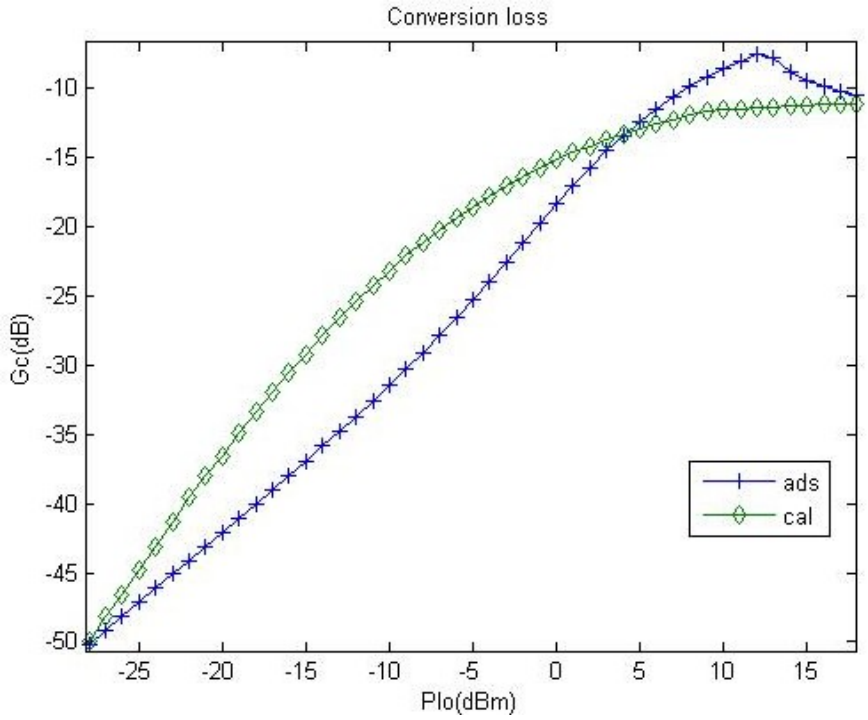

Figure 3.1.12: Conversion Loss of Derivation vs. ADS Single Device using 3 pins

3.2 Singly Balanced

For the singly balanced, shown in Figure 3.2.1, the LO is applied to two different MESFETs in a balun with 180 degree phase shift. In any given time one of the FETs will be an open switched while the other will be closed, thus a similar approach can be taken as before.

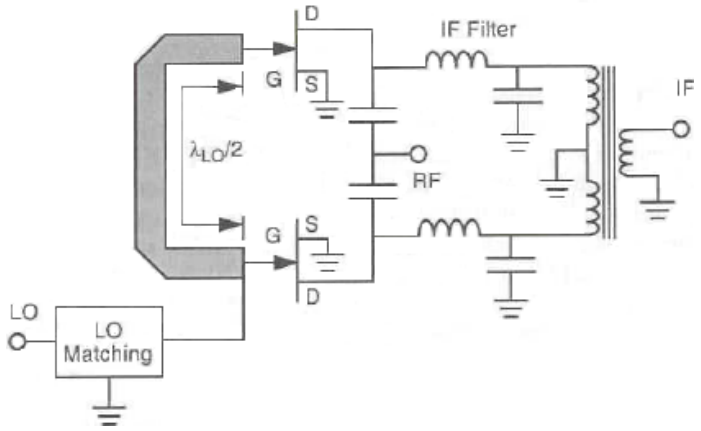

Figure 3.2.1: Singly Balanced

3.3 Doubly Balanced

The Doubly Balanced Mixer, shown in Figure 3.3.1, is very similar to the other two. At one cycle two transistors will be open which is demonstrated in Figure 3.3.2.

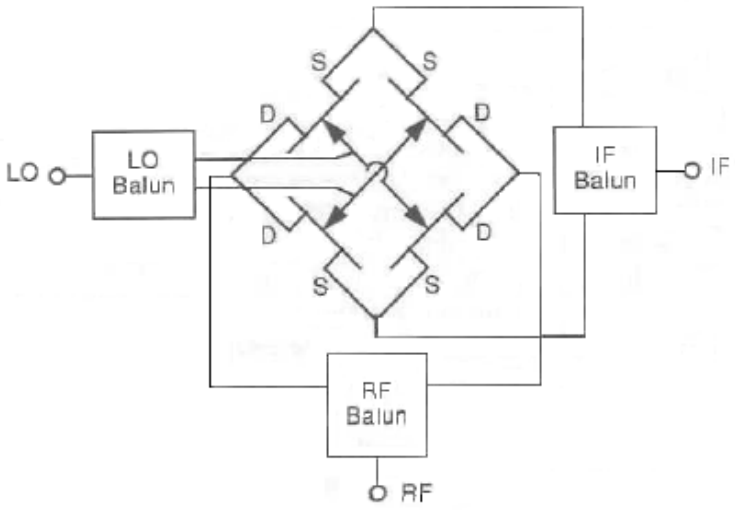

Figure 3.3.1: Doubly Balanced

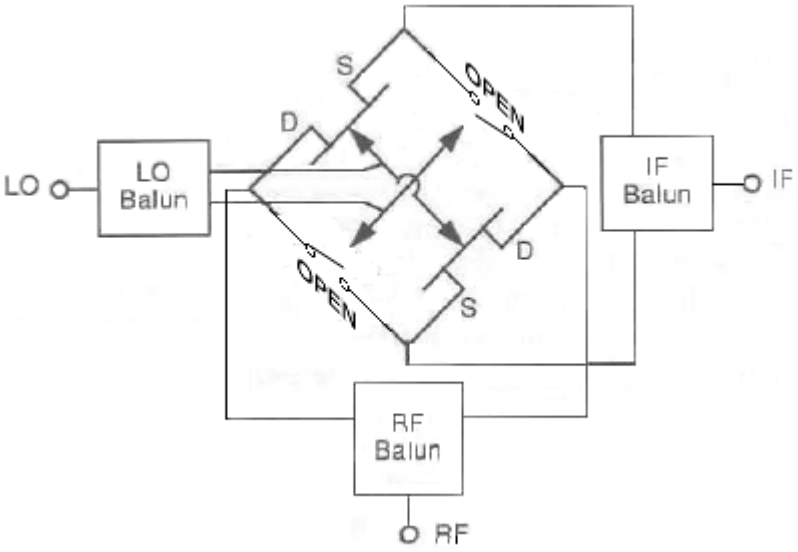

Figure 3.3.2: One Cycle of Doubly Balanced

A different case for a singly balanced mixer is shown in Figure 3.3.3. The low pass filters in the source are there to ground the FET's sources at the LO Frequency. Thus Figure 3.3.4 is shown as a simplified balanced mixer for one cycle.

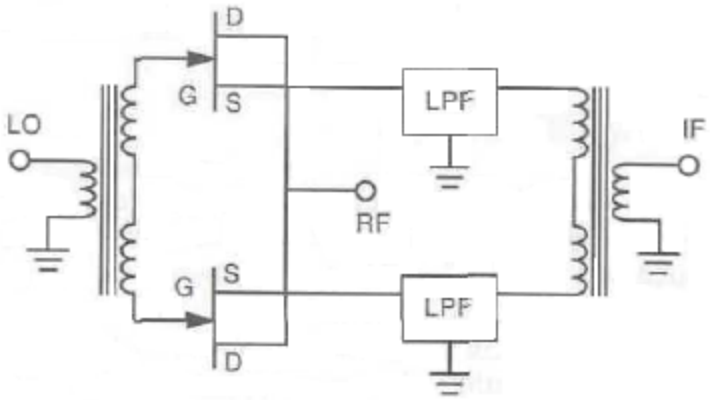

Figure 3.3.3: Alternate Singly Balanced

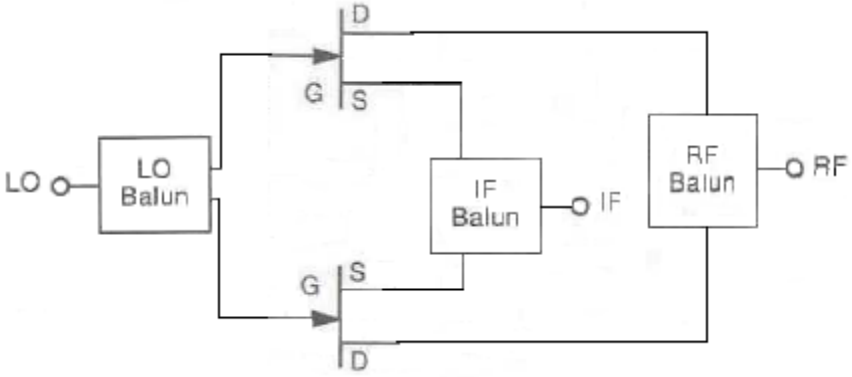

Figure 3.3.4: One Cycle Doubly Balanced Simplified Circuit

Simulation results for a ring mixer are then compared to a single FET device and the derivations that were done before, shown in Figure 3.3.5. The ring mixer takes more LO power than the single FET mixer and the conversion loss is not improved by a big factor.

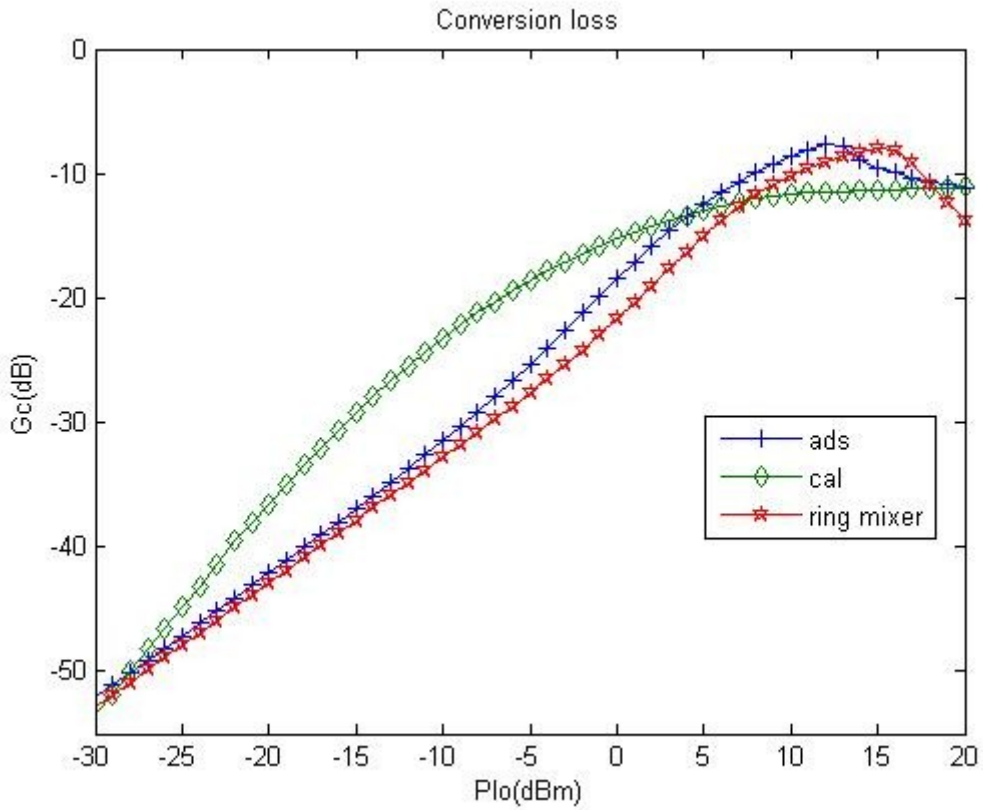

Figure 3.3.5: Conversion Loss of Single Device (3 pins) vs. Ring Mixer

CHAPTER IV

3 PHASE MIXER

4.1 Theory of 3 Phase Mixer

The 3 phase FET mixer was created to improve the conversion loss and it is shown in theory that it has a better conversion loss than the previous mixers. If the FETs are treated as ideal switches and the RF signal is split into three signals such as:

$$V_1 = \frac{V_0}{2}\left(e^{j(\omega_1 t+0)} + e^{-j(w_1 t+0)}\right),$$

$$V_2 = \frac{V_0}{2}\left(e^{j\left(\omega_1 t+\frac{2\pi}{3}\right)} + e^{-j\left(w_1 t+\frac{2\pi}{3}\right)}\right),$$

$$V_3 = \frac{V_0}{2}\left(e^{j\left(\omega_1 t-\frac{2\pi}{3}\right)} + e^{-j\left(w_1 t-\frac{2\pi}{3}\right)}\right).$$

Then the Fourier transform coefficient is found as:

$$C_n = \frac{1}{T}\int_0^{T/6} e^{-jm\omega_2 t}dt + \int_{5T/6}^{T} e^{-jm\omega_2 t}dt$$

$$C_n = \frac{j}{2\pi m}(e^{\frac{-j\pi m}{3}} - e^{\frac{-j5\pi m}{3}}).$$

Thus the Fourier series of the first voltage signal V_1 is shown as:

$$f_1(t) = \sum_{m=-\infty}^{\infty} \frac{j}{2\pi m}(e^{\frac{-j\pi m}{3}} - e^{\frac{-j5\pi m}{3}})e^{jm\omega_2 t}.$$

The same procedure is taken for the other voltage signals and their Fourier series are found as:

$$f_2(t) = \sum_{m=-\infty}^{\infty} \frac{j}{2\pi m}(e^{-j\pi m} - e^{\frac{-j\pi m}{3}})e^{-jm\omega_2 t}$$

$$f_3(t) = \sum_{m=-\infty}^{\infty} \frac{j}{2\pi m}(e^{\frac{-j5\pi m}{3}} - e^{-j\pi m})e^{-jm\omega_2 t}$$

Finally the output voltage will be found as:

$$V_{01} = f_1V_1 + f_2V_2 + f_3V_3$$

and to get $\omega_1 + \omega_2$ m=1:

$$f_1V_1 = \frac{jV_0}{4\pi}[\left(e^{-\frac{j\pi}{3}} - e^{-\frac{j5\pi}{3}}\right)e^{j(\omega_2+w_1)t} - \left(e^{\frac{j\pi}{3}} - e^{\frac{j5\pi}{3}}\right)e^{-j(\omega_2+w_1)t}$$

$$f_2V_2 = \frac{jV_0}{4\pi}[\left(e^{-j\pi} - e^{-\frac{j\pi}{3}}\right)e^{j(\omega_2+w_1)t}e^{\frac{j2\pi}{3}} - \left(e^{j\pi} - e^{\frac{j\pi}{3}}\right)e^{-j(\omega_2+w_1)t}e^{\frac{-j2\pi}{3}}$$

$$f_3V_3 = \frac{jV_0}{4\pi}[\left(e^{-\frac{j5\pi}{3}} - e^{-j\pi}\right)e^{j(\omega_2+w_1)t}e^{\frac{-j2\pi}{3}} - \left(e^{\frac{-j5\pi}{3}} - e^{j\pi}\right)e^{-j(\omega_2+w_1)t}e^{\frac{j2\pi}{3}}$$

where the final solution is:

$$V_{01} = \frac{3\sqrt{3}}{2\pi}V_0\cos(\omega_1 + \omega_2)\,t$$

The conversion loss is then found as:

$$G_c = \frac{27}{4\pi^2} = -1.65dB$$

Note that the FETs were treated as ideal switches and the input voltage was a square wave signal, the conversion loss for a ring mixer is found the same way and had a conversion loss of -3.922dB. In real world applications where state of the art mixers are fabricated, the conversion loss is about 3 to 4 dB lower than the ideal case.

4.2 Mixer Setup

To produce the mixer, 9 FET devices were used to have a 3 phase input for V_{LO}, V_{RF}, and then combine the outputs. The VLO and VRF splitters are shown in Figure 4.2.1 and Figure 4.2.2. The combiner is essential the same as the VRF splitter and is shown in Figure 4.2.3. The FETs are then shown in Figure 4.2.4 with the mixer simulation setup in Figure 4.2.5.

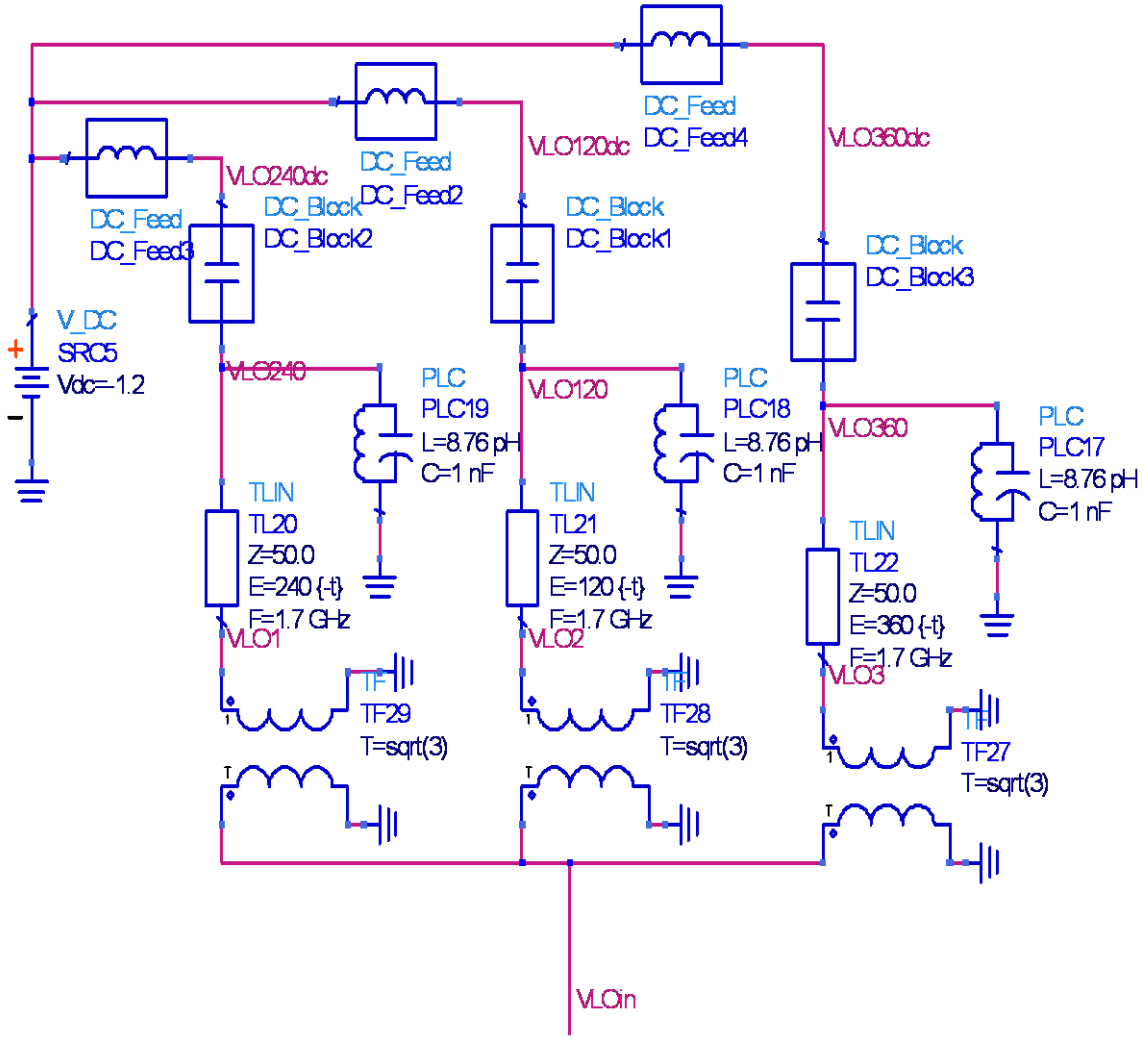

Figure 4.2.1: VLO Splitter and Voltage Bias

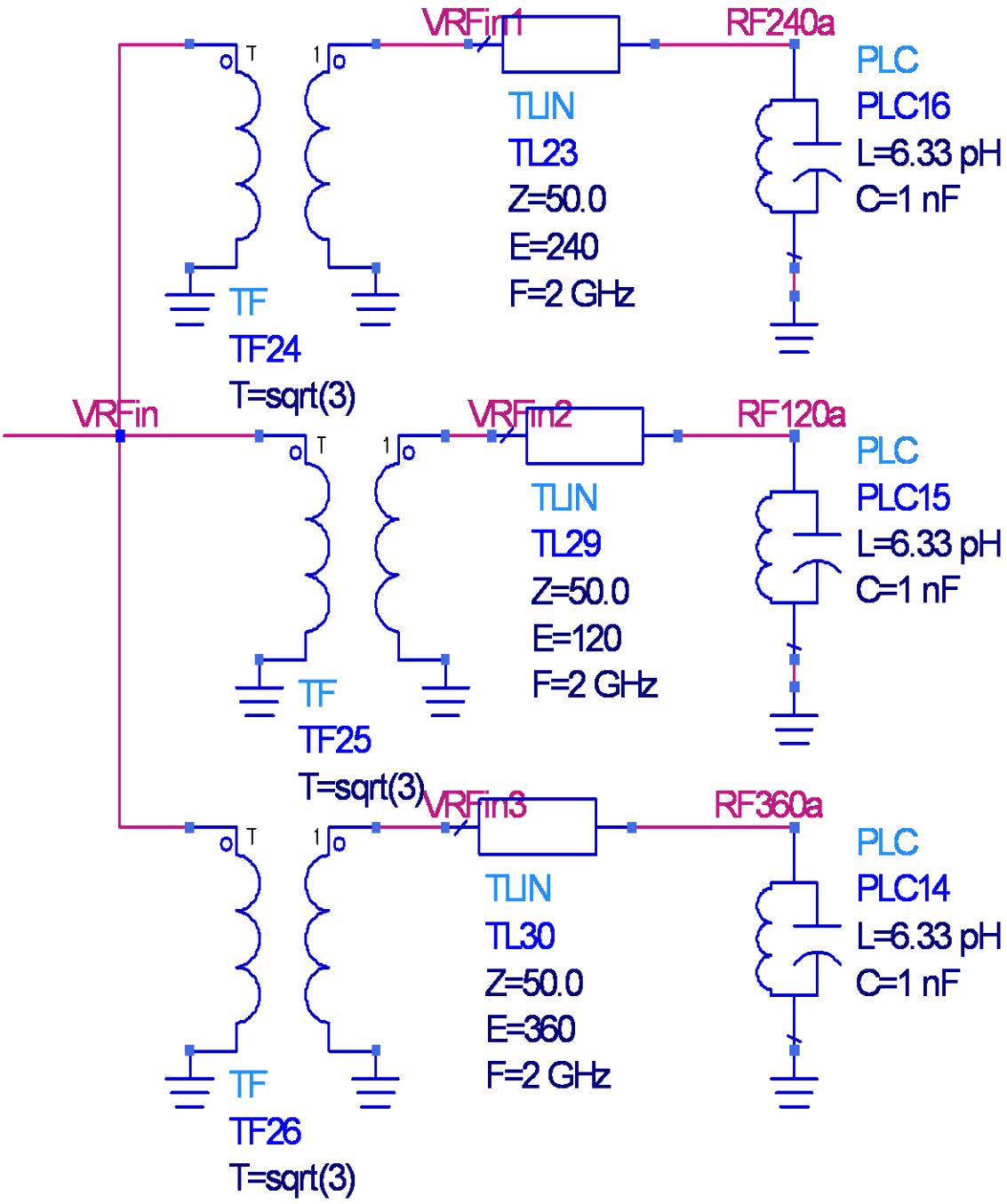

Figure 4.2.2: VRF Splitter and Transmission Line Phase Shift

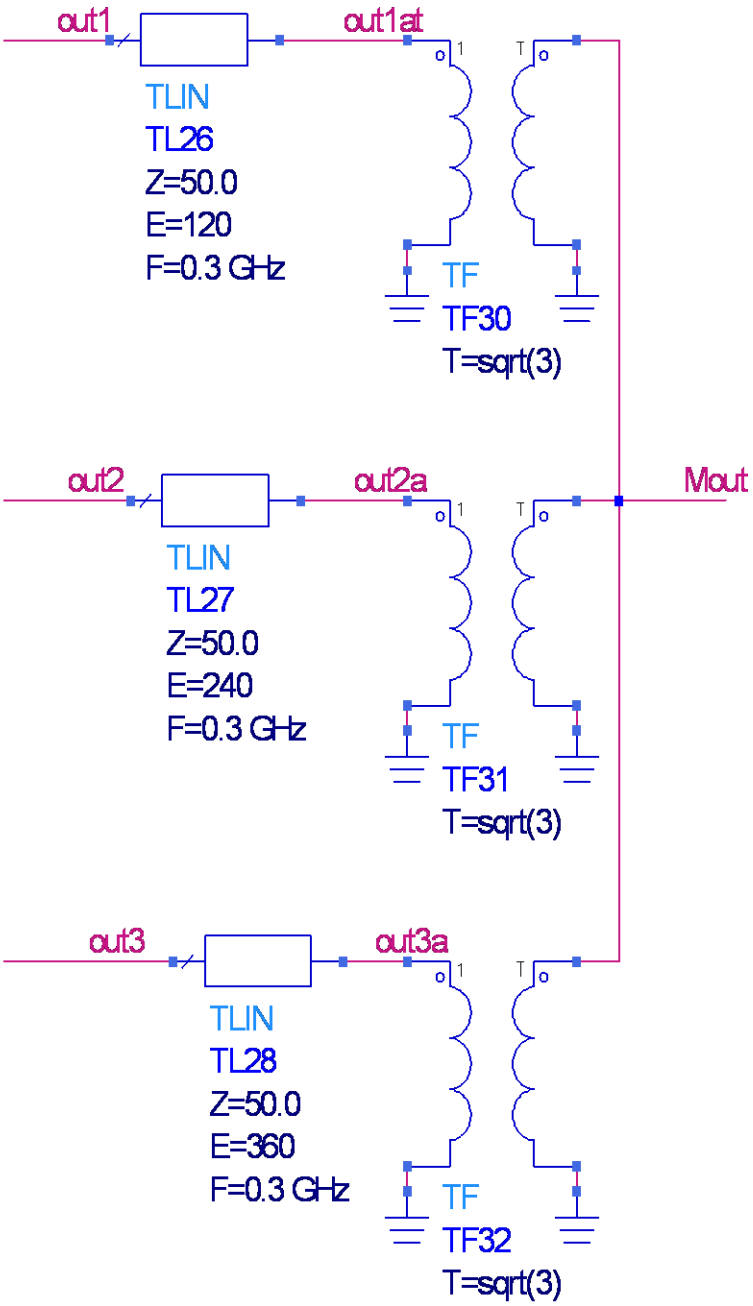

Figure 4.2.3: Output Combiner

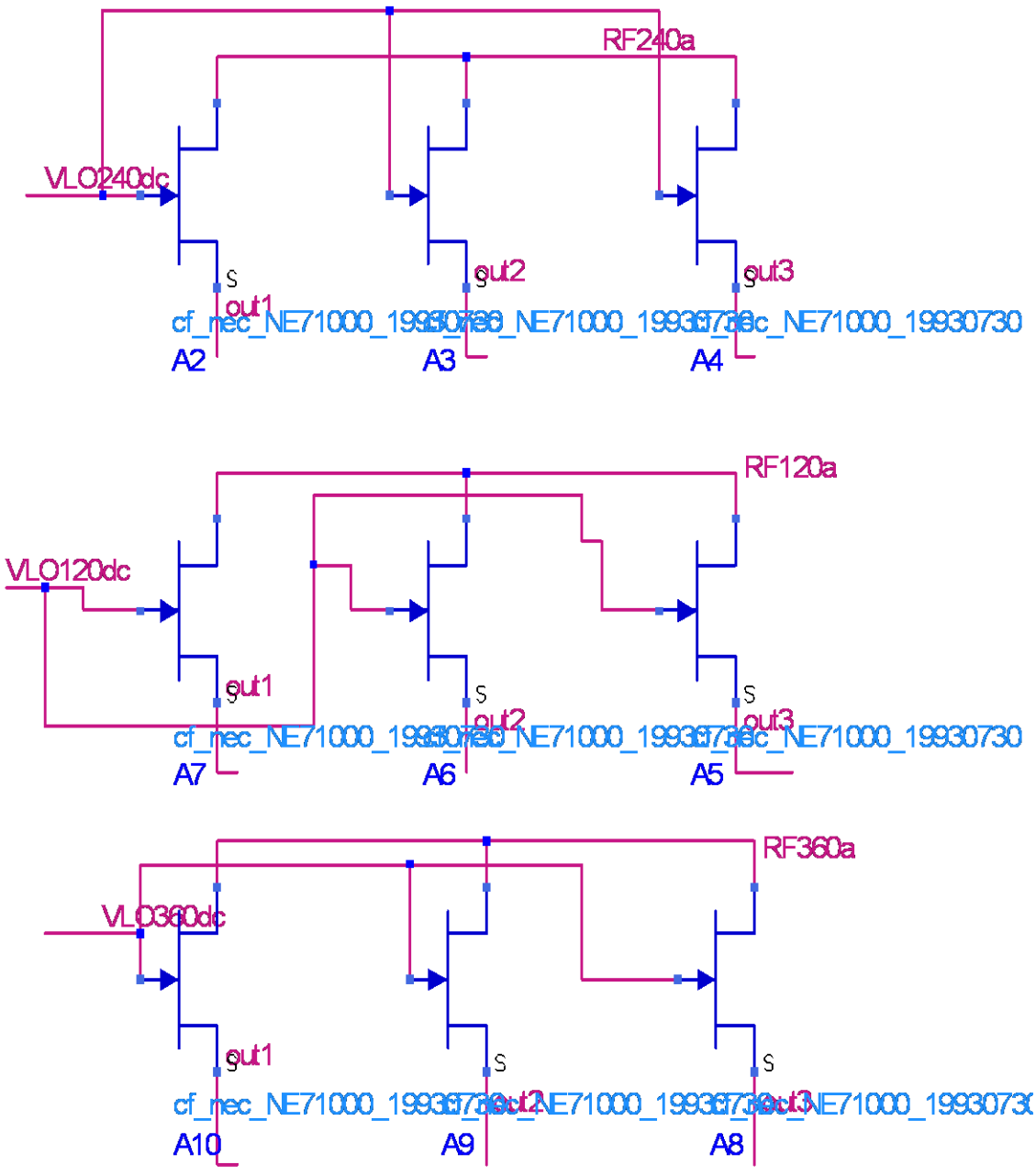

Figure 4.2.4: FET Setup for 3 Phase Mixer

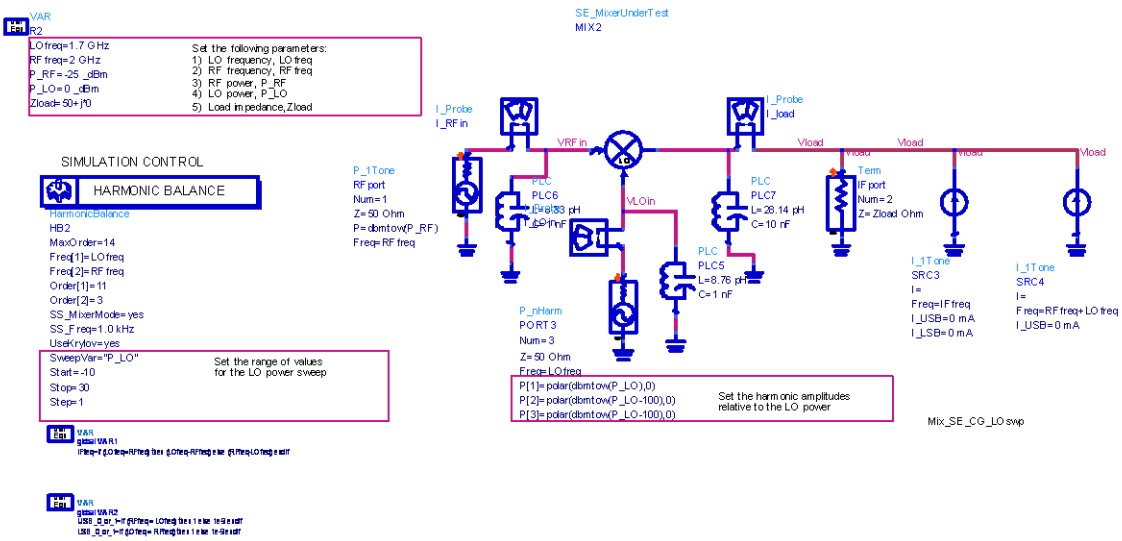

Figure 4.2.5: Mixer Setup

4.3 Impedance Matching

The impedance and the voltage standing wave ratio, VSWR, for the RF and LO ports can be seen in Table 4.3.1 and Table 4.3.2. A VSWR value of 1 would indicate a perfect match; and as seen in the tables, the impedance of the ports are very close to it. By improving the impedance in the IF port the conversion loss is -10.42 dB.

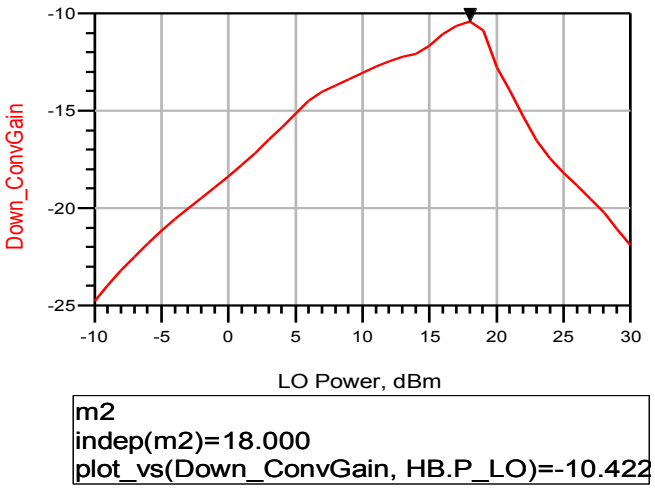

Figure 4.3.1: Conversion Loss

LO Power	Impedance	Reflection Coefficient	VSWR
-10.00	55.03 + j6.49	0.08 / 48.67	1.17
-9.00	56.60 + j6.53	0.09 / 41.19	1.19
-8.00	58.40 + j6.50	0.10 / 34.30	1.22
-7.00	60.45 + j6.36	0.11 / 28.04	1.25
-6.00	62.75 + j6.07	0.13 / 22.38	1.29
-5.00	65.31 + j5.58	0.14 / 17.25	1.33
-4.00	68.10 + j4.82	0.16 / 12.57	1.38
-3.00	71.10 + j3.74	0.18 / 8.28	1.43
-2.00	74.27 + j2.28	0.20 / 4.32	1.49
-1.00	77.56 + j0.41	0.22 / 0.66	1.55
0.00	80.87 - j1.90	0.24 / -2.69	1.62
1.00	84.09 - j4.62	0.26 / -5.74	1.69
2.00	87.09 - j7.68	0.28 / -8.49	1.76
3.00	89.72 - j10.97	0.29 / -10.95	1.83
4.00	91.85 - j14.35	0.31 / -13.15	1.90
5.00	93.44 - j17.70	0.32 / -15.14	1.96
6.00	94.35 - j20.81	0.34 / -16.93	2.01
7.00	91.91 - j21.22	0.33 / -18.35	1.97
8.00	88.20 - j20.08	0.31 / -19.46	1.89
9.00	85.71 - j19.45	0.30 / -20.42	1.84
10.00	83.49 - j18.87	0.29 / -21.36	1.80
11.00	81.05 - j18.13	0.27 / -22.40	1.75
12.00	78.28 - j17.10	0.26 / -23.57	1.69
13.00	75.17 - j15.78	0.24 / -24.90	1.62
14.00	71.79 - j14.17	0.21 / -26.41	1.54
15.00	67.87 - j11.39	0.18 / -27.00	1.44
16.00	64.52 - j9.60	0.15 / -28.68	1.36
17.00	61.01 - j8.50	0.12 / -33.28	1.29
18.00	57.06 - j7.60	0.10 / -43.03	1.21
19.00	48.07 - j5.19	0.06 / -107.33	1.12
20.00	32.71 - j2.20	0.21 / -171.22	1.53
21.00	26.92 - j1.64	0.30 / -174.72	1.86
22.00	22.92 - j1.39	0.37 / -175.98	2.18
23.00	20.49 - j1.25	0.42 / -176.56	2.44
24.00	19.28 - j1.14	0.44 / -176.94	2.60
25.00	18.76 - j1.02	0.45 / -177.29	2.67
26.00	18.67 - j0.88	0.46 / -177.65	2.68
27.00	18.87 - j0.74	0.45 / -178.02	2.65
28.00	19.15 - j0.60	0.45 / -178.40	2.61
29.00	19.38 - j0.46	0.44 / -178.77	2.58
30.00	19.54 - j0.33	0.44 / -179.12	2.56

Table 4.3.1: Impedance and VSWR Table Looking into the RF ports

LO Power	Impedance	Reflection Coefficient	VSWR
-10.00	6.13 - j71.89	0.92 / -69.37	25.09
-9.00	6.11 - j72.09	0.92 / -69.23	25.28
-8.00	6.08 - j72.32	0.92 / -69.06	25.51
-7.00	6.05 - j72.60	0.93 / -68.86	25.78
-6.00	6.01 - j72.92	0.93 / -68.63	26.09
-5.00	5.97 - j73.30	0.93 / -68.36	26.45
-4.00	5.93 - j73.74	0.93 / -68.04	26.87
-3.00	5.88 - j74.26	0.93 / -67.68	27.36
-2.00	5.82 - j74.84	0.93 / -67.27	27.91
-1.00	5.77 - j75.51	0.93 / -66.81	28.53
0.00	5.71 - j76.26	0.93 / -66.29	29.22
1.00	5.65 - j77.09	0.94 / -65.74	29.98
2.00	5.58 - j77.98	0.94 / -65.14	30.81
3.00	5.52 - j78.94	0.94 / -64.52	31.70
4.00	5.46 - j79.94	0.94 / -63.88	32.63
5.00	5.40 - j80.98	0.94 / -63.22	33.60
6.00	5.54 - j82.02	0.94 / -62.56	33.40
7.00	12.07 - j82.25	0.88 / -61.80	15.53
8.00	27.99 - j79.17	0.74 / -60.11	6.68
9.00	45.89 - j71.53	0.60 / -56.57	3.99
10.00	62.57 - j59.19	0.48 / -50.28	2.82
11.00	75.95 - j43.01	0.38 / -40.04	2.21
12.00	84.83 - j24.60	0.31 / -24.89	1.90
13.00	88.98 - j5.82	0.28 / -6.10	1.79
14.00	88.86 + j11.63	0.29 / 11.87	1.82
15.00	80.56 + j19.24	0.27 / 23.81	1.75
16.00	71.36 + j16.93	0.22 / 30.45	1.57
17.00	67.41 + j14.02	0.19 / 32.04	1.47
18.00	66.87 + j11.40	0.17 / 28.46	1.42
19.00	67.78 + j9.08	0.17 / 22.65	1.41
20.00	64.12 + j6.77	0.14 / 22.24	1.32
21.00	58.07 + j4.78	0.09 / 28.11	1.19
22.00	52.01 + j3.22	0.04 / 56.21	1.08
23.00	46.45 + j2.06	0.04 / 148.72	1.09
24.00	41.65 + j1.22	0.09 / 170.91	1.20
25.00	37.67 + j0.64	0.14 / 176.64	1.33
26.00	34.41 + j0.23	0.18 / 178.98	1.45
27.00	31.78 - j0.03	0.22 / -179.89	1.57
28.00	29.69 - j0.19	0.25 / -179.34	1.68
29.00	28.03 - j0.26	0.28 / -179.12	1.78
30.00	26.69 - j0.27	0.30 / -179.13	1.87

Table 4.3.2: Impedance and VSWR Looking into the LO Port

LO Power	Impedance	Reflection Coefficient	VSWR
-10.00	50.42 + j0.21	0.00 / 25.66	1.01
-9.00	50.48 + j0.26	0.01 / 28.14	1.01
-8.00	50.53 + j0.31	0.01 / 30.51	1.01
-7.00	50.56 + j0.37	0.01 / 33.07	1.01
-6.00	50.57 + j0.42	0.01 / 36.30	1.01
-5.00	50.53 + j0.47	0.01 / 41.15	1.01
-4.00	50.43 + j0.50	0.01 / 49.16	1.01
-3.00	50.24 + j0.52	0.01 / 65.18	1.01
-2.00	49.91 + j0.50	0.01 / 100.19	1.01
-1.00	49.44 + j0.44	0.01 / 141.39	1.01
0.00	48.78 + j0.37	0.01 / 162.82	1.03
1.00	47.92 + j0.28	0.02 / 172.08	1.04
2.00	46.82 + j0.19	0.03 / 176.52	1.07
3.00	45.51 + j0.10	0.05 / 178.62	1.10
4.00	43.98 + j0.04	0.06 / 179.63	1.14
5.00	42.29 - j0.02	0.08 / -179.85	1.18
6.00	40.48 - j0.04	0.11 / -179.75	1.24
7.00	38.72 - j0.02	0.13 / -179.90	1.29
8.00	37.46 - j0.04	0.14 / -179.81	1.33
9.00	36.35 - j0.04	0.16 / -179.82	1.38
10.00	35.06 - j0.02	0.18 / -179.91	1.43
11.00	33.43 - j0.01	0.20 / -179.95	1.50
12.00	31.48 - j0.03	0.23 / -179.90	1.59
13.00	29.25 - j0.05	0.26 / -179.84	1.71
14.00	26.87 - j0.06	0.30 / -179.81	1.86
15.00	23.76 - j0.03	0.36 / -179.91	2.10
16.00	20.57 - j0.03	0.42 / -179.90	2.43
17.00	17.83 - j0.07	0.47 / -179.82	2.80
18.00	15.53 - j0.11	0.53 / -179.71	3.22
19.00	13.27 - j0.13	0.58 / -179.67	3.77
20.00	11.15 - j0.10	0.64 / -179.76	4.48
21.00	10.04 - j0.10	0.67 / -179.76	4.98
22.00	9.22 - j0.13	0.69 / -179.69	5.42
23.00	8.64 - j0.16	0.71 / -179.63	5.79
24.00	8.25 - j0.17	0.72 / -179.59	6.06
25.00	7.97 - j0.18	0.72 / -179.57	6.27
26.00	7.77 - j0.18	0.73 / -179.57	6.44
27.00	7.62 - j0.18	0.74 / -179.57	6.56
28.00	7.52 - j0.19	0.74 / -179.56	6.65
29.00	7.46 - j0.19	0.74 / -179.56	6.70
30.00	7.45 - j0.19	0.74 / -179.55	6.71

Table 4.3.3: Impedance and VSWR Looking into the IF Port

CHAPTER V

CONCLUSION

The thesis has shown good understanding of the mixers discussed in Chapter III along with a development of a new idea shown in Chapter IV. The simulations in Chapter III for the derivations versus ADS harmonic balance were in fairly reasonable agreement with each other. During the course of the thesis research no papers about a subthreshold 3 phase mixers were discovered. There is an active mixer with RF signals at 0°, 45°, and 90° shown in [23] however this thesis topic did not go into the discussion of active type mixers or harmonic rejection.

Future work of the 3 phase mixer could involve proper impedance matching done at each port. The results were fairly reasonable since there should be some loss due to impedance mismatch. Another thing is that none of the mixers can achieve the ideal theoretical conversion loss because the FETs were treated as simple switches so there should also be a +/- 3dB loss to account for.

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APPENDIX A

APPENDIX A

MAIN MATLAB CODE

```
clear;clc;close all;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Author: Jesus Angel Torres
% Description: This is the main code to compute the conversion loss of the
% FET Mixers for a single device. The code can be modified to a mixer of
% common source configuration or for 3 pin configuration by adding an
% impedance to the source.
% Last Modified: Friday November 11, 2011
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%% Parameters from NE71000 MESFET %%%%%%%%%%%%%%%%%%%%%%%%
K=0.102;  % Slope of the channel conductance in the on-state

Rg = 2.5; %de-embed
Rs = 2.4; %de-embed
Rd = 0.2; %de-embed

Cgs = 0.145e-12; %from paper
Cgd = 0.106e-12; % from paper


%%%%%%%%%%%%%%%%%%%% Mixer Impedance %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
ZG = 50;          % External Gate Impedance (50 ohms unmatched)
ZD = 50;          % External Drain Impedance (50 ohms unmatched)
ZS = 50;          % External Source Impedance (50 ohms unmatched)
RL = 50;          % Load Resistance
%%%%%%%%%%%%%%%%%%%%%%%% Frequencies used are: %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Lo_f = 1.7*10^9;   % LO frequency
Rf_f = 2*10^9;     % RF frequency
wLO = Lo_f * 2*pi; % LO frequency in radians
wRF = Rf_f*2*pi;   % RF frequency in radians
%%%%%%%%%%%%%%%%%%%%%%%% The voltages are: %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
n = 1024;                   % Sampling
t = linspace(0,1/Rf_f,n);   % time
% VLO amplitudes for waveforms
Vlo = [2.6 2.516 2.438 2.365 2.296 2.231 2.168 2.107 2.045 1.978 1.897...
    1.757 1.569 1.398 1.246 1.111 0.990 0.882 0.787 0.701 0.625 0.557...
    0.496 0.442 0.394 0.351 0.313 0.279 0.249 0.222 0.198 0.176 0.157...
    0.140 0.125 0.111 0.099 0.088 0.079 0.070 0.062 0.056 0.050 0.044...
```

```
    0.039 0.035 0.031 0.028 0.025 0.022 0.020 0.018 0.016 0.014 0.012...
    0.011 0.010 0.009 0.008 0.007 0.006 0.00557 0.00496 0.00442 0.00394...
    0.00351 0.00313 0.00279 0.00249 0.00222 0.00198];

% VRF amplitudes for waveforms
Vrf = [0.079 0.077 0.075 0.073 0.071 0.069 0.067 0.066 0.064 0.062 0.060...
    0.056 0.051 0.046 0.041 0.037 0.034 0.030 0.027 0.024 0.022 0.020...
    0.018 0.016 0.014 0.013 0.011 0.010 0.009 0.008 0.007 0.00669...
    0.00603 0.00544 0.00492 0.00445 0.00404 0.00367 0.00334 0.00305...
    0.00279 0.00256 0.00236 0.00218 0.00202 0.00187 0.00175 0.00164...
    0.00154 0.00146 0.00138 0.00131 0.00126 0.00120 0.00116 0.00112...
    0.00108 0.00105 0.00102 0.00100 0.00098 0.00096 0.00094 0.00093...
    0.00091 0.00090 0.00089 0.00088 0.000875 0.000868 0.000862];

%% Generating waveforms
% waveforms for Vlo and Vrf
[V_lo,V_rf,V_losin] = V_lo_rf_waves2(Vlo,Vrf,wLO,wRF,t);

[VGS] = creates_VGS(V_lo,wLO,Cgs,Cgd,Rs,Rd,Rg,ZS); % Creates internal Vgs
plots_results(t,V_lo,V_rf,VGS); %plots figures

%% Finding conductance
[g1] = num_g1(Vlo,wLO,Cgs,Cgd,Rd,Rs,Rg,K,ZS);
%% Solve for gain

Gc = g1.^2 * real(ZD)*real(ZS);
Gc = abs(Gc);
Gc = mag2db(Gc);
Gc = fliplr(Gc);

% Conversion loss values from ADS Agilent
Gc_ads = [-95.145,-94.148,-93.15,-92.152,-91.154,-90.155,-89.156...
    ,-88.156,-87.157,-86.157,-85.157,-84.157,-83.157,-82.156,-81.156...
    ,-80.155,-79.154,-78.152,-77.15,-76.147,-75.143,-74.138,-73.131...
    ,-72.122,-71.109,-70.091,-69.065,-68.028,-66.974,-65.896,-64.781...
    ,-63.613,-62.369,-61.019,-59.531,-57.869,-56.009,-53.942,-51.682...
    ,-49.258,-46.711,-44.083,-41.416,-38.747,-36.107,-33.530,-31.046...
    ,-28.686,-26.479,-24.450,-22.622,-21.008,-19.611,-18.424,-17.415...
    ,-16.555,-15.819,-15.186,-14.639,-14.165,-13.755,-13.460,-13.338...
    ,-13.262,-13.201,-13.148,-13.100,-13.055,-13.012,-12.972,-12.934];

% depending on how many points were choosen
n = length(Gc_ads);
Plo_ads = linspace(-50,20,n); %dbm

figure
plot(Plo_ads,Gc_ads,'-+',Plo_ads,Gc,'-d')
legend('ads','cal',0)
xlabel('Plo(dBm)')
ylabel('Gc(dB)')
title('Conversion loss')
```

APPENDIX B

APPENDIX B

VLO AND VRF CODE

```
function [V_lo,V_rf,V_losin] = V_lo_rf_waves2(Vlo,Vrf,wlo,wrf,t)
% Author: Jesus Angel Torres
% Last modified: November 11, 2011
% This function will define the VLO and VRF waveforms

[r,c]=size(Vlo);      % getting size of Vlo
xy = length(t);       % length of time

V_lo=zeros(c,r);      % allocating memory
V_rf=zeros(c,r);      % allocating memory
V_losin=zeros(c,r);   % allocating memory

for xx=1:c
    for xy2=1:xy
        V_lo(xx,xy2) = Vlo(xx)*cos(wlo*t(xy2));     % creates Vlo waveform
        V_rf(xx,xy2) = Vrf(xx)*-sin(wrf*t(xy2));    % creates Vrf waveform
        V_losin(xx,xy2) = Vlo(xx)*sin(wlo*t(xy2)); %creates Vlo+90 waveform
    end
end
```

APPENDIX C

APPENDIX C

INTERNAL VGS CODE

```
function [VGS] = creates_VGS(V_lo,wlo,Cgs,Cgd,Rs,Rd,Rg,Zs)
% Author: Jesus Angel Torres
% Description: creates VGS VGS uses V_losin since from derivation the
% imaginary component will give it a shift. Change between unmachted and
% matched as required.

% VGS = V_losin / (2*wlo*(Cgs + Cgd)*(Rd + Rs*Rd/(Rs+Rd))); %when matched
VGS = V_lo / (1i*wlo*(Cgs+Cgd)*(Zs+Rg+Rs*(Rd+50)/(Rs+(Rd+50)))+1);
%unmatched
```

APPENDIX D

APPENDIX D

CODE FOR FIGURES

```
function plots_results(t,V_lo,V_rf,VGS)
% Author: Jesus Angel Torres
% Last Modified: November 11, 2011
% Description: This function simply plots the data

%% plots Vlo and Vrf
figure
plot(t,V_lo)
xlabel('time')
ylabel('voltage')
title('LO voltage')
grid on

figure
plot(t,V_rf)
xlabel('time')
ylabel('voltage')
title('RF voltage')
grid on

%% Plots Vgs
figure
plot(t,VGS)
title('Internal gate-source voltage')
xlabel('time')
ylabel('VGS')
grid on
```

APPENDIX E

APPENDIX E

CODE FOR NUMERICAL CALCULATION OF CONDUCTANCE

```
function [g1] = num_g1(Vlo,wLO,Cgs,Cgd,Rd,Rs,Rg,K,Zd)
% Author: Jesus Angel Torres
% Last Modified: November 11, 2011
% Description: This function will solve for the conductance using numerical
% methods.
n = 1024; %number of steps

x = linspace(-pi/2,pi/2,n);
m = length(Vlo);
for x2=1:m
    for y=1:n
 Vg_lo(x2,y)=Vlo(x2).*cos(x(y))/(1i*wLO*(Cgs+Cgd)*(Zd+Rg+Rs*Rd/(Rs+Rd))+1);
    end
end
g = K*Vg_lo;
for r_v1 = 1:m
    for x_x=1:n
        denum(r_v1,x_x) = (g(r_v1,x_x)*(Rs+Rd)+1);
            f_wlo(r_v1,x_x) = g(r_v1,x_x)./(g(r_v1,x_x)*(Rs+Rd+Zd)+1);
    end
end

for x2=1:m
    for y=1:n
        f_wlo2(x2,y) = f_wlo(x2,y)*cos(x(y));
    end
end

figure
plot(x,f_wlo2)
title('fwlo')

[r,c]=size(Vlo);
for n2 = 1:c
g1(n2) = 1/pi*trapz(x,f_wlo2(n2,:));
end
g1 = abs(g1);
figure
g22= fliplr(g1);
plot(g22)
title('conductance')
```

BIOGRAPHICAL SKETCH

Jesus Angel Torres was born in December 16, 1983 in Pasadena, Texas. He received two Bachelor of Science degrees in Electrical Engineering and Mathematics from the University of Texas Pan American (UTPA) in 2007. In spring of 2011 he graduated with a Master of Science in Electrical Engineering, where he was involved in classes dealing with digital integrated circuit design, semiconductive devices, electromagnetic theory and applications, and radio communication circuits. During his masters he became a member of the Golden Key International Honour Society.

He has served as a teaching assistant for the Mechanical Engineering department where he taught MATLAB to undergraduate students at UTPA. He also served as a research assistant for the Electrical Engineering department at UTPA. Research has been a huge factor in his educational studies and has jumped onto several topics throughout his graduate studies. Topics in research have been in creating a computer data acquisition for a motor and generator system, Nano-FET technology, and GaAs/GaN devices.

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