High Gain Magnetically Coupled Single Switch Quadratic Modified SEPIC DC-DC Converter

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Abstract—This article proposes, analyzes, and tests an improved high voltage gain dc-dc converter based on a single-ended primary-inductor converter (SEPIC). The proposed magnetically coupled quadratic modified SEPIC converter (MCQ-MSC) employs a coupled transformer with an optimized design to obtain a high voltage boost factor by controlling the transformer's turn ratio along with the switching duty cycle. Thanks to the unique structure of the coupled transformer, high voltage gain is obtained at low turns ratio, which is highly desirable for high voltage applications and the compact size of the converter. In addition to the coupled transformer, a voltage-boosting module is utilized to achieve a very high output voltage for a low switching duty cycle. The proposed inverter has a single switch with a wide control range of duty cycle (0<D<1), causing low conducting losses and high efficiency. Furthermore, a clamping circuit is successfully designed to remove the leakage inductance effects of the coupled transformer on the power switch. The proposed MCQ-MSC drains a continuous current from the input dc source, which makes it a suitable choice for renewable energy sources (RES). The hardware prototype of the proposed converter is tested to verify the mathematical expressions and theoretical results.

Index Terms— Magnetically coupled inductors, SEPIC converter, single-switch topology, voltage-boosting module.

I. INTRODUCTION

In recent years, the applications of renewable energy sources (RES) and energy storage systems (ESS) have sparked a heated debate among the diverse industrial sections. However, the main impediment of RES and ESS is their bounded voltage range with intermittent characteristics. Considering the crucial role of DC-DC converters in providing the required voltage for these applications, they can be exploited to convert the low and intermittent input voltage of PV sources (12-48 V) to the demanded voltage of the microgrids buses (200-800V) [1-2]. The same challenge is for electric vehicle (EV) applications [3]. On the other hand, conventional dc-dc boost converters such as ZETA, SEPIC, and CUK topologies suffer from a limited range of output voltage. To achieve an output voltage of 200-800V, converters must be controlled by a high switching duty cycle, which is practically not viable because turning on the power switches for long intervals causes operation malfunction, efficiency reduction, and high power losses. Consequently, the practical voltage boost factor in the aforementioned conventional converters is 4-5 [4].

To overcome the low voltage gain issues of the conventional converters, various techniques like switched inductors cells, switched capacitors cells, multi cells, and multi-stages have been employed [5]. For instance, in [1], a cascaded connection of the boost and buck-boost converters has been used to attain high voltage gain. A voltage multiplier cell, a boost converter in [3], and a switched capacitor in [4] have been exploited for voltage gain increment. Nonetheless, these techniques lead to high costs and volume of the converters. Various coupled inductor-based DC-DC converters have been introduced to generate a high output voltage with fewer circuit elements [6-10]. Generally, the voltage gain can be raised by increasing the transformer's turn ratio, which increases convert size and control complexity [11]. To avoid increasing the transformers' turn numbers for high voltage applications, quadratic boost, quadratic quadrupler boost, and quadratic flyback boost structures have been employed in [6-9]. Furthermore, to attain low switching loss with the zero voltage switching technique, the magnetizing inductance of the coupled transformer is used in [7].

Recently, many magnetically coupled inductor impedance source structures such as Y-source [12], Γ-source [13], and asymmetrical Γ-source [14] networks have been introduced to obtain a high voltage gain with a low switching duty ratio. Nevertheless, they suffer from the narrow duty cycle control range and huge voltage spikes on the power switches [15-16]. To limit the voltage spikes, various clamping circuits have been applied to the magnetic coupling impedance source networks [16]. However, their narrow duty ratio control range is still a significant problem. Modified semi-SEPIC converters based on coupled inductors with full duty cycle control have been proposed in [17-18] to eliminate the abovementioned drawbacks. These topologies increase the voltage gain by lowering the transformer's turn ratio. However, lowering the turn ratio must be done regularly. Otherwise, distortions in output waveforms occur, restricting the operation to low-power applications.

To overcome the drawbacks of conventional converters, a novel dual winding modified SEPIC converter is proposed in this paper [19]. This paper continues the earlier work in [20], briefly introducing a quadratic SEPIC converter. This paper presents a comprehensive presentation of the proposed converter; closed-loop control, dynamic response evaluations, parameters design, comparative analysis, power loss analysis, components load factors, and experimental results. The proposed converter integrates a coupled inductor with a voltage-boosting module to deliver a high output voltage for high-voltage applications. This paper is organized as follows;

circuit description, operating principle, and coupled transformer's leakage inductance effect are given in section II. Section III deals with voltage gain analysis, the voltage stress on the semiconductors, and the dynamic behavior of the proposed system. Section IV provides a thorough comparison of the proposed and similar conventional topologies. Design consideration of the proposed converter is given in section V. Finally, the experimental results, power loss analysis, and components load factor evaluation are presented in sections VI, VII, and VIII, respectively.

II. PROPOSED MAGNETICALLY COUPLED QUADRATIC MODIFIED SEPIC DC-DC CONVERTER (MCQ-MSC)

A. Circuits Description

Fig. 1 shows the circuit diagram of the proposed MCQ-MSC. Similar to the original SEPIC converter, the proposed MCQ-MSC contains only one power switch (S), one input inductor (L_1), one middle capacitor (C_2), one output diode (D_o), and one output capacitor (Co). The middle inductor in a conventional SEPIC topology is replaced with a coupled dual winding transformer with a turn ratio of n = N1/N2. In addition, the power switch is linked with the input source by a voltage-boosting module. The boosting module includes one inductor (L_2), one capacitor (C_1), and two diodes (D_1, D_2). One diode (D_3) and one capacitor (C_3) enhance the voltage gain further. The magnetizing inductance (L_m) is modeled on the secondary winding, and an impedance source network connects the input and output sides of the converter. The proposed topology has the following main features: 1) exploiting a single power switch; 2) low conducting losses; 3) a wide range of duty cycle control (0<D<1); 4) simple control implementation; 5) continuous input current; 6) high voltage boost ability; 7) optimized coupled transformer's turn ratio; 8) non-isolated common-ground structure; 9) eliminating voltage spikes by using the clamping circuit and 10) removing leakage inductance effects without utilizing snubber circuit.

B. Operation Principle of the Proposed MCQ-MSC

To simplify the operation principle of the proposed converter following suppositions have been conceived: the components are ideal; the capacitors' and inductors' resistance are ignored; ON resistance of the power switch, voltage drop of diodes, and parasitic capacitance are neglected.

In a switching cycle of a Continuous Current Mode (CCM), there are three operation states as follows:

1) State I - interval [t_0 - t_1]

As shown in Fig 2(a), the power switch and D2 are turned ON in state I, and D_1, D_3, and D_o are reverse biased by capacitors C_1, C_3, and C_o, respectively. Inductor L_1 is charged by the input source (V_{dc}) via the current path of V_{dc}-L_1-D_2-S-V_{dc}.
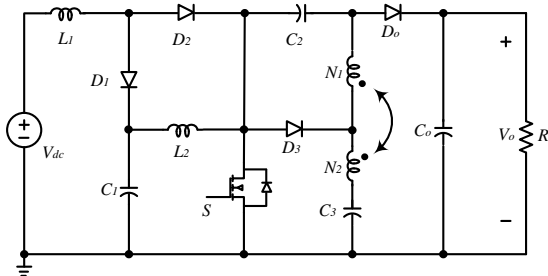

Fig. 1. Proposed magnetically coupled quadratic modified SEPIC converter

Also, the inductor L_2 is energized by capacitor C_1 with the current path of C_1-L_2-S-C_1. Windings N_1 and N_2 are charged through the current path of N_2-N_1-C_2-S-C_3-N_2. The resistive load is supplied through the output capacitor Co, which is isolated from the input source. In this interval, the current of L_1, L_M, and L_2 are rising. Fig.3 demonstrates the critical characteristic current waveforms of inductors, diodes, and the power switch.

2) State II - interval [t_1 - t_2]

Fig. 2(b) shows the operation state II when C_2 turns OFF D_2 and the power switch (S) is switched OFF. In this mode, L_1 discharged the stored energy into C_1 via the path of V_{dc}-L_1-D_1-C_1-V_{dc}. C_2 is charged with L_2 via the current path of C_1-L_2-C_2-D_o-C_o-C_1. The saved energy in the coupled inductors is discharged to the C_3 and load via the path of C_3-N_2-N_1-V_o-C_3. From t_1 to t_2, the current of L_1, L_M, and L_2 are decreased, as shown in Fig. 3.

3) State III- interval [t_2 - t_3]

For steady-state analysis, the coupled inductor is assumed ideal. Nevertheless, its leakage inductance effect is noticeable. Due to the leakage inductance effect, D_o is turned OFF before the end of the switching period while the power switch is still OFF. This mode is demonstrated as mode III in Fig. 2(c). By designing a coupled inductor with high magnetizing inductance and low leakage inductance, the effect of this state can be ignored. The parasitic capacitor in the power switch and its resonance with the leakage inductance causes voltage spikes across the power switch. During state II, when the switch is turned OFF, the power switch is clamped to $-V_{C2}+V_{Co}$, shown in Fig. 2(b). Additionally, the saved energy in leakage inductance is absorbed by C_2 and C_3, leading to the voltage spike voiding across the switch, shown in Fig. 2 (c). Hence, the snubber circuit is not needed in the proposed topology, which reduces size and cost.
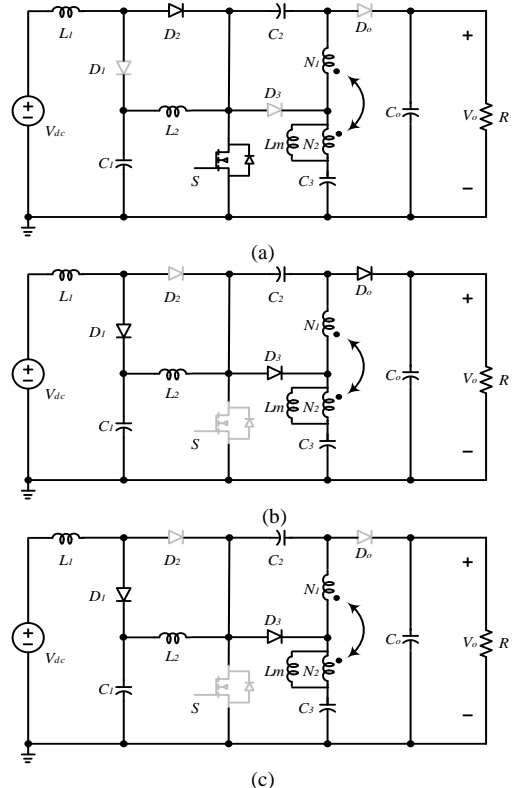

(a)

(b)

(c)

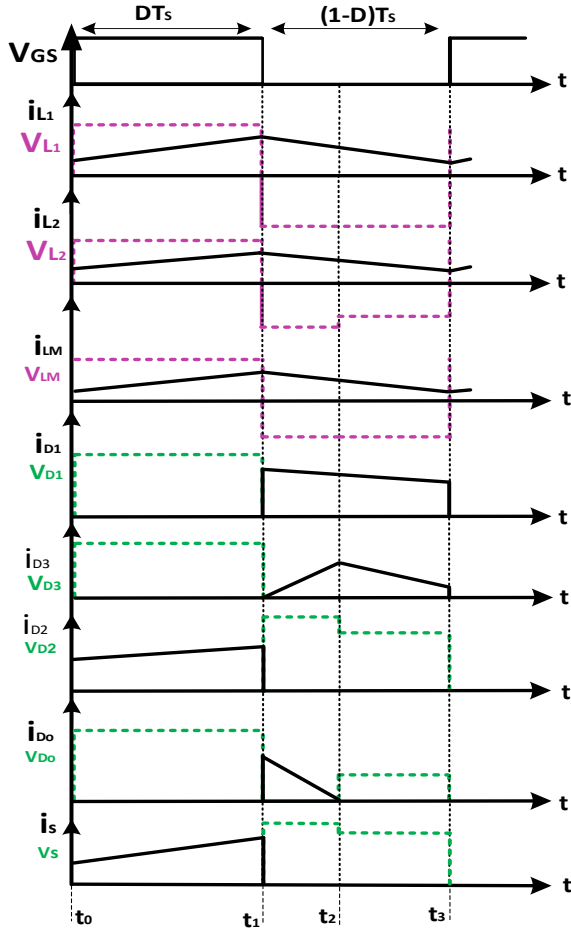Fig. 2. Equivalent circuits of the proposed MCQ-MSC. (a) State I. (b) State II. (c) State III.
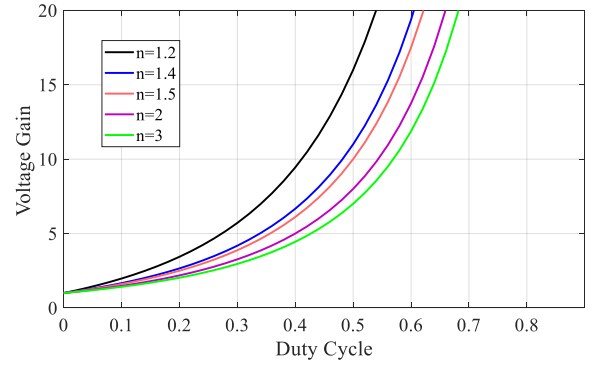
Fig. 3. Characteristic waveforms of the MCQ-MSC in CCM.

Fig. 4. Duty cycle versus voltage gain in MCQ-MSC with different *n*.

$$V_{Lm} = \frac{-V_{C2}}{n} \tag{7}$$

$$V_{L2} = \frac{V_{C2}}{n} - V_{C3} + V_{C1} \tag{8}$$

Applying the volt-second balance principle for the inductors and magnetizing L_m, (9)-(11) are achieved where T_s represents the switching period.

$$\int_0^{DT_s} V_{L1}\, dt + \int_{DT_s}^{T_s} V_{L1}\, dt = 0 \tag{9}$$

$$\int_0^{DT_s} V_{L2}\, dt + \int_{DT_s}^{T_s} V_{L2}\, dt = 0 \tag{10}$$

$$\int_0^{DT_s} V_{Lm}\, dt + \int_{DT_s}^{T_s} V_{Lm}\, dt = 0 \tag{11}$$

Also, the voltage across capacitors can be obtained as:

$$V_{C1} = \frac{1}{1-D} V_{dc} \tag{12}$$

$$V_{C2} = \frac{nD}{(1-D)^2\,(n-1)} V_{dc} \tag{13}$$

$$V_{C3} = \frac{n-1+D}{(1-D)^2\,(n-1)} V_{dc} \tag{14}$$

In addition, the output dc voltage is achieved as:

$$V_o = \frac{n-1+nD}{(1-D)^2\,(n-1)} V_{dc} \tag{15}$$

Hence, the voltage gain equation is obtained as:

$$G = \frac{V_o}{V_{dc}} = \frac{n-1+nD}{(1-D)^2\,(n-1)} \tag{16}$$

The voltage gain of the proposed converter from (16) is plotted in Fig. 4. It can be seen that the voltage gain of the proposed MCQ-MSC can be increased by decreasing *n*. This interesting feature of the proposed converter leads to lower the converter's size, control complexity, and implementation cost.

Furthermore, considering the described operating principles in Fig. 2, the dynamic equations of the proposed MCQ-MSC can be extracted. In this regard, the voltages of all inductors (i_{L1}, i_{L2}, and i_{Lm}) and the currents of the capacitors (i_{C0}, i_{C1}, i_{C2}, and i_{C3}) should be calculated. Accordingly, all the dynamic equations are summarized in Table I.

III. Circuit Analysis of the Proposed Converter

A. Voltage Gain Analysis in Steady-State

Ideally, the losses of the source, diodes, inductors, and power switch are neglected. In addition, the voltage ripples of the capacitors are negligible. Moreover, the voltage relation between windings N_1 and N_2 is assumed as:

$$n = \frac{V_{N1}}{V_{N2}} \tag{1}$$

Thus, from Fig. 2(a) and by applying Kirchhoff's Voltage Law (KVL) in state I, the voltage expressions of the inductors and magnetizing L_m are given as:

$$V_{L1} = V_{dc} \tag{2}$$
$$V_{L2} = V_{C1} \tag{3}$$
$$V_{Lm} = \frac{V_{C3} - V_{C2}}{n-1} \tag{4}$$

From Fig. 2(b) and by applying KVL in state II, the voltage equations of the inductors and the magnetizing L_m are:

$$V_{L1} = V_{dc} - V_{C1} \tag{5}$$
$$V_{L2} = V_{C1} + V_{C2} - V_o \tag{6}$$

B. Voltage Stress on the Semiconductors

According to Fig. 2(b), the voltage stress on the switch is the difference between V_O and V_{C2}. Consequently, the voltage on the power switch (V_S) is obtained as:

$$V_S = V_o - V_{C2} = \frac{(n-1)V_o}{n-1+nD} \tag{17}$$

From Fig. 2(a), the voltage stress on the diode D_1 is derived as

$$V_{D1} = V_{C1} = \frac{(1-D)\,(n-1)V_o}{(n-1+nD)} \tag{18}$$

From Fig. 2(b), the voltage stress on the diode D_2 is derived as

$$V_{D2} = V_o - V_{C1} - V_{C2} = \frac{D\,(n-1)V_o}{n-1+nD} \tag{19}$$

From Fig. 2(a), the voltage stress on the diode D_3 is obtained in (20).

$$V_{D3} = \frac{V_{C3} - V_{C2}}{n - 1} + V_{C3} = \frac{nV_o}{n - 1 + nD} \qquad (20)$$

From Fig. 2(a), the voltage stress on the output diode (D_o) is derived as (21).

$$V_{Do} = V_o - V_{C2} = \frac{(n - 1)V_o}{n - 1 + nD} \qquad (21)$$

C. Dynamic Response Evaluations

Considering the described operating principles in Fig. 2, the dynamic equations of the proposed MCQ-MSC can be extracted. In this regard, the voltages of all inductors (i_{L1}, i_{L2}, and i_{Lm}) and the currents of the capacitors (i_{C0}, i_{C1}, i_{C2}, and i_{C3}) should be calculated. Accordingly, all the dynamic equations are summarized in Table I. In this section, the frequency response (Bode plot) from input-to-output voltages (Vo/Vin) and control-to-output voltage (Vo/d) of the proposed converter obtained in Simulink/ MATLAB are depicted in Fig. 5 (a) and (b). Regarding these figures, the suggested converter is stable with nonminimum phase behavior. This is because of the right half-plane (RHP) zero in the control-to-output transfer function. The nonminimum phase behavior imposes an extra phase shift to the transfer function's loop gain and limits the converter's bandwidth. The values of parameters are Vin = 24 V, D = 0.52, f=40 kHz, R = 100 Ω, $L_1 = L_2 = 200$ uH, $C_1 = C_2 = C_3 = C_o = 100$uF.
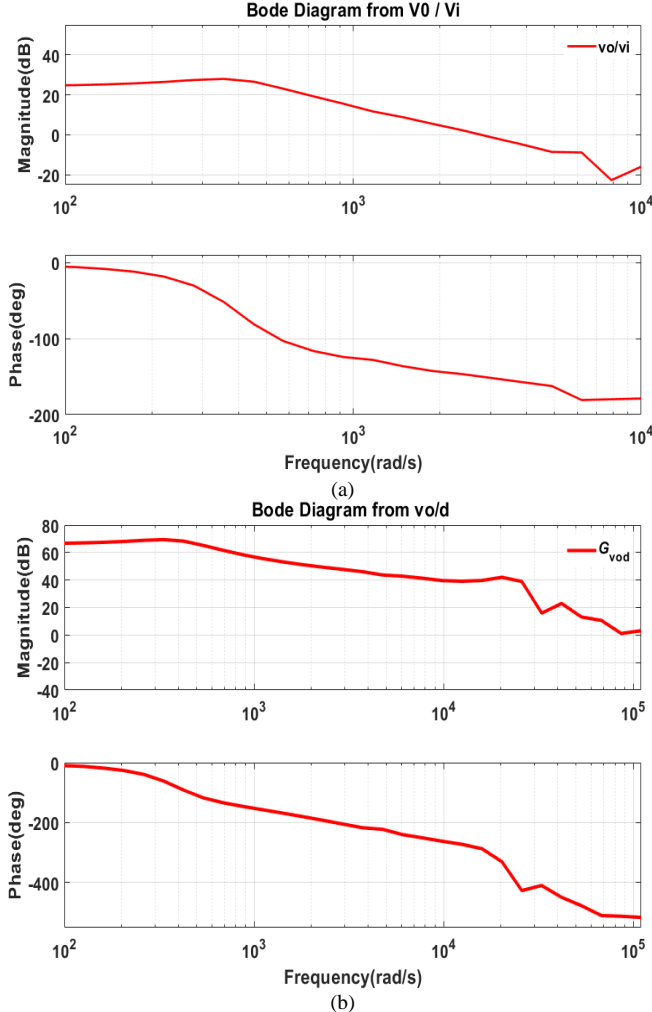

Fig. 5. Bode plot diagrams of the proposed converter. (a) input-to-output and (b) control-to-output.

IV. COMPARISON OF THE PROPOSED MCQ-MSC AND SIMILAR TOPOLOGIES

A. Voltage Stress Comparative analysis

Table II compares similar quadratic non-isolated high gain converters for physical and operational features to demonstrate the proposed circuit's advantages. Physical features include the number of switches (s), diode (d), capacitor (s), coupled-inductor (CI), inductor (L), and total device count (T). Also, operational ones consist of voltage gain, stress, boosting, and soft/hard switching. For a fair comparison, the transformer's turns ratio of the presented topology is supposed $n=N_1/N_2$.

Fig. 6 to Fig. 9 compare the voltage gain and voltage stress across the semiconductors in the proposed and similar converters. Fig. 6 illustrates the voltage gain versus the switching duty cycle of the proposed and conventional topologies for $n = 1.25$ (see Table II). Accordingly, the proposed MCQ-MSC topology offers the highest voltage gain for the duty cycle range of $D>0.35$. Comparisons of the normalized maximum voltage stress across the power switch and the output diode (D_o) are provided in Fig. 7 and Fig. 8, respectively. MCQ-MSC offers the lowest voltage stress compared with similar conventional topologies. This leads to low-cost semiconductor switches and diodes with lower power loss. MCQ-MSC offers a broader switching duty ratio control range than the conventional transformer-based impedance source DC-DC converters.
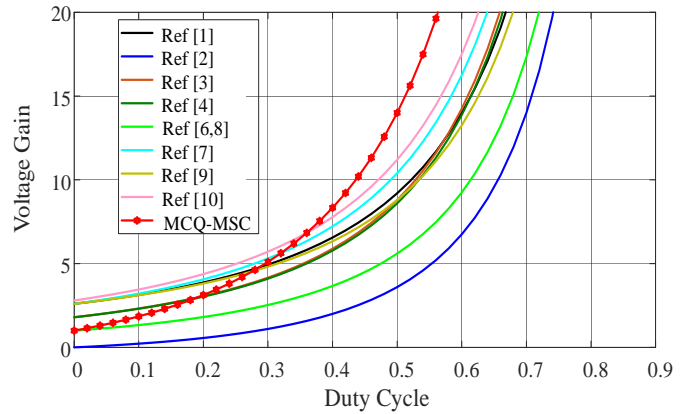

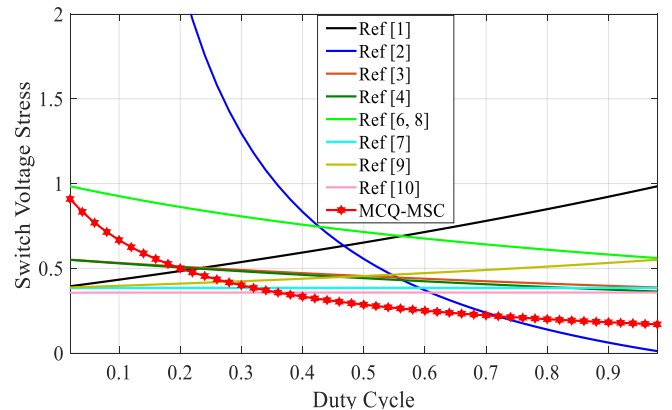Fig.6. Comparison of the voltage gains of the proposed MCQ-MSC and similar conventional converters for n=1.25.

Fig. 7. Comparison of the normalized voltage stress on the power switch in the proposed MCQ-MSC and similar conventional topologies for n=1.25.
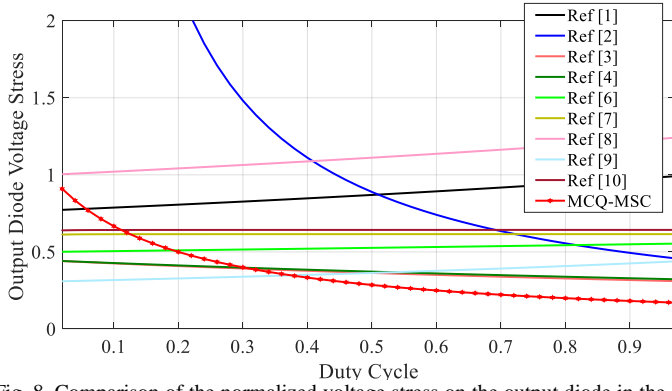
Fig. 8. Comparison of the normalized voltage stress on the output diode in the proposed MCQ-MSC and similar conventional topologies for n=1.25.
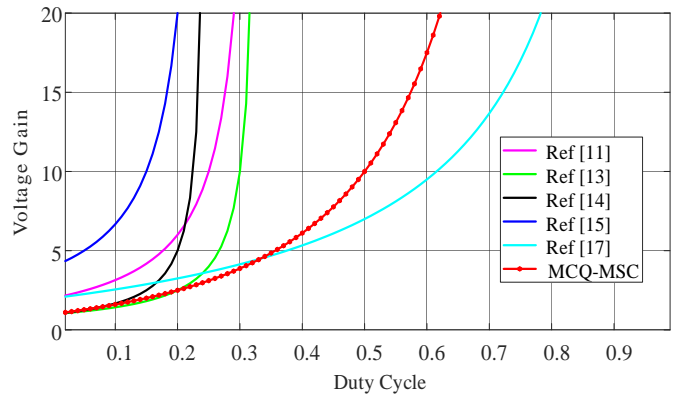

Fig. 9. Comparison of the voltage gain and control range of duty cycle in the proposed MCQ-MSC and conventional trans inverse converters for n=1.5.

Fig. 9 proves that Γ-source [13] and asymmetrical Γ-source [14] networks and the proposed trans-inverse converters in [11] and [15] suffer from the narrow switching duty ratio control range.

In addition, the proposed MCQ-MSC provides a higher voltage gain compared with the new trans-inverse semi-SEPIC converter [17], which offers a higher voltage gain in the minor switching duty cycle.

TABLE I. DYNAMIC EQUATIONS OF THE PROPOSED MCQ-MSC

parameter	value		
	Mode I ($t_0 < t < t_1$)	Mode II ($t_1 < t < t_2$)	Mode III ($t_2 < t < t_3$)
$L_1 \frac{di_{L1}}{dt}$	v_{dc}	$v_{dc} - v_{C1}$	$v_{dc} - v_{C1}$
$L_2 \frac{di_{L2}}{dt}$	v_{C1}	$v_{C1} + v_{C2} - v_{CO}$	$v_{C1} - v_{C3} + \frac{v_{C2}}{n}$
$L_m \frac{di_{Lm}}{dt}$	$\frac{v_{C2}-v_{C3}}{1-n}$	$-\frac{v_{C2}}{n}$	$-\frac{v_{c2}}{n}$
$C_o \frac{dv_{Co}}{dt}$	$-\frac{v_o}{R}$	$C_o\left(\frac{1}{(C_3+C_o)}i_{L2} - \frac{1}{(C_3+C_o)}\frac{v_{co}}{R} + \frac{C_3(n-1)}{C_2(C_3+C_o)n^2+C_oC_3(n-1)^2}i_{Lm} - \frac{C_3(C_3+nC_o)(n-1)}{C_2(C_3+C_o)n^2+C_oC_3(n-1)^2}i_{L2} - \left(\frac{\frac{C_3}{(C_3+C_o)}(1-\frac{C_o}{(C_3+C_o)})(\frac{n-1}{n})^2}{(C_2+\frac{C_oC_3(n-1)^2}{(C_3+C_o)n^2})}\right)\frac{v_{co}}{R} \right)$	$-\frac{v_o}{R}$
$C_1 \frac{dv_{c1}}{dt}$	$-i_{L2}$	$i_{L1} - i_{L2}$	$i_{L1} - i_{L2}$
$C_2 \frac{dv_{c2}}{dt}$	$\frac{i_{Lm}}{n-1}$	$C_2\left(\frac{\frac{1}{n}}{(C_2+\frac{C_oC_3(1-\frac{1}{n})^2}{(C_3+C_o)})}i_{Lm} - \frac{\frac{1}{n}(C_3+C_o)+C_o(1-\frac{1}{n})}{(C_2+\frac{C_oC_3(1-\frac{1}{n})^2}{(C_3+C_o)})(C_3+C_o)}i_{L2} - \frac{n(n-1)C_3}{C_2(C_3+C_o)n^2+C_oC_3(n-1)^2}\frac{v_{co}}{R} \right)$	$\frac{i_{Lm}-i_{L2}}{n}$
$C_3 \frac{dv_{c3}}{dt}$	$\frac{i_{Lm}}{1-n}$	$\left(\frac{1}{(1-n)} - \frac{C_2}{(1-n)(C_2+\frac{C_oC_3(1-\frac{1}{n})^2}{(C_3+C_o)})}\right)i_{Lm} - \left(\frac{C_2(n-1)(1-\frac{C_o}{(C_3+C_o)})}{(1-n)(C_2+\frac{C_oC_3(1-\frac{1}{n})^2}{(C_3+C_o)})}\right)\frac{v_{co}}{R} + \left(-\frac{n}{(1-n)} - \frac{C_2(C_3+C_o)+C_oC_2(n-1)}{(1-n)(C_2+\frac{C_oC_3(1-\frac{1}{n})^2}{(C_3+C_o)})(C_3+C_o)}\right)i_{L2}$	i_{L2}

B. Components Load Factors Evaluation

This section investigates components load factors (CLFs) as an evaluation metric of the proposed converter. Since the number of the components in the proposed converter and the selected topologies is different, the CLF of the power switch, input inductor, coupled transformer, output diode, and output capacitor are investigated as a fair comparison, and according to [21-23], the CLF can be expressed by (22); Where $(V^*.I^*)$ and P_{Total} represent the apparent power of a component and the total load power, respectively. Ideally, power losses are not considered, and it is assumed that $P_{Total} = P_{IN} = V_{dc} . I_{L1}$.

$$CLF = \frac{V^*.I^*}{P_{Total}} \tag{22}$$

In addition, the ripples of the RMS currents are ignored. For the used MOSFET, the peak voltage stress across the power switch is assumed as V^*, and the RMS value of its current is applied for I^*. Hence, the CLF of the power switch can be calculated as follow:

$$S - CLF = \frac{V_{sw,max} . I_{S,RMS}}{V_{dc} . I_{L1}} \tag{23}$$

Like the MOSFET CLF, the maximum blocking voltage of diode is chosen as V^*. Furthermore, the average current of the output diode is selected as I^*. Thus,

$$D_O - CLF = \frac{V_{D4,max} . I_{Do,Avg}}{V_{dc} . I_{L1}} \tag{24}$$

For the input inductor and coupled transformer, the average voltage and RMS current of the inductors and windings are selected as V^* and I^*, respectively. Hence, for the input inductor and coupled transformer, (25) and (26) are obtained.

$$L_1 - CLF = \frac{V_{L_1,Avg} . I_{L1,RMS}}{V_{dc} . I_{L1}} \tag{25}$$

$$T - CLF = \frac{V_{N_1,Avg} . I_{N1,RMS} + V_{N_2,Avg} . I_{N2,RMS}}{V_{dc} . I_{L1}} \tag{26}$$

According to the obtained equations, the CLF amounts of the used components for the selected converters in [1], [2], [6], and the proposed converter at the boost factor of 13.8 are demonstrated in Fig. 10. It can be seen that MCQ-MSC provides lower semiconductors (power switch and output diode) CLF than the selected topologies. As a result, the proposed converter can be a better choice for high voltage applications when the lower stress of the semiconductors is a vital issue.

V. DESIGN CONSIDERATION OF THE PROPOSED MCQ-MSC

L_1: The input inductor (L_1) limits the input current ripple. It can be designed based on (27). Where, ΔI_{L1} represents the maximum permitted current ripple.

$$L_1 = \frac{V_{L1}.D}{\Delta I_{L1}.f_s} > \frac{V_{dc}.D}{\Delta I_{in}.f_s} \tag{27}$$

L_2: For the allowable current ripple (ΔI_{L2}), the minimum value of the inductor L_2 is calculated as:

$$L_2 = \frac{V_{L2}.D}{\Delta I_{L2}.f_s} > \frac{V_{dc}.D}{(1-D)^2 \Delta I_{Lin}.f_s} \tag{28}$$

L_m: Furthermore, the proper value of the magnetizing inductor of the coupled inductor can be determined by:

$$L_M > \frac{V_{Lm}.(1-D)}{\Delta I_{LM}.f_s} > \frac{nD.V_{dc}}{(1-D)\Delta I_o.(n-1)f_s} \tag{29}$$

C_o: To limit the output voltage ripple, the output capacitor (C_o) can be obtained as in (30). Where ΔV_{Co} is the maximum tolerant voltage ripple, usually recommended as $1\%.V_o$.

$$C_o = \frac{DV_{out}}{R_L.\Delta V_{co}.f_s} \tag{30}$$

C_1, C_2, and C_3: Moreover, other circuit capacitors can be designed based on their maximum current values and the allowable voltage ripple as in (31)-(33), where, ΔV_{Ci} is the maximum voltage ripple of each capacitor.

$$C_1 = \frac{D.i_{L2}}{\Delta V_{C1}.f_s} = \frac{(1-D)GV_{out}}{\Delta V_{C1} R_L.f_s} \tag{31}$$

$$C_2 = \frac{i_{c2}.D}{\Delta V_{c2}.f_s} = \frac{i_{N2}.D}{\Delta V_{c2}.f_s} \tag{32}$$

$$C_3 = \frac{i_{c3}.D}{\Delta V_{c3}.f_s} = \frac{i_{N2}.D}{\Delta V_{c3}.f_s} \tag{33}$$
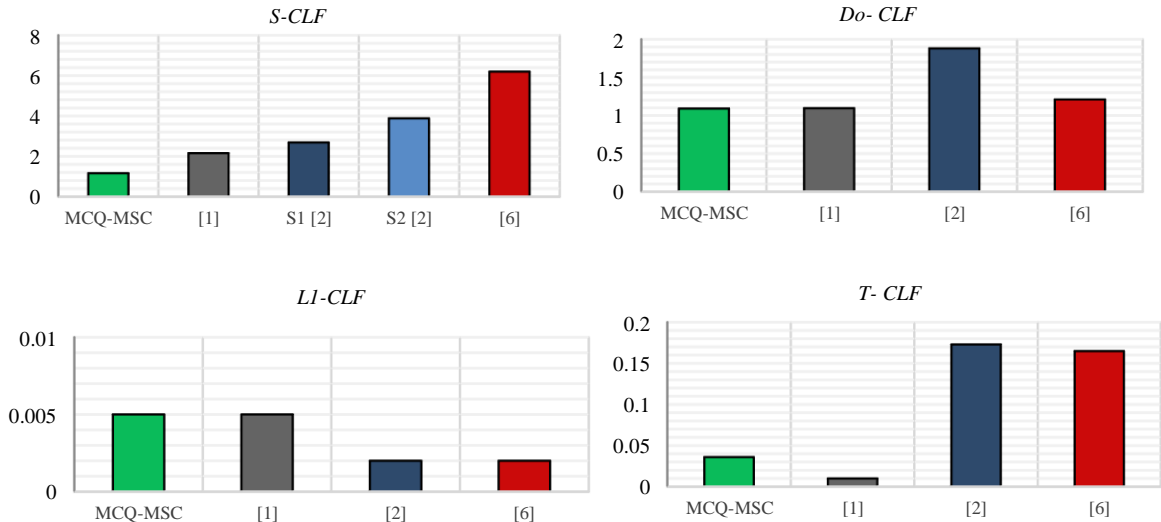

Fig. 10. Values of the components load factors at G= 13.8.

TABLE II. COMPARISON OF THE HIGH VOLTAGE NON-ISOLATED QUADRATIC CONVERTERS

Converter Topology	[1]	[3]	[4]	[6]	[7]	[8]	[P]
s	2	1	1	1	2	1	1
d	4	6	6	6	6	5	4
c	4	5	5	4	6	3	4
CI+L	1+1	1+1	1+1	1+2	1+1	1+2	1+2
T	12	14	14	14	16	12	12
Voltage Gain	$\dfrac{1 + D + 2(\frac{1-D}{n})}{(1-D)^2}$	$\dfrac{1 + \frac{1}{n} + \frac{D}{n}}{(1-D)^2}$	$\dfrac{(\frac{3D+2}{n}) + (2-D)}{2(1-D)^2}$	$\dfrac{1 + \frac{D}{n}}{(1-D)^2}$	$\dfrac{1 + \frac{2}{n}}{(1-D)^2}$	$\dfrac{1 + \frac{D}{n}}{(1-D)^2}$	$\dfrac{n-1+nD}{(1-D)^2\,(n-1)}$
Voltage - Boosting Technique	Cascade Connection of Boost and Buck-Boost converters + Coupled Inductor	Voltage Multiplier Cell+ Boost Converter + Coupled Inductor	Switched-Capacitor + Coupled Inductor	Quadratic Boost Converter + Coupled Inductor	Quadratic Quadrupler Boost Converter + Coupled Inductor	Quadratic Fly back Converter + Coupled Inductor	Quadratic Boost Converter + Coupled Inductor
Parameterized switch (Vs/Vo)	$\dfrac{(1+D)}{1 + D + 2(\frac{1-D}{n})}$	$\dfrac{1}{1 + \frac{1}{n} + \frac{D}{n}}$	$\dfrac{(2 + D(\frac{1}{n}-1))}{(\frac{3D+2}{n}) + (2-D)}$	$\dfrac{1}{1 + \frac{D}{n}}$	$\dfrac{1}{1 + \frac{2}{n}}$	$\dfrac{1}{1 + \frac{D}{n}}$	$\dfrac{(n-1)}{n-1+nD}$
Voltage Stress on Output Diodes	$\dfrac{(1 + \frac{2-D}{n})V_o}{(1-D)^2}$	$\dfrac{(\frac{V_o}{n})}{1 + \frac{1}{n} + \frac{D}{n}}$	$\dfrac{(\frac{2V_o}{n})}{\frac{3D+2}{n} + (2-D)}$	$\dfrac{(2 + D(\frac{1}{n}-1))V_o}{1 + (\frac{1}{n})D}$	$\dfrac{(\frac{V_o}{n})}{1 + \frac{2}{n}}$	$\dfrac{(1 + D(\frac{1}{n}-1))V_o}{1 + (\frac{D}{n})D}$	$\dfrac{(n-1)V_o}{n-1+nD}$
Soft-Switching	No	No	No	No	Yes	No	No
Efficiency at P$_O$=100W	96.1 %	93.1 %	93 %	92.8 %	91 %	93 %	93 %

VI. EXPERIMENTAL RESULTS

A hardware prototype of the proposed MCQ-MSC is designed, fabricated, and implemented to verify theoretical analyses. Considering the renewable sources' low output voltage, the proposed converter's input voltage is kept low (29 V), whereas the proposed converter's output voltage is considered high (400 V) as desired for the DC microgrids and electric vehicles. Under these conditions, the operation of the proposed topology is evaluated both in steady and dynamic state conditions. A photo of the experimental setup is depicted in Fig. 11. The circuit parameters of the proposed converter are given in Table III. The coupled inductor is executed using an iron powder core, and its turn ratio is n=1.35.
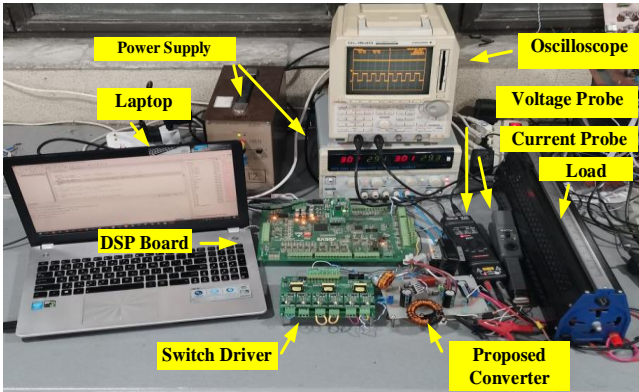

Fig. 11. Photo of the experimental setup.

TABLE III. CIRCUIT PARAMETERS

Components	Type
MOSFET	IRFP460
Diode	MUR860
DSP	TMS320F28335
Drivers	LPE113-01-01
Voltage Sensor	Minmax-MAU1511627
Current Sensor	Honeywell-CSNE151-100
Switching frequency	40 kHz
L$_1$= L$_2$	200µH
C$_1$= C$_2$= C$_3$= C$_4$	100µF

The dual loop PI controller is employed to analyse the proposed converter's closed-loop operation, shown in Fig. 12. The outer loop regulates the output voltage, and the inner loop controls the input inductor L_1 current. The controller is implemented through a digital signal processor (DSP) with a sampling time (T$_S$) of 100 microseconds.

Fig. 13(a) illustrates the circuit's voltage waveforms for D=0.53. The input voltage is 29 V, and the output voltage approaches 400 V, verifying (16). Similarly, Fig. 13(b) shows identical waveforms for D=0.6. Fig. 14 shows the current and voltage waveforms of the inductors (L_1 and L_2) under steady-state operation. The performance of both inductor currents is stable and reacts smoothly at exact variation moments. In addition, the inductors' voltages confirm that L_1 and L_2 charge and discharge correctly. Also, the voltage and current waveforms of the switch are shown in Fig. 15.

The proposed converter's transient response is first evaluated under a sudden change in the output voltage reference. Fig. 16 shows the dynamic response of the proposed

converter when the output voltage reference changes from 400 volts to 350 volts while the input voltage is kept constant during the test. In such conditions, the output load Ro is 780 Ω. It is noted that the converter reacts rapidly to this change, and the output voltage reaches smoothly to its new level. Furthermore, the DC-DC converter is tested due to a load alteration. Fig. 17 demonstrates the transient performance of the proposed converter when the output load varies from Ro=640 Ω to Ro=500 Ω. As can be perceived, after an acceptable undershoot at the exact load alteration moment, the output voltage approaches the steady-state conditions. Also, the output current responds appropriately to this change.
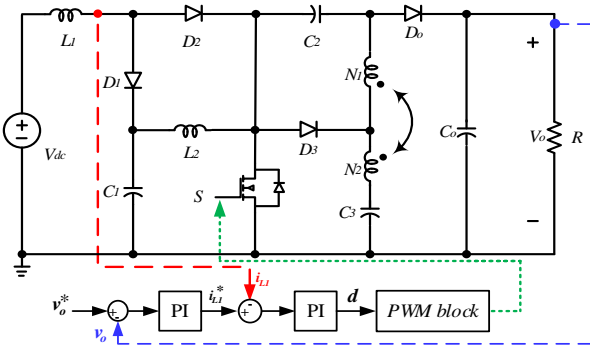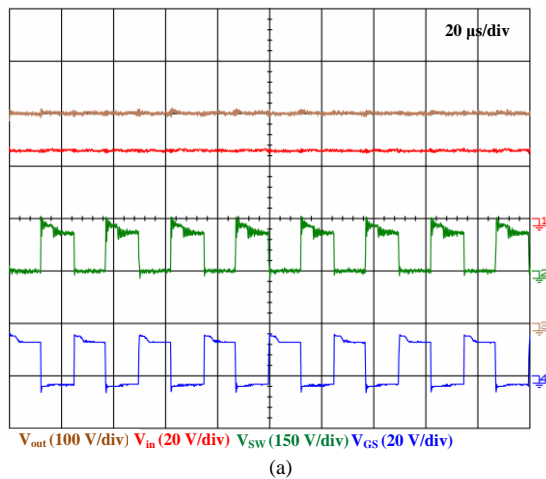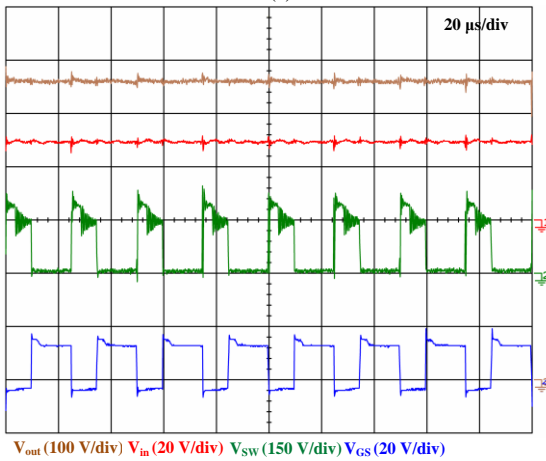

Fig. 12. Schematic overview of the closed-loop control for MCQ-MSC.

V$_{out}$ (100 V/div) V$_{in}$ (20 V/div) V$_{SW}$ (150 V/div) V$_{GS}$ (20 V/div)

(a)

V$_{out}$ (100 V/div) V$_{in}$ (20 V/div) V$_{SW}$ (150 V/div) V$_{GS}$ (20 V/div)

(b)

Fig. 13. Output waveforms of the proposed MCQ-MSC for different values of d. (a) For D=0.53. (b) For D=0.6.

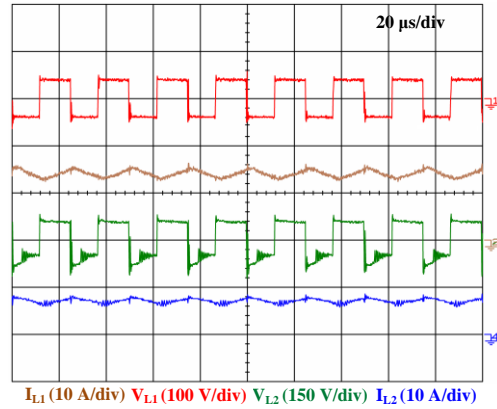**I$_{L1}$ (10 A/div) V$_{L1}$ (100 V/div) V$_{L2}$ (150 V/div) I$_{L2}$ (10 A/div)**

Fig. 14. The proposed MCQ-MSC inductors L$_1$ and L$_2$ steady-state response.

Vout (200 V/div) I$_{sw}$ (20 A/div) V$_{sw}$ (150 V/div)
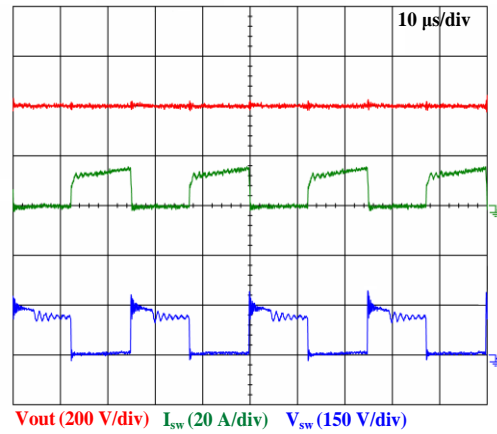
Fig. 15. The proposed MCQ-MSC switch steady-state response.

I$_{out}$ (0.5 A/div) V$_{out}$ (100 V/div) I$_{in}$ (5 A/div) V$_{in}$ (20 V/div)
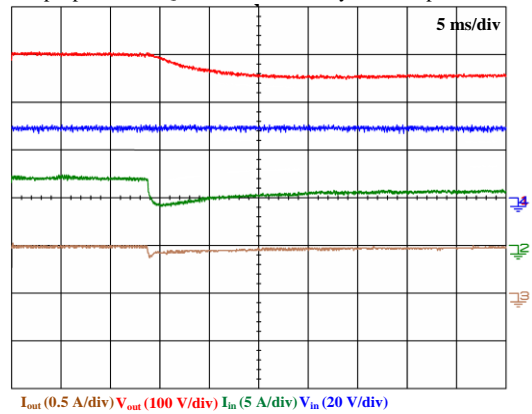
Fig. 16. Transient response of the proposed MCQ-MSC when output voltage reference changes from 400 V to 350 V.

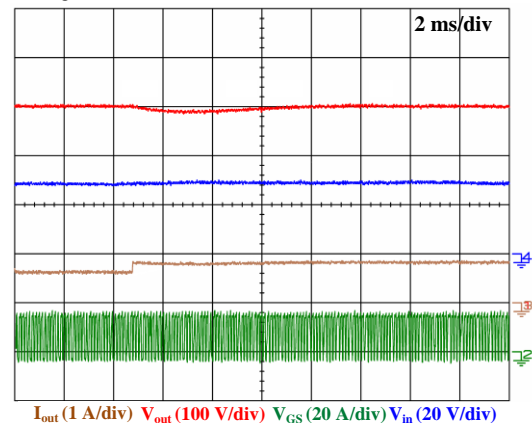**I$_{out}$ (1 A/div) V$_{out}$ (100 V/div) V$_{GS}$ (20 A/div) V$_{in}$ (20 V/div)**

Fig. 17. Dynamic response of MCQ-MSC under a sudden output load change.

VII. POWER LOSS ANALYSIS

The significant power losses originate from the capacitors' semiconductors losses, magnetic losses, and ESR [24-26]. The switch power loss includes the MOSFET conduction and switching losses. Hence, the transistor's conduction loss is obtained from (34); Where r_{DS}, $I_{S,AVG}$ and $I_{S,RMS}$ represent the On-resistance of MOSFET and average and RMS values of the transistor's current, respectively.

$$P_{con} = r_{DS} I_{S,RMS}^2 + V_{DS,on} I_{S,AVG} \tag{34}$$

Likewise, the turn-on and turn-off switching power loss of the switch can be calculated from (35):

$$\begin{cases} P_{sw-ON} = 0.5 f_{sw} I_{DS(ON)} V_{DS} t_{ON} \\ P_{sw-OFF} = 0.5 f_{sw} I_{DS(OFF)} V_{DS} t_{OFF} \end{cases} \tag{35}$$

Where $I_{DS(ON)}$ and $I_{DS(OFF)}$ are the MOSFET current at turn-on and turn-off instants, respectively. Likewise, t_{ON} and t_{OFF} represent the time of turn-on and turn-off transition of the power switch. Hence, the switching power loss of the MOSFET is:

$$\begin{aligned} P_{sw} &= P_{sw-ON} + P_{sw-OFF} \\ &= 0.5 f_{sw} V_{DS} (I_{DS(ON)} t_{ON} + I_{DS(OFF)} t_{OFF}) \end{aligned} \tag{36}$$

Hence, the power loss in the power switch is expressed by:

$$\begin{aligned} P_{FET} &= P_{con} + P_{sw} = r_{DS} I_{S,RMS}^2 + \\ &0.5 f_{sw} V_{DS} (I_{DS(ON)} t_{ON} + I_{DS(OFF)} t_{OFF}) \end{aligned} \tag{37}$$

The forward voltage drop power losses of the diodes can be expressed by:

$$P_{V_F} = \sum_{i=1}^{4} V_F I_{Di} \tag{38}$$

Where V_F and I_{Di} are forward voltage drops and average currents of diodes. In addition, the power losses of the diodes due to their parasitic resistances (r_D) are expressed by (39); Where $I_{Di,RMS}$ is the RMS value of diodes' currents.

$$P_{r_D} = \sum_{i=1}^{4} r_D . I_{Di,RMS}^2 \tag{39}$$

Thus, the total power losses of the diodes can be obtained as:

$$P_D = P_{VF} + P_{r_D} = \sum_{i=1}^{4} V_F I_{Di} + \sum_{i=1}^{4} r_D . I_{Di,RMS}^2 \tag{40}$$

The magnetic power losses come from core, copper, and ESR losses. From [24], the coupled inductors' core losses are gained by (41). Where B_{max}, β, K_{fe}, A_c, and l_m present peak AC flux density, core loss exponent, core loss coefficient, core cross-sectional area, and mean magnetic path length, respectively.

$$P_{fe} = B_{max}^{\beta} K_{fe} A_c l_m \tag{41}$$

Additionally, the copper losses of the L_1, L_2, and coupled inductors can be obtained from (42-44):

$$P_{cu,L1} = \frac{\rho I_{L1,RMS}^2 (MLT)}{W_A K_u} \tag{42}$$

$$P_{cu,L2} = \frac{\rho I_{L2,RMS}^2 (MLT)}{W_A K_u} \tag{43}$$

$$P_{cu,T} = \frac{\rho (N_1 I_{N1,RMS} + N_2 I_{N2,RMS})^2 (MLT)}{W_A K_u} \tag{44}$$

Where ρ, $I_{L1,RMS}$, $I_{L2,RMS}$, MLT, WA, Ku, N_1, N_2, $I_{N1,RMS}$, and $I_{N2,RMS}$ present wire effective resistivity, input inductor's RMS current, RMS current of L_2, mean length per turn, core window area, winding fill factor, the primary winding turns number, the secondary winding turns number, RMS current of the primary winding, and RMS current of the secondary winding, respectively. Also, the power losses of the magnetic components due to their parasitic resistances are expressed by:

$$P_{ESR,L} = r_{L1} I_{L1,RMS}^2 + r_{L2} I_{L2,RMS}^2 + r_{N1} I_{N1,RMS}^2 + r_{N2} I_{N2,RMS}^2 \tag{45}$$

Hence, the total magnetic components' power losses is:

$$P_L = P_{cu,L1} + P_{cu,L1} + P_{cu,T} + P_{fe} + P_{ESR,L} \tag{46}$$

The power losses of capacitors' ESRs are derived as:

$$P_C = P_{ESR,C} = \sum_{i=1}^{4} r_{Ci} . I_{Ci,RMS}^2 \tag{47}$$

Thus, the total power losses of the proposed converter can be attained as (48).

$$P_{Loss,Total} = P_S + P_D + P_L + P_C \tag{48}$$

The efficiency of the proposed MCQ-MSC is calculated based on the theoretical relations, simulation results, datasheets, and magnetic elements' design. Additionally, C_O, r_{L1}, r_{L2} r_{N1}, r_{N2}, r_C are about 5 nF, 0.2 Ω, 0.2 Ω, 0.1 Ω, and 0.08 Ω, respectively. Fig. 18. shows the calculated efficiency of the proposed converter for various load currents and output voltages.

The full load efficiency (overall) is confirmed by experimental setup to be η=365 / (365+40) ≈ 90 percent. The power loss distribution at the full load (based on calculation) is shown in Fig. 19.
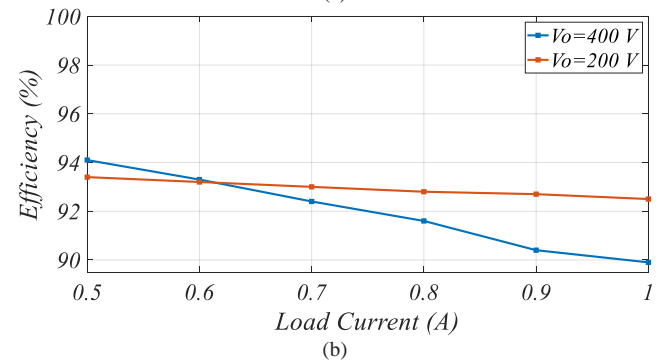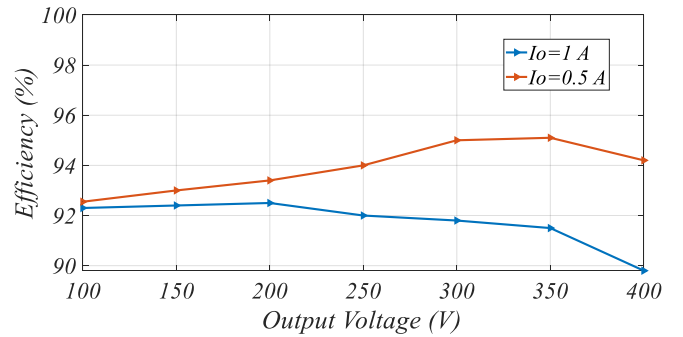

(a)

(b)

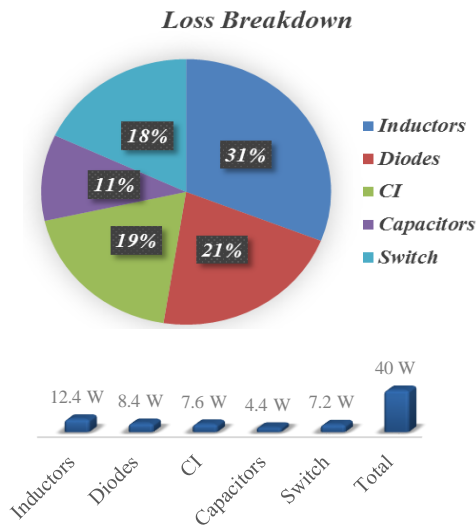Fig. 18. Calculated efficiencies of the proposed MCQ-MSC for different load currents and output voltages

Fig. 19. Power loss distribution at Po= 365W (based on calculation, overall efficiency confirmed by experiment at full load)

VIII. CONCLUSION

This paper proposes a new high-gain dc-dc converter suitable for high voltage and renewable energy applications. The proposed converter employs a single power switch, simplifying the control process. It integrates a coupled inductor and a voltage boosting module to achieve high output voltage applicable for DC microgrid and EV charging systems. Because of the unique design of the coupled transformer, the proposed converter attains a high voltage gain for a low and easily controllable value of the duty cycle. Unlike the conventional impedance source topologies and most other high voltage gain DC-DC topologies, the proposed MCQ-MSC provides a wide control range of switching duty cycle instead of the narrow range. The presented converter not only inherits the advantages of the non-isolated transformer types of quadratics and SEPIC converters but also offers a higher voltage transfer ratio with the low normalized voltage stress across its semiconductors. Besides, a clamping circuit provides a safe path for the leakage inductance energy and avoids generating voltage spikes across the power switch. Finally, experimental results have been presented to verify the proposed converter's operation.

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