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Degenerate parallel conducting layer and conductivity type conversion observed from p-$Ge_{1-y}Sn_y$ (y = 0.06%) grown on n-Si substrate

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Electrical properties of p-$Ge_{1-y}Sn_y$ (y = 0.06%) grown on n-Si substrate were investigated through temperature-dependent Hall-effect measurements. It was found that there exists a degenerate parallel conducting layer in $Ge_{1-y}Sn_y$/Si and a second, deeper acceptor in addition to a shallow acceptor. This parallel conducting layer dominates the electrical properties of the $Ge_{1-y}Sn_y$ layer below 50 K and also significantly affects those properties at higher temperatures. Additionally, a conductivity type conversion from p to n was observed around 370 K for this sample. A two-layer conducting model was used to extract the carrier concentration and mobility of the $Ge_{1-y}Sn_y$ layer alone. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4754625]

There has been a great interest in the possibility of broadening the role of Si technology into the realm of optical signal generation and processing. This concept represents a paradigm in the integration of Si electronics with Si-based photonics in the same single Si chip. Unfortunately, group-IV semiconductors are poor light emitters due to the indirect nature of electronic bandgap, and thus there are no practical Si- or Ge-based light sources yet. In order to overcome the limitations imposed on these indirect bandgap semiconductors, a strong interest has recently emerged in engineering Si- and Ge-based direct bandgap semiconductors. In the case of Ge, direct-bandgap light emission[1,2] as well as an optically pumped Ge laser[3] have been demonstrated using n-type doped tensile-strained Ge-on-Si. As an alternative, fabrication of Sn-containing, device-quality, relaxed, broad range of $Ge_{1-y}Sn_y$ binary alloys[4,5] and $Ge_{1-x-y}Si_xSn_y$ ternary alloys[6,7] deposited directly on Si substrates has been demonstrated. It was reported that the $Ge_{1-y}Sn_y$ alloys grown on Si undergoes an indirect to direct bandgap transition near y = 0.06–0.08,[8] which is substantially lower than the theoretically predicted Sn content of y = 0.2.[9] Mathews *et al.*[10] reported direct-bandgap photoluminescence with tunable emission wavelength depending on the Sn concentration in $Ge_{1-y}Sn_y$ alloys grown on Si. Direct-bandgap electroluminescence was also observed from Si/$Ge_{1-y}Sn_y$ p-i-n heterostructure diodes.[11] Also, Werner *et al.*[12] produced GeSn p-i-n photodetectors grown by molecular beam epitaxy on Si. Very recently, a complementary metal oxide semiconductor compatible detector based on a 0.25% Sn-doped layer was reported.[13] All of these observations strongly indicate the possibility that the $Ge_{1-y}Sn_y$ materials may lead to Si- and Ge-based light emitting diodes, laser diodes, and other various optoelectronic devices, which can all be integrated with current Si technology on a single Si chip.

Although many structural and optical properties of $Ge_{1-y}Sn_y$ alloys have been studied,[4,14,15] very few studies have been carried out on the electrical properties of these materials.[13,16,17] Therefore, in order to better understand the electrical properties of these recently developed materials and to aid in the development of optoelectronic and electronic devices, temperature dependent Hall (TDH) effect measurements were made on the unintentionally doped p-$Ge_{1-y}Sn_y$ (y = 0.06%) epitaxial layer grown on n^--Si substrate, and the results are reported here.

The Ge-like material of $Ge_{0.9994}Sn_{0.0006}$ epitaxial layer was grown via deuterated stannane (SnD_4) assisted reactions of pure digermane (Ge_2H_6) at a low-temperature of 390 °C and at a pressure of 0.30 Torr directly on a high resistivity (>6000 Ω-cm) (100) n-type Si substrate using an ultra high vacuum chemical vapor deposition (UHVCVD) method.[4] The thickness of epitaxial film is estimated to be 800 nm as measured by Rutherford backscattering, and the thickness of Si substrate is 445 μm. After growth, the sample was annealed three times using rapid thermal annealing (RTA) at 680 °C for 10 s each. The RTA treatment reduces the levels of threading dislocations and relaxes the strain in the epitaxial layers.

Prior to ohmic contact metal deposition, the $Ge_{1-y}Sn_y$ wafer was cut into small pieces of 5×5 mm^2, degreased using acetone and methanol in an ultrasonic bath for 5 min, followed by a dip in a diluted HF solution for 10 s, a rinse in de-ionized water for 5 min, and finally blown dry with high purity nitrogen gas. The ohmic contacts were defined using photolithography and deposited by an e-beam deposition system with 200-Å Cr followed by 2000-Å Au at the four corners of the sample, and the contacts were not annealed. The TDH measurements were carried out using the van der Pauw method in a field of 5 kG at temperatures ranging from 25 to 700 K. The as-grown, annealed sample showed p-type conductivity.

The measured sheet carrier concentrations for the p-$Ge_{0.9994}Sn_{0.0006}$ sample (○ and ●) are plotted in Fig. 1 as a

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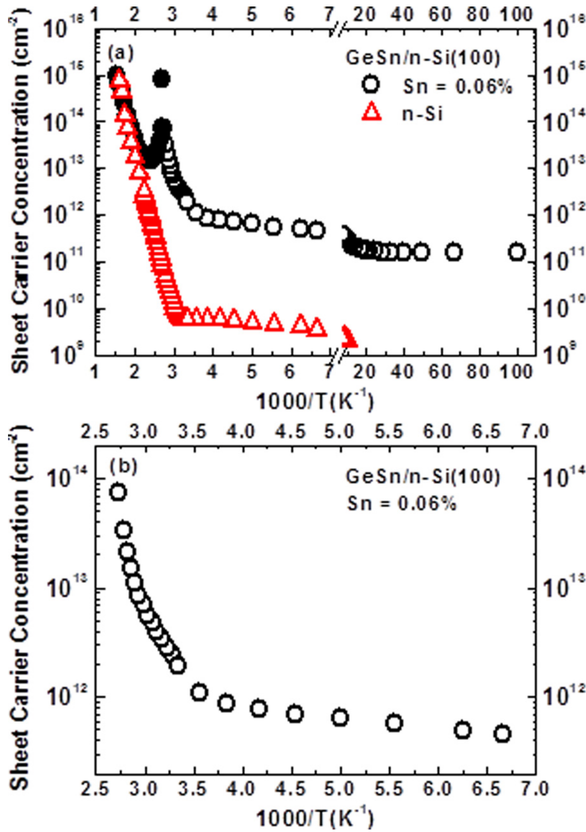

FIG. 1. (a) The apparent measured sheet hole carrier concentrations for p-$Ge_{0.9994}Sn_{0.0006}$/n^--Si sample (○ for p-type and ● for n-type) and n^--Si substrate (Δ) plotted as a function of inverse temperature. Open circles and solid circles indicate p- and n-type conductivity, respectively. The break in 1000/T axis separates the high and low temperature regimes for the purpose of clarity. (b) The apparent measured sheet hole carrier concentrations for the p-$Ge_{0.9994}Sn_{0.0006}$/n^--Si plotted as a function of inverse temperature with an expanded scale to show the two acceptor levels more clearly.

function of inverse temperature. For the purpose of clarity, a break in x-axis of Fig. 1(a) was made between the high and low temperature regimes. In order to determine the effect of the n^--Si substrate on the Hall measurements of the p-$Ge_{1-y}Sn_y$ layer, we also carried out Hall measurements of an identical n^--Si substrate (Δ) alone, and those results are plotted in Fig. 1(a) as well. As shown in Fig. 1(a), the p-type carrier concentration remains constant ($\sim 1.5 \times 10^{11}\,cm^{-2}$) below about 50 K, indicating the existence of a degenerate parallel conducting layer. Then, the carriers increase exponentially with temperature up to about 280 K due to the ionization of shallow acceptors as shown in the expanded scale plot of Fig. 1(b). As the temperature increases further above about 280 K, the hole concentration starts to increase again exponentially but with a different rate up to about 330 K, which is also clearly shown in Fig. 1(b), possibly indicating the activation of second, deeper acceptors. The hole concentration (○) increases rapidly with the further increase in temperature above around 330 K, reaching a carrier singularity peak near 370 K, where the apparent conductivity changes from p- to n-type. Then, the apparent n-type carrier concentration (●) decreases initially as the temperature increases further, and finally starts to increase exponentially with temperature due to increasing intrinsic carriers as shown in Fig. 1(a). The figure also shows the significant effect of Si substrate on the Hall data at these higher temperatures.

Similar conductivity type conversions and degenerate parallel conducting layers were also observed for unintentionally doped p-$Ge_{0.999}Sn_{0.001}$/n^--Si, p-$Si_{0.09}Ge_{0.882}Sn_{0.028}$/$n^-$-Si, and boron-doped p-Ge/n^--Si samples. For these samples, the conductivity type conversion from p to n occurred at 390, 385, and 440 K, and the observed sheet hole concentrations of the parallel conducting layers were 2.7×10^{11}, 3.58×10^{12}, and $7.0 \times 10^{11}\,cm^{-2}$, respectively. The detailed results of the Hall-effect measurements of these samples will be reported elsewhere. A zero Hall coefficient has also been previously reported in lightly boron-doped p-Si ($10^{12}\,cm^{-3}$),[18] boron-doped p-SiGeC thin film grown on n^--Si substrate,[19] and an unintentionally doped p-InSb grown on GaAs substrate.[20]

The degenerate parallel conducting layer observed below 50 K could be due to surface conducting layer,[20–22] impurity band,[23,24] and/or degenerate conducting layer in the interfacial region.[25,26] Since the degenerate conducting layer was observed from the unintentionally lightly p-type doped sample and shows temperature independent hole carriers, the first two cases could be ruled out. On the other hand, the structural properties of interfacial region of the similar sample were examined with high-resolution electron microscopy, showing the presence of periodic arrays of edge type dislocations confined to the interface plane without propagating to the top of the epitaxial layer.[17] Apparently, dislocation defects in the interfacial region were generated during growth to accommodate the misfit strain caused by a significant lattice mismatch between the $Ge_{1-y}Sn_y$ ($\sim$4% for $y \leq 0.1\%$) layer and the Si substrate. This implies that the observed parallel conducting layer could be due to the presence of a degenerate conducting layer in the interfacial region. However, further studies are needed to determine the exact source of a parallel conducting layer. The thickness of the parallel conducting layer is unknown at present.

It is well known that when both holes, p, and electrons, n, are present in a semiconductor, the Hall coefficient in the low magnetic field limit is given by[27]

$$R_H = \frac{p - b^2 n}{e(p + bn)^2},$$

where e is the electronic charge and $b = \mu_e/\mu_h$, where μ_e and μ_h are the electron and hole mobility, respectively. At low temperatures, the intrinsic carriers, n_i, freeze out, and the extrinsic p-type conduction becomes dominant for a p-type semiconductor. As temperature increases above around room temperature, intrinsic carriers come into play for narrow bandgap materials such as the current $Ge_{0.9994}Sn_{0.0006}$ and Ge samples, going through $R_H = 0$ when $p = b^2 n = b n_i$ with $n_i^2 = np$. As the temperature increases beyond the $R_H = 0$ point, where $p < b^2 n$ or $p < b n_i$, the contribution from the intrinsic electrons will become dominant because of their higher mobility (for the case when $\mu_e > \mu_h$), giving rise to an apparent n-type conduction in the Hall measurements. More specifically, when we assumed all acceptors, N_A, and donors, N_D, are ionized, $p(T) = [N_A - N_D] + n_i^2(T)/p(T) = [N_A - N_D] + n_i(T)/b$, and thus, the semiconductor may act as an apparent n-type material for $n_i \geq [N_A - N_D]b/(b^2 - 1)$.

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An accurate quantitative explanation for the change in the conductivity type for the current sample is not a simple matter due to several multiple conducting layers of p-$Ge_{1-y}Sn_y$ layer, p-interfacial layer, and n-Si substrate. Furthermore, in the high temperature region, the contribution of both intrinsic electrons and holes as well as their mobilities from p-$Ge_{1-y}Sn_y$ and n-Si substrate should also be taken into account for the conductivity type conversion along with those from the extrinsic carriers. In principle, if we knew all the necessary values for the epitaxial layer as well as the other conducting layers involved, then the type conversion temperature could be reasonably well predicted, but unfortunately, many of those parameters are unknown for the current sample. However, in order to have an idea of conductivity type conversion for this Ge-like p-$Ge_{0.9994}Sn_{0.0006}/n^-$-Si sample, a simplified calculation is illustrated here by neglecting the effects of intrinsic carriers and mobilities of n-Si substrate, and deep acceptor concentration and mobility. If we assume some reasonable values of parameters such as $\mu_e/\mu_h \approx 2.13$ (used the same value as bulk Ge[28]) and $(N_A - N_D) \approx 5 \times 10^{15}\,\mathrm{cm}^{-3}$ for $Ge_{1-y}Sn_y$ layer, then the p- to n-type conversion ($R_H = 0$) would occur at around $n_i \approx [N_A - N_D]b/(b^2 - 1) \approx 3 \times 10^{15}\,\mathrm{cm}^{-3}$, which corresponds to the value of intrinsic carriers in Ge (GeSn) around 426 K. This value is roughly comparable with the observed type-conversion temperature of 370 K for the Ge-like p-$Ge_{0.9994}Sn_{0.0006}$. Note here that as shown in Fig. 1(a), the effect of n^--Si substrate in the high temperature region could be significant, and it could further bring down the type conversion temperature.

The apparent measured Hall mobilities of the $Ge_{0.9994}Sn_{0.0006}$ sample are plotted in the inset of Fig. 2 as a function of temperature. The mobilities at very low temperatures remain approximately constant at around 110 $\mathrm{cm^2/V{\cdot}s}$ due mainly to the parallel conducting layer. After that, the hole mobility increases with temperature, peaking at around 130 K, then starts to decrease with temperature, exhibiting a mobility kink at around 280 K, and then decreases more rapidly until it reaches zero at around 370 K. The kink that appears at around 280 K nearly coincides with the onset temperature of the ionization of deep acceptors. Beyond this kink, the mobility decreases rapidly and the ionized deep acceptor concentration increases with temperature. The maximum measured hole mobility for this $Ge_{1-y}Sn_y$ sample is 638 $\mathrm{cm^2/V{\cdot}s}$, which is much smaller than that of a Ge epitaxial layer grown on a similar n-Si substrate by a factor of 3. This may be partially due to alloy scattering as well as difference in parallel conducting layer scattering.

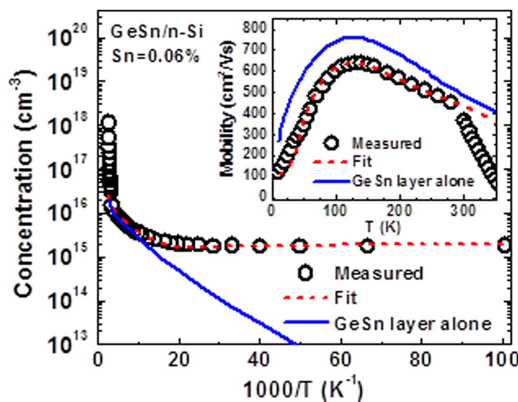

FIG. 2. Apparent measured carrier concentration plotted as a function of inverse temperature for p-$Ge_{0.9994}Sn_{0.0006}/n^-$-Si at temperatures below the conductivity type conversion. The dashed line (red) is a theoretical curve fit to the experimental data generated using a two conducting layer model with both shallow and deep acceptors. The solid line (blue) is the estimated carrier concentrations of the p-$Ge_{0.9994}Sn_{0.0006}$ epitaxial layer alone as a function of inverse temperature. The inset shows the apparent mobilities along with a theoretical fitting curve (dashed line) and the mobilities of the epitaxial layer alone (solid blue line) plotted as a function of temperature.

The mobility fitting curve is shown in the inset of Fig. 2 as a dashed curve (red). It is found to have a $\sim T^{0.56}$ dependence at low temperatures and a $\sim T^{-2.0}$ dependence at high temperatures up to around 280 K. It is believed that the deviation from the typical temperature dependent ionized impurity scattering ($\propto T^{3/2}$) and phonon scattering ($\propto T^{-3/2}$)[29] is due mainly to alloy scattering as well as carrier scattering near the $Ge_{1-y}Sn_y$ and Si interface. A more detailed description of the alloy scattering on mobility behavior can be found in Ref. 13.

In order to extract the electrical properties of the $Ge_{1-y}Sn_y$ layer alone from the measured TDH data, a two conducting layer model was applied. As shown in Fig. 1, for the temperatures below the carrier concentration singularity, only carriers in the epitaxial and parallel conducting layers are dominant, whereas for the temperatures above the singularity, intrinsic carriers from both the $Ge_{1-y}Sn_y$ and Si layers become dominant. The relevant relationships for a two-layer analysis for the low temperature region are[25,30]

$$p = \frac{(\mu_1 p_1 + \mu_2 p_2)^2}{\mu_1^2 p_1 + \mu_2^2 p_2} \tag{1}$$

and

$$\mu = \frac{\mu_1^2 p_1 + \mu_2^2 p_2}{\mu_1 p_1 + \mu_2 p_2}, \tag{2}$$

where p is the measured Hall concentration, μ is the measured Hall mobility, μ_1 and μ_2 are the mobilities, and p_1 and p_2 are the carrier concentrations of the p-$Ge_{1-y}Sn_y$ and p-parallel conducting layers, respectively. The measured sheet hole concentration p is given by $p = r_H/eR_H$. Here, the Hall factor, r_H, is defined as the ratio of the Hall mobility and the drift mobility, and for this analysis, the values for both the p-$Ge_{1-y}Sn_y$ and the parallel conducting layer have been set to unity.

As shown in Fig. 1(b), the hole concentration p_1 in the GeSn layer consists of a shallow acceptor and a deep acceptor compensated by a donor concentration and is given by the charge balance equation[31]

$$p_1 = \frac{N_{A1}}{1 + \dfrac{p_1}{\Phi(E_1, T)}} + \frac{N_{A2}}{1 + \dfrac{p_1}{\Phi(E_2, T)}} - N_D, \tag{3}$$

where N_{A1} (N_{A2}) is the shallow (deep) acceptor concentration, E_1 (E_2) is the ionization energy of the shallow (deep) acceptor level, N_D is the total donor concentration, and $\Phi(E,T) = (g_1/g_0)\, N'_V\, T^{3/2}\, \exp(-E/kT)$. Here, g_0 is the

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degeneracy of the unoccupied acceptor state (assume $g_0 = 4$), g_1 is the degeneracy of the occupied state (assume $g_1 = 1$), and N'_V is the effective density of states of Ge ($N'_V \approx 9.6 \times 10^{14}\,\mathrm{cm}^{-3}$ for $m^* = 0.33m_0$) in the valence band at 1 K, assuming that the effective density of states of $Ge_{0.9994}\,Sn_{0.0006}$ is not much different from that of Ge.

For the Hall mobility, the Mattheissen's rule is used and is given by

$$\frac{1}{\mu_i} = \frac{1}{\mu_I} + \frac{1}{\mu_L}, \tag{4}$$

where μ_i is the effective mobility of the GeSn layer, μ_I is the mobility due mainly to ionized impurity scattering, which is dominant at low temperatures, and μ_L is the mobility due mainly to phonon scattering, which is dominant at high temperatures. The temperature dependence of μ_I and μ_L was determined from a simultaneous parametric fit of p and μ given by Eqs. (1) and (2) to the measured carrier and mobility data. N_D was determined from the same simultaneous fit of p and μ to the measured carrier and mobility data. N_D is used as a free parameter only in Eq. (3). In the Mattheissen's rule, a low temperature region mobility of $AT^{0.56}$ and a high temperature region mobility of $BT^{-2.0}$ were used with A and B as proportionality factors used also as free parameters in the fitting.

A parametric fit of Eqs. (1)–(4) to the measured Hall carrier concentrations and mobilities has been made for the $Ge_{0.9994}Sn_{0.0006}$ as shown in Fig. 2 as dashed lines (red). For plotting purposes, the volume carrier concentrations of both the epitaxial and the parallel conducting layers were normalized by dividing both sheet carriers with the thickness of the epitaxial layer of 800 nm. The agreement between the data and the fit is reasonably good at lower temperatures, but the fit begins to diverge from the data as the temperature approaches the zero Hall coefficient point where carrier concentrations artificially increase rapidly near the singularity point. Also, the carrier concentrations and mobilities of the $Ge_{0.9994}Sn_{0.0006}$ layer alone are plotted as solid lines (blue) in Fig. 2 and inset of Fig. 2 as a function of inverse temperature and temperature, respectively. The results indicate that the carrier concentrations and mobilities of the $Ge_{0.9994}\,Sn_{0.0006}$ layer alone are clearly affected by those of the parallel conducting layer. The true 300 K Hall mobility of the epitaxial layer is significantly higher (487 vs. 364 $\mathrm{cm}^2/\mathrm{V\cdot s}$) than the measured mobility. It is believed that the difference in mobilities is mainly due to the carrier scattering near the parallel conducting layer. The resulting fitting parameters obtained for the $Ge_{1-y}Sn_y$ ($y = 0.06\%$) layer are: $N_{A1} = 9.3 \times 10^{16}\,\mathrm{cm}^{-3}$, $E_1 = 7.5\,\mathrm{meV}$, $N_{A2} = 9.0 \times 10^{16}\,\mathrm{cm}^{-3}$, $E_2 = 140\,\mathrm{meV}$, and $N_D = 8.8 \times 10^{16}\,\mathrm{cm}^{-3}$. At present, the exact sources of the shallow (7.5 meV) and deeper (140 meV) acceptors are unknown. The activation energy of 7.5 meV obtained for a shallow acceptor is close to the accepted boron acceptor energy level of 10 meV at a very low doping level. However, the SIMS measurement results showed no detectable boron impurities (within the detection limit of about mid $10^{15}\,\mathrm{cm}^{-3}$) in the sample. Thus, it needs further investigation to find the sources of acceptors.

In summary, the electrical properties of unintentionally doped p-$Ge_{1-y}Sn_y$ ($y = 0.06\%$) grown on Si substrate by UHVCVD have been investigated as a function of temperature. The temperature-dependent Hall-effect measurements show that there exists a p-type degenerate parallel conducting layer in $Ge_{1-y}Sn_y$/n-Si, which affects significantly the electrical properties of the $Ge_{1-y}Sn_y$ layer. In addition to a shallow acceptor of 7.5 meV (possibly boron), unknown deeper acceptor (140 meV) was also observed in the $Ge_{1-y}Sn_y$ layer. Also, a conductivity type conversion from p to n was observed at around 370 K for this sample. This type-conversion temperature is low enough that it may affect the properties of electronic and optoelectronic devices and their operations above room temperature. The carrier concentration and mobility of the $Ge_{1-y}Sn_y$ layer alone were extracted using a two conducting-layer model, and they are $1.39 \times 10^{16}\,\mathrm{cm}^{-3}$ and 487 $\mathrm{cm}^2/\mathrm{V\cdot s}$ at room temperature, respectively. This study should prove to be useful for the development of direct bandgap $Ge_{1-y}Sn_y$ devices grown on Si, which may eventually lead to the electrically injected light emitting diodes and laser diodes.

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