A 40-GHz Load Modulated Balanced Power Amplifier using Unequal Power Splitter and Phase Compensation Network in 45-nm SOI CMOS

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***Abstract*—In this work, a ten-way power-combined power amplifier is designed using a load modulated balanced amplifier (LMBA)-based architecture. To provide the required magnitude and phase controls between the main and control-signal paths of the LMBA, an unequal power splitter and a phase compensation network are proposed. As proof of concept, the designed power amplifier is implemented in a 45-nm SOI CMOS process. At 40 GHz, it delivers a 25.1 dBm P_{sat} with a peak power-added efficiency (PAE) of 27.9%. At 6-dB power back-off level, it achieves 1.39 times drain efficiency enhancement over an ideal Class-B power amplifier. Using a 200-MHz single-carrier 64-QAM signal, the designed amplifier delivers an average output power of 16.5 dBm with a PAE of 13.1% at an EVM_{rms} of -23.9 dB and ACPR of -25.3 dBc. The die size, including all testing pads, is only 1.92 mm². To the best of the authors' knowledge, compared with the other recently published silicon-based LMBAs, this design achieves the highest P_{sat}.**

***Index Terms* — Doherty amplifier, load-modulated balanced amplifier (LMBA), millimeter-wave (mm-wave) power amplifier, power back-off capability, radio-frequency integrated circuits (RFIC), silicon-on-insulator (SOI).**

I. Introduction

Advanced digital-modulation schemes, such as quadrature amplitude modulation (QAM), have been widely used for many modern wireless systems, ranging from Wi-Fi and Internet-of-Things (IoTs) [1]-[5] to the emerging millimetre-wave (mm-wave) network [6]-[16]. Although employing such complex modulation schemes could significantly enhance spectrum efficiency, it results in an increased design complexity for power amplifiers (PAs) due to the relatively large peak-to-average power ratio (PAPR) of signal. To support a high-order QAM signal, such as 64-QAM, the PA must have a reasonably good linearity, which is almost impossible to be obtained when it operates at the saturated output power level. To satisfy a required linearity specification, one common practice is to operate the PA at its power back-off (PBO) levels with a deteriorated efficiency. Therefore, how to enhance the efficiency of a PA at PBO levels becomes a pressing issue for both academia and industry. Moreover, the design considerations in practice consist of not only linearity, output power and power-added efficiency (PAE), but also impedance matching, stability, and footprint. To solve all these issues together, significant efforts on silicon-based PA design have been made in the past decades and several breakthroughs have been achieved. As far as PA design with enhanced efficiency at PBO levels is concerned, most of the state-of-the-art designs utilize the two classical architectures, namely Doherty and Chireix (also known as Outphasing) that both were originally invented in 1930s [17]-[18]. It would be obvious to ask if there is any alternative architecture that could also be potentially used to enhance efficiency.

Recently, an interesting type of architecture was presented in the literature, namely load modulated balanced amplifier (LMBA). The concept was revealed in [19], and then further analysed in [20]. The LMBA-based design has three distinguished features comparing with Doherty- and Chireix-based designs. Firstly, it utilizes a balanced amplifier (BA) structure. Thus, excellent input and output impedance matching across a wide bandwidth can be simply obtained, which is very useful for phased-array related applications. Secondly, as a quadrature coupler is used as the output power-combining network, it inherently offers a 3-way power combining that leads to an increased output power. The load-modulation network is inherently embedded into the quadrature coupler used at the output. Finally, as demonstrated in [19]-[29], this approach can support PA design with enhanced efficiency at PBO levels. However, most of the LMBA-based design examples found in the literature so far are implemented in PCB technology with discrete transistors, and using this concept for silicon-based mm-wave PA design has only been verified to some extent [28]-[29].

Design of a fully integrated LMBA in silicon-based technology is facing some major challenges. First and foremost, silicon devices have limited capability to generate high output power, comparing with their counterparts in compound semiconductor [30]. Therefore, output power combining is usually required to achieve a relatively high output power. However, on-chip passive components are inherently bulky and lossy, which has an adverse impact on overall performance of the PA, especially output power, and efficiency. Because of these reasons, the designs presented in [28]-[29] have limited

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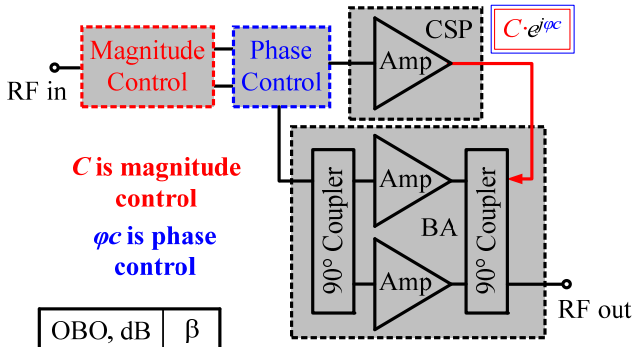


OBO, dB	β
3.5	0.5
4.8	0.4
6.7	0.3
9.5	0.2

Output power back-off (OBO): $10 \log \frac{(1+\beta)^2}{(2\beta)^2}$

Controlled signal path parameter: $\alpha = \frac{(1-\beta)^2}{(2\beta)^2}$

Fig. 1. Simplified block diagram of the proposed PA using LMBA-based architecture. Note: The detailed theoretical analysis can be found in [19]-[20].

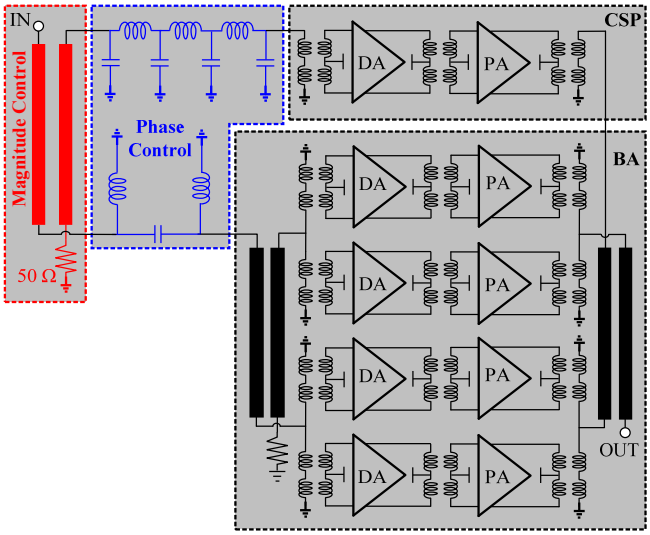


Fig. 2. Simplified circuit schematic of the PA shown in Fig. 1.

output power of less than 23 dBm. In addition, how to accurately control the magnitude and phase relations between the control-signal path (CSP) and the main BA path brings another layer of complexity to the design. Any magnitude or phase misalignment between these two paths could severely affect efficiency enhancement at PBO levels. Regarding magnitude control, adaptive biasing technique along with an equal power splitter is a commonly used approach, which has been verified in [28]-[29]. In this work, an alternative approach is presented. As the BA and CSP amplifier should be biased in different operations, an unequal power splitter is used. Moreover, regarding phase control, a transmission-line (TL)-like phase shifter is used in [28], and a digitally controlled vector-summing phase shifter is used in [29]. Both designs result in a relatively large die area, which ideally needs to be minimized. To address this concern, a novel phase compensation network will be presented in this work.

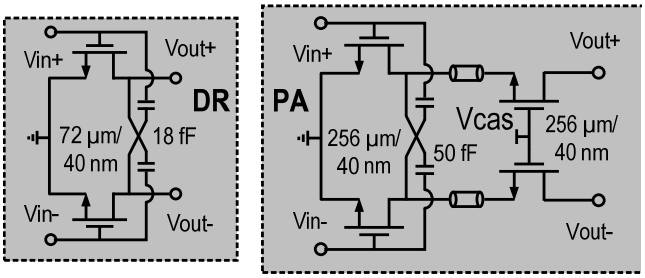
The rest of this paper is organized in the following way. In Section II, the detailed design analysis and considerations for each building block used for the designed LMBA will be provided. The measurement results will be given in Section III and finally the conclusion will be drawn in Section IV.

II. Design of LMBA using Unequal Power Splitter and Phase Compensation Network

A. Overview of the Proposed Architecture

The block diagram of the proposed LMBA is shown in Fig. 1. As can be seen, there are four major parts in the presented architecture: BA, CSP, Magnitude Control, and Phase Control. The operation of a LMBA is briefly given here. To achieve efficiency enhancement at PBO levels, the status of the power cells in the CSP need to be carefully controlled. When the input power is relatively small, the power cells in the CSP are turned off. Therefore, a relatively large impedance is presented at the output port of the BA. As a result, the BA will rapidly reach its voltage saturation. Once the input power becomes large enough, (i.e., reaches the designed PBO level), the power cells in the CSP are turned on and start injecting a current into the coupler. Due to the impedance characteristics of a coupler, if specific magnitude and phase conditions can be satisfied by the injected current, the load impedance of the LMBA will be "modulated" to an optimal impedance, which results in an output power expansion as well as efficiency enhancement at PBO level of the overall LMBA.

To satisfy the specific magnitude and phase conditions, so that the required load-modulation mechanism could be enabled, the injected signal $C \cdot e^{j\varphi c}$ in terms of magnitude and phase differences between the CSP and BA paths should be carefully controlled. In this work, a quadrature coupler with an unequal power ratio is proposed for magnitude control that can achieve an optimized value for C. Meanwhile, to obtain an appropriate value for φ_c, a phase compensation network is proposed for phase control, which offers design flexibility for layout. Furthermore, the value of modulation parameter β must also be carefully determined, according to different output PBO requirements. A summary of the required values of β for some typical output PBO levels is also given in Fig. 1. In this design, a 4-dB output PBO is chosen to be the target, and thus $\beta = 0.5$ [20]. It should be noted that the detailed analysis for a generic LMBA design has been presented in [19]-[20]. In this work, therefore, the primary focus is given to the detailed implementation of silicon based LMBA. For the in-depth theoretical analysis, the reader could refer to the original works presented in [19]-[20]. It should be noted that the 4-dB PBO is selected mainly for the sake of design simplicity. It requires the output impedance transformation ratio to be approximately 2, which could be simply achieved using a transformer-based balun. Moreover, the technical discussion related to the BA design will be limited to a minimum in this work, as design considerations for mm-wave BA can be found in [31]-[33]. Instead, more insight of LMBA design will be explored, especially the design choice for magnitude and phase control will be discussed in detail.



Summarized load-pull results

2-way combined power cell	Ropt	Rpae	Max Pout	Max PAE
P3dB	9.1 + j8.5 or 17 Ω // 219 fF	9.4 + j13 or 27 Ω // 204 fF	21.8 dBm	51.3%
P1dB	9.4 + j13 or 27 Ω // 204 fF	6.3 + j17.9 or 57 Ω // 198 fF	20 dBm	50.8%

Fig. 3. Simplified schematic of the designed differential power cell for CSP and BA as well as the summarised load-pull results.

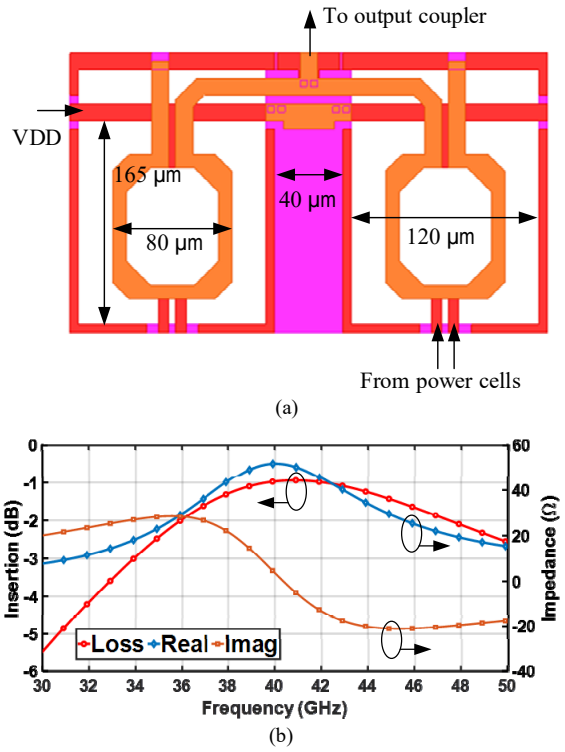


Fig. 4. The 4-in-1 balun used in output power-combining network, (a) top-view of the EM structure, and (b) EM simulated results.

To implement the block diagram shown in Fig. 1, the simplified circuit schematic of the designed LMBA is given in Fig. 2. As can be seen, a distributed-element-based quadrature coupler is used as a power splitter at the input of the designed LMBA that has an unequal power-splitting ratio. Followed by this input power splitter, a lumped-element-based network is used for the phase control network. The signal through the lowpass filter (LPF) path is fed into the CSP, while the signal through the highpass filter (HPF) path is connected to the BA path. Similar to the conventional BA design, 3-dB quadrature couplers are required. The widths of the metal strips used for input and output quadrature couplers are slightly different. A wider metal line is used for the output quadrature coupler to minimize insertion loss. Moreover, the designed BA has two paths. To achieve a relatively high output power, each path consists of a 4-way (2-way in differential) power-combined power cell. Each power cell has a drive amplifier (DA) to boost the gain and the transform-based network is extensively used for input/output and inter-stage impedance matching.

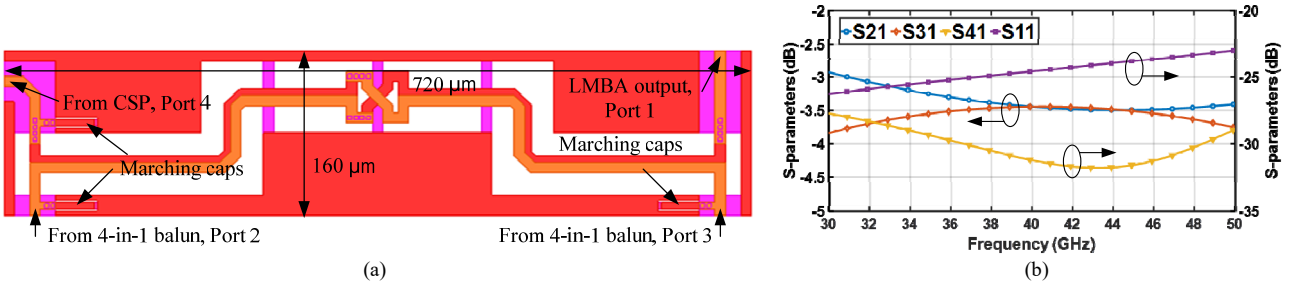
B. Design Considerations in Differential Power Cells

It is similar to the other power-combined PA design; power cell plays an extremely important role. The transistor-level schematic of the differential power cell as well as the summarized load-pull simulation results are given in Fig. 3. As can be seen, the power cell designed in the BA has two stages, namely power stage (PA), and driver stage (DR). The DR is designed with a common-source (CS) configuration, which is operated under a 1-V supply voltage. To further boost the output power, a cascode configuration with a 2-V supply voltage is used for the PA. Moreover, capacitive neutralization is used for both the DR and PA to achieve a good stability and a relatively high-power gain. The same supply voltage arrangements are also used for the power cells in the CSP. On the other hand, a 0.23-V gate bias is used for both the DR and PA in the BA, but only a 0.1-V gate bias is used in the CSP. In such a way, it is ensured that the power cells in the CSP operates in Class C.

As the targeted goal of this design is to achieve an output power of more than 25 dBm for the LMBA, the required output power of the power cell used for the BA should be around 22 dBm. Taking into consideration of the insertion loss from passive components (1.5 dB is assumed) as well as leaving sufficient design margin, an output power of 20 dBm is determined to be the design target for a differential power cell used for the BA. By running load-pull simulations at 40 GHz, it has been found that the optimal impedance is 9.4+j13 and the impedance for maximum PAE is 6.3+j17.9. Based on the design theory provided in [20], the required impedance for pre-matching needs to be approximately 57 Ω. It means that the output impedance needs to be modulated from 57 Ω to 27 Ω in this design. A transformer-based balun is ideally suitable for this requirement, as it could satisfy the impedance transformation ratio and pre-matching conditions with a miniaturized footprint. Once the design for the output stage of the power cell is completed, a DR also needs to be carefully designed to ensure it could provide sufficient output power to drive the PA. Finally, the differential power cell used for CSP amplifier is designed in a similar way.

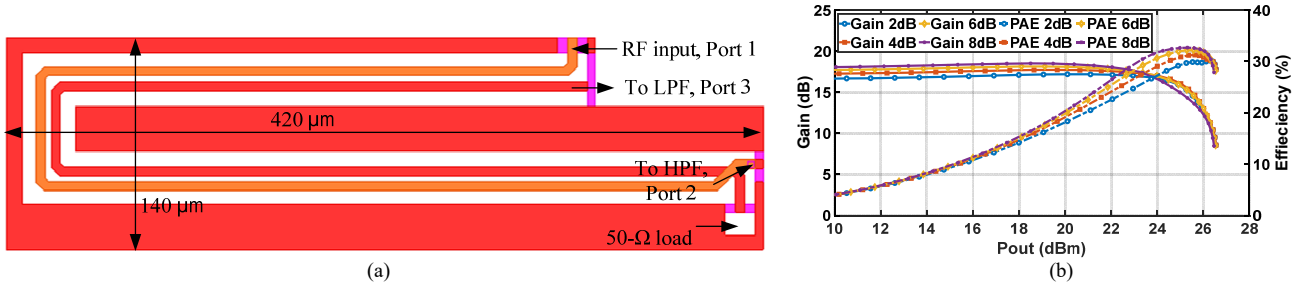
C. Design Considerations of Power-Combining Network

The output power-combining network plays one of the most significant roles for the designed LMBA, which consists of two 4-in-1 transformers-based baluns and an output quadrature coupler. The top-view of their EM structures are shown in Figs. 4(a) and 5(a), respectively. As can be seen in Fig. 4(a), the physical dimensions of a 4-in-1 balun is given, and it is formed by connecting two transformer-based baluns in parallel. To



(a) (b)

Fig. 5. The quadrature coupler used in output power-combining network, (a) top-view of the EM structure, and (b) EM simulated S-parameters.



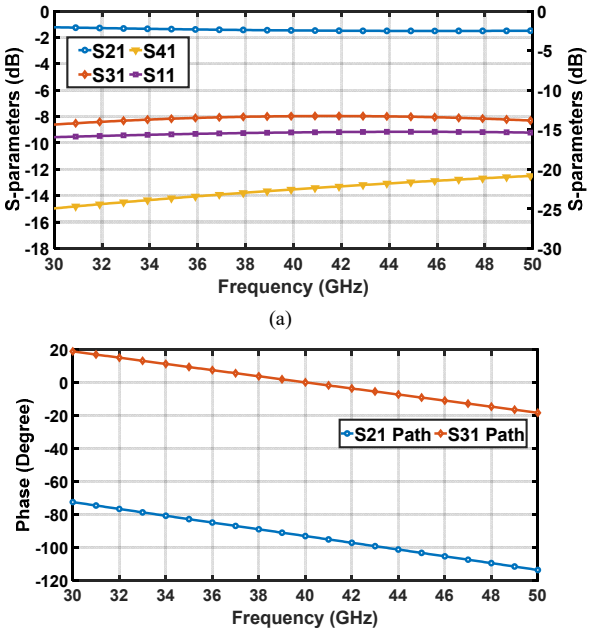
(a) (b)

Fig. 6. Input power splitter, (a) top-view of the EM structure, (b) impact on large-signal CW performance due to different power-splitting ratio.

minimize the insertion loss of the balun, the width of the metal line is selected to be 8 μm. At 40 GHz, the EM simulation results have shown that the 4-in-1 balun has an impedance of 56 Ω, and its insertion loss is less than 1 dB, which can be found in Fig. 4(b). As shown in Fig. 5(a), a broadside-coupled structure is used for the designed output coupler, so that a relatively strong coupling could be maintained. The two most critical design parameters here are insertion loss (shown as S_{31} and S_{21}) and isolation (shown as S_{41}). Both have an adverse impact on the output power as well as efficiency. Therefore, the performance of this quadrature coupler also needs to be extensively optimized in EM simulation. As shown in Fig. 5(b), the designed coupler has an insertion loss of less than 0.5 dB and an isolation of better than 30 dB.

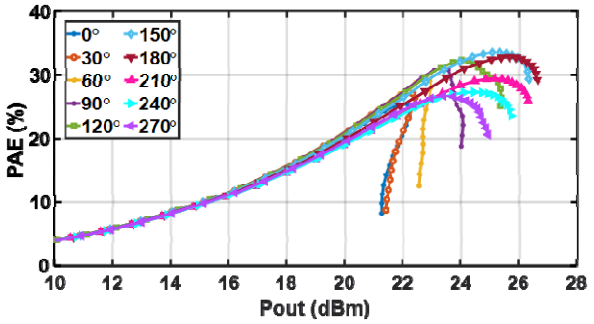
D. Design Considerations in Magnitude and Phase Controls

In Fig. 6(a), the EM structure used for magnitude control is presented, which acts like an unequal power splitter. Unlike the 3-dB quadrature coupler designed for output power-combining network that usually requires a relatively strong coupling factor between two metal lines, this design is implemented by an edge-coupled quadrature coupler and the unused isolation port is terminated by an on-chip 50-Ω load. To ensure the CSP amplifier will not be turned on until sufficient input power is provided to this path, the power-splitting ratio needs to be carefully determined. A case study was conducted by simulating the large-signal performance of the designed LMBA with different power-splitting ratios, and the simulation results are given in Fig. 6(b). As illustrated, an 8-dB power splitting ratio gives the best overall performance. It should be noted that an ideal quadrature coupler is used here, which allows the output power at both THRU and COUP ports to be tuned. Moreover, the 2/4/6/8-dB power ratio used in this study is simply defined as the magnitude difference between these two ports in dB rather than the coupling factor of a quadrature coupler. To obtain this ratio, the gap between two metal lines needs to be adjusted through multiple design iterations. The EM simulation results of the input power splitter are presented in Fig. 7. As shown, the simulated isolation (shown as S_{41}) is more than 20 dB and the insertion losses for the THRU (shown as S_{31}) and COUP (shown as S_{21}) ports are 1.9 dB and 8 dB at 40 GHz, respectively. In addition, a reasonable phase difference between Port 2 and Port 3 is also achieved.

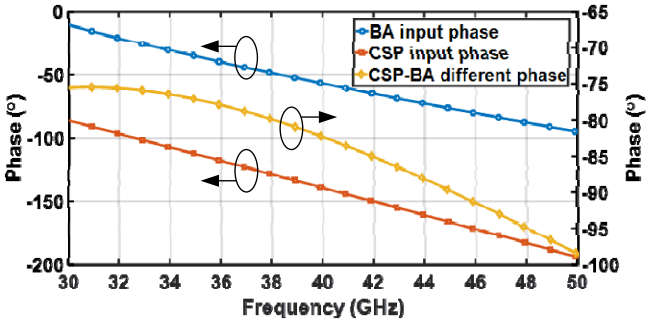


(a) (b)

Fig. 7. EM simulation results of the input power splitter, (a) S-parameters, and (b) phase responses. Note: the THRU port is connected to BA path and COUP port is connected to CSP path. The phase difference between these two ports is 92°at 40 GHz.

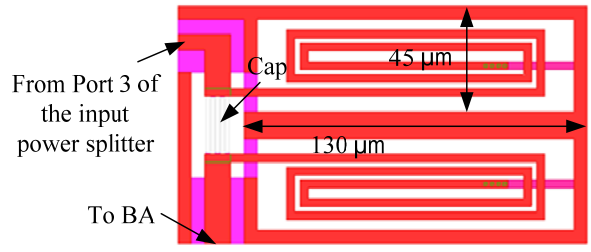


(a)

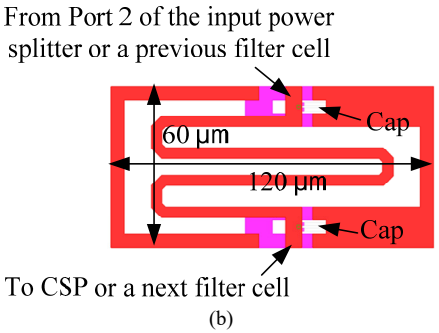


(b)

Fig. 8. Case study – impact on PAE due to different phase relation between CSP and BA path, (a) simulated PAE and Pout with different phase relation, and (b) EM simulated phase responses between CSP and BA path.



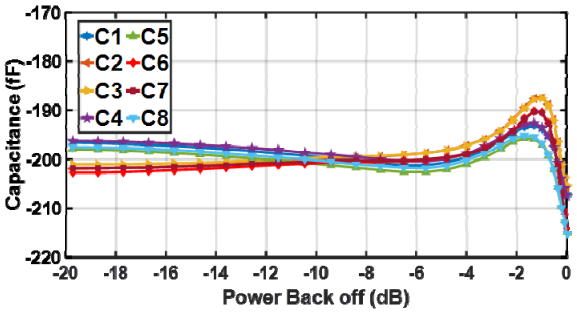
(a)



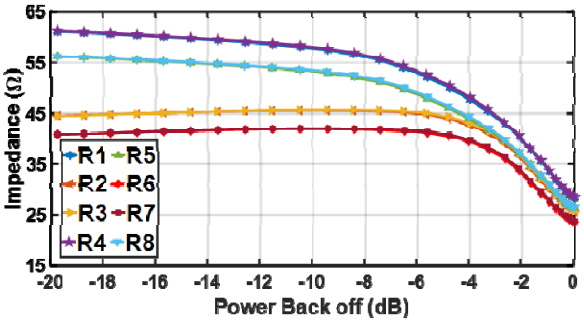
(b)

Fig. 9. Phase compensated network, (a) top-view of the L-C-L-based high-pass filter network (L is 450 pH and C is 150 fF, and (b) top-view of the single-cell C-L-C-based lowpass filter cell (L is 100 pH and C is 20 fF). Note: the width of the metal strip is 3 µm.

Moreover, as previously mentioned, the phase relationship between CSP and BA paths is also critical. To determine the required phase relationship between the CSP and BA paths,



(a)



(b)

Fig. 10. Simulated load trajectories of the designed power cells, (a) capacitance part, and (b) resistance part.

parametric studies are conducted as well. An ideal phase shifter is inserted between Port 3 (COUP port) of the input power splitter and the CSP path. The simulation results are presented in Fig. 8. It can be found that the designed LMBA will achieve an optimized performance if the phase shifter could provide a 150°-180° phase delay. Since the COUP port (connected to CSP) of the input power splitter has a 90° leading phase, comparing with the signal at THRU port (connected to BA), the signal through the phase control network needs to generate a 60°-90° lagging phase at the input of CSP, comparing with the signal at the input of the BA. Since implementing a 90° delay line using a TL is relatively long at 40 GHz [26], a phase compensation network is used to synthesize the phase relationship between these two paths, which consists of an LPF and an HPF. To minimize the footprint without compromising the required phase condition, the lumped-element-based approach is used. The illustration of how the filters should be connected with the input power splitter is shown in Fig. 6(a), the THRU and the COUP ports are connected to a HPF and a LPF for phase adjustment, respectively.

As far as the filters design is concerned, a series-connected capacitor along with two shunt-connected inductors are used to implement the HPF and it is placed at the BA path as it introduces a positive phase shift. Meanwhile, an LPF that generates a negative phase shift is used at the CSP. The LPF is implemented by cascading three LPF cells that consist of a series-connected inductor with two shunt-connected capacitors. The EM structures of the HPF and the filter cell used for LPF are shown in Fig. 9. At 40 GHz, the simulation results indicate that an 82° lagging phase between the CSP and BA paths is obtained. To verify this result is meaningful for LMBA design,

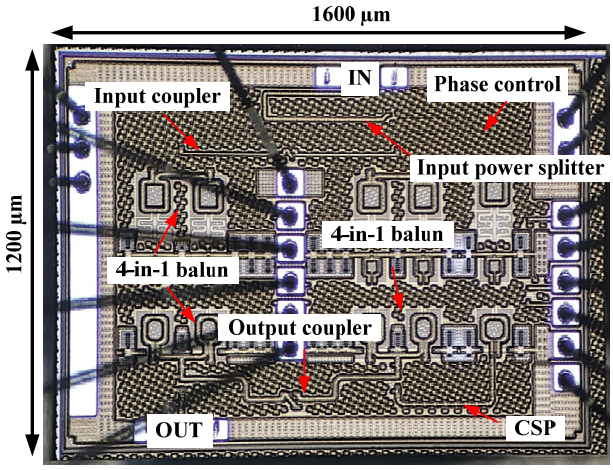


Fig. 11. Die microphotograph of the designed LMBA.

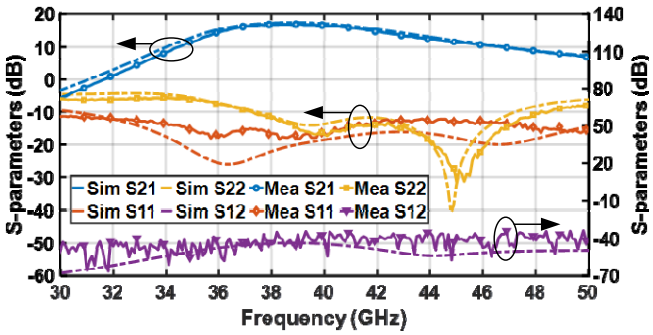


Fig. 12. Measured small-signal S-parameters of the designed LMBA.

the impedance variations of all power cells in terms of capacitance and resistance parts are simulated, and the results are given in Fig. 10. As can be seen, the impedances of all power cells are shifted to around 27 Ω at saturated output power level, which is expected. It should be noted that as can be observed in Fig. 10, there are mismatches in terms of impedance for different power cells. This is mainly caused by the non-idealities of the output coupler, such as the magnitude and phase errors between THRU and COUP ports. In addition, the limited isolation of the coupler also has an adverse impact on impedance mismatch.

III. Measurement Results

To evaluate the performance of the presented PA, it is fabricated in a 45-nm SOI CMOS process. The die microphotograph is given in Fig. 11. Including the testing pads, the die size is only 1.2 × 1.6 mm^2.

A. Small-Signal Performance

To evaluate the presented LMBA's small-signal performance, a test was designed. The pads are connected to a PCB board. A vector network analyzer N5290A from Keysight was used for On-wafer G-S-G probing. The necessary calibration was made by using the short-load-open-thru (SLOT). It moved the reference plane from the connectors of the equipment to the tips of the RF probes. The measured S-parameters are plotted in Fig. 12. As illustrated, a good agreement between the measured and EM simulated results is obtained. At 40 GHz, the measured small-signal gain is 16.8 dB. Because a BA-like architecture is used, excellent input and output impedance matching, and reverse isolation are obtained, which indicates good stability.

B. Large-Signal Performance with Continuous-Wave Signal

To further evaluate the performance of the presented LMBA, a continuous-wave (CW) large signal was also measured. The setup used for this measurement is given in Fig. 13. As can also be seen in Fig.13, the Keysight E8257D and a driver amplifier are utilized to provide the CW input signal required. Furthermore, two Keysight U8487A USB Thermocouple Power Sensors along with a Keysight 87301D coaxial directional coupler and Keysight BenchVue software (used as a power meter) are used to monitor the power levels at the input and output of the designed LMBA.

The saturated output power (namely P_{sat}), P1dB, PAE at P_{sat}, and PAE at 6-dB PBO level are all given in Fig. 14. As can be seen, the designed LMBA achieves a P_{sat} of 25.1 dBm, and peak PAE (namely PAE_{max}) of 27.9% at 40 GHz. At 6-dB PBO from P_{sat}, the PA achieves a PAE of 19%. Thus, it indicates 1.39 times drain efficiency (DE) enhancement at 6-dB PBO with respect to an ideal Class-B amplifier.

C. Large-Signal Performance with Modulated Signal

The third part of our measurements is about large-signal performance with the modulated signal. A single-carrier 64-QAM signal with a 200-MHz bandwidth is used to evaluate the performance of this design in terms of error vector magnitude (EVM) and the adjacent channel power ratio (ACPR). It should be noted that a 200-MHz is used mainly due to hardware limitations.

The measurement setup is shown in Fig. 15. As shown, the modulated baseband signal is generated by using Keysight M8190A arbitrary waveform generator (AWG) along with Signal Studio software and then this signal is up-converted to 40 GHz with Keysight PSG E8267D microwave vector signal generator. After the modulated signal is amplified by the designed LMBA, Keysight PXA N9030B signal analyzer along with 89600 vector signal analyser (VSA) software are used to demodulate the amplified signal. For an accurate power measurement, a pair of Keysight U8487A power sensors along with 87301D directional couplers are used again at both input and output ports. The measured EVM and ACPR results are given in Fig. 16. Without any digital pre-distortion (DPD), this design achieves an average power (namely P_{avg}) of 16.5 dBm with an average PAE (namely PAE_{avg}) of 13.1% at an EVM_{rms} of -23.9 dB and ACPR of -25.3 dBc.

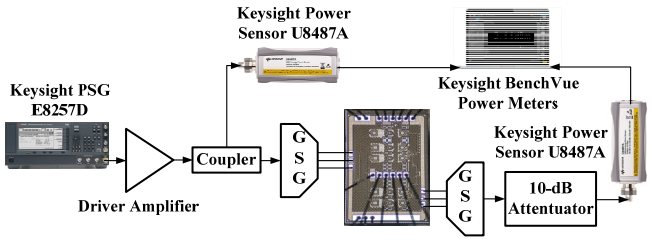


Fig. 13. Test bench used for large-signal CW characterization.

TABLE I

PERFORMANCE SUMMARY OF THE DESIGNED LMBA WITH THE OTHER STATE-OF-THE-ART DESIGNS OPERATING AT 30 GHZ AND ABOVE.

	LMBA			Doherty		Linear	
	This work	[28] Chappidi IMS 20	[29] Qunaj ISSCC 21	[7] Huang ISSCC 21	[13] Hu JSSC 19	[11] Vigilante JSSC 18	[9] Chappidi JSSC 17
Tech.	45-nm SOI	65-nm CMOS	28-nm CMOS	45-nm SOI	0.13-µm SiGe	28-nm CMOS	0.13-µm SiGe
Arch.	Unequal power splitter with LPF/HPF network	Equal power splitter with TL phase shifter	Equal power splitter with VS phase shifter	Coupler-based Doherty	Reconfigurable Doherty	Wideband Class AB	Frequency Reconfigurable
VDD (V)	2	1.1	1	2	1.5	0.9	4
Freq. (GHz)	40	33	36	40	37	40	40
Gain (dB)	16.8	10	18	N/A	17.1	20.8	18
P_{sat} (dBm)	25.1	20	22.6	21.8	17.1	15.9	23.6
PAE_{max} (%)	27.9	22.3	32	27.8	22.6	18.4	25
$PAE_{6\text{-dB PBO}}$ (%)	19	16.2*	24.2	19.6	16.6	n/a	n/a
Mod. scheme	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM
Data rate (Gb/s)	1.2[#]	6	18	3	3	1.5	3
EVM_{rms} (dB)	-23.9	-27	-25.1	-25.2	-30.3	-25^	-21.7
P_{avg} (dBm)	16.5	10.6	15.5	12.6	9.5	10.1^	11.7
PAE_{avg} (%)	13.1	12.1	20	15.6	19.2*	5.8^	8.3
Area (mm^2)	1.92	1.47	1.44	2.28	1.76	N/A	1.02

Note: *last stage drain/collector efficiency, **graphical estimation, ^@34 GHz, [#]limited by testing equipment.

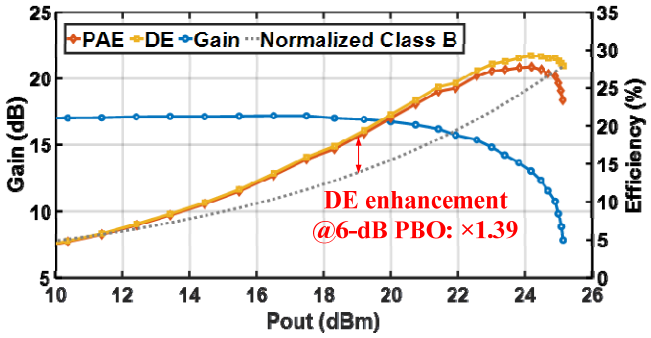


Fig. 14. Measured large-signal CW performance of the designed LMBA. Note: P_{sat} = 25.1 dBm, OP1dB = 21.9 dBm, PAE@OP1dB = 25%, peak PAE = 27.9%, PAE@6-dB PBO = 19%, Peak DE = 29.3%, DE@6-dB PBO = 19.4%.

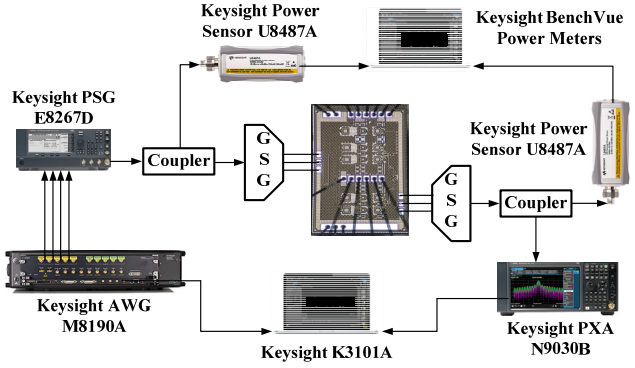


Fig. 15. Test bench used for large-signal modulated-signal characterization.

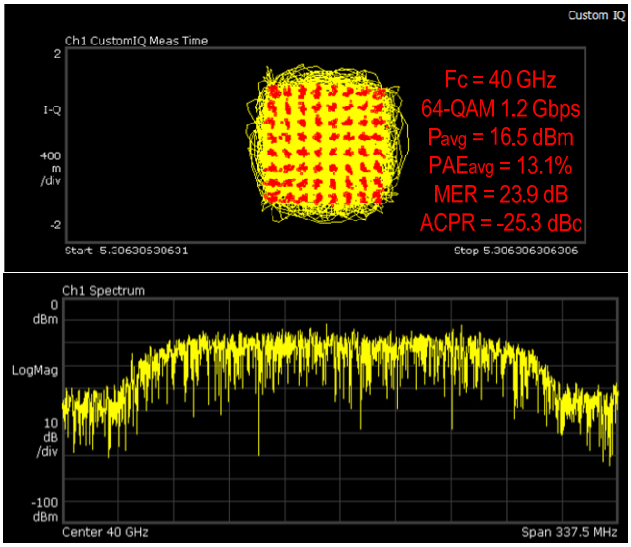


Fig. 16. Measured EVM and ACPR performance with the modulated signal.

D. Comparisons with The Other State-of-the-Art Designs

To further evaluate the presented LMBA, the performance of our design was summarized and compared with some other state-of-the-art designs. Since all the PAs were designed to be used for different applications under different circumstances, it is not possible to provide simple like-for-like comparisons for all of them. However, by summarizing and comparing their performance, useful information can still be collected. Moreover, although the original concept of single- and dual-input LMBAs has been explored by using discrete components

[20]-[27], there are only two works that can be found in the literature, which use an LMBA-based architecture for silicon-based PA design [28]-[29]. Compared with these two designs as well as the other recently published Doherty-like designs, the presented work achieves the highest output power in terms of P_{sat} and P_{avg} with relatively good PAE at both P_{sat} and 6-dB PBO levels. Thus, it demonstrates that the presented LMBA-based architecture is feasible for power-efficient silicon-based PA design.

IV. Conclusions

In this work, a 40-GHz PA is designed using LMBA-based architecture in a 45-nm SOI CMOS technology. The detailed analysis and considerations for each critical building block used in this design are provided. The designed LMBA is operated under a 2-V power supply. At 40 GHz, the P_{sat} is greater than 25.1 dBm and the PAE at P_{sat} and 6-dB PBO levels are 27.9% and 19%, respectively. Furthermore, it can support 64-QAM digital modulation. The measured average power is better than 16.5 dBm to maintain an EVM_{rms} of less than -23.9 dB. Based on the achieved overall performance, it can be concluded that the presented approach is feasible for silicon-based mm-wave PA design with high output power and enhanced efficiency at PBO levels. Therefore, it can be treated as an alternative approach along with the well-known Doherty and Outphasing approaches for energy-efficient PA design.

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