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Design and Implementation of High-Efficiency, Lightweight, System-Friendly Solid-State Circuit Breaker

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DESIGN AND IMPLEMENTATION OF HIGH-EFFICIENCY, LIGHTWEIGHT, SYSTEM-FRIENDLY SOLID-STATE CIRCUIT BREAKER

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ABSTRACT

Direct current (DC) distribution system has shown potential over the alternative current (AC) distribution system in some application scenarios, e.g., electrified transportation, renewable energy, data center, etc. Because of the fast response speed, DC solid-state circuit breaker (SSCB) becomes a promising technology for the future power electronics intensive DC energy system with fault-tolerant capability.

First, a thorough literature survey is performed to review the DC-SSCB technology. The key components for DC-SSCB, including power semiconductors, topologies, energy absorption units, and fault detection circuits, are studied. It is observed that the prior studies mainly focus on the basic interruption capability of the DC-SSCB. There are not so many studies on SSCB's size optimization or system-friendly functions.

Second, an insulated gate bipolar transistor (IGBT) based lightweight SSCB is proposed. With the reduced gate voltage, the proposed SSCB can limit the peak fault current without the bulky and heavy fault current limiting the inductor, which exists in the conventional SSCB circuit. Thus, the specific power density of the SSCB is substantially improved compared with the conventional design. Meanwhile, to understand the impact of different design parameters on the performance of SSCB, an analytical model is built to establish the relationship between SSCB dynamic performance and operating conditions considering the key components and circuit parasitics. Simulation and test results demonstrate the accuracy of the proposed model.

To limit the fault current with the proposed SSCB without a current limiting inductor, power semiconductors need to operate in the active region temporarily. During

this interval, a severe voltage oscillation has been observed experimentally, leading to the DC-SSCB overstress and eventually the failure. A detailed MATLAB/Simulink model is built to understand the mechanism causing the voltage oscillation. Three suppression methods using enhanced gate drive circuitry are proposed and compared. Test results based on a 2kV/1kA SSCB prototype demonstrate the effectiveness of the proposed oscillation mitigation method and the accuracy of the derived model. Meanwhile, when the system fault impedance is close to zero (e.g., high *di/dt*), the influence of the parasitic inductance contributed by interconnection (e.g., bus bar, module package, etc.) cannot be neglected. To study the influence of the bus bar connections on SSCB with high *di/dt*, a Q3D extractor is adopted to extract the parasitic parameters of the SSCB and understand the influence of different bus bar connections. A vertical bus bar is proposed to suppress the side effect and verified by the Q3D extractor and experimental results.

Finally, a system-friendly SSCB is demonstrated. The proposed gate drive enables the SSCB to operate in the current limitation mode for the overcurrent limitation. The current limitation level and limitation time can be tuned by the gate drive. Then, this dissertation provides an all-in-one solution with integrated circuitries as the fault detector, actuator for the semiconductor's operating status regulation, and coordinated control. This allows the developed SSCB to limit system fault current not exceeding short-circuit current rating (SCCR) and also take different responses under different fault cases. The feasibility and the effectiveness of the proposed system-friendly SSCB are validated with experimental results based on a 200V/10A SSCB demonstrator.

DEDICATION

I dedicate my dissertation work to Joy Yang who always supports me during my Ph.D. study.

I also dedicate my dissertation work to Dr. Zheyu Zhang who always provides precious suggestions and help during my Ph.D. study.

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CHAPTER ONE

1 INTRODUCTION

This chapter starts with an introduction to the direct current (DC) fault-tolerant system in emerging DC distribution system applications. Then the significance of the DC circuit breaker (DC-CB) for the DC fault-tolerant system is demonstrated. Meanwhile, the state-of-the-art of different DC-CBs is also discussed and compared in this chapter. After examing the excellent performance of the DC solid-state circuit breaker (DC-SSCB), this chapter demonstrates the profits and challenges of designing a fast, lightweight, and reliable DC-SSCB. Finally, the organization of this research dissertation is presented.

1.1 Application Background

Battle of the currents [1], the war between DC and alternative current (AC), has continued for several hundred years since Thomas Edison and Nikola Tesla advocated DC and AC power, respectively. Compared with DC power, AC power is cheaper and more convenient to generate through the AC generator. With the help of the transformer, AC is also easier to realize voltage transformation. Moreover, because of the nature of AC, the system overcurrent fault can be easily interrupted through the zero-crossing point without any arc. AC is also suitable for high voltage long-distance power transmission. Due to the above reasons, AC won the battle temporarily and dominated the industry and residential power system in the past decades.

However, with the development of power electronics, the DC distribution system has shown some potential to gradually take the place of the AC distribution system in some

application scenarios, e.g., electrified transportation, renewable energy, data center, etc. Compared with the AC distribution system, the DC distribution system is more compatible with renewable energy sources, battery energy storage systems (BESS), electric vehicles, etc. Meanwhile, the DC distribution system is more efficient. Because DC appliances do not need to transform the AC to DC anymore. Last but not least, high-voltage DC (HVDC) is also a better candidate for ultra-long-distance power transmission.

1.1.1 DC distribution system

Research regarding electrified transportation has dominated power electronics in recent years. Electric vehicles, electric ships, and electric aviation are the main parts of electrified transportation. Take electric aviation as an example. Since 2019, the US Department of Energy has announced more than $88 million in funding for electric aviation [2, 3]. Moreover, more and more start-ups focusing on consumer electric aviation are emerging, e.g., Joby Aviation, Lilium, Archer, etc.

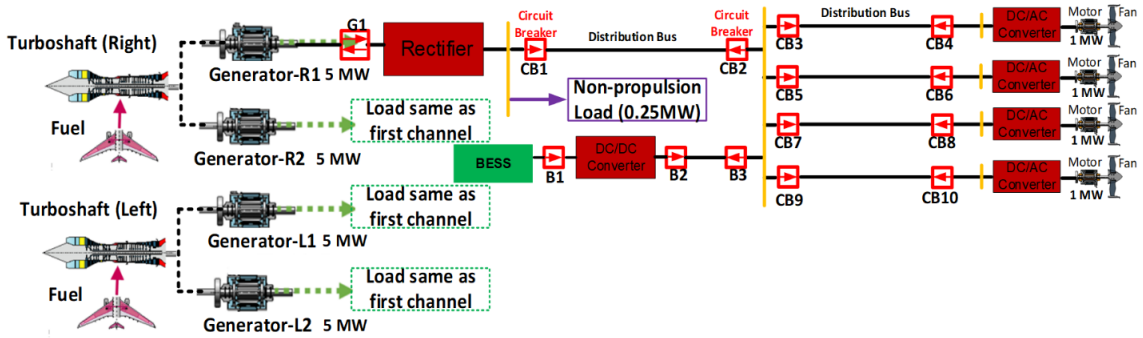


Figure 1. 1: Configuration of the EAP system.

Figure 1. 1 illustrates the configuration of the electrified aircraft propulsion (EAP) system. EAP is a crucial enabler in improving fuel efficiency, emissions, and noise levels in commercial transport aircraft [4-6]. It mainly comprises the generator, motor, power

converter, BESS, and CB. The power rating of the electrical power system to support EAP is in the range of megawatts (MWs) or tens of MWs, which is much higher than the existing power system on commercial more electric aircraft, such as B797 and A380. The weight of the cable is vital to the EAP system. Firstly, the cable for the AC distribution system always has three or four wires; meanwhile, the cable in the DC distribution system only needs two wires. Secondly, with the same root-mean-square (RMS) current, the DC cable can carry $\sqrt{2}$ times power than the AC cable. Last but not least, with the absence of the skin effect and reactive power flow, there is less power loss for the DC cable [7]. Thus, to reduce the total weight of the electric power system, especially the cable weight, the medium voltage direct current (MVDC) system offers a promising option due to its unique advantages compared with the traditional AC system [8]. Accordingly, the DC distribution system is more competitive for electric aviation than the AC distribution system.

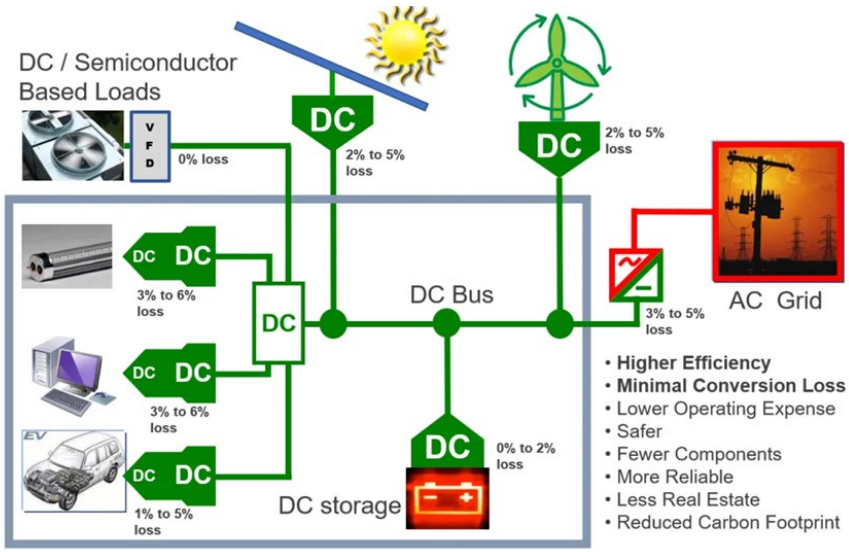


Figure 1. 2: Configuration of the DC distribution system with renewable energy.

Currently, all over the world is facing a challenge to transform from traditional fossil fuels to renewable energy sources. Thanks to the development of power electronics, the power system with high penetration of renewable energy is becoming feasible. Denmark aims to achieve 100% renewable energy electricity generation by 2050 [9]. China aims to reach a combined 1,200GW of solar and wind capacity by 2030 and own 80% of its total energy from non-fossil fuel sources by 2060 [10, 11]. President Biden took bold executive action for the United States to motivate domestic clean energy manufacturing in June 2022 [12]. Biden-Harris administration also announced $425 Million to expand state clean energy programs in August 2022 [13].

Figure 1. 2 illustrates the configuration of the DC distribution system with renewable energy. The shown DC microgrid is composed of photovoltaics (PV), wind energy, BESS, and DC load. Because PV, wind energy, BESS, and DC load can directly connect with the DC bus through DC-DC converters without additional DC-AC or AC-DC converters. Moreover, the DC distribution system can also save the cost of the cable. The DC distribution system is more efficient and inexpensive for the high renewable energy penetration power system than the AC distribution system.

With the coming of Web 3.0, more and more data need to be computed and stored. Accordingly, almost every internet giant joins the competition to develop the next-generation data center [14, 15]. A reliable distribution power system plays an essential role in the uninterruptable operation of the data center. And the next-generation DC distribution system can help the data center power system become more reliable and efficient [16].

1.1.2 Challenges of the DC distribution system

Although the DC distribution system can benefit the development of electrified transportation, renewable energy, and data center power systems, there are still some obstacles to limiting the development of the DC distribution system. The related fast, reliable fault-tolerant-capable system is one of the fundamental challenges, and it is also the research emphasis of this dissertation.

No matter the AC or DC distribution, a reliable fault-tolerant-capable system is quite important to them. The reliable CB is one of the most critical components of the fault-tolerant-capable system. With the help of the AC characteristic, it is not hard for AC-CB to interrupt the fault current during the zero-crossing point. However, there is no zero-crossing point for the DC distribution system, and the DC-CBs must face high voltage and current when they interrupt the high fault current. And the severe arc may occur during the interruption period and negatively influence the system operation and operator life safety. Moreover, the developing power system with a high penetration of power electronics provides more requirements for the fault-tolerant-capable system. The traditional distribution protection system cannot satisfy the new requirements of the modern fault-tolerant-capable system. Accordingly, to fit with the contemporary DC distribution system with high penetration of power electronics, the next-generation DC-CB should have the following challenges [17]:

1. Because the power electronics system is susceptible to the high current value, a DC-CB with a fast response time is of vital significance to interrupt the overcurrent as soon as possible.

2. DC-CB should be sensitive enough to detect the relatively low fault current caused by the interfaced power converter.
3. It is easy to happen a severe arc during the interruption of the DC distribution system with a high current level. Thus, eliminating arc capability is essential for DC-CB.
4. Ride-through capability for healthy parts of the system.
5. In some cases, the DC distribution system can operate on an island or grid-connected mode. Thus, the fault trigger threshold of the DC-CB should be tuned under different DC distribution operation modes.

1.2 DC fault-tolerant-capable system

	MCB	SSCB	HCB
Response time	Tens of ms	<100us	Few ms
Losses	Few watts	Hundreds of watts	Few watts
Weight and volume	Relatively small	Relatively large	Relatively small

Table 1. 1: Comparison among different DC-CB.

As the DC fault-tolerant-capable system's enabler, the DC-CB study can trace back to 1976 [18]. Depending on the operation principle of DC-CB, DC-CB can be categorized into mechanical circuit breaker (MCB), SSCB, and hybrid circuit breaker (HCB). Table 1. 1 illustrates the differences between three different DC-CBs.

1.2.1 Mechanical circuit breaker

MCB is one of the most traditional circuit protection breakers. During regular operation, the mechanical switch contacts help the MCB build up a current flow path, and

the resistance can be as low as 10 μΩ [18]. When the overcurrent is detected, an electric arc will happen when the mechanical switch contacts separate to interrupt the fault. Cooling and lengthening are leveraged to extinguish the produced electric arc. Once the electric arc is extinguished, the dielectric strength starts to rebuild, and MCB isolates the fault. Based on the arc quenching medium and cooling arrangement, the traditional MCB can be categorized into vacuum interrupter, air arc chute CB, sulfur hexafluoride (SF_6) CB, etc. [19].

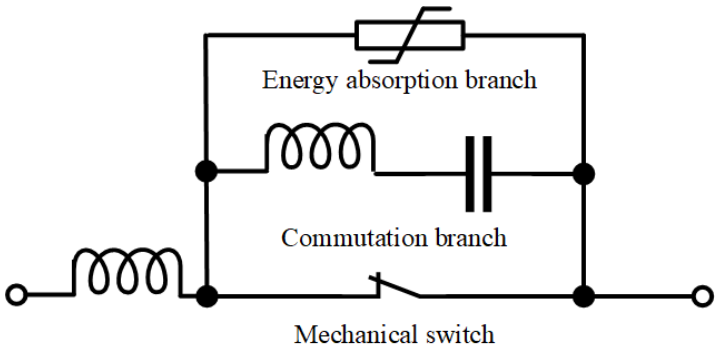


Figure 1. 3: Topology of the passive resonance DC-MCB.

However, the interruption of those traditional MCBs highly relies on the zero-crossing point of the AC distribution system. Accordingly, resonance DC-MCB is proposed to satisfy the requirements of the DC distribution system. Figure 1. 3 shows the typical topology of the passive resonance DC MCB. It mainly comprises a mechanical switch branch, a commutation branch, and an energy absorption branch. During regular operation, the mechanical switch keeps on-state and helps the MCB have a low conduction loss. Once the fault happens, the mechanical switch will be turned off. Following the electric arc, the fault current will commute from the mechanical switch branch to the communication branch. The commutation branch can provide a zero current crossing point

to extinguish the arc. Finally, the current will flow into the energy absorption branch, and the residual system energy will be dissipated.

1.2.2 Solid-state circuit breaker

With the development of power electronics, DC-SSCB has gradually become the research hotspot [20]. Instead of the mechanical switch in DC-MCB, DC-SSCB leverages the power semiconductor (e.g., gate turn-off thyristors (GTOs), integrated gate-commutate thyristors (IGCTs), insulated gate bipolar transistors (IGBTs), etc.) to control the current path on and off. The typical topology of the DC-SSCB is illustrated in Figure 1. 4. It consists of a bidirectional power semiconductor block, an energy absorption branch, and a current-limiting inductor. The bidirectional power semiconductor can be two paralleled IGCTs or two IGBTs in a series connection.

During normal operation, the bidirectional power semiconductor block is conducted, and its conduction loss determines the efficiency of the DC-SSCB. Take IGBT-based DC-SSCB as an example. As shown in Figure 1. 5, IGBT-based DC-SSCB conduction loss is the combination of the IGBT and diode conduction loss. For a 3000V bidirectional IGBT block [21], with a 1000A system current, the equivalent conduction resistance for DC-SSCB is about 4mΩ. When the fault happens, the current-limiting inductor can decrease the increasing ratio of the fault current. Meanwhile, once the fault is detected, the bidirectional semiconductor block will be turned off. Then the current commutes from the power semiconductor to the energy absorption branch. Finally, the energy absorption branch will dissipate the residual system energy and limit the voltage

across the power semiconductor. It is noted that there will not be any electric arc during the turn-off process of the DC-SSCB.

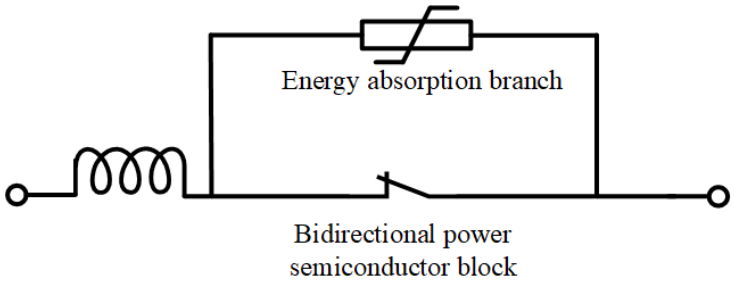


Figure 1. 4: Topology of the typical DC-SSCB.

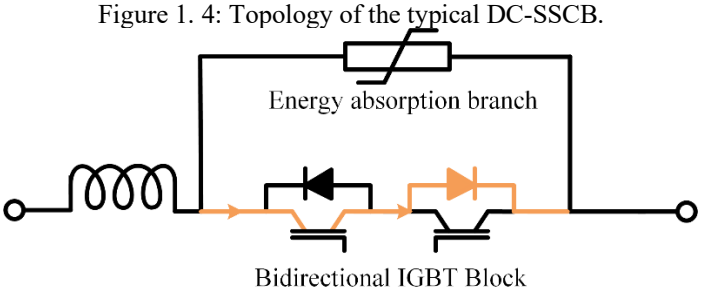


Figure 1. 5: Conduction loop of the IGBT-based DC-SSCB.

1.2.3 Hybrid circuit breaker

HCB is more like the combination of MCB and SSCB. To some extent, it possesses the advantages of MCB and SSCB [22].

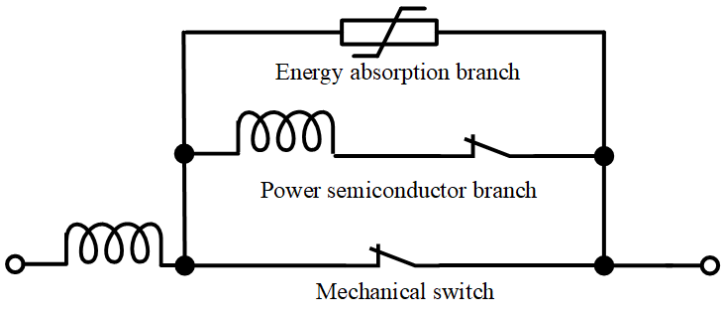


Figure 1. 6: Topology of the typical DC-HCB.

The typical DC-HCB is shown in Figure 1. 6. It mainly consists of a mechanical switch, a power semiconductor branch, and an energy absorption branch. During regular operation, similar to MCB, the mechanical switch keeps on-state and helps the DC-HCB have a low conduction loss. When the fault is detected, the mechanical switch will be turned off, and the fault current will commute from the mechanical switch to the power electronics branch, which can help the mechanical switch extinguish the electric arc. Once the mechanical switch can entirely block the system's DC voltage, the power semiconductor will be turned off, and the current will commute from the power semiconductor branch to the energy absorption branch. Finally, like SSCB, the energy absorption branch will dissipate the residual system energy and limit the voltage across the power semiconductor.

1.2.4 Comparison among different DC-CB technology

Table 1. 1 compares the characteristics of MCB, SSCB, and HCB. Compared with MCB, with the help of power electronics technology, SSCB, and HCB possess a faster response time. However, because HCB still needs to commute the fault current from the mechanical switch to the power semiconductor, the response time of HCB is slower than SSCB. The response time of SSCB can be as low as several microseconds, while the response time of HCB and MCB can be a few milliseconds and tens of milliseconds, respectively.

Thanks to the mechanical switch, the conduction loss of the MCB and HCB is minimal, which makes the efficiency of MCB and HCB can achieve almost 100%. However, the conduction loss of the power semiconductor limits the efficiency of SSCB.

Additionally, SSCB is much more sensitive to high current; thus, it needs a larger current-limiting inductor. Moreover, an additional reliable cooling system is essential for the power semiconductor. Accordingly, with a larger current-limiting inductor and a power electronics cooling system, the size and volume of SSCB are larger than MCB and HCB.

As mentioned in Section 1.1.2, a fast fault-tolerant-capable system is vital for the DC distribution system with a high penetration of power electronics. The fast response time of DC-SSCB fits with the requirement of the DC distribution system with a high penetration of power electronics. Therefore, DC-SSCB is selected as the research object of this dissertation. The proposed DC-SSCB can improve the shortcomings of the traditional DC-SSCB.

1.3 Challenges for DC-SSCB

As mentioned in Section 1.2, although DC-SSCB has a satisfactory response time (as low as several microseconds), it still has some disadvantages that impede its development, e.g., relatively large size and rather large losses. Moreover, the power electronics technology for DC-SSCB is a double-edged sword. On the one hand, it may cause some oscillation issues; on the other, it can endow DC-SSCB with more potential, e.g., tunable fault trigger threshold, tunable response time, advanced fault current detection method, etc.

1.3.1 Size (DC-SSCB level issue)

The current-limiting inductor and the cooling system for power semiconductors make the size and volume of DC-SSCB not as expected. One 500A, 300uH inductor can be up to 100kg. Moreover, it is costly to build such a big inductor. Thus, the current-

limiting inductor is a severe burden for the DC distribution system with multiple DC-SSCBs. Considering that the cooling system is inevitable for power semiconductors, it is meaningful to optimize the current-limiting inductor design for DC-SSCB.

1.3.2 Losses (DC-SSCB level issue)

Compared with MCB and HCB, the higher conduction loss for DC-SSCB limits the development of DC-SSCB. However, with the development of the wide-bandgap (WBG) semiconductors (e.g., silicon-carbide (SiC) and gallium-nitride (GaN), the lower on-state resistance of the WBG semiconductors can help DC-SSCB decrease the conduction loss and the size of the cooling system.

1.3.3 Oscillation (DC-SSCB level issue)

Because the power semiconductors in DC-SSCB need to deal with high voltage and high current during fault interruption, the power semiconductors may happen severe oscillation. How to interrupt the high current and high voltage without any oscillation is a challenge for DC-SSCB design.

1.3.4 System-friendly functionality (System level issue)

As Section 1.1.2 mentioned, the DC distribution with high penetration of power electronics requests more requirements for the DC-CB from the system level. Through leveraging the power electronics technology, DC-SSCB is a promising solution to overcome new challenges from the next-generation fault-tolerant-capable system. According to the challenges in Section 1.1.2, DC-SSCB should possess the following characteristics:

1. The fault current trigger threshold can be tuned by the operation mode of the DC distribution system.
2. The fault detection should be sensitive enough to protect the vulnerable interfaced power converter.
3. The response time of DC-SSCB can be adjusted according to system-level or converter-level requirements.
4. DC-SSCB has the ride-through capability for the rest healthy parts of the system.
5. DC-SSCB can take different actions based on different fault cases.

DC-SSCB has the potential to realize the above functions. However, how to fully leverage the power electronics technology to realize those functions and how to integrate those functions into DC-SSCB are burdensome. It is noted that it is almost impossible for MCB and HCB to realize those functions.

1.4 Dissertation Layout

This dissertation is organized as follows:

Chapter 2 reviews the research activities in DC-SSCB. Based on the result of the literature review, there is no lightweight DC-SSCB for aviation applications. And there is no current limitation technique to take place of the bulky current limitation inductor. Moreover, most of the papers focus on the interruption capability of DC-SSSB and ignore the system-friendly functions of DC-SSCB. For the DC distribution system, DC-SSCB needs to have the fault distinguish capability, fault ride-through capability, tunable response time, tunable fault trigger current, etc.

Chapter 3 proposes a high-power density SSCB without the current limiting inductor for aviation applications. The proposed SSCB can limit the maximum peak fault current level through *V-I* curve characteristics, thus achieving a power density over 100kW/kg for hybrid electric propulsion applications. The gate voltage can also tune the peak fault current level. The proposed gate voltage-based current limitation strategy can limit the system peak current to 2000 A when the gate voltage is 12 V.

SSCB's behavior is sensitive to power semiconductors, gate drives, energy absorbers (e.g. varistor), and their coupling. Thus, it is critical to understand the impact of different design parameters on the performance of SSCB, especially on the fault current interruption. Chapter 4 proposes an analytical model to establish the relationship between SSCB dynamic performance when the fault is being cleared dependence on design variables and operating conditions. Then the sensitivity analysis is performed based on the proposed model to identify the most critical design parameters. Finally, simulation and test results based on a 2kV/1kA SSCB prototype demonstrate the accuracy of the proposed model, which provides fundamentals for the design optimization of SSCB considering gate drive and energy absorber.

To limit the fault current with DC-SSCB, power semiconductors need to operate in the active region temporarily. During this interval, a severe voltage oscillation is observed, leading to the DC-SSCB overstress and eventually the failure. Chapter 5 aims to understand the mechanism causing the voltage oscillation and devise solutions to suppress it. First, a MATLAB/Simulink model is built with comprehensive considerations of power semiconductors, parasitic, gate drive, and metal oxide varistor (MOV). Then a sensitivity

study is performed to identify the critical impact factor(s) causing the voltage oscillation. Afterward, three suppression methods using enhanced gate drive circuitry are proposed and compared. Finally, test results based on a 2kV/1kA SSCB prototype demonstrate the effectiveness of the proposed oscillation mitigation method and the accuracy of the derived model.

Chapter 6 analyzes the influence of the bus bar's connection to the IGBT module-based SSCB when the dead short happens (system inductance is almost zero). With the help of the Q3D extractor, when the dead short happens, it is proven that the gate loop can couple with the electromagnetic field generated by the power loop. The induced voltage can influence the gate voltage and saturation current. To eliminate the influence of the electromagnetic field of the power loop on the gate loop, a vertical bus bar is proposed. Based on the result of the Q3D extractor, the vertical bus bar-based SSCB can have a smaller L_E, which means that the power loop has less impact on the gate loop. Accordingly, the saturation current (maximum limiting current) for SSCB can be no longer influenced by the bus bar connection.

To increase the current interrupting capability for the DC solid-state circuit breaker (DC-SSCB), power semiconductors need to possess a higher pulse current. Moreover, for the power electronics protection system, it is also important to enable the system with a fault current limitation capability. Chapter 7 presents a gate drive circuit design for the system-friendly SSCB with current limitation capability. The proposed gate drive enables the SSCB to operate in the current limitation mode to limit the overcurrent in the aviation system. The current limitation mode can help the aviation system limit the inrush current

during startup and realize fault ride-through for the healthy part when the fault occurs. Finally, test results based on a 200V/150A SSCB with the current limitation mode prototype verify the proposed intelligent gate drive design for SSCB with cryogenic cooling.

Chapter 8 provides an all-in-one solution for system-friendly SSCB, with integrated circuitries as the fault detector, actuator for the semiconductor's operating status regulation, and coordinated control to seamlessly transition from one mode to another (e.g., normal mode, precaution mode, i^2t mode, and interruption mode). This allows the developed SSCB to limit system fault current not exceeding short-circuit current rating (SCCR) and also take different responses under different fault cases. First, two improved fault detection circuits are introduced to better serve the SSCB application. Second, four operation modes are proposed for SSCB to realize system-friendly functions. Third, by leveraging four different operation modes, a control strategy is demonstrated to take different actions based on different fault cases. Finally, the feasibility and the effectiveness of the proposed system-friendly 200V/10A SSCB is validated with experimental results.

Chapter 9 presents the conclusion and future work.

CHAPTER TWO

2 LITERATURE REVIEW

Based on the online library, the first DC-SSCB supported by NASA was invented in 1973 [23]. The proposed silicon-controlled rectifier (SCR) based 270V DC-SSCB can interrupt 18A in 600 μs. In Japan, a thyristor-based [24] 750 V/600 A DC-SSCB can interrupt a 5000 A fault current within 250 μs in 1974. Before 2000, because AC dominated the power system, compared with DC-SSCB, AC-SSCB received more attention. However, since 2010, with the development of power electronics technology, renewable energy, electrified transportation, etc., the DC power distribution system became popular and DC-SSCB gradually became a research hotspot for DC power distribution systems.

2.1 Review for SSCB based on different teams

Research on DC-SSCB by Dr. John Shen's team from the Illinois Institute of Technology (IIT) can trace back to 2015 [25]. Their studies focused on the 300~400V wide-bandgap (WBG) based self-powered DC-SSCB. Based on WBG normally-ON power semiconductors, paper [25] proposed a novel category of self-powered DC-SSCBs. The topology is illustrated in Figure 2. 1. When the fault is detected by sensing the drain-source voltage rise, the power drawing from the fault condition is leveraged to turn off the normally-ON power semiconductor. An isolated DC-DC converter protects the power semiconductor's gate drive circuit. Based on a 1200 V SiC JFET, a 400V self-powered DC-SSCB can interrupt a fault current of 125 A in 1 μs. Moreover, [25] verifies that the low ON-resistance normally-ON WBG power semiconductors help DC-SSCB increase its

efficiency. In the following seven years, most studies on DC-SSCB from Dr. John Shen's team were based on the self-powered DC-SSCB proposed in [25]. [26, 27] proposed a bidirectional self-powered 400 V DC-SSCB with back-to-back connected normally-ON 1200 V SiC JFET. The proposed bidirectional self-powered DC-SSCB can turn off a 150 A fault current in 0.7 μs, which is the fastest DC-SSCB at that time. Based on the topology in [25], GaN FET is first leveraged as the static switch for self-powered DC-SSCB in [28]. Then, cascaded 1200V normally-on SiC JFETs are leveraged to increase the self-powered DC-SSCB's interruption voltage and current [29]. With 1200V DC bus voltage, the proposed cascaded SiC JFETs-based DC-SSCB can interrupt 125 A in 2.5 μs. Since 2017, Dr. John Shen's team has begun to study the self-powered DC-SSCB with some intelligent functions. [30] reported a self-powered DC-SSCB with an adjustable current-time tripping profile for protection. In a hierarchical power system, the current-time tripping profile can serve to prevent the DC-SSCB from accidentally tripping owing to an inrush of transient current. It also allows for selective coordination across several SSCBs with varied current-time tripping profiles. Then, a SiC-based self-powered DC-SSCB with three operation states was proposed in [31]. Besides the ON and OFF states, it also has PWM current limiting state, which enables the self-powered DC-SSCB to progressively charge the electronic loads' input capacitors at a constrained current level during load startup. Furthermore, based on the PWM current limiting state in [31], Dr. John Shen's team proposed an algorithm in [32] that can calculate the inductance between the short circuit fault location and the self-powered DC-SSCB. The distance of the fault location can be calculated by measuring the response of the voltage pulses sent to the DC system. Based

on [31] and [32], SiC-based and GaN-based tri-mode self-powered DC-SSCB "ibreaker" were demonstrated in [33] and [34], respectively. The GaN-based "ibreaker" efficiency can be up to 99.92%.

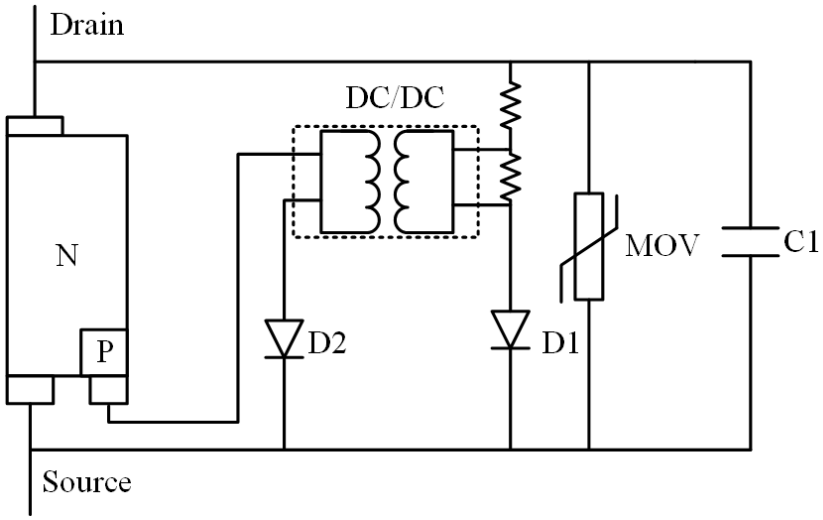


Figure 2. 1: Topology of the self-powered DC-SSCB.

ASEA Brown Boveri (ABB) began its research on DC-SSCB in 2012. They focus on the high power, high current DC-SSCB for shipment application. Paper [35] [36] proposed a parallel connected varistors-based snubber circuit for DC-SSCB, which can decrease the stray inductance to limit the peak overvoltage during the fault current interruption. Thus, one varistor is leveraged for energy absorption, while the other is for overvoltage protection. Based on a 2.5kV reverse blocking-IGCT (RB-IGCT), an air-cooled 1MW bi-directional DC SSCB was developed in [37]. RB-IGBCT's low on-state voltage drop and high turn-off current capability make it become an outstanding candidate for DC-SSCB's power semiconductor. Then, ABB continued some research on the RB-IGCT-based DC-SSCB, including high current application [38], thermal design [39], parallel connection test [40], busbars design [41], etc. Their latest three anti-parallel RB-

IGCT branches in parallel based 1 kV/5 kA high current DC-SSCB with 99.9% efficiency can interrupt 15 kA fault current within 20 μs for all-electric Ships [42]. ABB DC-SSCB team also explored the feasibility of SiC-based [43] and GaN Gate Injection Transistor (GIT) based DC-SSCB [44]. They studied the transient thermal performance of SiC and GaN (e.g., GaN GIT can withstand over 150 °C junction temperature for short durations). Additionally, from the system level, ABB also launched several studies on the DC-SSCB for the shipment distribution system [45, 46].

Since 2013, the University of Tennessee, Knoxville (UTK) has begun to launch studies on DC-SSCB. UTK team focuses on the SiC-based DC-SSCB and the improvement of the DC-SSCB stability and reliability. Paper [47, 48] demonstrated and compared three overcurrent protection strategies for SiC MOSFET. A 600 V SiC DC-SSCB with the proposed overcurrent protection strategy can interrupt a 100 A fault current in 200 ns. Then, in 2018, the short-circuit characteristic of the Gen3 10 kV/20 A SiC MOSFET was tested in [49]. Based on the two series connected SiC MOSFET tested in [49], a 1200V DC-SSCB with a single gate driver was delivered in [50]. The proposed 1200V DC-SSCB can interrupt 75 A fault current within 1.5 μs. To improve the reliability of DC-SSCB, [51] investigated the heatsink's influence on the power switch's dynamic thermal performance. Moreover, they proposed a method to characterize the i^2t capability of devices under the worst operating scenario for DC-SSCB. To solve the instability issues of the SiC power module for DC-SSCB application during high current switching transients, [52] found that the parallel stability can be affected by the switching trajectory. Accordingly, they improved the stability of DC-SSCB during high-current switching transients by

manipulating the switching trajectory. Recently, UTK began to study GaN-based DC-SSCB. Cooperating with ABB, [44] evaluated the overcurrent capability of 600V GaN GITs. Then, [53] demonstrated a current limiting control strategy for two series connected GaN-based DC-SSCB. By alternating two GaN switches and leveraging TVS diodes, which have better robustness and energy absorption capability, the current limiting function of DC-SSCB is improved.

As the critical component of the DC distribution system, DC-SSCB also attracts the attention of China. Tsinghua University's teams focused their studies on high power, high current DC-SSCB. Based on IGCT, [54] developed a 375 V/5 kA DC-SSCB for AC/DC hybrid distribution system. The proposed DC-SSCB can break 5kA within 100 μs. Then, an optimized low ON-state voltage IGCT (LO-IGCT) (e.g., 1.11 V at the current of 2000A) based DC-SSCB is proposed in [55]. The test result showed that the selected LO-IGCT-based DC-SSCB's blocking voltage could be higher than 4500 V, and the controllable current could be up to 2400 A. Recently, an oscillating commutation-based 8kV DC-SSCB was introduced in [56]. Thanks to the compound IGCTs, the proposed 8kV DC-SSCB can interrupt 7kA within 20 μs.

2.2 Review for SSCB

Figure 2. 2 illustrates the key components of the DC-SSCB. Based on different functions, a DC-SSCB can mainly be separated into four main parts: power semiconductor, voltage clamping & energy absorption circuit, fault detection circuit, and gate driver.

Power semiconductor is leveraged to conduct the system's current. During normal operation, the power semiconductor keeps on-state; when the short-circuit is detected, the

power semiconductor can be turned off to interrupt the fault current. The voltage clamping & energy absorption circuit is leveraged to clamp the voltage across the power semiconductor during the interruption transient and absorb the extra system energy during the turn-off process. The fault detection circuit monitors the operation state of the DC-SSCB online and produces a fault signal when the fault is detected. Finally, the gate driver receives the control signal from the fault detection circuit. Once the fault is detected, the gate driver will control the power semiconductor to interpret the fault current.

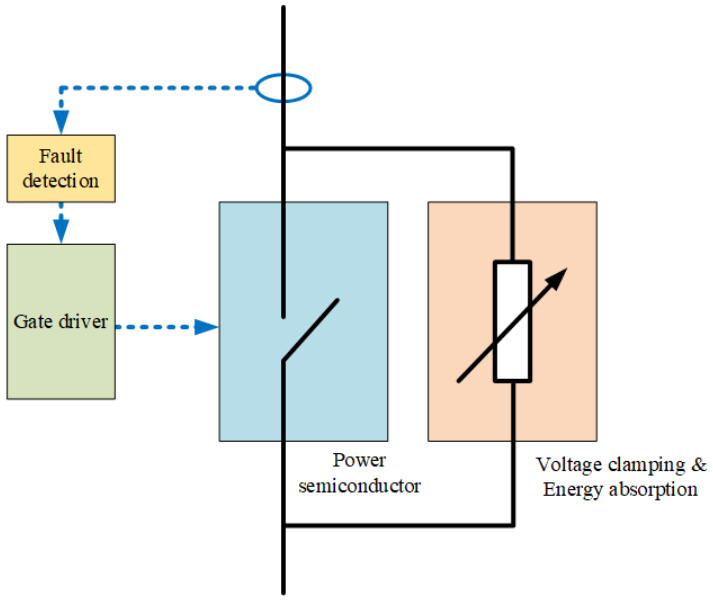


Figure 2. 2: Key components of the traditional DC-SSCB.

2.2.1 Power semiconductors for SSCB

As the core component of the DC-SSCB, the power semiconductor determines the performance of the DC-SSCB.

Firstly, the continuous DC collector/drain current and collector-emitter/drain-source blocking voltage of the power semiconductor determine the rating current and voltage of DC-SSCB.

Secondly, because the power semiconductor keeps on-state during the normal operation of DC-SSCB, the on-state resistance of the power semiconductor dominates the power loss of DC-SSCB. In other words, the power semiconductor's on-state resistance influences the efficiency of DC-SSCB.

Thirdly, the power semiconductor's short circuit capability also plays an important role in DC-SSCB. The worst scenario for DC-SSCB without a current limitation inductor is that there is a dead short-circuit close to DC-SSCB. The system inductance can be close to zero, and the fault current di/dt can achieve 800V/μs for a 200 V DC bus voltage. Normally, there will be some delay in the fault detection process and the power semiconductor turn-off process. When the system inductance is close to zero, the fault current can force the power semiconductor to enter the active region before the gate driver entirely turns off the power semiconductor. Thus, the power semiconductor's short circuit capability is crucial to ensure that the power semiconductor is robust enough to hand with the high fault current.

Finally, the switching speed of the power semiconductor is also significant for DC-SSCB. As mentioned in the last paragraph, when the system inductance is close to zero, the power semiconductor is highly likely to face the high system fault current and enter the active region. Thus, the high switching speed can help the power semiconductor reduce the time to tolerate the high current. For example, the turn-off speed for GaN-based DC-SSCB

is about 200 ns, while for IGBT-based DC-SSCB is about 1 μs, which means that the IGBT has to stand another 800 ns high system fault current.

It has to be pointed out that the cost and availability of the power semiconductor are also crucial for the selection of DC-SSCB's power semiconductor. Some power semiconductors have appropriate characteristics for DC-SSCB application (e.g., low conduction loss, reverse blocking capability, good short-circuit capability, etc.). However, considering that they are expensive or hard to mass produce, they are unsuitable for DC-SSCB.

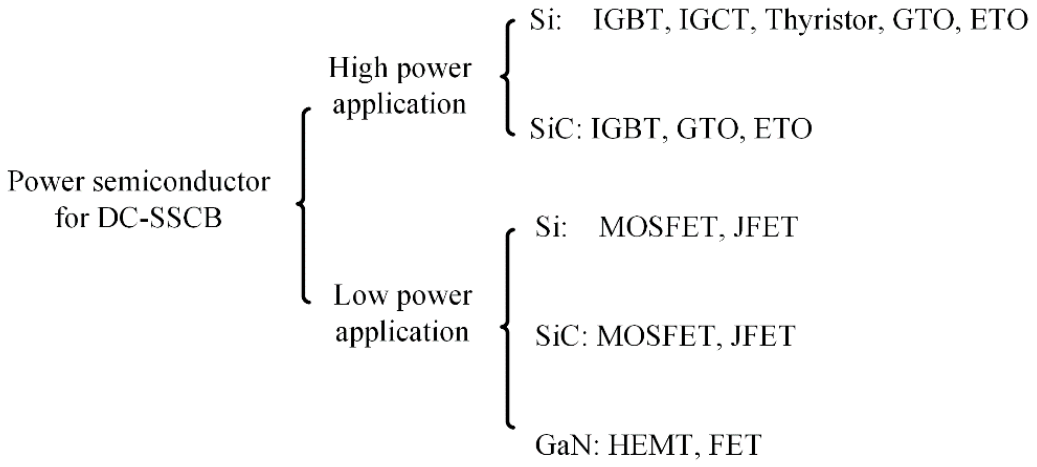


Figure 2. 3: Power semiconductor's categorization for DC-SSCB application.

Figure 2. 3 shows the power semiconductor's categorization for DC-SSCB application based on the different power levels. For low-power DC-SSCB (e.g., DC bus voltage is lower than 650V), Si-based MOSFET [57], JFET, SiC-based MOSFET, JFET, and GaN-based FET are popular. The characteristics comparison among some typical power semiconductors (e.g., GaN, SiC MOSFET, SiC JFET, and Si MOSFET) for low-power DC-SSCB is displayed in Figure 2. 4. Regardless of the cost, the conduction loss,

current capability, blocking voltage capability, short circuit capability, and switching speed are selected metrics. The power semiconductor has better performance from the inner layer to the outer layer of the pentagon.

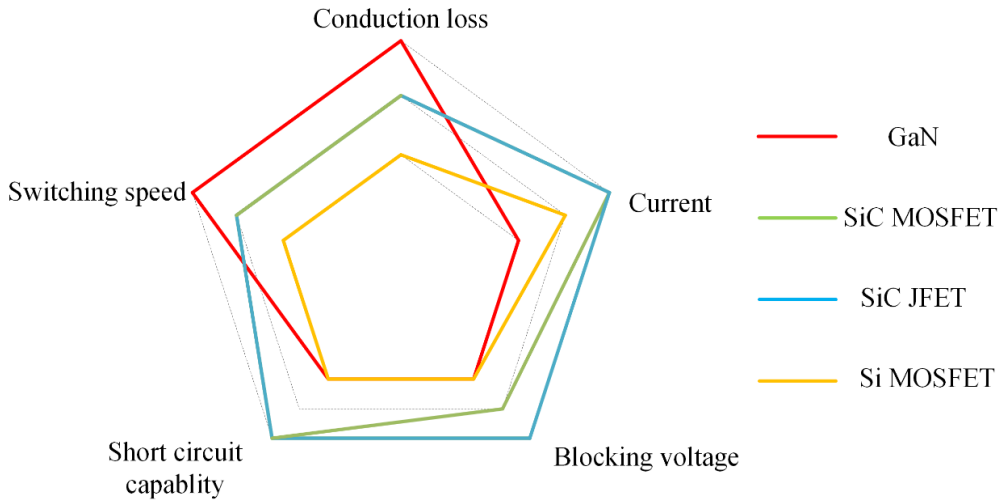


Figure 2. 4: Comparison of typical power semiconductors for low-power DC-SSCB.

Firstly, compared with Si-based power semiconductors, WBG power semiconductors' thinner drift regions are realized by the higher electric breakdown field, which helps WBG power semiconductors have relatively low on-state resistance. Moreover, the GaN's high mobility further decreases the on-state resistance [58, 59]. Accordingly, GaN-based DC-SSCB has the lowest conduction loss, which means the highest efficiency. Meanwhile, SiC-based DC-SSCB's conduction loss is higher than GaN-based DC-SSCB but lower than Si-based DC-SSCB.

Secondly, because of the higher saturated electron velocity and lower input/output capacitance (WBG power semiconductors have a smaller die size to achieve the same current capability), WBG power semiconductors have better performance on switching speed [58, 59]. Because GaN-based power semiconductors have better-saturated electron

velocity than SiC-based power semiconductors, GaN-based power semiconductors switching speed is faster than SiC-based power semiconductors.

Thirdly, for short-circuit capability, Si-based power semiconductors are better than SiC-based power semiconductors, and SiC-based power semiconductors are better than GaN-based power semiconductors. Because WBG-based power semiconductors have higher current density than Si-based power semiconductors under short-circuit scenarios. Accordingly, the lower thermal capacitance and the higher transient power density make the WBG-based power semiconductor have a faster temperature rise, and worse short-circuit withstand time.

Fourthly, compared with Si-based power semiconductors, SiC-based power semiconductors have a higher electric breakdown field, which helps SiC-based power semiconductors have a less thickness with the same voltage rating. Moreover, SiC-based power semiconductors can support a higher current density with higher thermal conductivity. Accordingly, SiC MOSFET has a higher rating voltage and current than Si MOSFET. However, because of the limitation of the technology, the commercial GaN-based power semiconductors' rated voltage, and rated current are limited to 650 V and 60 A, respectively.

For high-power DC-SSCB (e.g., DC bus voltage is higher than 650V), Si-based IGBT, IGCT, thyristor, GTO, and SiC-based IGBT, GTO, ETO are popular. The characteristics comparison among some typical power semiconductors (e.g., Si IGBT, Si IGCT, and SiC ETO) for high-power DC-SSCB is displayed in Figure 2. 5. Regardless of the cost, the conduction loss, current capability, blocking voltage capability, short circuit

capability, and switching speed are selected metrics. The power semiconductor has better performance from the inner layer to the outer layer of the pentagon.

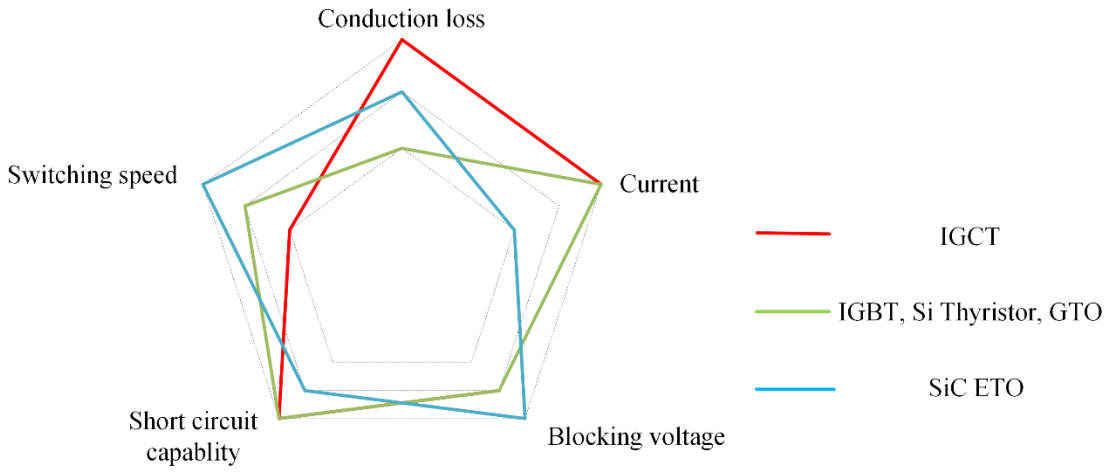


Figure 2. 5: Comparison of typical power semiconductors for high-power DC-SSCB.

Besides the advantages of the thyristor (e.g., SCR), the Gate Turn-Off thyristor (GTO) can interrupt the fault current when desired. However, the turn-off conditions for GTO are hard to meet, which makes the gate driver complicated. Then, based on the GTO, IGCT was invented. And IGCT has become a promising power semiconductor candidate for high-power DC-SSCB. Compared with Si IGBT, IGCT has lower conduction loss and higher surge current capability. IGCT can be categorized into reverse conducting (RC)-IGCT, reverse blocking (RB)-IGCT, and asymmetric IGCT [60]. RB-IGCT is the most popular IGCT for DC-SSCB applications. For WBG power semiconductors, because of the limitation of the technology, GaN-based power semiconductors cannot be applied to high-power applications. Meanwhile, the rated voltage and current of SiC-based power semiconductors can be up to 1700 V and 600 A, which are far away from the Si-based power semiconductor.

Therefore, the trade-off among conduction loss, switching speed, short circuit capability, rated current, and voltage for DC-SSCB is inherent in the selection of the power semiconductor. For low-power applications, WBG power semiconductors are suitable for their low conduction loss and fast switching speed. Meanwhile, Si-based power semiconductors are more robust with a high system current. For high-power applications, RB-IGCT is an outstanding candidate for DC-SSCB. But when considering the cost and availability, IGBT maybe also a good candidate

2.2.2 Topologies of solid-state circuit breaker

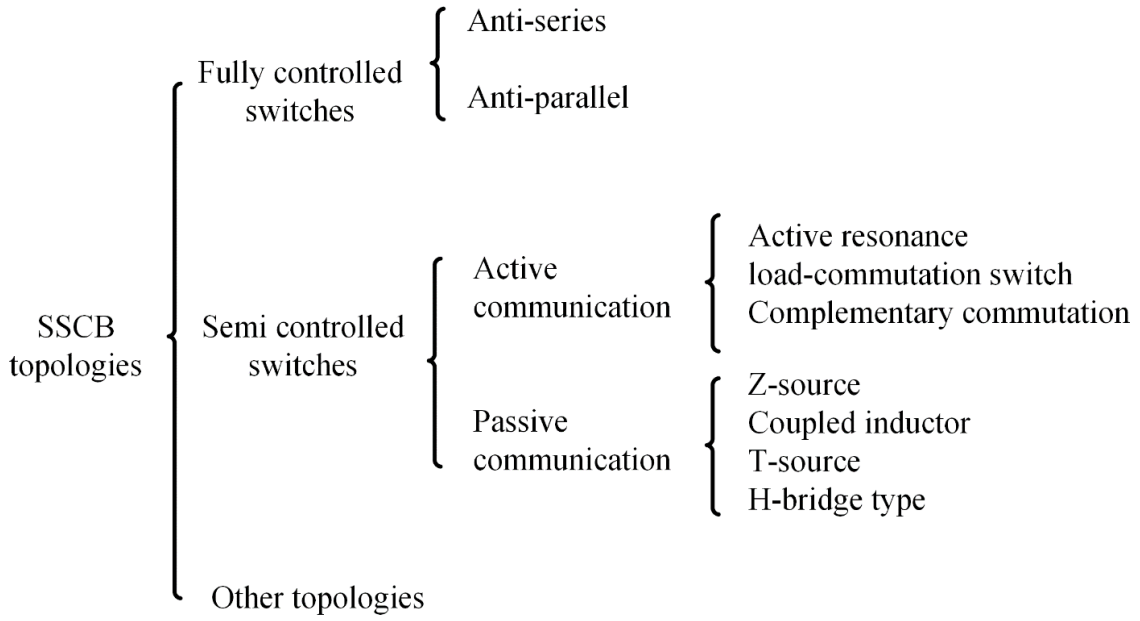


Figure 2. 6: Summarization of different topologies for DC-SSCB.

As shown in Figure 2. 6, the topology of DC-SSCB is highly related to the characteristics of the power semiconductor. In most cases, considering that the modern DC distribution system is bidirectional, the power semiconductors block of DC-SSCB is

expected to block bipolar voltage and conduct a bidirectional system's current. Accordingly, to fit with the bidirectional DC distribution system and the characteristics of the power semiconductor, the DC-SSCB's topology can be divided into fully controlled switches-based topology, semi-controlled switches-based topology, and other topologies. This Section does not consider the topology to increase the rating voltage and rating current for DC-SSCB.

2.2.2.1 Topologies of solid-state circuit breaker

Fully controlled power semiconductors have been widely leveraged by DC-SSCB, e.g., IGBT, IGCT, MOSFET, HEMT, etc. For a bidirectional DC-SSCB, the power semiconductor block must block bipolar voltage and conduct bidirectional current.

For the reverse conducting (RC) device (e.g., unipolar FETs), their integral body diode can help them conduct the reverse current. Meanwhile, for bipolar devices (e.g., IGBT), the manufacturer usually packages a paralleled diode with the IGBT to realize the reverse conducting. Thus, as shown in Figure 2. 7, no matter for RC devices or bipolar devices with paralleled diodes, they all require an anti-series connection to block bipolar voltage.

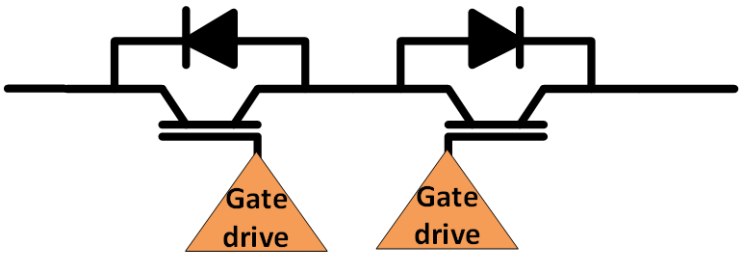


Figure 2. 7: Anti-series topology for IGBT.

For the reverse blocking (RB) device (e.g., RB-IGCT), their inherent characteristics allow them to block the reverse voltage, which means that they do not need to connect anti-series to block bipolar voltage. However, they have to leverage the anti-parallel topology to conduct the bidirectional current, which is shown in Figure 2. 8.

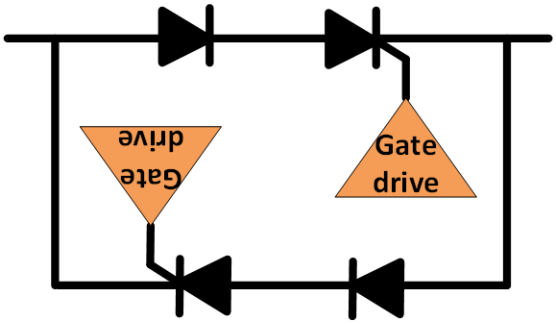


Figure 2. 8: Anti-parallel topology for RB-IGCT.

2.2.2.2 Topologies of solid-state circuit breaker

Unlike fully controlled power semiconductors, since the gate terminal cannot directly turn off semi-controlled power semiconductors (e.g., thyristors), they need an auxiliary circuit to interrupt the fault current. Thyristors are born with reverse blocking characteristics, meaning they need to be connected anti-parallel for the bidirectional DC-SSCB. Based on the commutation strategies, thyristor-based DC-SSCB can be divided into active commutation and passive communication to interrupt the fault current.

Based on the topology, active commutation can be categorized into active resonance, load-commutation switch, and complementary commutation [61]. Figure 2. 9 shows the basic topology of the active resonance-based commutation. When the fault is detected, the fault signal can turn on the auxiliary switch to generate a resonant current through the inductor and capacitor. The generated resonant current can help the active resonance DC-SSSB's main thyristor turn off [62, 63]. Compared with active resonance,

an auxiliary IGBT connects in series with the thyristor for load-commutation switch-based commutation. When the fault is detected, the auxiliary IGBT will be turned off, and with the help of the MOV, the thyristor can be turned off to interrupt the fault current [64]. Finally, for complementary commutation, DC-SSCB leverages the energy stored in a precharge capacitor to turn off the thyristor when the fault is detected. Paper [65] proposes three different AC-SSCB topologies based on the complementary commutation.

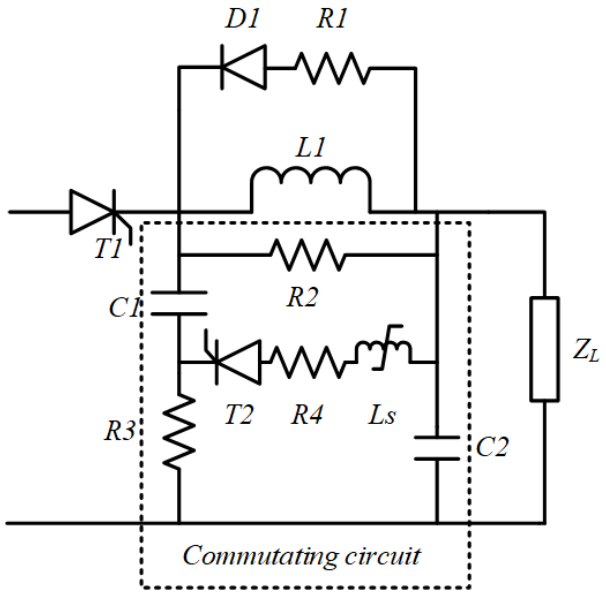


Figure 2. 9: Topology of the active resonance-based DC-SSCB.

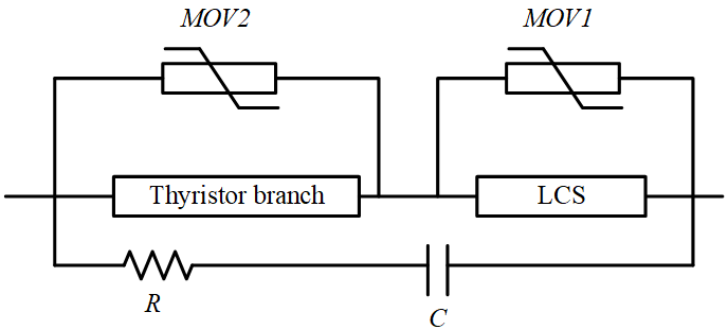


Figure 2. 10: Topology of the load-commutation switch-based DC-SSCB.

For passive commutation, when the fault happens, the fault current can naturally commutate from the thyristor to the low-impedance coupled inductors or capacitors. The first Z-source-based passive commutation DC-SSCB is proposed in [66]. The basic Z-source topology is illustrated in Figure 2. 11. When the fault happens, an LC-based Z-source circuit is leveraged to turn off the thyristors. The Z-source circuit's natural commutation (without current sensing for fault detection) enables the DC-SSCB to have a fast operation. Based on [66], more modified Z-source DC-SSCBs with auxiliary switches are developed [67, 68]. For example, to decrease the high starting current of the thyristor and eliminate the negative current flowing through the load of the conventional Z-source network, an auxiliary IGBT-based modified Z-source network for DC-SSCB is proposed in [67]. Moreover, coupled inductors are leveraged to improve the performance of the passive commutation DC-SSCB [69-71]. The paper [70] first presents a coupled-inductor-based passive commutation DC-SSCB, which can tune the current level to automatically turn off the thyristor by changing the coupled inductor's turn ratio. Then, to decrease the response time of the passive commutation DC-SSCB and keep the tunable fault current tripping level, T-source DC-SSCB is proposd in [72]. As shown in Figure 2. 12, T-source DC-SSCB is composed of a capacitor and a two-winding coupled transformer. Besides, H-bridge-based topology is also a good candidate for passive commutation [73], which is shown in Figure 2. 13. An H-bridge construction with the inductor and capacitor components makes it possible for a thyristor inside the bridge to open and interrupt the fault current.

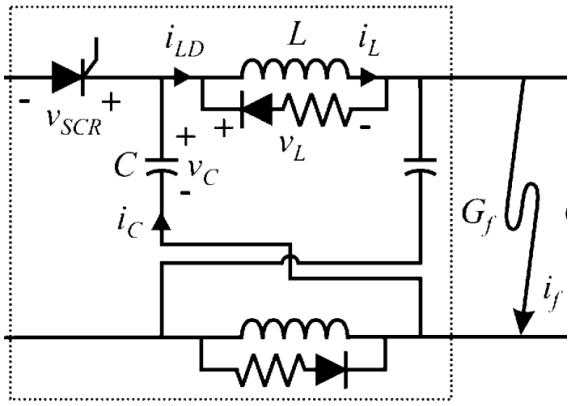


Figure 2. 11: Topology of the Z-source-based DC-SSCB.

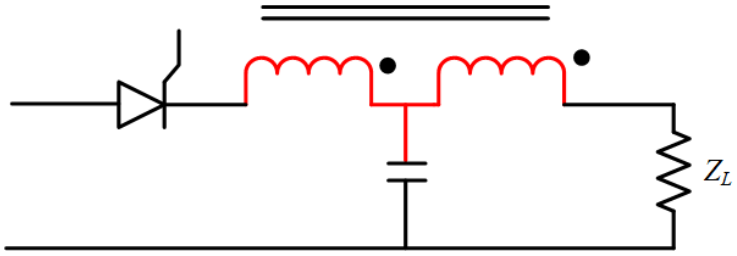


Figure 2. 12: Topology of the T-source-based DC-SSCB.

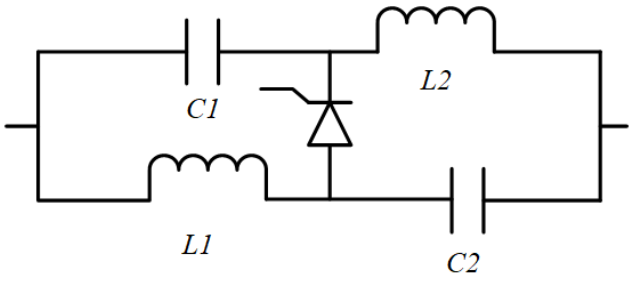


Figure 2. 13: Topology of the H-bridge-based DC-SSCB.

2.2.2.3 Other topology

As mentioned at the beginning of this Section, the self-powered DC-SSCB based on normally ON devices from Dr. John Shen's team is a unique topology. Normally ON devices (e.g., GaN HEMT, SiC JFET) can conduct the system current automatically

without any gate drive circuit control during normal operation. When the fault is detected, an isolated dc-dc converter is leveraged to convert the increased ON-state voltage to a negatively biased gate voltage to turn off the normally ON devices. An n-type and p-type MOSFET-based fault current sensing topology is proposed in [74]. Besides, By combining the advantages of different power semiconductors, hybrid power semiconductors-based DC-SSCB topologies are also studied by many researchers [56].

2.2.3 Voltage clamping & energy absorption circuit for SSCB

As one of the most important components for DC-SSCB, voltage clamping, and energy absorption circuit enables the safe turn-off of the power semiconductor. It not only limits the maximum voltage across the power semiconductor during the power semiconductor's turn-off transient but also absorbs the extra energy stored by the system inductance after the power semiconductor is fully turned off.

Based on the operation principle of the voltage clamping and energy absorption circuit, it can be classified as passive voltage clamping and active voltage clamping, which is shown in Figure 2. 14. Passive voltage clamping leverages the passive components (e.g., metal oxide varistors (MOV), transient voltage suppression diodes (TVS), and capacitor-related snubber circuits) to clamp the voltage across the power semiconductor. Meanwhile, with the help of the auxiliary switches, the active voltage clamping enables more freedom for the voltage clamping, enhancing the performance of the passive voltage clamping components.

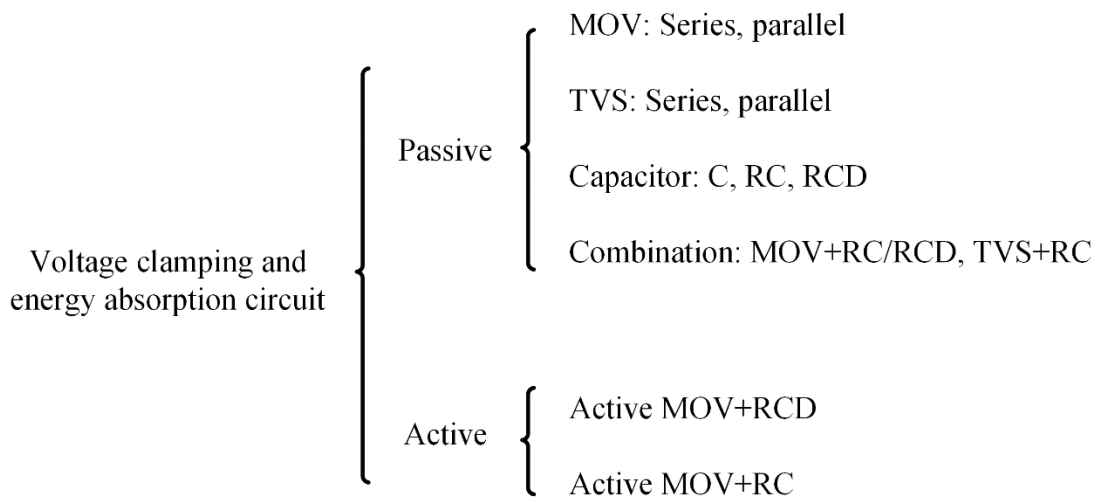


Figure 2. 14: Classification of the voltage clamping and energy absorption circuit.

2.2.3.1 Passive voltage clamping

MOV is one of the most common passive voltage clamping components for DC-SSCB. MOV is a voltage-dependent component made from zinc oxide, silicon oxide, etc. The MOV's resistance varies from being a nearly open circuit to a very low value when exposed to high-voltage transients, clamping the transient voltage to a safe level. During DC-SSCB normal operation, the voltage across the MOV is lower than MOV's clamping voltage, MOV stays at a high impedance state, and the system current flows through the power semiconductor. Once the fault happens, the high voltage across the power semiconductor forces the impedance of the MOV to decrease to almost zero, and the system current commutate from the power semiconductor to MOV. Thus, to make sure a reliable clamping voltage for the power semiconductor, the selection of MOV plays a significant role. Paper [75] proposes a four-step MOV selection method for DC-SSCB.

To improve the performance of the MOV-based voltage clamping circuit, multiple MOVs are connected in series or parallel. Because of the MOV technology limitation,

MOVs are required to connect in series to fit with the high-voltage DC-SSCB. MOVs are also connected in parallel, enabling higher current flow through the MOV block when the power semiconductor is turned off. Besides, paper [35] [36] proposes a paralleled MOV-based topology to split the functions of voltage clamping and energy absorption. To maintain a low stray inductance, the MOV for voltage clamping is placed close to the power semiconductor. Meanwhile, the MOV for energy absorption can be placed away from the power semiconductor, which is good for the MOV's heat dissipation. However, MOV is easy to get degraded during the energy absorption process for DC-SSCB. And the high dv/dt can also cause the power semiconductor's gate-source terminal ringing, gate oxide degradation, false turn-on, etc. Accordingly, an active voltage clamping technique for MOV is required to avoid degradation, which will be demonstrated later [76].

TVS is another promising passive voltage clamping component for DC-SSCB [53, 77]. TVS is a silicon avalanche device typically selected for the fast response time (low clamping voltage), lower capacitance, and low leakage current. TVS works though restricting the voltage using p-n junctions that are bigger than those of a typical diode, enabling it to safely carry higher currents to the ground. Compared with MOV, TVS is much more expensive, which limits its application to DC-SSCB.

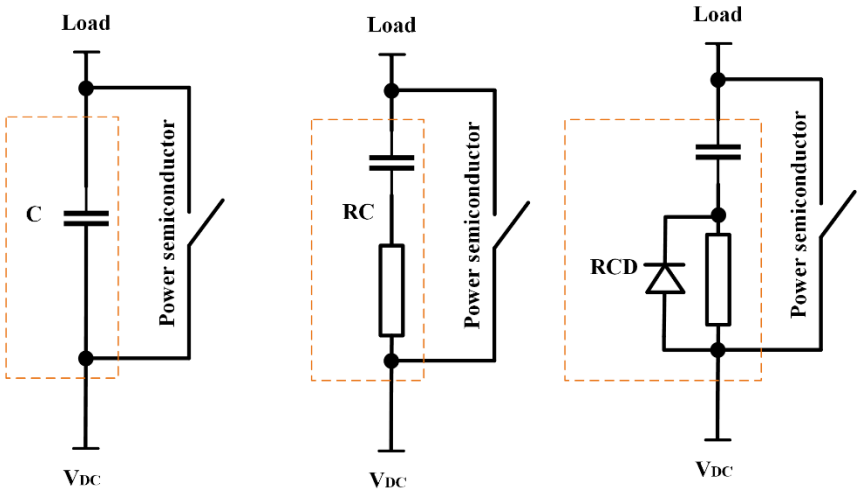


Figure 2. 15: Capacitor-related snubber circuit for DC-SSCB.

The capacitor-related snubber circuit is also a good candidate for passive voltage clamping. Figure 2. 15 illustrates the three topologies for capacitor-related snubber for DC-SSCB. Same with the snubber to limit the transient dv/dt and voltage spike for power semiconductors in the power converter, the capacitor-related snubber can also be leveraged to DC-SSCB to suppress the overvoltage during the DC-SSCB turning-off process. During the turn-off process of the power semiconductor in DC-SSCB, the capacitor snubber can decrease the *dv/dt* across the power semiconductor and absorb the residuary system energy. Thus, the capacitor should have the capability to withstand a high charging current during the turning-off transient. However, the capacitor is highly likely to oscillate with the system inductance during the turn-off process, which is dangerous for DC-SSCB operation. Accordingly, resistor-capacitor (RC) and resistor-capacitor–diode (RCD) snubber are proposed to take the place of the capacitor snubber. For RC snubber, the additional resistor can help the capacitor damp the oscillation during the power semiconductor turn-off transient. However, the voltage drop across the resistor can increase the voltage spike

across the power semiconductor, which is undesired. Accordingly, an RCD-based snubber [78-80] is developed by parallelling a diode with the resistor to eliminate the voltage drop on the resistor during the turn-off transient. [81] compares the voltage clamping capability between RC snubber and RCD snubber. However, the capacitor-related snubber cannot fully absorb all the residual energy after the interruption, which leaves extra voltage stress to the power semiconductor.

Considering that MOV, TVS, and capacitor-related voltage clamping schemes all have their own disadvantages, some hybrid voltage clamping schemes are proposed to combine the advantages of different voltage clamping schemes, e.g., MOV+RC [82], MOV+RCD [80, 83-85], and TVS+RC, which are illustrated in Figure 2. 16. For only MOV or TVS-based DC-SSCB, the high *dv/dt* during the turn-off transient may fault trigger the power semiconductor, cause gate oscillation, and gate-oxide degradation. An extra capacitor-related snubber can help DC-SSCB limit the *dv/dt* during the turn-off transient. To develop a high economic efficiency MOV+RC voltage clamping method by decreasing the cost of the passive components for DC-SSCB, Paper [82] optimizes the design for the MOV+RC through a new dynamic mode. By paralleling an additional MOV with the resistor, a MOV2+RC voltage clamping circuit is proposed in [86]. The proposed MOV2+RC voltage clamping circuit can limit the peak voltage and smooth DC-SSCB's turn-off voltage slew rate. Recently, the MOV+RCD voltage clamping circuits have attracted more and more studies from all over the world. Paper [62] proposes a design methodology for DC-SSCB's MOV+RCD voltage clamping circuit based on the snubber charging time and the thermal dissipation. Moreover, to minimize the capacitance of the

snubber for DC-SSCB with series-connected IGBT, a novel hybrid voltage-balancing scheme for series series-connected IGBT with related MOV+RCD is demonstrated in [80].

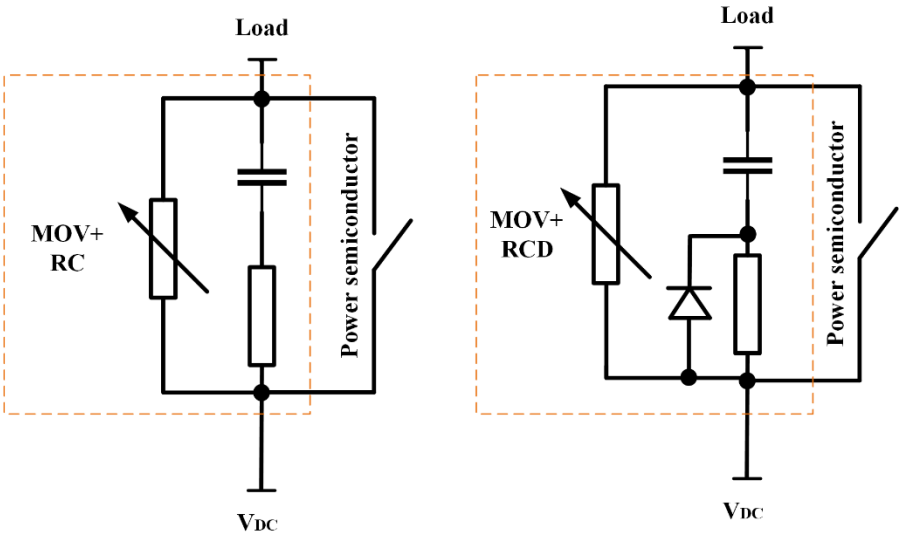


Figure 2. 16: Hybrid passive voltage clamping topologies for DC-SSCB.

2.2.3.2 Active voltage clamping

Although the passive voltage clamping schemes require fewer components and are easier to implement, they still have some disadvantages. Paper [87] demonstrates the limitations of the passive clamping scheme-based DC-SSCB.

It is generally known that both single and multiple current impulses can cause MOVs to degrade. Moreover, for MOV-based voltage clamping circuits, the MOV's leakage current under the DC bus voltage has to be very small. Meanwhile, the power semiconductor's rated voltage should be higher than the MOV clamping voltage. Those limitations make the voltage utilization of the power semiconductor small. To solve those problems, [88] proposes an active MOV-RCD with an auxiliary switch. The typical active

MOV-RCD-based DC-SSCB is shown in Figure 2. 17. A novel voltage clamping circuit called the electronic MOV (eMOV) is proposed in [89] to increase the voltage suppression index (peak voltage / DC bus voltage) of the voltage clamping circuit and decrease the system conduction losses. eMOV is an active MOV+RC with the auxiliary break-over diode (BOD) and SCR to reduce the system conduction loss. BOD shares the dc bus voltage during the standby state. Meanwhile, SCR with its high pulse current capability provides fast fault current bypass by inserting the MOV into the circuit for fault current extinction Finally, the comparison among different voltage clamping is summarized in Table 2. 1.

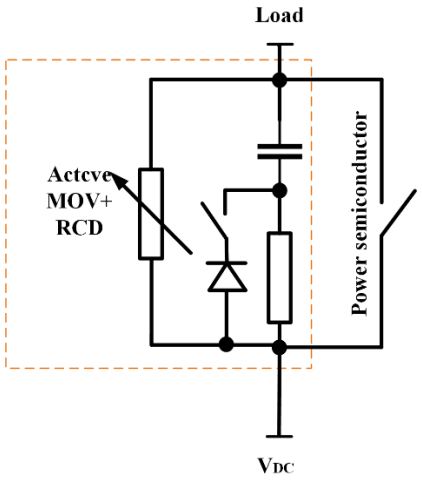


Figure 2. 17: Active MOV+RCD voltage clamping topologies for DC-SSCB.

Voltage clamping scheme	Advantages	Disadvantages
MOV	✓ Simple ✓ Cheap	• High *dv/dt* • MOV degradation
TVS	✓ Simple ✓ Fast response	• High *dv/dt* • Expensive
C	✓ Simple ✓ Cheap ✓ Low *dv/dt*	• Oscillation with system inductance • Absorb part of the residual energy • Not for high-power application
RC	✓ Simple ✓ Cheap ✓ Low *dv/dt*	• Absorb part of the residual energy • Additional voltage drop on the resistor • Not for high-power application

RCD	✓ Simple ✓ Cheap ✓ Low *dv/dt*	• Absorb part of the residual energy • Not for high-power application
MOV+RC	✓ Simple ✓ Low dv/dt	• Additional voltage drop on the resistor • The trade-off between *dv/dt* and response time • MOV degradation
MOV+RCD	✓ Simple ✓ Low dv/dt	• The trade-off between *dv/dt* and response time • MOV degradation
Active MOV+RCD	✓ Improve voltage utilization ✓ Reduce MOV degradation	• Complicated • Expensive
eMOV (Active MOV+RC+BOD)	✓ High voltage suppression index ✓ Less system conduction losses	• More Components • Complicated

Table 2. 1: Comparison of different voltage clamping schemes.

2.2.4 Fault detection circuit for SSCB

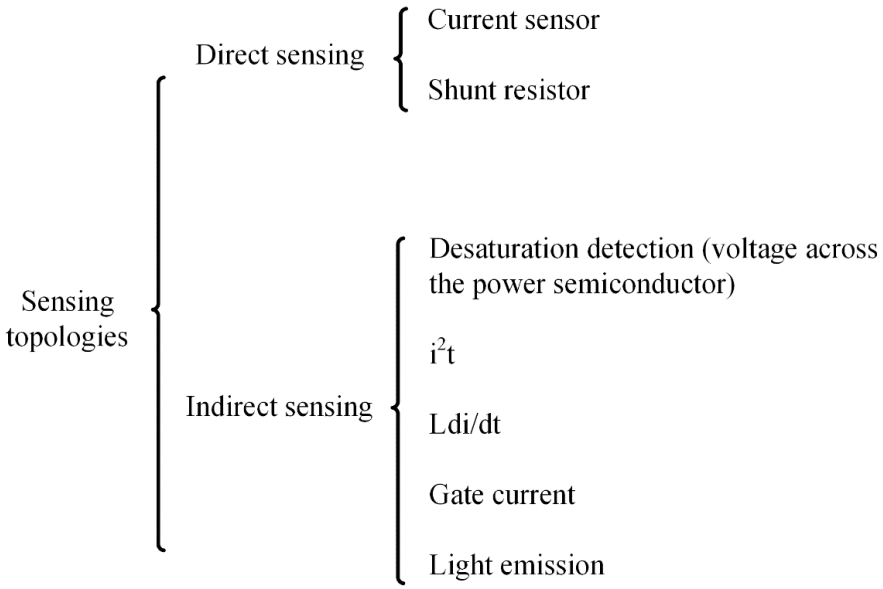


Figure 2. 18: Categorization of the fault current sensing technology for DC-SSCB.

The fault detection circuit is leveraged to detect the overcurrent event. In the worst scenario, the short-circuit point happens close to the DC-SSCB, which makes the system inductance almost zero, and the fault current increases very fast. Thus, the fault current sensing technology should have enough bandwidth and response time. Additionally,

considering that the DC-SSCB design is sensitive to efficiency, the related fault current sensing technology should be energy efficient. The common fault current sensing technologies are categorized in Figure 2. 18. The sensing technology can be categorized into direct sensing and indirect sensing. Direct sensing technology senses the system current directly to trigger the short-circuit protection, while indirect sensing technology leverages other short-circuit-related parameters (e.g., the voltage across the power semiconductor, fault current increasing ratio, etc.) to trigger the short-circuit protection.

2.2.4.1 Direct sensing

Direct sensing is the most common fault-sensing technology for DC-SSCB. The system's current can be directly sensed by the current sensor (e.g., giant magneto-resistive [90], hall-effect current sensor [91], etc.). However, the current sensor-based sensing topology increases the total cost of the DC-SSCB, and they may not have enough bandwidth when the system inductance is almost zero. And some current sensors are sensitive to ambient temperature (e.g., hall-effect current sensor). The shunt resistor current sensor is another convenient method to sense the system fault current [36]. It is easy to implement and can also have a fast response speed with a good design [92]. However, the voltage drop on the sensing resistor can cause extra power loss to the DC-SSCB.

2.2.4.2 Indirect sensing

For indirect sensing technologies, they do not need to face the high system fault current. They trip the protection by sensing the voltage across the power semiconductor, thermal performance, system current increasing ratio, etc.

Desaturation detection is a common indirect overcurrent detection method. It has already been applied to many commercial gate drive IC (e.g., ACPL-339J). The desaturation detection circuit senses the voltage across the on-state power semiconductor. When the current flowing through the power semiconductor increases, the voltage across the on-state power semiconductor will also increase with the system current. Once the detected voltage across the on-state power semiconductor is higher than the threshold voltage, the protection will be triggered. The desaturation detection has a fast response time and a mature circuit. However, it needs to be designed carefully for the trade-off between noise immunity and response time. Moreover, unlike direct sensing technology, desaturation protection will not be triggered on a fixed system fault current. Because the junction temperature and degradation state can influence the voltage across the on-state power semiconductor.

Ldi/dt is another indirect current sensing technology by adding an inductor in series with the power semiconductor [93]. Desaturation detection detects the voltage across the power semiconductor, while *Ldi/d*t detects the voltage across the power semiconductor plus the auxiliary inductor. Thus, *Ldi/dt* based sensing technology can take the system's current increasing ratio into account, which helps the *Ldi/dt* have a faster response time than the desaturation detection. However, it has the same drawbacks as desaturation detection.

There are also some other current sensing techniques. [79] leverages the gate current of reverse-conducting SiC JFET to detect the overcurrent event. Moreover, [94]

proposes an intensity of light-based overcurrent detection. Because the light emitted by the SiC JFET die is related to the value of the system's current.

Unlike the other sensing technologies, i^2t is another detection metric that protects the system from continuous overheating [95]. The other current sensing technologies can only trigger protection when detecting a high fault current. They cannot take any action for a continuous high system current (lower than the fault trigger level). But i^2t detection can protect the system from the thermal perspective. Finally, some typical system current sensing technologies are compared in Table 2. 2.

Sensing technology	Advantages	Disadvantages
Current sensor	✓ Simple ✓ Fixed trigger current ✓ No extra loss	• Temperature sensitive • Limited bandwidth • Expensive
Shunt resistor current sensing	✓ Simple ✓ Fast response	• Voltage drop and extra loss on the resistor • No galvanic isolation
Desaturation detection	✓ Simple ✓ Fast response ✓ No extra loss	• The trade-off between noise immunity and response time • Not fixed protection trigger current
Ldi/dt	✓ Simple ✓ Extra fast response ✓ No extra loss	• The trade-off between noise immunity and response time • Not fixed protection trigger current • Additional detection inductor
i^2t	✓ Thermal protection	• Need to cooperate with fast system current sensing technology

Table 2. 2: Comparison of typical system current sensing technologies.

2.2.5 System-friendly function

With the development of DC-SSCB, besides the basic function of DC-SSCB (e.g., fault current interruption), some other functions are also developed for DC-SSCB, e.g., soft start-up, fault location detection, fault current limiting, and soft reclosing.

As the system protection equipment, it is good for DC-SSCB to have the capability of fault location detection. The first DC-SSCB with a short-circuit fault location detection function is proposed in [32]. The proposed DC-SSCB has a unique PWM current limiting mode. In the PWM current limiting, an algorithm is proposed to calculate the short-circuit distance using the power line's per-unit inductance value by measuring the response of the voltage pulses injected into the DC power network. Moreover, the paper [96] also proposes a new topology for DC-SSCB, which can determine the fault location by injecting signals into the isolated power line with short-circuit fault.

Besides the fault location detection function, the current limiting function is also important for DC-SSCB. For example, it is good to enable the DC-SSCB with an inrush current limitation function during the system start-up. A segmented resistor current limiting module is leveraged to restrict the fault current's increasing rate in [97]. The blocking capacitor absorbs the system's fault current. And the DC blocking circuit can quickly reduce the system's fault current to a safe level. The paper [98] presents a new topology for DC-SSCB with the system's current limitation function without any negative impact on the normal operation of DC-SSCB. Moreover, a peak current protection control is demonstrated in [99] to limit the system fault current by a comparator-based analog circuit to control the auxiliary switch.

It is important for DC-SSCB to distinguish the overcurrent and short-circuit to improve the reliability of DC-SSCB. Paper [100] proposes a digitally controlled current-time profile-based DC-SSCB for overcurrent protection and short-circuit protection. The

proposed current-time profile can help DC-SSCB avoid the fault triggered by the inrush current caused by the power electronics system's start-up.

Finally, reclosing is another important function of DC-SSCB to recover the system after the fault. To reduce the repetitive voltage and current stress on the DC-SSCB, [101] proposes a DC-SSCB with a soft reclosing function.

2.3 Summary

Finally, Table 2. 3 summarizes the state-of-the-art of low-power and high-power DC-SSCB in the last five years. The power semiconductor, power rating, interruption capability, connection type, energy absorption way, efficiency, application, and features are listed in the table. It can be found that the research of DC-SSCB has several trends.

1) Because of the low on-state resistance, the WBG has gradually become the mainstream of the DC-SSCB's main switch.

2) A mixture of power semiconductors-based topology is becoming attractive. Because it can leverage the advantages of different semiconductors.

3) The modular DC-SSCB, which can be connected in parallel or series, is an important piece of equipment for the future MVDC.

4) The advanced voltage clamping and energy absorption circuit is one of the key factors to enhance the performance of DC-SSCB.

5) With the help of power electronics technology, DC-SSCB can possess some other system-friendly functions.

Low power									
Paper	Date	Power semiconductor	Power rating	Interruption capability	Connection type	Energy absorption	Efficiency	Application	Features
[61] USA	08/2022	Thyristor SK655KD	200V/12A	120A	Y-type	MOV	99.79%	N/A	Fast commutation; Reliable MOVopearion; Reliable reclosing and rebreaking
[102] USA	03/2022	SCR 40TPS12A	400V/7A	20A	H-bridge	MOV	N/A	LV/MVDC	Modular extension; Pre-fault interruption
[88] USA	10/2022	SiC MOSFET C3M0016120D	720V/100A	183A	Single device	MOV-RCS; Active MOV-RCD	99.97%	N/A	Two novel active snubbers
[103] Mexico	5/2021	GaN FETs TP65H035WSQA	180V/3A	20A	Two series GaN	RCD	N/A	AC/DC low-power system	Voltage overshoot suppression; Detect and process fault in 282ns
[67] India	6/2021	SCR 40TPS12	120V/3.5A	48A	Modified Z-Source	N/A	N/A	N/A	Solve the problems of the traditional Z-source SSCB
[104] USA	6/2021	SiC MOSFET C3M0016120D	600V/ N/A	164A	Single device	Active MOV +RC	N/A	N/A	Select the clamping voltage of MOVs close to the nominal voltage of the dc system
[104] USA	3/2021	Thyristor+IGBT	600V/5A	45A	Series IGBT and thyristor	MOV	N/A	N/A	A novel SSCB based on mixture device
[105] USA	11/2020	GaN FET TP90H050WS	380V/20A	70A	Two series paralleled GaN	RC	99.95%	Datacenter	Intelligent DC-SSCB with three operation modes
			1000V/10A	70A				EV charging	
[96] China	11/2018	IGBT	200V/15A	30A	Series IGBT+LCR	N/A	N/A	N/A	Fault Location Function
[50] China +USA	8/2018	SiC MOSFET C2M0045170D	1200V/ N/A	75A	Two series SiC MOSFET	MOV+RC	N/A	N/A	A single isolated gate driver for multiple devices
High power									
[106] USA	10/2022	SiC MOSFET CAB450M12XM3	4kV/100A	1kA	Parallel and Cascade module	MOV-RCD	99.98%	MVDC	Modular SSCB economic analysis; Parallel and cascade scalability
[107] China	10/2022	SiC JFET UJN1205K	5kV/63A	63A	Cascade module	MOV-RC	N/A	MVDC	Single-gate drive; Active clamp control strategy
[56] China	10/2022	Multi IGCT	8kV/ N/A	7kA	Series v-IGCT and i-IGCT	Oscillation branch + MOV	N/A	MVDC	Oscillating-commutation; Compound IGCTs
[108] China	3/2022	Thyristor+IGBT	500V/5A 5kV analysis	60A	Full-bridge mixture SSCB	MOV	N/A	MVDC	Fewer components for bidirectional mixture DC-SSCB

[109] USA	12/2021	SiC MOSFET	1kV/500A	1.8kA	Series SiC module	TVS	99.51%	Electrified aircraft propulsion	Development procedure
[80] Norway	12/2021	Si IGBT	3kV/ N/A	56A	Series IGBT	MOV+RCD	N/A	MVDC	Novel voltage-balancing scheme
[41] USA	2/2021	RB-IGCT	1kV/5kA	10kA	two parallel RB-IGCT	MOV	99.9%	Marine power system	Optimized busbar design; High efficiency; High power
[96] USA	4/2018	SiC ETO	4.5kV/200A	200A	Parallel ETO	MOV	N/A	MVDC	ETO potential for SSCB

Table 2. 3: DC-SSCB state-of-the-art.

CHAPTER THREE

3 DESIGN OF A FAST, LIGHTWEIGHT DC-SSCB

3.1 Introduction

The electrified aircraft propulsion (EAP) system is critical for commercial transport aircraft to improve fuel efficiency, emissions, and noise levels. Naturally, to reduce the total weight of the electric power system, the medium voltage direct current (MVDC) system becomes a suitable and promising power configuration for the EAP system. In some cases, the system inductance can be small, and the short circuit fault circuit can increase to an extremely high value in several microseconds. It makes the power electronics-based MVDC EAP system more fragile. Moreover, the developing EAP system depends on the power electronics-based system, and rapid protection system is essential due to the nature of the power electronics converter. Unlike the AC system breaker, the DC system breaker can't clear the fault at the zero-crossing point. For the safety and reliability operation of the system, there should not be an electric arc during the current interruption process for the DC breaker. Therefore, a rapid and reliable DC protection system is vital to the DC EAP system. As the critical component of the DC protection system, the DC solid-state circuit breaker (DC-SSCB) enables the safe and reliable operation of the EAP system.

Traditionally, as illustrated in Figure 3. 1, to limit the peak value of the system fault current, the current limiting inductor is used in the DC-SSCB, which is bulky and heavy. For electrified aircraft, it is always beneficial to load more cargo or increase the cruising range by decreasing the total weight of the EAP system. However, the current limiting

inductor-based traditional DC-SSCB is so heavy for electrified aircraft. Accordingly, a lightweight DC-SSCB can play an essential role in electrified aircraft.

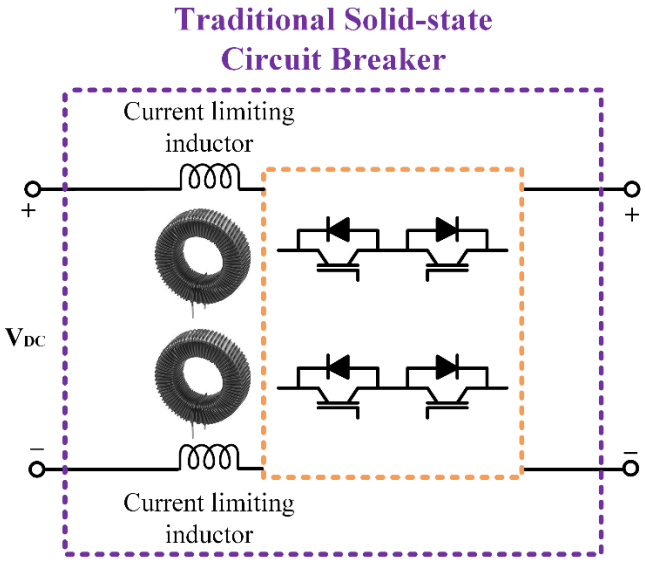


Figure 3. 1: Topology of the traditional bidirectional DC-SSCB.

3.2 Topology of DC-SSCB without current limiting inductor

Figure 3. 2 illustrates the proposed limiting inductor-free two-pole bidirectional DC-SSCB. Compared with the traditional DC-SSCB, the proposed DC-SSCB abandons the current limiting inductor, which makes DC-SSCB lighter and smaller.

The proposed DC-SSCB consists of power semiconductor switches, gate drives for power semiconductors, and energy absorption circuits. The power semiconductor switches are used to interrupt the short circuit fault current. During regular operation, the power semiconductors are in an ON state; when the short circuit fault is detected, the power semiconductors will be turned off to interrupt the fault current. In this chapter, IGBT will be used as the power semiconductor. The gate drive is the critical component of the DC-

SSCB. It detects the short circuit fault and controls the power semiconductor to turn on or off. During the fault current interruption period, the energy absorption circuit clamps the DC bus voltage and absorbs the extra energy. Metal oxide varistor (MOV), transient voltage suppressor (TVS) diode, and RC snubber circuit are good candidates for the energy absorption circuit. The selection of the energy absorption circuit depends on the application demand. In this chapter, MOV will be used as the energy absorption circuit.

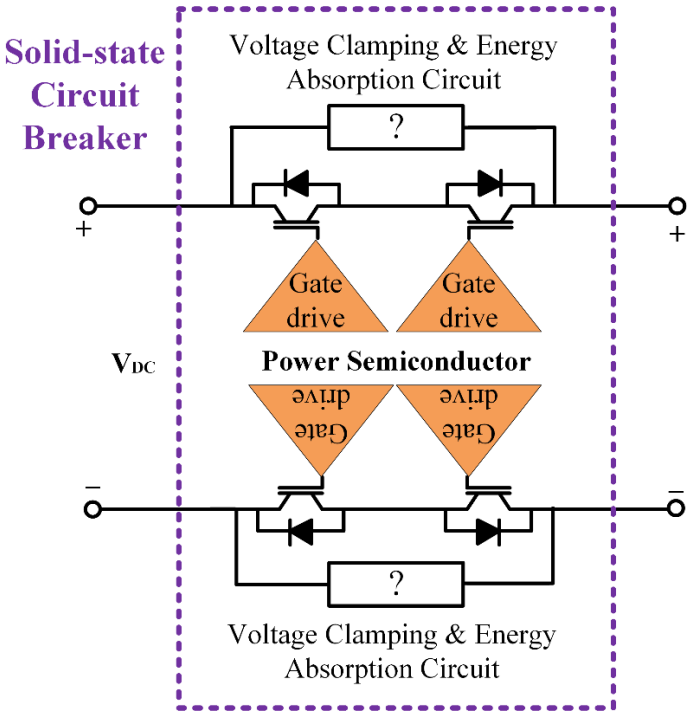


Figure 3. 2: Topology of the proposed two-pole bidirectional DC-SSCB.

For such a DC-SSCB without a current-limiting inductor, the *i-v* output characteristics of the power semiconductor switch are utilized to limit the peak fault current. As illustrated in Figure 3. 3, taking the IGBT as an example, it can operate in the saturation, active, and cut-off regions. When the IGBT operates in the active region, the collector current i_C can be limited by the IGBT *i-v* characteristics. Thus, when a short circuit occurs,

the high fault current forces the power semiconductor device to operate in the active region to limit the system fault current. Additionally, the saturation current of the IGBT I_{sat0}, I_{sat1}, and I_{sat2} are related to the gate-emitter voltage v_{GE}, which means that the current limitation level of the DC-SSCB can be tuned by v_{GE}.

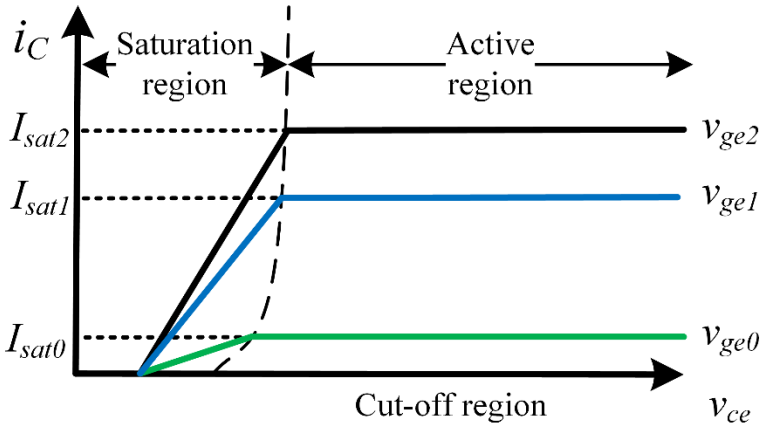


Figure 3. 3: V-I curve of the IGBT.

3.3 Gate drive design for the proposed SSCB

The gate drive is the brain of the proposed DC-SSCB. For the proposed DC-SSCB, short circuit fault detection is completed by the gate drive. And the gate drives turn off the semiconductor when the fault is detected. Gate drives also maintain the on-state of the power semiconductor during regular operation. Because of the different application scenarios, compared with the traditional gate drive for pulse-width modulation (PWM)-based power converter operation, the requirements of gate drive design for DC-SSCB are different.

3.3.1 *Overview of the gate drive circuit*

Figure 3-4 illustrates the simplified schematic of the gate drive circuit for DC-SSCB. It includes seven main functional blocks: isolated power supply, signal isolator, gate drive integrated circuit (IC), gate resistor, desaturation detection, soft turn-off, and decoupling capacitor. The rest of this section will demonstrate the details of those functional blocks and compare the varieties between the gate drive design for the PWM-based power converter and DC-SSCB. In this section, a 3300V 1000A IGBT FZ1000R33HE3 from Infineon is selected as the device under test (DUT) for DC-SSCB.

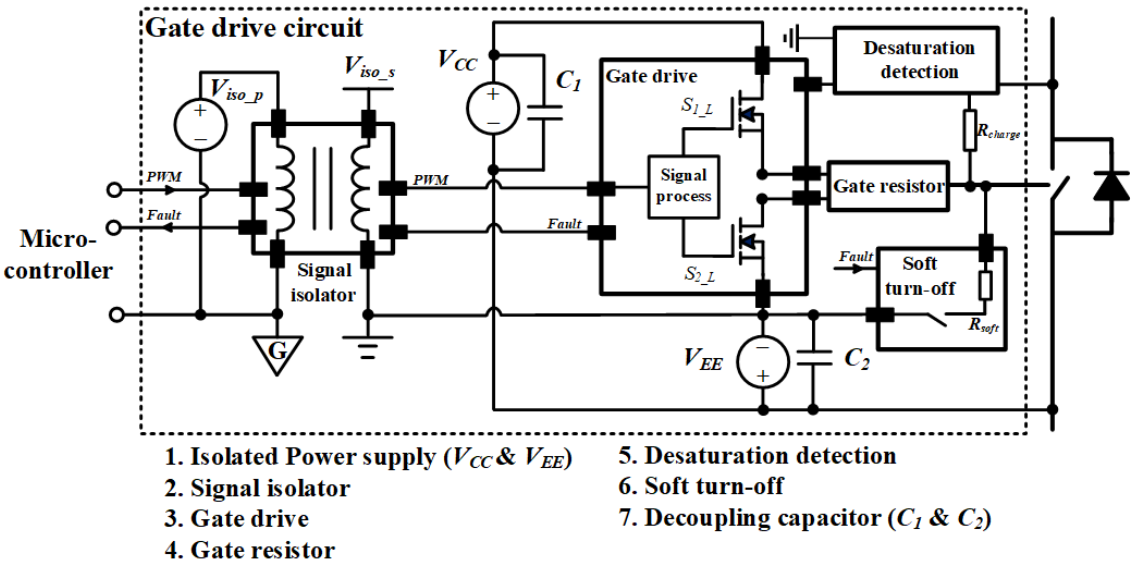


Figure 3. 4: Simplified schematic of the gate drive circuit for DC-SSCB.

3.3.2 *Isolated power supply*

The isolated power supply offers the essential isolation and voltage required for the gate drive circuit to operate. Additionally, it provides the necessary voltage and power for turning the power semiconductor in DC-SSCB on and off. Note that the low-dropout (LDO)

linear regulators are often adopted to adjust the output voltage of the isolated power supply to best serve the corresponding power semiconductor.

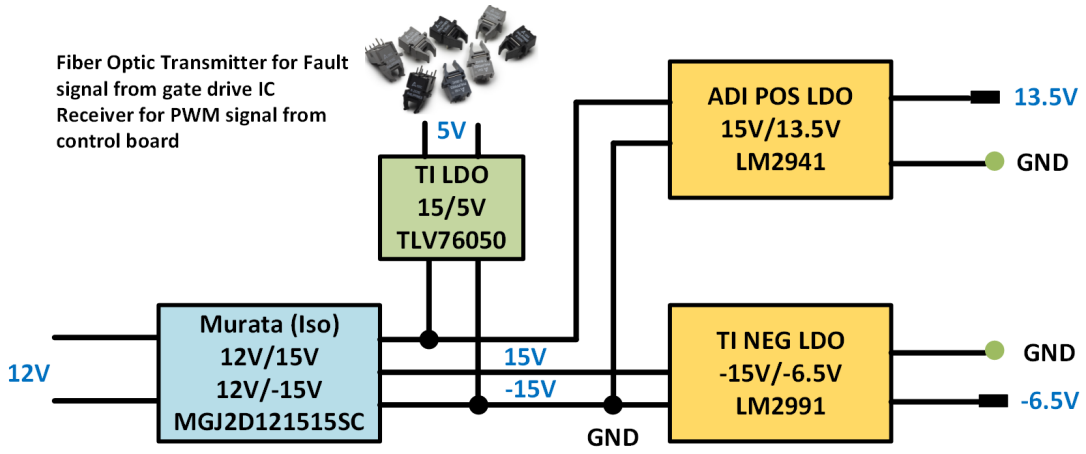


Figure 3. 5: Power supply configuration.

Figure 3. 5 illustrates the power supply design with 12V input (typical voltage in hybrid-electric propulsion). It includes one isolated power supply and multiple LDOs to provide suitable voltage for different purposes.

The design of the isolated DC-DC converter is described below:

Step 1: Determine the required galvanic isolation capability V_{iso_ips} based on the power semiconductor's (Infineon FZ1000R33HE3) breakdown voltage V_{BD_semi}. Also, note the high-altitude application for the EAP system would induce additional isolation requirements (e.g., partial discharge).

$$V_{iso\_ips} > V_{BD\_semi} = 3300V \tag{3. 1}$$

Step 2: Determine the required common mode transient immunity (CMTI) based on the estimated *dv*/*dt*. Most isolated power supply datasheets provide input-to-output capacitance rather than CMTI. Thus, a low input-to-output capacitance is an equivalent

indicator of strong CMTI capacity. The requirement for the DC-SCCB application could be less restrictive since only one *dv/dt* event occurs under the fault condition with a relatively slow slew rate for the sake of overvoltage mitigation. According to the datasheet of the power semiconductor (Infineon FZ1000R33HE3), the CMTI of the isolated power supply should meet:

$$CMTI > \max(\frac{dv}{dt}(on), \frac{dv}{dt}(off)) = \max(\frac{1800V}{0.21\mu s}, \frac{1800V}{0.78\mu s}) = 8.57kV/\mu s \quad (3.2)$$

Step 3: Determine the output voltage based on the required driving voltage of the power semiconductor. In most cases, the output voltage of the isolated power supply is not the same as the necessary driving voltage of the power semiconductor. Then additional LDOs should be introduced. Based on the characteristics of FZ1000R33HE3, +15V and -15V are selected as the positive and negative outputs of the isolated power supply.

Step 4: The circuit configuration in Figure 3. 5 determines the output power requirement of the isolated power supply. In the design, the isolated power supply for the gate drive circuit has positive and negative outputs, i.e., V_{CC} (+15V) and V_{EE} (-15V), respectively. Thus, the power requirement of the isolated power supply is separated into two parts.

For VCC, it provides power for the one fiber receiver (control signal), one fiber transmitter (fault signal), gate drive IC, and power dissipated during the switching transition.

$$P_{pos} > P_{iso} + P_{gd\_pos} + P_{sw\_pos} \quad (3.3)$$

where P_{iso} is the power dissipation of fiber optics-based signal isolator along with extra loss induced by LDO; P_{gd_pos} is the power consumed by the gate driver IC; P_{sw_pos} is the

power dissipated during the switching transition. The selection of the fiber optics-based signal isolator (transmitter AFBR-1624Z and receiver AFBR-2624Z) and gate drive IC (ACPL-339J) will be demonstrated in the rest of this section.

P_{iso} is the combination of power loss on fiber optic receiver P_{rec} for PWM signal and power loss on fiber optic transmitter P_{trans} for fault signal. Considering that it is less likely to have a fault signal, P_{trans} can be neglected.

$$P_{iso} = P_{rec} + P_{trans} = f_{LDO} * V_{iso} * \frac{V_{iso}}{R_{gd-rec}} + 0 = 3 * 5 * \frac{5}{287 + 143} = 0.178W \quad (3.4)$$

where f_{LDO} is the factor of the extra loss induced by LDO (input voltage/output voltage = 15/5 = 3); V_{iso} is the fiber optics-based signal isolator input power voltage; $R_{gd\text{-}rec}$ is the resistance between gate drive IC and receiver.

Because gate dive IC needs to produce the fault signal for DC-SSCB, and drive the power semiconductor with V_{CC} and V_{EE}. P_{gd_pos} consists of power loss on the fault signal output P_{gd_fault} and power loss for V_{CC} P_{gd_VCC}.

$$P_{gd\_pos} = P_{gd\_fault} + P_{gd\_VCC} = f_{LDO} * V_{gd} * i_{gd\_fault} + V_{CC} * i_{CC} = 3 * 5 * 0.0025 + 15 * 0.012 = 0.184W \quad (3.5)$$

where V_{gd} is the gate drive IC input power voltage; i_{gd_fault} is the fault logic output current; i_{CC} is the output supply current of V_{CC}.

In most cases, the IGBT in the proposed DC-SSCB is in the on-state. The IGBT will turn off only when the circuit detects the fault. Thus, the P_{sw_pos} is negligible.

$$P_{sw\_pos} = 0W \quad (3.6)$$

The negative output provides the power for the gate drive IC and the dissipated power during the switching transition.

$$P_{neg} > P_{gd\_neg} + P_{sw\_neg} = V_{EE} * i_{EE} + 0 = 15 * 0.011 + 0 = 0.165W \quad (3.7)$$

where P_{gd_neg} is the power consumed by the gate driver IC for V_{EE}; P_{sw_neg} is the power dissipated during the switching transition, and i_{EE} is the output supply current for the gate drive IC of V_{EE}.

Step 5: Select an isolated power supply to meet the abovementioned requirements. This design selects a Murata Power Solutions MEJ2 series DC/DC converter and several LDOs.

First, to provide isolation between the control signal and the power, the isolated MGJ2D121515SC is selected. The MGJ2D121515SC has two outputs: one is 15V output for V_{CC}, and the other is -15V for V_{EE}.

Then, to make the gate driver more flexible for different turn-on/-off driving voltage, a positive LDO (LM2941) and a negative LDO (LM2991) are connected with the +15V and -15V, respectively.

Finally, it needs to be noted that the fiber optic transmitter and receiver are utilized in this design to transmit the PWM signal and the fault signal between the controller and the gate drive. The transmitter power of the fault signal from the gate drive IC and the receiver power of the PWM signal from the control board are provided by the secondary side of the MGJ2D121515SC. Two LDOs with the part number of TLV76050 are used to provide the 5 V outputs to the transmitter and receiver, respectively.

Since the gate drive is designed for DC-SSCB applications, as discussed above, the CMTI requirement of the power supplies is not the primary design concern. The following table summarizes the details of the power supply design.

Part	Manufacturer	Part Number	Output Voltage 1	Output Voltage 2	Isolation Capacitor	Power	Input Voltage	Current Max
12/15V& -15V isolated power supply	Murata	MGJ2D121515SC	15 V	-15 V	4 pF	2 W	12 V	67 mA
Positive LDO	TI	LM2941	Adjustable		N/A	3.6 W	3 to 18 V	1A
Negative LDO	TI	LM2991	Adjustable		N/A	3 W	3 to 18 V	1 A
12/5V and 15/5V power supply	TI	TLV76050	5 V		N/A	0.5W	0 to 30 V	100 mA
Overall needed power: 527mW Needed power from the positive output of the isolated power supply: 362mw Needed power from the negative output of the isolated power supply: 165mW								

Table 3. 1: Design summary of power supply.

3.3.3 Signal isolator

The signal isolator provides the galvanic isolation between the microcontroller's ground and the gate drive's ground. It ensures the signal transmission between the microcontroller and the gate drive is safe and reliable.

The design of the signal isolator is described below:

Step 1: Determine the required galvanic isolation capability V_{iso_sig} based on the power semiconductor's (Infineon FZ1000R33HE3) breakdown voltage V_{BD_semi}. For DC-SSCB, when the fault is detected, during the turn-off process of the power semiconductor, the over-voltage across the power semiconductor makes the potential difference across the

signal isolator higher than the system DC bus voltage. Accordingly, the signal isolator's galvanic isolation capability must be greater than the system DC bus voltage.

$$V_{iso\_sig} > V_{BD\_semi} = 3300V \tag{3. 8}$$

Step 2: Determine the required CMTI based on the estimated *dv*/*dt*. In the design of PWM-based converters, CMTI is a crucial selection criterion for the signal isolator. The requirement for the DC-SSCB application could be less restrictive since only one *dv/dt* event occurs under the fault condition with a relatively slow slew rate for the sake of overvoltage mitigation. According to the datasheet of the power semiconductor (Infineon FZ1000R33HE3), the CMTI of the signal isolator should meet:

$$CMTI > \max(\frac{dv}{dt}(on), \frac{dv}{dt}(off)) = \max(\frac{1800V}{0.21\mu s}, \frac{1800V}{0.78\mu s}) = 8.57kV/\mu s \tag{3. 9}$$

Step 3: Select a signal isolator to meet the requirements discussed above. The fiber optic transmitter AFBR-1624Z and receiver AFBR-2624Z from Broadcom are used in this design.

Step 3: Select a signal isolator to meet the requirements discussed above. The fiber optic transmitter AFBR-1624Z and receiver AFBR-2624Z from Broadcom are used in this design. It's also essential to consider the signal's transmission frequency range, propagation delay, and signal isolator distortion. Specifically, maximum and minimum signal transmission frequencies have to satisfy the required switching frequency range of PWM-based converters, which is not a limitation for the DC-SSCB application since the turn-off event of the IGBT occurs only under the fault condition. The signal isolator's propagation

delay and distortion should be sufficiently small to prevent adding unacceptable reaction latency. For the DC-SSCB application, these two selection criteria are relatively easy to meet.

Step 4: Select a signal isolator to meet the requirements discussed above. The fiber optic transmitter AFBR-1624Z and receiver AFBR-2624Z from Broadcom are used in this design.

As illustrated in Figure 3. 6, two fiber optics are adopted on the gate drive: one for the PWM control signal and the other for the short circuit fault signal. The PWM signal transmits from the fiber optic transmitter on the micro-controller to the fiber optic receiver on the gate drive board; the short circuit fault signal transmits from the fiber optic transmitter on the gate drive board to the fiber optic receiver on the micro-controller. The parameters of the selected fiber optics are summarized in Table 3. 2.

Part Number	Max. frequency	Max. isolation working voltage	CMTI	Propag. delay
AFBR-2624Z	50 MBd	high	> 100 V/ns	30 ns
AFBR-1624Z	50 MBd	high	> 100 V/ns	30 ns

Table 3. 2: Design summary of the isolator.

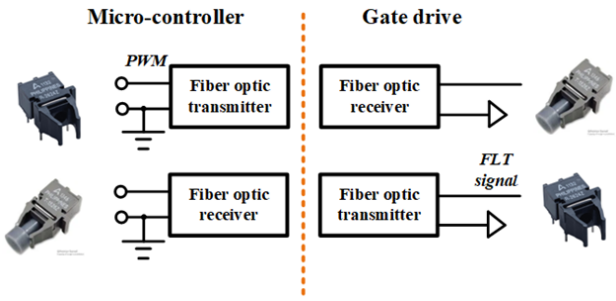


Figure 3. 6: Signal isolator configuration.

3.3.4 Gate drive IC and related buffer circuit

The gate driver IC offers the required voltage to turn on and turn off the power semiconductor, the required current to charge and discharge the input capacitance of the power semiconductor, and the low pull-up/down resistance with quick response for rapid switching.

In this design, ACPL-339J from Avago is selected. The pin names and the circuit diagram of the ACPL-339J gate drive IC are illustrated in Figure 3. 7. "VCC1" is the positive input supply voltage, and "VCC2" is the positive output supply voltage. "VEE" is the negative output supply voltage, and "VE" is a common (IGBT emitter) output supply voltage. "Fault" changes from logic low to high output once the voltage on the DESAT pin exceeds an internal reference voltage of 8 V (with reference to VE). "DESAT" is desaturation voltage input. Specifically, when the voltage on DESAT exceeds an internal threshold voltage (8 V in this case) during the on-state of the power electronics, FAULT, and VGMOS pins are changed from the logic low to the high state. Table 3-3 shows the details of the selected gate drive IC. Note that the VGMOS pin could be used to enable the soft-turn-off circuit.

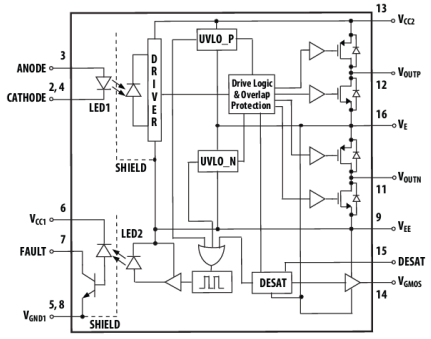


Figure 3. 7: Circuit diagram of gate drive IC.

Part Number	Propagation delay	VCC Range	Peak output current	DESAT Threshold	Pull-up/-down resistance (min)	power dissipation
ACPL-339J	100-300 ns	15-30 V	1 A	8 V	1.5 Ω	600 mW

Table 3. 3: Design summary of gate drive IC.

For power semiconductors with high-power applications, the gate drive IC's driving capability may be insufficient. Thus, an additional current buffer circuit is essential to improve the gate drive circuit's driving capability.

The design of the signal isolator is described below:

Step 1: The voltage rating V_{buffer} should be higher than the gate voltage.

$$V_{buffer} > V_{CC} - V_{EE} = 30V \tag{3. 10}$$

Step 2: The sinking/sourcing current capability I_{buffer} should be higher than the maximum gate current. In this case, we only consider the inner gate resistance $R_{g(inner)}$ for R_{g_total} to leave some margin.

$$I_{buffer} > I_{g\_\max} = \frac{V_{CC} - V_{EE}}{R_{g(inner)}} = \frac{30}{0.75} = 40A \tag{3. 11}$$

Step 3: The pull-up/-down resistance R_{buffer} should be smaller than the internal gate resistance of the power semiconductor.

$$R_{buffer} < R_{g(inner)} = 0.75\Omega \tag{3. 12}$$

Accordingly, in the design, Vishay Semiconductors SI4564DY is selected. Table 3. 4 shows the details of the current buffer specified in this gate drive design.

Part Number	Drain-Source Breakdown Voltage	Type	I_D (Pulsed)	$Q_{g.max}$	$R_{DS(on)}$ N, P	Gate resistance
Si4564DY	+40 V/-40 V	P-N MOSFET Bridge	40 A	63 nC	20, 28 mΩ	0.3 Ω/ 1.3 Ω

Table 3. 4: Design summary of the selected current buffer.

3.3.5 Gate resistor

The switching speed is under the control of the gate resistor. In this section, the gate resistor refers to the external resistor, and the user can tune it.

For a PWM-based converter, the design of the gate resistor is a trade-off among switching stress, switching speed, and switching loss. For the DC-SSCB application, gate resistance design is less critical than the PWM-based converter since the power semiconductor remains on-state during regular operation.

Power rating design is also essential to the gate resistor. For a PWM-based converter, the power the isolated power supply provides to drive the power semiconductor is dissipated by the gate resistor, which means that the power rating of the gate resistor should be higher than the power dissipated during the switching transition. In the DC-SSCB application, this design criterion is not critical since the power semiconductor remains on-state during regular operation.

With the help of the gate drive IC and current buffer, the turn-on and turn-off gate resistor can be designed separately to control the turn-on/-off speed of the power semiconductor. The turn-on gate resistor connects with the current buffer's P MOS source terminal; the turn-off gate resistor connects with the current buffer's N MOS drain terminal. Table 3. 5 illustrates the detail of the turn-on/-off gate resistor.

Manufacturer	Part Number	Resistance	Power Rating	Temp Coefficient	Tolerance	Operating Temp
Vishay	MMB02070C1009FB200	10 Ω	1 W	+50 ppm/°C	±1%	-55 °C ~ 155 °C

Table 3. 5: Design summary of the turn-on/-off gate resistor.

3.3.6 Desaturation protection

The principle of desaturation protection is to leverage the power semiconductor's (IGBT in this section) desaturation characteristics for detecting the overcurrent and short circuit faults by sensing the increased collector-emitter voltage v_{CE}. Then the fault is cleared by turning off the IGBT gently.

The desaturation protection is based on the V-I curve characteristic of the IGBT shown in Figure 3. 3. During normal operation, IGBT keeps the on-state to let the load current flow through. In this scenario, IGBT works in the saturation area with a low on-state v_{CE} (related to IGBT on-state conduction resistance). Once the fault happens, IGBT is forced to move from the saturation area to the active area by the short-circuit current. Meanwhile, v_{CE} rises quickly, and the short current can be limited to the desaturation current I_{desat}, which relies on v_{GE}. Therefore, with the help of the V-I curve characteristic of the IGBT, the fault current can be clamped to I_{desat}. And I_{desat} can also be tuned by v_{GE}. Lastly, based on the V-I curve, v_{CE} is highly sensitive to the overcurrent, especially when IGBT enters the active area. Accordingly, v_{CE} can be leveraged to detect the short circuit fault.

For the DC-SSCB, under normal operating condition, gate drive logic input is always high to maintain the IGBT on-state. v_{CE} is online monitored by the desaturation detection circuit and compared with the preset v_{CE} protection threshold V_{thre} of the gate drive IC ACPL-339J. V_{thre} is preset by the gate drive IC to enable desaturation protection under the fault condition when v_{CE} rises to the boundary between the saturation region and

the active region of IGBT V_{CETH}. The detail of the desaturation detection circuit is illustrated in Figure 3. 8.

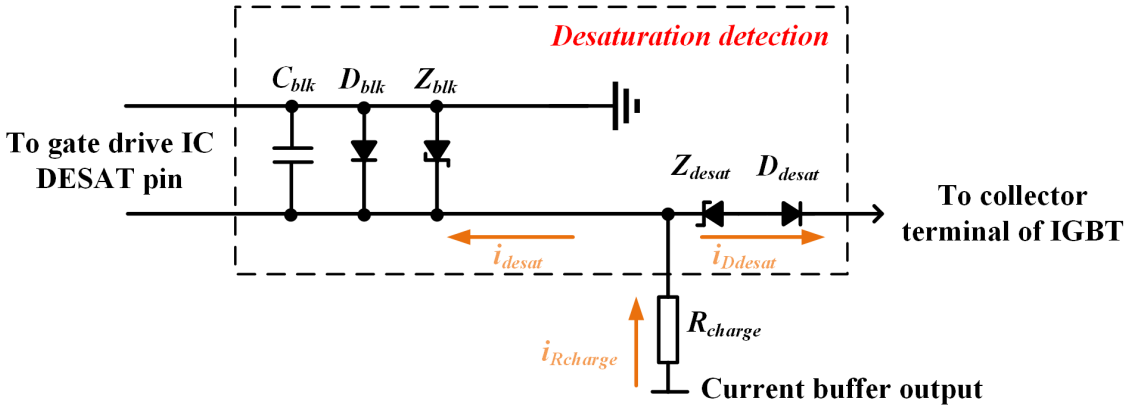


Figure 3. 8: Schematic of the desaturation detection circuit.

v_{CE} detection circuit comprises v_{CE} sensing diode D_{desat}, Zener diode Z_{desat}, v_{CE} related resistor divider R_{blk1} and R_{lk2}, charing resister R_{charge}, blanking capacitor C_{blk}, and gate drive "DESAT" pin protection diode D_{blk} and Z_{blk}.

Sensing diode D_{desat} will be forward biased to sense the v_{CE} when the IGBT is on, while reverse biased to block the dc bus voltage when the IGBT is off. Z_{desat} is introduced to adjust the gate drive IC DESAT pin voltage approaches the protection threshold V_{thre} when v_{CE} rises to the boundary between the saturation region and the active region of IGBT.

The blanking capacitor C_{blk} is charged by the V_{CC} from the current buffer through the charge resistor R_{charge} to provide the blanking time during the turn-on transition and is utilized to immune the noise from the power stage during the operation. In parallel with C_{blk}, the Schottky diode D_{blk} prevents the substrate diode of the gate drive optocoupler from being forward biased to avoid the negative voltage across the "DESAT" pin, while the

Zener diode D_{z_blk} is used to clamp any positive voltage spike across the gate drive IC DESAT pin.

The design of the desaturation detection circuit is described below:

Step 1: Z_{desat} for v_{CE} sensing adjustment circuit. It is important to determine V_{CETH} based on the V-I curve of IGBT FZ1000R33HE3. As shown in Figure 3. 9, V_{CETH} is about 6.5V when v_{GE} is 12V.

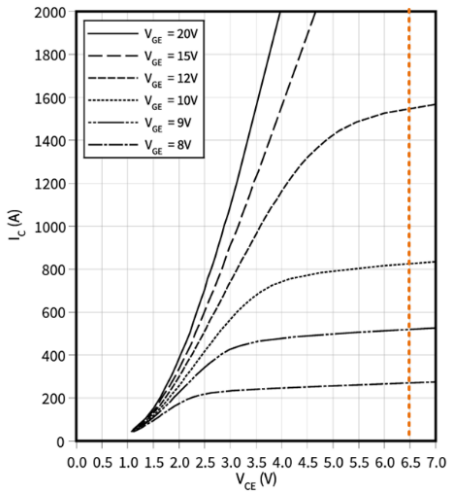


Figure 3. 9: The V-I curve of FZ1000R33HE3.

According to the operation principle of the desaturation protection, once v_{CE} approaches V_{CETH}, V_{Cblk} should be equal to V_{thre}, which is 8V for the selected gate drive IC ACPL-339J, then the protection is tripped. Assuming that the forward voltage of the D_{desat} V_{f_Ddesat} is 1V and Z_{desat} is leveraged to adjust V_{CETH}, V_{zdesat} can be calculated as:

$$V_{zdesat} = V_{thre} - V_{f\_Ddesat} - V_{CETH} \approx 8 - 1 - 6.5 = 0.5V \quad (3.\ 13)$$

Considering that 0.5V is relatively small for the Zener diode, there is no need for Z_{desat} to adjust V_{CETH}. Additionally, when v_{GE} is higher than 12V, V_{CETH} is higher than 4.5V,

and the current design makes the protection more sensitive. However, relatively sensitive protection is not bad for DC-SSCB.

Step 2: Select C_{blk} and R_{charge}.

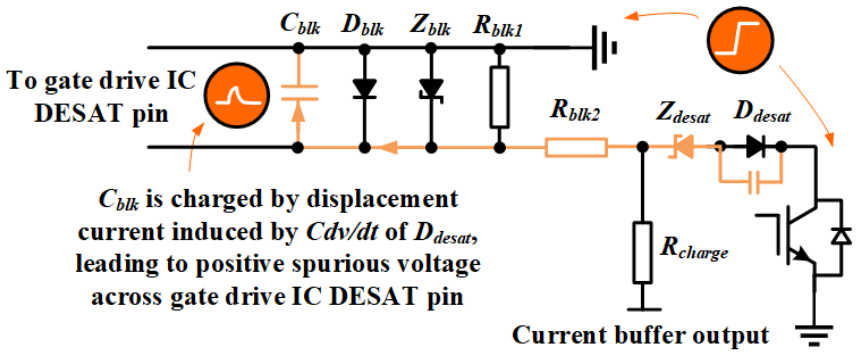


Figure 3. 10: Desaturation detection's displacement current during turn-off transient.

To ensure the fast reaction of short circuit protection, the capacitance should be sufficiently low. More specifically, to make IGBT's short-circuit withstand time (SCWT) longer than the response time of protection, the time constant τ_{vcs} for the C_{blk} charging circuit is expected to be sufficiently small. Based on the RC charging loop (C_{blk} and R_{charge}), the τ_{vcs} for the C_{blk} charging circuit can be expressed as (during the calculation, the junction capacitance of D_{blk} and Z_{blk} should also be involved in C_{blk}):

$$\tau_{vcs} = R_{charge} \times C_{blk} \tag{3. 14}$$

Then the blanking time (charging C_{blk} to V_{thre} to trigger the protection) is derived:

$$t_{blk} = \tau_{vcs} \ln\left(\frac{V_{CC}}{V_{CC} - V_{thre}}\right) < SCWT \tag{3. 15}$$

To lessen the harmful effects of D_{desat} displacement current and reverse recovery current during *dv/dt* (as shown in Figure 3. 10), C_{blk} should be significantly greater than the D_{desat}'s junction capacitance. Considering 5pF junction capacitance for D_{desat}, a 6800pF blanking capacitor is selected to ensure more than 1000x difference for enhanced noise immunity.

Assuming the blanking time is 2.7µs, and the capacitance of C_{blk} is 6800pF, R_{charge} needs to be 520Ω.

Step 3: Select D_{desat}.

Considering that the breakdown voltage of FZ1000R33HE3 is 3300 V, based on the conservative assumption, the breakdown voltage of D_{desat} should be similar.

The current rating should be designed based on the calculation below.

The charging current is calculated as:

$$i_{Rcharge} = \frac{V_{CC} - V_{f\_Ddesat} - V_{zdesat} - v_{CE}}{R_{charge}} = \frac{V_{CC} - 1 - 0 - v_{CE}}{520} = \frac{V_{CC} - 1 - v_{CE}}{520} \quad (3.\ 16)$$

Accordingly, the current through sensing diode D_{desat} is expressed as:

$$i_{Ddesat} = i_{Rcharge} - i_{desat} = \frac{V_{CC} - 1 - v_{ce}}{520} \quad (3.\ 17)$$

Thus, considering the lowest v_{CE}, i.e., 0.75 V knee voltage of FZ1000R33HE3 and the highest VCC, i.e., 15V for FZ1000R33HE3, the maximum current of the sensing diode is

$$i_{Ddesat} = \frac{15 - 1 - 0.75}{520} = 25mA \tag{3. 18}$$

Accordingly, a 3300V GeneSiC GAP3SLT33-220FP SiC Schottky diode with 5pF junction capacitance is selected and summarized in Table 3. 6. And there is no need to adjust the sensed v_{CE}.

Part	Manufacturer	Part Number	V_F / I_F	Voltage Rating	Junction capacitance
D_{desat}	GeneSiC	GAP3SLT33-220FP	1.5V(175˚C) / 0.3 A	3300 V	5 pF

Table 3. 6: Design summary of D_{desat}.

3.3.7 Soft-turn-off

During clearing the fault, IGBT has to be softly turned off to reduce voltage overshoot under the short-circuit condition. The fault signal in the gate drive IC will disable the current buffer and enable the soft-turn-off circuits consisting of v_{GE} clamping Zener diode Z_{ge} and soft-turn-off resistor R_{soft} Figure 3. 11 shows the schematic of the soft-turn-off circuit.

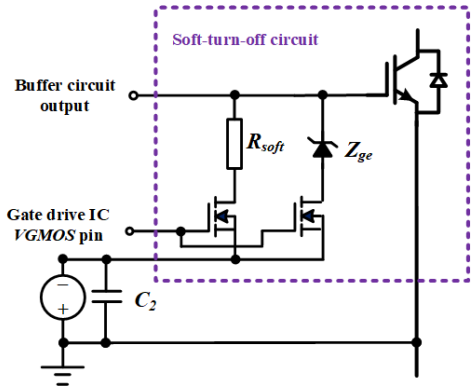


Figure 3. 11: Schematic of the soft-turn-off circuit.

Additionally, under the fault condition, IGBT v_{CE} rises rapidly due to the short circuit current (forcing IGBT transition from saturation area to active area) and the turn-off of the IGBT. As shown in Figure 3. 12, this high *dv/dt* introduces displacement current via gate-collector capacitance (i.e., Miller capacitance) of the IGBT flowing through the gate loop, leading to a spurious positive gate voltage higher than v_{GE} under the normal condition. In the end, the shoot-through current (i.e., the desaturation current of the IGBT) becomes larger.

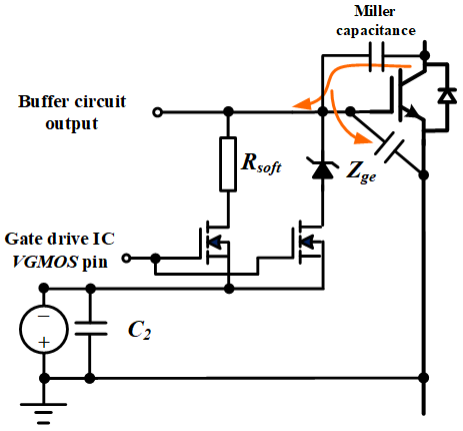


Figure 3. 12: Influence of the Miller Capacitor on the soft-turn-off circuit.

For this design, we only keep the R_{soft} branch. For the soft-turn-off resistor R_{soft}, the resistance should be designed to limit the turn-off speed to limit the voltage spikes across the IGBT and will be determined based on the test results later.

3.3.8 Decoupling capacitor

During the switching transient, the decoupling capacitor is responsible for supplying the transient power for the gate terminal. V_{CC} and V_{EE} provide the gate driving power. However, because of the relatively large volume, the power supply of V_{CC} and V_{EE}

physically cannot be positioned close to the gate drive and IGBT. Accordingly, large parasites are unavoidably introduced. Therefore, to avoid the parasitic contributed by the power supply and enhance the dynamic performance of the gate drive, locally placing the compact footprint and low equivalent series inductance (ESL) decoupling capacitor is essential. For DC-SSCB application, the decoupling capacitor is important to stabilize the V_{CC} and V_{EE} during normal operation and fault interruption.

For the gate voltage to remain steady throughout the switching transient, there should be enough capacitance for the decoupling capacitor. Conservatively, the decoupling capacitor must provide all the gate driving power during the switching transient.

$$C_1 > \frac{Q_g}{k_{VCC} \times V_{CC}} \tag{3. 19}$$

$$C_2 > \frac{Q_g}{k_{VEE} \times V_{EE}} \tag{3. 20}$$

where Q_g is the gate charge of IGBT; C_1 and C_2 are the decoupling capacitors for V_{CC} and V_{EE}, respectively; k_{VCC} and k_{VEE} are coefficients indicating the voltage variation percentages of V_{CC} and V_{EE}, respectively. In most cases, 1% - 5% is recommended.

Moreover, the decoupling capacitor's rating voltage has to be higher than VCC and $|V_{EE}|$.

The design of the decoupling capacitor is described below:

Step 1: Required capacitance should satisfy (5% for k_{VCC} and k_{VEE}):

$$C_1 > \frac{Q_g}{k_{VCC} \times V_{CC}} = \frac{28\mu C}{5\% \times 15} = 38\mu F \quad (3.\ 21)$$

$$C_2 > \frac{Q_g}{k_{VEE} \times V_{EE}} = \frac{28\mu C}{5\% \times 15} = 38\mu F \quad (3.\ 22)$$

Step 2: The surface mount ceramic capacitor is usually leveraged to minimize the ESL from the decoupling capacitor. Moreover, it is preferable to use several capacitors with tiny capacitance in parallel since this setup can further lower ESL. Figure 3. 13 shows the decoupling capacitor configuration in this design. The detail of those ceramic capacitors is summarized in Table 3. 7.

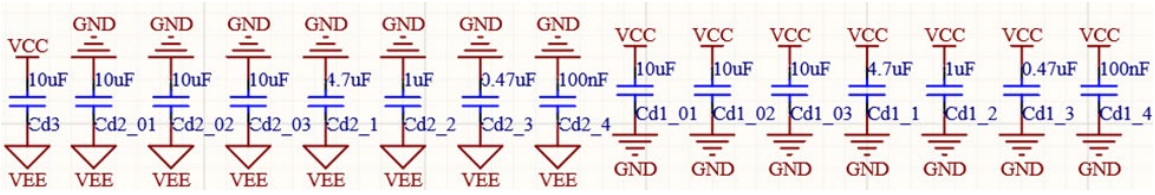


Figure 3. 13: Schematic of the decoupling capacitor configuration.

Part	Manufacturer	Part Number	Capacitance	Rating voltage	Package
Decoupling capacitor	Samsung	CL31Y106KBKVPJE	10μF	50 V	1206
	Samsung	CL21A475KBQNNNE	4.7μF	50 V	0805
	Samsung	CL21B105KBFNFNE	1μF	50 V	0805
	Samsung	CL21B474KBFNFNE	0.47μF	50 V	0805
	Samsung	CL21B104KBCNNNC	100nF	50 V	0805

Table 3. 7: Design summary of the decoupling capacitor.

3.3.9 Gate drive design result

Based on the above design procedures, Figure 3. 14 illustrates the gate drive design result for DC-SSCB.

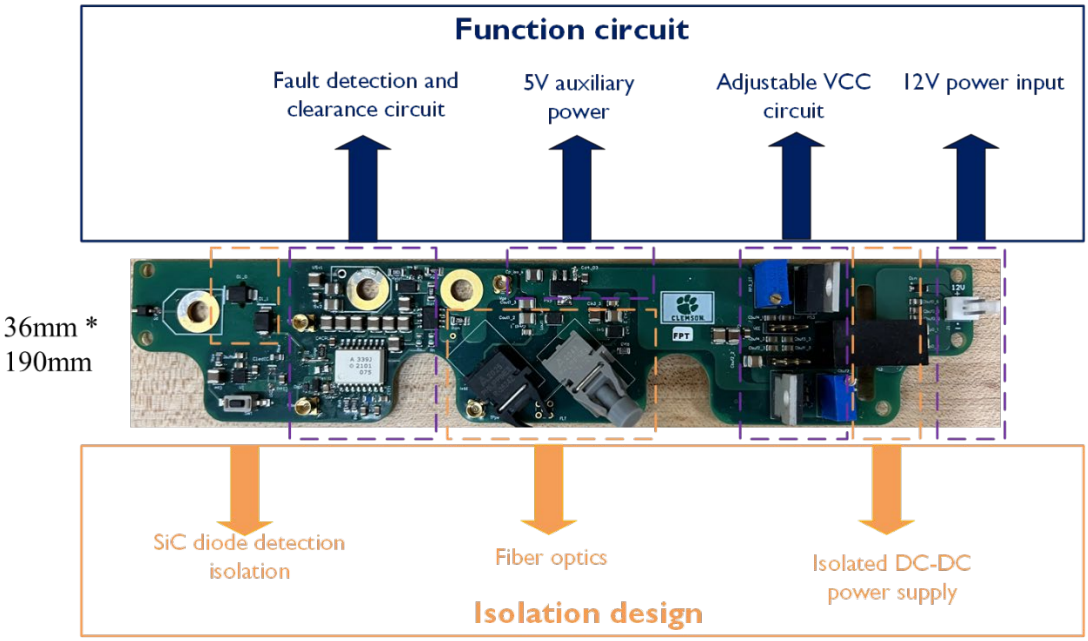


Figure 3. 14: Gate drive design result.

3.4 Test platform and experimental verification

3.4.1 Test setup

Figure 3. 15 displays a 2 kV/1kA SSCB prototype based on the specifications for NASA's STARC-ABL [110] concept to demonstrate the practicability of the proposed DC-SSCB without a current limitation inductor. The key parameters are summarized in Table 3. 8. The adjustable *Vcc* allows the DC-SSCB with different current limitation capabilities.

Parameters	Value
IGBT	FZ1000R33HE3
MOV	V511BA60
L_{MOV}	250 nH
R_g	10 Ω
Turn-on V_{CC}	10V-15 V
Turn-off V_{EE}	-7.5 V

Table 3. 8: Parameters of the SSCB prototype.

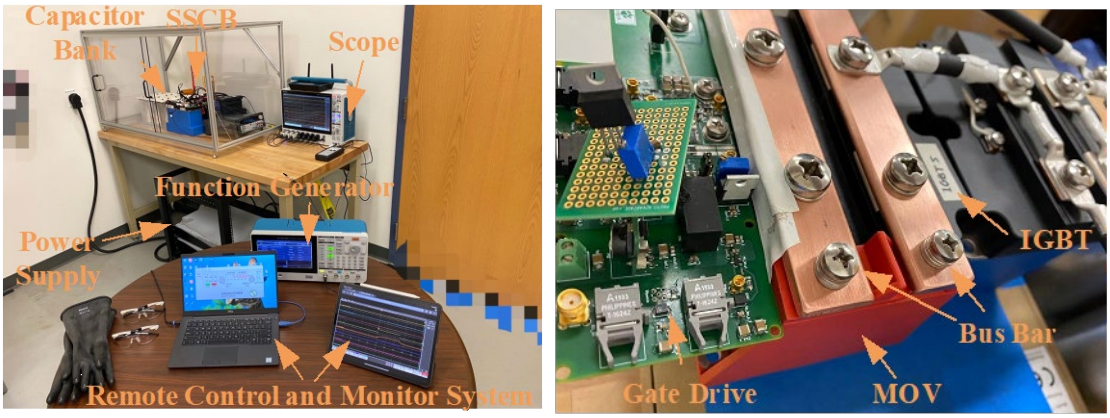


Figure 3. 15: DC-SSCB prototype and testbed.

3.4.2 Experimental verification

3.4.2.1 Peak current limitation capability

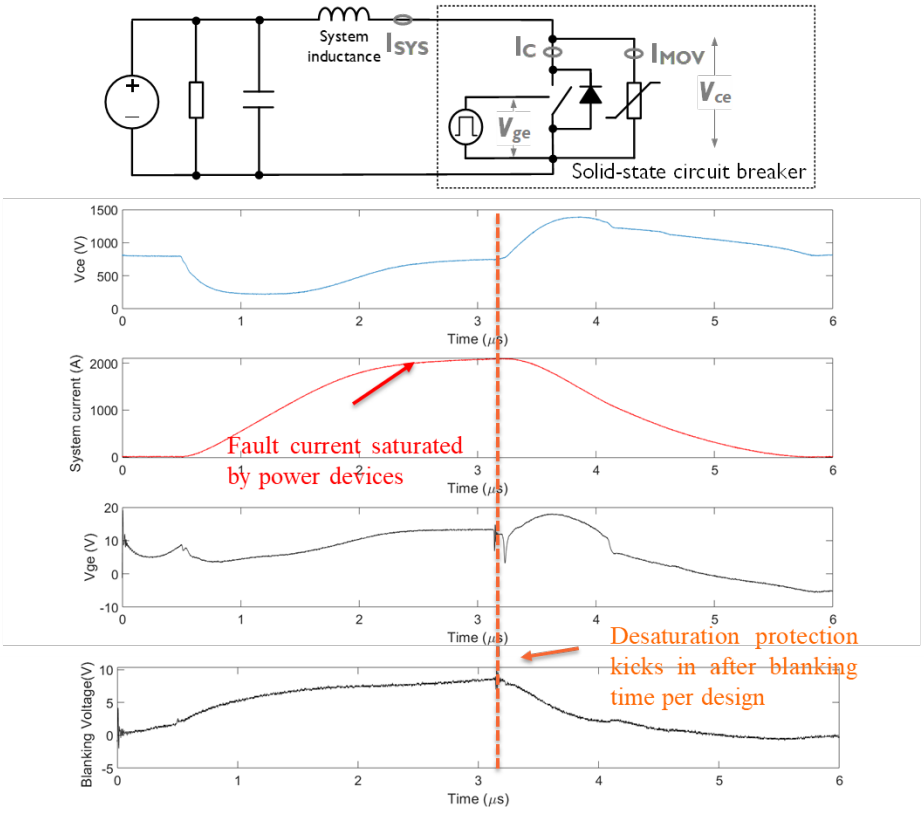


Figure 3. 16: DC-SSCB test waveform when system inductance is 0.

For DC-SSCB, the worst scenario is that the system inductance is almost zero, which means that there is no inductor limiting the system fault current increase. The system fault current can increase to an extremely high value quickly, and it is hard for the DC-SSCB to clear the fault in time. Figure 3. 16 shows the waveform of DC-SSCB without the current limiting inductor when the system inductance is zero. It can be found that the system's current is limited to about 2000 A at 3 μs with 11V gate voltage.

More tests are delivered in Figure 3. 17 to study the influence of gate voltage on the current limitation level. It can be found that with the gate voltage increase, the limitation current also increases.

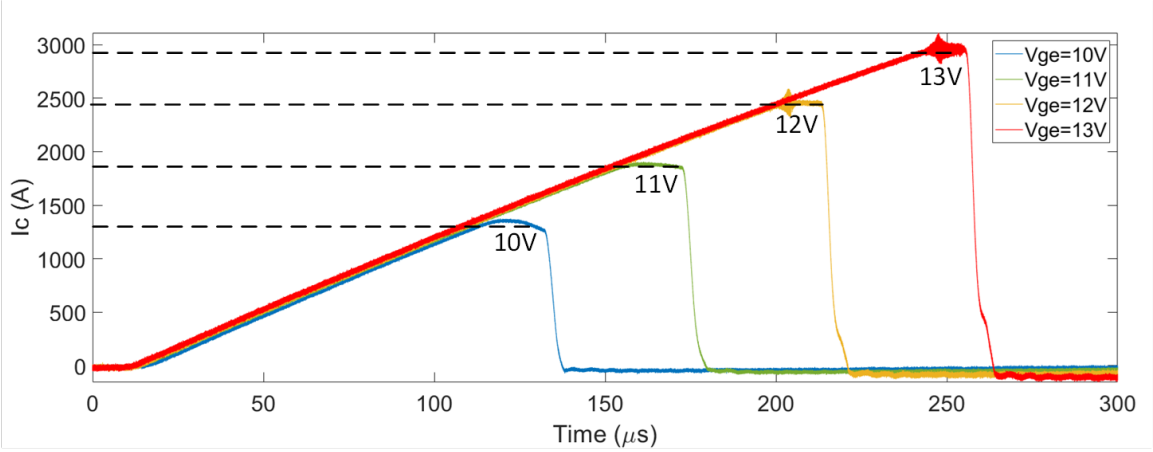


Figure 3. 17: DC-SSCB collector current under different gate voltage.

The ambient temperature also influences the characteristics of the IGBT. Thus, Figure 3. 18 summarizes the influence of the ambient temperature and gate voltage on the IGBT's saturation current (limitation current). It can be concluded that the higher the ambient temperature, the lower the DC-SSCB's limitation current.

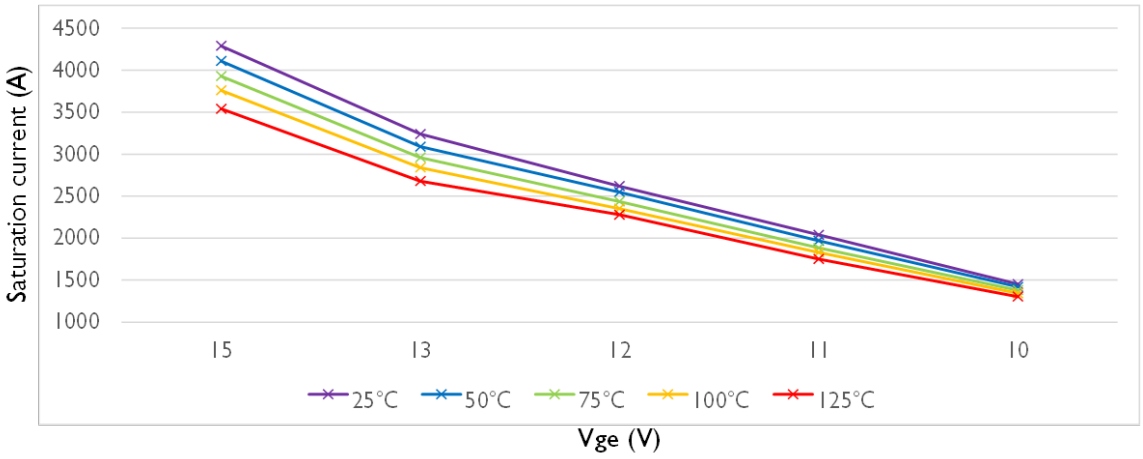


Figure 3. 18: DC-SSCB saturation current with different v_{GE} and ambient temperatures.

3.4.2.2 Interruption capability

Interruption capability is one of the most important features of DC-SSCB. Figure 3. 19 and Figure 3. 20 show the system current and collector-emitter voltage under different scenarios, respectively. Test results show that the proposed DC-SSCB without the current limiting capacitor can interrupt the fault current reliably under different system inductance and ambient temperatures.

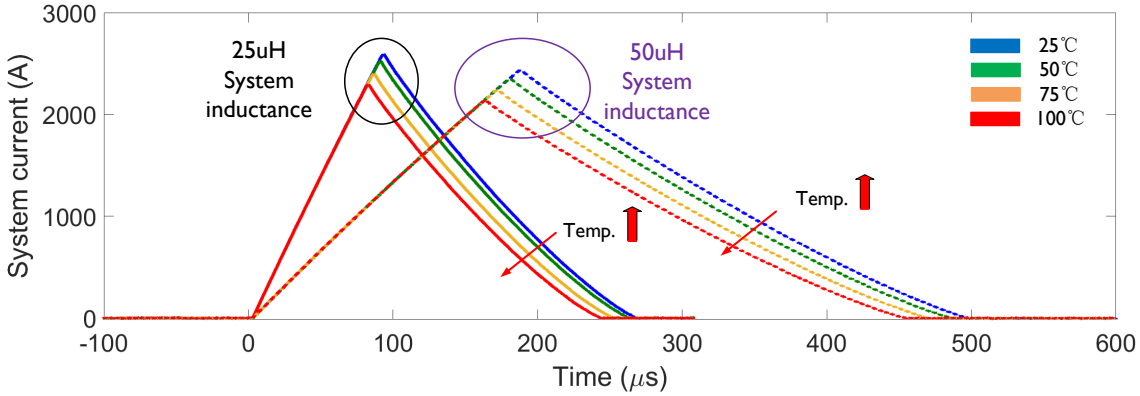


Figure 3. 19: System current with different fault inductance and ambient temperatures.

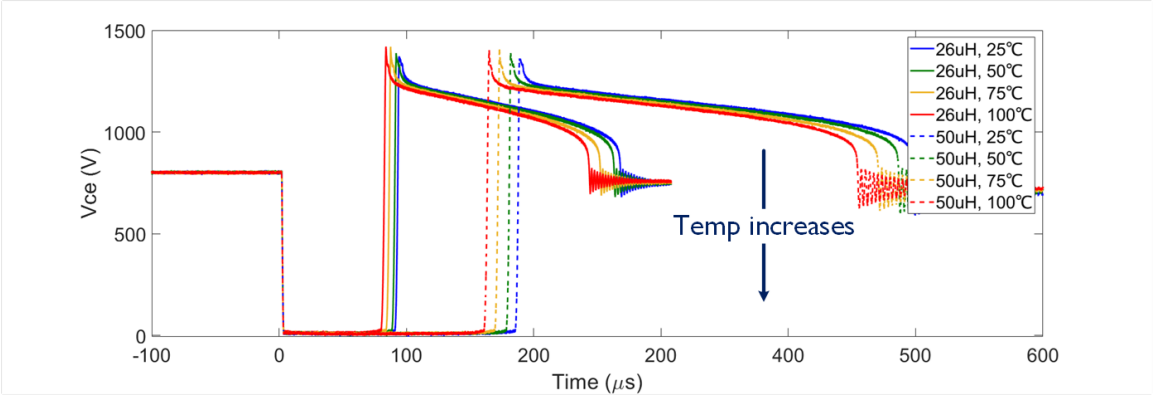


Figure 3. 20: SSCB's v_{CE} under different system inductance and ambient temperature.

3.5 Conclusion

This chapter proposes a high-power density solid-state circuit breaker without the current limiting inductor for aviation applications. The proposed SSCB can limit the maximum peak fault current level through V-I curve characteristics, thus achieving a high specific power density for hybrid electric propulsion applications. The gate voltage can also tune the peak fault current level. Detailed design and analysis of the proposed SSCB are presented. Experimental results show the feasibility and effectiveness of the proposed solution.

CHAPTER FOUR

4 MODELING OF DC-SSCB

4.1 Introduction

As the enabler of next-generation DC power distribution systems, DC-SSCB behavior is sensitive to power semiconductors, gate drives, energy absorber (e.g., varistors), and their coupling. Thus, it is critical to understand the impact of different design parameters on the performance of DC-SSCB, especially on the fault current interruption. This section proposes an analytical model to establish the relationship between SSCB dynamic performance when the fault is being cleared depending on design variables and operating conditions. Then the sensitivity analysis is performed based on the proposed model to identify the most critical design parameters. Finally, simulation and test results based on a 2kV/1kA SSCB prototype built in Chapter 3 demonstrate the accuracy of the proposed model, which provides fundamentals for the design optimization of SSCB considering gate drive and energy absorber.

4.2 SSCB modeling

As illustrated in Figure 4. 1, for the bidirectional DC-SSCB designed in Chapter 3, two identical SSCBs are installed in the positive and negative poles of the DC system, respectively. Each SSCB consists of two anti-series Si IGBTs with anti-parallel diodes to carry and break bi-directional currents. The MOV is connected in parallel with the IGBT block to clamp the peak voltage. L_{sys} is the system inductor under the fault, and V_{DC} is the DC bus voltage.

DC-SSCB detail model with key parameters is illustrated at the top of Figure 4. 1. This section considers that the DC-SSCB is working with a single-direction current. Specifically, the proposed SSCB model consists of one power semiconductor, a related gate drive, and MOV. It is noted that IGBT is selected as the semiconductor under analysis due to its low cost, high reliability, and availability. However, a similar method can be leveraged for other power semiconductors, including emerging wide bandgap devices.

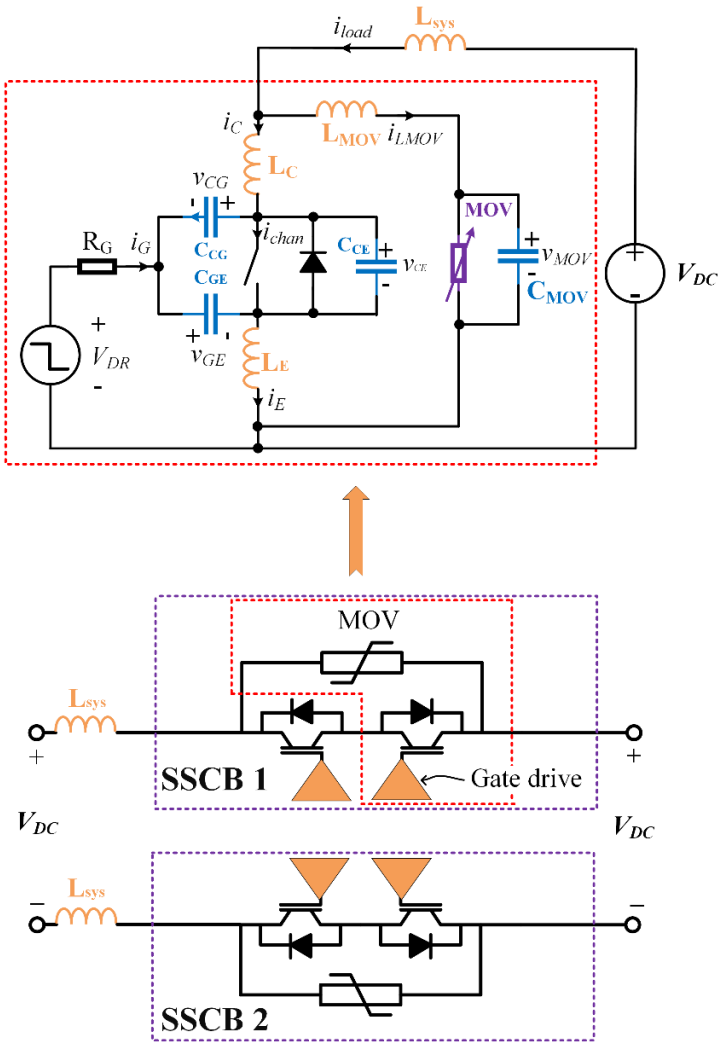


Figure 4. 1: DC-SSCB with detail model.

Regarding the IGBT, its channel, together with collector-gate capacitance C_{CG}, collector-emitter capacitance C_{CE}, gate-emitter capacitance C_{GE}, collector inductance L_C, and emitter inductance (i.e., common source inductance) L_E are considered. It has to be pointed out that the tail current is not focused here since its impact on the peak clamping voltage is limited. Driving voltage V_{DR} (V_{CC} and V_{EE} refer to turn-on/-off driving voltages, respectively) and gate resistance R_G are included in the following analysis. The model also considers MOV *V-I* characteristics, its associated capacitance C_{MOV}, and parasitic inductance L_{MOV} primarily contributed by the interconnection (e.g., bus bar) between IGBT and MOV. Figure 4. 2 shows a typical *V-I* curve of the MOV. The *V-I* curve consists of the pre-breakdown region, normal operating region, and recovery region dependent on the current. During the normal operation of DC-SSCB, MOV works in the pre-breakdown region. When the protection is triggered, MOV can operate in the normal operating region to clamp the overvoltage of v_{CE} and absorb the fault current from the IGBT during the turn-off process.

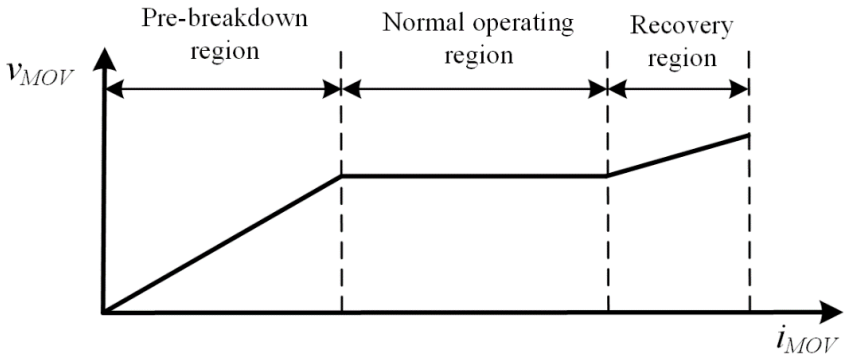


Figure 4. 2: Typical *V-I* curve of the MOV.

Figure 4. 3 shows the typical fault current interruption transition for DC-SSCB. It shows the performance of v_{GE}, v_{CE}, channel current i_C, and MOV current i_{mov} during fault

current interruption transition. Before t_0, there is no fault, and the DC-SSCB works in normal condition. Then, a short circuit fault occurs at t_0, and the DC-SSCB protection is triggered at t_1 based on the conventional desaturation protection. In this Section, we assume that the desaturation protection is fast enough, which means that IGBT remains at the saturation region when the protection is triggered.

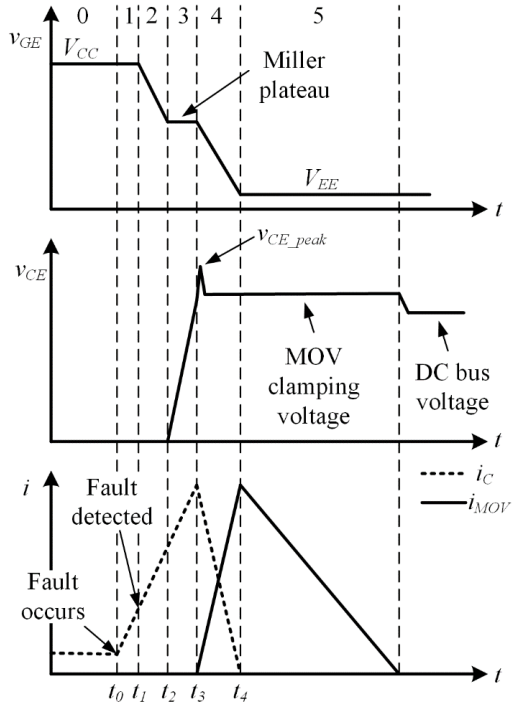


Figure 4. 3: Fault current interruption transition.

The current interruption transition consists of five subintervals, including *subinterval 1*: desaturation detection delay from t_0 to t_1; *subinterval 2*: power semiconductor turn-off delay from t_1 to t_2; *subinterval 3*: v_{CE} voltage rise from t_2 to t_3; *subinterval 4*: current commutation between power semiconductor and MOV from t_3 to t_4, and *subinterval 5*: MOV energy absorption after t_4.

In this Section, only state equations are provided. For the actual implementation, it could be solved by analytical formula or numerical solver, which is not the focus of this chapter. Therefore, only the state-space models are derived below. Current i_E through L_E, i_C through L_C, MOV current i_{MOV}, v_{GE}, and v_{CE} are selected as the independent variables for the state equations. It is noted that the final values of the aforementioned independent variables in the last subinterval become the initial values for the upcoming subinterval.

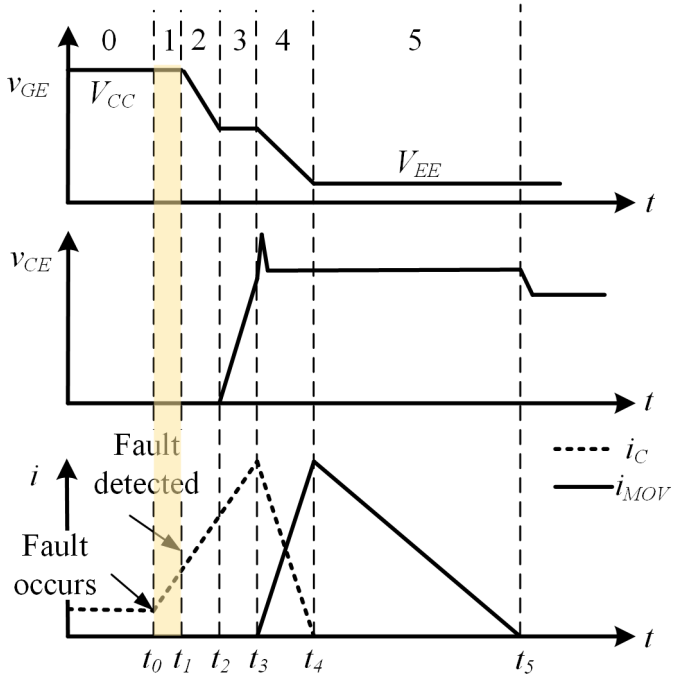


Figure 4. 4: Fault current interruption transition with Subinterval I highlight.

Subinterval I: Desaturation detection delay

During this subinterval, from t_0, the short circuit fault current forces v_{CE} to increase. Because the protection is not triggered, IGBT remains on-state, operates in saturation area, and v_{GE} remains at V_{CC}. Meanwhile, MOV works in the pre-breakdown region. Then, at t_1,

v_{CE} is higher than the desaturation protection threshold voltage, triggering the protection. During this subinterval, i_{MOV} and v_{CE} are small and negligible.

Subinterval II: IGBT turn-off delay

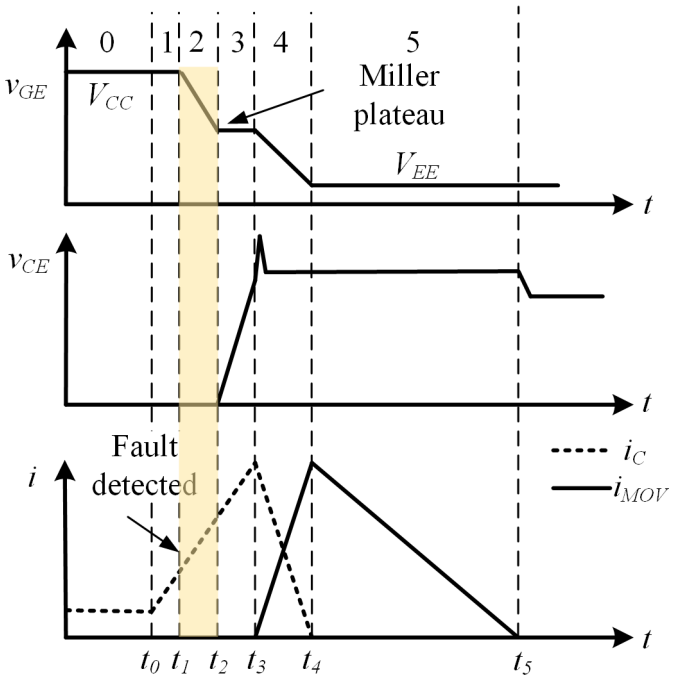


Figure 4. 5: Fault current interruption transition with Subinterval II highlight.

During this subinterval, the desaturation protection has been triggered. As illustrated in Figure 4. 5, v_{GE} decreases from the turn-on gate voltage V_{CC} to Miller plateau voltage V_{Miller}. In this subinterval, MOV works in the pre-breakdown region, and the IGBT remains in the saturation region. Assuming the leakage current of MOV in the pre-breakdown area is small and negligible, yielding

$$\begin{cases} \dfrac{V_{CC} - v_{GE} - L_E \dfrac{di_E}{dt}}{R_g} + C_{CG} \dfrac{dv_{CG}}{dt} = C_{GE} \dfrac{dv_{GE}}{dt} \\ \dfrac{V_{CC} - v_{GE} - L_E \dfrac{di_E}{dt}}{R_g} + C_{CG} \dfrac{dv_{CG}}{dt} = C_{GE} \dfrac{dv_{GE}}{dt} \\ i_C = g_{fs}(v_{GE} - V_{th}) + C_{CG} \dfrac{dv_{CG}}{dt} + C_{CE} \dfrac{dv_{CE}}{dt} \\ i_{MOV} = 0 \\ v_{CE} = 0 \end{cases}$$

where g_{fs} represents the transconductance, V_{th} refers to threshold voltage and $v_{CE} = v_{CG} + v_{GE}$.

Subinterval III: v_{CE} voltage rise

During this subinterval, as illustrated in Figure 4. 6, v_{GE} remains V_{Miller}, i_C follows i_{load}, while v_{CE} starts to increase. In this subinterval, MOV remains pre-breakdown region, and the IGBT moves to the active area from the saturation area. Then, the space-state equation in Subinterval III is expressed as

$$\begin{cases} \dfrac{V_{CC} - v_{GE} - L_E \dfrac{di_E}{dt}}{R_g} + C_{CG} \dfrac{dv_{CG}}{dt} = C_{GE} \dfrac{dv_{GE}}{dt} \\ i_E = g_{fs}(v_{GE} - V_{th}) + C_{GE} \dfrac{dv_{GE}}{dt} + C_{CE} \dfrac{dv_{CE}}{dt} \\ i_C = g_{fs}(v_{GE} - V_{th}) + C_{CG} \dfrac{dv_{CG}}{dt} + C_{CE} \dfrac{dv_{CE}}{dt} \\ V_{DC} = v_{CE} + L_C \dfrac{di_C}{dt} + L_E \dfrac{di_E}{dt} + L_{sys} \dfrac{di_{load}}{dt} \\ i_{MOV} = 0 \end{cases}$$

where $i_{load} = i_{LMOV} + i_c$.

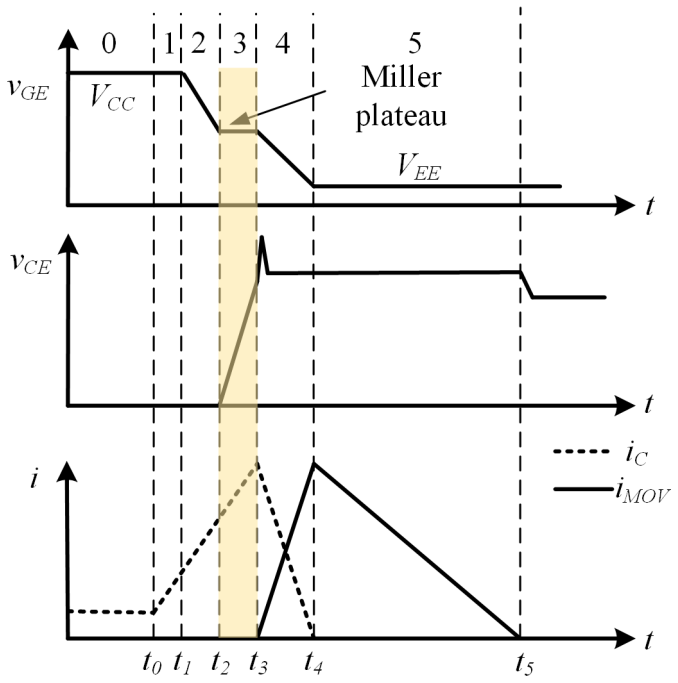


Figure 4. 6: Fault current interruption transition with Subinterval III highlight.

Subinterval IV: current commutation

As illustrated in Figure 4. 7, current commutation is the crucial subinterval during the current interruption transition of DC-SSCB, v_{GE} keeps decreasing, current commutates from IGBT to MOV. In this time interval, MOV transitions to the normal operating region as v_{CE} exceeds the threshold voltage of the MOV, and IGBT remains in the active region. Based on the data provided by the MOV datasheet, MOV *v-i* characteristics are able to be expressed as

$$v_{MOV} = f\left(i_{MOV}\right)$$

Accordingly, the model in subinterval IV is summarized below

$$\begin{cases} \dfrac{V_{CC} - v_{GE} - L_E \dfrac{di_E}{dt}}{R_g} + C_{CG} \dfrac{dv_{CG}}{dt} = C_{GE} \dfrac{dv_{GE}}{dt} \\ i_E = g_{fs}(v_{GE} - V_{th}) + C_{GE} \dfrac{dv_{GE}}{dt} + C_{CE} \dfrac{dv_{CE}}{dt} \\ i_C = g_{fs}(v_{GE} - V_{th}) + C_{CG} \dfrac{dv_{CG}}{dt} + C_{CE} \dfrac{dv_{CE}}{dt} \\ V_{DC} = v_{CE} + L_C \dfrac{di_C}{dt} + L_E \dfrac{di_E}{dt} + L_{sys} \dfrac{di_{load}}{dt} \\ V_{DC} = L_{sys} \dfrac{di_{load}}{dt} + v_{LMOV} + v_{MOV} \end{cases}$$

where

$$\begin{cases} i_{load} = i_{LMOV} + i_c \\ v_{LMOV} = L_{MOV} \dfrac{di_{LMOV}}{dt} \\ i_{LMOV} = i_{MOV} + C_{MOV} \dfrac{df(i_{MOV})}{dt} \end{cases}$$

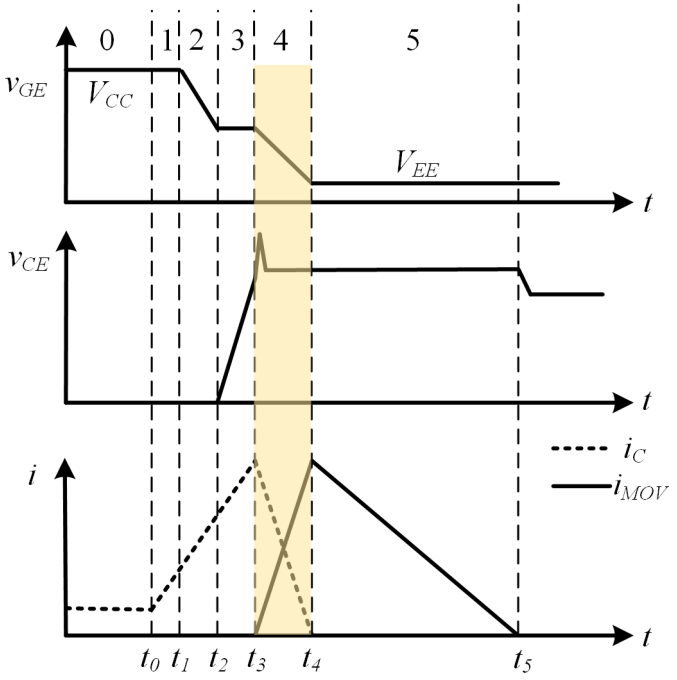


Figure 4. 7: Fault current interruption transition with Subinterval IV highlight.

Subinterval V: energy absorption

During this subinterval, as illustrated in Figure 4. 8, IGBT current approaches zero, and the current flowing through the MOV keeps decreasing. MOV continues in the normal operating region in this subinterval, and the IGBT works in the cut-off region. Then, the space state equation of the Subinterval V can be derived as:

$$\begin{cases} \dfrac{V_{CC} - v_{GE} - L_E \dfrac{di_E}{dt}}{R_g} + C_{CG} \dfrac{dv_{CG}}{dt} = C_{GE} \dfrac{dv_{GE}}{dt} \\ i_E = C_{GE} \dfrac{dv_{GE}}{dt} + C_{CE} \dfrac{dv_{CE}}{dt} \\ i_C = C_{CG} \dfrac{dv_{CG}}{dt} + C_{CE} \dfrac{dv_{CE}}{dt} \\ V_{DC} = v_{CE} + L_C \dfrac{di_C}{dt} + L_E \dfrac{di_E}{dt} + L_{sys} \dfrac{di_{load}}{dt} \\ V_{DC} = L_{sys} \dfrac{di_{load}}{dt} + v_{LMOV} + v_{MOV} \end{cases}$$

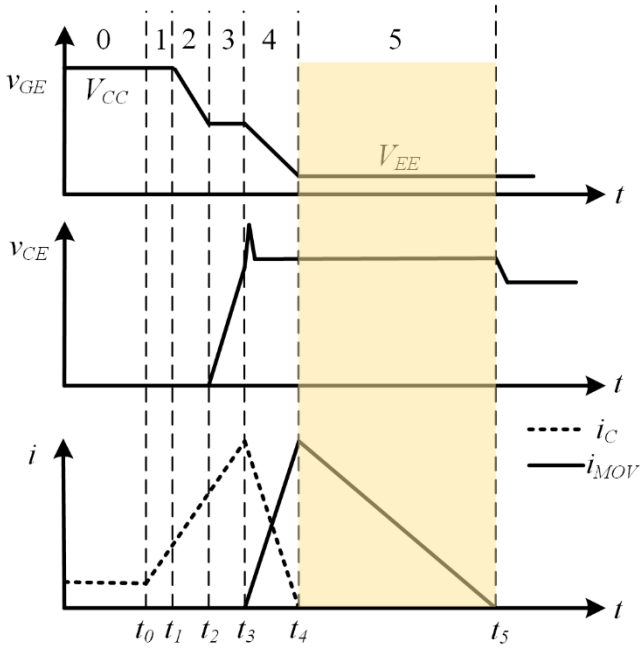


Figure 4. 8: Fault current interruption transition with Subinterval V highlight.

4.3 Model verification

To verify the effectiveness of the proposed DC-SSCB model, based on the design and test platform in Section 3, a 2kV/1kA DC-SSCB prototype is established. The critical parameters of the built DC-SSCB model are shown in Table 4. 1.

Meanwhile, according to the parameters in Table 4. 1 and the DC-SSCB detail model in Figure 4. 1, a Matlab Simulink-based simulation model is built in Figure 4. 9. Based on the datasheet information, the look-up table block realizes the nonlinear characteristics of IGBT and MOV. According to the output of the look-up table, current controlled sources are leveraged to represent the behavior of IGBT and MOV.

Parameters	Value
V_{DC}	800V
IGBT	FZ1000R33HE3
MOV	V511BA60
L_{MOV}	250nH
L_{sys}	55μH
R_g	10Ω
V_{CC}	15V
V_{EE}	-7.5V

Table 4. 1: The critical parameters of the built DC-SSCB model.

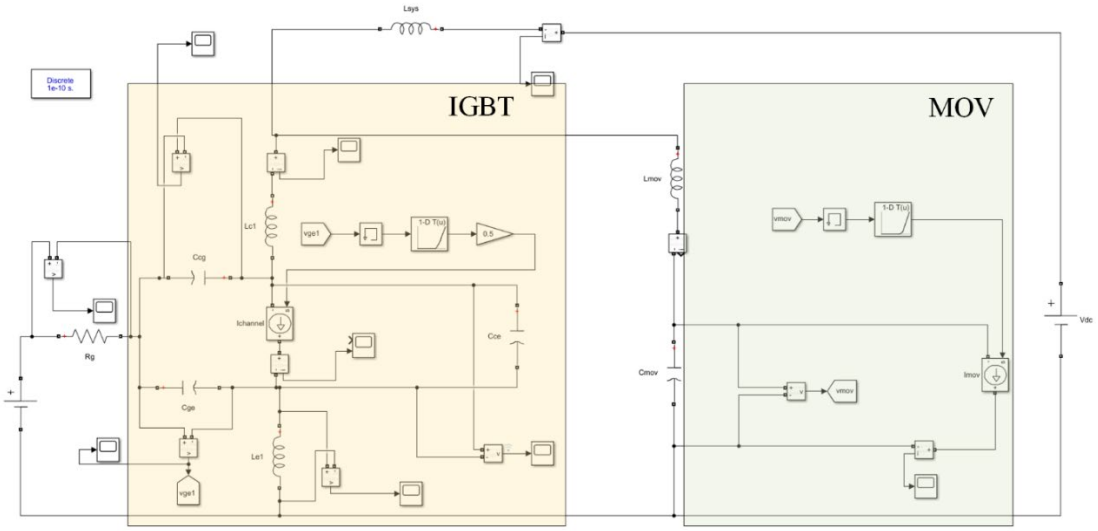


Figure 4. 9: Matlab Simulink-based simulation model for DC-SSCB.

Figure 4. 10, Figure 4. 11, and Figure 4. 12 show the comparison of v_{CE}, i_c, and i_{mov} between model and test results. The comparison results show that the results based on the derived model agree with the test results under the operating conditions of 800V/3000A, as evidenced by a 1.3% maximum mismatch of clamping voltage (20 V mismatch out of 1530 V) and 1.1% maximum mismatch of clamping current (33A mismatch out of 3100A).

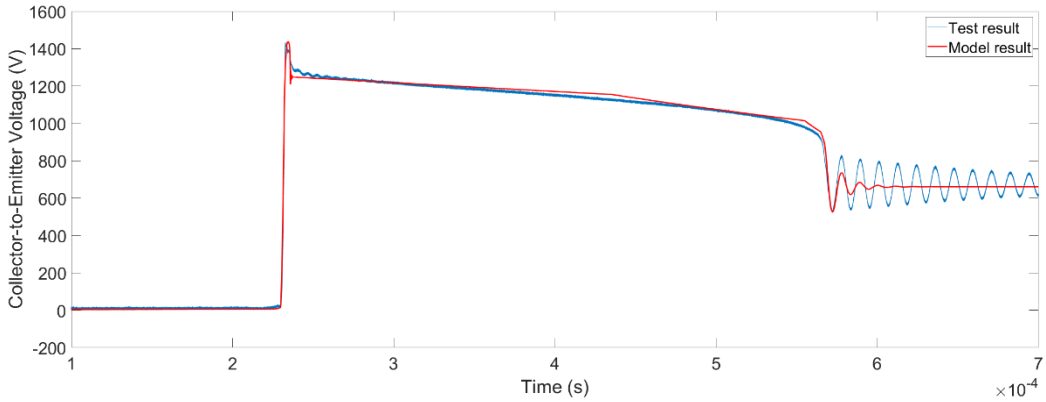


Figure 4. 10: Comparison of v_{CE} between model and test results.

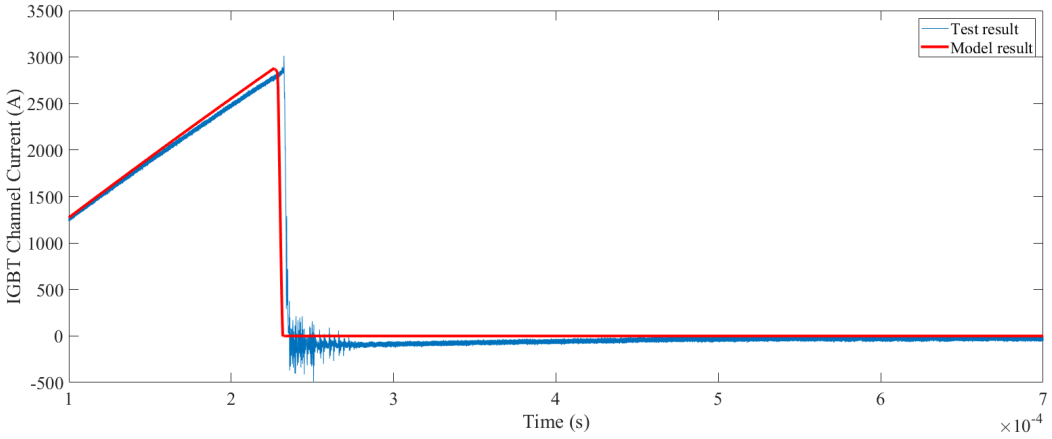


Figure 4. 11: Comparison of i_C between model and test results.

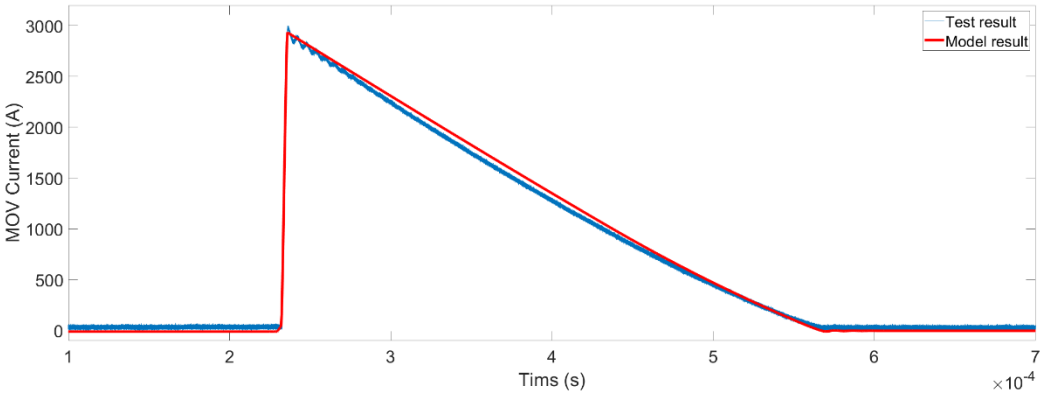


Figure 4. 12: Comparison of i_{MOV} between model and test results.

4.4 Sensitivity analysis

As can be observed in the derived model, numerous parameters play roles in the DC-SSCB dynamic behavior. Some of them are highly coupled with each other, such as L_{sys}, C_{CG}, C_{CE}, C_{GE}, L_E, L_C, V_{DR}, R_G, C_{MOV}, and L_{MOV}, as illustrated in Figure 4. 1.

Thus, from the perspective of DC-SSCB designers, it is significant to identify the sensitive parameters of the DC-SSCB dynamic behavior. Therefore, more design attention

could be paid to these parameters while other insignificant elements can be de-emphasized. Furthermore, it brings an opportunity to simplify the model derived above with reduced order of state equations for better engineering insights. Consequently, it is essential to perform a sensitivity analysis to quantify the impact of each parameter on the dynamic behavior of DC-SSCB during the current interruption phase.

The peak value of v_{CE}, V_{CE_peak}, is identified as one of the most critical dynamic performance metrics for the DC-SSCB design, which determines the selection of MOV and the safe operation of DC-SSCB. Considering that the value of C_{CG}, C_{CE}, C_{GE} are dominated by IGBT, L_{sys}, L_E, L_C, V_{DR}, R_G, C_{MOV}, and L_{MOV} are selected as sensitivity analysis input variables.

MATLAB is used to perform the sensitivity analysis with the proposed DC-SSCB model based on the embedded sensitivity analysis toolbox. L_{sys}, L_E, L_C, V_{DR}, R_G, C_{MOV}, and L_{MOV} are selected as sensitivity analysis input variables to study their influence on V_{CE_peak}. 300 samples are randomly selected based on the Monte Carlo method with the parameter sweeping ranging listed in Table 4. 2.

Based on the 300 randomly generated samples, the scatter subplots display the V_{CE_peak} as a function of each parameter in the parameter set.

The number of points in each scatter plot equals the number of rows in the parameter set. The last column of subplots displays histograms of the probability distribution of the evaluated cost function values (V_{CE_peak}). It can be found in Figure 4. 13

that V_{CE_peak} is highly monotonically related to the parameter L_E and L_{MOV} indicating L_{MOV} and L_E are more critical to V_{CE_peak}.

Parameters	Lower limit	Upper limit
L_{MOV}	100nH	300nH
L_{sys}	30μH	70μH
R_g	5Ω	15Ω
V_{CC}	10V	18V
V_{EE}	-10V	-5V
L_C	10nH	30nH
L_E	8nH	20nH
C_{MOV}	1nC	5nC

Table 4. 2: Input variables range for sensitivity analysis.

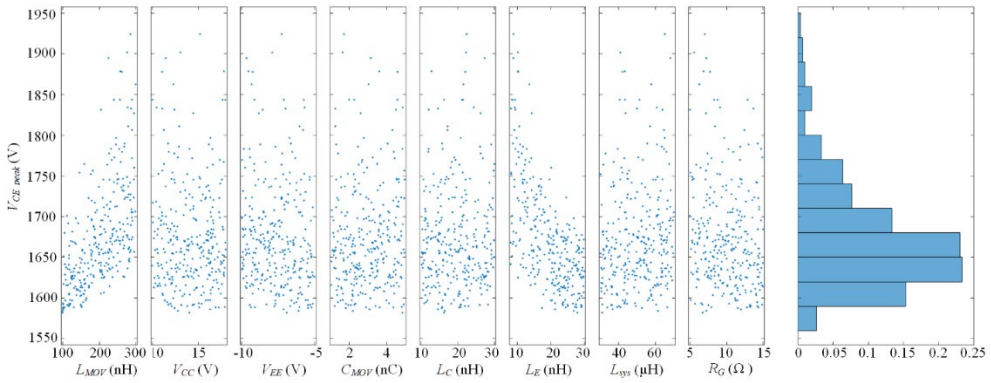


Figure 4. 13: Scatter plot of the sensitivity analysis for DC-SSCB.

Then the quantitative analysis is performed to investigate the influence of L_{sys}, L_E, L_C, V_{DR}, R_G, C_{MOV}, and L_{MOV} on V_{CE_peak}. Results are illustrated in Figure 4. 14. Five indexes (i.e., correlation, rank correlation, Kendall correlation, standardized regression, and standardized regression) are leveraged to quantify the input variables' influence on V_{CE_peak}. Correlation is utilized to analyze how the input variables and V_{CE_peak} are related; Standardized regression is used to analyze how the input variables linearly influence

V_{CE_peak}. Partial correlation indicates how the input variables and V_{CE_peak} are related without the influence of the other variables.

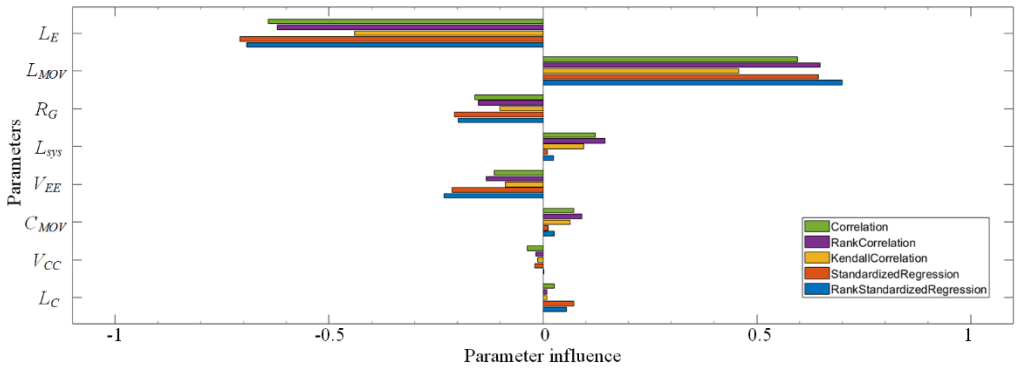


Figure 4. 14: Parameter influence on V_{CE_peak}.

The values of the five indexes are located between -1 and +1. When the value is between 0 and +1, the higher the value, the higher the positive correlation between the corresponding input variable and V_{CE_peak}. When the value is between -1 and 0, the lower the value, the higher the negative correlation between the corresponding input variable and V_{CE_peak}.

Thus, as can be observed in Figure 4. 14, L_E is highly negative correlation to the V_{CE_peak}; L_{MOV} is highly positive correlation to the V_{CE_peak}, which is consistent with the scatter plot result. Similarly, it can also be observed that the V_{CE_peak} is negatively correlated to R_g and V_{EE}. Additionally, L_{sys} has a positive influence on the V_{CE_peak}. Accordingly, Table 4. 3 summarizes the relationship between L_{sys}, L_E, L_C, V_{DR}, R_G, C_{MOV}, $L_{MOV,}$ and V_{CE_peak}.

Correlation	Parameters
↑ ↑	L_{MOV}
↑	L_{sys}
↓ ↓	L_E
↓	R_G
	V_{EE}
--	V_{CC}
	L_C
	C_{MOV}
↑ ↑ : positive correlation greatly ↑ : positive correlation slightly ↓ ↓ : negative correlation greatly ↓ : negative correlation slightly --: weak correlation	

Table 4. 3: Input variables range for sensitivity analysis.

Therefore, the model proposed in Figure 4. 1 can be simplified by removing the weak correlation parameters, e.g., L_C and C_{MOV}, as illustrated in Figure 4. 15, which allows the order reduction of DC-SSCB state equations.

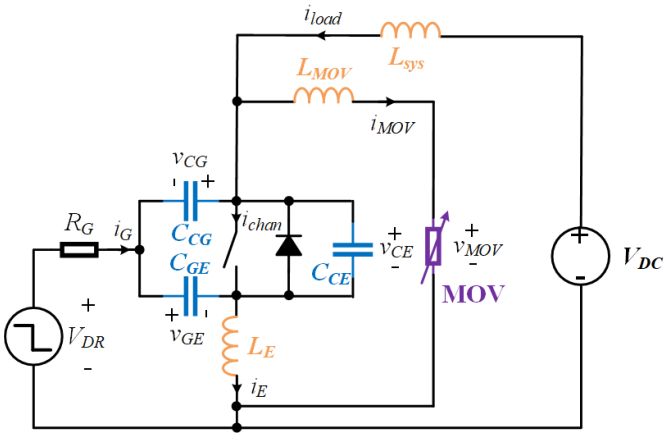


Figure 4. 15: Simplified model of the proposed DC-SSCB.

4.5 Conclusion

This chapter proposes an analytical DC-SSCB model, offering fundamentals for the design optimization of DC-SSCB with the holistic consideration of power semiconductor, gate drive, MOV, and associated parasitics. Based on the experimental verification, it shows the proposed DC-SSCB model can accurately estimate the peak clamping voltage with no more than 1.3% mismatch as compared to the test result, while the maximum mismatch of the clamping current is 1.1%. Moreover, the sensitivity analysis indicates that L_{MOV} and L_E are the most crucial impact factors, while C_{MOV} and L_C are the parameters with the least influence on V_{CE_peak}. This offers the fundamentals to further simplify the derived models with order reduction of the state equations; in the meantime, it guides the co-design optimization of the gate drive, MOV, and parasitic management for high-density SSCB.

CHAPTER FIVE

5 OSCILLATION ISSUE AND SOLUTION FOR SSCB

5.1 Introduction

For the proposed DC-SSCB, the protection is triggered upon desaturation detection [111]. The SSCB gate drive circuit monitors v_{CE}. When v_{CE} indicates that the device has left its normal working region and entered the active region, the SSCB can interrupt the fault by turning off the power semiconductor switch through the gate drive. Moreover, if the fault current approaches the protection triggering threshold faster than the desaturation protection response time (e.g., short-circuit fault at the SSCB terminal with low system inductance), the fault current can still be limited based on the *V-I* characteristics where the IGBT gate voltage remains at the normal on-state voltage. This leads to the most stressful situation for IGBT and is a unique operating condition for limiting inductor-free SSCB that is usually not desired/occurred in a normal pulse width modulation (PWM)-based converter operation.

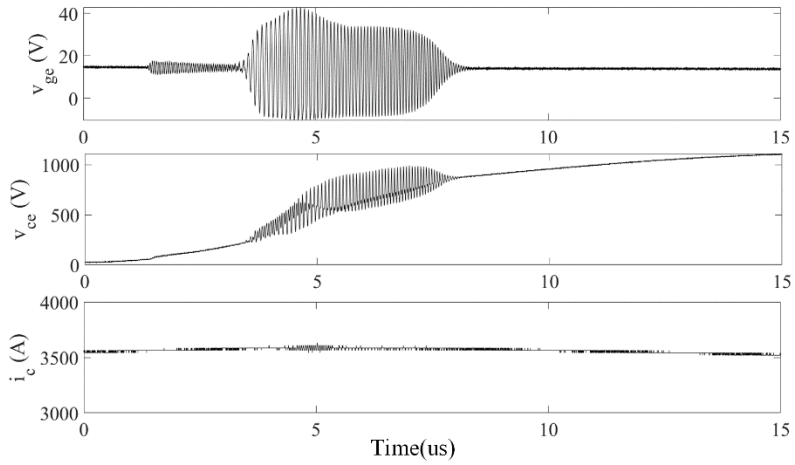


Figure 5. 1: Experimental oscillation waveform of v_{GE} and v_{CE}.

As shown in Figure 5. 1, when the IGBT enters the active region, severe oscillation of v_{GE} and v_{CE} is observed in the test, which could damage the device. Meanwhile, the i_c of the IGBT is limited by its i-v characteristics. It is noted that the IGBT is not turned off during the oscillation, which represents the worse condition where the gate drive is not fast enough to turn off the IGBT when the fault occurs. Thus, it is of vital significance to analyze the mechanism causing the oscillation and suppress it.

5.2 Literature review

In most cases, the oscillation can happen during the switching transition and short-circuit condition. Extensive studies have been performed to analyze the power device voltage oscillation, especially for emerging wide bandgap (WBG)-based devices during the fast-switching transition. Ref. [112] reviews the categories, the reasons, the negative effects, the influence of the parasitic parameters, and the suppression approaches for the WBG switching oscillations.

For the SSCB, the oscillation is most likely associated with the "short-circuit" condition where a large current and high voltage exists simultaneously. Thus, this review focuses on the oscillation under the short-circuit condition. The study of IGBT oscillation under short-circuit dates back to 2000. Without differential oscillation, Ref. [113] utilizes one IGBT chip for analysis and concludes that the Miller feedback capacitance causes the oscillation. However, there is no apparent oscillation in gate-emitter voltage, and the IGBT does not enter the active region. A small-signal model for the IGBT model with two chips is established in [114] to analyze the oscillation when the IGBT enters the active region. However, the influence of different parameters on the oscillation is not assessed, and the

proposed suppression method is not satisfactory. The oscillation when the IGBT enters the active region is also observed in [115]. A low-pass filter-based gate loop is proposed to suppress the gate oscillation. However, Ref. [115] does not fully explain the cause of the oscillation. The junction temperature and the stray inductance are identified as critical impact factors during the short-circuit of the IGBT module in [116] but with a limited method for oscillation suppression. Refs. [117, 118] analyze and mitigate the IGBT chip oscillation under the short-circuit condition from the level of IGBT inner construction by inserting an n-doped layer at the surface of the IGBT. In a nutshell, [115-118] do not consider the influence of the multi-chip arrangement in the IGBT module, and the proposed suppression methods are relatively hard to implement. Moreover, [119, 120] also analyze and suppress the oscillation under the short-circuit condition for SSCB. However, their oscillation occurs in the turn-off time interval, which is not sufficient to explain the oscillation observed in Figure 5. 1.

Semiconductor Device Operation Scenario		Single Die	Power Module with Multiple Chips
Normal PWM operation	Switching transient (gate voltage changes)	Yes	Yes
	Short-circuit (gate voltage does not change)	Yes	Yes
SSCB operation	Switching transient (gate voltage changes)	Yes	Yes
	Short-circuit (gate voltage does not change)	No	No (work of this chapter)

Table 5. 1: Summarization of the semiconductor oscillation under different scenarios.

Table 5. 1 summarizes the state-of-the-art studies on power semiconductor oscillation under different scenarios. It can be found that the oscillation phenomenon has been widely investigated. According to the semiconductor operation scenarios, it can be divided into PWM operation in power converters and SSCB operation. Specifically, the oscillation can occur when the gate voltage changes or when the gate voltage does not

change. For the SSCB application, there are some works focusing on semiconductor oscillation. A few papers explored the oscillation in SSCB during the switching transition when the gate voltage changes to turn-off voltage to cut off the fault. However, there is no study of the oscillation in SSCB during short circuit with no change in gate voltage. Thus, this chapter fills the gap in the study of SSCB oscillation under the short circuit condition. In summary, the contributions of this chapter include 1) the first time analyzing the SSCB oscillation with MOV model during a short circuit with gate constantly on; 2) the first time analyzing the SSCB oscillation with multi-dies semiconductor model with multiple parameters/parasitics mismatch; 3) holistically exploring potential solutions for oscillation suppression with experimental verification.

5.3 Oscillation analysis

To analyze the process when the SSCB enters the active region, a detailed model holistically considering power semiconductor device characteristics, gate drive, MOV, and associated parasitics is developed in Figure 5. 2. It is noted that a power module with multiple dies is needed for the target high-power EAP system. Accordingly, as illustrated in Figure 5-2, a power module consisting of two chips is focused on as the first step. A similar methodology could be utilized for more than two chips packaged in one module. Analysis results for three chips and four chips are also presented in this chapter.

Specifically, the model in Figure 5. 2 considers two IGBT channels together with corresponding collector-gate capacitances C_{CG1}, C_{CG2}, collector-emitter capacitances C_{CE1}, C_{CE2}, gate-emitter capacitances C_{GE1}, C_{GE2}, collector inductances L_{C1}, L_{C2}, gate inductances L_{G1}, L_{G2}, and emitter inductances (i.e., common source inductances) L_{E1}, L_{E2}. Also, driving

voltage V_{DR}, outer gate resistance R_G, and inner gate resistance R_{G1} and R_{G2} are included in the following analysis. The model also includes MOV V-I characteristics, its associated capacitance C_{MOV}, and parasitic inductance L_{MOV} contributed by the interconnection (e.g., bus bar) between the IGBT module and the MOV. Additionally, L_{sys} and V_{DC} are the system inductance and DC bus voltage of the system under protection, respectively.

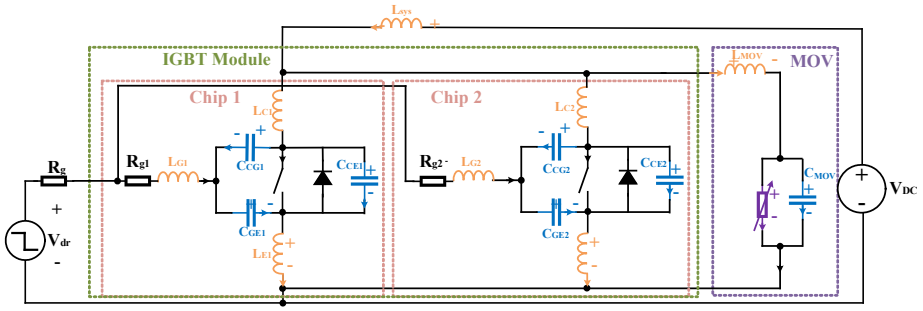


Figure 5. 2: SSCB detail model.

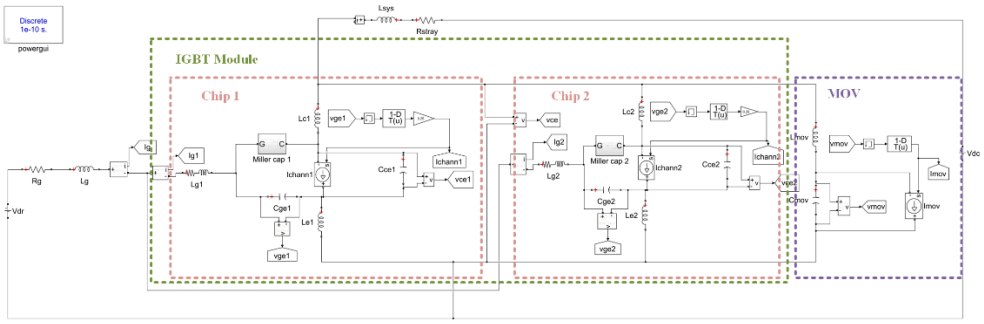


Figure 5. 3: MATLAB/Simulink model for the IGBT module with two chips.

For the SSCB model in Figure 5. 2, a MATLAB/Simulink model with IGBT details is built up in Figure 5. 3. The two chips with mismatched collector-gate capacitances, collector-emitter capacitances, gate-emitter capacitances, collector inductances, emitter inductances, and V-I characteristics in the simulation are considered. Based on the

datasheet, the *V-I* characteristic is represented with a 1-dimensional look-up table (LUT), and the parasitic values are selected. It is noted that considering that there are two chips in the module, the value utilized in the model per chip is scaled based on the IGBT module parameter in the datasheet. Moreover, the nonlinear characteristic of the Miller capacitor of the IGBT and *V-I* curve of the MOV are also included in the simulation.

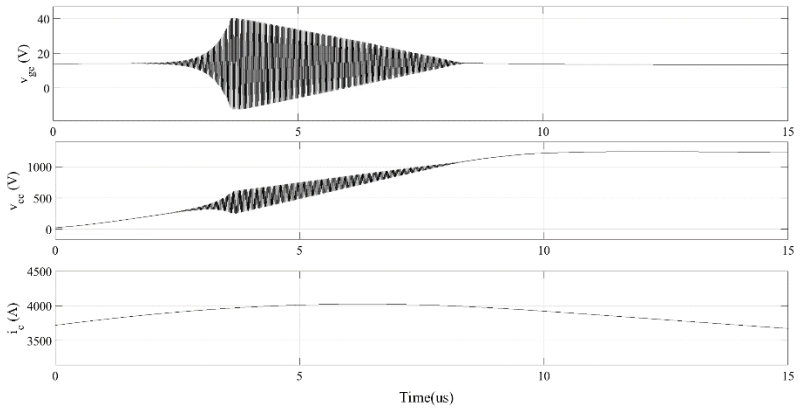


Figure 5. 4: Simulation waveform for chips with different parameter values.

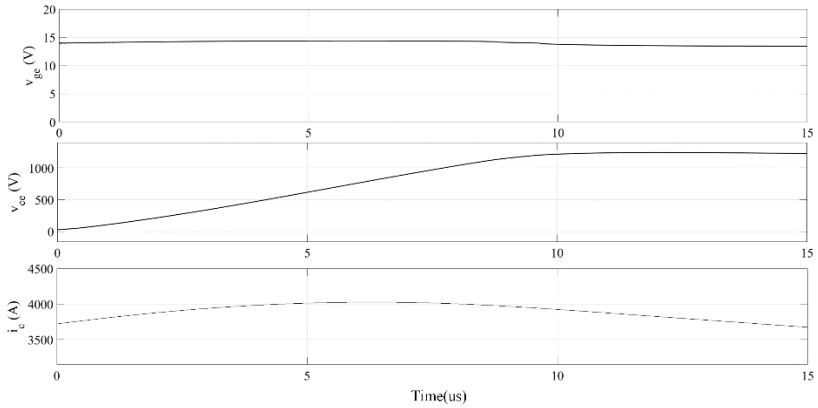


Figure 5. 5: Simulation waveform for chips with different parameter values.

Following the same test shown in Figure 5. 1, Figure 5. 4 shows the v_{GE} and v_{CE} waveforms when the module enters the active region in the simulation. It can be found that v_{GE} and v_{CE} start to oscillate when the module enters the active region, which agrees with

the experimental waveforms in Figure 5. 1. It is noted that when the two chips share the same parameter values, the simulation results in Figure 5. 5 shows that there is no oscillation on v_{GE} and v_{CE}, which further proves that the chip characteristics difference aggravates the oscillation. The oscillation frequency when the IGBT enters the active region has been analyzed in [113] through small-signal analysis, which will not be repeated here. This chapter furthers the understanding with the consideration that the chips with parameter mismatch could further worsen the oscillation.

To suppress the oscillation, it is of vital significance to determine which parameters play an important role during the oscillation. Thus, the sensitivity analysis is conducted based on MATLAB/Simulink to identify the most critical impact factor(s) on the oscillation.

The maximum variance value of v_{CE} is identified as one of the essential dynamic performance characteristics to measure the severity of the oscillation in the sensitivity analysis.

$$\delta^2 = \frac{\sum (X_i - \mu)^2}{N} \tag{5. 1}$$

where N is the number of samples; μ is the mean value of the samples; X_i is the ith sample value.

Parameters	Value	Unit
Collector-emitter capacitance C_{CE1}	0.75	*nF*
Gate-emitter capacitance C_{GE1}	68	*nF*
Collector inductance L_{C1}	50	*nH*
Emitter inductance L_{E1}	10	*nH*
Gate inductance L_{G1}	30	*nH*
Gate resistance R_{G1}	1	*mΩ*
Gate threshold voltage V_{TH1}	7.9	*V*
Transconductance *gfs1*	304.8	*S*

Table 5. 2: Parameters of chip 1.

Parameters	Min.	Max.	Unit
Collector-emitter capacitance C_{CE2}	0.67	0.83	nF
Gate-emitter capacitance C_{GE2}	61	75	nF
Collector inductance L_{C2}	45	55	nH
Emitter inductance L_{E2}	9	11	nH
Gate inductance L_{G2}	27	33	nH
Gate resistance R_{G2}	0.9	1.1	$m\Omega$
Gate threshold voltage V_{TH2}	7.2	8.8	V
Transconductance $gfs2$	274.5	335.5	S
MOV parasitic capacitance C_{MOV}	2.7	3.3	nF
Parasitic inductance between IGBT and MOV L_{MOV}	0.09	0.11	μH

Table 5. 3: Input variables range for sensitivity analysis.

Considering that the internal device can have different parasitic parameters, the parameters of one device and corresponding parasitics in Figure 5. 2 are selected as sensitivity analysis variables, which include collector inductance L_{C1}, L_{C2}, gate inductance L_{G1}, L_{G2}, emitter inductance L_{E1}, L_{E2}, collector-emitter capacitance C_{CE1}, C_{CE2}, and gate-emitter capacitance C_{GE1}, C_{GE2}. Then, the device gate threshold V_{TH} and transconductance g_{fs} are also selected as input variables. Moreover, the parasitic capacitance and inductance of the MOV are analyzed. To analyze which IGBT chip's characteristics mismatch matter on the oscillation, the parameter/parasitic values associated with IGBT chip 1 are fixed in the simulation, shown in Table 5. 2. Then, IGBT chip 2's parameter/parasitic values are changed in the sensitivity analysis to get different variance values of the collector-emitter voltage during the oscillation, which is utilized to find out which parameter's difference matters most for the oscillation. Thus, 500 samples are randomly selected based on the Monte Carlo method with the parameter sweep ranges listed in Table 5. 3. Additionally, the MOV parasitic capacitance C_{MOV} and the parasitic inductance between IGBT and MOV L_{MOV} are also listed in Table 5. 3 for sensitivity analysis to study the influence of the MOV on the oscillation when IGBT enters the active region.

Based on the 500 randomly generated samples, Figure 5. 6 shows the scatter plot of the sensitivity analysis. The scatter subplots display the variance value of v_{CE} as a function of each parameter in the parameter set. The number of points in each scatter plot equals the number of rows in the parameter set. The last column of subplots displays histograms of the probability distribution of the evaluated cost function values. It can be found in Figure 5. 6 that the variance value of v_{CE} is highly monotonically related to the parameter L_e, indicating that the mismatch of L_e between chip 1 and chip 2 has a significant influence on the oscillation.

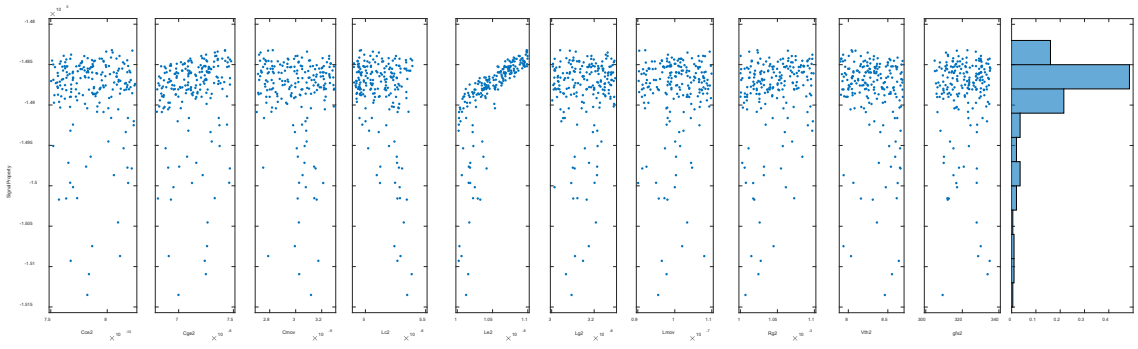


Figure 5. 6: Scatter plot of the sensitivity analysis for SSCB.

Then the quantitative analysis is performed to investigate the influence of L_{e2}, L_{c2}, R_{g2}, V_{TH2}, C_{ge2}, C_{ce2}, L_{g2}, C_{MOV}, L_{MOV}, and g_{fs2} on the variance of v_{CE} during the oscillation with different number of chips. Results are illustrated in Figure 5. 7 with tornado plots. Seven indexes (i.e., correlation, rank correlation, Kendall correlation, standardized regression, rank standardized regression, partial correlation, and rank partial correlation) are used to quantify the influence of the input variables on the maximum variance of v_{CE} during the oscillation. Correlation is utilized to analyze how the input variables and the

variance value of v_{CE} are related; Standardized regression is used to analyze how the input variables linearly influence the maximum variance value of v_{CE}. Partial correlation indicates how the input variables and the maximum variance value of v_{CE} are related without the influence of the other variables. In the tornado plot, the variables are sorted based on the correlation coefficient, which means that the L_{e2} has the most influence on the variance value of v_{CE}.

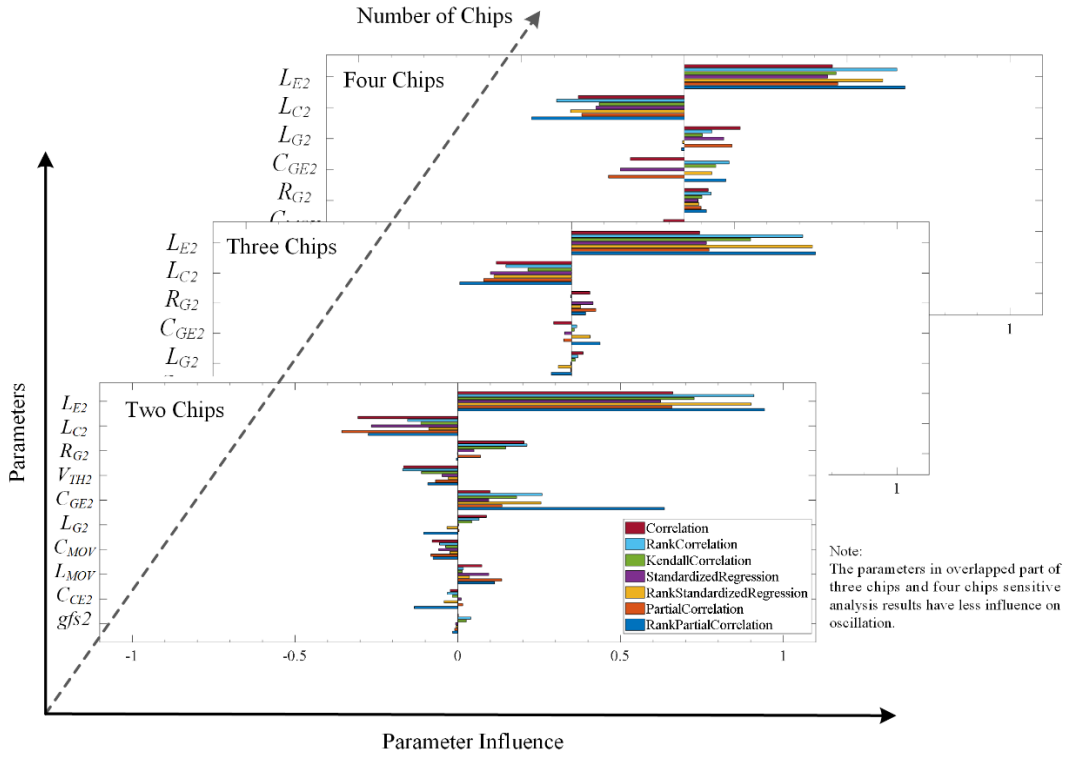


Figure 5. 7: Parameter influence on the variance value of v_{CE}.

The values of the seven indexes are located between -1 and +1. The magnitude indicates how much the maximum variance value of the v_{CE} is influenced by the corresponding parameter, and the sign illustrates the increase of the corresponding parameter value relates to an increase or decrease of the maximum variance value of the

v_{CE}. Specifically, L_{E2}, R_{G2}, C_{GE2}, $L_{G2,}$ and L_{MOV} have positive correlation coefficients, indicating that their increase will increase the maximum variance value of v_{ce}. Meanwhile, L_{C2}, V_{TH2}, and C_{MOV} have negative correlation coefficients, indicating that their decrease will increase the maximum variance value of v_{ce}. Considering that parameter values of chip 1 are fixed in the sensitivity analysis, the results in Figure 5. 6 and Figure 5. 7 further prove that the mismatch between chip 1 and chip 2 can aggravate the oscillation.

	L_E	L_C	R_G	V_{TH}	C_{GE}	L_G	C_{MOV}	L_{MOV}	C_{CE}	gfs
Correlation	**	*	*	*	*	*	*	*	--	--

**: Correlation greatly *: Correlation slightly --: Weak correlation

Table 5. 4: The correlation of different parameters.

Thus, based on the result of the tornado plot in Figure 5. 7, the difference in the L_E, L_C, R_G, V_{TH}, C_{GE}, L_G, C_{MOV}, and L_{MOV} can aggravate the oscillation. Meanwhile, the difference in the C_{CE} and g_{fs} do not have so much influence on the oscillation. Table 5. 4 summarizes the correlation of different parameters

5.4 Oscillation suppression methods

According to the analysis in Section 5.3, to suppress the oscillation, it is of vital significance to remove the mismatch among different IGBT chips. However, it is hardly possible for the manufacturer to make every chip identical; changing the module package's inner parasitic parameters is also challenging for the user. Therefore, a gate drive-based oscillation suppression method is preferred. Figure 5. 8 illustrates the gate drive circuit of the SSCB. As the main function circuit to detect the short circuit fault, the detection circuit is leveraged to detect v_{CE}. The detected value is compared with the threshold voltage through the comparator to trigger the protection with a fault signal. To reduce *di/dt* during

the turn-off process, R_{soft} is leveraged to reduce the turn-off speed of the IGBT when the fault occurs. Moreover, R_{g_on} and R_{g_off} are the external gate resistors to control the turn-on and turn-off speed of the IGBT. The gate turn-on voltage V_{CC}, turn-off voltage V_{EE}, and the MOSFETs S_{1_L} and S_{2_L} comprise the gate drive buffer circuit to turn on/off the IGBT.

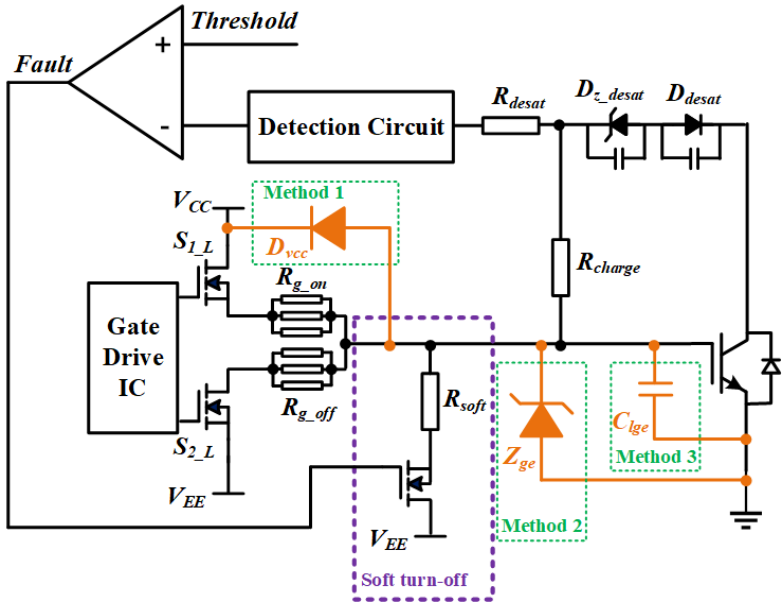


Figure 5. 8: SSCB gate drive with the proposed oscillation suppression methods.

The test waveforms in Figure 5. 1, and the simulation waveforms in Figure 5. 4 show that v_{GE} constantly oscillates with v_{CE}. When the IGBT enters the active region, according to the *V-I* output characteristics, v_{CE} is highly related to v_{GE}. Accordingly, we can stabilize v_{GE} to suppress the oscillation on v_{CE} when the IGBT enters the active region.

The most direct way is to increase the gate loop resistance by increasing the external gate resistance, which can suppress the gate oscillation. It can be realized by increasing the value of R_{g_on}.

Besides the approach to increase the gate loop resistance, three other oscillation suppression methods are proposed in this section, as illustrated in Figure 5. 8. The core

principle of the three proposed solutions is to stabilize v_{GE}, and then suppress the v_{CE} oscillation. The proposed methods include:

Method 1: a diode D_{VCC} is anti-paralleled with the gate resistor to directly connect V_{CC} and the IGBT gate terminal to limit v_{GE} to V_{CC}. When the gate terminal voltage exceeds V_{CC}, it will be clamped to remain at V_{CC}.

Method 2: a Zener diode Z_{ge} is paralleled with the IGBT collector and emitter terminals. The Zener diode clamps the potential difference between the ground (emitter) and collector. Thus, the v_{GE} value cannot be higher than the breakdown voltage of the Zener diode. It is noted that the Zener voltage should be a little higher than V_{CC} to prevent the influence of the Zener diode on V_{CC} during the normal operation of the SSCB.

Method 3: a decoupling capacitance C_{lge} is paralleled with the collector and emitter terminals of the IGBT to absorb noise current (e.g., displacement current during *dv/dt*), and then stabilize v_{GE}.

5.5 Experimental verification

The effectiveness of the proposed oscillation suppression methods are verified with the platform built in Chapter 3. CWTMini HF30B Rogowski coil with a 6kA peak-current rating is used to measure the system current. The differential probe TMDP0200 is used to measure the voltage.

5.5.1 Overview of the gate drive circuit

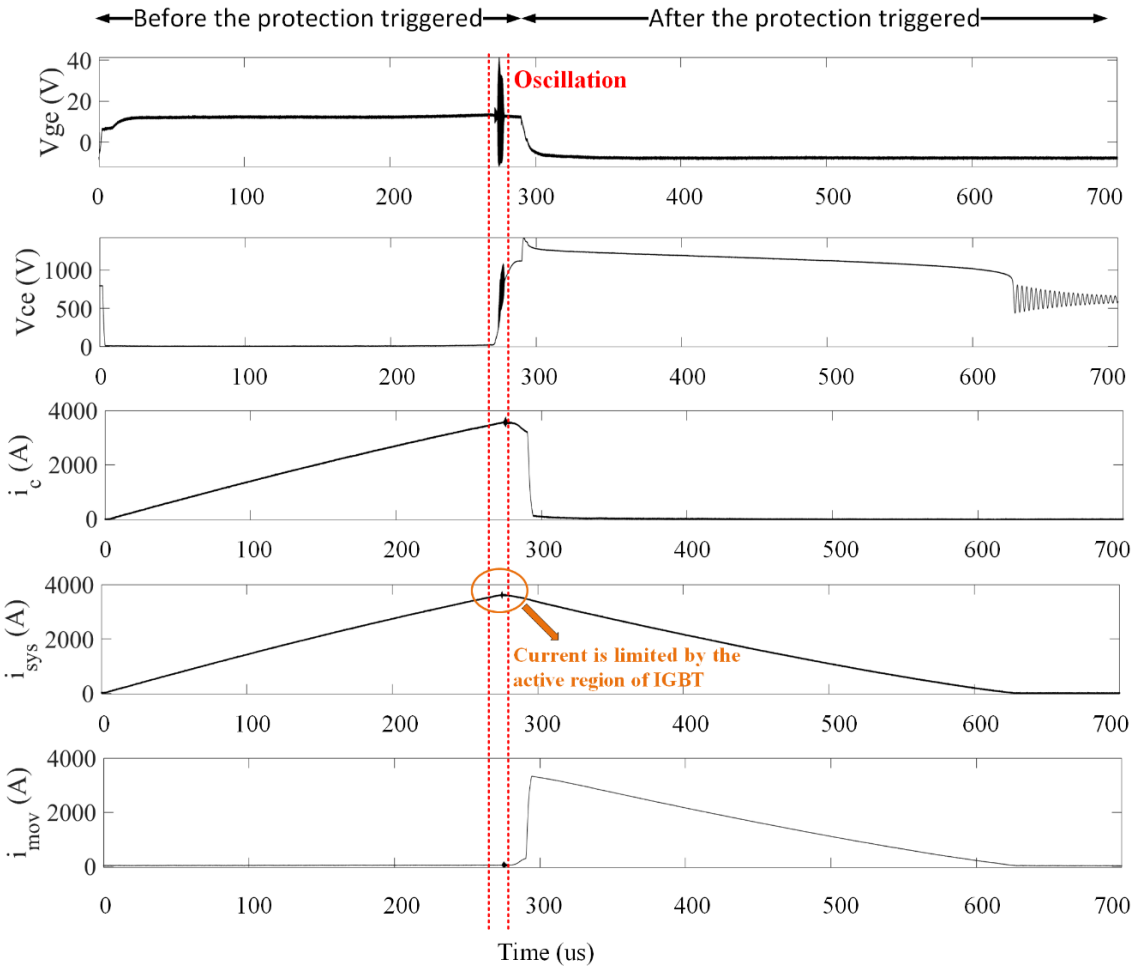


Figure 5. 9: Waveform of the SSCB without the oscillation suppression methods.

Figure 5. 9 illustrates the waveforms of v_{GE}, v_{CE}, the IGBT module current *ic*, the system current i_{sys}, and the current flowing through the MOV i_{MOV} during the whole process of a short circuit fault. It can be observed that when the IGBT enters the active region, there is obvious oscillation on v_{CE} and v_{GE}. The system's current i_{sys} is limited by the IGBT when the IGBT enters the active region.

5.5.2 *Verification of the increasing gate loop resistance method*

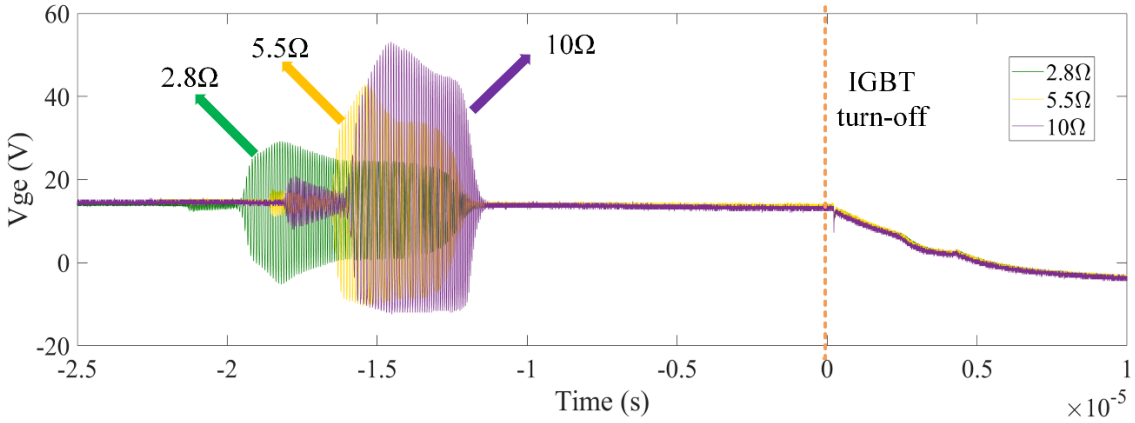


Figure 5. 10: v_{GE} when IGBT enters the active region with different gate resistance.

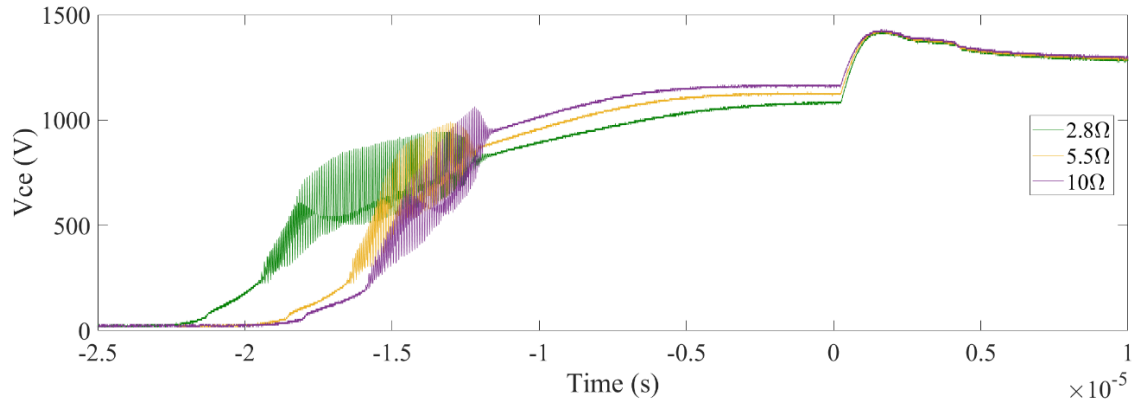


Figure 5. 11: v_{CE} when IGBT enters the active region with different gate resistance.

To validate the effectiveness of the mitigation approach of increasing the gate loop resistance, additional outer gate resistors with 2.8Ω, 5.5Ω, and 10Ω are introduced into the gate loop, respectively. Figure 5. 10 and Figure 5. 11 illustrate the waveforms of v_{GE} and v_{CE} with different gate loop resistances to suppress the oscillation when the IGBT enters the active region. The SSCB is turned off at 0s. Before 0s, the IGBT enters the active region with a specific gate loop resistor. It can be found that there still is obvious oscillation when the gate loop resistance increases to 10Ω. With the gate loop resistance increase, the v_{CE} oscillation performance becomes a little better. However, the oscillation on v_{GE} and v_{CE} is

still obvious, which may cause damage to the SSCB. The reason is that increasing lumped gate resistance is not good enough to dampen the oscillation on the gate terminal. Moreover, increasing the gate loop resistance will affect the switching speed of the power semiconductor, which is important to the SSCB. Therefore, it is not recommended to suppress the oscillation by increasing the gate loop resistance for this kind of oscillation.

5.5.3 Verification of the proposed methods

As mentioned in Section 5.4, three other methods are also evaluated in this section. Figure 5. 12 illustrates the waveforms of v_{GE}, v_{CE}, and i_c when the IGBT enters the active region with different oscillation suppression methods. According to the test results, it can be found that the diode-based method 1 and the Zener diode-based method 2 work well. The gate voltage is well clamped by both methods; and accordingly, the oscillation on v_{ce} is also damped. Although there still is a little oscillation remaining, it will not influence the operation of the SSCB. It is noted that the oscillation cannot be removed completely with method 1 and method 2. Because the oscillation source is from the inner construction of the IGBT module, method 1 and method 2 cannot change the inner construction of the IGBT module. Table 5. 5 summarizes the effectiveness of the proposed suppression methods. It can be found that the proposed methods can reduce the maximum v_{CE} amplitude during oscillation by about 50%.

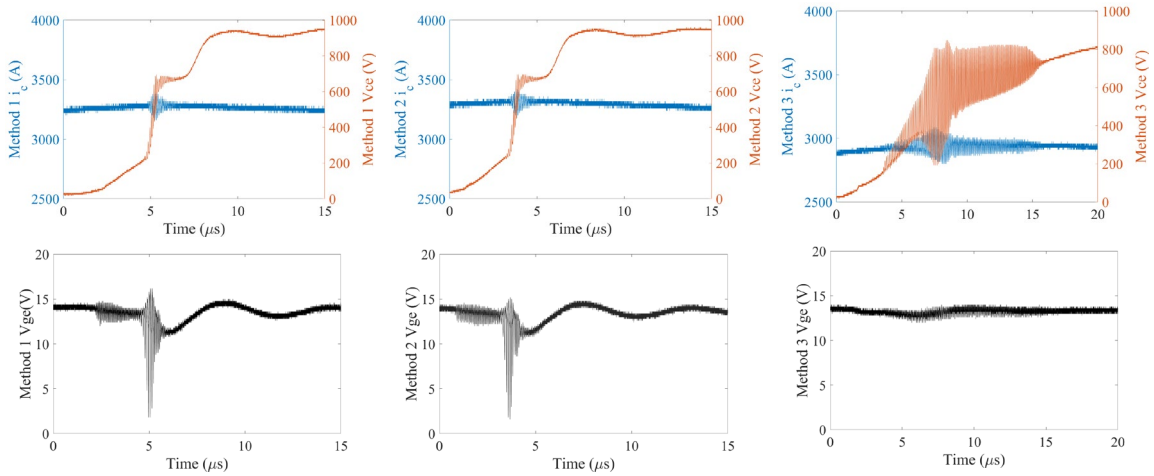


Figure 5. 12: Waveforms of SSCB with the proposed oscillation suppression methods.

	Maximum v_{ce} amplitude during oscillation (V)	Oscillation index
Without suppression	403	100%
Method 1	196	48.6%
Method 2	201	49.9%
Method 3	616	152.9%

Table 5. 5: Maximum v_{CE} amplitude during oscillation under different conditions

However, from Figure 5. 12, the additional C_{ge}-based method 3 does not work well and even makes the oscillation on v_{CE} more severe. Meanwhile, v_{GE} is much more stable than method 1 and method 2. Initially, C_{lge} is to increase the value of C_{GE} to stabilize v_{ce}. However, the additional gate-emitter capacitance can form the first-order oscillation with L_G, which aggravates the oscillation and aligns with the sensitivity analysis in Section 5.3.

Therefore, the traditional method of increasing the gate loop resistance has limited effectiveness in oscillation suppression. Methods 1 and 2 are preferred for damping the oscillation. However, method 3 will aggregate the oscillation.

5.6 Conclusion

This chapter analyses the mechanism causing oscillation of v_{GE} and v_{CE} when the lightweight DC-SSCB without a current limiting inductor enters the active region. Three suppression approaches are proposed by stabilizing the gate-emitter voltage. Analysis results show that the difference in L_E, L_C, R_G, V_{TH}, C_{GE}, L_G, C_{MOV}, and L_{MOV} can aggravate the oscillation. The mismatch between L_E has the most influence on the oscillation. Then, experiment results illustrate that clamping v_{GE} by paralleling a Zener diode between the gate and emitter terminals or connecting positive driving voltage and gate terminal through a clamping diode can effectively suppress the oscillation on v_{CE} by about 50%. However, increasing the lumped gate resistance and paralleling an additional gate-emitter capacitor are not effective.

CHAPTER SIX

6 INFLUENCE OF BUS BAR CONNECTION TO SSCB

6.1 Introduction

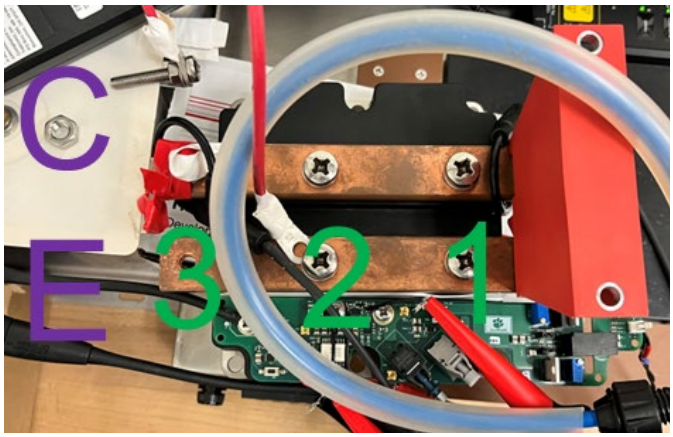


Figure 6. 1: Saturation current under different bus bar connections.

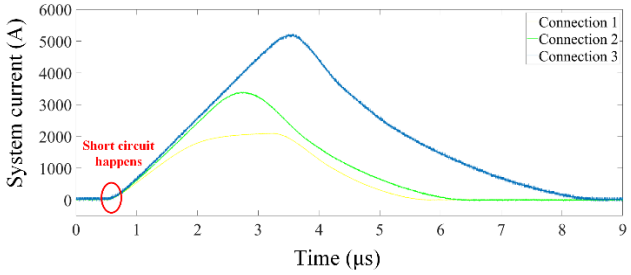


Figure 6. 2: Waveform of system current with different bus bar connections.

For DC-SSCB, the worst scenario is that the system inductance is almost zero (dead short), which means that there is no inductor limiting the system fault current increase. The system fault current can increase to an extremely high value quickly. Meanwhile, considering the system inductance is almost zero, we cannot ignore the influence of the DC-SSCB's parasitic inductance (e.g., bus bar inductance). Figure 6. 1 shows the bus bar connection of the DC-SSCB. One bar connects with the IGBT's collector terminal, and the other bar connects with the IGBT's emitter terminal. However, when the dead short

happens with different bus bar connections, the peak current limitation level (saturation current) is also changed, which is shown in Figure 6. 2. The relation between the bus bar connection and the saturation current is shown in Figure 6. 3. It can be found that connection 1 has the lowest saturation current, while connection 3 has the highest saturation current. In real applications, the high saturation current can damage the current-sensitive power converter. Accordingly, it is important to study the influence of the bus bar connection on SSCB when the dead short happens.

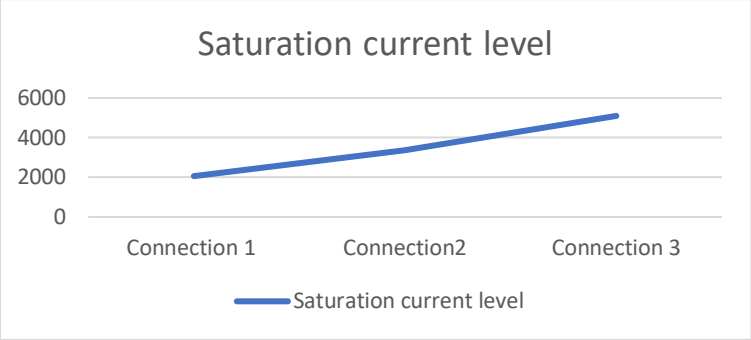


Figure 6. 3: Saturation current under different bus bar connections.

6.2 Parasitic inductance analysis

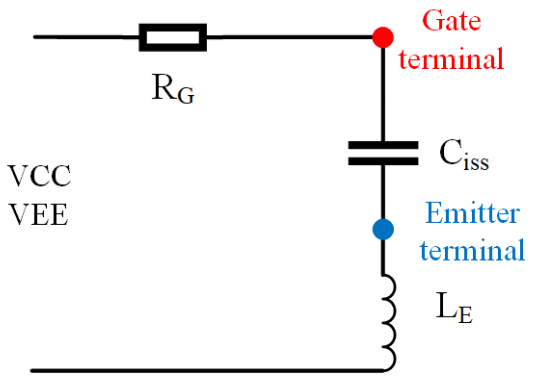


Figure 6. 4: Simplified gate loop schematic.

Because the saturation current is related to the gate voltage, the changing of the saturation current caused by different connections can be explained by the changing of the gate voltage. Spontaneously, as shown in Figure 6. 4, we can assume that the gate voltage can be influenced by the gate loop inductance when high *di/dt* happens which is caused by the dead short. The high *di/dt* during turn-off through the bus bar can induce the electromagnetic field. And the induced electromagnetic field can couple with the gate loop of the gate driver and induce an extra voltage to the gate voltage through L_E. The induced electromagnetic field is related to the current direction and distribution through the bus bar, which makes the different bus bar connections have different L_E and gate voltage to change the saturation current.

To verify the assumption and study the parasitic inductance of the IGBT module, Ansys Q3D Extractor is leveraged to realize the multiphysics parasitic extraction for IGBT module FZ1000R33HE3. Figure 6. 5 demonstrates the 3D model built by Ansys Q3D Extractor.

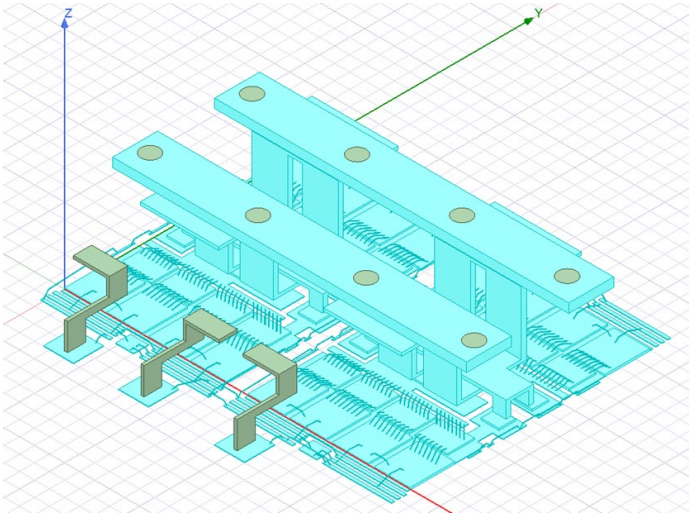
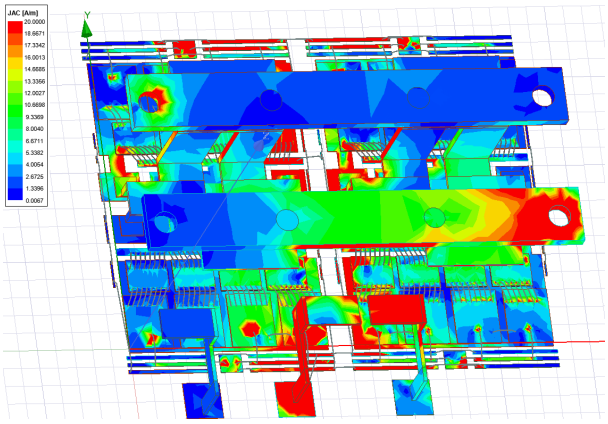
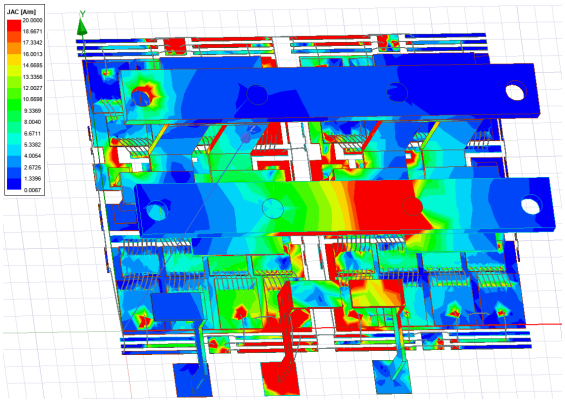


Figure 6. 5: 3D model built by Ansys Q3D Extractor.

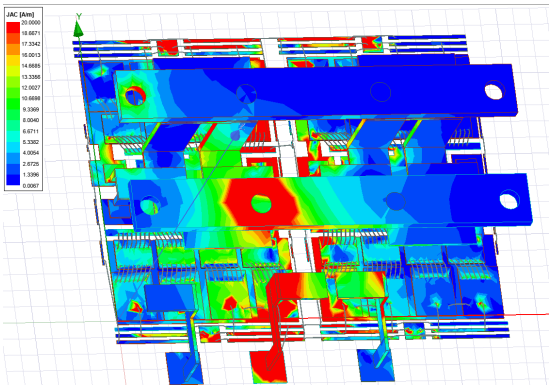
To study the influence of the power loop on the gate loop when the high *di/dt* happens, the IGBT's Kelvin gate terminal, Kelvin emitter terminal, and power collector terminal are assigned as the source excitation, while the power emitter terminal is assigned as the sink excitation in the Q3D simulation. Then, the location of the sink excitation for the power emitter is changed to study the influence of the bus bar's connection to the IGBT's parasitic L_E. Figure 6. 6 illustrates the IGBT's magnetic field strength with different traditional bus bar connections. The red color means a higher magnetic field strength. It can be found that with different bus bar connections, the distribution of th magnetic field strength is different, which means that the L_E can be influenced by the different bus bar connections through the power loop magnetic field.



(a) Connection 1



(b) Connection 2



(c) Connection 3

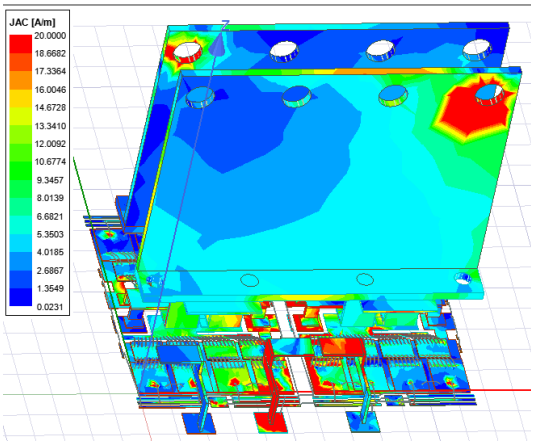
Figure 6. 6：Magnetic field strength with different traditional bus bar connections.

According to the result of the Q3D simulation, Table 6. 1 listed the power collecter to gate terminal inductance, power collecter to Kelvin emitter inductance, and L_E which is the difference between power collecter to Kelvin emitter inductance and power collecter to gate terminal inductance. It can be found that different bus connections result in different L_E values. Then, the voltage induced by different L_E values changes the gate voltage during high *di/dt*. Finally, the different gate voltages generate different saturation currents once high *di/dt* happens.

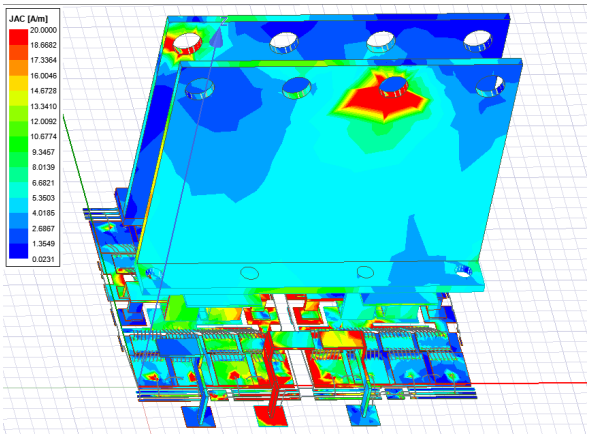
	Power collecter to gate terminal inductance	Power collecter to Kelvin emitter inductance	Mutual emitter inductance (L_E)
Connection 1	13.22nH	20.06nH	-7.38nH
Connection 2	4.73nH	9.74nH	-5.01nH
Connection 3	2.67nH	2.45nH	0.22nH

Table 6. 1: Mutual emitter inductance with different traditional bus bar connections.

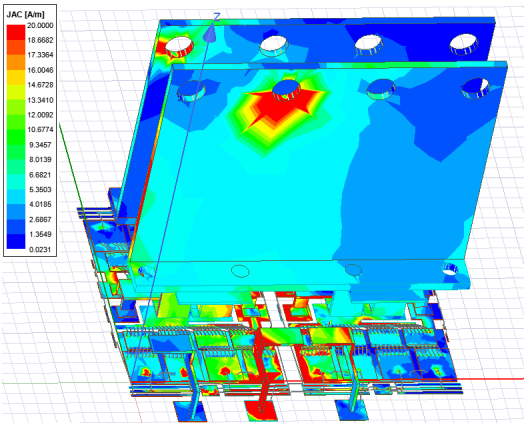
6.3 Saturation current clamping method



(a) Connection 1



(b) Connection 2



(c) Connection 3

Figure 6. 7: Magnetic field strength with different vertical bus bar connections

Based on the analysis in Section 6.2, it is important to eliminate the influence of the power loop on the gate loop. To eliminate the influence of the power loop's electromagnetic field on the gate loop, a vertical bus bar takes place of the traditional bus bar. Figure 6. 7 illustrates the IGBT's magnetic field strength with different vertical bus bar connections. For the vertical bus bar, because the power loop's electromagnetic field is parallel to the gate loop, there will be not too much coupled electromagnetic field for the gate loop. Accordingly, LE generated by the vertical bus bar should be smaller than L_E generated by the traditional bus bar. Table 6. 2 shows the value of L_E with different vertical bus bar connections. The effectiveness of the vertical bus bar can be proved by the comparison between Table 6. 1 and Table 6. 2. Because the vertical bus bar can decrease the value of LE, there will be less change in gate voltage when high di/dt happens, and the influence of bus bar's connection to the saturation current can be eliminated.

	Power collecter to gate terminal inductance	Power collecter to Kelvin emitter inductance	Mutual emitter inductance (L_E)
Connection 1	17.64nH	20.42nH	-2.78nH
Connection 2	10.78nH	12.35nH	-1.57nH
Connection 3	8.46nH	8.78nH	0.32nH

Table 6. 2: Mutual emitter inductance with different vertical bus bar connections.

6.4 Conclusion

This chapter analyses the influence of the bus bar's connection to the IGBT module-based SSCB when the dead short happens (system inductance is almost zero). With the help Q3D extractor, when the dead short happens, it is proven that the gate loop can couple with the electromagnetic field generated by the power loop. The induced voltage can influence the gate voltage and saturation current. To eliminate the influence of the electromagnetic field of the power loop on the gate loop, a vertical bus bar is proposed. Based on the result of the Q3D extractor, the vertical bus bar-based SSCB can have a smaller L_E, which means that the power loop has less impact on the gate loop. Accordingly, the saturation current (maximum limiting current) for SSCB can be no longer influenced by the bus bar connection.

CHAPTER SEVEN

7 GATE DRIVE FOR SYSTEM-FRIENDLY DC SSCB

7.1 Introduction

To better serve the DC distribution system, the new generation DC-SSCB should possess the capabilities to fit with the unique challenges of the modern DC distribution system, e.g., adjustment of fault trigger threshold for different system operation modes; response time adjustment capability according to system level or converter level requirements; sensitive enough to protect the vulnerable interfaced power converter; ride-through capability for the rest healthy parts of the system. Accordingly, to enable DC-SSCB with fault ride-through capability and protect the vulnerable interfaced power converter, this section proposes an intelligent gate drive for DC-SSCB with the current limitation mode to limit the fault current. Moreover, with the proposed discrete components-based intelligent gate drive, the fault trigger threshold and response time of DC-SSCB can be tuned to fit different scenarios.

Meanwhile, to increase the current interrupting capability for DC-SSCB, power semiconductors need to possess a higher pulse current tolerance. Instead of leveraging a power semiconductor with a higher rating power, low temperature is also a proper approach to improve the pulse current tolerance capability of the power semiconductor. Moreover, the low temperature can decrease the on-state resistance to enhance the efficiency of DC-SSCB. Additionally, low-temperature cooling provides a low ambient temperature to allow higher temperature rise and less heat removal. Thus, this section also studies the influence of the low temperature on the performance of DC-SSCB.

Finally, test results from a 200V/150A Gallium nitride (GaN) based DC-SSCB prototype with the current limitation mode verify the proposed intelligent gate drive design for system-friendly DC-SSCB. The performance of the corresponding DC-SSCB has also been tested under different low temperatures.

7.2 Basic of the proposed system-friendly DC-SSCB

7.2.1 Topology the proposed system-friendly DC-SSCB

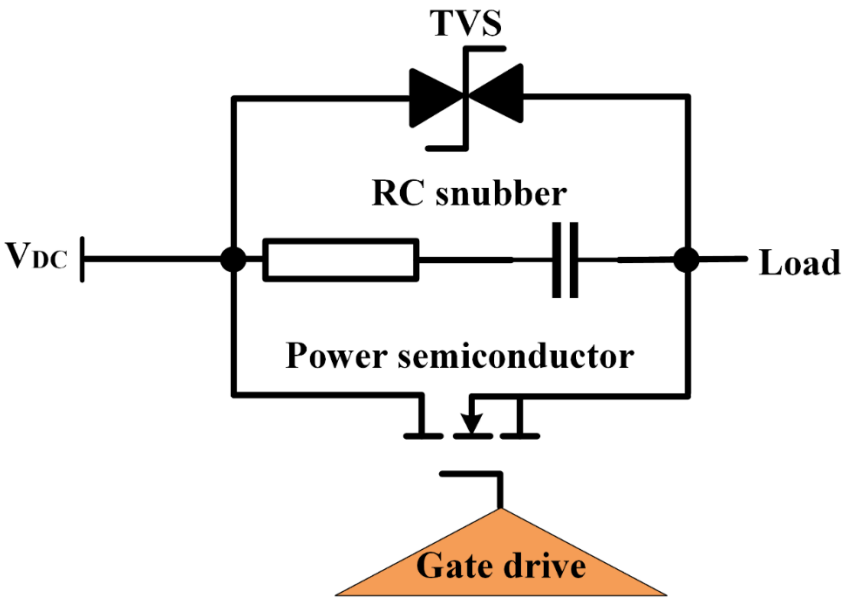


Figure 7. 1: Topology of the system-friendly DC-SSCB.

Based on the lightweight DC-SSCB without current limiting inductor topology in Chapter 3, Figure 7. 1 illustrates the topology of the system-friendly DC-SSCB. Compared with other power semiconductors, GaN possess a lower on-state resistance. Thus, to increase the efficiency of DC-SSCB, GaN is leveraged as the power semiconductor to interrupt the fault current. Transient voltage suppression (TVS) diode and snubber RC

circuit cooperate to absorb the power semiconductor's extra energy during the turn-off interval of the DC-SSCB.

7.2.2 System consideration for DC-SSCB: EAP system as a case

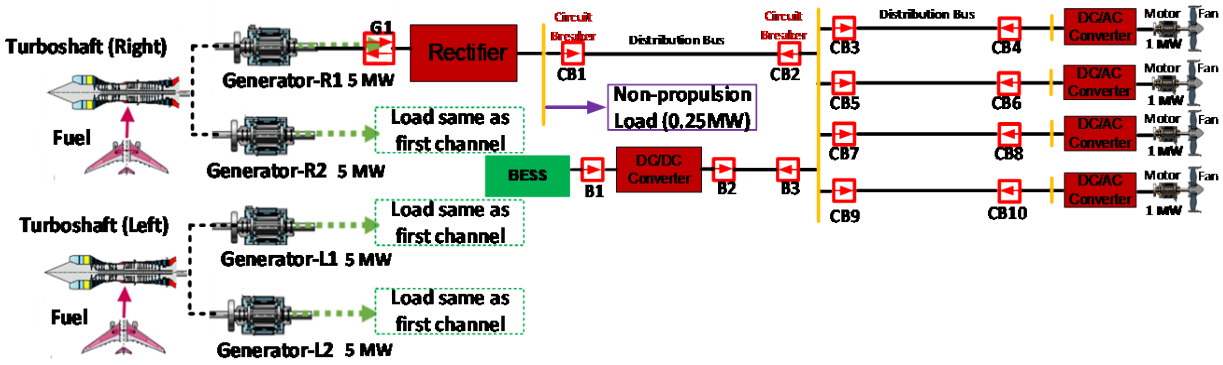


Figure 7. 2: System configuration of the electrified aviation system.

The weight-energy tradeoff is an obstacle to limiting the development of the EAP system. The EAP-related batteries, cables, converters., etc., can take a large proportion of the takeoff weight of the electrified aircraft. Accordingly, as mentioned in section 1, the MVDC system can be an appropriate solution for the EAP system power configuration to reduce the aircraft's weight. As the critical component of the MVDC protection system, a safe, reliable, and lightweight DC-SSCB with a fast response time is of vital significance.

Recently, the cryogenically cooled EAP attracted increasing attention in the aviation industry [121]. From the system level, the supportive power systems for the superconducting motors and generators will become essential. Then, combining superconductive systems with cryogenic power electronics can reduce the system's complexity and improve power density by removing the extra thermal insulation and temperature regulation system. Therefore, to enhance the performance of the DC-SSCB

and the integration of the EAP system, it is significant to develop an SSCB that can leverage the advantages of the cryogenic cooling system.

Figure 7. 2 illustrates the basic MVDC system configuration for the aviation system [122]. It consists of the power converter, BESS, generator, motor, and protection equipment. The breaker and limiter are controlled separately to protect the power system. Circuit breakers are located at both ends of the distribution bus to interrupt the short circuit fault from the motor side or the generator side. The current limiter can be leveraged to limit the inrush current during the system startup and limit the short circuit current or overload current.

For a traditional EAP system, the breaker and the limiter are two different components. In the past decades, there is not so much research on equipment with breaker and limiter functions simultaneously. However, this section proposes a new intelligent gate drive circuit for DC-SSCB, which enables DC-SSCB with current limitation capability. The proposed intelligent gate drive circuit for DC-SSCB with current limitation capability can decrease the complexity, weight, and cost of the EAP protection system.

7.3 Gate drive design for system-friendly DC SSCB

The simplified schematic of the proposed discrete components-based intelligent gate drive circuit for DC-SSCB is illustrated in Figure 7. 3. Compared with the commercial gate drive IC (e.g., ACPL-339J from Broadcom) with integrated functions (e.g., desaturation protection), the proposed discrete components-based intelligent gate drive circuit allows more flexibility for DC-SSCB application, e.g., the current limitation mode

for DC-SSCB, fault trigger threshold adjustment, etc. Moreover, the typical minimum operating temperature for commercial gate drive IC with integrated functions (ACPL-339J) is about 220K (-55°C). Thus, the commercial gate drive IC with integrated functions may meet some problems during low-temperature operation. However, the CMOS technology-based discrete components can help the intelligent gate drive circuit survive at 90K ambient temperature. Table 7. 1 compares the discrete components-based gate drive circuit and commercial gate drive IC.

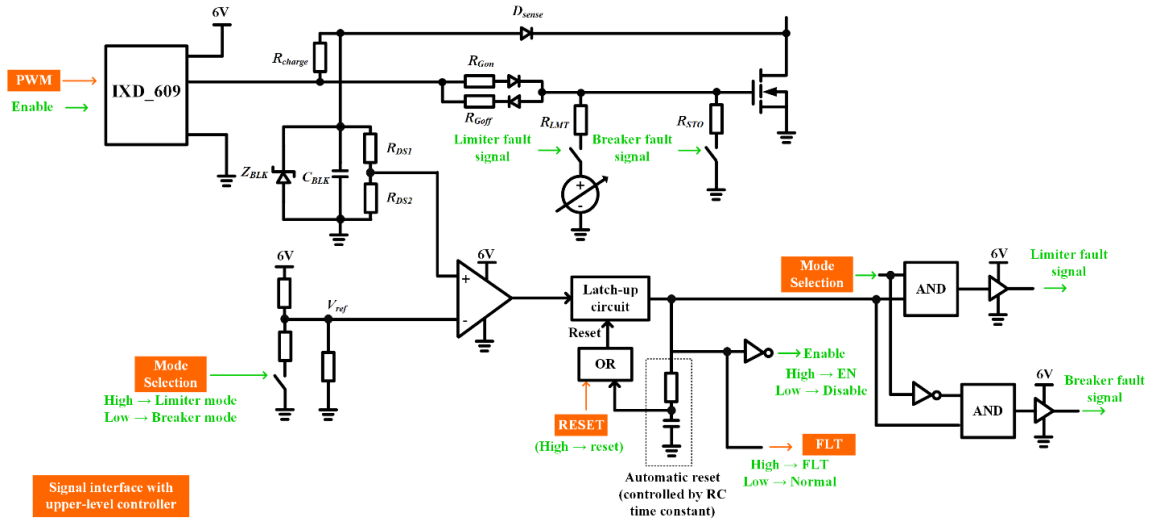


Figure 7. 3: Proposed intelligent gate drive circuit for system-friendly DC-SSCB.

Properties	The discrete components-based gate drive circuit	Commercial gate drive IC (ACPL-339J)
Desaturation protection	Yes	Yes
Tunable fault trigger threshold	Yes	No
Tunable fault response time	Yes	Yes
Flexibility for DC-SSCB application	Yes	No
Low-temperature operation	Yes	No

Table 7. 1: Comparison between different gate drive designs.

Figure 7. 3 also shows the three main input signals (e.g., mode selection signal, PWM signal, and reset signal) and one output signal (e.g., fault signal) of the proposed gate drive circuit interfacing with the upper-level controller.

The mode selection signal controls the operation mode of the DC-SSCB. When the mode selection signal is low, DC-SSCB operates in the traditional breaker mode; when the selection signal is high, DC-SSCB operates in the current limiter mode. PWM signal is leveraged to control the power semiconductor. The reset signal can clear the detected fault and help the DC-SSCB back to under the control of the PWM signal. Finally, the intelligent gate drive circuit can generate a fault signal and send it to the upper-level controller when the fault is detected.

7.3.1 Gate drive design for breaker mode

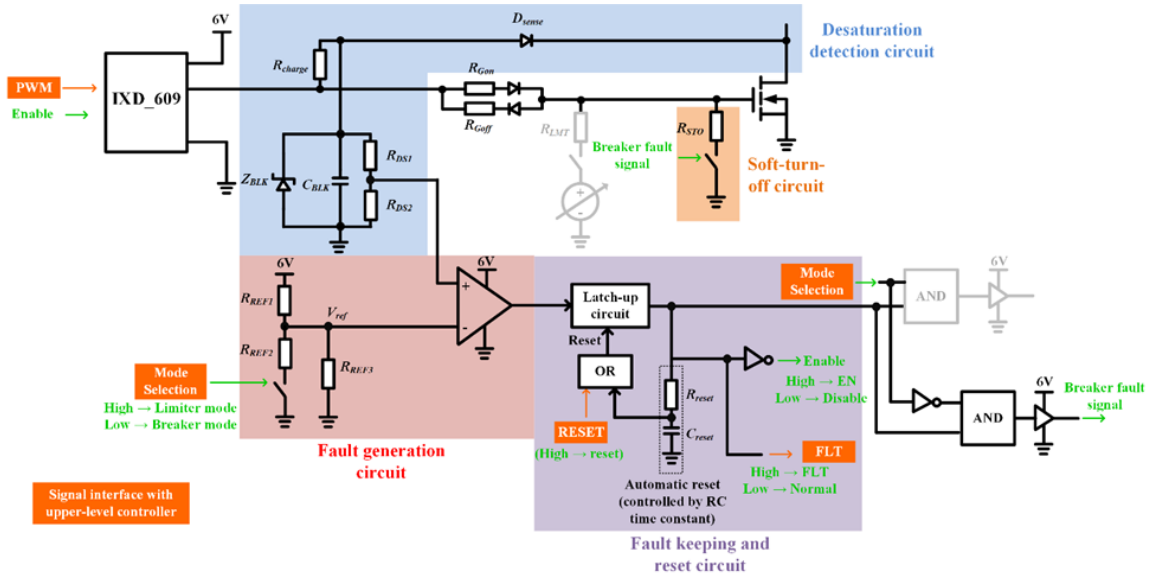


Figure 7. 4: Proposed gate drive circuit with breaker mode.

Figure 7. 4 illustrates the schematic of the intelligent gate drive circuit for system-friendly DC-SSCB under the breaker mode. When the mode selection signal is low, the DC-SSCB will operate in the breaker mode. The grey circuit parts are for the limiter mode and do not work in the breaker mode. With the input PWM signal, CMOS technology-based basic gate drive IXD_609 is leveraged to control the DC-SSCB during normal operation.

7.3.1.1 Detail of gate drive design for DC-SSCB breaker mode

The breaker mode intelligent gate drive circuit comprises the desaturation detection circuit, fault generation circuit, fault keeping and reset circuit, and soft-turn-off circuit.

As shown in the blue part of Figure 7. 4, the short circuit fault detection is realized by desaturation detection. The principle of desaturation detection has been introduced in section 3. The desaturation detection circuit is composed of the sensing diode D_{sense}, charging resistor Rcahrge, blanking capacitor C_{BLK}, protection Zener diode Z_{BLK}, and the voltage divider formed by R_{DS1} and R_{DS2}. D_{sense} interfaces with the drain terminal of the GaN device to monitor the drain-source voltage v_{DS} during the normal operation of DC-SSCB. The blanking capacitor C_{BLK} is charged by the gate voltage from the gate drive IC IXD_609 through the charge resistor R_{charge} to provide the blanking time during the turn-on transition and is utilized to immune the noise from the power stage during the operation. Z_{BLK} is leveraged to protect the input pin of the comparator in the fault generation circuit. The sensed v_{DS} can be adjusted by R_{DS1} and R_{DS2} to meet different system design requirements.

$$v_{DS\_adj} = \frac{R_{DS2}}{R_{DS1} + R_{DS2}} \times v_{ds} \quad (7.1)$$

The fault generation circuit comprises the reference voltage V_{ref} generation circuit and a comparator. With the control of mode selection signal, breaker mode and limiter mode have different V_{ref}. V_{ref} for limiter mode should be smaller than breaker mode. That is because limiting the system's fault current is always good as soon as possible to protect the vulnerable interfaced power converter or bypass the short circuit fault before the fault is cleared. For breaker mode, if V_{ref} is so small, DC-SSCB may be too sensitive to trigger the protection by mistake. Then V_{ref} will be compared with the v_{DS_adj} from the desaturation detection circuit through the comparator. Once v_{DS_adj} is higher than V_{ref}, the comparator can generate a high-level pulse and send it to the fault-keeping and reset circuit.

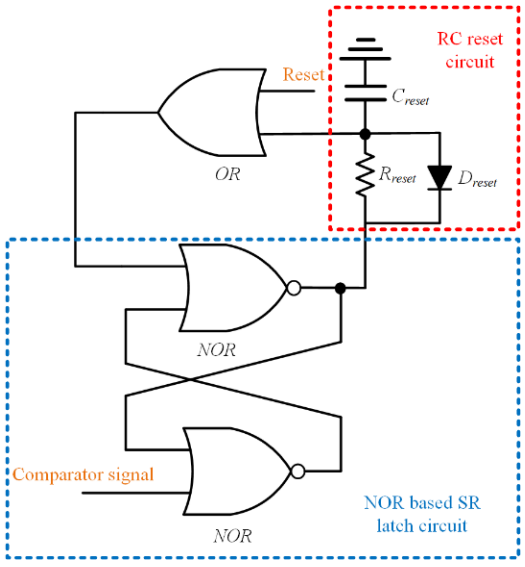


Figure 7. 5: Detail of the SR latch circuit and corresponding RC reset circuit.

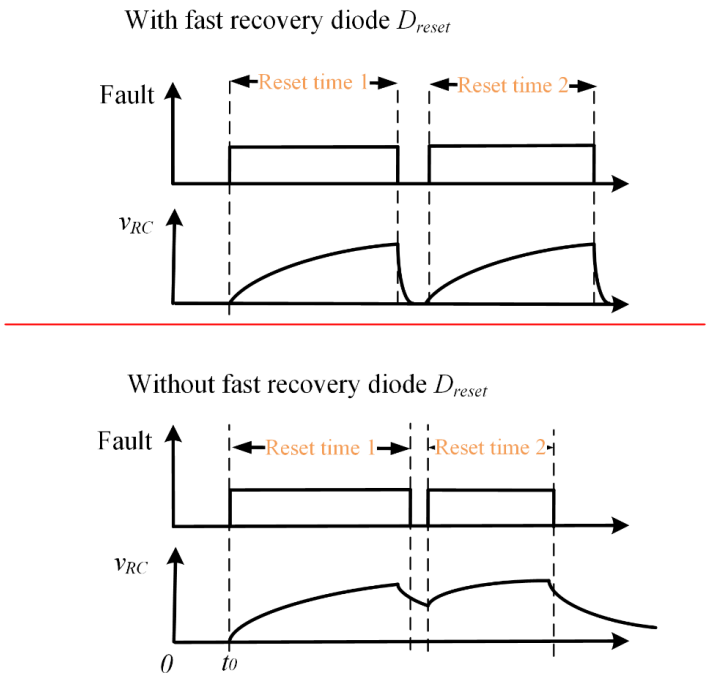


Figure 7. 6: Reset time waveform when two consecutive fault signals exist.

As illustrated in Figure 7. 5, the fault keeping and reset circuit comprises a NOR-based SR latch circuit, an RC reset circuit, and an OR logic gate. When the comparator detects the fault, the high-level pulse will be delivered to the NOR gate-based SR latch circuit to keep the fault signal. The generated fault signal will be sent to the upper-level controller, and the enable pin of the gate drive IC IXD_609 to disable the function of the gate drive IC. Meanwhile, the RC reset circuit is leveraged to clear the fault signal automatically, and the RC constant determines the reset time. It is noted that the reset diode D_{reset} is to accelerate the discharging time of the RC circuit. Figure 7. 6 shows the reset time waveform with and without Dreset when two consecutive fault signals exist. v_{RC} is the voltage across C_{reset}. The first fault happens at t_0; the fault signal becomes high level, and

C_{reset} begins to be charged. Once v_{RC} arrives at the reset threshold voltage of the RS latch circuit, the fault signal can be cleared. Then, v_{RC} can decrease to 0V immediately for the RC circuit with D_{reset}, while v_{RC} needs to decrease to 0V based on the RC constant for the RC circuit without D_{reset}. If the second fault signal is close to the first fault signal, v_{RC} of the RC circuit with D_{reset} can increase from 0V, which cannot influence the reset time. However, because C_{reset} is still discharging, v_{RC} of the RC circuit with D_{reset} cannot rise from 0V, which decreases the reset time. Therefore, the D_{reset} is essential to the fault reset function. Finally, the input reset signal from the upper-level controller also can clear the fault through the OR logic gate.

Finally, with the help of the inverse and AND logic gates, the fault signal and the mode selection can generate the breaker fault signal. Because the gate drive IC is disabled by the fault signal, the breaker fault signal can control the soft-turn-off branch to gently turn off the power semiconductor. The detail of the soft-turn-off has already been mentioned in Chapter 3.

7.3.1.2 Operation principle of the DC-SSCB breaker mode

Figure 7. 7 shows the typical waveform of the DC-SSCB in breaker mode. There is not so much difference with the analysis in Chapter 4. i_{DS} is the current flow through the GaN device, i_{snub} is the current flow through the RC snubber, and i_{tvs} is the current flow through the TVS. A short circuit fault happens at t_0. At t_1, the sensed v_{DS_adj} is higher than the reference voltage for breaker mode, and the protection is triggered. Then, during the time interval t_1 to t_4, gate-source voltage v_{GS} decreases from turn-on voltage to turn-off

voltage, and the system fault current is interrupted. Finally, after t_4, TVS will gradually dissipate the extra energy from the system.

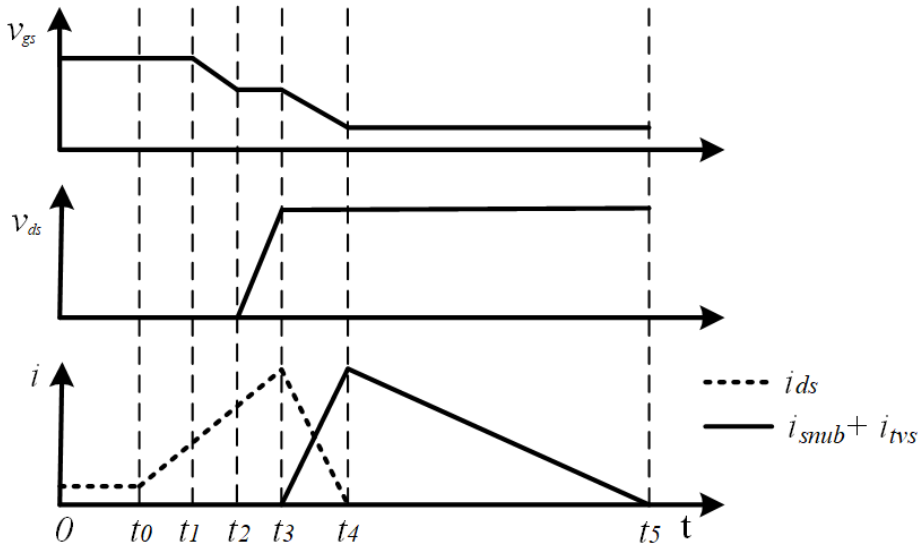


Figure 7. 7: Typical waveform of the DC-SSCB breaker mode.

7.3.2 Gate drive design for limiter mode

Limiter mode utilizes the *V-I* characteristics of the GaN device to limit the system current. Once the intelligent gate drive detects the overcurrent event, the intelligent gate drive will force the GaN device to enter the active region by actively decreasing the gate voltage. Because the GaN device has arrived at the active region, the system current is under the control of the gate voltage. Because the gate voltage and the limited system current are not high during the current limitation period, the GaN device's thermal is not a big concern.

7.3.2.1 Detail of gate drive design for DC-SSCB limiter mode

Figure 7. 8 illustrates the schematic of the intelligent gate drive circuit for system-friendly DC-SSCB under the limiter mode. When the mode selection signal is high, the DC-SSCB will operate in the limiter mode. The grey circuit parts are for the breaker mode and do not work in the limiter mode. With the input PWM signal, CMOS technology-based basic gate drive IXD_609 is leveraged to control the DC-SSCB during normal operation.

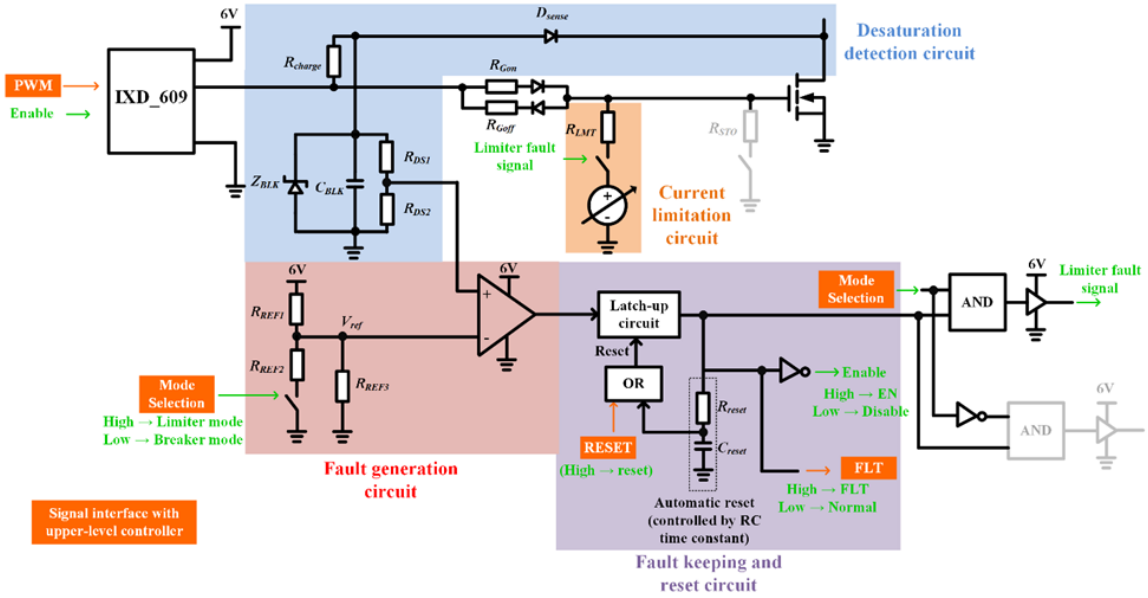


Figure 7. 8: Proposed gate drive circuit with limiter mode.

The limiter mode intelligent gate drive circuit comprises the desaturation detection circuit, fault generation circuit, fault keeping and reset circuit, and current limitation circuit.

Like the breaker mode, desaturation detection is leveraged to detect the overcurrent event. If the detected v_{DS} is higher than the reference voltage for the limiter mode, the fault pulse will be delivered to the fault keeping and reset circuit. Then, the fault signal generated by the fault keeping and reset circuit will be sent to the upper-level controller. It will also

combine with the mode selection signal to create the limiter fault signal. Then, to limit the system current, the current limitation circuit receives the limiter fault signal and decreases v_{GS} to force the GaN device to enter the active region. v_{GS} decides the system's current limitation value based on the *V-I* characteristics of the GaN device.

Considering that the requirement for limiting current varies with different scenarios, it is essential to change v_{GS} online to turn the current limitation level for the modern DC distribution system. Figure 7. 9 shows the current limitation circuit's online adjustable gate voltage implementation circuit. The online adjustable gate voltage implementation circuit consists of one digital potentiometer and an LDO with adjustable output. Most digital potentiometers are built from a resistor ladder integrated circuit shown in Figure 7. 10. The digital potentiometer's internal topology consists of a simple serial string of resistors with digitally addressable electronic switches between the wiper and these resistors. The wiper locates between the point of A (POA) and the point of B (POB). The input of the digital potentiometer determines the address of the wiper. For the digital potentiometer in Figure 7. 9, to control the location of the wiper, the upper-level controller sends the address of the wiper to the digital potentiometer through the serial peripheral interface (SPI) communication. SPI communication relies on the chip selection (CS) signal, the clock (SCK) signal, and the serial data in/out (SDI/SDO) signal to complete the data transmission. With the SPI control, the resistance between POB and the point of the wiper (POW) can be expressed as

$$R_{WB} = \frac{R_{AB} \times N}{N_{step}} \quad (7.2)$$

where N_{step} is the total step for a digital potentiometer (e.g., a 7-bit digital potentiometer has 127 steps, an 8-bit digital potentiometer has 257 steps); N is the wiper address (0-127 for a 7-bit digital potentiometer, 0-257 for an 8-bit digital potentiometer) sent by the SPI communication; R_{AB} is the resistance between POA and POB.

To realize the online adjustable gate voltage control, an adjustable LDO to generate the required gate voltage is also important. The output of the adjustable LDO can be derived as follows

$$V_{LDO\_out} = V_{adj} \times (1 + \frac{R_{WB}}{R_2}) \quad (7.3)$$

where V_{adj} (1.2V-1.3V for most adjustable LDOs) is the voltage across the ADJ and GND of the LDO, providing the reference voltage for the output; R_2 is the resistor between the OUT and ADJ pin of the LDO.

Based on the output equation of the adjustable LDO, with the fixed R_2, the output of the LDO can be controlled by the digital potentiometer.

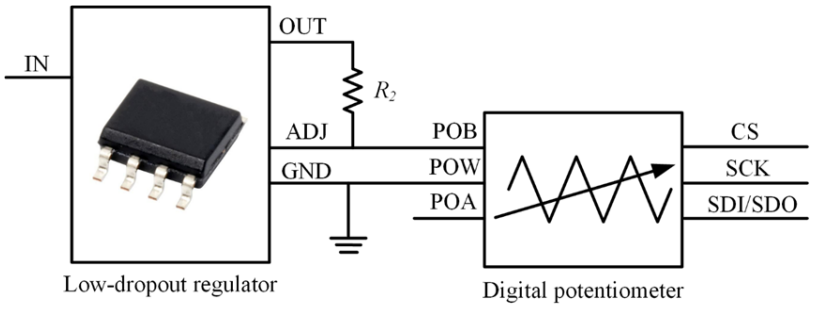


Figure 7. 9: Design of the online adjustable gate voltage implementation circuit.

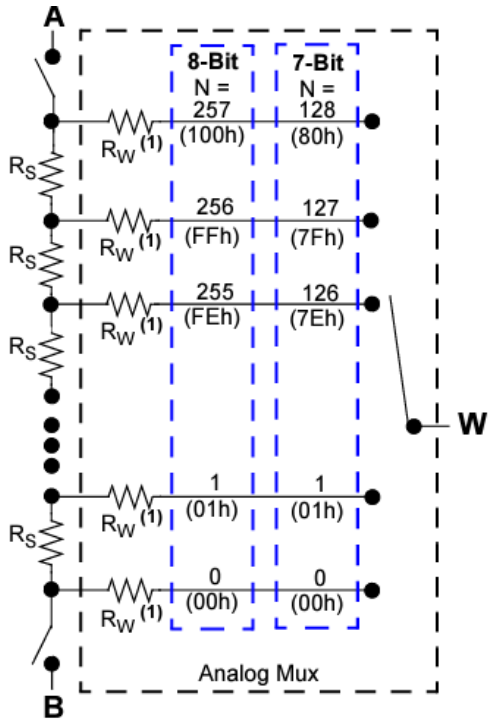


Figure 7. 10: Resistor block of the digital potentiometer.

7.3.2.2 Operation principle of the DC-SSCB limiter mode

The typical waveform for the limiter mode is demonstrated in Figure 7. 11. The overcurrent event happens at t_0, and the limiter mode detects the overcurrent at t_1. It shows the waveform of v_{GS}, v_{DS}, the system's current i_{sys}, the current flowing through TVS i_{TVS}, and the current flowing through the RC snubber i_{snub} during fault current limitation transition. The analysis focuses on the behavior of GaN and TVS.

Before t_0, there is no fault, and the DC-SSCB with limiter mode works in normal condition. GaN keeps at on-state. The drain-source current i_{DS} follows the system current. Meanwhile, there is no current flow through TVS and RC snubber. Then, an overcurrent

event occurs at t_0, and the DC-SSCB protection is triggered at t_1 based on the desaturation protection.

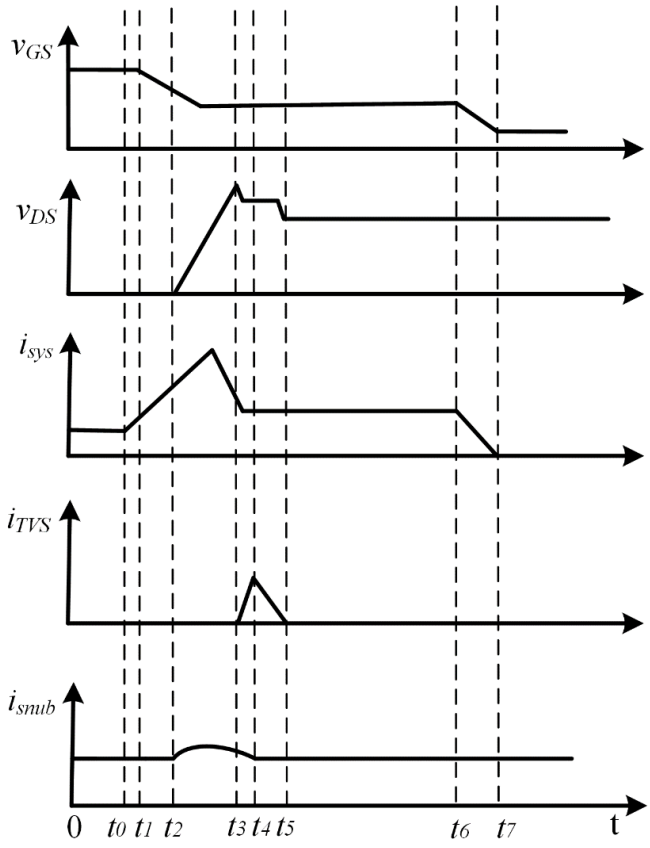


Figure 7. 11: Typical waveform of the DC-SSCB limiter mode.

The current limitation transition consists of six main subintervals, including *subinterval 1*: desaturation detection delay from t_0 to t_1; *subinterval 2*: current limitation delay from t_1 to t_2; *subinterval 3*: current commutation between GaN and RC snubber from t_2 to t_3; *subinterval 4*: current commutation among GaN, RC snubber, and TVS from t_3 to t_4; *subinterval 5*: current commutation between GaN and TVS from t_4 to t_5, and *subinterval 6*: system current limitation from t_5 to t_6. The behavior after t_6 depends on the system operating condition. Significantly, the system's current limitation time relies on the fault

reset time. The detailed operation principle of the DC-SSCB limiter mode is illustrated in Figure 7. 12.

Subinterval I: Desaturation detection delay

During this subinterval, from t_0, the short circuit fault current forces v_{DS} to increase. Because the protection is not triggered, v_{GS} remains at turn-on gate voltage, and GaN operates in the saturation area. Meanwhile, there is no current flow through TVS and RC snubber. Then, at t_1, v_{DS} is higher than the desaturation protection threshold voltage, triggering the protection.

$$\begin{cases} i_{sys} = i_{DS} \\ i_{TVS} = 0 \\ i_{snub} = 0 \end{cases}$$

Subinterval II: Current limitation delay

During this subinterval, the desaturation protection has been triggered. v_{GS} needs to decrease from the turn-on gate voltage to the system current limitation voltage V_{lmt}. In this subinterval, v_{GS} keeps falling, and GaN remains at the saturation area. Meanwhile, there is no current flow through TVS and RC snubber. i_{sys} keeps increasing due to the short circuit.

$$\begin{cases} i_{sys} = i_{DS} \\ i_{TVS} = 0 \\ i_{snub} = 0 \end{cases}$$

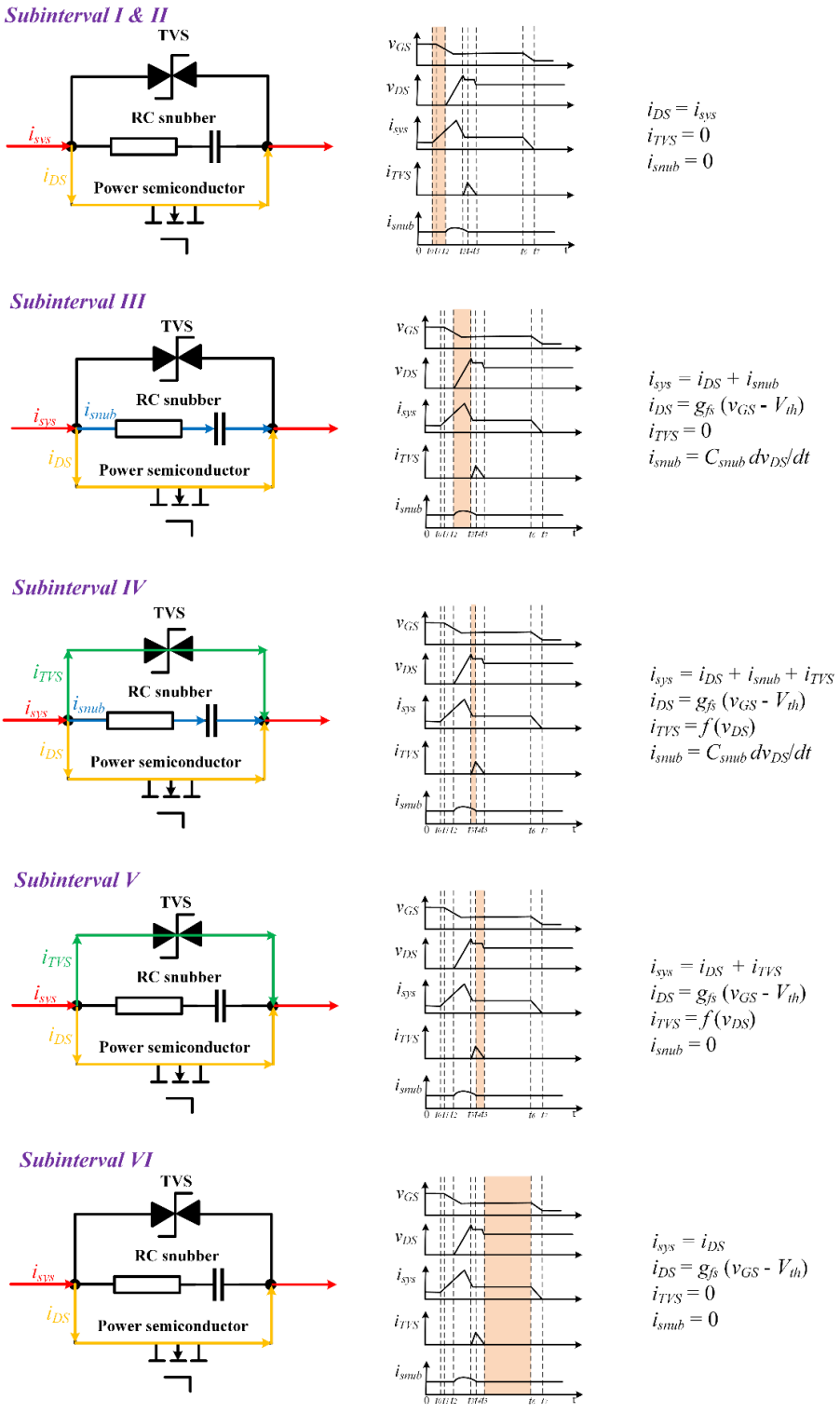


Figure 7. 12: Operation principle of the DC-SSCB limiter mode.

Subinterval III: current commutation between GaN and RC snubber

During this subinterval, the limiter begins to limit i_{sys}, v_{GS} decreases to V_{lmt}, and part of the current commutates from GaN to RC snubber. Specifically, the system fault current enforces the GaN enters the active region, which limits the current flowing through GaN i_{DS} and raises v_{DS} voltage. The high dv_{DS}/dt induces the current flowing through the RC snubber, which makes the current commutate from GaN to the RC snubber. Because v_{DS} does not arrive at the breakdown voltage of TVS, there is no current flowing through TVS. Then, the equation of the current flowing each branch in Subinterval III is expressed as:

$$\begin{cases} i_{sys} = i_{DS} + i_{snub} \\ i_{DS} = g_{fs}(v_{GS} - V_{th}) \\ i_{TVS} = 0 \\ i_{snub} = C_{snub}\, dv_{DS}/dt \end{cases}$$

where g_{fs} represents the transconductance of GaN, V_{th} refers to the threshold voltage of GaN, and C_{snub} is the value of the capacitor in the RC snubber.

Subinterval IV: current commutation among GaN, RC snubber, and TVS

During this subinterval, TVS begins to clamp v_{DS} to absorb the extra energy during the current limitation interval of the limiter mode. To be specific, v_{DS} arrives at the breakdown voltage of TVS, and TVS begins to conduct the current. Because TVS cannot clamp v_{DS} immediately, there is still dv_{DS}/dt that induces the current flowing through the RC snubber. Thus, together with RC snubber, TVS begins to commutate the current from the power semiconductor. Meanwhile, GaN still operates in the active region, and i_{DS} is fixed by v_{GS}. Significantly, if the extra energy during the current limitation interval is small

(v_{DS} cannot achieve the breakdown voltage of TVS), TVS will not be conducted in subinterval IV. Then, the equation of the current flowing each branch in Subinterval IV is derived as:

$$\begin{cases} i_{sys} = i_{DS} + i_{snub} + i_{TVS} \\ i_{DS} = g_{fs}(v_{GS} - V_{th}) \\ i_{TVS} = f(v_{DS}) \\ i_{snub} = C_{snub}\, dv_{DS}/dt \end{cases}$$

where $i_{TVS} = f(v_{DS})$ is based on the *i*-*v* curve of TVS.

Subinterval V: current commutation between GaN and TVS.

TVS is still conducted during this subinterval to dissipate the residual system energy and limit the voltage across the power semiconductor. However, because v_{DS} has already been clamped by TVS, there is no current flow through the RC snubber anymore. Meanwhile, GaN still operates in the active region, and i_{DS} is fixed by v_{GS}. It is also noteworthy that if TVS is not conducted in subinterval IV, TVS will also not be conducted in section V. Thus, the equation of the current flowing each branch in Subinterval V can be derived as:

$$\begin{cases} i_{sys} = i_{DS} + i_{TVS} \\ i_{DS} = g_{fs}(v_{GS} - V_{th}) \\ i_{TVS} = f(v_{DS}) \\ i_{snub} = 0 \end{cases}$$

Subinterval VI: system current limitation

During this subinterval, the residual system energy has been dissipated by TVS, and there is no current flowing through TVS. GaN still operates in the active region, and

i_{DS} is fixed by v_{GS}. Considering that TVS and RC snubber are not conducted, i_{sys} is only determined by i_{DS}. Significantly, the duration time of subinterval VI relies on the fault reset time, which is mentioned in Section 7.2.1.1. Accordingly, the equation of the current flowing each branch in Subinterval VI is yielded:

$$\begin{cases} i_{sys} = i_{DS} \\ i_{DS} = g_{fs}(v_{GS} - V_{th}) \\ i_{TVS} = 0 \\ i_{snub} = 0 \end{cases}$$

Finally, the current limitation ends at t_6. The behavior after t_6 depends on the system operating condition. If the system is shut down due to the short circuit, GaN will be turned off. Meanwhile, if the system is not shut down and the fault current still exists, the intelligent gate drive will decrease v_{GS} again to start a new circle of current limitation.

7.3.3 Gate drive design result

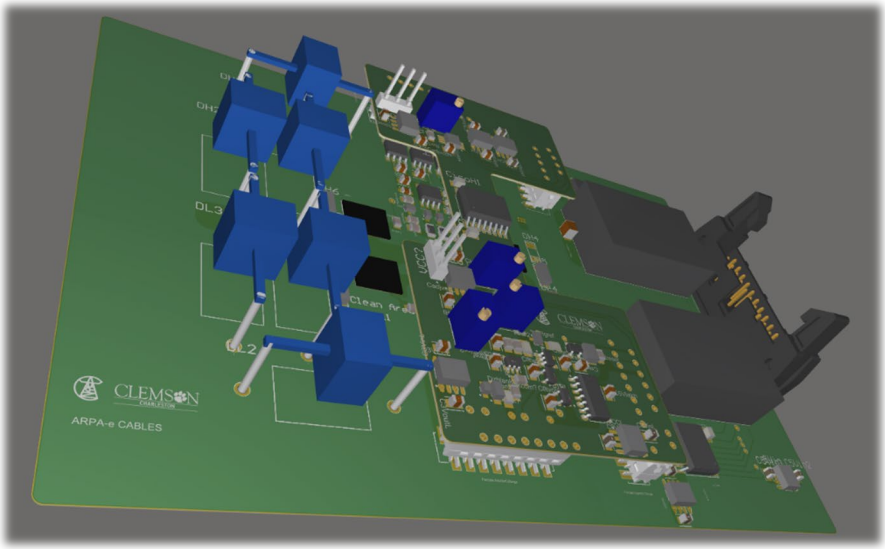


Figure 7. 13: 3D view of the final gate drive design.

Based on the discussion above, the intelligent gate drive for system-friendly DC-SSCB has been designed through Altium Designer. The 3D view of the final intelligent gate drive design is shown in Figure 7. 13. GaN, RC snubber, TVS, and gate drive are on one assembled board. GaN, RC snubber, and TVS are on the bottom board, while the intelligent gate drive is on the bottom and top board.

7.4 Experimental demonstration of the gate drive for DC-SSCB

This section aims at evaluating the proposed intelligent gate drive performance of system-friendly DC-SSCB. As illustrated in Figure 7. 14, A 200V/150A DC-SSCB prototype has been built to demonstrate the effectiveness of the proposed intelligent gate drive circuit for the system-friendly DC-SSCB with current limitation capability. GaN, RC snubber, TVS, and gate drive are on one assembled board. Critical parameters of the proposed system-friendly DC-SSCB prototype are shown in Table 7. 2.

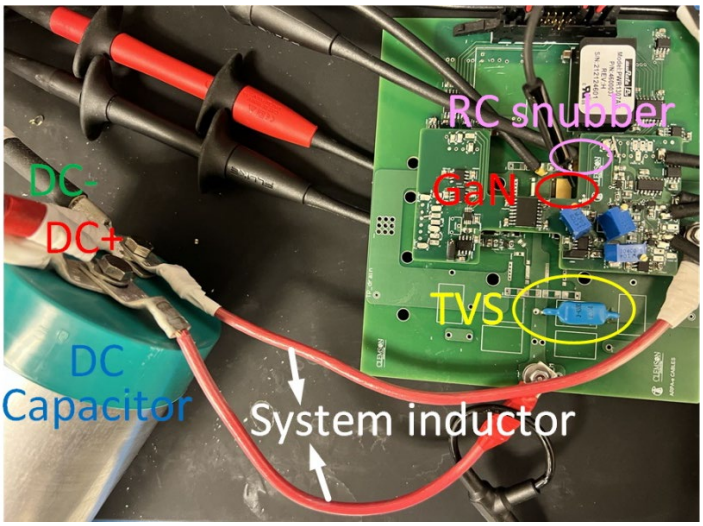


Figure 7. 14: Prototype of the proposed system-friendly DC-SSCB with gate drive.

Parameters	Value
V_{DC}	200V
GaN	GS66516T
TVS	AK3-430
Resistance of RC snubber	0.5Ω
Capacitance of RC snubber	150nF
R_g	15Ω
Turn-on gate voltage	6V
Turn-off gate voltage	-3V

Table 7. 2: Critical parameters of the system-friendly DC-SSCB prototype.

Figure 7. 15 shows the test platform for the proposed intelligent gate drive for system-friendly DC-SSCB. The function generator produces the input PWM signal to the intelligent gate drive. The PWM signal makes GaN keeps the on-state to mimic the short circuit fault. The system inductor is leveraged to emulate the different real system inductances. Different test waveforms are observed through an 8-channel mixed signal oscilloscope.

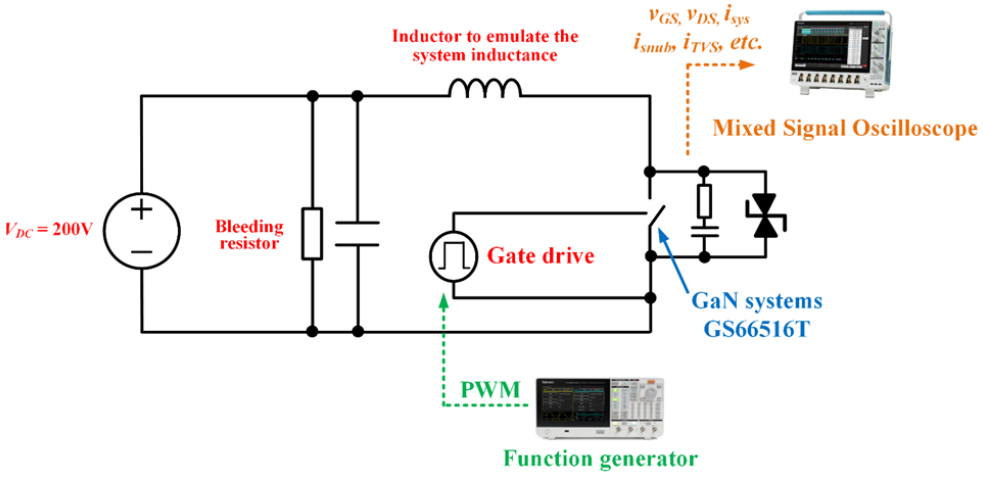


Figure 7. 15: Test platform for the proposed gate drive for system-friendly DC-SSCB.

7.4.1 Verification of the gate drive for DC-SSCB in breaker mode

Based on the platform in Figure 7. 15, several tests have been implemented to verify the proposed intelligent gate drive for system-friendly DC-SSCB. Figure 7. 16 illustrates the waveform of the proposed system-friendly DC-SSCB in breaker mode when L_{sys} = 5.7μH. v_{desat} is the sensing v_{DS} to trigger the protection, and v_{flt} is the fault signal to control DC-SSCB.

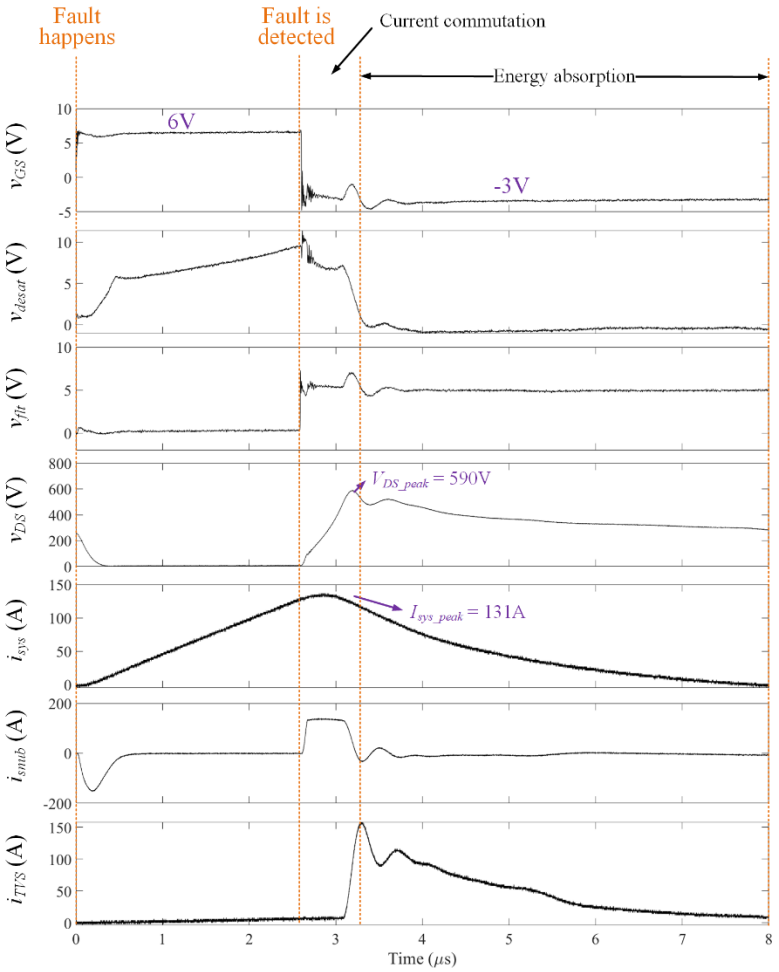


Figure 7. 16: Waveform of breaker mode when L_{sys} = 5.7 μH.

At 0 μs, the function generator sends a high signal to the intelligent gate drive, and GaN is conducted to emulate the short circuit fault. The increasing ratio of i_{sys} is based on the value of L_{sys}. When GaN is turned on, the high dv_{DS}/dt induces the current flowing through the RC snubber from 0 μs to 0.5 μs. Since DC-SSCB is always conducted during normal operation and the fault happens when DC-SSCB is conducted, this will not occur in the real scenario.

When the fault happens, v_{desat} and i_{sys} keep increasing. Since the fault is not detected, v_{GS} = 6V, and GaN keeps on-state. Then, at 2.6 μs, v_{desat} increases to the threshold voltage, triggering the protection. v_{GS} decreases to -3V to turn off DC-SSCB. From 2.6 μs to 3.2 μs, current commutate from GaN to RC snubber and TVS. Peak drain-source voltage V_{DS_peak} is clamped by TVS to 590V, and the peak system current I_{sys_peak} is 131A. Finally, after 3.2 μs, TVS keeps dissipating the extra system energy produced during the interruption process.

Figure 7. 16 has already illustrated the waveform of the proposed system-friendly DC-SSCB in breaker mode when L_{sys} = 5.7μH. The high L_{sys} can help DC-SSCB limit the increasing ratio of the fault current and leave enough response time for DC-SSCB. However, it is highly possible that the short circuit happens close to the DC-SSCB, which makes the value of L_{sys} extremely small. Thus, DC-SSCB should be fast enough to detect the short circuit fault when there is almost no system inductance. In order to verify the proposed intelligent drive when L_{sys} is almost zero, Figure 7. 17 shows the waveform of the proposed system-friendly DC-SSCB in breaker mode when L_{sys} = 0.4 μH. The system inductor is only a 10 cm 14 AWG cable.

At 0 μs, the function generator sends a high signal to the intelligent gate drive, and GaN is conducted to emulate the short circuit fault. Because L_{sys} is only 0.4 μH, i_{sys} increases to about 180A in 400 ns. Then, at 400 ns, v_{desat} increases to the threshold voltage, triggering the protection. v_{GS} decreases to -3V to turn off DC-SSCB. Thus, the response time of the proposed intelligent gate drive can be as fast as 400ns. Then, from 400 ns to 1000 ns, current commutates from GaN to RC snubber. There is no current flowing through TVS. The energy stored in the inductor can be expressed as $1/2\,Li^2$. Because system inductance is almost zero, there is no extra system energy produced during the interruption process need to be dissipated by TVS.

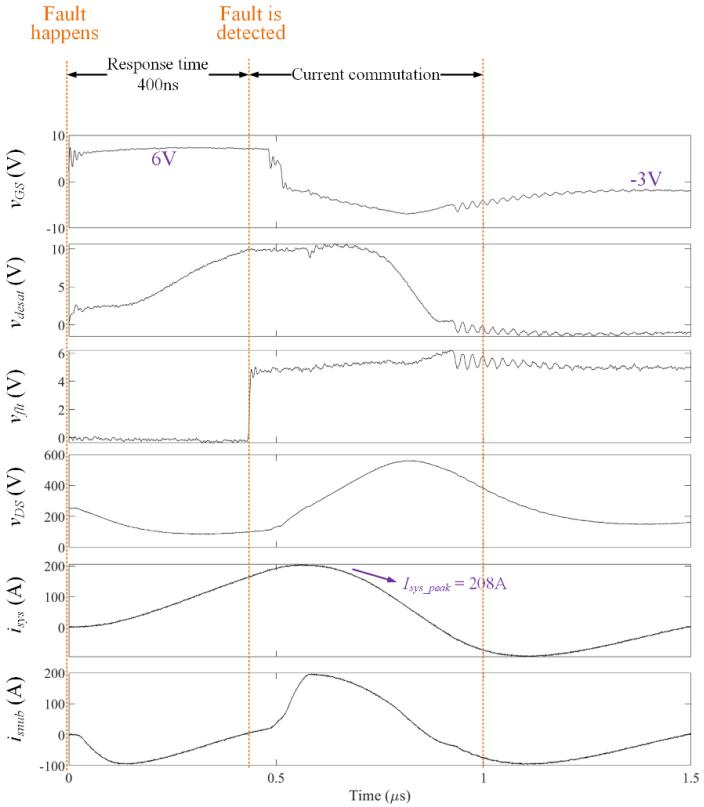


Figure 7. 17: Waveform of breaker mode when L_{sys} = 0.4 μH.

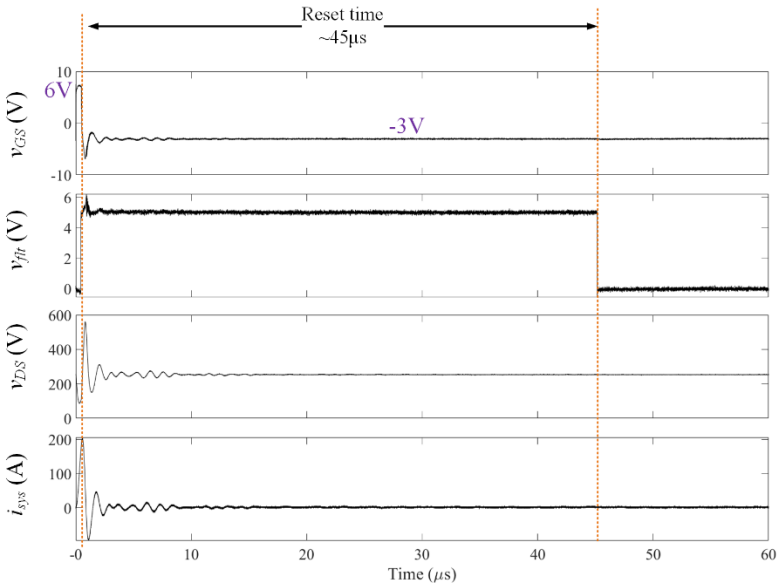


Figure 7. 18: Reset function verification for breaker mode.

The reset function is critical to the DC-SSCB. Because it determines fault clearance and the restart time for the protection system. The reset function-related waveform of the proposed system-friendly DC-SSCB is shown in Figure 7. 18. The fault signal keeps about 45µs, and the fault reset time is determined by the RC constant of the reset function circuit. The input PWM signal cannot control the intelligent gate drive during the reset time. When the fault signal disappears, the input PWM can control the intelligent gate drive again. Once the fault is cleared, DC-SSCB will be conducted; once the fault still exists, DC-SSCB will interrupt the fault current again.

7.4.2 Verification of the gate drive for DC-SSCB in limiter mode

To verify the current limitation function, Figure 7. 19 shows the waveform of the proposed system-friendly DC-SSCB in limiter mode when L_{sys} = 5.7 µH.

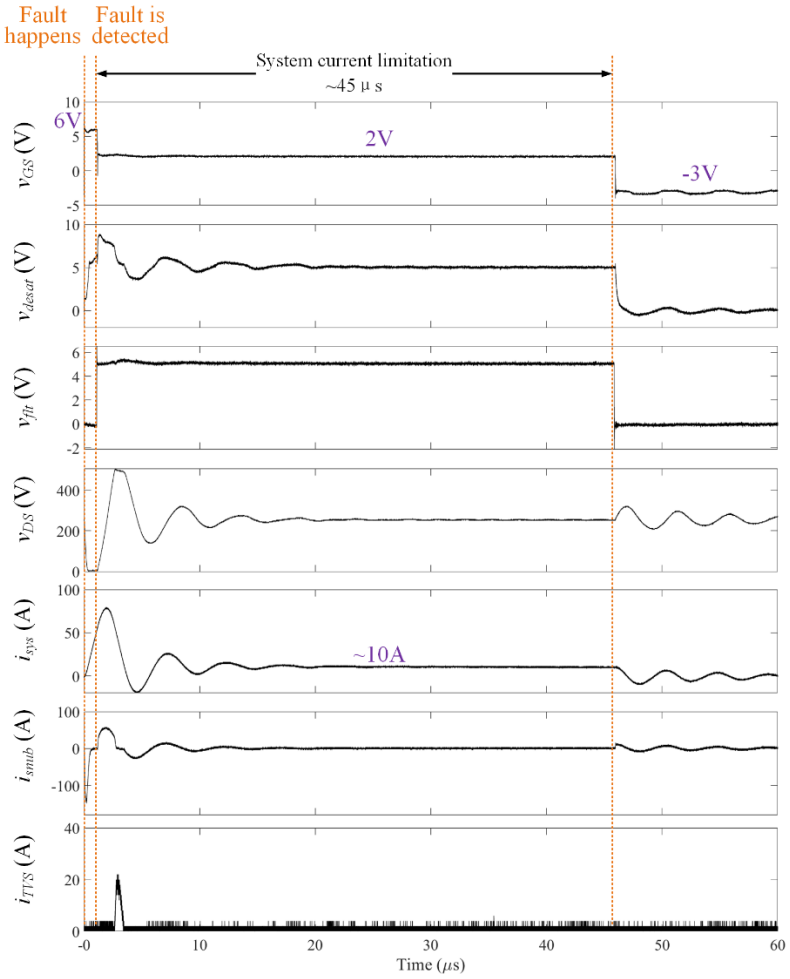


Figure 7. 19: Waveform of limiter mode when L_{sys} = 5.7 μH.

At 0 μs, the function generator sends a high signal to the intelligent gate drive, and GaN is conducted to emulate the short circuit fault. Then, when the fault is detected, v_{GS} is controlled by the intelligent gate drive decreasing to the current limitation gate voltage (2V in this case). Because GaN has arrived in the active region and the current flowing through the GaN is determined by the current limitation gate voltage, which can limit the system fault current. For the case in Figure 7. 19, the current limitation gate voltage is 2V, and i_{DS} is limited to about 10A. Meanwhile, TVS and RC snubber cooperate in dissipating the extra

energy generated when DC-SSCB starts to limit the system current. Following the fault signal, the system's current limitation time is 45μs, which is determined by the RC constant of the reset function circuit. Finally, v_{GS} will decreases to -3V to turn off DC-SSCB when the input PWM signal is low.

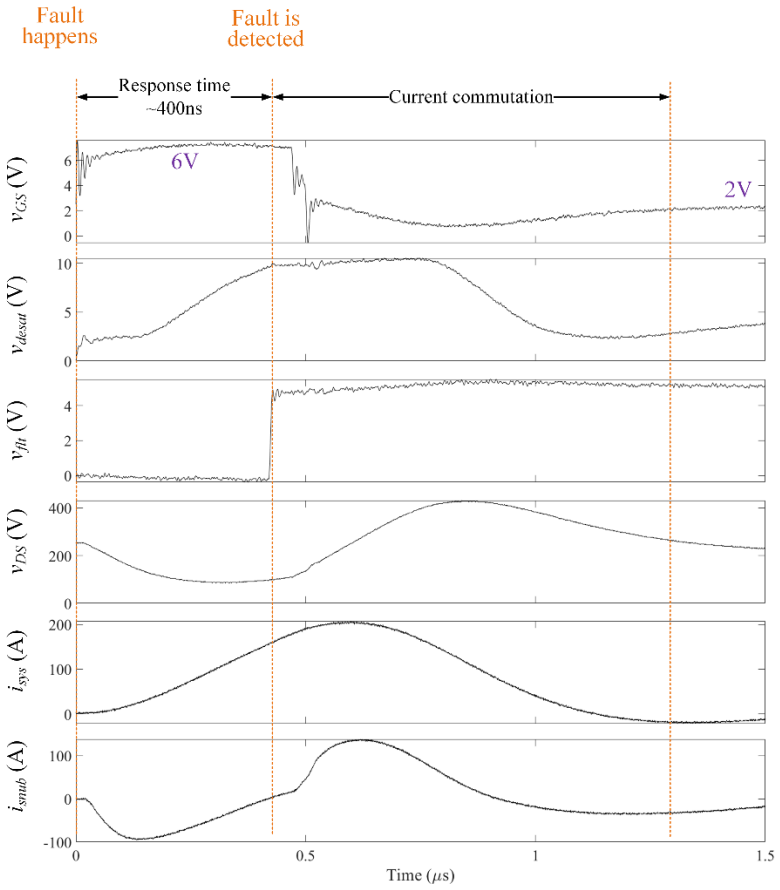


Figure 7. 20: Waveform of limiter mode when L_{sys} = 0.4 μH.

Same with the breaker mode for DC-SSCB, the limiter mode for DC-SSCB also has to reliably detect and limit the system current when the short circuit fault is close to

DC-SSCB. Figure 7. 20 shows the waveform of the proposed system-friendly DC-SSCB in limiter mode when L_{sys} = 0.4 μH in the first 1.5μs.

At 0 μs, the function generator sends a high signal to the intelligent gate drive, and GaN is conducted to emulate the short circuit fault. Because L_{sys} is only 0.4 μH, i_{sys} increases to about 180A in 400 ns. Then, at 400 ns, v_{desat} increases to the threshold voltage, triggering the protection. v_{GS} decreases to 2V to limit the system fault current. Thus, the response time of the proposed intelligent gate drive can be as fast as 400ns in limiter mode. Then, from 400 ns to 1300 ns, current commutates from GaN to RC snubber. Since the system inductance is almost zero, no extra system energy is generated during the current limitation that needs to be dissipated by TVS. Thus, there is no current flowing through TVS.

Figure 7. 21 shows the whole waveform of the proposed system-friendly DC-SSCB in limiter mode when L_{sys} = 0.4 μH. At 0 μs, the function generator sends a high signal to the intelligent gate drive, and GaN is conducted to emulate the short circuit fault. Then, when the fault is detected, v_{GS} is controlled by the intelligent gate drive decreasing to the current limitation gate voltage (2V). Because GaN has arrived in the active region and the current flowing through the GaN is determined by the current limitation gate voltage, which can limit the system fault current. For the case in Figure 6-20, the current limitation gate voltage is 2V, and i_{DS} is limited to about 10A. Meanwhile, RC snubber is leveraged to dissipate the extra energy generated when DC-SSCB starts to limit the system current. The system's current limitation time is 45μs. Finally, v_{GS} will decreases to -3V to turn off DC-SSCB when the input PWM signal is low.

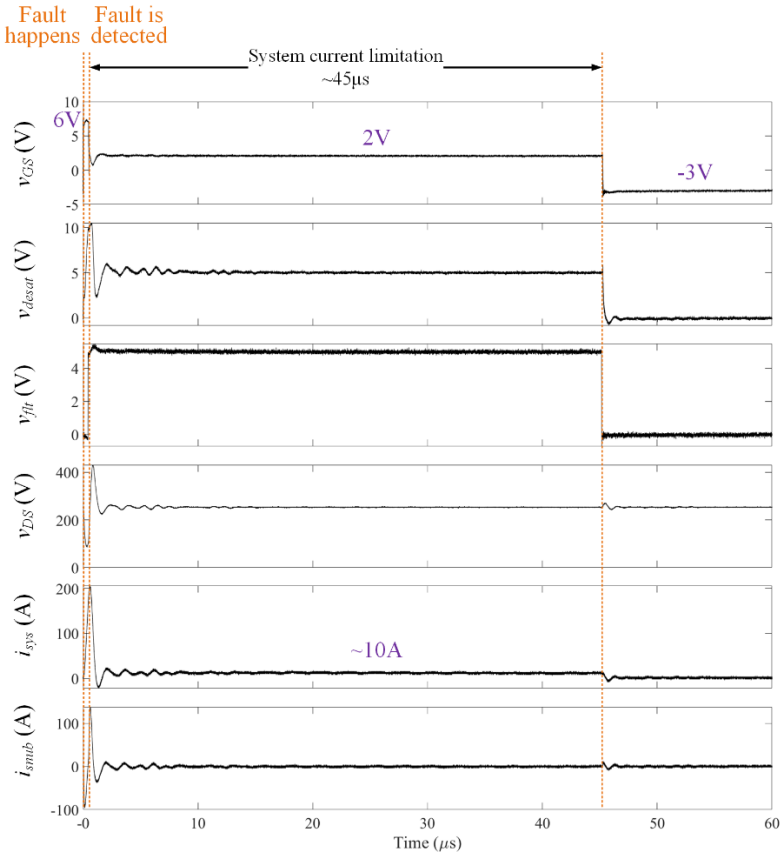


Figure 7. 21: Waveform of limiter mode when L_{sys} = 0.4 µH.

Last but not least, to set the limitation gate voltage for the limiter mode under different scenarios, it is essential to know the relationship between current limitation gate voltage and system limitation current. Several tests have been implemented to measure the system limitation current with different current limitation gate voltages. Figure 7. 22 shows the relationship between current limitation gate voltage and system limitation current.

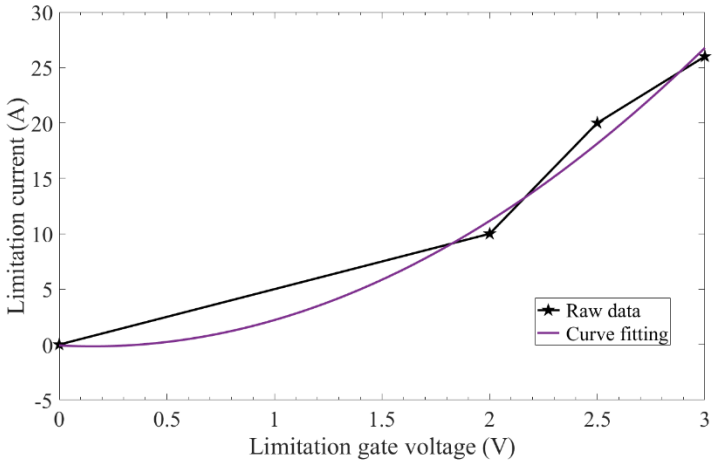


Figure 7. 22: Relationship between current limitation gate voltage and system current.

7.5 Conclusion

This chapter demonstrates the intelligent gate drive circuit design for the SSCB with current limitation capability. The proposed intelligent gate drive enables the SSCB with breaker mode and limiter mode. The limiter mode can help the fault-tolerant-capable system with ride-through capability for healthy parts of the system. For limiter mode, the current limitation is realized by decreasing the gate voltage and the power semiconductor can limit the system fault current based on the *V-I* curve characteristics. The current limitation level can be tuned by the gate voltage. And the limitation time is determined by the reset function. Experimental results show the feasibility and effectiveness of the proposed intelligent gate drive circuit design for the system-friendly SSCB.

CHAPTER EIGHT

8 OVERALL DESIGN FOR SYSTEM-FRIENDLY DC SSCB

8.1 Introduction

A few studies have explored system-friendly functions for DC-SSCB, including soft start-up, fault location detection, fault current limiting, and soft reclosing. As the system protection equipment, it is suitable for DC-SSCB to have the capability of fault location detection. The first DC-SSCB with a short-circuit (SC) fault location detection function is proposed in [32]. The proposed DC-SSCB has a unique PWM current limiting mode. In the PWM current limiting, an algorithm is leveraged to calculate the SC distance using the power line's per-unit inductance value by measuring the response of the voltage pulses injected into the DC power network.

Besides the fault location detection function, the current limiting function is also essential for DC-SSCB. For example, it is preferred to enable the DC-SSCB with an inrush current limitation function during the system start-up. A feasible method is to decrease the gate voltage once the overcurrent event is detected [123, 124]. The fault current can force the power semiconductor to enter the saturation region, and the V-I curve determines the system's current limitation level. To improve the current limiting capability of the semiconductor in the saturation region, a current limiting strategy for SSCB with series-connected switching cells in [53]. However, these studies only focus on the system's current limitation capacity of SSCB. A holistic control strategy lacks to coordinate SSCB's limiter and breaker capabilities to serve as a DC distribution system-friendly player.

It is also essential for DC-SSCB to distinguish the overcurrent and SC for DC-SSCB. Ref [100] proposes a digitally controlled current-time profile-based DC-SSCB for overcurrent protection and SC protection. The proposed current-time profile can help DC-SSCB avoid the fault triggered by the inrush current caused during the start-up of the power electronics intensive system. However, it requires an additional microcontroller to control SSCB, which is complicated and expensive.

To enable reliable operation, the power system with high penetration of power electronics is more demanding for the SSCB-based protection system:

- The fault current cannot exceed SC current rating (SCCR) defined by the system (e.g., 10X) [125].
- Limit the worst scenario fault current below SSCR and trip the SSCB instantaneously (e.g., sub-μs).
- Interrupt the relatively low current fault, instead of instantaneous response, following the i^2t capability of SSCB for better fault type self-awareness and system protection coordination.
- Stand by and bypass a temporary fault with self-recovery capability.

The proposed system-friendly SSCB aims to provide an all-in-one solution with 1) integrated circuitries to serve as fault detectors (not only to detect the fault but also predict the fault current considering absolute fault current and *di/dt*) and actuator (to manage power device's operating status), and 2) coordinated control to seamlessly transition from one mode to another (normal mode, precaution mode, i^2t mode, and interruption mode). For

the fault detector, by introducing the influence of *Ldi/dt*, an improved fault detection circuit is proposed, which considers the value and the increasing ratio of the system's current. Meanwhile, for the actuator, the precaution mode can ensure the system's current cannot be higher than SCCR; i^2t mode guides SSCB's response to the low current fault based on the power device's thermal characteristics [126]; interruption mode is leveraged to interrupt the system's fault current. For the coordinated control, based on the different fault system scenarios, the proposed hardware-based controller can guide four different modes to enable SSCB to take action accordingly.

In summary, the contributions of this section include:

- Compared with traditional desaturation detection, the proposed fault detection circuit, which considers both absolute fault current and *di/dt*, improves the response by up to 10X.
- An SSCB with four operation modes is presented, which can be leveraged to realize system-friendly functions. Moreover, with a real-time gate drive voltage control circuit, SSCB's maximum current limitation level can be tuned programmable.
- By leveraging the improved fault detection circuits and four operation modes, a system-friendly SSCB is developed, which can automatically take different actions according to different fault cases to better serve the modern power system.

8.2 Overview of the system-friendly SSCB

Figure 8. 1 overviews functional blocks of the proposed SSCB, including two fault detectors, three actuators, and a controller.

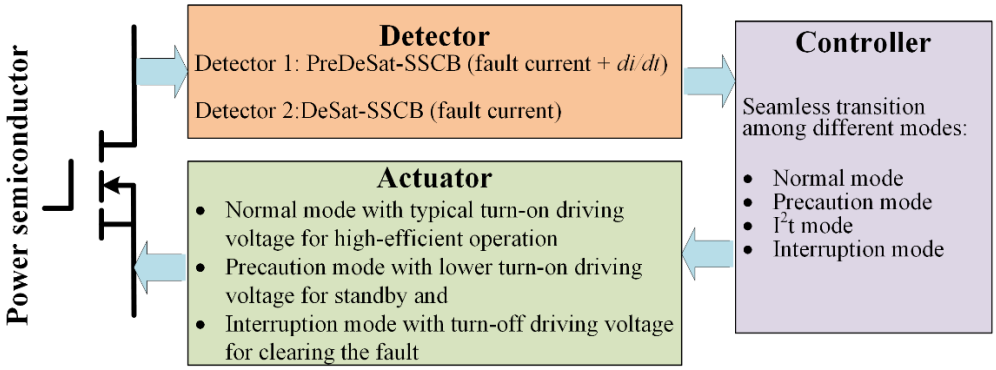


Figure 8. 1: System configuration of the proposed SSCB.

Two fault detectors are devised: PreDeSat-SSCB and DeSat-SSCB.

- PreDeSat-SSCB relies on a *di/dt*-enabled fast fault current indicator, generating the precaution signal to alert SSCB of SC risk.
- DeSat-SSCB depends on a modified, SSCB-suitable desaturation detection, generating the SC tripping signal to interrupt SSCB.

Once the fault is predicted/detected by the detectors, the controller identifies the fault types and decides the actions of the actuator based on the following operation modes.

- ***Normal mode****: Under* normal operation, SSCB's gate voltage stays at turn-on gate voltage ($V_{GS\text{-}on}$) through the actuator to conduct the normal system current with high efficiency.
- ***Precaution mode***: Precaution mode is triggered by the precaution signal from the *di/dt* based fast fault current indicator, and SSCB's gate voltage decreases to precaution voltage (V_{prec}) through the actuator to ensure the system's current (i_{sys}) cannot exceed system's SCCR.

- ***I²t mode***: i^2t mode is triggered by an external i^2t detection unit, and SSCB's gate voltage decreases to turn-off voltage ($V_{GS\text{-}off}$) through the actuator to interrupt the low current fault. The interruption time depends on the power device's intrinsic thermal limit and the current i_{sys}.
- ***Interruption mode***: Interruption mode is triggered by the SC tripping signal from the normal fault detector, and SSCB's gate voltage decreases to $V_{GS\text{-}off}$ through the actuator to interrupt the current at SSCB's SC tripping threshold.

According to the inputs from the detector, the actuator will control the gate voltage to manage the operating status of the power device in SSCB.

- Under the normal mode, gate voltage remains a typical turn-on driving voltage for high-efficient operation.
- Under the precaution mode, gate voltage reduces to the level where the corresponding desaturation current follows the device's V-I curve to the SCCR.
- Under the interruption mode, gate voltage decreases to turn-off driving voltage to clear the fault.

By leveraging the different operation modes, the controller can enable SSCB to take different actions according to different fault cases, as summarized in Table 8. 1. Once *di/dt*-based fast fault current indicator generates the precaution signal, SSCB enters precaution mode to ensure the maximum i_{sys} cannot exceed the system's SCCR and standby. Then, based on different fault cases, SSCB is controlled to enter different operation modes, as illustrated in Figure 8. 2.

Fault scenarios	Actions
Low impedance fault *(System's fault current approaches SCCR and hits DeSat-SSCB's tripping threshold)*	***Step 1***: Normal mode → Precaution mode ***Step 2***: When i_{sys} hits SSCB tripping threshold, SSCB enters interruption mode to interrupt the fault current.
High impedance fault *(System's fault current lower than SSCR)*	***Step 1***: Normal mode → Precaution mode ***Step 2***: Based on the power device's thermal performance, SSCB is interrupted by the i^2t signal from the external control unit.
Short-time overcurrent *(System's start-up, fault fast recovery)*	***Step 1***: Normal mode → Precaution mode ***Step 2***: Back from precaution mode to normal mode, once the i_{sys} is back to normal.

Table 8. 1: SSCB's actions in different fault cases.

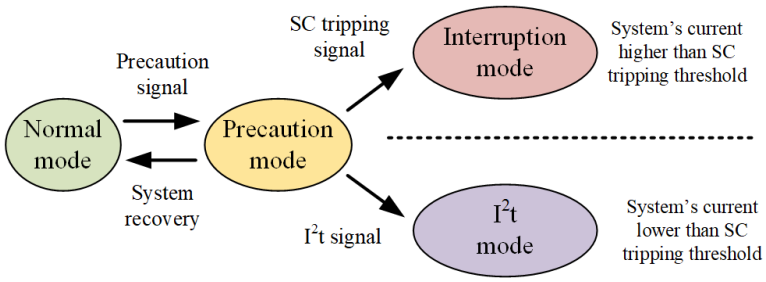


Figure 8. 2：Operation modes transformation for the proposed SSCB.

8.3 Fault detector

A fast and reliable fault detection method is significant to SSCB. Current sensors and desaturation detection (DeSat) [127] are widely leveraged to detect the overcurrent event for SSCB. Because of DeSat's fast response, simplicity, flexibility, and low cost, some studies select desaturation detection as the fault detector. DeSat also has been widely applied to the gate drive design of the PWM-based converter to protect the power semiconductors [128]. However, to better serve SSCB, a modified, SSCB-suitable DeSat detection circuit is preferred.

8.3.1 Desaturation detection for SSCB

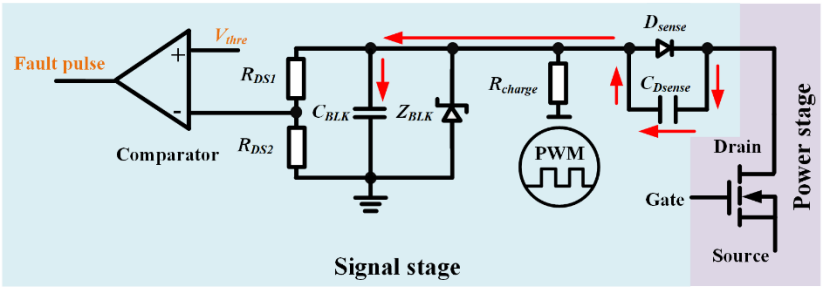


Figure 8. 3: Desaturation detection for PWM-based converter.

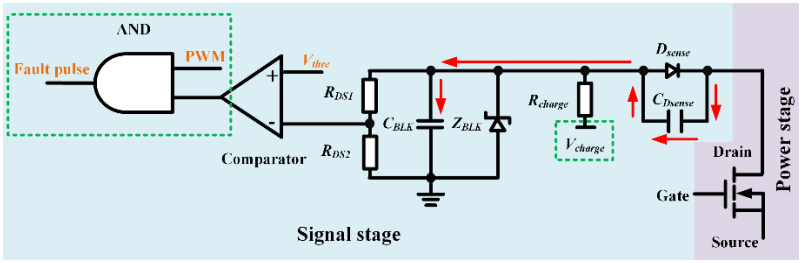


Figure 8. 4: Desaturation detection for SSCB.

Figure 8. 3 shows the schematic of desaturation detection for a PWM-based converter (DeSat-PWM). It mainly comprises drain-source voltage v_{DS} sensing diode D_{sense}, v_{DS} related resistor divider R_{DS1} and R_{DS2}, charing resister R_{charge}, blanking capacitor C_{BLK}, voltage comparator, comparator protection diode Z_{BLK}.

One of the most critical design considerations for desaturation detection is the selection of the D_{sense}. Besides the basic requirement that the breakdown voltage of D_{sense} should be higher than the maximum v_{DS} of the power device, the parasitic capacitance of the v_{DS} should be as small as possible. As shown in Figure 8. 3, the high dv_{DS}/dt can induce a charging current for C_{BLK} through C_{Dsease}, likely triggering the protection falsely.

The modified schematic of desaturation detection for SSCB (DeSat-SSCB) is displayed in Figure 8. 4. Instead of $V_{GS\text{-}on}$, a fixed voltage V_{charge} (e.g., 15V) charges C_{BLK}. An additional "AND" gate connecting with the output of the comparator and PWM is required to avoid false overcurrent detection when the power device is off. The modified desaturation detection for SSCB mainly provides two benefits:

- For DeSat-PWM, the voltage across the blanking capacitor v_{BLK} cannot exceed $V_{GS\text{-}on}$. For DeSat-SSCB, with a separate and more flexible charging source V_{charge}, there will be more margin for DeSat-SSCB to set the protection threshold, which is especially beneficial for GaN transistors with low $V_{GS\text{-}on}$ (e.g., 6V).

- For the discrete components-based DeSat [129], once the fault event is detected, the gate drive IC (e.g., IXDD609) will be disabled, causing a high impedance at the gate drive IC output. Hence, for DeSat-PWM, the charging source of R_{charge}, which is determined by the gate drive output, becomes floated without steady potential. However, for DeSat-SSCB, with the fixed charging source for R_{charge}, its operation state is regardless of the gate drive IC.

In the proposed SSCB, the modified DeSat-SSCB is leveraged to detect if i_{sys} reaches SSCB's tripping threshold.

8.3.2 *Fast pre-desaturation detection for SSCB*

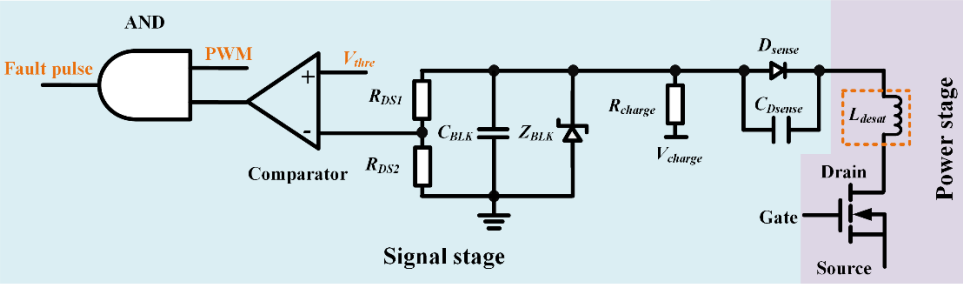


Figure 8. 5: Fast desaturation detection for SSCB.

It is "ideal" to predict the fault event, allowing SSCB to be precautious for the modes' transition under different fault cases. With this, based on the DeSat-SSCB, a fast pre-desaturation detection for SSCB (PreDeSat-SSCB) is proposed in Figure 8. 5. Introducing an extra inductance L_{desat} in the power loop (e.g., power loop parasitics), the sensing voltage is also contributed by L_{desat}×di/dt. Because severe SC fault is usually associated with high di/dt, the proposed PreDeSat-SSCB is more sensitive to the SC fault not only due to the absolute fault current value but also its di/dt trend. It is noted that the proposed PreDeSat-SSCB cannot be leveraged to the power converter, or it may trigger the protection during the switching transition under its normal PWM operation.

With the L_{desat}, the detection voltage for PreDeSat-SSCB can be rewritten as

$$v_{detect} = v_{DS} + L_{desat}\frac{di_D}{dt} \tag{8. 1}$$

where i_D is the current flowing through the power device's drain-source terminal.

Figure 8. 6 shows the test waveform of detection voltage with different L_{desat} (e.g., 0 nH, 8 nH, and 15 nH) under the di_D/dt of 300 A/μs. It can be observed that the PreDeSat-

SSCB can detect the influence of *di/dt*. Figure 8. 7 illustrates the relationship among L_{desat}, *di/dt*, and the time of the detection voltage (using 10 V as an example threshold). The relationship shows that the larger the L_{desat} and the faster *di/dt*, the shorter the detection response time.

In the proposed SSCB, the PreDeSat-SSCB is leveraged to detect whether SSCB is under the SC risk. It generates the fault signal once the system with a relatively high current and *di/dt*, which can help SSCB "predict" the fault and be alerted. Once the protection signal associated with the PreDeSat-SSCB is tripped, SSCB enters the precaution mode.

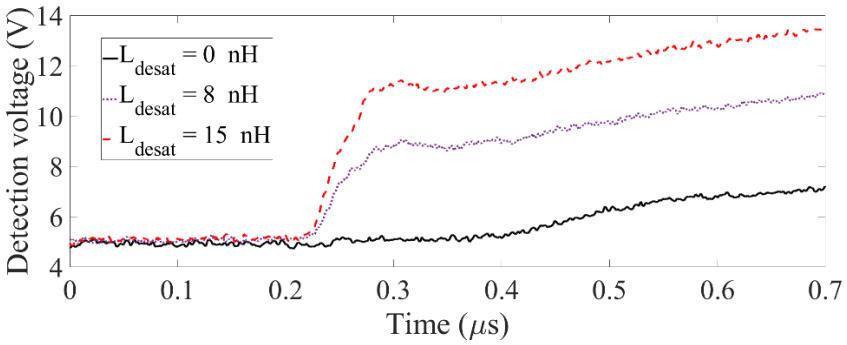


Figure 8. 6: Waveform of detection voltage under different L_{desat}

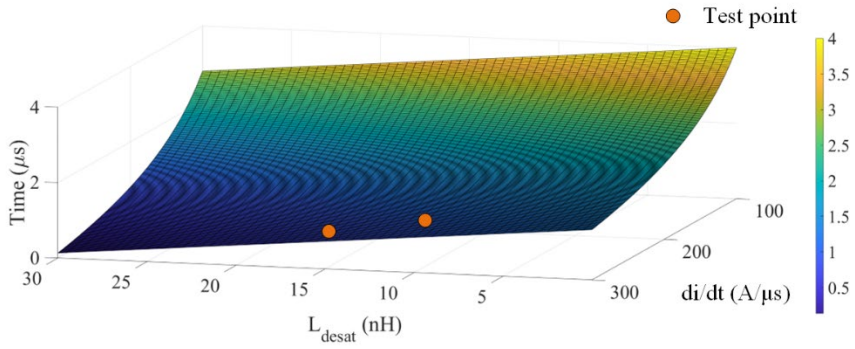


Figure 8. 7: Relationship among L_{desat}, di/dt, and response time.

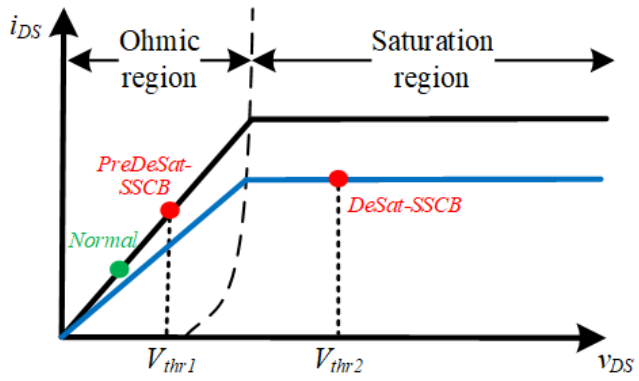


Figure 8. 8: Detection point for PreDeSat-SSCB and DeSat-SSCB.

Figure 8. 8 demonstrates the protection threshold settings associated with PreDeSat-SSCB and DeSat-SSCB, respectively. To allow the PreDeSat-SSCB to identify the potential SC fault promptly, its threshold voltage V_{thr1} is relatively small where the corresponding device current is much higher than the normal operating current but lower than the saturation current. For DeSat-SSCB, a relatively high threshold voltage V_{th2} is selected to ensure SSCB's interruption when the device is fully saturated.

8.3.3 I^2t detection

By leveraging the thermal performance of the SSCB's power device, the external i^2t detection unit pre-defines an i^2t curve for SSCB. Once SSCB standing time for a low fault current achieves the i^2t preset time, an i^2t signal will be sent to SSCB to interrupt SSCB.

8.4 Actuator

As mentioned in Section II, the proposed SSCB has four operation modes: normal mode, precaution mode, i^2t mode, and interruption mode. According to different operation modes, SSCB's actuator circuitries in Figure 8. 9 control gate voltage differently to manage the power device characteristics of SSCB.

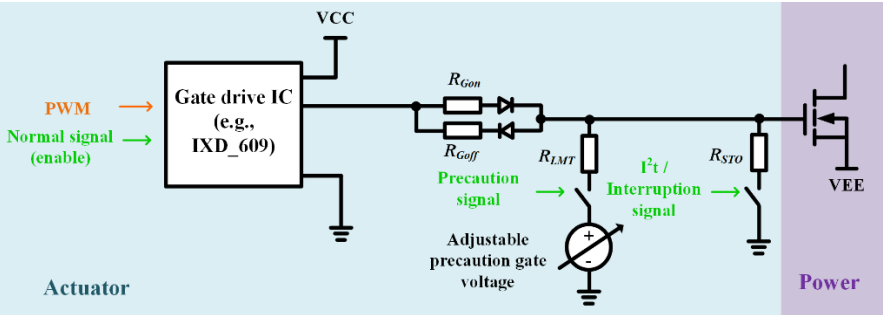


Figure 8. 9: Proposed actuator and its circuit implementation.

8.4.1 Normal mode

When there is no fault, SSCB keeps at normal mode. The normal mode signal controls the enable pin of the gate drive IC. Once the normal mode signal is effective, the gate drive IC will be enabled, and the power device's gate voltage under the control of the PWM signal. Once the normal mode signal is ineffective, the gate drive IC will be disabled as a high impedance, and the gate voltage will be dominated by the other operation mode.

8.4.2 Precaution mode

Once the potential SC fault is detected by the PreDeSat-SSCB-based sensitive detector, SSCB enters precaution mode. Precaution mode leverages the V-I curve characteristic to avoid i_{sys} being higher than SCCR. As shown in Figure 8. 10, once SSCB enters precaution mode, the power device's gate voltage decrease from $V_{GS\text{-}on}$ to V_{prec}. If the SC fault current approaches SCCR, the power device would be forced to enter the saturation region, and the i_{sys} is limited to the saturation current pre-defined by lower gate voltage V_{prec}. In other words, the V_{prec} should be selected such that the corresponding saturation current is lower than SSCR. Meanwhile, because the saturation current is a

function of the gate voltage, by adjusting V_{prec}, the current limitation level can also be conveniently adjusted to satisfy the system's SSCR requirement. Programmable V_{prec} can be achieved by the circuit in Figure 7. 9. It consists of one digital potentiometer (DPM) and a low dropout voltage regulator (LDO) with adjustable output.

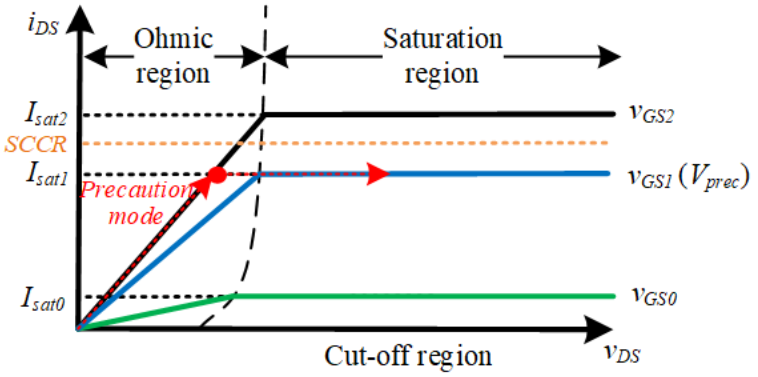


Figure 8. 10: Typical V-I curve for a power device.

8.4.3 I^2t mode

Once SSCB receives an i^2t detection enable signal from the external control unit, SSCB enters i^2t mode. During the operation of SSCB, the external i^2t detection and protection unit monitors i_{sys} and calculates the i^2t value. Based on the pre-defined device's i^2t capability curve, once the sensed i^2t exceeds the device's capability, an i^2t fault is tripped and its protection signal is transmitted to SSCB. Once entering i^2t mode, SSCB's gate voltage can decrease from V_{prec} to $V_{GS\text{-}off}$ to avoid damage to the power device by a thermal issue.

8.4.4 Interruption mode

When i_{sys} hits SSCB tripping threshold, the proposed DeSat-SSCB generates the interruption signal and SSCB enters the interruption mode instantaneously. Once entering

interruption mode, SSCB's gate voltage can decrease from V_{prec} to $V_{GS\text{-}off}$ to turn off power devices. Table 8. 2 summarizes the details of different operation modes.

Mode	Detector			Actuator		
	DeSat	PreDeSat	Ext. i^2t	$V_{GS\text{-}on}$	V_{prec}	$V_{GS\text{-}off}$
Normal	×	×	×	○	×	×
Precaution	×	○	×	×	○	×
I^2t	×	×	○	×	×	○
Interruption	○	×	×	×	×	○

○: with ×: without

Table 8. 2: Detail of different operation modes.

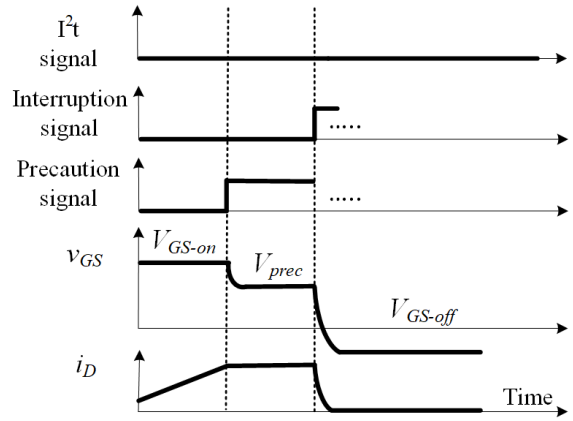
8.5 Coordinated control of system-friendly SSCB

As mentioned in Table 8. 1, to help SSCB takes various actions under different fault cases, a coordinated controller is developed. As a reminder, the threshold V_{thr2} of the DeSat-SSCB corresponds to the SSCB's tripping current threshold, and V_{prec} corresponds to the saturation current value lower than SCCR.

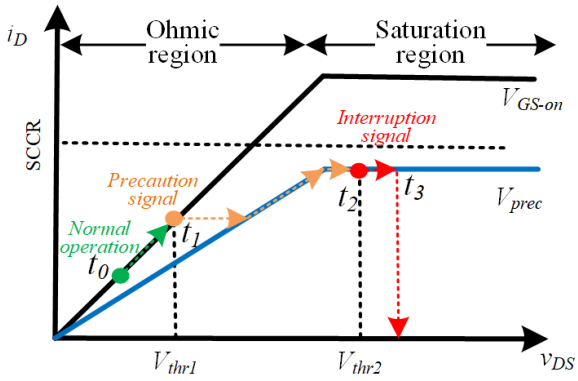
8.5.1 Low impedance fault

Figure 8. 11 illustrates the control logic and device V-I trajectory under the low impedance fault. The proposed PreDeSat-SSCB and DeSat-SSCB generate the precaution signal and interruption signal, respectively. PreDeSat-SSCB is faster to detect the SC event. Once PreDeSat-SSCB generates an effective precaution signal at t_1, v_{GS} will drop from $V_{GS\text{-}on}$ to V_{prec} to ensure the i_{sys} is lower than SCCR. Then at t_2, with the system fault current approaches SCCR, DeSat-SSCB is triggered to generate an effective interruption signal, and SSCB transitions from the precaution mode to the interruption mode. With hundreds of ns blanking time, SSCB interrupts the system fault current at t_3. Due to the sensitive

PreDeSat-SSCB detection, SSCB transitions to the precaution mode promptly, allowing v_{GS} decreases to V_{prec} in time to limit the system fault current below SCCR. Based on the analysis in Section III, V_{prec} can be tuned to change the fault current limitation level according to the system requirements.



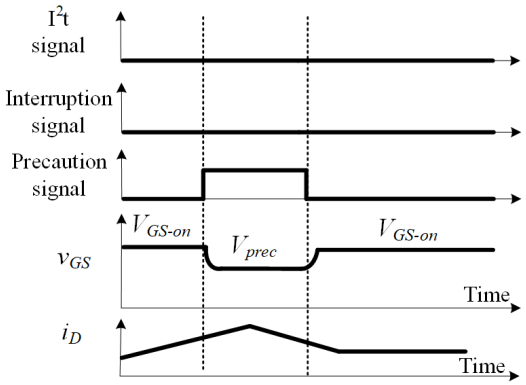
(a) Control logic



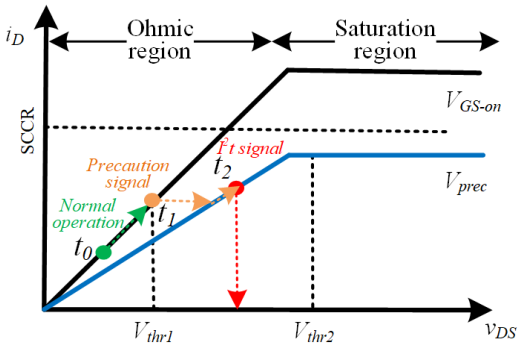
(b) Operating trajectory

Figure 8. 11: Operation principle under the low impedance fault.

8.5.2 *High impedance fault*



(a) Control logic



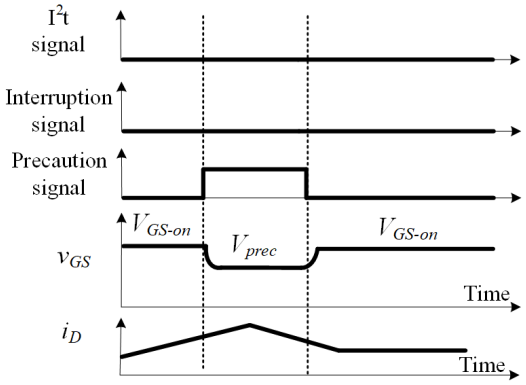
(b) Operating trajectory

Figure 8. 12: Operation principle under the high impedance fault.

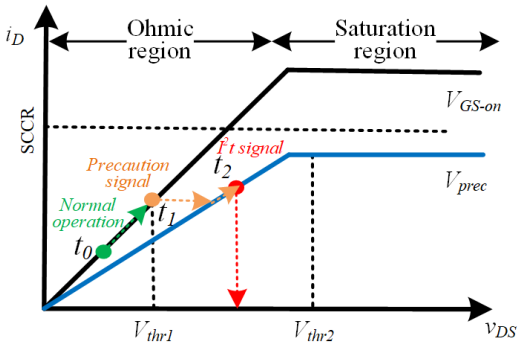
Figure 8. 12 illustrates the control logic and device V-I trajectory under the high impedance fault. Similar to low impedance fault, once PreDeSat-SSCB generates an effective precaution signal at t_1, v_{GS} drops from $V_{GS\text{-}on}$ to V_{prec}. Because of the high impedance fault, it is assumed that the system fault current is lower than SCCR, therefore, DeSat-SSCB fault detection will not be enabled. In this case, the external i^2t control unit kicks in to let SSCB enter i^2t mode from precaution mode and interrupts the fault at t_2. This

operation scenario allows SSCB to stand by with a relatively low fault current, offering time for system-level protection coordination, which is particularly beneficial to the current sensitive power distribution system with high penetration of power electronics.

8.5.3 Fault fast recovery case



(a) Control logic



(b) Operating trajectory

Figure 8. 13: Operation principle under the fast fault recovery.

The control logic and SSCB trajectory under the fault fast recovery case are shown in Figure 8. 12. Assume PreDeSat-SSCB generates an effective precaution signal at t_1 due

to a fault event, lowering v_{GS} to be V_{prec}. However, the fault is recovered between t_1 and t_2 (either the fault disappears automatically, or the fault is cleared by the local SSCB), and the system's current is back to the normal value at t_2. Because the fault time is shorter enough to not trigger the i^2t mode, the precaution signal would disappear and v_{GS} is back to normal $V_{GS\text{-}on}$. This operation scenario enables SSCB with the fault ride-through capability. The short-time overcurrent fault or event cannot influence the operation of SSCB.

8.6 System-friendly SSCB implementation and verification

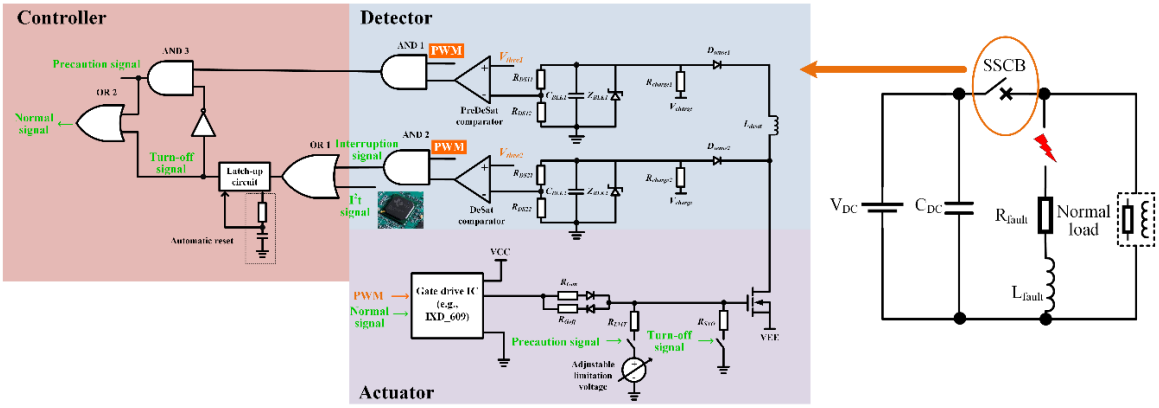


Figure 8. 14: Schematic of the proposed SSCB.

Integration with Sections III-V, Figure 8. 14 shows the schematic of the proposed SSCB.

8.6.1 Implementation

8.6.1.1 Detector

The detection circuit is composed of DeSat-SSCB and PreDeSat-SSCB. The sensitive PreDeSat-SSCB is leveraged to detect the potential SC fault. Meanwhile, the DeSat-SSCB is leveraged to detect SSCB's SC tripping threshold current. To make the

precaution mode more sensitive to potential SC fault, the threshold voltage of PreDeSat-SSCB V_{thre1} should be relatively small. Meanwhile, the threshold voltage of DeSat-SSCB V_{thre2} needs to fit with SSCB's SC tripping threshold current.

8.6.1.2 Controller

The controller comprises several logic gate ICs to generate SSCB's control signal. The precaution pulse is generated by PreDeSat-SSCB, while DeSat-SSCB generates the interruption pulse. The i^2t signal is from the external control unit. The generated precaution pulse is sent to an AND gate (AND 3). Meanwhile, the generated interruption pulse is sent to an OR gate (OR 1) with the external i^2t signal. The output of OR 1 will be sent to a latch-up circuit to generate the turn-off signal to interrupt the system's current. The precaution signal will AND with the inversed turn-off signal generating the precaution mode control signal, to avoid the conflict between limitation and turn-off signal. Finally, the precaution mode control signal and turn-off signal will be OR together to generate the enable signal for the gate drive IC (normal mode control signal). The enable signal is leveraged to control the gate drive IC for the power device.

8.6.1.3 Actuator

The actuator circuit mainly comprises the gate drive IC, precaution voltage control branch, and turn-off control branch. The gate drive IC is leveraged to control the power device under normal conditions. Once SSCB enters precaution mode, the gate drive IC will be disabled. The precaution signal can conduct the precaution voltage control branch, and v_{GS} can drop to V_{prec} to ensure i_{sys} cannot be higher than SCCR. Meanwhile, the turn-off

signal generated from the interruption signal and i^2t signal can conduct the turn-off control branch, and v_{GS} can drop to turn-off voltage to interrupt the system's fault current.

8.6.2 Experimental verification

A GaN-based 200V/10A SSCB is prototyped to demonstrate the feasibility and effectiveness of the proposed system-friendly SSCB, as shown in Figure 8. 15. TABLE III summarizes the key parameters. The test platform is mainly composed of the DC power supply V_{DC}, fault trigger breaker, system fault impedance Z_{fault}, and the proposed SSCB. A separate fault trigger breaker is introduced to create the SC fault events. Once the fault trigger breaker is conducted, it can be assumed that the SC occurs. Z_{fault} can emulate the fault system impedance once the SC occurs. The response of the proposed SSCB to different SC fault cases could be tested by adjusting Z_{fault}.

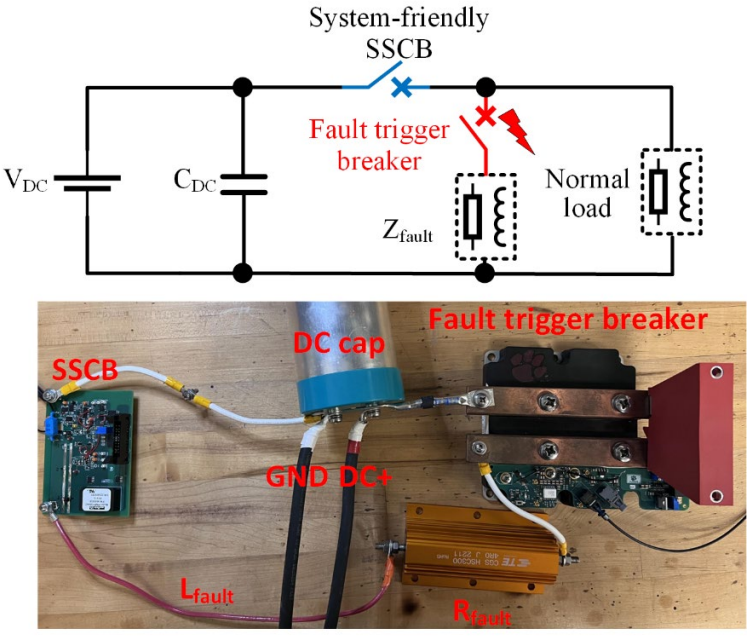


Figure 8. 15: Test platform for the proposed SSCB.

Parameters	Value
Power device	GS66516T
Snubber	150nF, 0.5Ω
TVS	AK3-430
SCCR	150A
DC bus voltage	200V
Turn-on voltage	6V
Turn-off voltage	-3V
Precaution voltage	4V
Gate Drive IC	IXDD609

Table 8. 3: Parameters of the proposed SSCB.

8.6.2.1 Low impedance fault

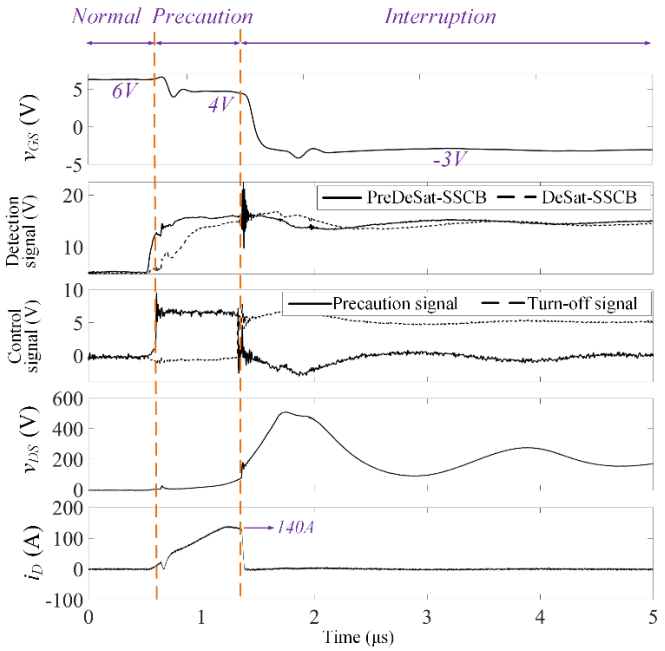


Figure 8. 16: Test waveform under the low impedance fault (L_{fault}=0.7μH).

Figure 8. 16 illustrates the waveform of the SSCB when the fault system inductance L_{fault} is 0.7 μH, which is primarily contributed by interconnecting wire instead of a dedicated inductor. The SC fault happens at 0 μs, and v_{GS} is 6 V. Then, at approximately 0.5 μs, the PreDeSat-SSCB detects the potential SC, SSCB enters precaution mode, and

v_{GS} drops to 4 V, which corresponds to the predefined SCCR in Table 8. 3. DeSat-SSCB detects the overcurrent at about 1.4 µs, SSCB enters interruption mode, and v_{GS} drops from 4 V to -3V to interrupt the system's current. Based on the waveform, it can be found that the proposed SSCB can interrupt a low impedance fault in 1 µs; meanwhile, the current flowing through the power device i_D is limited by the precaution voltage to 140 A stably.

8.6.2.2 High impedance fault

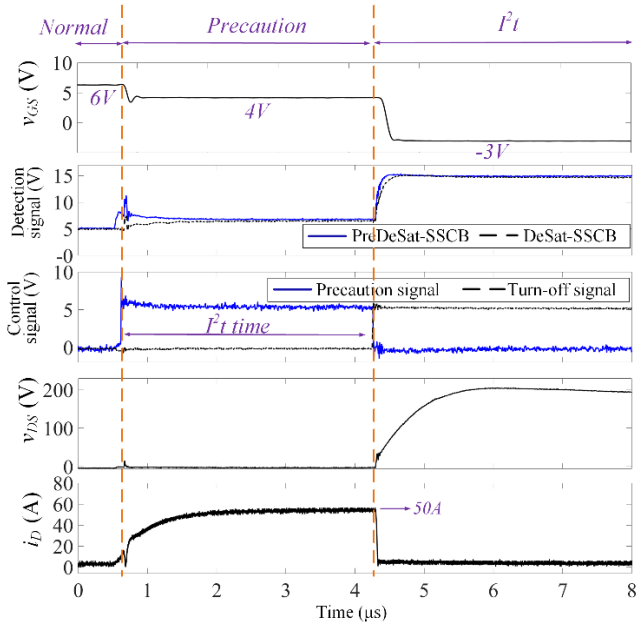


Figure 8. 17: Test waveform under the low impedance fault (L_{fault}=2 µH, R_{fault}=4 Ω).

Figure 8. 17 illustrates the waveform of the SSCB with 2 µH system inductance L_{fault} and 4 Ω system resistance R_{fault}. The system's maximum fault current is limited to 50A by R_{fault}. The SC fault happens at 0 µs, and v_{GS} is 6 V. At 0.8 µs, the PreDeSat-SSCB detects the potential SC, SSCB enters precaution mode, and v_{GS} drops to 4 V. Approximately 4 µs later, SSCB receives an emulated i^2t signal for the sake of test and

enters i^2t mode. I^2t signal generates a turn-off signal and v_{GS} drops from 4V to -3V to interrupt the system's fault current. Because the v_{DS} does not achieve the threshold voltage for DeSat-SSCB, DeSat-SSCB is not triggered in this case. The test results agree with the analysis above.

8.6.2.3 Fault fast recovery case

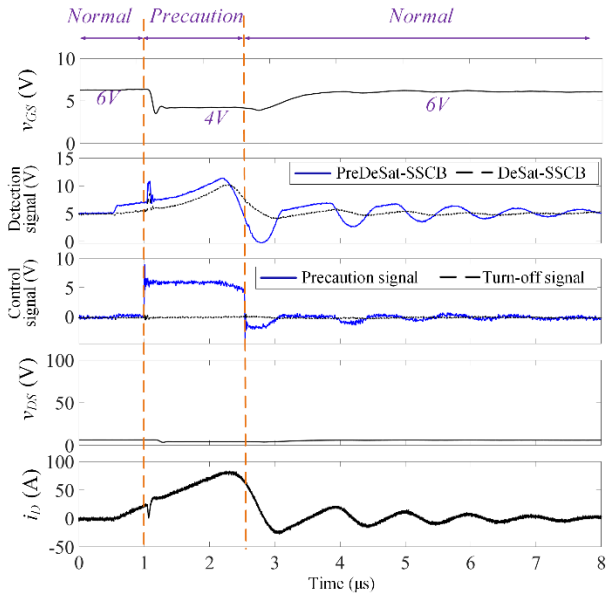


Figure 8. 18: Test waveform under the fault fast recovery case.

Figure 8. 18 illustrates the waveform of the SSCB under a fault fast recovery case. The SC fault happens at 0 μs with 6 V v_{GS}. Then, at 1μs, the PreDeSat-SSCB detects the potential SC, and SSCB enters precaution mode with 4 V v_{GS}. Then, the fault recovers at 2.2 μs. With the fault recovery, the system's current decreases. Accordingly, PreDeSat-SSCB detected v_{DS} decreases and becomes lower than PreDeSat-SSCB's threshold voltage. Then, the precaution signal disappears, and v_{GS} increases from 4V to 6V to resume the system's normal operation. During this process, because the fault time is shorter than the

i^2t time and the system's fault current is not high enough, i^2t and interruption modes are not triggered.

8.7 Conclusion

A system-friendly SSCB is developed and demonstrated. The key takeaways and findings are summarized below.

1) Two fault current detection circuits, DeSat-SSCB and PreDesat-SSCB, are suitable for the SSCB application. Particularly, the PreDeSat-SSCB, considering both the fault current absolute value and *di/dt*, results in the increased fault detection response speedup by 10 X as compared to conventional desaturation detection based on the test.

2) Four operation modes, including normal mode, precaution mode, i^2t mode, and interruption mode, are offered: i) normal mode with the normal driving voltage makes the efficient operation of the SSCB, ii) precaution mode with reduced driving voltage ensures the system's fault current lower than SCCR; iii) i^2t mode helps SSCB interrupt low fault current considering power devices' intrinsic thermal limit; iv) interruption mode allows SSCB's interruption at SSCR within 200 ns to 1 μs.

3) Coordinated control enables SSCB to take corresponding actions to various fault cases: i) once the SC and/or high *di/dt* event is detected through PreDeSat-SSCB, the proposed SSCB lowers the power device gate voltage to ensure the system's maximum fault current below SCCR; ii) under the low-impedance fault when the fault current approaches SCCR, the proposed SSCB based on DeSat-SSCB triggering signal can interrupt the fault within 200 ns to 1 μs; iii) under the high-impedance fault when the fault

current does not exceed SCCR, the proposed SSCB can interrupt the fault based on an external i^2t detection and protection unit; iv) finally, the SSCB is capable of fast fault recovery, i.e., when the fault is cleared by a local SSCB and the protection signal by PreDesat-SSCB disappears, the SSCB is able to be back under the normal operation

CHAPTER NINE

9 CONCLUSION AND FUTURE WORK

9.1 Conclusion

Based on the literature review, it is observed that no design and modeling effort for the ultra-dense DC-SSCB exists for aviation applications, which includes no lightweight current limitation technique to eliminate the bulky and heavy current limitation inductor. Moreover, most of the papers focus on the interruption capability of DC-SSSB with limited emphasis on the system-friendly functions. For the DC distribution system, it is important for DC-SSCB to have fault self-awareness, fault ride-through capability, tunable response time, tunable fault trigger current, etc.

Firstly, this dissertation proposes a design of a 2 kV/1 kA high-power density SSCB enabled by a gate driver without the current limiting inductor for aviation applications. The proposed SSCB can limit the maximum peak fault current level through power module *V-I* curve characteristics with tunable driving voltage, thus achieving a power density over 100kW/kg. The peak fault current level can also be flexibly tuned by driving voltage. The proposed gate voltage-based current limitation strategy can limit the system peak current in a range of 2000 A - 3000 A depending on gate voltage under different operating temperatures.

Secondly, an analytical DC-SSCB model is also proposed. It offers fundamentals for the design optimization of DC-SSCB with the holistic consideration of power semiconductors, gate drive, MOV, and associated parasitics. Based on the experimental verification, it shows the proposed DC-SSCB model can accurately estimate the peak

clamping voltage with no more than 1.3% mismatch as compared to the test result, while the maximum mismatch of the clamping current is 1.1%. Moreover, the sensitivity analysis indicates that L_{MOV} and L_E are the most crucial impact factors, while C_{MOV} and L_C are the parameters with the least influence on V_{CE_peak}. This offers the fundamentals to further simplify the derived models with order reduction of the state equations; in the meantime, it guides the co-design optimization of the gate drive, MOV, and parasitic management for high-density SSCB.

Thirdly, the mechanism causing oscillation of v_{GE} and v_{CE} when the lightweight DC-SSCB without a current limiting inductor enters the active region is analyzed. Three suppression approaches are proposed by stabilizing the gate-emitter voltage. Analysis results show that the difference in L_E, L_C, R_G, V_{TH}, C_{GE}, L_G, C_{MOV}, and L_{MOV} can aggravate the oscillation. The mismatch between L_E has the most influence on the oscillation. Then, experiment results illustrate that clamping v_{GE} by paralleling a Zener diode between the gate and emitter terminals or connecting positive driving voltage and gate terminal through a clamping diode can effectively suppress the oscillation on v_{CE} by about 50%.

Meanwhile, the influence of the bus bar's connection to the IGBT module-based SSCB when the dead short happens (system impedance is close to zero) is also analyzed. With the help of the Q3D extractor, when the dead short happens, it is proven that the gate loop can couple with the electromagnetic field generated by the power loop. The induced voltage can influence the gate voltage and saturation current. To suppress the influence of the electromagnetic field of the power loop on the gate loop, a vertical bus bar mechanical connection structure is proposed. Based on the result of the Q3D extractor, the vertical bus

bar-based SSCB results in a more evenly distributed coupling inductance L_E, which means that the power loop has less impact on the gate loop. Accordingly, the saturation current (maximum limiting current) for SSCB could be no longer influenced by the bus bar connection.

Then, a gate drive circuit design for the system-friendly SSCB with current limitation capability is presented. The proposed gate drive enables the SSCB with breaker mode and limiter mode. The limiter mode can help the fault-tolerant-capable system with ride-through capability for healthy parts of the system. For the limiter mode, the current limitation is realized by lowering the gate voltage and the power semiconductor can limit the system fault current based on its *V-I* characteristics. The current limitation level can be flexibly tuned by the gate voltage. And the limitation time is programmable. Based on a 200V/10A GaN-based SSCB engineering prototype, experimental results show that the system current can be limited to 20 A when v_{GS} = 2V to help the healthy part ride through the fault. Moreover, the lower the junction temperature, the higher the current limitation level.

Finally, the overall design of a system-friendly SSCB is developed and demonstrated. Two fault current detection circuits, DeSat-SSCB and PreDesat-SSCB, are suitable for the SSCB application. Particularly, the PreDeSat-SSCB, considering both the fault current absolute value and *di/dt*, results in the increased fault detection response speedup by 10 X as compared to conventional desaturation detection based on the test. The system-friendly SSCB has four operation modes. Four operation modes, including normal mode, precaution mode, i^2t mode, and interruption mode, are offered: i) normal mode with the normal driving

voltage makes the efficient operation of the SSCB, ii) precaution mode with reduced driving voltage ensures the system's fault current lower than SCCR; iii) i^2t mode helps SSCB interrupt low fault current considering power devices' intrinsic thermal limit; iv) interruption mode allows SSCB's interruption at SSCR within 200 ns to 1 μs. Then, coordinated control enables SSCB to take corresponding actions to various fault cases: i) once the SC and/or high *di/dt* event is detected through PreDeSat-SSCB, the proposed SSCB lowers the power device gate voltage to ensure the system's maximum fault current below SCCR; ii) under the low-impedance fault when the fault current approaches SCCR, the proposed SSCB based on DeSat-SSCB triggering signal can interrupt the fault within 200 ns to 1 μs; iii) under the high-impedance fault when the fault current does not exceed SCCR, the proposed SSCB can interrupt the fault based on an external i^2t detection and protection unit; iv) finally, the SSCB is capable of fast fault recovery, i.e., when the fault is cleared by a local SSCB and the protection signal by PreDesat-SSCB disappears, the SSCB is able to be back under the normal operation

9.2 Future work

For aviation applications, SSCB still needs to do more test to make sure the product satisfy the aviation class requirements. For example, to verify SSCB's thermal performance in high-altitude with thin air, it is essential to deploy a high-altitude thermal test.

For system-friendly SSCB, the hardware solution is proposed. However, more works need to be completed from the system level. For example, methods to cooperate with different system-friendly SSCBs are important. Moreover, it is also important to learn

how to design system-friendly SSCB parameters to better serve the system, e.g., current limitation time, current limitation voltage, fault detection sensitivity, etc.

In some cases, one single power-based SSCB cannot satisfy the requirements of the high-power system. Thus, it is important to study how to parallel devices for SSCB. For example, it is important to study how to let fault current even flow through different power devices. Otherwise, some power devices flowing with high current may be damaged during the SC fault.

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