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Assessing Hardware Security Threats Posed by Hardware Trojans in Power Electronics

Quinn Kinzie
qkinzie@clemson.edu

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Quinn Kinzie
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Dr. Yingjie Lao, Committee Chair
Dr. Zheyu Zhang
Dr. Christopher Edrington

Abstract

This study investigates the threat of hardware Trojans (HTs) in power electronics applications, a rising concern due to the growing demand for cost-effective embedded solutions in power systems. With the supply chain for electronic hardware devices expanding globally, particularly to low-cost foundries in foreign locations, there is an increasing risk of HT attacks. While there has been extensive research on HTs in computer applications, little consideration has been given to their threat in power electronics. This study demonstrates the effectiveness of a power electronics HT by implementing a novel HT design into a gate drive circuit. Additionally, the research proposes several HT designs that exploit factors unique to power circuits, such as high power delivery and analog circuitry in order to illustrate the distinct attack space. The research highlights the need for enhanced detection, protection, and prevention methods in power electronics applications and offers a roadmap for future studies to develop more effective countermeasures and algorithms to mitigate the risks of HT attacks in power electronics.

Acknowledgments

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Chapter 1

Introduction

1.1 Hardware Security

Power electronics are rapidly evolving with the integration of computers and electronics in embedded systems, a revolution driven by the Internet of Things (IoT). Power systems are being enhanced with unprecedented computational power. Meanwhile, the migration to network-enabled monitoring systems and control approaches is connecting power electronic devices all over the world [1–3]. This transformation is impacting a diverse range of technological industries, ranging from life-saving medical devices to cutting-edge military operations [4–7]. Due to the widespread use of hardware devices in critical systems, hardware security has become an increasingly important research area. Contrary to the remote nature of cyberattacks, hardware attacks occur within the physical system, presenting adversaries with another avenue for attacks distinct from the software and network domains [8].

In order to employ a hardware attack, the attacker must have physical access to the victim's device at some point in its life cycle. However, as the supply chain for electronic hardware devices expands globally to include low-cost foundries in foreign locations, the opportunities for attacks are also increasing. This is because electronic components become more accessible and vulnerable to exploitation, allowing untrusted actors to infiltrate the supply chain and introduce malicious hardware or software [9, 10]. This shift in design flow can be attributed to the trend of shrinking transistor technologies and increasingly complex device fabrication, which have driven up manufacturing costs [11]. In order to remain competitive in the dynamic market, companies outsource some stages of device production to third-party vendors in low-cost countries where trust has yet to be established. Intellectual property (IP) theft can occur, by which untrusted parties can abuse their access to client IP by stealing ideas and implementing them for commercial gain [12]. Additionally, untrusted fabrication centers may engage in covert overproduction of electronic devices, which they can sell at a profit without incurring any design costs [13].

1.2 Hardware Trojans

In addition to theft, an adversary with access to the device can execute various nefarious attacks, such as mechanical damage, intellectual property theft, and reverse engineering. Furthermore, if they obtain the device netlist before production, they can insert hidden, malicious circuitry known as a hardware Trojan (HT) to compromise device security and functionality. Hardware Trojans are particularly common in integrated circuits (ICs), which are used in power electronics for processing information and controlling other devices [14]. Due to their compact and complex design, ICs are frequently outsourced to third-party vendors for manufacturing, making them prime targets for hardware Trojan attacks [15]. The HT architecture can be decomposed into a trigger and a payload, as shown in Fig. 1.1. The trigger relies on a specific input combination or rare event to determine when the Trojan will be activated, while the payload is the malicious behavior the Trojan delivers to the system.

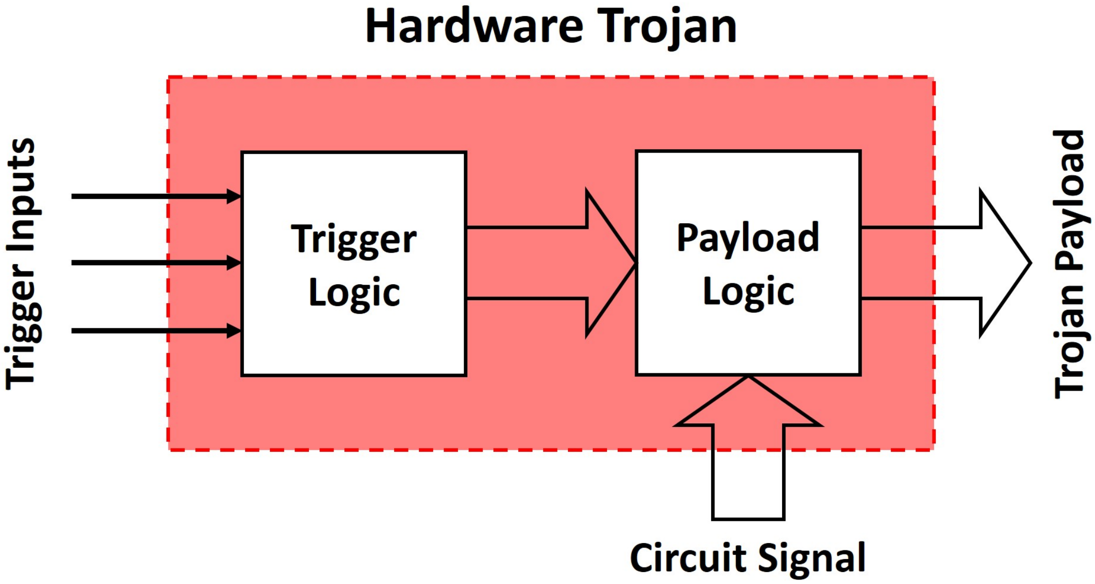


Figure 1.1: Hardware Trojan Architecture

1.3 Research Motivation

While there is substantial research into HTs in computer applications and various publications outlining HT detection and protection approaches [16, 17], there has been little consideration in the academic community of their threat within power electronics applications. As a result, there are few, if any, publications on the topic. This thesis explores the novel and unexplored research space of HTs designed to target power electronics and investigates two main research objectives. The first was to demonstrate the effectiveness of a power electronics HT, achieved through the design, implementation, and analysis of a novel and functional power electronics HT inserted into a gate drive IC. The second objective was to shed light on the vulnerabilities and scope of the attack space in the gate drive IC, accomplished by proposing several HT payload and trigger designs that are viable for implementation in the gate drive IC. The purpose of this research is to demonstrate and assess the viability of HT attacks in power electronics, with the goal of advancing HT detection, protection, and prevention methods for power electronics applications.

This thesis is organized as follows: Chapter 2 provides an overview of HT attacks, details previously proposed HT detection methods, and argues for the importance of developing such approaches for power electronics applications. Chapter 3 outlines the methodology of this study. Chapter 4 describes the implementation and analysis of a novel power electronics HT designed to attack the gate drive IC's fault protection circuitry. Chapters 5 and 6 propose several HT payloads and triggers designed for the gate drive IC, addressing the implementation efficacy and limitations of each attack. Finally, research conclusions and future work are discussed in Chapter 7.

Chapter 2

Background

2.1 Threats in the Supply Chain

The widespread implementation of electronic hardware has led to the development of various types of hardware attacks that can compromise a system's functionality or privacy, including physical damage, reverse engineering, piracy of IP, and hardware Trojans [18–20]. Given the variety of potential attacks, companies must be mindful of hardware threats at every point in the product lifecycle, all the way through design, fabrication, application, and disposal. Fig. 2.1 highlights some of the most significant hardware security threats at each stage in the product lifecycle.

2.2 Hardware Trojans

A hardware Trojan refers to malicious circuitry that is discretely inserted into an existing circuit during the design or manufacturing stage of production. The HT architecture is composed of two parts: a trigger and a payload. Under normal operating conditions, the HT remains dormant and does not affect the behavior of the circuit. However, once the Trojan is triggered, the payload executes malicious activity within the circuit. Sections 2.3 and 2.4 examine hardware Trojan payloads and triggers, respectively, providing an overview of their taxonomy and detailing examples of their implementation.

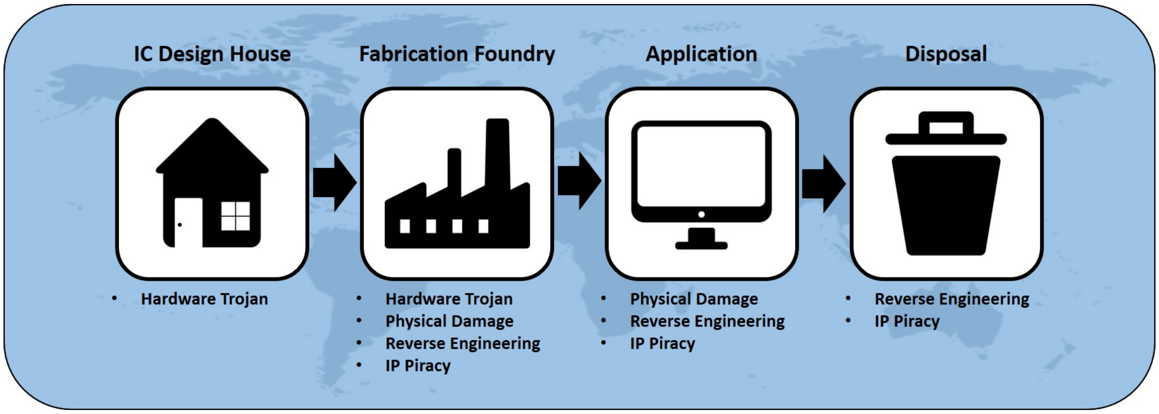


Figure 2.1: Security threats at each stage in the product lifecycle

2.3 Payload

The payload of the HT is the malicious behavior performed by the HT within the compromised circuit. The payload mechanism must be implemented stealthily into the device so that it is challenging to identify by physically inspecting the hardware. It is also essential that the payload's behavior is not evident during standard functionality so that it will be undetectable during pre-implementation testing. Attackers accomplish low detectability in the HT design by employing a trigger mechanism. The payload remains dormant until triggered, meaning that the trigger mechanism must isolate the payload function from the standard functionality of the circuit. Once triggered, the payload performs malicious actions based on the attacker's intention. Three common goals of HT payloads are to compromise functionality, damage circuitry, or leak sensitive information. This taxonomy and numerous HT benchmarks are details in a database provided by Trust-Hub [21, 22], a resource sponsored by the National Science Foundation to facilitate research and technology development in the domain of hardware security. Many of the HT examples described below will be drawn from this database.

Payloads that ***compromise functionality*** may include denial-of-service or altering a system function [23–25]. For example, a denial-of-service attack was designed to disable a medical implant device by activating a continuous shift register function and draining the device battery [21,22]. On the other hand, altering system functionality may involve delivering an incorrect output or causing a program to malfunction. For example, a Trojan payload was designed to hinder data encryption by flipping a bit in the encrypted output upon activation [21, 22].

Payloads that ***damage circuitry*** involve identifying and exploiting a vulnerability in the system through which hardware or software can be damaged [26]. Damage can occur through actively hostile operations or passive modifications that cause the system to harm itself or degrade over time. [15] outlines techniques for dynamically adjusting a device's voltage and switching frequencies within its functional specifications but at levels that induce stress on the system. This stress can lead to performance degradation and accelerated hardware aging over time.

Payloads that ***leak information*** involve broadcasting sensitive information from the compromised device [26–28]. Trojans that leak information do not require a trigger since they typically do not affect the fundamental behavior of the circuit and will only be detected through power monitoring or some other form of side-channel analysis. A Trojan of this kind was proposed that utilizes voltage modulation on an unused pin to generate a radio frequency (RF) signal containing the encryption key, which can be intercepted and collected using an AM radio [21, 22] .

2.4 Trigger

The trigger of the HT is the event that activates the HT and delivers the payload. HT triggers bypass functional testing by relying on rare events, such as an atypical set of inputs or an unusual system state. Three common types of HT triggers are user-input by physical access, internal trigger by counter or event, and always-on [21, 22].

User-Input Trojans require the attacker to have physical access to the device in the field. [29] describes a "kill-switch" HT attack implemented into a microcontroller. The Trojan activates upon an attacker delivering an external signal, causing the Trojan to shut down the device. In [21,22], another Trojan is described, which leaks a private secret key whenever a specific text code is provided to the system. A strength of this type of trigger is that the attacker can precisely facilitate when the Trojan is activated. However, user-input attacks are often impractical if the device is in motion or resides in an unknown location.

Internal Trigger Trojans allow for a more autonomous attack, relying on the input scheme or state of the system to trigger the HT. Using this type of trigger, a HT can pass functionality testing by remaining dormant during testing and then triggering after it is in active use [30]. A widely used internal trigger mechanism for Trojan activation involves a time-based approach. The Trojan is programmed to activate only after a predetermined value on a counter or timer has been reached [31–33]. A time-based Trojan may leak sensitive information after a predetermined number of clock cycles or instruction executions. On the other hand, a state-based trigger may activate the Trojan when it detects a specific address on the first eight bits of an address bus [21, 22].

Always-On Trojans are permanently active and do not require a trigger. These types of HTs typically involve leaking or broadcasting sensitive data but may also include analog attacks, which involve changing physical parameters or components from the design specifications to cause faster device aging and degradation [26, 34]. Since the payload does not affect the system's primary function, the HT may not need a delayed trigger to ensure the Trojan passes testing. Always-On Trojans have been implemented by introducing additional components or modifying the physical properties of transmission lines to facilitate crosstalk, allowing the extraction of signals through covertly added transmission lines or external receivers [21, 22].

2.5 Previous HT Detection Methods

A variety of approaches have been developed to detect the insertion of hardware Trojans in electrical hardware, both during production testing and run-time. The approaches discussed in this section are Functional Testing, Structural Testing, Side-Channel Analysis (SCA), Run-Time Monitoring, Functional Obfuscation, and Structural Obfuscation.

Hardware Trojan can be detected through ***Functional Testing*** methods [35, 36], in which input schemes are applied to the system, and the observed outputs are compared with the expected outputs. This method aims to drive the system into all expected states in order to trigger the Trojan and reveal the attack at the output. While this method can be effective for simpler systems with few I/O ports, it has numerous shortcomings. First, as systems become more complex, the number of inputs and system states in a single device grows exponentially. As a result, exhaustive test procedures that check every input pattern are becoming impractical [37]. Secondly, HTs may perform unexpected functions that will not be detected in standard test schemes [29]. Thirdly, input testing may not reveal the Trojan if it is triggered by sequential events or activates under unexpected conditions [38].

HT detection by ***Structural Testing*** is addressed in [15, 36]. Structural testing involves examining the physical device after manufacturing to confirm the fabricated circuitry matches the intended design. However, without state-of-the-art inspection equipment, this is most easily accomplished through destructive reverse engineering. By removing the packaging and delayering the IC, the structure of the circuit can be observed to confirm it is Trojan-free. The disadvantage of this approach is that it is both time-consuming and requires sinking the cost of destroyed components [39]. Additionally, reverse engineering will likely fail to detect Trojans if they are only implemented in some of the manufactured chips.

This method is expanded upon through the use of ***Side-Channel Analysis (SCA)*** to detect unwanted circuitry [40, 41]. In this method, a "side-channel fingerprint" is developed by taking parametric measurements of a "golden model" chip, whose functionality and security have been confirmed by extensive I/O testing, destructive RE, or development in a trusted foundry [42]. These parametric measurements include power consumption, electromagnetic radiation, thermal emissions, or timing path delay. SCA detects Trojans in future chips by comparing the side-channel fingerprint of the device under test to that of the golden model. SCA is a promising detection technique, but it has its weaknesses. Like the previous detection methods, SCA suffers from scaling concerns as greater chip complexity leads to increased noise interference and process variation, making it difficult to confirm the presence of a HT [43, 44]. For this reason, SCA is most effective when the chip has low process variation and the Trojan consumes most of the chip's power and space resources. Conversely, it will begin to detect false positives when the chip has large amounts of process variation and the Trojan makes up a small portion of the circuit [45]. Multi-parameter side-channel analysis can help mitigate this problem by analyzing the process variation of multiple parameter measurements [46]. This approach helps eliminate the effects of process variation and reveals the parametric effects of the Trojan, making it easier to detect and address the attack.

Run-Time Monitoring techniques have been proposed which use machine learning (ML) to detect Trojans in real-time while the infected device is in operation [47, 48]. The ML algorithm can learn to recognize the system's usual performance, allowing it to detect anomalies caused by HT activation. The system can be designed to shut down in self-protection or reconfigure the system architecture to avoid the effects of the Trojan. ML models can also be employed during testing to automate and accelerate the collection and analysis of parametric measurements [15]. Research into ML Run-Time detection approaches is promising, but the techniques have significant overhead challenges. ML detection approaches demand a significant investment in software and hardware resources, including a larger dataset for ML algorithm training, increased system complexity, and implementation challenges [49].

In place of post-fabrication detection techniques, [50] proposes two front-end HT prevention techniques, ***Functional Obfuscation*** and ***Structural Obfuscation***. In the Functional Obfuscation method, an additional hardware layer is added to lock the functionality of the circuit until one or more digital keys are used to unlock it. Without the key, the device will not run, and the behavior cannot be observed, making it difficult for adversaries to study the circuit and extract IP or HT vulnerabilities [51]. On the other hand, Structural Obfuscation involves reorganizing the circuit's physical layout or adding arbitrary circuitry to make it difficult for an adversary to determine the circuit's behavior by visual inspection. Obscuring the circuit design makes it difficult for adversaries to reverse engineer the circuit and insert HTs [52]. For obfuscation to be viable, the circuit must be sufficiently complex, or it will be difficult to hide the circuit's functionality. The proposed obfuscation methods protect against reverse engineering methods without affecting the circuit's behavior. However, they present a design tradeoff that pits prevention efficacy against area, power, delay, and production overhead.

2.6 Security in Power Electronics

All of the previously discussed HT detection methods were studied and applied in computer technology applications. In this section, the security discussion will shift to the power electronics domain. In recent years, there has been increasing recognition of cybersecurity threats in power systems due to the growing use of IoT devices and remote control methods in power applications [53–57]. In addition to the system-level discussion of cybersecurity, there have been publications outlining board-level approaches to detecting HTs in PCB applications [58, 59]. However, there are limited publications addressing HT attack and detection methods in power applications at the IC/component level. This section will first cover the progress of power electronics security approaches at the system and board levels. Secondly, it will address the need for research into HT detection methods and IC-level security for power applications.

The discussion of security in the power electronics domain has pertained primarily to the system-level cybersecurity threats arising from network-driven control of power systems [60–63]. If an attacker can breach the network that provides remote-control capabilities for vehicles or industrial equipment, they can potentially gain unauthorized access to the controls. This could allow them to disable devices or even shut down the entire control system, presenting a significant risk to the safety and operation of the equipment [64]. In addition, the high volume of data traffic between IoT devices on a compromised network can make it easier for cybercriminals to engage in IP piitse information, further exacerbating the risks associated with a network breach. The high switching speeds and power consumption required in power systems applications make it crucial to quickly detect and respond to cyberattacks in order to prevent potential damages to the system [14].

Regarding hardware security in power electronics, the literature has only gone as deep as discussing the detection of HT attacks at the board level. For example, [58] suggests in-system measurement testing by which trace impedances and passive component values are confirmed in order to validate the integrity of the board design. This method may require the insertion of test points on the board to provide external access circuit nodes. It also requires significant space and cost overhead to accomplish the in-system test implementation. Alternatively, [59] proposes a method of detecting HTs on the PCB during in-field operation by monitoring the power consumption and using tuned thresholds to determine the presence of hardware Trojan activity. However, this detection approach assumes that the PCBs are functioning correctly with no faults. This is problematic due to the reliability problem in power electronics.

Reliability issues are prevalent in power electronics, as high-frequency switching and temperature cycling cause aging and stress on the physical components within the system. Over time, the thermal stress and power consumption lead to frequent failures in power devices [65]. Therefore, maintenance and component replacement are expected in the product lifecycle, and component failures do not raise suspicion of hardware attacks. As a result, HT attacks may be misdiagnosed as reliability faults, putting the reliability and security of the system at risk. For this reason, it is critical to advance research into power-related HT implementations and novel detection techniques that can identify HTs designed to evade traditional testing methods. Furthermore, as the advancement of IC technology drives their increasing implementation in power electronics [66, 67], thereby expanding the supply chain and introducing new vulnerabilities, the need for HT countermeasures grows even more vital.

Chapter 3

Methodology

3.1 Attacking the Gate Drive IC

In order to study hardware vulnerabilities in power systems, a typical power electronics circuit was chosen as a benchmark. The experimental circuit is a gate drive circuit with fault detection, specifically the ACPL-339J Dual-Output Gate Drive IC. The mechanics of this circuit were modeled in PSPICE ORCAD Capture circuit simulation software. The circuit was constructed in PSPICE and studied for vulnerabilities.

An overview of the gate drive architecture is shown in Fig. 3.1. The circuit drives a low-voltage PWM input to a high-voltage output. The ACPL-339J IC is equipped with short-circuit detection, which will trigger protective shut-down procedures within the device when a short-circuit fault is detected at the output. In the case of a short-circuit fault, the fault protection will electrically isolate the output from PWM logic, breaking the path from input to output. Additionally, the logic activates a transistor that provides a path from the output transistor's gate terminal to ground, effectively shutting off the device to prevent it from damage.

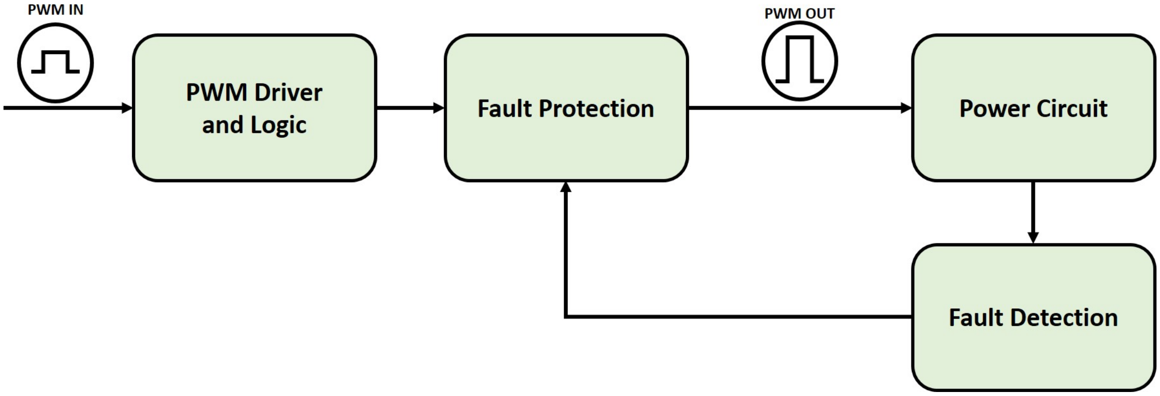


Figure 3.1: Basic architecture of the gate drive circuit

3.2 Fault Condition Trojan

The first goal of this research was to attack the fault detection circuitry and demonstrate how simple logic operations in a power electronics IC can pose security threats to the system. A hardware Trojan was proposed that could be implemented into the fault detection circuitry. This Trojan is referred to as the Fault Condition Trojan and will be discussed in Chapter 4.

3.3 HT Payload and Trigger Designs

After that, the research aim shifted to expanding the hardware security discussion into the power electronics domain by presenting new attacks that can be implemented into the gate drive circuit. Four payloads and five triggers were proposed that could be implemented into the gate drive circuitry. The proposed payloads and triggers were analyzed separately to emphasize the distinct characteristics and harmful potential of each attack mechanism.

The HT payloads and triggers proposed and investigated in this study were selected based on their expected effectiveness in the gate drive IC environment. Specifically, they exploit unique factors of the power electronics domain. For example, while payloads in computers typically exploit low-power digital logic, power electronics such as the gate drive IC have higher power levels and analog circuitry. These characteristics create new opportunities for payloads that can damage the circuit and surrounding systems. As a result, this study focuses on analyzing HT payloads that utilize analog characteristics of power electronics to cause damage to the circuitry in the gate drive

IC. Additionally, trigger mechanisms in computers are often concealed by complex circuitry and a myriad of input combinations. In contrast, the gate drive IC is a relatively simple and deterministic circuit comprised mostly of analog components. The pinout diagram for the gate drive IC is shown in Fig. 3.2 [68]. By inspection, it is easy to conclude that the device has limited I/O behavior from which to draw inspiration for effective hardware attacks. The IC's two primary functions are driving a PWM signal voltage from low-power inputs to high-power outputs and short-circuit protection. HT triggers were chosen to exploit these mechanisms and other factors, such as time and temperature. Chapters 5 and 6 will discuss the implementation efficacy and limitations of each proposed attack mechanism.

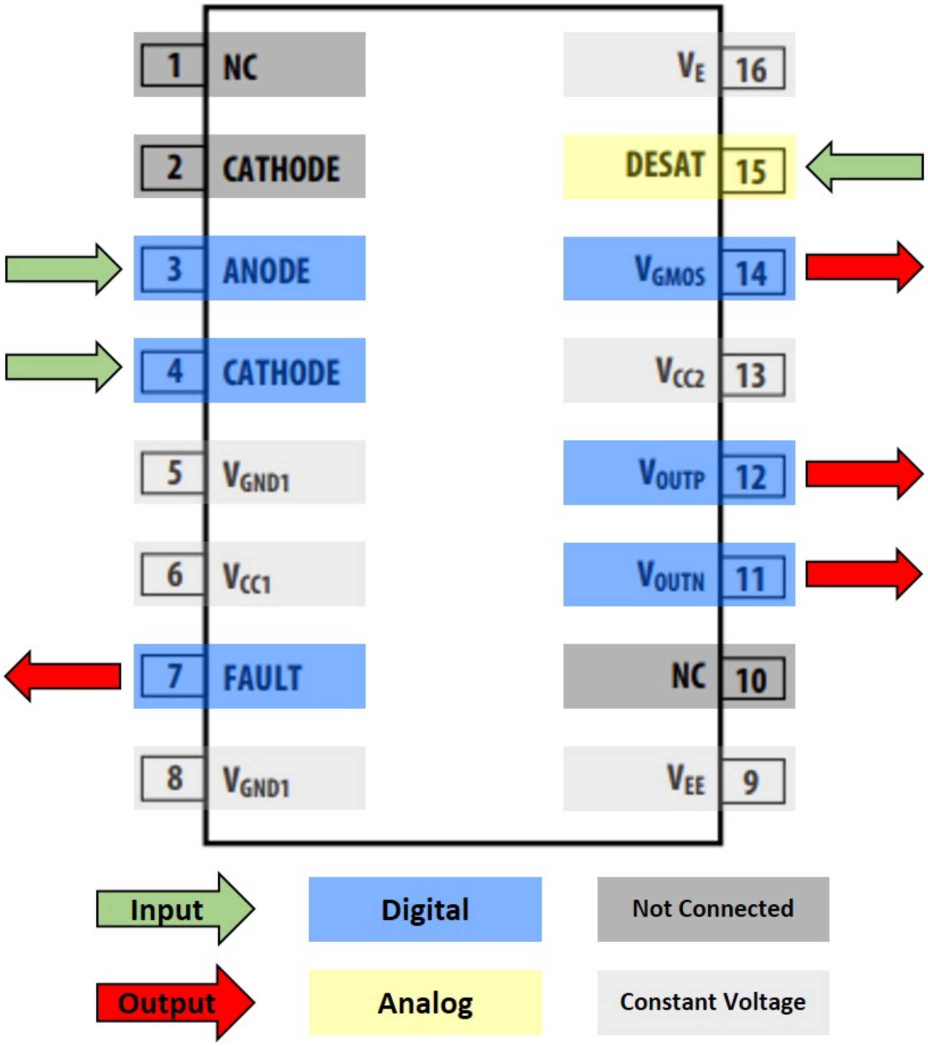


Figure 3.2: Pinout diagram of the ACPL-339J Gate Drive IC

Chapter 4

Fault Condition Trojan

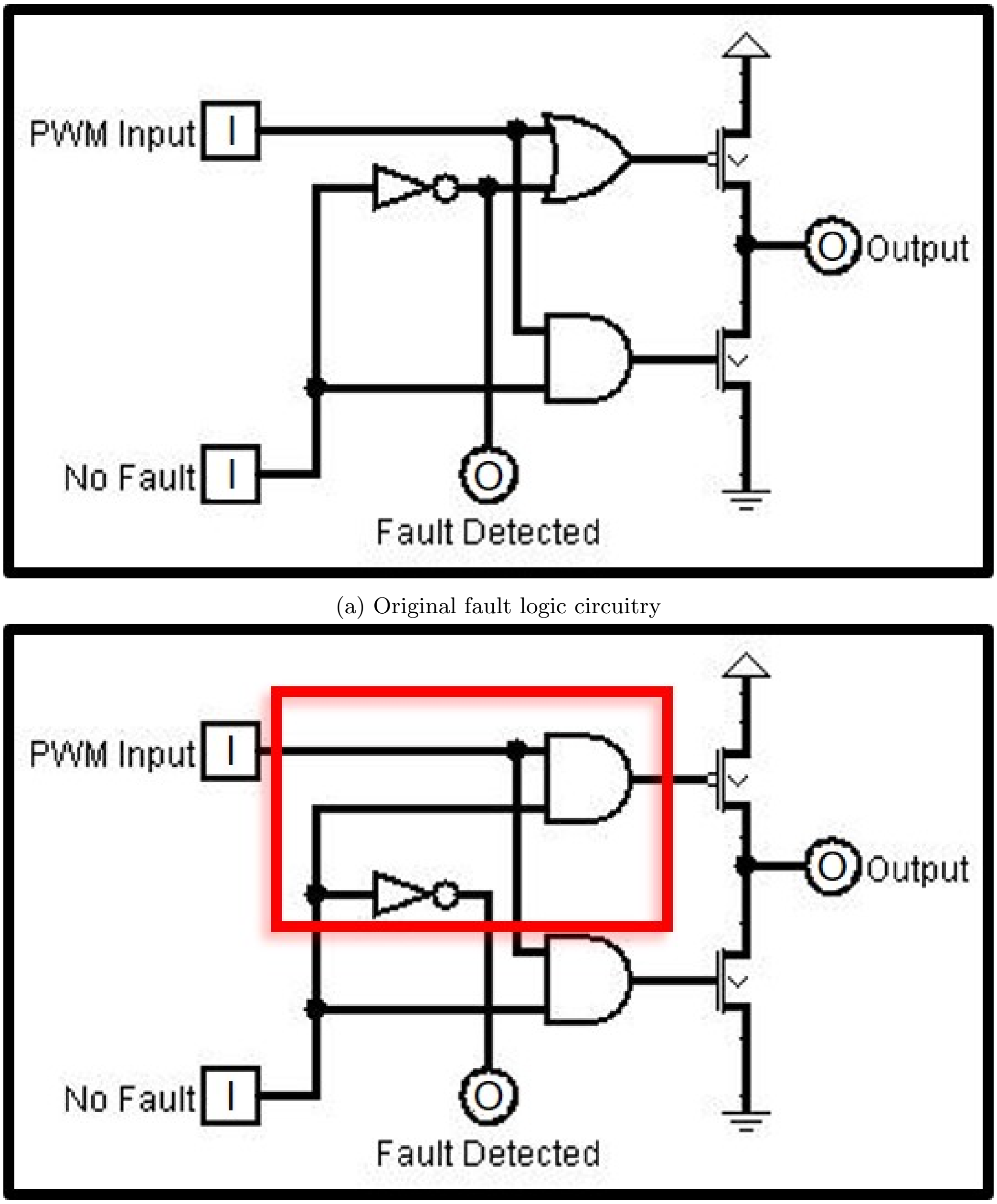
4.1 Exploiting the Fault Detection Logic

The Fault Condition Trojan was designed for the ACPL-339J gate drive IC and modeled in PSPICE simulation software. This Trojan demonstrates how an attacker can exploit simple logic implemented in a power electronics circuit. Specifically, it attacks the gate drive's fault logic, which is integrated with the system's desaturation (DESAT) short-circuit fault detection. The fault logic controls the transistors that propagate the input PWM signal to the output under normal conditions. When a short circuit fault is detected, the logic is designed to suspend vulnerable transistors so they do not sustain damage from conducting high currents.

The Fault Condition Trojan is implemented by swapping out one of the gates in the fault detection logic and modifying the gate connections, as shown in Fig. 4.1. The Trojan is triggered when a short circuit fault is detected at the output. Once triggered, the Trojan latches the output transistor in the active state, preventing the system's protective shut-down and forcing the transistor to conduct the short-circuit current.

4.2 Trojan Behavior

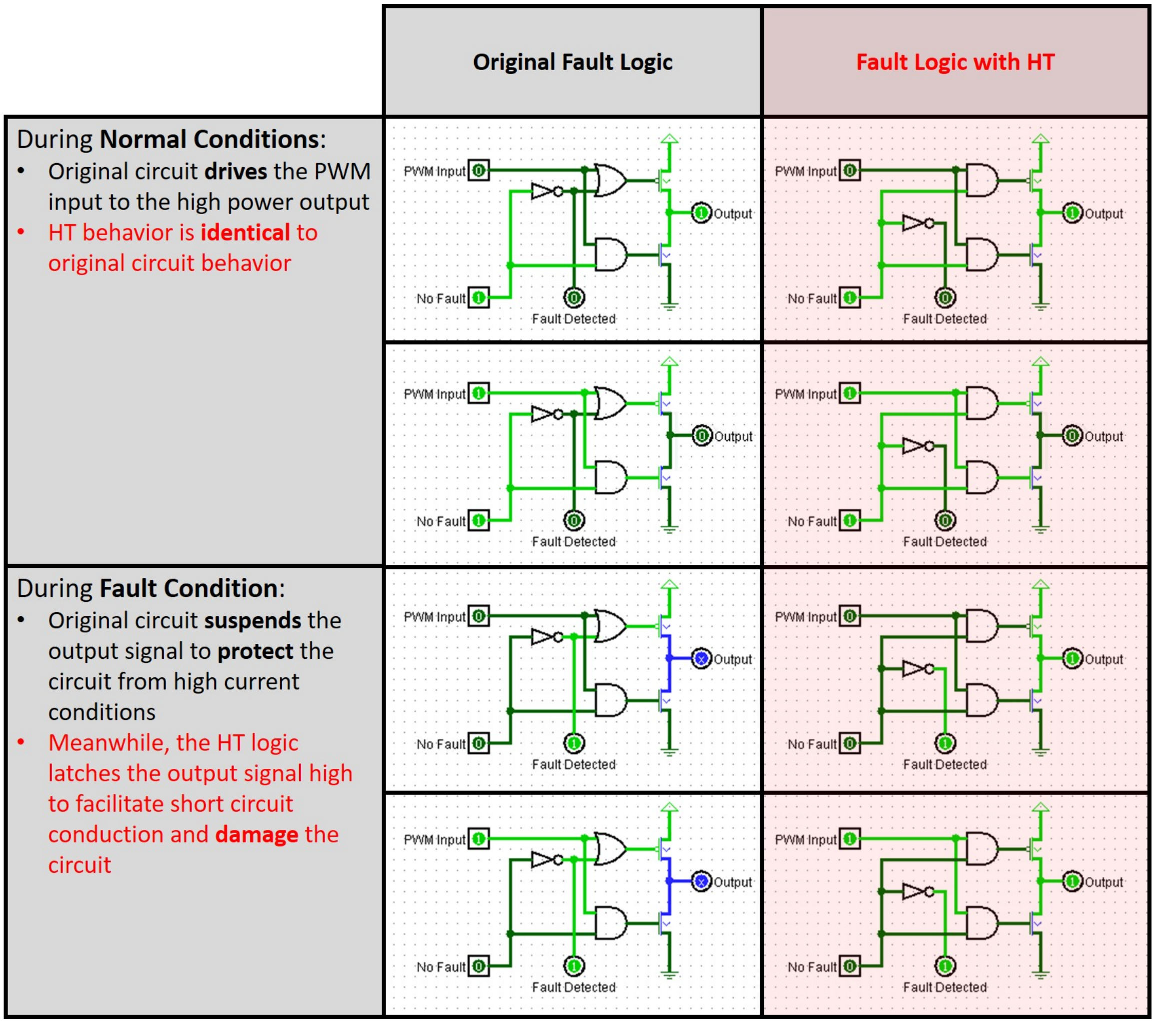
The circuit behavior before and after the insertion of the Trojan is shown in Fig. 4.2. Under normal operation, the circuit sends an inverted version of the input signal to the output to control the output power transistor, such that the voltage across the transistor mirrors the input voltage.



(a) Original fault logic circuitry

(b) Fault logic with Fault Condition Trojan inserted

Figure 4.1: The Fault Condition Trojan is implemented by slightly altering the fault logic. The red box shows where the OR gate was replaced with an AND gate, along with a couple of rewired connections



Original Fault Logic

Fault Logic with HT

During **Normal Conditions**:

- Original circuit **drives** the PWM input to the high power output
- HT behavior is **identical** to original circuit behavior

During **Fault Condition**:

- Original circuit **suspends** the output signal to **protect** the circuit from high current conditions
- Meanwhile, the HT logic latches the output signal high to facilitate short circuit conduction and **damage** the circuit

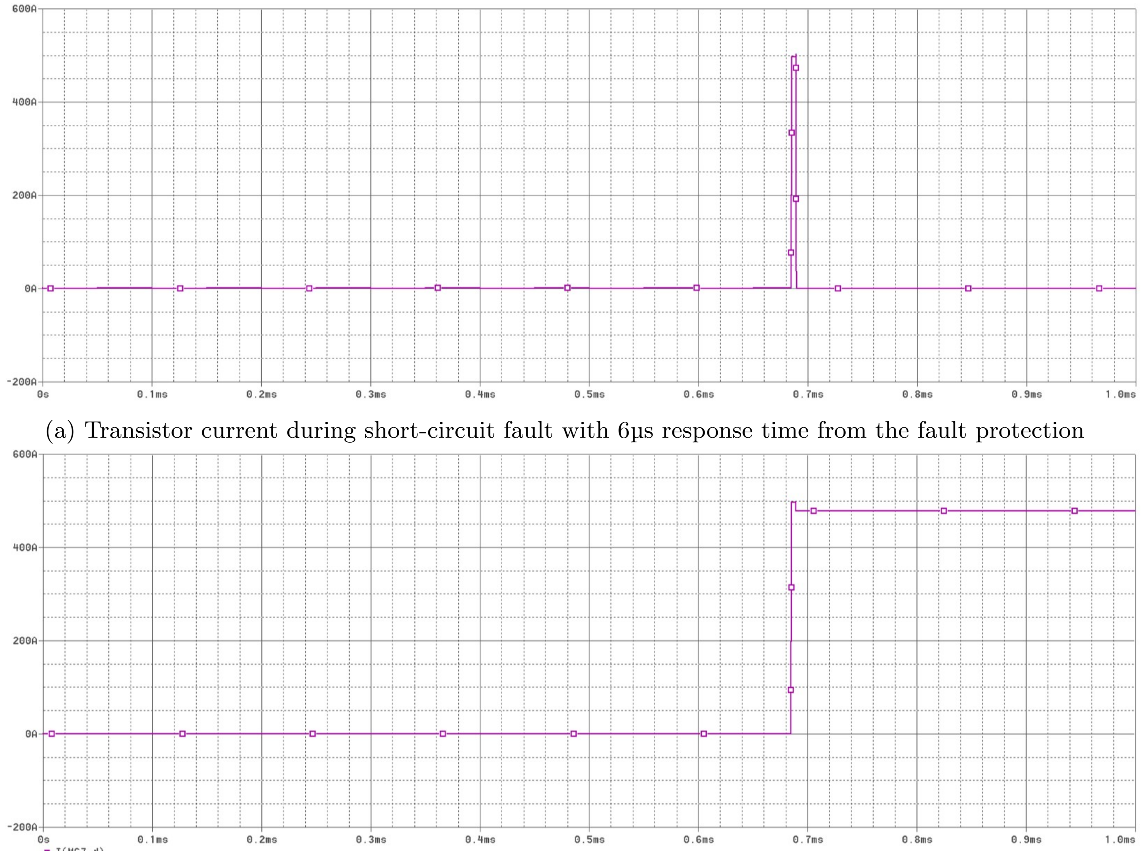
Figure 4.2: Behavioral comparison of the HT vs. the original circuit for every input/fault combination

When a fault is detected, the “No Fault” input voltage drops to zero, causing the logic to suspend the gate voltage of the output transistor. This shuts off the transistor, preventing it from conducting the short-circuit current and sustaining damage. The Trojan logic functions precisely the same under normal operation. When the “No Fault” signal is high, indicating that no fault has occurred, the Trojan logic sends an inverted version of the input signal to the output transistor. However, once a fault condition is detected, the Trojan behaves differently. Instead of suspending the output transistor, the Trojan ties the gate to a constant high voltage, forcing the transistor to conduct the short-circuit current.

4.3 Analysis

The Trojan-induced open-switch condition will damage the power transistor and likely cause issues with the circuitry downstream receiving a PWM signal that is constantly high [69]. Power switching devices, such as the TP65H035WS 650V GaN FET used at the output of the experimental gate drive circuit, can only withstand short-circuit currents for up to 13µs before sustaining damages [70]. Therefore, when this Trojan is activated during a short circuit fault, the output switching device will likely be destroyed. This demonstrates how an attacker could easily modify a circuit's logic, transforming its behavior from safeguarding against short circuit faults to exposing and damaging critical components and systems precisely when they are most vulnerable and in need of protection.

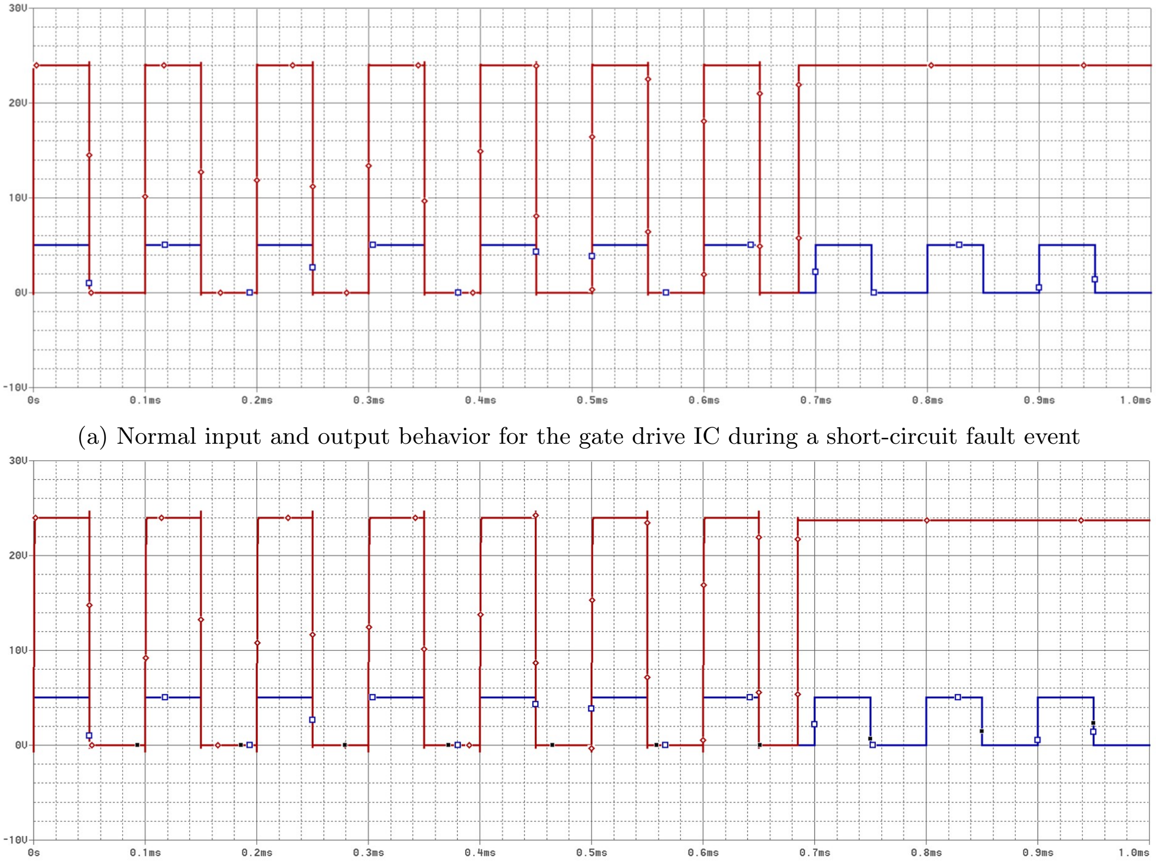
The transistor current during a short circuit fault is shown in Fig. 4.3a, which exhibits the response time of the gate drive's fault detection circuitry as it reacts to employ self-protective measures, shutting off the transistor in just under 7µs. On the other hand, Fig. 4.3b shows the transistor current for the Fault Condition Trojan, which prevents the gate drive's protective protocols and forces the transistor to bear the short-circuit current. Fig. 4.4a shows the input and output waveforms of the PWM signal during a fault-induced shutdown. The output voltage is latched to logic high after the short-circuit fault is detected at 685µs. This is because the switching transistor has been disabled by the protective circuitry, and the voltage difference across its source and drain indicates that current is not flowing. The I/O signals for the compromised circuit, shown in Fig. 4.4b, appear to behave similarly. However, after close inspection, it can be observed that the output voltage across the transistor experiences a slight drop after the fault occurs and the Trojan is triggered. This indicates that the high voltage drop observed across the transistor is not due to inactivity but is caused by its conduction of the short-circuit current, resulting in a significant portion of the voltage being dissipated through damaging levels of power consumption.



(a) Transistor current during short-circuit fault with 6µs response time from the fault protection

(b) Transistor current during short-circuit fault with extended short-circuit conduction due to the HT

Figure 4.3: Current spike through the output power MOFSET due to a short-circuit fault event at 685µs



(a) Normal input and output behavior for the gate drive IC during a short-circuit fault event

(b) Input and output behavior of the Fault Condition Trojan during a short-circuit fault event

Figure 4.4: The input and output voltages of the gate drive IC before and during a short-circuit fault event at 685µs

Chapter 5

Payload Designs

This chapter details the additional hardware Trojan payloads designed to attack the gate drive IC. The proposed payloads include Denial of Service, Circuit Damage, Internal Auxiliary System Attack, and Digital Communication Attack. At the end of the chapter, a system-level overview of the proposed payloads is illustrated in Fig. 5.1, and the discussion of results is summarized in Table 5.1.

5.1 Payload Type 1: Denial of Service

Description: This payload is delivered at the output of the circuit, known as a Denial of Service (DoS) attack. When triggered, a time-variant or normally active output is latched in an inactive state so that the behavior is disabled. This was implemented in the gate drive circuit by adjusting the PWM logic to disable the power transistor at the output. As a result, the output PWM signal becomes a constant low voltage, delivering no power to the output circuit.

Implementation Efficacy: This payload results in the system function or output being disabled, causing the system to shut down and require inspection and repair. If the DoS attack shuts down part of a grouped system, strain or damage could occur to the connected systems. A DoS attack has severe effects if it results in a system shutdown during crucial functionality, such as an aerial vehicle losing power mid-flight. A DoS attack is also relatively easy to implement since disabling any vital part of the system generally disables the output. DoS attacks are less likely to raise suspicion since faults are common in power electronics, meaning the fault is expected to be attributed to a reliability issue rather than malicious intent.

Limitations: The attack's severity depends on the vitality of the disabled function. A DoS attack may not result in significant damage or catastrophic results if it does not occur during crucial functionality. The attack may be attributed to a system fault and result in the failed device being replaced without causing substantial harm to the compromised system.

5.2 Payload Type 2: Circuit Damage

Description: This payload is delivered at the output of the circuit. When triggered, a time-variant output, such as a PWM, is tied in the active state. This is implemented in the gate drive circuit by altering the PWM logic to latch the output transistor in the active mode, delivering constant full power to the output power circuit.

Implementation Efficacy: Latching a circuit output to a high voltage will likely deliver damaging power levels to the devices and loads at the output. This is especially true in the case of a PWM circuit, where the power level is intentionally limited and moderated with switching methods. Payload Type 2 is very effective in causing harm to the target and may cause the system to be out of commission or need repair. The results can be catastrophic if this payload is delivered during a short circuit condition. The high power levels of the application make a circuit damage attack much more accessible to implement than in computer applications.

Limitations: Payload Type 2 requires careful design to properly exploit a system vulnerability such that physical damage is inflicted on the system. It is also a suspicious attack. Once the attack has occurred, the system will likely be closely inspected in root cause analysis. This means this type of attack will likely only be successful once, so its effects must be significant or it will not be very effective.

5.3 Payload Type 3: Internal Auxiliary System Attack

Description: This payload is delivered to an internal auxiliary system. The system can be activated or disabled depending on the desired attack. For example, a system may be falsely triggered when it is not supposed to, or it can be disabled so that it stops functioning or isn't functional when needed. Such systems can include internal monitoring, maintenance systems, or fault detection. In the gate drive circuit, this is implemented using logic to disconnect the digital input to the fault protection circuitry. When a fault is detected, the signal never makes it to the protection circuitry, resulting in the circuit failing to initiate protective methods and the output receiving the full effect of a short circuit fault.

Implementation Efficacy: If the fault protection circuitry is disabled, then the system cannot protect itself in the case of a short circuit fault. In our system, the fault protection circuitry disables the input logic and grounds the gate of the output power transistor. The result is that the transistor is shut off, ensuring that the high short-circuit current cannot pass through the transistor. An attack on this system allows the circuit to sustain severe damages during a short circuit fault. Payload Type 3 also has a lower detection probability at run-time, as it does not affect the primary function of the circuit. Therefore, it is less likely to be detected during primary functionality testing or after activation.

Limitations: Critical auxiliary systems are likely to be tested for correct functionality. To ensure this attack makes it through testing without being detected, it is necessary to carefully consider the vitality of the function under attack and choose trigger conditions.

5.4 Payload Type 4: Digital Communication Attack

Description: This payload is delivered to the internal digital communication system within the device. A digital communication line can be disabled, or a signal can be sent at an incorrect time. In the gate drive, this is implemented using simple logic to disable the IC's digital output pin related to the fault detection circuitry. The gate drive IC has a digital output pin that switches from low to high when a fault is detected. This Fault pin can be connected to a system controller to shut off power to the device at fault or manage the shutdown of related systems to protect the overall system from harm. By disabling this pin, the attack prevents communication with the controller and can result in protective protocols failing to initiate.

Implementation Efficacy: The Fault pin can be used to communicate with a control system in order to shut the system down so that the other portions of the system don't continue to run while the compromised system is malfunctioning. There are severe effects to disabling the subsequent communication systems of the fault detection circuitry. Attacking the Fault pin disables the device's communication of the fault to neighboring circuits, resulting in some parts of the converter running while the compromised device shuts down. Therefore, in the case of a fault, this attack causes damage to the greater system. An advantage of this attack is that it has lower detectability in functionality testing since it does not affect the main function of the circuit. It also may be less easily detected after triggering since it only affects subsequent functions.

Limitations: The fault pin attack requires a fault to occur. It also relies on the Fault pin being utilized for fault protection methods. The attack will be ineffective if the pin is not used for protective measures.

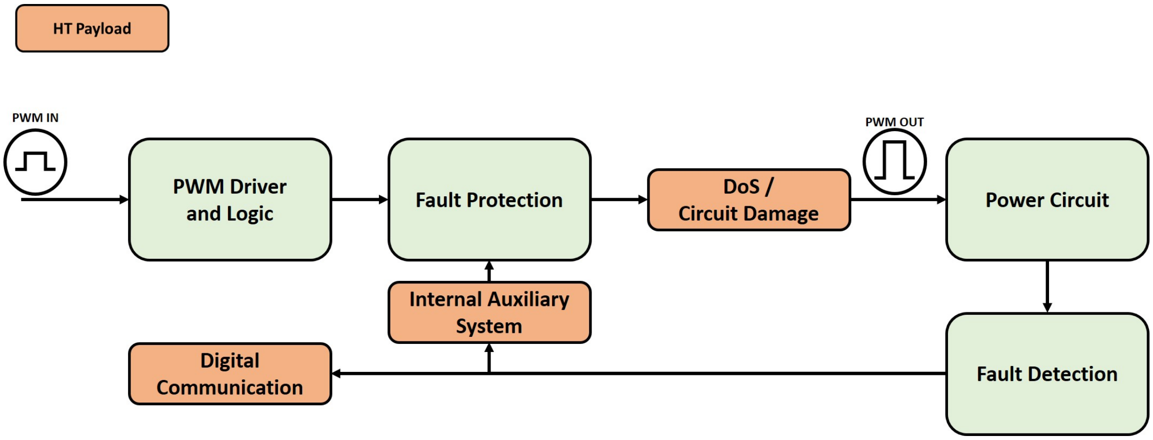


Figure 5.1: Proposed HT payloads for the gate drive IC

Payload	***Effect***	***Severity***	***Ease of Implementation***	***Stealthiness***
DoS	Disable output	Medium - High	High	Medium
Damage	Damage output switching transistor	High	Medium - High	Low
Auxiliary System	Cause auxiliary system to malfunction	Medium - High	High	Low - Medium
Digital Communication	Cause digital communication to malfunction	Low - Medium	High	High

Table 5.1: Summary of performance metrics for proposed HT payloads

Chapter 6

Trigger Designs

This chapter details the hardware Trojan triggers designed to attack the gate drive IC. The proposed triggers activate depending on the factors of time, system state, signal frequency, duty cycle, and temperature. At the end of the chapter, a system-level overview of the proposed triggers is illustrated in Fig. 6.1, and the discussion of results is summarized in Table 6.1.

6.1 Trigger Type 1: Time-based

Description: This trigger activates the Trojan after a certain amount of time. This time can be measured in real-time or run-time. In the case of real-time, the timer runs independently from the system and will activate the Trojan after a designated number of weeks or months. This design is best suited when the product deployment timeline is known, or there is a specific necessary time window for the attack. Alternatively, if the trigger is dependent on run-time, the timer is powered by the system or perpetuated by an internal clock. Since the timer will only run when the system is active, the trigger delay will depend on the time the system is actually running. This is a more optimal design if there is a long delay between product testing and deployment, or if it is necessary for the payload to be delivered during run-time.

A time-based trigger can be implemented with a counter, where the clock is connected to some binary signal in the circuit, such as a square wave, PWM signal, or digital signal. The trigger mechanism waits for a certain number of cycles and then activates the Trojan. The trigger delay is designed according to the switching frequency of the counter's input signal and the desired total trigger delay time. An independently powered clock is necessary for a real-time trigger delay, and standard testing and usage practices must be considered for a run-time trigger delay. In the gate drive, the counter clock is controlled by the PWM input for runtime measurement, but can be controlled by another internal voltage depending on the application. For example, the counter clock may be connected to the Fault pin such that it triggers the Trojan after a certain number of faults occur.

Implementation Efficacy: A real-time timer attack has very low detectability since it cannot be manually triggered. A run-time trigger would require many days or months of testing to detect the Trojan by activation. This trigger also has near-certain trigger probability since the attack is imminent given enough time.

Limitations: A real-time trigger requires an independent power source so that the timer can continue to run while the system is powered off, making it difficult to implement in smaller ICs.

6.2 Trigger Type 2: Fault Condition (State-based)

Description: A State-based trigger activates the Trojan when the system enters a particular state, such as a suspension state entered after the detection of a fault condition. Other system states may include low power mode, sleep, emergency lock-down, etc. A state-based Fault Condition attack exploits the short circuit fault detection circuitry. The implementation of this attack is discussed in more detail in the Fault Condition Trojan section above.

Implementation Efficacy: The gate drive's output transistor will sustain damages from the high current flowing through it. Additionally, the power circuit receiving the PWM control signal will receive full power delivery, potentially causing damage to electronic components and systems. The trigger probability of the fault condition Trojan is very high since faults occur commonly in dynamic power applications.

Limitations: A Fault Condition trigger will likely be detected in the product testing phase, as fault conditions are expected in power electronics systems, and fault detection systems will likely be tested for performance verification.

6.3 Trigger Type 3: Frequency

Description: This trigger activates the Trojan if the frequency of its input signal exceeds a particular threshold or enters a specific frequency range. This is implemented in the gate drive circuit by connecting the Trojan to the PWM input signal. Edge detection circuitry is used to detect the rising edge of the PWM signal and determine the signal frequency. The measured frequency is compared with the trigger condition frequency to activate the trigger when the trigger condition is met.

Implementation Efficacy: The Frequency Trigger can be tuned for a particular application. The detectability and trigger probability of a frequency Trojan will vary depending on the application and the design of the trigger. The further the designed trigger frequency is from the device's average functioning frequency, the less likely the trigger is to activate. The trigger likelihood of the Trojan is a matter of probability over the lifetime of the device.

Limitations: There is a tradeoff between the detectability and trigger probability of the frequency trigger. The more likely the trigger is to activate in the field, the more likely it will be detected in testing. Conversely, the stealthier the device is designed to be in the testing stage, the less likely it is to activate in the field to deliver the Trojan payload.

6.4 Trigger Type 4: Duty Cycle

Description: The duty cycle trigger activates the Trojan if the duty cycle of the input signal passes a particular threshold or enters a specific duty cycle range. This trigger is implemented in the gate drive IC using RC filtering to extract the duty cycle percentage value in reference to the source voltage. Comparators set the thresholds and trigger the Trojan when the designated duty cycle value or range is reached.

Implementation Efficacy: The implementation efficacy of the duty cycle trigger is very similar to that of the Frequency Trigger. Detectability and Trigger probability can be tuned by design and vary depending on the application.

Limitations: Similar to the Frequency Trigger, the designer of the duty cycle trigger must weigh the trade-off between a stealthy design with low detectability and an effective design with high trigger probability.

6.5 Trigger Type 5: Thermal

Description: The Thermal Trigger activates the Trojan if the ambient temperature passes a particular threshold or enters a specific temperature range. A thermal sensor hidden inside the device measures the temperature of the system, and comparison circuitry determines if the designed temperature threshold or range is reached. If so, the Trojan payload is delivered to the circuit.

Implementation Efficacy: Similar to the frequency and duty cycle triggers, the trigger probability depends on the application and the chosen temperature thresholds.

Limitations: A thermal trigger is very likely to be triggered in the testing phase because thorough temperature testing is a common practice to verify system functionality at temperatures beyond the specified temperature range.

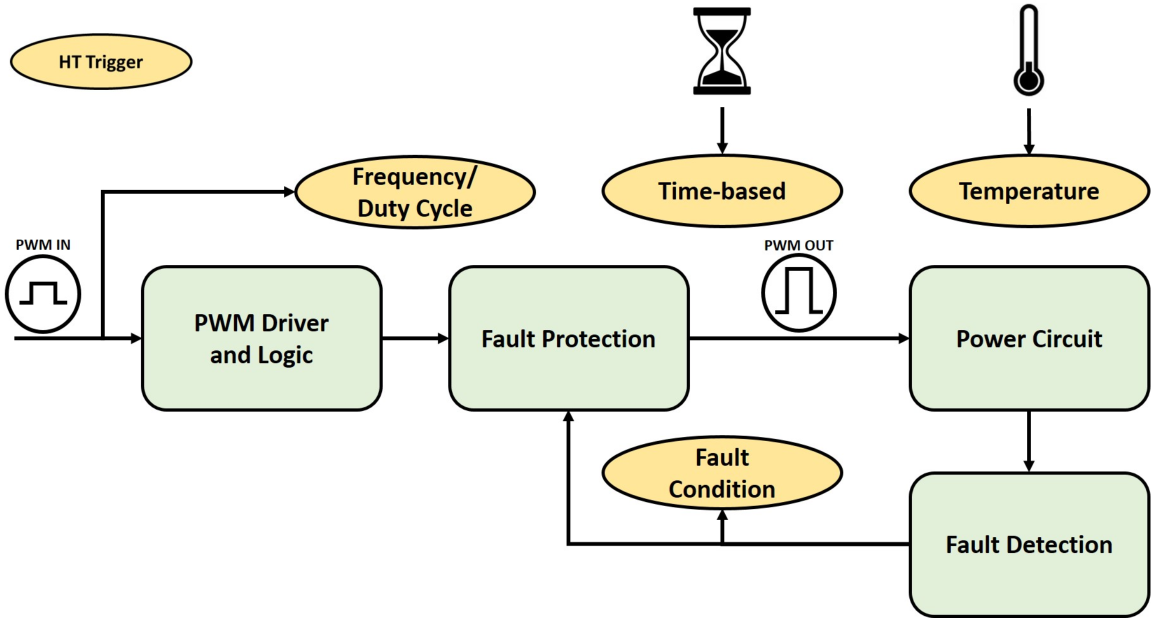


Figure 6.1: Proposed HT triggers for the gate drive IC

Trigger	***Trigger Condition***	***Trigger Probability***	***Ease of Implementation***	***Stealthiness***
Time	Timer reaches a predetermined value	Almost certain	Medium	High
Fault	Short-circuit fault is detected	Almost certain	High	Low
Frequency	Frequency of input signal enters specified range	Unlikely (tunable)	Medium	Medium - High
Duty Cycle	Duty cycle of input signal enters specified range	Unlikely (tunable)	Medium	Medium - High
Thermal	Temperature enters specified range	Unlikely (tunable)	Medium	Low

Table 6.1: Summary of performance metrics for proposed HT triggers

6.6 Trigger Combinations

In the previous sections, the efficacy and limitations of each attack mechanism were discussed in isolation. However, the performance of these triggers can be optimized when combined. By pairing the triggers together, the strengths can be optimized, and the weaknesses can be mitigated. It is important to consider these combinations, as they can make the Trojans much stealthier, and thus much more difficult to detect. We propose three significant trigger combinations in order to highlight the power of combining the triggers in a single application. The improved performance metrics of each trigger combination are covered in Table 6.2.

6.6.1 Timer + Frequency

Consider the combination of the Time-based Trigger with the Frequency Trigger. A design challenge of the Frequency Trigger is the trade-off between a stealthy design and a design that is likely to trigger. However, if it is combined with the Time-based Trigger is added, the combined trigger allows the attacker to guarantee that the Trojan will remain dormant until after the allotted time. This frees the attacker from the constraint of selecting a frequency or frequency range that is unlikely to be tested. Instead, the frequency can be chosen to optimize for the particular application. The Time-based Trigger can be combined with other triggers to create a time buffer before the other trigger becomes live and is ready to activate the Trojan. This can help the other triggers pass performance testing or buy time to build trust in the compromised system before deploying the payload.

6.6.2 Temperature + Fault Condition

Consider the implications of combining the Thermal Trigger with the Fault Condition Trigger. A shared weakness of these two triggers is that their trigger conditions are commonly tested in product testing schemes and, therefore, are likely to be detected during testing. Fault detection circuitry is likely to be tested to ensure the system can protect itself in the likely case of a fault. Similarly, the system will likely undergo thermal testing to verify temperature specifications and ensure proper functionality under extreme thermal conditions. However, if the two triggers are combined in series, such that both trigger conditions be met to activate the Trojan, the detection probability is drastically decreased. Consider the case where a high-temperature threshold is paired with a fault condition trigger. The likelihood that fault condition testing will be performed at extreme temperatures is low. It is more likely that fault testing and thermal testing will be performed independently of one another. Since the Trojan will pass fault condition testing at average temperatures, and a fault condition is unlikely to be detected or tested during thermal testing, the Trojan has a much higher chance of passing test procedures and making it out into the field.

6.6.3 Frequency + Duty Cycle

The Frequency Trigger and Duty Cycle Trigger may be combined to adjust their trigger probability. The trigger probability of each of these two triggers is tunable based on the chosen threshold or range. However, the Trojan's trigger probability can also be tuned by combining the two triggers, allowing for more reasonable threshold values. Then the trigger likelihood will have an additional input dimension and cannot be detected by a simple frequency or duty cycle sweep. Even at low probabilities, activation of the trigger is probable over a high amount of run time in the field.

Trigger Combination	***Trigger Probability***	***Ease of Implementation***	***Stealthiness***
Time + Frequency	Almost Certain	Medium	High
Thermal + Fault	Likely	High	High
Frequency + Duty Cycle	Likely	Medium	High

Table 6.2: Summary of optimized performance metrics achieved by combining trigger conditions

Chapter 7

Conclusions

7.1 Summary

The rapid growth of embedded systems in power electronics and the growing demand for cost-efficient solutions have led to the increased use of low-cost foundries in foreign countries, creating more opportunities for HT attacks. Despite extensive research on HTs in computer applications, there is a notable lack of consideration in the academic community regarding their potential threat in power electronics, resulting in a scarcity of related publications. This study ventured into the uncharted territory of HT research in power electronics, aiming to advance the improvement of functional testing schemes and the development of effective countermeasures against these attacks. By shedding light on this crucial area of concern, this study aimed to inspire further research and innovation in the field, ultimately leading to safer and more secure power electronics systems.

This research explored several HT attacks designed to target power electronics applications. A novel, functional hardware Trojan was implemented into a gate drive IC, which exploited the device's short-circuit fault protection logic in order to damage the output during a fault condition. Furthermore, several HT payloads and triggers were proposed which exploit the unique factors of the power electronics domain, such as high power delivery and analog circuitry. The proposed attack mechanisms are summarized in Fig. 7.1. The results demonstrated the potential of HT attacks in power electronics, highlighting the need for enhanced detection, protection, and prevention methods in power electronics applications.

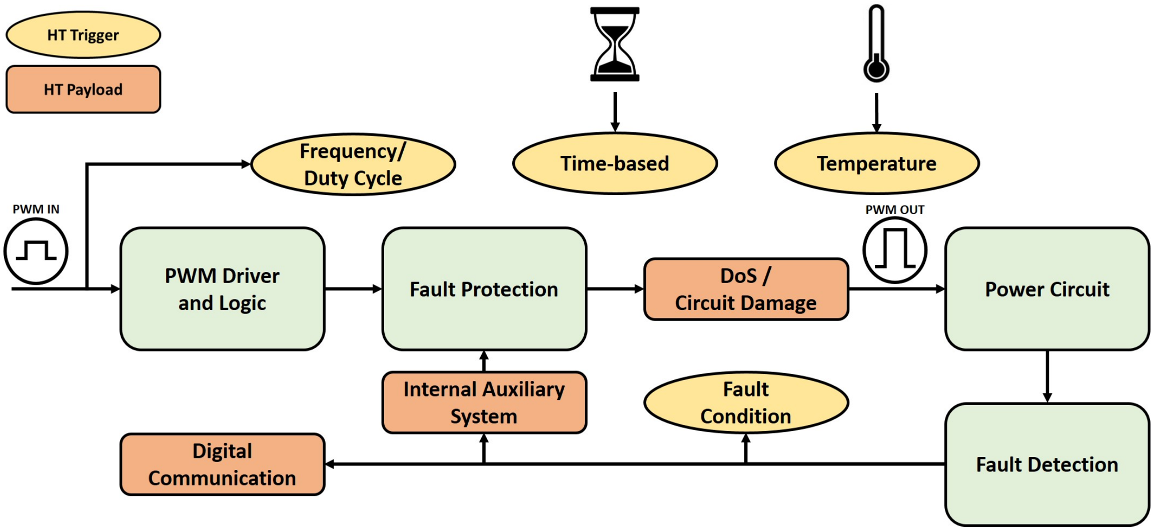


Figure 7.1: Summary of proposed HT payloads and triggers for the gate drive IC

7.2 Future Works

To build upon this research, further studies can be conducted to provide deeper insights into the design process of power electronics HT implementation by incorporating real-world benchmarks. This can help in understanding the impact of HT attacks on the performance and reliability of power systems. Additionally, by completing the HT design process through design, implementation, and testing, new insights can be acquired about attackers' approaches when employing HT attacks, which can help in developing more effective countermeasures. In particular, future research can focus on developing and evaluating detection and prevention schemes that mitigate the risks of HT attacks. This can involve the development of new algorithms and methodologies that can identify the presence of HTs in the system and analyze the system's behavior under HT attacks.

In summary, this study highlights the importance of addressing the threat of HT attacks in power electronics systems and provides a roadmap for future research in this area. With continued efforts to improve the design and security of power electronics systems, we can ensure their reliable and secure operation in critical applications.

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