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UNIVERSAL SHORT-CIRCUIT AND OPEN-CIRCUIT FAULT DETECTION FOR AN INVERTER

A Thesis Presented to the Graduate School of Clemson University

In Partial Fulfillment of the Requirements for the Degree Master of Science Electrical Engineering

> by Buck Ferguson Brown, III May 2023

Accepted by: Dr. Zheyu Zhang, Committee Chair Dr. Christopher Edrington Dr. Johan Enslin

ABSTRACT

Short-circuit and open-circuit faults of an inverter's power device often lead to catastrophic failure of the entire system if not detected and acted upon within a few microseconds, particularly for emerging wide bandgap (WGB) power semiconductors. While a significant amount of research has been done on the fast and accurate protection and detection of short-circuit faults, there has been less success corresponding to the research on open-circuit faults. Common downfalls include protection and detection that are too application-specific, take longer than a couple of microseconds, and are not costefficient. This study proposes a new open-circuit fault protection and detection system integrated with a pre-existing short-circuit system called desaturation protection. First, a literature review is conducted to confirm the necessity of the new protection and detection scheme. Second, the operation principle of the newly proposed protection and detection circuitry is discussed, and design considerations are given. Third, a comprehensive case study revolving around implementing the new protection and detection system is conducted using Synopsys/Saber simulation software. Fourth, an experiment is devised and constructed to showcase the protection and detection scheme's success, effectiveness, and adaptability in a real-world environment. Fifth, concluding remarks are given, summarizing all the work presented in this study. The results of testing the proposed system illustrate the success and reliability of the new fault protection and detection system.

ii

DEDICATION

The author would like to dedicate this work to his fantastic family. His wife and parents make accomplishments like this possible through their endless encouragement; his grandfather continues to inspire him to pursue this fascinating field of study; and his in-laws provide unprecedented support. He extends his sincerest appreciation to them and thanks the Lord for putting them in his life.

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TABLE OF CONTENTS

TITLE P	AGE	i
ABSTRA	АСТ	ii
DEDICA	ATION	iii
ACKNO	WLEDGMENTS	iv
LIST OF	TABLES	vii
LIST OF	FIGURES	viii
I.	INTRODUCTION	1
II.	DESIGN METHODOLOGY	5
	Desaturation Protection Design Additional Open-Circuit Fault Protection and Detection Open-Circuit Fault in the Forward Direction Open-Circuit Fault in the Reverse Direction Potential Solution Design Considerations	
III.	SIMULATION VERIFICATION	22
	Short-Circuit Fault Forward Current Open-Circuit Fault Reverse Current Open-Circuit Fault Freewheeling Diode Power Device Channel	
IV.	EXPERIMENTAL VALIDATION	
	Experimental Setup Power Stage Board Open-Circuit Fault Generation Board Gate Drive Board Auxiliary Equipment Combined Circuit Testing Process Control Signals Component Selection	
	Results and Discussion	

RKS	CONCLUDING REMARK	V.
	RENCES	REFER

LIST OF TABLES

Table II.I: Summary of additional design considerations	21
Table III.I: Simulation component values	23
Table IV.I: Parameters and components for experimental setup	48

LIST OF FIGURES

Figure 1.1:	Generic power device with protection and detection circuit and gate drive	1
Figure 2.1:	Simple single-phase inverter	3
Figure 2.2:	Forward current operation)
Figure 2.3:	Typical MOSFET cross-section in inversion10)
Figure 2.4:	Reverse current flowing through freewheeling diode1	1
Figure 2.5:	Typical MOSFET cross-section with current flowing through freewheeling diode	2
Figure 2.6:	Reverse current flowing through device inversion channel and freewheeling diode split 50/5012	3
Figure 2.7:	Typical MOSFET cross-section with current flowing through device inversion channel and freewheeling diode14	4
Figure 2.8:	Reverse current flowing through device inversion channel and freewheeling diode practically split15	5
Figure 3.1:	Effect of short-circuit fault with and without new protection and detection scheme on (a) drain current, (b) drain-to-source voltage, (c) voltage across the blanking capacitor, and (d) fault signal24	1
Figure 3.2:	Effect of forward current open-circuit fault with and without new protection and detection scheme on (a) drain current, (b) drain-to-source voltage, (c) voltage across the blanking capacitor, and (d) fault signal	7
Figure 3.3:	Effect of reverse current open-circuit fault in freewheeling diode with and without new protection and detection scheme on (a) drain current, (b) drain- to-source voltage, (c) voltage across the blanking capacitor, and (d) fault signal	1
Figure 3.4:	Effect of reverse current open-circuit fault in power device channel with and without new protection and detection scheme on (a) drain current, (b) drain-to- source voltage, (c) voltage across the blanking capacitor, and (d) fault signal	1
Figure 4.1:	Power stage board	3

39
40
41
42
45
46
50
51
55

CHAPTER ONE

INTRODUCTION

The growth of electrical energy production throughout the past few decades is unmatched. In 2011, 40% of the energy consumed in the United States was electrical [1]. As this rise in electrical energy production increases, the demand for reliable, highquality electrical components used in electrical energy production and conversion increases. While the reliability of electrical components used in electrical energy production has improved vastly over the past decades, the reliability of electrical components used in electrical energy conversion has lacked such drastic improvement.

In 2005, 30% of electricity flowed through power electronic converters [2]. This fact is no surprise considering power electronic converters are used in applications such as uninterruptable power supply systems, power supplies for telecommunication equipment, high voltage DC (HVDC) systems, distributed energy sources for renewable energy generation, battery energy storage systems, and power conversion systems for process technology [3]. Furthermore, 80% of electricity is expected to flow through power electronic converters in 2030 by the United States Department of Energy (DOE) as the nation pushes toward ambitious renewable energy penetration. However, these power electronic converters, specifically inverters, are often the bottleneck for reliable performance [4]. For example, based on the field data given by [5], photovoltaic (PV) inverters are responsible for 45% to 70% of PV service tickets, which significantly worsens the levelized cost of energy (LCOE) in the PV system. These inverters often fail due to the sensitive switching components within the inverter, such as Silicon Carbide

(SiC) MOSFETs or Gallium Nitride (GaN) HEMTs, being damaged and producing a fault, even leading to cascaded catastrophic failure of the entire inverter. In order to prevent such calamity, fault protection and detection in inverters is needed.

There have been many previous efforts to solve the problem of fault protection and detection in inverters. The two most common faults that occur are short-circuit faults and open-circuit faults. Short-circuit faults result in abnormally large currents. As these currents increase, the components' temperatures within the inverter increase, leading to inverter failure. This permanent damage occurs on a sub-microsecond scale, especially for emerging wide bandgap (WGB) power semiconductors. Due to such an apparent problem, short-circuit faults within inverters have been extensively studied. One solution, called desaturation protection, is widely applied and documented in [6].

Open-circuit faults also have drastic effects on components within an inverter. Most power electronic loads are inductive, so when an open circuit occurs, and there is no place for the current through the load to flow, there is a massive voltage spike across the opened power device due to high di/dt. The components within the inverter cannot withstand such high voltages for extended periods, so the inverter is damaged.

As with the short-circuit fault, there have been many attempts at protecting against and detecting open-circuit faults. However, unlike with the short-circuit fault, there lacks a universal, fast, and cost-efficient open-circuit fault protection and detection system.

In [7] and [8], an open-circuit fault protection and detection scheme for gridconnected inverters is proposed. However, [7] focuses on detection in a wind energy

conversion topology, and [8] focuses on detection in a grid-connected, three-phase, neutral point clamped topology. While both techniques successfully protect against and detect open-circuit faults within their given topologies, they are quite different. There is a trend of application-specific solutions throughout the related literature. As further examples, [9] considers a cascaded H-bridge multilevel inverter topology; [10] considers a T-type multilevel converter topology; and [11] considers a power converter in a PM-BLDC motor contained in an electric vehicle. Each solution proposed in [7]-[11] is significantly different due to its application-specific nature.

In recent literature, the speed and cost of protection and detection are two other significant issues pertaining to protecting against and detecting open-circuit faults in inverters. While [12] offers a solution for open-circuit fault protection and detection, it requires a minimum of 3.5 ms before protection and detection can occur. Newer data-driven and model-data-hybrid driven methods—[13] and [14] respectively—take a minimum of several switching periods (over 100 μ s) before they protect against and detect open-circuit faults. Additionally, some solutions require multiple sensors, bringing with them a high cost, as seen in [7], [8], and [12].

Therefore, it is essential to make a new fault protection and detection design for power devices capable of detecting short-circuit and open-circuit faults within a few microseconds. The new design should be universal and inexpensive. Through the modification of pre-existing desaturation protection techniques, the proposed fault protection and detection system is shown in Figure 1.1.



Figure 1.1: Generic power device with protection and detection circuit and gate drive

CHAPTER TWO

DESIGN METHODOLOGY

In this chapter, the design illustrated in Figure 1.1 is detailed. First, the shortcircuit protection and detection the circuitry provides is highlighted, and then the novel open-circuit protection and detection the circuitry provides is described. At the end of the section, practical design considerations are given.

Desaturation Protection Design

A standard desaturation protection circuit is the foundation of the circuit shown in Figure 1.1. This desaturation protection circuit (often called "desat") detects and protects against short-circuit faults. It consists of the following: a charging resistor, R_{CHG} ; a sensing diode, D_{sense} ; a blanking capacitor, C_{BLK} ; a positive comparator with a positive threshold voltage, v_{CSTH+} ; and a latch-up circuit. How the desaturation protection circuit functions is detailed in [6]. In order to work properly, its various components must be appropriately sized.

The equation used for determining the positive threshold voltage is given as

$$v_{CSTH+} = v_{DSTH} + v_{f_Dsense} \tag{1}$$

where v_{DSTH} is the drain-to-source threshold voltage of the power device, and v_{f_Dsense} is the forward voltage of the sensing diode, D_{sense} . The drain-to-source threshold voltage is found by examining the datasheet of the power device used in the circuit. The user must determine their desired drain-to-source threshold voltage based on the power device's operating gate-to-source voltage, v_{GS} , and threshold drain current, i_{DTH} . The forward voltage of the sensing diode is found from the sensing diode's datasheet.

Following the calculation for the positive threshold voltage, the blanking capacitance is found using

$$C_{BLK} > k_{Cj_Dsense} \cdot C_{j_Dsense} \tag{2}$$

where C_{j_Dsense} is the junction capacitance of the sensing diode, and k_{Cj_Dsense} is a scaling factor relating the junction capacitance of the sensing diode and the blanking capacitance. The junction capacitance of the sensing diode is found from the sensing diode's datasheet. The scaling factor, k_{Cj_Dsense} , is designed to ensure that C_{BLK} is significantly larger than C_{j_Dsense} to avoid the noise current induced by $C_{j_Dsense} \cdot dv_{DS}/dt$. Practically, it is chosen to be at least 50.

Next, the charging resistance is calculated. However, before it is calculated, the circuit's time constant is chosen according to the desired blanking time. Generally, it is chosen to be slightly longer than the turn-on switching time to avoid false triggering during the normal turn-on transient. This time constant is represented as:

$$\tau = R_{CHG} \cdot C_{BLK} \tag{3}$$

Rearranging (3) to solve for R_{CHG} yields:

$$R_{CHG} = \frac{\tau}{C_{BLK}} \tag{4}$$

The final aspect of the desaturation protection design is a latch-up circuit. Internally, this circuit consists of a simple SR latch with the reset pin low. Therefore, when a fault is detected, the output of the latch-up circuit reports it regardless of future inputs. This output signal is tied to the gate drive, so the power device is turned off when a fault signal is received. In addition, a "soft" resistor connected to the gate of the transistor is activated, increasing the gate resistance and allowing for a "soft" turn-off. Therefore, through desaturation protection, a short-circuit fault is detected, and the gate drive of the power device is shut down, protecting against cascaded failure throughout the system.

Additional Open-Circuit Fault Protection and Detection

There are two different classifications of inverter open-circuit faults, and it is essential to understand the difference between them. An open-circuit fault can occur when current is flowing through the power device in the forward direction, from drain to source (using MOSFETs' terminology as an example), or when current is flowing through the power device in the reverse direction, either from source to drain or through the freewheeling diode. To illustrate this, consider the simple single-phase inverter circuit without any passive components shown in Figure 2.1 [15]. In this setup, there are two nchannel MOSFETs, the AC current enters the middle node, and the gate signals behave as shown by the waves next to the gates of each MOSFET. The following analysis draws on the semiconductor physics of lateral-structure MOSFETs provided by [16] and [17]. After the different types of open-circuit faults are examined, the open-circuit fault protection and detection design is detailed.



Figure 2.1: Simple single-phase inverter

Open-Circuit Fault in the Forward Direction

If current flows through the power device in the forward direction, it flows from the drain to the source. A depiction of this type of operation is given in Figure 2.2. Based on the gate signals, the lower power device is on, and the upper power device is off. Since the lower MOSFET is turned on (assuming turned on means $V_{GS} > V_T$) and has a positive drain-to-source voltage, an inversion channel is formed. This inversion channel allows electrons to flow from the source to the drain by drift mechanisms. Therefore, since the load current is entering the middle node, the current will flow from the drain to the source of the lower device. A cross-section of a typical MOSFET under such operating conditions is shown in Figure 2.3.



Figure 2.2: Forward current operation

If an open-circuit fault occurs when current flows through the lower power device in the forward direction, the current through the load flows through the freewheeling diode of the upper power device. Therefore, there is no voltage spike across the lower power device due to high *di/dt*, and catastrophic failure is avoided. However, having the lower power device permanently off is still a control issue, and the inverter cannot function properly without repair. Hence, it is still important to be able to detect the opencircuit fault. While seemingly unknown, desaturation protection allows for the detection of open-circuit faults when current flows through the power device in the forward direction. When a forward current open-circuit fault occurs, the drain-to-source voltage of the power device becomes the DC bus voltage. Assuming this voltage is greater than



Figure 2.3: Typical MOSFET cross-section in inversion

the positive threshold voltage, v_{CSTH+} , of the desaturation protection, the open-circuit fault will be detected, and the power device will be turned off.

Open-Circuit Fault in the Reverse Direction

If current flows through the power device in the reverse direction, it flows from the source to the drain. Whereas forward current only flows through the channel of the power device, reverse current can flow through either the channel or the freewheeling diode of the power device. These reverse current open-circuit faults are estimated to account for about half of all power device open-circuit faults since current flows in the forward direction about the same amount of time it flows in the reverse direction in inverter circuitry. With only traditional desaturation protection implemented, it can take



Figure 2.4: Reverse current flowing through freewheeling diode

anywhere from 50 µs to 200 µs (depending on switching frequency) before reverse current open-circuit faults turn into forward current open-circuit faults and can subsequently be detected and protected. Since there is nowhere for reverse current to flow if an open-circuit fault occurs, this amount of elapsed time will likely allow permanent damage to the device and the surrounding inverter.

Clearly, a new protection and detection scheme is required if reverse current open-circuit faults are to be protected and detected. Before this scheme is described, the physics behind reverse current operation is briefly discussed since it is vital to understand that reverse current open-circuit faults can occur when the reverse current is flowing through the channel of the power device or the freewheeling diode of the power device.



Figure 2.5: Typical MOSFET cross-section with current flowing through freewheeling diode

This is a very valuable point of emphasis since some evidence suggests freewheeling diode open-circuit faults do not occur as often as inversion channel open-circuit faults, and thus, are not as important to protect and detect [18].

First, consider the case illustrated in Figure 2.4. In this scenario, both upper and lower power devices are turned off. This is a typical operating point in power electronic converters known as deadtime. Since both power devices are turned off, no inversion channel is formed in either power device. As a result, the preferred method of current conduction through the utilization of drift mechanisms is not possible. Alternatively, the freewheeling diode, which is a PN junction, allows for current conduction through diffusion mechanisms. While not as efficient, current can still be conducted via this



Figure 2.6: Reverse current flowing through device inversion channel and free wheeling diode split 50/50

method. A cross-section of a typical MOSFET under these operating conditions is shown in Figure 2.5.

If an open-circuit fault occurs in the upper power device of the circuit shown in Figure 2.4, there is no place for the current to flow; thus, catastrophic failure is likely to occur. Therefore, the new open-circuit fault protection and detection scheme must protect against and detect reverse current open-circuit faults that occur when current flows through the power device's freewheeling diode.

Second, consider the case illustrated in Figure 2.6. In this scenario, the upper power device is turned on while the lower power device is turned off. Since the current is



Figure 2.7: Typical MOSFET cross-section with current flowing through device inversion channel and freewheeling diode

entering the middle node, the drain-to-source voltage of the upper power device is negative. Despite this, an inversion channel is still formed in the upper device since a MOSFET is relatively symmetrical. At first examination, it may appear that half of the load current flows through the inversion channel of the upper power device while the other half of the load current flows through the freewheeling diode of the upper power device. This assumption is depicted in Figure 2.6. However, different results are obtained if the physics of the MOSFET is examined more closely. A typical MOSFET under these operating conditions is shown in Figure 2.7. As stated previously, the conduction of current through the MOSFET's freewheeling diode is not preferred when compared to the



Figure 2.8: Reverse current flowing through device inversion channel and freewheeling diode practically split

conduction of current through the MOSFET's inversion channel. This is because the conductivity of the MOSFET's inversion channel is much higher than the conductivity of the MOSFET's freewheeling diode. Therefore, most of the current flows through the MOSFET's inversion channel, not the MOSFET's freewheeling diode. A more accurate depiction of this phenomenon is shown in Figure 2.8.

If an open-circuit fault occurs in the upper power device of the circuit shown in Figure 2.8, there is no place for the current to flow; thus, catastrophic failure is likely to occur. Therefore, the new open-circuit fault protection and detection scheme must protect against and detect reverse current open-circuit faults that occur when current is flowing predominantly through the channel of the power device and slightly through the freewheeling diode of the power device.

The previous analysis was done using MOSFETs as an example. This was done because MOSFETs arguably have the most rigorous requirements when trying to protect against and detect reverse current open-circuit faults. The other prevalent power devices utilized in inverter topologies are insulated gate bipolar transistors (IGBTs). While these devices are governed by different physics, the analysis conducted for MOSFETs can easily be extended to IGBTs. The main difference is that an IGBT is not almost symmetrical like a MOSFET; thus, reverse current cannot flow through the channel of an IGBT. Therefore, the only type of reverse current open-circuit fault that can occur in an IGBT is a reverse current open-circuit fault of the freewheeling diode. Hence, only in the case of IGBTs are reverse current open-circuit faults synonymous with freewheeling diode open-circuit faults.

Potential Solution

Nothing new must be developed to protect against and detect forward current open-circuit faults—desaturation protection is sufficient. However, to protect the inverter against reverse current open-circuit faults and detect when reverse current open-circuit faults occur, the standard desaturation protection circuit must be enhanced. These enhancements are illustrated in Figure 1.1. They include three addendums to the traditional desaturation protection circuitry. The first addendum is the insertion of a branch in parallel with the drain and source terminals of the power device consisting of a diode, D_{open} , in anti-series with a Zener diode, D_z . The second addendum is the inclusion

of a noise immunity resistor, R_n , and its corresponding bypass diode, D_n . The third addendum is the introduction of a bipolar comparator with a negative threshold voltage, v_{CSTH-} . The output of this comparator is connected to the same latch-up circuit used for short-circuit fault detection.

Adding the branch consisting of a diode in anti-series with a Zener diode diminishes the catastrophic failure due to a reverse current open-circuit fault and allows for fault detection. During regular operation, current does not flow through this branch because the Zener diode blocks the current. When a reverse current open-circuit fault occurs, the Zener diode enters its breakdown region, allowing current to flow through the branch. As a result, the voltage across the branch is clamped to a specific value and is expressed as

$$v_{OC} = -v_{f_Dopen} - v_{z,b} \tag{5}$$

where v_{f_Dopen} is the forward voltage of the diode, and $v_{z,b}$ is the breakdown voltage of the Zener diode. The breakdown voltage of the Zener diode is up to the user to decide. Whereas traditionally there is no place for the current flowing through the load to go when a reverse current open-circuit fault occurs, it now has an alternative path.

The noise immunity resistor and corresponding bypass diode are essential to prevent the false triggering of the detection system due to switching ringing and interference [19]. They prevent the blanking capacitor from drastic fluctuations in the sensed voltage. Therefore, this noise immunity branch delays detection by approximately a microsecond, which is determined by the maximum switching time of the device under investigation. However, it is important to note that the protection given by the new opencircuit branch is ubiquitous.

Due to the constant voltage across the newly implemented open-circuit branch, it is easy to detect when a reverse current open-circuit fault occurs. The negative comparator leverages the voltage across the blanking capacitor and compares it with a negative threshold voltage given by

$$v_{CSTH-} = -(v_{f_Dopen} + v_{z,b}) \cdot x \tag{6}$$

where x is a scaling factor between 80-100% to compensate for potential nonidealities and ensure detection of the open-circuit fault. The outputs of the negative comparator and positive comparator are tied together before the latch-up circuit. This is done practically through an OR gate. Therefore, regardless of the fault type, the latch-up circuit output indicates if a fault has occurred.

Design Considerations

Aside from the previous theory used to size the components shown in Figure 1.1, a few considerations still need to be made before the circuit can be implemented in reality. In particular, special design considerations need to be made for five key components: the charging resistor, the sensing diode, the blanking capacitor, the Zener diode, and the standard diode contained in the open-circuit branch.

The first component that needs to be reconsidered is the charging resistor, R_{CHG} . Like always, the resistor's power rating corresponds to the power dissipated in the resistor. The power dissipated in the charging resistor is

$$P_R = \frac{v_R^2}{R_{CHG}} \tag{7}$$

where

$$v_R = v_{GS} - (v_{DS} + v_{f_Dsense}) \tag{8}$$

Under a traditional desaturation protection scheme, v_R is always less than v_{GS} since both v_{DS} and v_{f_Dsense} are positive values. However, with the additional reverse current opencircuit fault detection functionality, v_{DS} is negative when a reverse current open-circuit fault occurs. As a result, it is now possible for v_R to be greater than v_{GS} , and therefore, special attention must be given when determining the power rating of the charging resistor. It is also important to note that (7) and (8) are only applicable when considering the power device when it is turned on, undergoing a switching commutation, or experiencing a fault, since the power dissipated in the resistor when the power device is turned off is approximately zero.

The second component that needs to be reconsidered is the sensing diode, D_{sense} . When the diode is not blocking the drain-to-source voltage, the current through the sensing diode is

$$i_{Dsense} = \frac{v_{GS} - v_{f_Dsense} - v_{DS}}{R_{CHG}}$$
(9)

As with the resistor, when a reverse current open-circuit fault occurs, v_{DS} is negative, and i_{Dsense} is greater than it is under standard desaturation protection. As a result, special attention must be given to the maximum current flowing through the diode. In addition, the breakdown voltage of the sensing diode must be greater than the possible off-state

voltage of the power device. Furthermore, it is crucial that the sensing diode is a superfast recovery diode or a Schottky diode to reduce the noise produced when the sensing diode turns off. Likewise, the junction capacitance of the sensing diode should be as small as possible to reduce the displacement current induced during dv/dt when the power device turns off [6].

The third component that needs to be reconsidered is the blanking capacitor, C_{BLK} . As shown previously, the blanking capacitance is sized according to (2) and (3). The blanking capacitor should also be able to handle a voltage of

$$v_{CBLK} = v_{DS} - v_{Dsense} \tag{10}$$

Special attention should be given during switching transitions due to possible overshoot in voltages.

The fourth component that must be considered is the Zener diode in the opencircuit branch, D_z . When a reverse current open-circuit fault occurs, the current through the load flows through the open-circuit branch, meaning the load current flows through the Zener diode. Therefore, the Zener diode must be able to handle a pulse current equal to the rated current of the load. In addition to the current flowing through the load, the Zener diode must absorb the energy stored in the load. If the load is inductive, the Zener diode must be able to handle an energy of

$$E_Z = \frac{1}{2}L \cdot (I_{max})^2 \tag{11}$$

where L is the inductance of the load, and I_{max} is the maximum instantaneous current flowing through the load.

The fifth component that must be considered is the standard diode in the opencircuit branch, D_{open} . This diode must be sized to handle the voltage of the power device when it is turned off. Like the Zener diode, the diode in the open-circuit branch must also handle a pulse current equal to the rated current of the load.

The previous analysis showcases all the design considerations necessary when implementing the new open-circuit fault protection and detection circuitry. Table II.I concisely summarizes these.

Component	Design Considerations Beyond Traditional Desaturation Protection
R _{CHG}	• Power rating needs to be reconsidered since the voltage across the resistor can be greater than before, due to a negative drain-to-source voltage caused by the open-circuit branch
Dsense	• Special attention must be given to the maximum current flowing through the diode since it is larger than before, due to the possible negative drain-to-source voltage
CBLK	 Power rating needs to be reconsidered since the voltage across the capacitor can be greater than before, due to a negative drain-to-source voltage caused by the open-circuit branch Must be able to handle voltage overshoots
D_z	 Must be able to handle a pulse current equal to the rated current of the load Must be able to absorb the energy stored in the load
Dopen	 Must be sized to handle the voltage of the power device when it is turned off Must be able to handle a pulse current equal to the rated current of the load

Table II.I: Summary of additional design considerations

CHAPTER THREE

SIMULATION VERIFICATION

The reverse current open-circuit fault protection and detection scheme has been outlined and detailed. Before building it in an experimental setup, however, it is important to demonstrate its effectiveness in a simulation. Hence, this chapter focuses on the simulation verification of the new protection and detection circuitry.

Given a desired reverse current open-circuit fault detection speed, each component of the new scheme can be determined using (1)-(11). Afterward, the novel circuit architecture shown in Figure 1.1 can be added to any power device gate drive.

Showcasing the effectiveness of the reverse current open-circuit fault protection and detection scheme in every inverter topology is not feasible. Therefore, a case study utilizing the new circuitry is conducted. Two SiC MOSFETs are placed in a single-phase inverter topology (like that shown in Figure 2.1). A reverse current open-circuit detection speed of ~2.5 μ s is targeted. The DC bus voltage of the circuit is 800 V, and an inductive load current of 20 A enters the middle node of the circuit. Using (1)-(11), the values of the various components in Figure 1.1 are calculated. These values are listed in Table III.I, and the system is simulated using Synopsys/Saber with detailed device models. Stray resistance and inductance are added to account for the parasitic ones in practice. It is crucial to show that the new reverse current open-circuit fault protection and detection circuitry successfully protects against and detects short-circuit faults, forward current open-circuit faults, and reverse current open-circuit faults.

Component	Value
R _{CHG}	240 Ω
C _{BLK}	6 nF
R_n	240 Ω
VCSTH+	11.15 V
VCSTH-	-8 V
Vz,b	10 V

Table III.I: Simulation component values

While there is a given topology with specific values for each component used in this case study, it is again important to note that the proposed solution is universal in its nature. This is due to its device-level protection and detection design.

Short-Circuit Fault

To illustrate the effects of short-circuit faults, the upper power device is turned off, while the lower power device is turned on. This configuration results in no drain current through the upper power device and 800 V dropped across the upper power device. The short-circuit fault is introduced by turning the upper power device on at 100 µs. The effects of such an action are shown in Figure 3.1(a) and Figure 3.1(b) by the dotted orange lines labeled "NP," which stands for no protection. Figure 3.1(a) shows the drain current of the upper power device increase to above 200 A, even though the load has a rating of 20 A, causing increased drain-to-source voltage per power device I-V characteristics. This effect is shown in Figure 3.1(b), where it is seen that the drain-tosource voltage of the device increases to about 200 V. With such a large drain current and drain-to-source voltage, the power dissipated in the upper power device is unsustainable, and permanent damage is likely to occur.



Figure 3.1: Effect of short-circuit fault with and without new protection and detection scheme on (a) drain current, (b) drain-to-source voltage, (c) voltage across the blanking capacitor, and (d) fault signal

As stated before, short-circuit faults are protected through the desaturation protection scheme. While desaturation protection has previously been proven successful at detecting short-circuit faults, the proof is given here to show that the proposed integrated solution is also successful at detecting short-circuit faults.

The same fault that is used to create the "NP" signals of Figure 3.1(a) and Figure 3.1(b) is once again produced to create the "P" signals, which stands for protection, of Figure 3.1(a)-(d). The only difference is that the newly proposed scheme shown in Figure 1.1 is now implemented into the gate drive of the upper power device.

Before the fault occurs, the upper power device's drain current and drain-tosource voltage are equivalent to their corresponding "NP" signals. Since the upper power device is off at time zero, the voltage across the blanking capacitor charges to the gate-tosource voltage, which is -5 V. Since no fault has occurred, the fault signal is 0 V.

When the fault occurs at 100 μ s, the drain current and drain-to-source voltage initially follow the same pattern as their corresponding "NP" signals. The drain current of the power device reaches just over 200 A in less than 1 μ s. Since the upper power device is turned on, the voltage across the blanking capacitor begins to follow the drain-tosource voltage. After 1.736 μ s, the voltage across the blanking capacitor reaches the positive threshold voltage of 11.15 V, and the fault flag is triggered. The upper power device is turned off at this instant, and the drain current quickly and smoothly falls to 0 A. Such a smooth transition when the gate is turned off does not occur for the drain-tosource voltage. A transient spike takes the drain-to-source voltage just over 1 kV. Following this transient, the drain-to-source voltage experiences some parasitic ringing

and approaches its steady-state value of 800 V. Despite this transient behavior of the drain-to-source voltage, the voltage across the blanking capacitor remains smooth due to the noise immunity portion of the new circuitry. As evident by this test, the new protection and detection scheme successfully detects and protects against short-circuit faults, and in this case, does both in 1.736 µs.

Forward Current Open-Circuit Fault

To illustrate the effects of a forward current open-circuit fault, the upper power device is turned on while the lower power device is turned off. For this test only, the load of the system is placed across the lower power device, meaning the load current is flowing out of the middle node and from the drain to the source of the upper power device. At 100 μ s, an open circuit is introduced in the upper power device, emulating a forward current open-circuit fault.

The results of this test without the new protection and detection scheme are shown by the "NP" signals in Figure 3.2(a) and Figure 3.2(b). Initially, the drain current is the same as the load current, and the drain-to-source voltage is approximately 0 V. When the fault occurs, the drain current of the upper power device decreases almost instantly to 0 A. However, the drain-to-source voltage of the upper power device spikes to around 1.2 kV and then steadies to the DC bus voltage of 800 V.

While the drain-to-source voltage increases during a forward current open-circuit fault, it is not nearly as detrimental to the system as a short-circuit fault or a reverse current open-circuit fault. This is because the load current flows through the freewheeling diode of the lower power device.



Figure 3.2: Effect of forward current open-circuit fault with and without new protection and detection scheme on (a) drain current, (b) drain-to-source voltage, (c) voltage across the blanking capacitor, and (d) fault signal

However, a control issue arises since the gate of the upper power device is still turned on. This could be a significant problem if the current direction were to switch (like in inverter applications), and the forward current open-circuit fault turned into a reverse current open-circuit fault. Therefore, it is still essential to be able to detect such a fault. The protection scheme shown in Figure 1.1 can perform forward current open-circuit fault detection.

Running the same test as before but including the new protection and detection scheme in the gate drive of the upper power device results in the "P" signals shown in Figure 3.2(a)-(d). Before the fault occurs, it is seen that the initial drain current through the upper power device is approximately 20 A. There is a minute difference between the drain current of the "P" signal and the drain current of the "NP" signal. This difference is due to the load that is used in the simulation. For the "NP" signal, a current source with 20 A is used, whereas for the "P" signal, a non-ideal inductor with an initial current of 20 A is used. The non-ideal inductor is chosen for the test including the new protection and detection scheme to replicate a real-world environment more accurately. Despite this subtle difference, there should not be any difference in the capability of fault protection and detection. The initial drain-to-source voltage of the upper power device is 1-2 V because of a small amount of internal device resistance, and the initial voltage across the blanking capacitor is the sum of the drain-to-source voltage and the forward voltage of the sensing diode, which is around 2.5 V.

When the fault occurs at 100 μ s, the drain current goes to 0 A as expected. Since the load current flows through the freewheeling diode of the lower power device, the

drain-to-source voltage behaves just as it did without the protection and detection scheme in place—an initial spike in the drain-to-source voltage is observed due to the di/dt of the stray inductances in the circuit, and in steady-state, the upper power device blocks the DC bus voltage of 800 V.

Since the upper power device is turned on, the voltage across the blanking capacitor begins to follow the drain-to-source voltage. After 0.955 μ s, the voltage across the blanking capacitor reaches the positive threshold voltage of 11.15 V, and the fault flag is triggered. At this point, the upper power device is turned off, and the voltage across the blanking capacitor smoothly decreases to -5 V. As evident by this test, the new protection and detection scheme successfully detects and protects against forward current open-circuit faults, and in this case, does both in 0.955 μ s.

Note that the time of fault detection in this case is less than the time of detection in the short-circuit case. This is because the distance between 2.5 V and 11.15 V is less than the distance between -5 V and 11.15 V, so the voltage across the blanking capacitor reaches the positive threshold voltage faster in a forward current open-circuit fault than it does in a short-circuit fault.

Reverse Current Open-Circuit Fault

As mentioned in Chapter 2, reverse current open-circuit faults can occur when reverse current flows through the power device's freewheeling diode or when reverse current flows primarily through the inversion channel of the power device. If the power device is turned off, the reverse current flows through the power device's freewheeling diode. If the power device is turned on, the reverse current is primarily flowing through

the inversion channel of the power device. To highlight the full capability of the new protection and detection scheme, its effectiveness under both types of reverse current open-circuit faults is considered.

Freewheeling Diode

To illustrate the effects of a reverse current open-circuit fault of the freewheeling diode, the upper power device is turned off, and the lower power device is turned off. As with the short-circuit test, the load is placed across the upper power device, and hence, the load current enters the middle node. Therefore, the load current is flowing through the freewheeling diode of the upper power device. At 100 μ s, an open circuit is introduced in the upper power device, emulating a reverse current open-circuit fault.

The results of this test without the new protection and detection scheme are shown by the "NP" signals in Figure 3.3(a) and Figure 3.3(b). Initially, the drain current of the upper power device is -20 A, indicating the load current is flowing in the reverse direction through the power device (the freewheeling diode of the power device in this case). Furthermore, the drain-to-source voltage of the power device is around -4 V due to the voltage drop across the freewheeling diode. When the open-circuit fault occurs, the drain current of the upper power device decreases to zero as expected. The drain-tosource voltage of the power device plummets to drastically low numbers (around -10 MV in a matter of nanoseconds in this case study). Such high voltage will damage the system if maintained for any time.



Figure 3.3: Effect of reverse current open-circuit fault in freewheeling diode with and without new protection and detection scheme on (a) drain current, (b) drain-to-source voltage, (c) voltage across the blanking capacitor, and (d) fault signal

The severity of this type of fault should not be understated. Combining the preexisting desaturation protection, the open-circuit branch consisting of a diode and a Zener diode in anti-series, the noise immunity branch, and the negative voltage comparator allows this type of reverse current open-circuit fault to be protected and detected.

Running the same test as before but including the new protection and detection scheme in the gate drive of the upper power device results in the "P" signals shown in Figure 3.3(a)-(d). Before the fault occurs, the drain current and drain-to-source voltage are identical to their corresponding "NP" signals. The initial voltage across the blanking capacitor smoothly reaches the drain-to-source voltage value, around -4 V.

When the fault occurs at 100 μ s, the drain current goes to 0 A as expected. However, the drain-to-source voltage is clamped to the breakdown voltage of the Zener diode plus the forward voltage of the anti-series diode within 10 ns. Therefore, the drainto-source voltage is clamped to around -10 V. As a result, the reverse current open-circuit fault is protected almost instantaneously. The voltage across the blanking capacitor follows a very similar trend to the drain-to-source voltage and smoothly approaches -10 V, following the RC characteristics of the circuit. After 1.562 μ s, the voltage across the blanking capacitor reaches the negative threshold voltage of -8 V, and the fault flag is triggered.

As evident by this test, the new protection and detection scheme successfully protects against and detects reverse current open-circuit faults of the freewheeling diode. The protection against reverse current open-circuit faults of the freewheeling diode is

immediate, and in this case, the detection of reverse current open-circuit faults of the freewheeling diode occurs in 1.562 µs.

Power Device Channel

To illustrate the effects of a reverse current open-circuit fault of the inversion channel of the power device, the upper power device is turned on, and the lower power device is turned off. The load is placed across the upper power device; hence, the load current enters the middle node. Therefore, the load current is primarily flowing through the inversion channel of the upper power device. At 100 μ s, an open circuit is introduced in the upper power device, emulating a reverse current open-circuit fault.

The results of this test without the new protection and detection scheme are shown by the "NP" signals in Figure 3.4(a) and Figure 3.4(b). Initially, the drain current of the upper power device is -20 A, indicating the load current is flowing in the reverse direction through the power device (primarily through the power device channel in this case). Furthermore, the drain-to-source voltage of the power device is around -1 V due to the small voltage drop across the device's channel. Note that this voltage is less than the voltage of the previous case when the current only flows through the freewheeling diode. When the open-circuit fault occurs, the drain current of the upper power device decreases to zero as expected. The drain-to-source voltage of the power device plummets to drastically low numbers (around -10 MV in a matter of nanoseconds in this case study). Such high voltage will damage the system if maintained for any time.



Figure 3.4: Effect of reverse current open-circuit fault in power device channel with and without new protection and detection scheme on (a) drain current, (b) drain-to-source voltage, (c) voltage across the blanking capacitor, and (d) fault signal

The severity of this type of fault is clearly on par with the severity of the reverse current open-circuit fault of the freewheeling diode. However, through the combination of the pre-existing desaturation protection, the open-circuit branch consisting of a diode and a Zener diode in anti-series, the noise immunity branch, and the negative voltage comparator, this type of reverse current open-circuit fault can be protected and detected.

Running the same test as before but including the new protection and detection scheme in the gate drive of the upper power device results in the "P" signals shown in Figure 3.4(a)-(d). Before the fault occurs, the drain current and drain-to-source voltage are identical to their corresponding "NP" signals. The initial voltage across the blanking capacitor smoothly reaches the drain-to-source voltage value, around -1 V.

When the fault occurs at 100 μ s, the drain current goes to 0 A as expected. However, the drain-to-source voltage is clamped to the breakdown voltage of the Zener diode plus the forward voltage of the anti-series diode within 10 ns. Therefore, the drainto-source voltage is clamped to around -10 V. As a result, the reverse current open-circuit fault is protected almost instantaneously. The voltage across the blanking capacitor follows a very similar trend to the drain-to-source voltage and smoothly approaches -10 V, following the RC characteristics of the circuit. After 2.403 μ s, the voltage across the blanking capacitor reaches the negative threshold voltage of -8 V, and the fault flag is triggered. While not shown in any waveform, the upper power device is consequently turned off to prevent any control issues from arising in the future.

As evident by this test, the new protection and detection scheme successfully protects against and detects reverse current open-circuit faults of the device channel. The

protection against reverse current open-circuit faults of the device channel is immediate, and in this case, the detection of reverse current open-circuit faults of the device channel occurs in $2.403 \ \mu s$.

Note that the time of fault detection in this case is more than the time of detection in the case of the freewheeling diode. This is because the distance between -1 V and -8 V is more than the distance between -4 V and -8 V, so the voltage across the blanking capacitor reaches the negative threshold voltage faster in a reverse current open-circuit fault of the freewheeling diode than it does in a reverse current open-circuit fault of the device channel.

CHAPTER FOUR

EXPERIMENTAL VALIDATION

The newly proposed protection and detection scheme shown in Figure 1.1 is thoroughly described in Chapter 2. Furthermore, Chapter 3 shows that the scheme effectively protects against and detects the most common types of faults: short-circuit faults and open-circuit faults (both in the forward and reverse current scenarios). This is done through extensive simulation verification. The last step necessary to confirm the successful design of the protection and detection scheme is to demonstrate its effectiveness in a real-world environment. Hence, this chapter focuses on the experimental validation of the protection and detection circuitry shown in Figure 1.1. Since the standard desaturation protection scheme protects against and detects shortcircuit and forward current open-circuit faults, the following setup is designed only to test reverse current open-circuit faults.

Experimental Setup

The newly proposed design is not overly complex—it only consists of five more components than what already exists on a standard gate drive. However, much thought must go into the surrounding circuitry required to test the design in a two-level, singlephase circuit. This section highlights the three printed circuit boards (PCBs) used to test the new design. They are the power stage board, the open-circuit fault generation board, and the gate drive board. Then, the auxiliary equipment required for experimentation is mentioned. Finally, all experimental components are connected, and the combined circuitry, testing process, control signals, and component selection are explained. While



Figure 4.1: Power stage board

not the focus of this study, the experiment cannot be conducted without a proper understanding of the entire experimental setup.

Power Stage Board

The power stage board is the foundational board on which the other two boards are built. It is required to take a DC voltage input and produce an AC voltage output. Generally, it includes DC-link capacitors, decoupling capacitors, power devices, and loads [20]. The power stage board also included the sensing diode (D_{sense}) and the opencircuit fault detection branch (D_z and D_{open}) in this study. A picture of the power stage is shown in Figure 4.1.

Open-Circuit Fault Generation Board

To showcase the effectiveness of the new protection and detection scheme, a reverse current open-circuit fault must be created. There are a variety of ways in which this can be achieved. One such way is using an open-circuit fault generation (OCFG)



Figure 4.2: Open-circuit fault generation board

board. This board allows for a controlled way to open a switch. The switch used in this application is an IGBT without a corresponding freewheeling diode. Hence, when it is opened, there is no alternative path where current can flow, emulating an actual opencircuit fault. A picture of the OCFG board is shown in Figure 4.2.

Gate Drive Board

In its most basic form, the gate drive board is responsible for providing significant power to turn on and off the circuit's upper and lower power devices. More explicitly, it also contains signal isolators to allow galvanic isolation between the control and power loop; isolated power supplies to power the signal isolators, gate driver IC, and buffer; and protective circuitry, e.g., desaturation protection [21]. Therefore, the blanking capacitor, noise immunity diode, noise immunity resistor, charging resistor, and bipolar comparators are all contained on the gate drive board. In this experimental setup, two



Figure 4.3: Gate drive board

gate drive boards are required: one for the upper power device and one for the lower power device. A picture of one of these gate drive boards is shown in Figure 4.3.

Auxiliary Equipment

The auxiliary equipment required for the experiment includes the main power supply, computer interface, the auxiliary power supply, oscilloscope, function generator, inductive load, protective casing, and wires. The main power supply provides the DC voltage input of the power stage board, and the computer interface allows the user to control the main power supply. The auxiliary power supply powers the OCFG board and the gate drive boards. The oscilloscope, along with differential voltage probes and current sensors, are responsible for accurately measuring the necessary electrical signals of the circuit. The function generator produces the control signals sent to the OCFG board and gate drive boards. The inductive load is a house-made toroidal core inductor connected to



Figure 4.4: Combined circuit

the AC side of the power stage board. The protective casing is used to prevent any human contact with the potentially high-voltage circuitry when it is running, and the wires are chosen to handle the required voltage and current based on their positions within the circuit.



Figure 4.5: Schematic of experimental setup

Combined Circuit

The combined circuit, including everything previously mentioned, is shown in Figure 4.4. The schematic equivalent of the circuit used for testing is shown in Figure 4.5.

In the previous analysis, the upper power device was the device under test. However, note that in Figure 4.5, the lower power device is the device under test. This means the reverse current flows through the lower power device when the open-circuit fault occurs rather than the upper power device. This decision is solely based on the fact that one terminal of the load, the device under test, and the gate drive are connected to the ground terminal in this setup, whereas if the upper power device is the device under test, that same terminal is floated. Theoretically, this should decrease the likelihood of permanently damaging the components in the circuit.

Testing Process

The entire experimental setup has been outlined. However, it is important to understand that testing must be done in stages in any real-world environment. This includes planning, conducting intermediate tests, predicting the outcome of those tests, and comparing that prediction with what is obtained experimentally. While all of these tests (including multiple iterations of debugging) are not given in detail in this section, it is important to acknowledge their inevitable existence.

Control Signals

The control signals sent to the upper and lower gate drive boards and the OCFG board are paramount to obtaining meaningful results. These control signals are programmed on a function generator and sent to their corresponding boards. They are necessary to produce (1) a controlled amount of reverse current and (2) the reverse current open-circuit fault.

Unfortunately, experimentally producing an initial current through an inductor is much more complex than computationally producing an initial current through an inductor. Therefore, special care must be taken to ensure that a controlled amount of

current flows through the inductor when an open-circuit fault occurs. The change in current through an inductor can be found by

$$\Delta I_L = \frac{V_L}{L} \cdot \Delta t \tag{12}$$

If the initial current flowing through the inductor is assumed to be 0 A, and the voltage across the inductor is V_{DC} , then (12) can be rewritten as

$$I_L = \frac{V_{DC}}{L} \cdot \Delta t \tag{13}$$

Therefore, by knowing the inductance of the inductor and the DC voltage, the current flowing through the inductor can be controlled by varying the amount of time the DC voltage is dropped across the inductor.

The timing of the reverse current open-circuit fault is directly controlled by the signal sent to the OCFG board. In normal operation, the signal should be 5 V, meaning the device is shorted. If a fault is desired, the signal should be 0 V, meaning the device is opened. The fault should only occur after the desired load current is established and the upper power device is turned off, meaning reverse current flows through the lower power device.

Two different sets of control signals are produced. The first set corresponds to normal operation and is shown in Figure 4.6. It is assumed that the lower power device is turned off. If the inductance of the load is 262 μ H, the DC bus voltage is 50 V, and the desired inductor current is 5 A, by using (13), the amount of time the upper power device



Figure 4.6: Desired no fault control signals including (a) upper power device gate-to-source voltage, (b) IGBT gate-to-emitter voltage, and (c) inductor current

must remain turned on is 26.2 μ s. Therefore, Figure 4.6(a) shows the gate-to-source voltage control signal of the upper power device increase from 0 V to 3.3 V at 20 μ s and stay at 3.3 V until 46.2 μ s. At this point, the upper power device is turned off. Figure 4.6(c) confirms that this process increases the inductor current from 0 A to 5 A. Since no fault is desired in normal operation, the gate-to-emitter voltage control signal is constantly 5 V.

The second set of control signals corresponds to introducing a reverse current open-circuit fault and is shown in Figure 4.7. It is assumed that the lower power device is turned off. If the inductance of the load is 262μ H, the DC bus voltage is 50 V, and the



Figure 4.7: Desired fault control signals including (a) upper power device gate-to-source voltage, (b) IGBT gate-to-emitter voltage, and (c) inductor current

desired inductor current is 5 A, by using (13), the amount of time the upper power device must remain turned on is 26.2 μ s. Therefore, Figure 4.7(a) shows the gate-to-source voltage control signal of the upper power device increase from 0 V to 3.3 V at 20 μ s and stay at 3.3 V until 46.2 μ s. At this point, the upper power device is turned off. Figure 4.7(c) shows that this process increases the inductor current from 0 A to 5 A. Everything described so far about this set of control signals is identical to the set of control signals for normal operation. However, since a fault is now desired, the gate-to-emitter voltage control signal must decrease from 5 V to 0 V to turn the IGBT of the OCFG board off. To allow adequate time to ensure the upper power device is turned off and the current flows through the lower power device in the reverse direction, the IGBT is turned off at 100 µs.

The prior information is given under the assumption that the lower power device is constantly off. This is important because the function generator unit used in this experiment can only produce two synchronized signals at a time. Since a signal for the upper power device is needed and a signal for the IGBT is needed, no channel of the function generator remains to control the lower power device. In addition, it is not easy to synchronize an additional function generator, which would require three synchronized signals. With this in mind, the lower power device can either constantly remain on or off. Since the upper power device must turn on to charge the inductor, if the lower power device is always on, a short-circuit fault will occur the moment the upper power device is turned on. Therefore, the lower power device must be turned off throughout all experimental testing. This is important because it means that the reverse current is flowing through the freewheeling diode of the lower power device when the reverse current open-circuit fault occurs, not the inversion channel of the power device. Fortunately, the difference between the results when the reverse current flows through the freewheeling diode of the power device and the results when the reverse current flows through the channel of the power device is only the time necessary to detect the reverse current open-circuit fault (see Figure 3.3 and Figure 3.4). Therefore, showcasing the capability to protect against and detect reverse current open-circuit faults of the freewheeling diode implies the capability to protect against and detect both types of reverse current open-circuit faults.

Component Selection

A comprehensive table including all parameter and component information for the critical pieces of the experiment is given in Table IV.I.

Parameter or Component	Value or Part Number
R _{CHG}	240 Ω, 1/8 W
C_{BLK}	6 nF, 25 V
R_n	240 Ω, 1/8 W
VCSTH+	11.19 V
VCSTH-	-7.90 V
$v_{z,b}$	9 V to 15 V
D_n	Schottky diode, BAT54HT1G
Dsense	3.3 kV, GAP3SLT33-214
D_z	200 A surge TVS, SMCJ9.0CA-13-F
Dopen	3.3 kV, GAP3SLT33-214
Comparators	LM211D
L	262 μH
V _{DC}	50 V
IL	5 A
IGBT	1200 V, 50 A, IGW25N120H3FKSA1
MOSFET	1200 V, 100 A, C3M0021120K

Table IV.I: Parameters and components for experimental setup

There are a couple of points of emphasis concerning the experimental design and how it compares to the simulation cases presented in Chapter 3. The first difference is the breakdown voltage of the Zener diode. After investigation, not many Zener diodes can handle a surge current above 1 A. Therefore, a transient voltage suppressor (TVS) is used, which can handle much larger surge currents (in this case, 200 A). Consequently, the breakdown voltage is a function of current and can vary anywhere from 9 V to 15 V. Despite this, choosing a negative threshold voltage of -7.90 V ensures that the fault flag will be triggered regardless of the specific breakdown voltage of the TVS. The second difference is the DC bus voltage and inductor current; these values are lower than those

used in the original simulation case study. While the experimental setup is designed to handle much higher voltages and currents than 50 V and 5 A, since creating a reverse current open-circuit fault is potentially hazardous, a lower value for voltage and current is chosen.



Figure 4.8: Simulated measurements of (a) upper power device gate-to-source voltage, (b) lower power device drain-to-source voltage, (c) IGBT gate-to-emitter voltage, (d) inductor current, (e) blanking capacitor voltage, and (f) fault signal voltage



Figure 4.9: Experimental measurements of (a) upper power device gate-to-source voltage, (b) lower power device drain-to-source voltage, (c) IGBT gate-to-emitter voltage, (d) inductor current, (e) blanking capacitor voltage, and (f) fault signal voltage

Results and Discussion

Since the parameters in Table IV.I vary from those used in the prior simulation, and the device under test is now the lower power device rather than the upper power device, it is recommended to rerun the simulation to ensure the best probability of success when running the experimental test. Doing this yields the waveforms shown in Figure 4.8.

The signals developed in the previous section used to control the upper power device and IGBT are replicated in the simulation. These signals produce current through the inductor and create the reverse current open-circuit fault. The newly proposed protection and detection scheme is implemented in the lower power device. At 100 μ s, the reverse current open-circuit fault occurs. Based on the drain-to-source voltage signal, the fault is protected almost instantaneously. The fault is subsequently detected in 0.51 μ s.

Since the simulation results look promising, the experiment is considered to have a better chance of working properly. All precautions are established, and the experimental test is conducted. The results of the experimental test are shown in Figure 4.9.

The signals developed in the previous section used to control the upper power device and IGBT are used in the experimental test. These signals produce current through the inductor and create the reverse current open-circuit fault. Due to these signals, the gate-to-source voltage of the upper power device is high (meaning the upper power device is on) from 20 μ s to 46.2 μ s, and the gate-to-emitter voltage of the IGBT is high (meaning the IGBT is on) from 20 μ s to 100 μ s. In response to the gate-to-source voltage

of the upper power device, the drain-to-source voltage of the lower power device increases from 0 V to 50 V at 20 μ s and decreases from 50 V back to 0 V at 46.2 μ s. Furthermore, the current flowing through the inductor ramps from 0 A to 5 A from 20 μ s to 46.2 μ s. It then slowly declines from 46.2 μ s to 100 μ s due to the inevitable dissipative elements in the circuit. At 100 μ s, the reverse current open-circuit fault occurs by turning the IGBT off through the OCFG circuitry. At this time, the drain-to-source voltage is clamped to the voltage across the open-circuit branch. Thus, the fault is protected almost instantaneously. The voltage across the blanking capacitor smoothly approaches this clamped voltage until the negative threshold voltage of -7.90 V is reached. This threshold is reached at 0.807 µs, and the fault signal is set high. Therefore, the fault is detected in 0.807 µs. During this period, the current through the inductor decreases even faster due to the greater resistance present in the open-circuit branch diode, D_{open} . At around 170 µs, the inductor current reaches 0 A, and the drain-to-source voltage of the lower power device goes to 0 V following some parasitic ringing. This ringing is at a frequency bypassed by the blanking capacitor, so the voltage across the blanking capacitor simply transitions to 0 V. While not shown here, this test is successfully repeated over ten times in succession. Therefore, the newly proposed protection and detection scheme is experimentally proven to protect against and detect reverse current open-circuit faults successfully.

The simulated and experimental results are compared in Figure 4.10. Most signals are nearly identical to one another. The on-state gate-to-source voltage of the upper power device is 20 V in simulation, whereas it is 15 V experimentally. The drain-to-

source voltage of the lower power device, the gate-to-emitter voltage of the IGBT, and the inductor current are extremely similar in both the simulation and experiment. The voltage across the blanking capacitor in the simulation is initially less than the voltage across the blanking capacitor found in the experiment. This is because a Zener diode is used in simulation, whereas a TVS is used in the experiment. Therefore, the voltage across the Zener diode, and consequently the voltage across the blanking capacitor, is more constant (around -10 V) in the simulation. In contrast, the voltage across the TVS, and consequently the voltage across the blanking capacitor in the experiment. However, the general smoothing effect on the blanking capacitor voltage is the same in both the simulation and the experiment due to the circuit's charging resistor and noise immunity section. The fault is detected faster in simulation $(0.51 \ \mu s)$ than it is experimentally $(0.807 \ \mu s)$, but it is protected instantaneously (within 10 ns) in both cases.



Figure 4.10: Simulated versus experimental measurements of (a) upper power device gate-to-source voltage, (b) lower power device drain-to-source voltage, (c) IGBT gate-to-emitter voltage, (d) inductor current, (e) blanking capacitor voltage, and (f) fault signal voltage

CHAPTER FIVE

CONCLUDING REMARKS

This document proposes a new method for protecting against and detecting all common types of faults in inverter circuitry: short-circuit faults, forward current opencircuit faults, and reverse current open-circuit faults. This is done by enhancing preexisting desaturation protection circuitry. The physics behind the need for the new protection and detection scheme is discussed, and practical design considerations necessary for the real-life implementation of the new scheme are given.

Simulation results show that the new protection and detection circuitry (1) protects against and detects short-circuit faults in as fast as 1.736 μ s, depending on the size of the charging resistor and blanking capacitor; (2) protects against and detects forward current open-circuit faults in 0.955 μ s, depending on the size of the charging resistor and blanking capacitor; and (3) protects against reverse current open-circuit faults within 10 ns, while detecting reverse current open-circuit faults of the freewheeling diode in 1.562 μ s and detecting reverse current open-circuit faults of the power device channel in 2.403 μ s, both times depending on the size of the noise immunity resistor, charging resistor, and blanking capacitor. Experimental results confirm what is found in the simulation. Reverse current open-circuit faults of the freewheeling diode are shown to be protected in a few nanoseconds while being detected in 0.807 μ s.

In addition to the fast protection and detection speeds the new scheme produces, it is also cost-efficient due to a complete lack of sensors—only cheaper, easier to obtain components are required. Further, it is universal due to its power device level

implementation. Theoretically, it can be embedded in any inverter circuitry. In the future, various types of power devices and topologies can be experimentally tested to demonstrate the universal nature of the newly proposed fault protection and detection scheme.

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