



# Development of a CMOS A/D Converter for an Artificial Synapse

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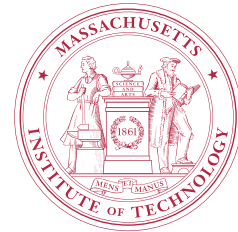


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## Abstract

This thesis deals with background, theory, design, layout and experimental test results of an analogue CMOS VLSI current-mode analog-to-digital converter. This system supports a project, whose goal it is to build a biologically relevant model of synaptic plasticity, named the *Artificial Synapse*. A critical part of the design, which is based on analogue CMOS VLSI circuits, is the ability to activate a discrete number of channels by sampling an analogue signal. Since currents are the signal of interest and transistors are biased in weak inversion (subthreshold regime), the system requires a current mode A/D circuit that it can operate at ultra-low power and current levels. To meet this need, two new innovative A/D converter approaches are proposed to replace the system's previous A/D converter design which suffered from a non-linear resolution, uncoded output code and heavy bit oscillations.

The initial technical requirements and key criteria for the new converter comprise a resolution of one nano ampere, an input current range between 0 – 100nA, conversion frequencies of up to 5kHz, and a power supply voltage of less than 1.5V. Temperature range, space occupation and power dissipation aspects were not specified due to the early stage of the related *Artificial Synapse* project.

The novel converters both produce seven bit thermometer codes, their functional principle can be best described as current mode flash analog-to-digital converters (ADCs). Due to the fact that the input signal is in the area of a subthreshold current, it is self-evident that the A/D converter design should operate at a subthreshold realm. To support low power operation, clocks or high currents could not be used and were excluded from the design from the very start. To encode the thermometer code into standard binary code, a seven-to-three encoder was designed and integrated on the chip.

In October 2003, the design was submitted for production to the MOSIS circuit fabrication service. The *AMI Semiconductor 1.5 micron ABN CMOS* process was chosen to manufacture the chip. When it was returned in January 2004, simulation results showed that both new A/D converter approaches accomplished excellent results which were expected from SPICE simulation results. With the new chip installed, it became possible to resolve input currents as small as one nano ampere and achieve conversion frequencies of up to 5kHz. The circuits also both meet the requirements which were set at the beginning of the project to operate at a power supply voltage of less than 1.5V, processing input currents in the range between 0 – 100nA.

A prototype printed circuit board (PCB) was developed, produced and employed for experiments with the chip. The major application of this test-bed is the ability to generate and measure extremely low currents with high precision. This enables the monitoring of the very small currents that are processed by the chip.

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## List of Abbreviations

A/D	analog-to-digital
AC	alternating current
ADC	analog-to-digital converter
AMPA	alpha-amino-3-hydroxy-5-methyl-4-isoxazole propionic acid
ASIC	application specific integrated circuit
BER	bit error rate
CAD	computer aided design
CMOS	complementary metal oxide semiconductor
D/A	digital-to-analog
DAB	digital audio broadcasting
DAC	digital-to-analog converter
DC	direct current
DNL	differential nonlinearity
DRC	design rule check
DSP	digital signal processing
DVB	digital video broadcasting
e.g.	exempli gratia
etc	etcetera
FPGA	field programmable gate array
FSR	full scale range
HST	Harvard-MIT Division of Health Sciences & Technology
I/O	input/output
IC	integrated circuit
INL	integral non-linearity
KV	Karnaugh Veitch
LSB	least significant bit
LSI	large scale integration
LVS	layout versus schematic
MIT	Massachusetts Institute of Technology
MOS	metal oxide semiconductor
MOSFET	Metal oxide semiconductor field emission transistor
MUX	multiplexer
PCB	printed circuit board
PGA	programmable gate array
PSRR	power supply rejection ratio
S/N	signal-to-noise
SIC	silicon integrated circuits
SPICE	simulation program with integrated circuit emphasis
UID	unique identification (number)
VLSI	very large scale integration
VS	versus
XOR	exclusive or

# 1 Introduction

## 1.1

### Aims and Motivation

Analog circuits have a reputation for being complex, hard to handle and error-prone. However, their ability to interface with the real world using continuous time and amplitude signals makes them indispensable. There are several reasons why it is interesting to develop integrated circuits which exploit the possibilities of analog integrated circuit design. One of them is the modeling of biologically inspired circuits. A side glance into biology reveals that Mother Nature exclusively employs signals in information processing networks that all have in common that they are continuous in time and amplitude. Hence, it is suggested as the most appropriate signal when trying to model biologically inspired circuits. Another aspect of these circuits is power dissipation. Living nerve cells use voltages in the order of millivolts to communicate with each other, in contrast electronic circuits use voltages as big as several volts to form a signal. Operating voltages smaller than one volt can only be achieved when the transistors are biased in the weak inversion regime.

This led to the idea to develop analog circuits which are weak inversion biased, low-voltage, low-power, and current mode. This thesis has the goal to develop an analog-to-digital converter using the design techniques mentioned. It proposes a novel approach which has not been tested previously.

## 1.2

### Previous Work

This Diploma Degree thesis supports the doctoral thesis of G. Rachmuth, whom is developing a biologically inspired *Artificial Synapse* (or *Silicone Synapse*) which models synaptic plasticity using CMOS VLSI technology. As part of the *Artificial Synapse*, an analog-to-digital converter has been developed and implemented. This converter, which represents a crucial part of the system, initially displayed erroneous behavior and delivered inaccurate results. This current diploma degree thesis discusses optimizing the previous design, leading to a completely new approach to the problem.

## 1.3

### Problem Statement

The core problem can be outlined as follows: In a biologically inspired system, relying on circuit design rules such as low-power and low-voltage operation, clocks and high currents can not be used. The system we are dealing with is based on current mode operation using transistors which are biased in weak inversion. Consequently, the analog-to-digital (A/D) conversion circuit which will be included into the system should ideally use the same kind of technology which is already being used. Although there are hundreds of different A/D converter designs available using all sorts of different operating principles,



there is no converter underlying them which entirely fulfills the requirements. Therefore, a new integrated circuit design is required which integrates into in the rest of the system.

To address the main requirements, the analog-to-digital converter has to:

- Operate at a subthreshold regime
- Use current-mode technique to represent information
- Be an analog circuit (discrete time and amplitude)
- Function with a power supply voltage of less than 1.5V
- Occupy only a small area on the die
- Offer adequate conversion rates
- Be integrable in a standard 1.5 $\mu$ m CMOS process
- Be capable of resolving current differences of 1nA
- Have a linear conversion characteristic
- Be tolerant towards production tolerances

At the same time, it should not:

- Be susceptible to any kind of noise
- Be dependent on exact matched devices
- Rely on exact external voltage or current references

## 1.4

### Thesis Outline

The thesis is structured in eleven main chapters. Starting with an introduction into the topic, the first chapter explains the reasons why this thesis was written. A problem statement summarizes the main areas of importance behind the research.

In chapter two, the theoretical background information is presented. Beginning with a closer look on the properties of analog circuits and CMOS technology, circuit design techniques are discussed and explained. This is followed by a description of the different transistor operation regions and peculiarities of current mode operation, including a closer look at current mirrors. Different established A/D conversion techniques are presented in the last sections of chapter two and a quick insight is given on how noise affects sub-threshold circuit operation. Finally, examples of different A/D converters are presented together with information on how to specify these converters scientifically.

Chapter three introduces the previous A/D converter design, which already existed before the beginning of this project as a first approach to the problem. Firstly the original design, on which the previous design is based, is presented. Subsequently, modifications on that design are described leading to the previous converter. Later in the chapter, experiments and results are discussed which were carried out with the previous design, pinpointing on the problems which arose in that context.

Chapter four reveals the first attempt to find a better solution for the given problem. After the principle of operation and the test setup are explained, a series of experimental results is presented. Starting with an analysis of the precision of the internal multiplier used in that circuit, a couple of direct current (DC) and dynamic tests are performed. Their results are compared, analyzed and visualized afterwards.

Chapter five is based on a current division A/D converter, in contrast to the current multiplication converter. However, they both require the same test procedures to measure their performance.

Chapter six explains the seven-to-three encoder as the third circuit which is part of this thesis. It encodes the seven bit thermometer code which is produced by the two A/D converters into three bit binary code. Experimental results and a performance analysis summarize the findings.

Chapter seven deals with layout techniques and verification methods for the whole chip design. Verification methods are explained and the layout of the die is shown.

Chapter eight focuses on the prototype test bed which holds the chip. The external current generation and measurement circuits are shown and explained along with the parts and components which have been included on the printed circuit board. Various schematics illustrate the circuits which have been realized.

Chapter nine summarizes the work and gives an overview of future areas of research. The thesis is completed by chapter ten holding the appendix section of the work and chapter eleven, which is reserved for the bibliography.

## 2 Background

### 2.1

#### 2.1 Analog CMOS VLSI

In the past, numerous people predicted there soon would be little need for analog circuitry. They said the world would only rely on digital circuits. This was about twenty five years ago, and indeed many applications have replaced most analog circuitry with their digital counterparts, e.g. digital video broadcasting (DVB), digital audio broadcasting (DAB), digital music, and so on. Since the level of integration in integrated circuit technology increased to a very high level, the development of digital components became more desirable because of its robustness and simplicity in design. It was also discovered that most analog functions can be done at least as well and often considerably better using digital techniques.

##### 2.1.1

#### 2.1.1 Analog Circuits

In spite of the benefits from using digital circuits, there are disadvantages, too. One of the main disadvantages is that they require more components, and therefore critically were more expensive. Of course, this doesn't matter any more since rapid developments in silicon technology changed this. But the need for good analog circuitry remains strong. One of the reasons for this is the fact that most VLSI (very large scale integration) systems require analog circuits or systems such as analog-digital (A/D) and digital-analog (D/A) converters, voltage comparators, and so on. This is not very surprising if you consider that the real world is analog. All digital implementations of complex integrated circuits can currently only be found in certain types of applications. Microprocessors and digital memory are two examples of this class of circuits. But even these circuits most often contain various types of analog circuits. To give a number, one could say a typical applications specific integrated circuit (ASIC) might contain about 15% analog circuitry and 85% digital ones.

As already mentioned, integrated circuits are becoming larger and larger due to increasing system integration. This makes it more likely that at least some portion of modern integrated circuits will include analog circuitry which is required to interface to the real world. Surprisingly, this analog circuitry is often the limiting factor for the overall system performance and the biggest challenge for the circuit designer when creating a working IC. On the other hand, the rapidly decreasing costs and the increasing complexity of digital integrated circuits have made it possible for digital technology to displace analog circuitry in an ever increasing number of application areas.

One other reason why designers in most cases prefer digital over an analog circuit is quite simple; to most of them, designing and testing analog circuits often appears to be a "mystical art". This section intends to explain the theoretical background underlying the research in this thesis. Of course, digital design will always be much more systematic than analog design. But this doesn't does not mean that analog designs are any less important.

### 2.1.2

#### CMOS Technology

The desirability of a close relationship between analog functions and digital circuits provides a strong impetus towards the use of a VLSI technology in which analog and digital circuit functions may be realized compatibly on the same chip. Since it is well established that CMOS technology is the desirable basis for the most complex LSI (Large Scale Integration) digital circuits, traditional bipolar transistor integrated circuit and hybrid circuit approaches are not appropriate. Circuit design solutions which employ CMOS technology are sought<sup>1</sup>.

Opportunities for the development of CMOS analog circuits come from the capabilities of the CMOS technology itself. The high density of circuit elements makes it possible to implement complex functions, analog as well as digital, in modest chip areas. For example, a CMOS operational amplifier requires only  $\frac{1}{2}$  to  $\frac{1}{3}$  the die area of an operational amplifier in bipolar transistor technology. Also important is the capability to store and non-destructively sense signals on capacitors<sup>1</sup>.

This insight has increased the interest in MOS (Metal Oxide Semiconductor) and later in CMOS (Complementary Metal Oxide Semiconductor) technology. Common VLSI application areas are industrial or consumer products, automotive and military. Here, interface problems have to be solved with the use of microprocessors as well as DSP's (Digital Signal Processors). A really well suited example for this is comfort and safety in modern cars. More examples for application areas with advantageous usage of CMOS technology are ADC's and DAC's, audio, video and speech processing and synthesis.

Also, the rapid increase of integration density has opened a new perspective for developing *silicon neural systems*. After many years of study, scientists have become confident that the powerful organizing principles found in the nervous system can be realized in SIC (Silicon Integrated Circuits). Integrated-circuit fabrication has evolved to the point where small, but identifiable, parts of the nervous system can be emulated on a single piece of silicon. Using CMOS technology, nervous systems such as See-Hear, optical motion sensor, silicon retina and electronic cochlea etc. have been realized<sup>2</sup>. Systems of this type scale gracefully to the extremely large complexity that only CMOS technology is capable of offering today.

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<sup>1</sup> P. R. Gray, D. A. Hodges, and R. W. Broderson, editors. *Analog MOS Integrated Circuits*. IEEE Press, New York, 1 edition, 1980.

<sup>2</sup> C. Mead. *Analog VLSI and Neural Systems*. Addison-Wesley Publishing Co., Reading, Mass., 1 edition, 1989.

### 2.1.3

#### Analog Integrated Circuit Design

The objective of analog circuit design is to transform specifications into circuits that satisfy those specifications. It is a challenging activity because the problem has many variables and many decisions must be made to achieve a successful design<sup>3</sup>.

Depending on the designer's individual experience and background, different designers are using different techniques to implement the same set of specifications. Today, computer verification is the most commonly used tool to verify a design before it is manufactured on silicon. It is very important to make sure that everything possible is checked before a design is submitted. The whole process of design, layout and production of an analog chip takes many months and has the character of a 'single shot'; if a mistake is not discovered before the chip is sent in, the whole development process will be delayed for months.

#### 2.1.3.1

##### Analog vs. Digital Design

It is important to compare analog and digital design to understand the implications of the present status of analog integrated circuit design. Table 1 compares analog and digital design. The information found in Table 1 suggests that digital design is easier and cheaper than analog design. This is confirmed by the fact that sophisticated computer aided design (CAD) tools exist for digital circuits which permit the design at the systems level. This allows the use of integrated circuit technology by systems engineers and leads to a cycle/success ratio of near unity. In contrast, complex analog integrated circuits require experienced circuit designers and have a cycle/success ratio that is between two and three.

**Table 1:** Comparison analog and digital design.

Characteristics	Analog Design	Digital Design
Signal Amplitude	Continuum of values for amplitude (and time)	Two amplitude states
Design Methodology	Customized	Standardized
Component Values	Continuum of values	Components with fixed values
Model Requirements	Requires precise modeling capability	Only requires a precise large signal model
Programmability	Hard to change after design	Easily programmable by software
Design Level	Designed at the circuit level	Designed at the systems level
Use of CAD Tools	Difficult to use with CAD tools	Amenable to CAD tools

Why have analog circuits continued to find use in large and very-large integrated circuits? The answer is found in the economic viewpoint. Many considerations make up the economic viewpoint. Technical considerations include such aspects as design time, probability of success, performance, and area. In general analog integrated circuits require more design time and have a smaller probability of success compared with digital integrated circuits. Analog circuits are only competitive with digital circuits in performance and area. Even if digital circuits could always outperform analog circuits with smaller or

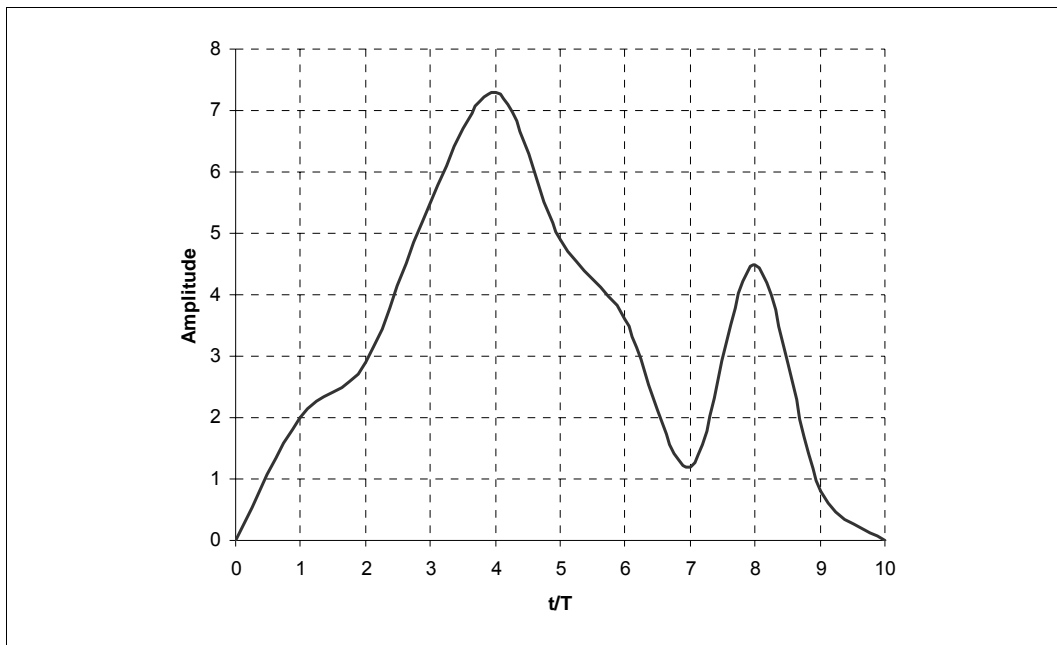
<sup>3</sup> P. E. Allen, D.R. Holberg. *CMOS Analog Circuit Design*. Oxford University Press Inc., Oxford, 1 edition, 1987.

equivalent area, analog circuits would still be required. This is because the source and final destination of information is often in analog form<sup>4</sup>.

### 2.1.3.2

#### **Definition of Analog and Digital Signals**

Integrated-circuit design is separated into two major categories: analog and digital. To characterize these two design methods, we must first define analog and digital signals. A *signal* will be considered to be any detectable value of voltage, current or charge. A signal should convey information about the state or behavior of a physical system. An *analog signal* is a signal that is defined over a continuous range of time and a continuous range of amplitudes. Figure 1 illustrates an analog signal. A *digital signal* is a signal that is defined only at discrete values of time and amplitude. Typically, the digital signal is a binary weighted sum of signals having only two defined values of amplitude as illustrated in Figure 2 and shown in Equation 1.

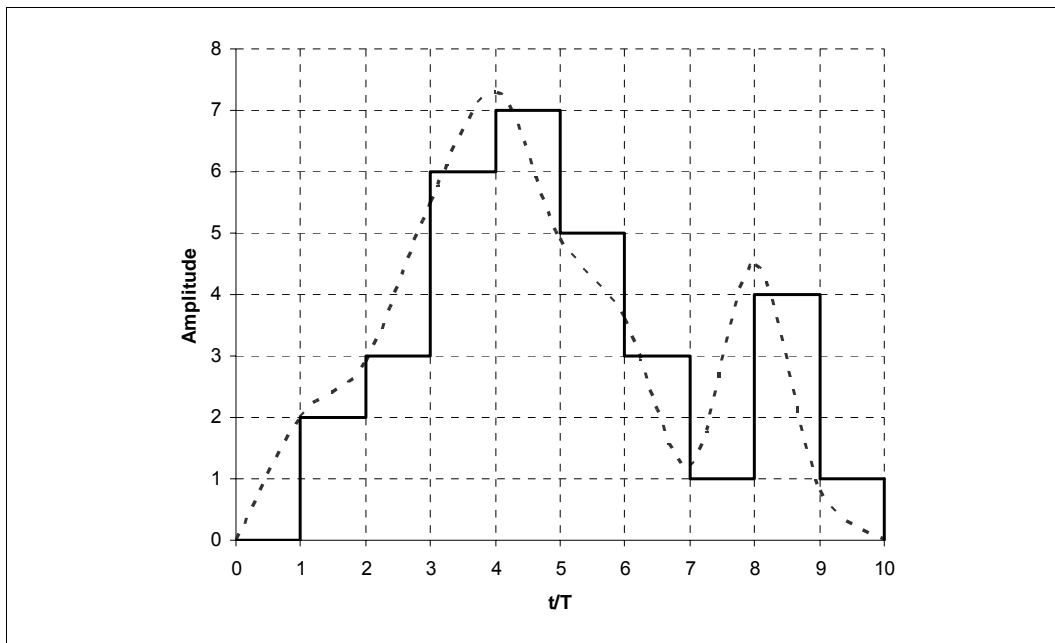


**Figure 1:** Analog and continuous time signal. T is the period of the signal or sampled signals.

$$D = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_N 2^{-N} = \sum_{i=1}^N b_i 2^{-i}$$

**Equation 1:** Digital signal as a binary weighted sum of signals, having only two defined values of amplitude.

<sup>4</sup> C. Ioumazou, F. J. Lidgley & D. G. Haigh. *Analogue IC design: the current-mode approach*. In: Chapter 18 by P. E. Allen. *Future of Integrated Circuit Design*. Peter Peregrinus Ltd., London, United Kingdom, 1 edition. 1990.



**Figure 2:** Digital signal.  $T$  is the period of the digital or sampled signals.

The individual binary numbers,  $b_i$ , have a value of either zero or one. Consequently, it is possible to implement digital circuits using only two defined states. This leads to a great deal of regularity and to an algebra that can be used to describe the function of the circuit. As a result, digital circuit designers have been able to adapt readily to the design of more complex integrated circuits<sup>3</sup>.

### 2.1.3.3

#### *Differences between Discrete and Integrated Design*

The differences between integrated and discrete analog circuit design are important. Discrete circuits use active and passive components that are not on the same substrate, whereas all of the components of an integrated circuit are on the same substrate. The most obvious difference between the two design methods is that geometry of the active devices and passive components in integrated circuit design are under the control of the designer. This gives the designer an entirely new degree of freedom in the design process. A second difference is that it is not feasible to breadboard the integrated-circuit design. Consequently, the designer must turn to simulation methods to confirm the design's performance. Computer simulation techniques have been developed that have several advantages, provided models are adequate. These advantages included the ability to monitor signals at any point in the circuit, the ability to open a feedback loop, the ability to easily modify the circuit elimination, and, as already mentioned above, elimination of breadboards.

Another difference is that the integrated circuit designer is restricted to a limited class of components which are compatible with integrated-circuit technology<sup>5</sup>.

<sup>5</sup> P. E. Allen, D. R. Holberg. *CMOS Analog Circuit Design*, pp. 5-7, Oxford University Press Inc., Oxford, 1 edition, 1987.

### 2.1.3.4

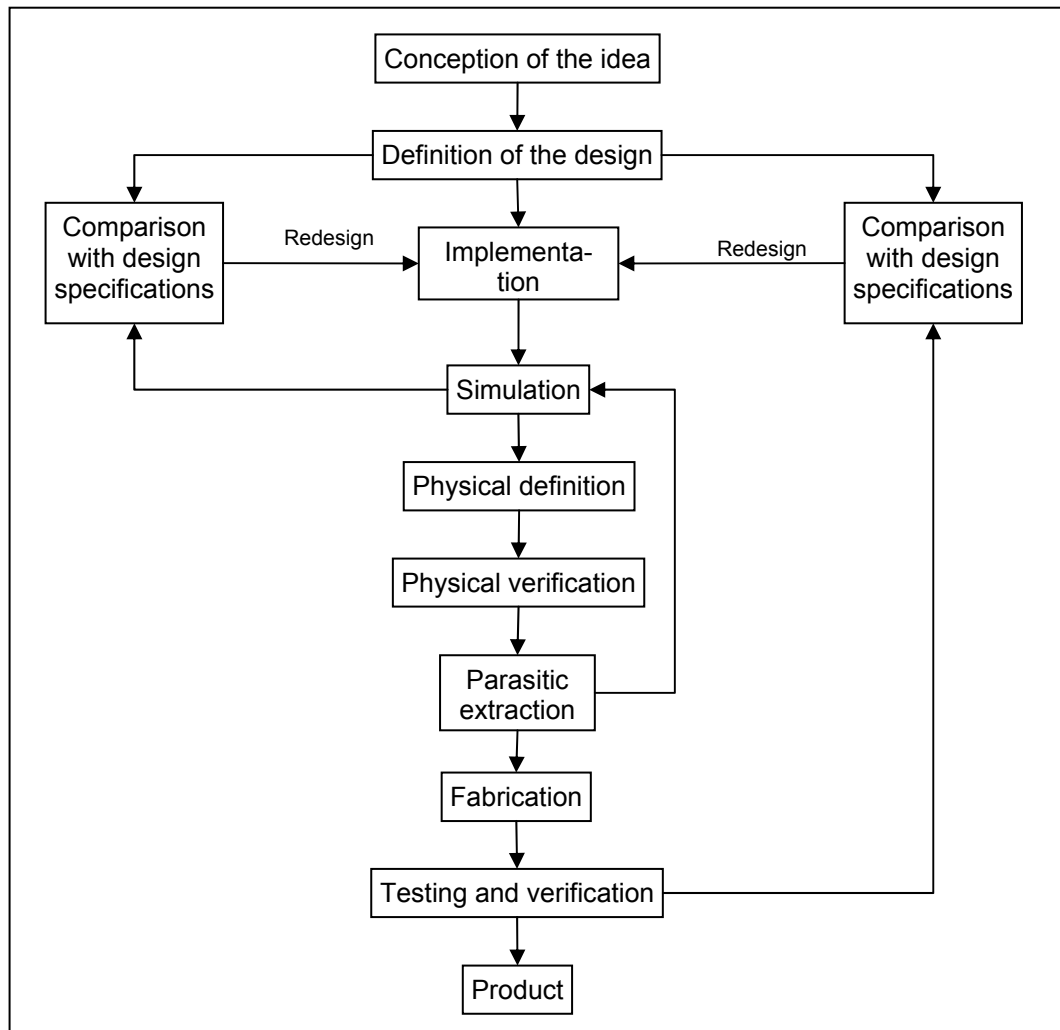
#### ***Steps of Integrated Circuit Design***

Figure 3 illustrates the general approach to the design of an integrated circuit. The major steps are:

1. Definition
2. Synthesis or implementation
3. Simulation or modeling
4. Geometrical description or layout
5. Simulation including the geometrical parasitics
6. Fabrication
7. Testing and verification

The designer is responsible for all of these steps except fabrication. The first major task is to define and synthesize the design. This step is crucial since it determines the performance capability of the design. When this task is completed, the designer must be able to confirm the design before it is fabricated. This leads to the second major task – using simulation methods to predict the performance of the circuit. At this point, the designer may iterate using the simulation results to improve the circuit's performance. Once satisfied with this performance, the designer can attack the third major task – a geometrical description (layout) of the circuit. This geometrical description typically consists of a computer database of variously shaped rectangles or polygons (in the x-y plane) at different levels (in the z-direction); it is intimately connected with the electrical performance of the circuit. Once the layout is finished, it is necessary to include the geometrical effects in a second simulation. If the results are satisfactory, the circuit is ready for fabrication. Then the designer is faced with the last major task – determining whether the fabricated circuit meets the design specifications. If the designer has not carefully considered this step in the overall design process, it is often impossible to test the circuit and determine whether or not the specifications have been met<sup>5</sup>.





**Figure 3:** The design process for analog integrated circuits.

#### 2.1.4

##### Neural Networks and Analog VLSI

Artificial neural networks, or neurocomputers, provide an alternative form of computation that attempts to mimic the functionality of the human brain<sup>6</sup>. These networks seem to be better suited for information processing applications and tasks, such as optimization, pattern recognition and associative recall, than traditional digital computers.

Artificial neural networks have experienced significant growth in the last few years. However, only very large scale integration (VLSI) can realize the true computing potential of massively parallel neural networks. The realization of these neurocomputers, which are optimized to the computation of neural models, follow one of two approaches<sup>7</sup>:

<sup>6</sup> R. P. Lippman. *An Introduction to Computing with Neural Nets*. IEEE ASSP Magazine, pp. 4-22, 1987.

<sup>7</sup> P. Treleaven, M. Pacheco, and M. Vallsco. *VLSI Architecture of Neural Networks*. IEEE Micro, pp. 8-27, 1989.

1. general-purpose neurocomputers that consist of programmable processor arrays for emulating a range of neural network models, or,
2. special-purpose neurocomputers that are dedicated hardware implementations of a specific neural network model.

A major consideration is that programmable neurocomputers are an order of magnitude slower than what can be achieved by directly fabricating a neural network in hardware. For this reason, far more neural hardware is being developed than programmable neural processors.

Technologies used in special purpose neural network implementation are broadly categorized into silicon<sup>2, 8, 9</sup>, using analog or digital or mixed analog/digital integrated circuits, and optical or electro-optical<sup>10, 11</sup>.

Although modern scaled MOS and Bi-CMOS technologies inherently possess increased high-speed analog capabilities, voltage signal handling is severely limited for analog applications. Therefore, more emphasis has recently been devoted to current-mode analog signal processing. This seems attractive for neural networks with increased complexity since many of the neural functions naturally involve currents rather than voltage<sup>12</sup>. Chapter 2.3 "Current-Mode Analog Integrated Circuits", presents more background information on the benefits of current-mode circuit operation. Also, the function principles of the most frequently used arithmetical operations will be explained.

## 2.2

### MOS Transistor Characteristics and Model

MOS is an abbreviation for Metal-Oxide-Semiconductor. Both  $n$ - and  $p$ -channel MOS devices have a similar structure. An  $n$ MOS transistor is a sandwich of several layers; from top to bottom it contains layer of metal, silicon dioxide, and a substrate which is a lightly doped  $p$ -type semiconductor with two heavily doped  $n^+$  regions one on either side. The four terminals are identified as gate, substrate, source and drain, respectively. The conductance of the channel can be controlled by the gate-to-source voltage therefore this device is essentially a *voltage-controlled current source*<sup>13</sup>.

Presently, the most popular technology for realizing microcircuits makes use of MOS transistors. Microcircuits containing both  $n$ -channel and  $p$ -channel transistors are called CMOS circuits, for *complementary* MOS. Most of the current CMOS technologies utilize polysilicon gates rather than metal gates.

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<sup>8</sup> C. Mead and M. Ismail. *Analog VLSI Implementation of Neural Systems*. Kluwer Academic Publishers, 1989.

<sup>9</sup> D. Del Corso, K. E. Grosspietsch, and P. Treleaven. *Silicon Neural Networks*. Special issue IEEE Micro, a collection of good papers on digital and analog artificial neural networks, 1989.

<sup>10</sup> T. E. Bell. *Optical Computing: A Field in Flux*. IEEE Spectrum, Vol. 23, No. 8, pp. 34-57, 1986.

<sup>11</sup> Y.S. Abu-Mostafa and D. Pslatis. *Optical Neural Computers*. Scientific American, Vol. 256, pp. 88-95, 1987.

<sup>12</sup> C. Ioumazou, F. J. Lidgley & D. G. Haigh. *Analogue IC design: the current-mode approach*. In: Chapter 17 by S. Bibyk and M. Ismail. *Neural Network Building Blocks for Analog MOS VLSI*, pp. 597/598, Peter Peregrinus Ltd., London, United Kingdom, 1 edition. 1990.

<sup>13</sup> Z. Wang. *Current-Mode Analog Integrated Circuits and Linearization Techniques in CMOS Technology*, pp. 9, 1 edition, Hartung-Gorre Verlag Konstanz, 1990 (Series in microelectronics; Vol. 7)

## 2.2.1

### Regions of Operation

According to the bias conditions, an MOS transistor may either enter one of the following regions: weak inversion, moderate inversion and strong inversion, as illustrated in Figure 4.

#### 2.2.1.1

##### Weak Inversion

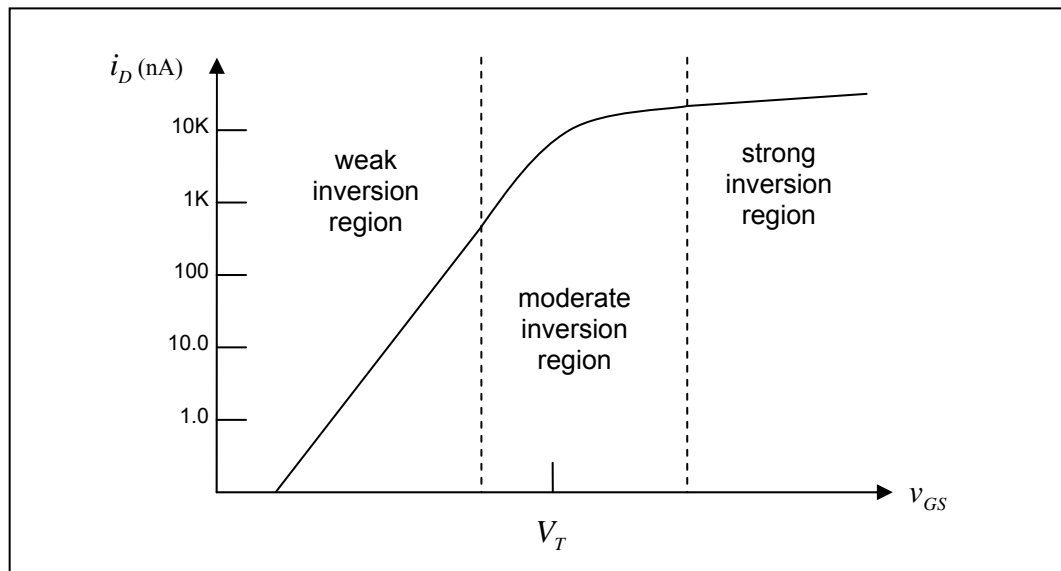
The condition for operating in weak inversion, also known as *subthreshold* operation region, is

$$|v_{GS}| < |V_T|$$

**Equation 2:** Condition for operation in weak inversion region.

where  $v_{GS}$  is the gate-to-source voltage and  $V_T$  is the device threshold voltage. In this case the surface is not strongly inverted and the drain current is very small and increases as an exponential function of  $v_{GS}$ . In other words, this means the current of transistors operating in this domain is exponentially dependent on the control voltages of the MOSFET.

Furthermore when MOSFETs are operated in the *subthreshold* domain, they draw small currents so power consumption is reduced.



**Figure 4:** Identifying three regions of MOS transistor operation.

More about circuits operating in the weak inversion regime can be found in section 2.4, titled *Characteristics of Subthreshold Operation*. It focuses on the characteristics of integrated circuits operating in the weak inversion domain, highlighting the relationship between the maximum achievable operation speed and power dissipation.

### 2.2.1.2

#### **Moderate Inversion**

This is the region in which the drain current can not be described either by exponential or by square-law characteristic and is situated between the weak inversion and the strong inversion.

### 2.2.1.3

#### **Strong Inversion**

When  $v_{GS}$  is larger than  $V_T$  the transistors operate in strong inversion region of its characteristics. According to the drain-to-source voltage  $v_{DS}$ , two regions may be defined.

- *The nonsaturation region:* the condition for nonsaturation operation is

$$|v_{GS} - V_T| > |v_{DS}|$$

**Equation 3:** Condition for operation in strong inversion region, nonsaturation.

For the given values of  $v_{DS}$  the channel extends from the source to the drain and the current of an  $n$ MOS transistor given by<sup>14</sup>

$$i_D = K[(v_{GS} - V_T)v_{DS} - \frac{1}{2}v_{DS}^2]$$

**Equation 4:** Drain current of an  $n$ MOS transistor in strong inversion, nonsaturation.

where  $K = \mu C_{ox} W / L$ .  $W$  is channel width,  $L$  is channel length,  $\mu$  is mobility of carriers, and  $C_{ox}$  is gate oxide capacitance per unit area.

- *The saturation region:* in the saturated mode of operation no inversion occurs at the drain end of the channel. However, current still flows as long as  $v_{GS} > V_T$ . In this mode the drain voltage can no longer influence the current. The condition for this is

$$|v_{GS} - V_T| \leq |v_{DS}|$$

**Equation 5:** Condition for operation in strong inversion region, saturation.

and the drain current of an  $n$ MOS transistor is<sup>15,14</sup>

$$i_D = \frac{K}{2}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

**Equation 6:** Drain Current of an  $n$ MOS transistor in strong inversion, saturation.

<sup>14</sup> R. Greorian and G. C. Temes. *Analog MOS Integrated Circuits for Signal Processing*. John Wiley & Sons, New York, 1 edition, 1986.

<sup>15</sup> P. R. Gray and R.G. Meyer. *Analysis and Design of Analog Integrated Circuits*. John Wiley & Sons, New York, 2 edition, 1984.

where  $\lambda$  is channel length modulation factor. The drain voltage at which saturation occurs is<sup>16</sup>  $|v_{DS}| = |v_{GS} - V_T|$ .

## 2.2.2

### Computer Simulation of MOS Circuits

One of the most important functions of analog integrated-circuit design is that of predicting or verifying the performance of the circuit or system. This function is accomplished through the use of modeling. Modeling is defined as the process by which the electrical properties of a semiconductor device or a group of interconnected devices are represented by means of mathematical equations, circuit representations, or tables. A more light-hearted definition of modeling proposed by Alava Archer states that *a model is an artifice that gives one the illusion of knowing more about a process than one actually does*<sup>17</sup>.

Modeling is most often done by using CAD (computer-aided design), which represents an efficient method for both analog and digital circuit design. SPICE (Simulated Program with Integrated Circuit Emphasis) is a general-purpose circuit simulation program for nonlinear DC, nonlinear transient, and linear AC analysis, and much more. With the help of SPICE, a circuit designer can simulate his or her circuit and check whether the designed circuit satisfies the requirements within a minute, without any measurements on the real circuit. Thus, computer simulation provides a fast, cheap, and convenient approach to analog circuit design. Fabrication without simulation can be an expensive proposition if the circuit does not work because of a mistake that could have been avoided by simulation. The economics of this situation have strongly favored the development of simulation capabilities rather than trial-and-error fabrication cycles.

Figure 5 shows how a simulator of analog circuits might be organized. The typical input to the simulator would be a topological description of the circuit on a branch-by-branch basis. Each branch would be identified as to the type of component, the nodes between it is connected, and other pertinent information. This is the point at which the parameters of the models for nonlinear devices are described to the simulator. In addition, the designer must identify all dependent sources applied to the circuit. The simulator will use this information to solve for the DC values of voltages and currents. Most simulators today use algorithms that guess the node voltages and use the models to calculate all branch currents. These branch currents are summed at every node to see if they satisfy Kirchhoff's current law. If they do not sum to zero within a specified limit, the simulator re-guesses the voltage using various algorithms until the nodal voltages converge on the values that cause all branch currents to sum to zero at each node within a specified tolerance.

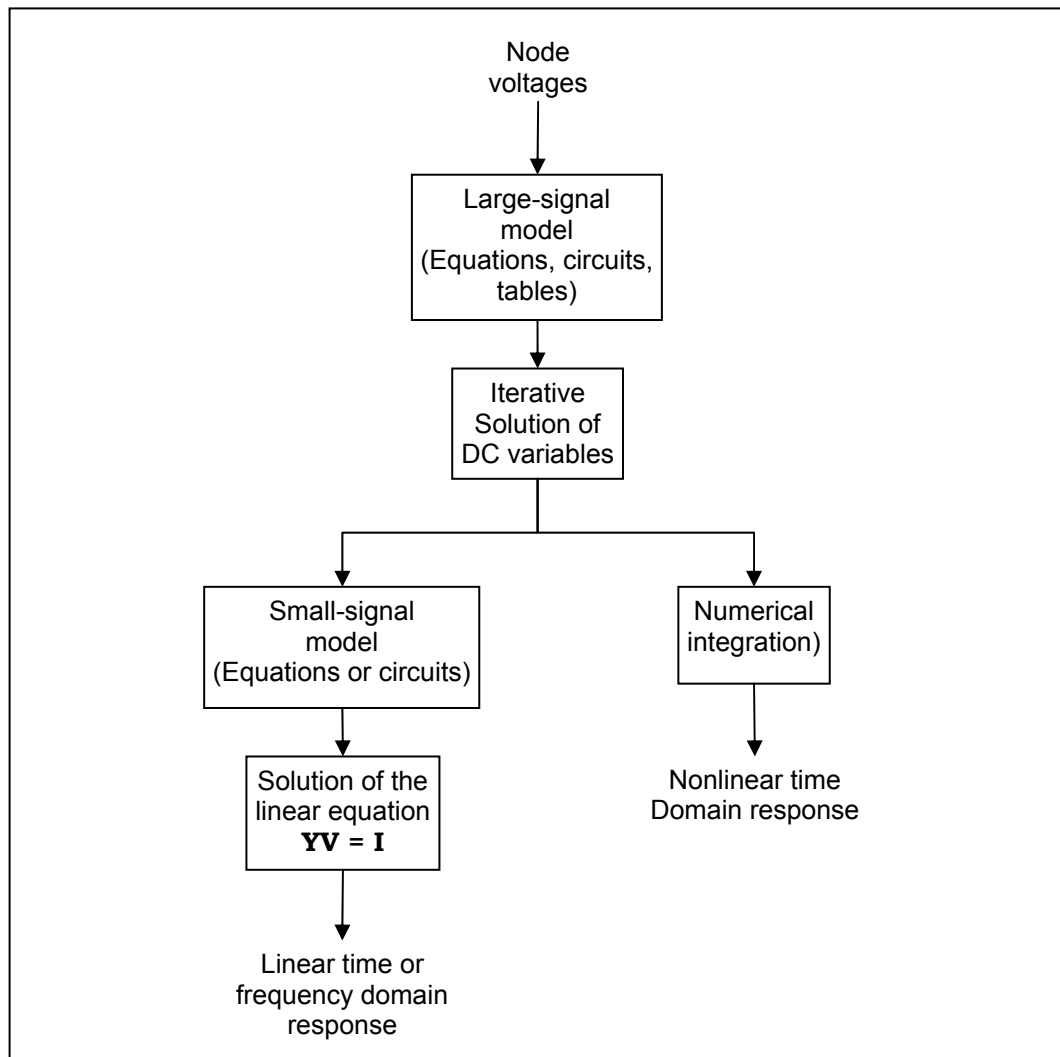
Once the circuit converges to a solution of the nodal voltages and currents, the simulation can take two paths. If the desired analysis is a small signal, then the small-signal models are evaluated. These models are linear and thus linear-matrix solution methods are used to evaluate the time or frequency domain response. Methods for solving these linear equations are well known<sup>18</sup>. The second path that can be taken is the use of nu-

<sup>16</sup> Z. Wang. *Current-Mode Analog Integrated Circuits and Linearization Techniques in CMOS Technology*. pp. 10/11, 1 edition, Hartung-Gorre Verlag Konstanz, 1990 (Series in microelectronics; Vol. 7)

<sup>17</sup> P. E. Allen, D. R. Holberg. *CMOS Analog Circuit Design*, pp. 95, Oxford University Press Inc., Oxford, 1 edition, 1987.

<sup>18</sup> G. S. Forsythe and C. B. Moler. *Computer Simulation of Linear Algebraic Equations*. Englewood Cliffs, New Jersey, Prentice-Hall, 1967.

merical integration to find the large-signal time or frequency domain response. The designer must then describe the time characteristics of dependent sources applied to the circuit. This method uses DC values as the initial starting point.



**Figure 5:** General organization of a simulator for analog circuits.

A time step is defined in which the simulator uses various numerical integration algorithms to find or predict the value of the nodal voltages at the end of the time step. Those algorithms are iterative and may be subject to convergence problems. Most simulators can vary the time step in order to try to enhance the tradeoff between convergence and computational efficiency<sup>19</sup>.

<sup>19</sup> P. E. Allen, D. R. Holberg. *CMOS Analog Circuit Design*, pp. 128/129, Oxford University Press Inc., Oxford, 1 edition, 1987.

## 2.3

### Current-Mode Analog Integrated Circuits

During the last 40 years, the vast majority of analog circuits have used voltages to represent and process relevant signals. However, recently, current-mode signal processing circuits, in which signals and state variables are represented by currents rather than voltages (Tomazou et al., 1990), have shown advantages over their voltage-mode counterparts.

#### 2.3.1

##### Advantages of Current-Mode Operation

Initially, the widespread use of MOS technology, with its unique ability to accurately store and transfer voltages or charge packets, led to the development of analog integrated circuit techniques in which voltage was used as the signal. Although these techniques are quite successful in many applications, reductions in the available supply voltage and the deterioration in the performance of the analog components caused by the move to ever smaller geometries, is likely to limit their performance<sup>20</sup>.

Generally current-mode circuits do not require amplifiers with high voltage gains thereby reducing the need for high performance amplifiers<sup>21</sup>. At the same time, current mode circuits generally do not require either high precision resistors or capacitors and when capacitors are used to store the signal, the capacitors need not display either good ratio matching or good linearity<sup>22, 23, 24</sup>. Consequently, current-mode circuits can be designed almost exclusively with transistors making them fully compatible with most digital processes<sup>20</sup>.

Current-Mode operated circuits include advantages such as higher bandwidth, higher dynamic range, and they are more amenable to lower power supplies. Furthermore, advances in integrated circuit design have meant that state-of-the-art analog integrated circuit design is now able to exploit the potential of current-mode analog signal processing, providing attractive and elegant solutions for many circuit and system problems.

In many applications, circuits operating in the current domain will bring benefits. One reason is that many signal sources are *current-type*, such as temperature sensors, photo sensors and many others in biomedicine. Processing the signal in current will not only avoid the use of a current-to-voltage converter but also cut down the components' cost.

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<sup>20</sup> C. Ioumazou, F. J. Lidgley & D. G. Haigh. *Analogue IC design: the current-mode approach*. In: Chapter 13 by C. A. T. Salama, D. G. Nairn and W. Singor. *Current Mode A/D and D/A Converters*. Peter Peregrinus Ltd., London, United Kingdom, 1 edition. 1990.

<sup>21</sup> J. B. Shyu, G. C. Temes, and F. Krummenacher. *Random Error Effects in Matched MOS Capacitors and Current Sources*. IEEE Journal of Solid-State Circuits, Vol. SC-19, pp. 948-955, 1984.

<sup>22</sup> J. B. Hughes, N. C. Bird, and I. C. Macbeth. *Switched Currents – A New Technique For Analog Samples-Data Signal Processing*. 1989 International Symposium on Circuits and Systems, Proceedings, pp. 1584-1587, Portland, 1989.

<sup>23</sup> W. Groeneveld, H. Schouwenaars, and H. Termeer. *A Self Calibration Technique for Monolithic High-Resolution D/A Converters*. ISSCC Digest of Technical Papers, Vol. 32, pp. 22-23, New York, 1989.

<sup>24</sup> D. Vallancourt, and Y. P. Tsvividis. *Sampled-Current Circuits*. Proceedings of the 1989 International Symposium on Circuits and Systems, pp. 1592-1595, Portland, 1989.

For example, a comparator for current input and voltage output can be implemented with only four MOS transistors, while in voltage domain it is impossible to realize with so few devices. In current domain, computations like addition and subtraction can be performed with just two current mirrors, while in voltage domain, these functions are very difficult to achieve for a large range of inputs (see sections 2.3.3 and 2.3.4 for more details on that topic). Especially in the low-voltage circuits, voltage-domain behavior will suffer due to the threshold voltage of the devices. Such difficulties can be overcome by operating in the current domain.

### 2.3.2

#### Details on Voltages and Currents

Basically, a circuit is designed to perform a certain task or function. It may be an arithmetic computation, an automatic control, or something else. Take computation as an example. We know that any computation can be achieved with both digital and analog circuits. In the past however, computations were mainly performed with analog circuits.

In the analog electronic system, there are two signal types: *voltages* and *currents*. Any voltage-type signal must have a reference at which its value is defined to be zero. The reference usually is the potential on another node. The reference potential can be constant such as ground, or it can be an active signal node. In contrast, operations on current-type signals are well defined; they do not suffer from any of the problems mentioned for voltage-type signals.

Table 2 is an overview of different techniques to encode information in electronic systems.

**Table 2:** System classification by means of value- and time domain.

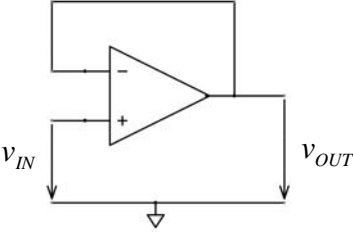
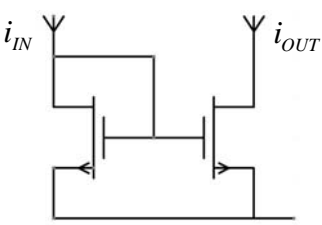
	Information is		
	Analog		Digital
	Voltage	Current	
Continuous time	Classic analog circuit technology, e.g. filters, amplifiers, ... Typical components: Discrete components and integrated function blocks	Current-mode circuits (exploiting the component's characteristic curves for currents and voltages) Typical components: Transistors, current sources, current mirrors, current amplifiers, current conveyor	Asynchronous digital systems
Discrete time	Circuits using switched capacitors Typical components: Linear capacitances, operational amplifiers, switches	Switched current circuits (based on current-mode circuits) Typical components: Transistors, switches, capacitances (don't necessarily have to be linear)	Classic digital technology Typical components: Gates, standard cells, function blocks



### 2.3.3

#### Identity Operation

In analog systems, identity operation is used to make *copies* of signal values. In voltage-type circuits, identity operation is performed by a voltage follower while in current-mode circuits it is performed by a current mirror (for more details on the current mirror function principle see chapter 2.5). For comparison these identity operations are shown in Figure 6. In ideal cases, a voltage follower is a voltage-controlled voltage source with infinite input resistance and zero output resistance, while a current mirror is a current-controlled current source with zero input resistance and infinite output resistance.

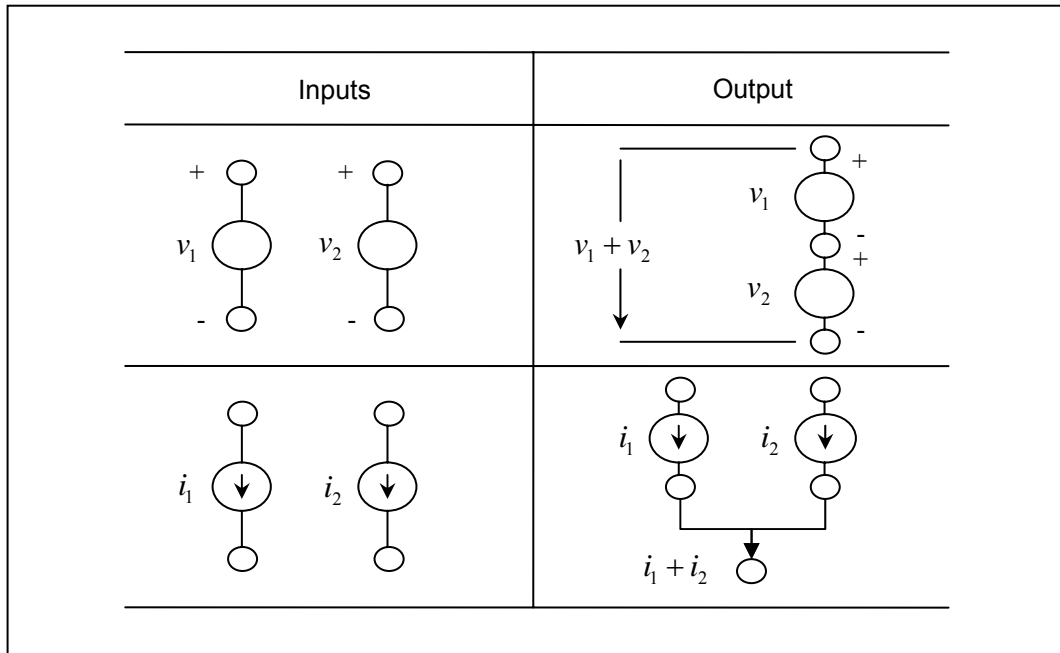
Identity operation	Circuit schematic
$v_{OUT} = v_{IN}$	 <p data-bbox="772 1093 963 1122">voltage follower</p>
$i_{OUT} = i_{IN}$	 <p data-bbox="788 1384 963 1413">current mirror</p>

**Figure 6:** A comparison of identity operation in voltage and current domains.

### 2.3.4

#### Adder and Subtractor

Addition and subtraction on current-type signals are particularly elegant in comparison with those on voltage-type signals because they follow from a basic law of physics – Kirchhoff's current law. While in voltage domain, these operations follow from Kirchhoff's voltage law. The difficulty in implementing both addition and subtraction in voltage domain lies in the nature of voltage – it requires a reference potential, i.e., a voltage is defined only if two nodes are specified. In current domain, however, only one node is required; these are illustrated in Figure 7.



**Figure 7:** Comparison of addition in voltage and current domains.

## 2.4

### Characteristics of Subthreshold Operation

In this chapter MOSFETs and their current-voltage characteristics in the *subthreshold* (also known as *weak inversion*) domain are discussed. The chapter will focus on how the operation speed of an integrated circuit, working in the subthreshold domain, depends on its power dissipation.

One of the reasons why transistors operating in this domain are so power efficient is the fact, that the conductance  $g_m$  is linearly linked with the drain current  $I_D$  ( $g_m \sim I_D$ ). Since the conductance again has direct influence on the settling time  $\tau = C/g_m$  and consequently the processing time  $f_{op} \sim 1/\tau$  of a circuit ( $C$  is the capacitance to be loaded, consisting of required and parasitic capacitances). While the power dissipation  $P_V$  and the drain current  $I_D$  are in linear coherence in subthreshold MOS circuits, power dissipation and processing time are interchangeable.

When operating in strong inversion regime, the conductance of a MOS transistor only increases with the square root of the drain current. Thus, for the power dissipation of a transistor we can write the equation shown below.

$P_V \sim f_{op}$	Weak Inversion
$\sqrt{P_V} \sim f_{op}$	Strong Inversion

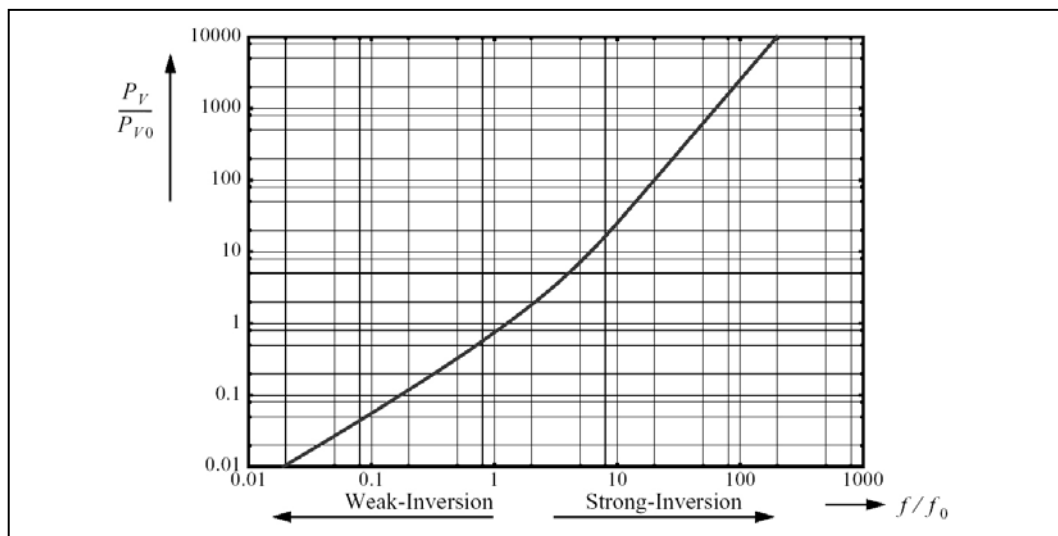
**Equation 7:** Power dissipation of a transistor when operating in subthreshold regime.

In order to double the system's computing power when operating in subthreshold regime, twice the amount of power is needed, whereas a system operating in strong inversion will need four times the amount of power to achieve the same performance, as illustrated in Figure 8. With Equation 7, the following correlation for a system consisting of  $N$  transistors can be made:

$P_V \sim N \cdot f_{op}$	Weak Inversion
$P_V \sim N \cdot f_{op}^2$	Strong Inversion

**Equation 8:** Power dissipation of a subthreshold system consisting of  $N$  transistors.

In subthreshold regime the amount of transistors, power dissipation and processing speed are linearly linked to each other. To achieve a certain processing speed, a certain power dissipation is necessary, thereby it does not matter if there are 100 transistors switching at 10kHz or 10 transistors switching at 100kHz. As soon as there's a frequency necessary which can't be obtained by using subthreshold currents, it is more efficient to use maximum parallelism from the power dissipation's point of view.



**Figure 8:** Power dissipation required for a certain processing speed. While subthreshold currents suffice to obtain the working frequency, power dissipation increases with the frequency. Are higher frequencies necessary, power dissipation increases by the square of the frequency. The standard frequency  $f_0$  is the maximum frequency which can be obtained through subthreshold currents,  $P_{V0}$  is the power loss at this point ( $f_0 = I_{D0} / 2\pi C \cdot nU_T$ ,  $P_{V0} = VI_{D0}$ ).

There is a whole class of these so called *low-power* circuits. They have been developed based on weak inversion operation characterized by the above model<sup>25, 26, 27, 28</sup>.

<sup>25</sup> E. Vittoz and J. Fellrath. *CMOS Analog Integrated Circuits Based on Weak Inversion Operation*. pp. 231-244, IEEE Journal of Solid-State Circuits, Vol. SC-12, No. 3, 1977.

<sup>26</sup> M. G. DeGrauwe, J. Rigenants, E. Vittoz and H. J. DeMan. *Adaptive Biasing CMOS Amplifiers*. pp. 522-528, IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 3, 1982.

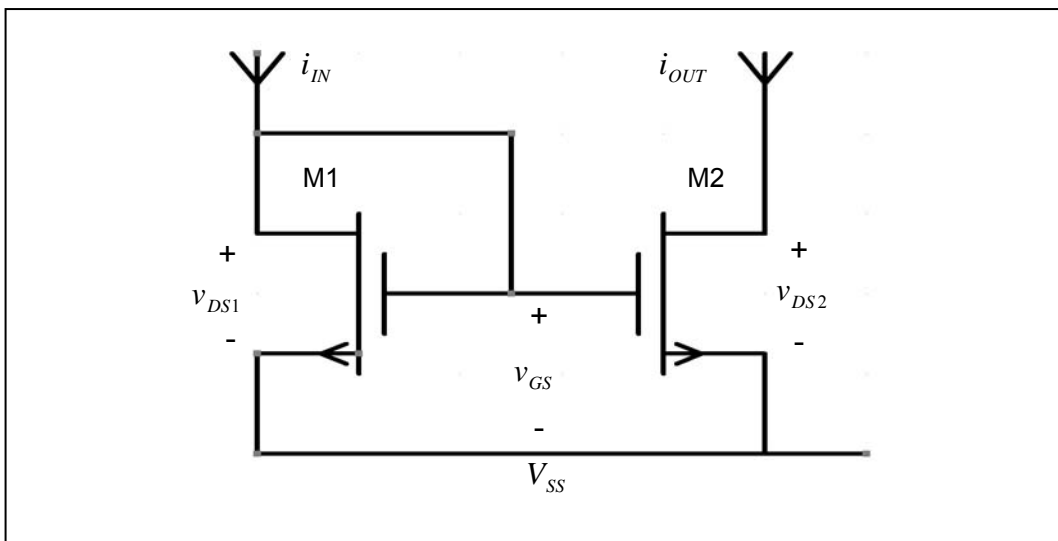
## 2.5

### The Current Mirror

An important building block in CMOS analog-circuit design is called the *current mirror*. As well as performing the identity operation and current amplification, current mirrors are also used both as biasing elements and as load devices for amplifier stages. Current comparators, current Schmitt triggers, and current A/D- and D/A-converters are additional examples of circuits and devices that benefit from the use of current mirrors.

#### 2.5.1

##### Function Principle



**Figure 9:** N-Channel current mirror.

The current mirror uses the principle that if the gate-source potential of two identical MOS transistors are equal, the channel currents should be equal. Figure 9 shows the implementation of a simple *n*-channel current mirror. The current  $i_{IN}$  is assumed to be defined by a current source or some other means and  $i_{OUT}$  is the output or “mirrored” current.  $M1$  is in saturation because  $v_{DS1} = v_{GS1}$ . Assuming that  $v_{DS2} \geq v_{GS} - V_{T2}$  is greater than  $V_{T2}$  allows us to use the equations in the saturation region of the MOS transistor. In the most general case, the ratio of  $i_{OUT}$  to  $i_{IN}$  can be described using the following equation.

$$\frac{i_{OUT}}{i_{IN}} = \left( \frac{L_1 W_2}{W_1 L_2} \right) \left( \frac{v_{GS} - V_{T2}}{v_{GS} - V_{T1}} \right)^2 \left( \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}} \right) \left( \frac{K'_2}{K'_1} \right)$$

**Equation 9:** Simple current mirror ratio of  $i_{OUT}$  to  $i_{IN}$ .

<sup>27</sup> W. Steinhagen and W. L. Engl. *Design of Integrated Analog CMOS Circuits – A Multichannel Telemetry Transmitter*. pp. 799-805, IEEE Journal of Solid-State Circuits, Vol. SC-13, No. 6, 1978.

<sup>28</sup> Y. Tsidis and R. Ulmer. *A CMOS voltage Reference*. pp. 774-778, IEEE Journal of Solid-State Circuits, Vol. SC-13, No. 6, 1978.

Normally, the components of a current mirror are processed on the same integrated circuit and thus all of the physical parameters such as  $V_T$ ,  $K'$ , etc., are identical for both devices. As a result, Equation 9 simplifies to

$$\frac{i_{OUT}}{i_{IN}} = \left( \frac{L_1 W_2}{W_1 L_2} \right) \left( \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}} \right)$$

**Equation 10:** Simplified current ratio equation for the simple current mirror.

If  $v_{DS2} = v_{DS1}$  (not always a good assumption), then the ratio of  $i_{OUT}/i_{IN}$  becomes<sup>29</sup>

$$\frac{i_{OUT}}{i_{IN}} = \left( \frac{L_1 W_2}{W_1 L_2} \right)$$

**Equation 11:** Current ratio for the simple current mirror in case  $v_{DS2} = v_{DS1}$ .

## 2.5.2

### Current Mirror Forming

As seen in the previous section,  $i_{OUT}/i_{IN}$  is a function of the aspect ratios that are under the control of the designer. This means,  $i_{OUT} = i_{IN}$  describes a current mirror;  $i_{OUT} > i_{IN}$  represents a current amplifier and a current attenuator can be obtained if  $i_{OUT} < i_{IN}$ . Thus either amplification or attenuation can be conveniently achieved by setting the aspect ratio or channel width ratio (setting  $L_1 = L_2$  in order to cancel the effect of channel-length modulation).

The purpose of forming a current mirror is primarily to create a current source or sink<sup>30</sup> whose output is equal to the input. For a current source, the output resistance is an important performance aspect. The current mirror introduced in the last chapter also is called *simple current mirror*. This is because there are several other approaches to improve the output resistance of this simple current mirror. The two most effective approaches are called *cascaded current mirror* and *Wilson current mirror*. They both offer raised output resistance and better accuracy. In CMOS however, neither of these mirrors are suitable for use with a low power-supply voltage because each requires an input voltage of at least two diode drops and has an output compliance voltage of a diode drop plus a saturation voltage<sup>31</sup>.

## 2.5.3

### Mismatch in Current Mirrors

There are three effects that cause the current mirror to be different than the ideal situation of Equation 11.

<sup>29</sup> P. E. Allen, D. R. Holberg. *CMOS Analog Circuit Design*, pp. 227, Oxford University Press Inc., Oxford, 1 edition, 1987.

<sup>30</sup> In current sources current flows out of the circuits while in current sinks current flows into the circuits.

<sup>31</sup> B. A. Minch. *A Low-Voltage Current Mirror for all Current Levels*. Unknown IEEE Journal, 2002.

These effects are:

1. Channel-length modulation
2. Threshold offset between the two transistors
3. Imperfect geometrical matching.

Consider the channel-length modulation effect. Assuming all other aspects of the transistor are ideal and the aspect ratios of the two transistors are both in unity, then Equation 10 simplifies to

$$\frac{i_{OUT}}{i_{IN}} = \left( \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}} \right)$$

**Equation 12:** Current ratio of the simple current mirror assuming that all effects except the channel-length modulation are ideal.

with the assumption that  $\lambda$  is the same for both transistors. This equation shows that differences in drain-source voltages of the two transistors can cause a deviation for the ideal unity current gain or current mirroring. Consequently, a good current mirror should have identical drain-source voltages and a high output resistance.

The second nonideal effect is that of offset between the threshold voltages of the two transistors. For clean silicon-gate CMOS processes, the threshold offset is typically less than 10mV for transistors that are identical and in close proximity to one another. Consider two transistors in a mirror configuration where both have the same drain-source voltage and all other aspects of the transistors are identical, except  $V_T$ . In this case, Equation 9 simplifies to:

$$\frac{i_{OUT}}{i_{IN}} = \left( \frac{v_{GS} - V_{T2}}{v_{GS} - V_{T1}} \right)^2$$

**Equation 13:** Current ratio of the simple current mirror assuming that all effects except the threshold offset between two transistors are ideal.

Thus, better current-mirror performance is obtained at higher currents, because  $v_{GS}$  is higher for higher currents and consequently  $\Delta V_T$  becomes a smaller percentage of  $v_{GS}$ .

The third nonideal effect of current mirrors is the error in the aspect ratio of the two devices. Differences in the drawn values of  $W$  and  $L$  are due to mask, photolithographic, etch and out-diffusion variations. These variations can be different even if two transistors are placed side by side. One way to avoid the effects of these variations is to make the dimensions of transistors much larger than the typical variation one might see. For transistors of identical size with  $W$  and  $L$  greater 10 $\mu\text{m}$ , the errors due to geometrical mismatch will generally be insignificant compared to offset-voltage and  $v_{DS}$ -induced errors<sup>32</sup>.

<sup>32</sup> P. E. Allen, D. R. Holberg. *CMOS Analog Circuit Design*, pp. 228-230, Oxford University Press Inc., Oxford, 1 edition, 1987.

## 2.6

### Noise in Subthreshold Circuits

To develop good analog circuit designs, a basic understanding of noise sources and analysis is required.

#### 2.6.1

##### Noise Definition

Noise is defined as any unwanted excitation in a circuit. It comes from both external sources and internal sources. Noise from external sources occurs because of unintended coupling of the circuit with other parts of the physical world; noise from internal sources appears because of unpredictable microscopic events in the devices that constitute the circuit. In principle, noise from the former can be eliminated through careful design whereas noise from the latter can be reduced but never eliminated. It is important to consider noise in the design of low-power systems because the signal levels (voltages or currents) are small. The noise level sets the size of the smallest signal that can be processed meaningfully by a physical system<sup>33</sup> (signal to noise ratio, *SNR*).

#### 2.6.2

##### Influence of Transistor Noise

The currents in subthreshold circuits are relatively small, therefore the influence of transistor noise can not be neglected. The power density spectrum of thermal noise of a transistor in weak inversion can be described as follows:

$$S_{I,th}(f) = 4kT \cdot G_N$$

**Equation 14:** Thermal noise of a transistor in weak inversion.

where  $T$  is the temperature,  $k$  the Boltzmann constant, and  $G_N$  the equivalent noise guide value of the conducting channel. For a transistor in weak inversion is  $G_N = g_m \cdot n / 2$ <sup>34</sup> with  $g_m = I / nU_T$ . For  $U_T$  it can be written  $U_T = kT / e$ . Thus Equation 14 can be simplified to

$$S_{I,th}(f) = 4kT \cdot \frac{n}{2} \cdot \frac{I}{nkT} \cdot e = 2eI$$

**Equation 15:** Simplified equation for thermal noise in weak inversion.

with  $e$  being the elementary charge and  $n$  being the subthreshold rate of rise constant. Furthermore, the 1/f-noise with the power density spectrum shown in the following equation matters.

<sup>33</sup> S. Liu, J. Kramer, G. Indiveri, T. Delbrück and R. Douglas. *Analog VLSI: Circuits and Principles*, pp. 313/314, The MIT Press, Cambridge, Massachusetts, 1 edition, 2002.

<sup>34</sup> C. Enz. *MOS modeling for LV-LI circuit design*. Advanced Engineering Course on CMOS & BiCMOS IC Design, 1995.

$$S_{I,fl}(f) = \frac{K_f}{C_{ox}'' \cdot WL \cdot f} \cdot g_m^2 = \frac{K_f}{C_{ox}'' \cdot WL \cdot f} \cdot \frac{I^2}{(nU_T)^2}$$

**Equation 16:** Power density spectrum of 1/f-noise in weak inversion.

Where  $K_f$  is a process independent noise constant,  $C_{ox}''$  is the gate capacity per area, and  $W$  and  $L$  are the transistor dimensions. The influence of noise in the sub-threshold regime can be minimized by increasing the current.

## 2.7

### Transistor Mismatch Model

The drain current mismatch not only depends on a device's dimensions but also on the operating point. It can be expressed by

$$\frac{\sigma_{i_D}^2}{i_D^2} = \frac{\sigma_K^2}{K^2} + 4 \frac{K}{i_D} \sigma_{V_T}^2$$

**Equation 17:** Drain current mismatch.

where  $\sigma_{i_D}^2$ ,  $\sigma_K^2$  and  $\sigma_{V_T}^2$  are variances of  $i_D$ ,  $K$  and  $V_T$ , respectively. The variation of threshold voltage is the dominant factor causing mismatch under lower drain current conditions.

It is known that the uniform distribution of the doping atoms in the bulk is a major contributor to threshold voltage mismatch and can be described by

$$\sigma_{V_T} = \frac{1}{\sqrt{LW}} \left( 2.59 \times 10^{-12} + 1.24 A_{ox} \right)^{\frac{1}{2}}$$

**Equation 18:** Distribution of the doping atoms in the bulk terminal.

where gate oxide capacitance matching factor  $A_{ox}$  is found to be  $6.431 \times 10^{-14} \text{ cm}^2$  for n-channel and  $3.0369 \times 10^{-12} \text{ cm}^2$  for p-channel MOS devices.

Oxide gradients and edge variations give rise to mismatch in  $K$ , which is found to be

$$\frac{\sigma_K^2}{K^2} = \left( 2.46 \times 10^{-13} + 0.65 \times 10^{-13} \right) \frac{1}{LW} + 4 \times 10^{-12} \left( \frac{1}{L^2} + \frac{1}{W^2} \right)$$

**Equation 19:** Oxide gradients and edge variations.



where the effective dimensions  $L$  and  $W$  are measured in centimeters. Comparing two expressions we note that the standard deviation of mismatch in  $V_T$  is inversely proportional to the square root of the effective channel area ( $W \times L$ ), while the mismatch in  $K$ , due to edge variation, is proportional to  $(1/L^2 + 1/W^2)^{1/2}$  and mismatch in  $K$ , due to mobility mismatch and gate capacitance mismatch, is inversely proportional to the effective channel area<sup>35</sup>.

## 2.8

### Analog to Digital Converters

This section examines the principles of different known types of analog-to-digital converters. The general objective of an A/D converter is to determine the output digital word corresponding to an analog input signal. Normal A/D converters use a clock which drives the conversion circuit. In order to convert an analog signal at a certain point in time to a digital word, a so called *sample and hold circuit* is required to perform this operation. However, the two different analog A/D converters described in thesis do not require such circuitry because they are analog circuits. Analog and digital ADC's have one thing in common; they can be characterized and specified in the same way. With this in mind, the necessary background information on that will be presented in the following sections, which will later be used in the characterization and specification part of the circuits described in this work (see chapter 4 and 5).

#### 2.8.1

##### Specification of A/D Converters

Regardless of the means of conversion, the A/D converter is a device that converts a continuous range of input amplitude levels into a discrete, finite set of digital words. In order to determine how accurate the conversion is, the converter needs to be specified. The main classification to do this is to distinguish between DC and dynamic specifications of the A/D converter.

##### 2.8.1.1

###### DC Specifications

DC specifications are also called static characteristics. They characterize behavior when the analog input signal remains unchanged at a fixed level.

###### 2.8.1.1.1 Absolute Accuracy

Accuracy of converters should not be confused with linearity and resolution. The *absolute accuracy* of a converter is the actual full-scale input or output (analog-to-digital or digital-to-analog converter) signal (voltage, current, or charge) referred to the absolute standard of the National Bureau of Standards. This absolute accuracy concerns the reference source used in the converter<sup>36</sup>.

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<sup>35</sup> Z. Wang. *Current-Mode Analog Integrated Circuits and Linearization Techniques in CMOS Technology*, pp. 22, 1 edition, Hartung-Gorre Verlag Konstanz, 1990 (Series in microelectronics; Vol. 7)

<sup>36</sup> R. van de Plassche. *Integrated Analog-to-Digital and Digital-to-Analog Converters*, pp. 41-69, Kluwer Academic Publishers, 1 edition, Netherlands, 1994.

### 2.8.1.1.2 **Relative Accuracy / Linearity**

The *relative accuracy* is the deviation of the output signal or output code of a converter from a straight line drawn through zero and full scale. Output signals or output codes must be corrected from possible zero offset. This relative accuracy is called: Integral Non Linearity (INL) or sometimes *linearity*<sup>36</sup>.

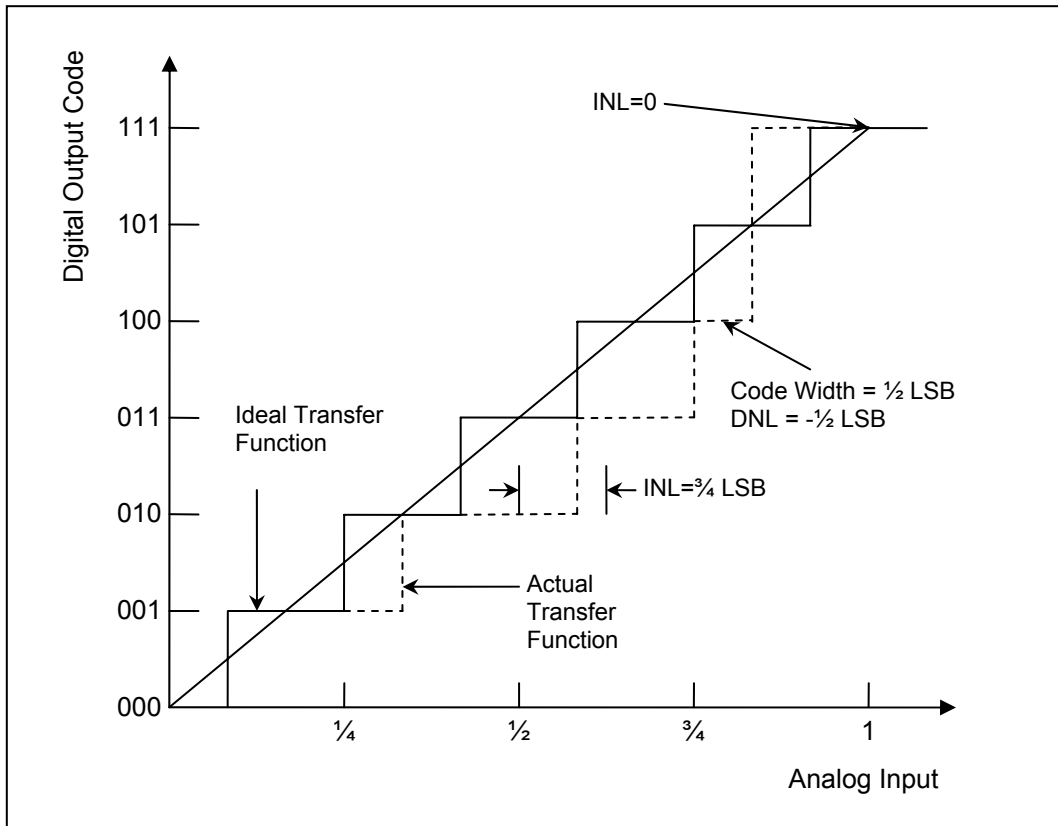
### 2.8.1.1.3 **Differential Nonlinearity**

*Differential Nonlinearity* (DNL) error describes the difference between two adjacent analog signal values compared to the step size (LSB weight) of a converter generated by transitions between adjacent pairs of digital code numbers over the full range of the converter. In case of an analog-to-digital converter the DNL can be written as:

$$DNL = A_{input}(Q_{m+1}) - A_{input}(Q_m) - 1LSB$$

**Equation 20:** Differential Non Linearity of an analog-to-digital converter.

$Q_{m+1}$  and  $Q_m$  are two adjacent quantization levels.  $A_{input}(Q_n)$  is the analog input signal corresponding to the quantization level  $Q_n$ <sup>36</sup>. In Figure 10 the transfer curve of a 3-bit A/D converter is shown. The drawn line shows the ideal transfer characteristic, while the dashed line indicates the measured transfer curve of a practical converter. Integral nonlinearity (INL), differential nonlinearity (DNL) and full-scale range (FSR) are shown partly as a function of the LSB error between the drawn line and the actual measured dashed lines. Furthermore, an example of a missing code is given in the picture. In a visualized way the nonlinearity errors are shown to improve understanding.



**Figure 10:** Transfer curve of a 3-bit A/D converter.

#### 2.8.1.1.4 Quantization and Quantization Error

Quantization  $Q$ , of an ideal A/D converter is related to the number of bits  $N$ , and the input range  $I_R$ , through the relationship

$$Q = \frac{I_R}{2^N}$$

**Equation 21:** Quantization error of an A/D converter.

In a real A/D converter, the error in the quantization step  $\Delta Q_i$  for the  $i$ th output code, can be expressed as the product of  $Q$  and the differential nonlinearity,  $DNL$

$$\Delta Q_i = DNL \cdot Q$$

**Equation 22:** Quantization error of a real A/D converter.

### 2.8.1.1.5 Offset

Input Amplifiers, output amplifiers and comparators in practical circuits inherently have a built-in offset voltage or offset-current. This offset is caused by the finite matching of components. The offset results in a non-zero input- or output voltage, current or digital code although a zero signal is applied to the converter<sup>36</sup>.

### 2.8.1.2

#### Dynamic Specifications

When looking at the dynamic specifications of an A/D converter, the speed of the conversion process is of interest.

#### 2.8.1.2.1 Signal-to-Noise Ratio

The most important dynamic specification of a converter is the *signal-to-noise* ratio. This signal-to-noise ratio depends on the resolution of the converter and automatically includes specifications of linearity, distortion, sampling time uncertainty, glitches, noise and settling time. Over half the sampling frequency, this signal-to-noise ratio must be specified and should ideally follow the theoretical formula:

$$S / N_{\max} = 6.02n + 1.76dB$$

**Equation 23:** Theoretical formula for the signal-to-noise ratio.

This S/N ratio is calculated for a sine wave input with maximum amplitude and the ratio between the frequency of the sine wave, and the sampling frequency should be irrational. In case input signals with a smaller amplitude are applied then the S/N ratio decreases in accordance to the input signal decrease<sup>36</sup>.

#### 2.8.1.2.2 Noise

Thermal noise (white-noise) from bit-currents, amplifiers and resistors, adds to the quantization noise. This thermal noise exhibits itself as a deviation from the theoretical maximum signal-to-noise ratio that an ideal converter can have. When the thermal noise specification is given for a converter, this figure is not a measure for the (dynamic) signal-to-noise ratio of the system. However, the noise of the individual bit currents must be much lower than the quantization “noise” of the system.

A simple calculation demonstrates the decrease in signal-to-noise ratio of a system compared to the signal-to-noise ratio of the basic converter in that system. Define the noise power of the quantizer as  $N_{\text{quantizer}}$  and the thermal noise power of the system as  $N_{\text{thermal}}$ . When there exists no correlation between the noise sources then the total noise system ( $N_{\text{system}}$ ) will be<sup>36</sup>:

$$N_{\text{system}} = \sqrt{N_{\text{quantizer}}^2 + N_{\text{thermal}}^2}$$

**Equation 24:** Noise in a system without correlation between the noise sources.

In rewriting Equation 24 to the quantizer noise, the result becomes:

$$N_{system} = N_{quantizer} \cdot \sqrt{1 + \frac{N_{thermal}^2}{N_{quantizer}^2}}$$

**Equation 25:** Rewritten system noise equation.

### 2.8.1.2.3 Bit Error Rate

In analog-to digital converters many decisions during a conversion process are performed. This phenomenon particularly common is in high-speed parallel-type converters. As soon as a wrong decision is made, the internal code is converted into a wrong output code. Sometimes the internal code can be a meta stable condition of a comparator. A meta stable code of a comparator is an output code level that does not confirm the logical levels for “1” or “0”. In such a case the conversion process from the internal code into the output code results in erroneous output codes. To obtain information about the error process the Bit Error Rate (BER) is defined. This figure defines the number of decision errors a converter makes. A high-quality analog-to-digital converter, for example, has BER numbers between  $10^{-10}$  and  $10^{-15}$ <sup>36</sup>.

### 2.8.1.2.4 Maximum Sampling Rate

The maximum sampling rate of a converter is difficult to define number. In some cases the reduction in dynamic range (S/N ratio) can be used to define the maximum sampling rate. A definition can be:

The maximum sampling frequency of a converter for which the dynamic range measured over the Nyquist bandwidth is reduced with 3 dB or 0.5 bit.

This definition gives a rough indication about the maximum sampling frequency<sup>36</sup>.

### 2.8.1.2.5 Settling Time

The settling time of a system is defined as the time needed from the start of a transition until the time the output reaches the new value within the specified accuracy. The settling time specification of the full step of a digital-to-analog converter is important for application of such a converter in a successive approximation analog-to-digital converter configuration<sup>36</sup>.

## 2.8.2

### Different Types of A/D Converters Based on Digital Circuits

Architectures for the realization of A/D converters can be roughly divided into three categories (Table 3) – low-to-medium speed, medium speed, and high speed. All converters presented in the following three subchapters use digital circuitry, including clocks. It is necessary to have a basic understanding how conventional digital voltage-mode A/D converters work in order to understand the changes to analog current-mode A/D converters presented in this thesis in chapters 4 and 5.

**Table 3:** Different A/D converter architectures.

Low-to-Medium Speed, High Accuracy	Medium Speed, Medium Accuracy	High Speed, Low-to-Medium Accuracy
Integrating Oversampling	Successive approximation Algorithmic	Flash Two-step Interpolating Folding Pipelined Time-interleaved

### 2.8.2.1

#### Low-to-Medium Speed A/D Converters

Integrating A/D converters are required for realizing high-accuracy data conversion when very slow moving signals are the signal source. They are known to have very low offset and gain errors and are highly linear. A further advantage of this type of converter is that they occupy only a very small amount of circuitry in their implementation. One application that has traditionally made use of integrating converters is measurement instruments such as voltage or current meters. In this context, the most common converter of its class will be introduced: the *dual-slope* converter. A simplified diagram for a dual-slope integrating converter is shown in Figure 11. Dual-slope refers to this converter performing its conversion in two phases, phase (I) and phase (II), in the following manner:

**Phase (I)** Phase (I) is a fixed time interval of length  $T_1$  determined by running the counter for  $2^N$  clock cycles. Thus, we have

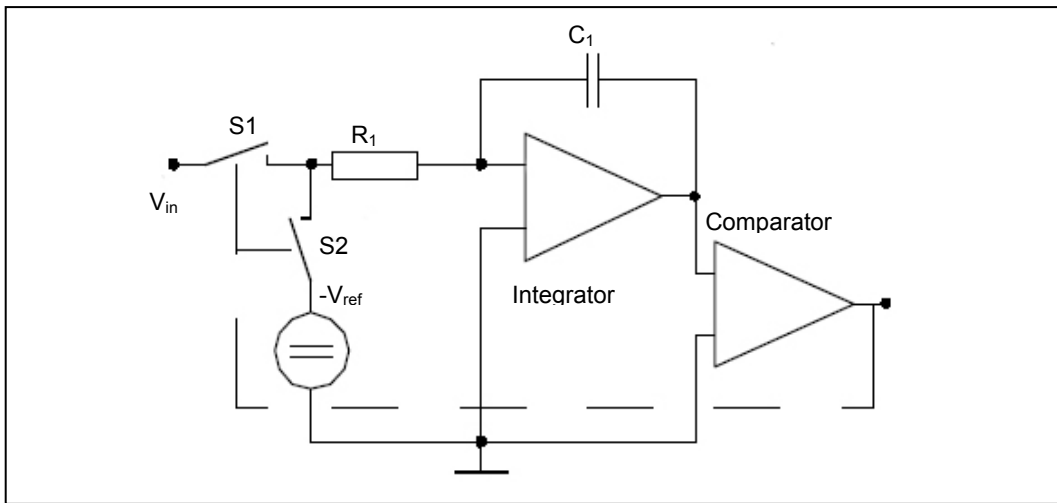
$$T_1 = 2^N T_{clk}$$

**Equation 26:** Time interval length for a dual-slope converter.

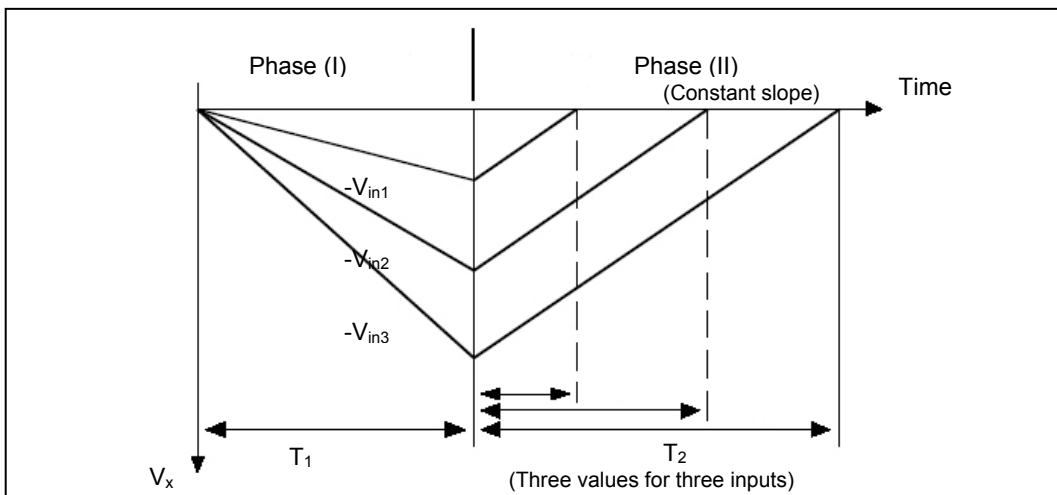
where  $T_{clk}$  is the period for one clock cycle. During this interval, the converter integrates the input signal.

**Phase (II)** Phase (II) occurs for a variable amount of time,  $T_2$ , as shown in Figure 12 for three different input voltages. At the beginning of this phase, the counter is reset and switch  $S_1$  is connected to  $-V_{ref}$ , resulting in a constant slope for the decaying voltage at  $V_x$ . To obtain the digital output value, the counter simply counts until  $V_x$  is less than zero, at which point that count value equals the digitized value of the input signal,  $V_{in}$ .

The dual-slope converter combines little construction complexity with high accuracy and linearity. Its accuracy is mainly limited through the capacitor's dielectric capacity for remembering. This causes the capacitor failure to release all the charge when it is discharged. Without this effect, in the range of  $10^{-5}$ , much better accuracy would be possible.



**Figure 11:** Integrating (dual-slope) A/D converter.



**Figure 12:** Operation of the integrating converter for three different input voltages.

### 2.8.2.2

#### Medium Speed A/D Converters

A second category of A/D converters is classified as medium-speed A/D converters. This class of A/D converters converts an analog input into an  $N$ -bit digital word in approximately  $N$  clock cycles. Consequently, the conversion time is less than that of the slow-to-medium converters. A representative for its class is the *algorithmic* A/D converter which is based on digital circuitry and voltage-mode operation (see Chapter 3, “*Current-Mode Algorithmic ADC*”). The *successive-approximation* converter is also part of this category, however it is omitted here and additional information can be found in <sup>37</sup>.

<sup>37</sup> R. van de Plassche. *Integrated Analog-to-Digital and Digital-to-Analog Converters*. Kluwer Academic Publishers, 1 edition, Netherlands, 1994.

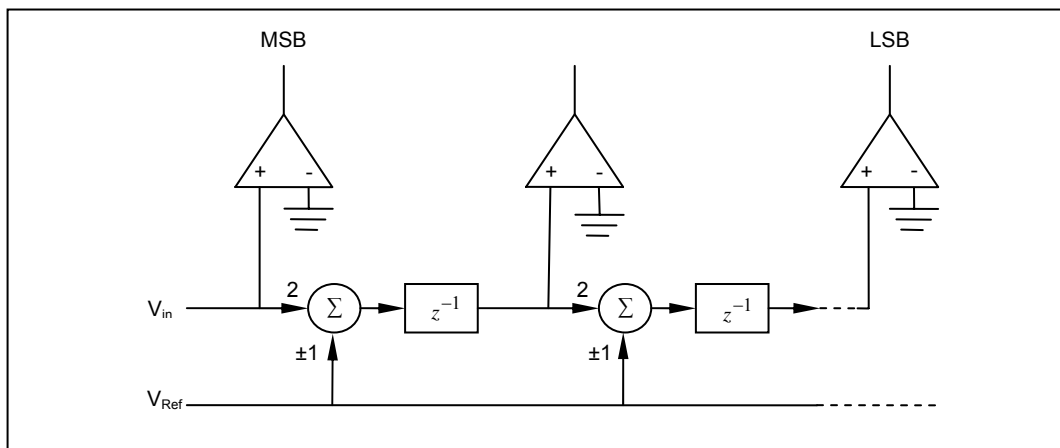
An  $N$ -bit algorithmic A/D converter, as shown in Figure 13, consists of  $N$  stages and  $N$  comparators for determining the signs of the  $N$  outputs. Each stage takes its input, multiplies it by two and adds or subtracts the reference voltage depending upon the sign of the previous output. The comparator outputs form an  $N$ -bit digital representation of the analog input (thermometer code) to the first stage.

The algorithmic A/D converter shown in Figure 13 may be reduced iteratively. The analog output of the  $i$ th stage can be expressed as

$$V_{oi} = [2V_{o,i-1} - b_i V_{\text{Ref}}] \cdot Z^{-1}$$

**Equation 27:** Analog output of an algorithmic A/D converter.

Where  $b_i$  is +1 if the  $i$ th-bit is 1 and -1 if the  $i$ th-bit is 0. This equation can be implemented with the circuit in Figure 14. It also incorporates the ability to sample and hold a voltage at the start of the conversion.

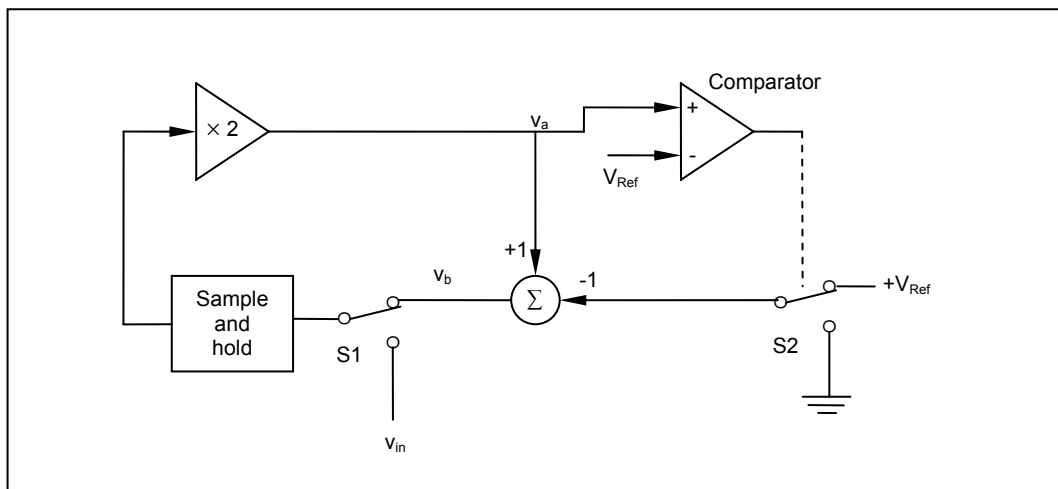


**Figure 13:** Pipeline implementation of the algorithmic A/D converter.

The algorithmic A/D converter has the disadvantage that the time needed to convert a sample is  $N$  clock cycles, although one complete conversion can be obtained in one clock cycle. The algorithmic A/D converter is considered to be ratio-independent because the performance does not depend upon the ratio accuracy of a capacitor or resistor array. The accuracy of the multiplication by two, of the algorithmic A/D converter, must be accurate to within 1 LSB<sup>38</sup>.

<sup>38</sup> P. E. Allen, D.R. Holberg. *CMOS Analog Circuit Design*, pp. 565-569, Oxford University Press Inc., Oxford, 1 edition, 1987.





**Figure 14:** Implementation of the iterative algorithmic A/D converter.

### 2.8.2.3

#### **High-Speed A/D Converters**

In many applications, it is necessary to have a smaller conversion time than is achievable with the A/D converter architectures presented so far. This has led to the development of high-speed A/D converters that use parallel techniques to achieve short conversion times. The ultimate conversion time is one clock cycle, which would typically consist of a set-up and convert phase.

The best known architecture for a high-speed A/D converter is the flash or parallel converter. Similar to the dual-slope and the algorithmic converter it also works in voltage mode, employing digital circuitry and a clock to realize the conversion process. Its structure consists of an array of comparators which compare the input voltage with a set of increasing reference voltages. In an  $N$ -bit flash analog-to-digital converter,  $2^N - 1$  reference voltages and comparator stages are used to convert the analog input signal into a thermometer-like digital output code. This code normally is then converted by an encoder or a ROM structure into a binary output code. An example of this type of converter is presented in Figure 15. It is a 3-bit, parallel A/D converter, dividing  $V_{Ref}$  into eight values, as indicated in the figure. Each of these values is applied to the positive terminal of a comparator. The outputs of the comparators are taken to a digital encoding network that determines the digital output word from the comparator outputs. Many versions of this basic concept exist. For example, the resistor string may be connected between  $+V_{Ref}$  and  $-V_{Ref}$  to achieve bipolar conversion.

The flash architecture shows a good speed performance and can easily be implemented in an integrated circuit as a repetition of simple comparator blocks and an encoder structure. However, this architecture requires  $2^N - 1$  comparators to achieve an  $N$ -bit resolution. The parallel structure makes it difficult to obtain high-resolution while maintaining at the same time low power consumption and a small die area. In today's technology, 8-bit converters with a reasonable die size and which consume moderate power are available. Increasing the resolution to 10 bits increases the die size and power consumption roughly four times. In practice, however, there is a limit to the power dissipation that can be handled in IC packages.

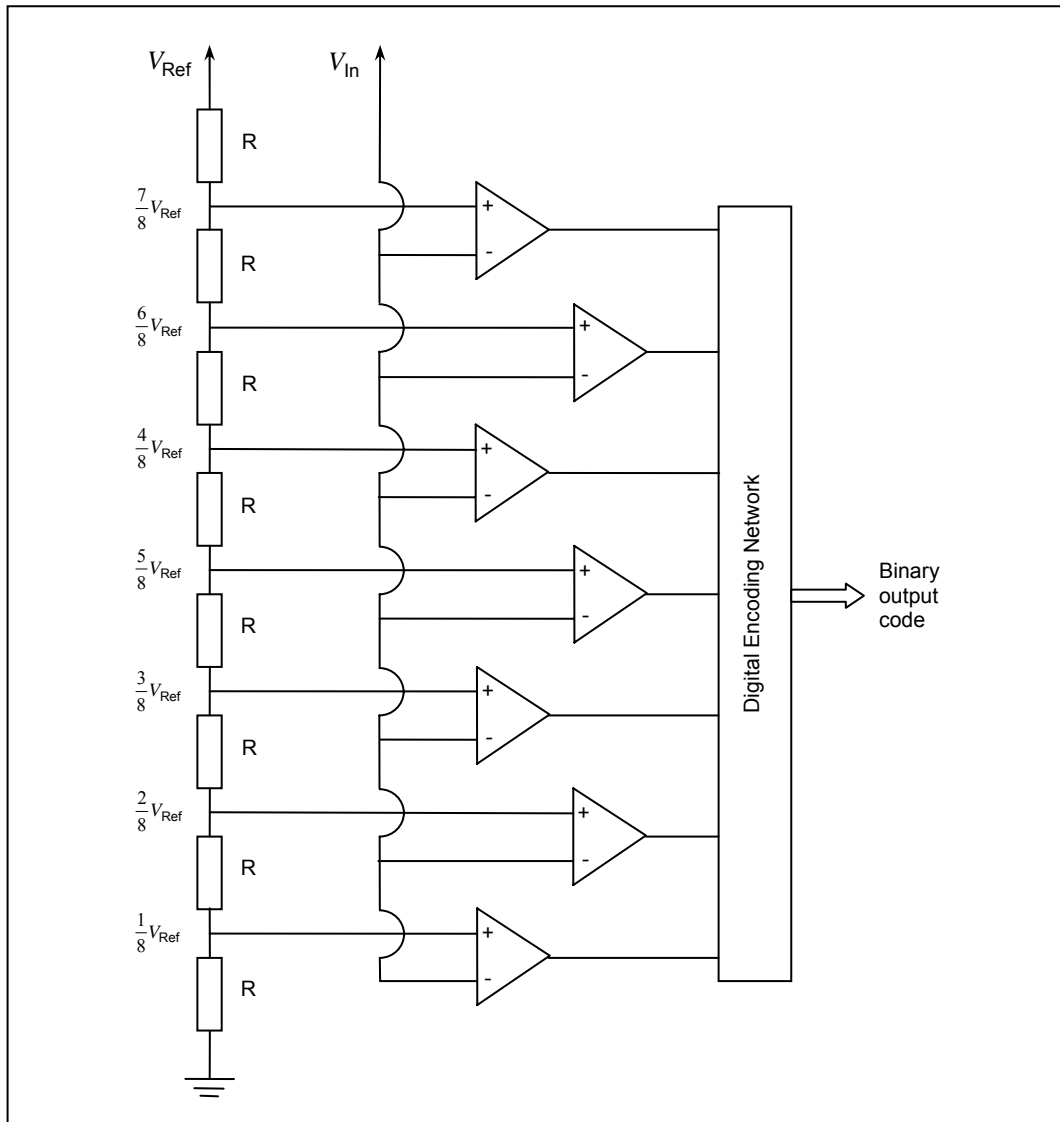


Figure 15: A 3-bit, parallel analog-to-digital converter.

## 2.9

### Summary

The current chapter served as an introduction to the methods and techniques used for the research which led to this thesis. Beginning with the basics of CMOS VLSI analog technology to the operation principles of current-mode circuits, a wide spread area was covered. In the last section of chapter 2, conventional analog-to-digital conversion techniques were discussed, including the explanation of A/D specification terms.

## 3 Current-Mode Algorithmic ADC and Previous Design

### 3.1

#### Introduction

The design of an A/D converter which makes use of the current-mode technique is fairly new. There are a couple of useful applications which make use of a fully integrated VLSI converter, accepting currents as its input signal. The related work of this thesis, the *Artificial Synapse*, requires something even more sophisticated: To perform computations within the analog chip, so called  $\alpha$ -amino-3-hydroxy-5-methyl-4-isoxazole propionic acid (AMPA) receptor ion channels need to be turned on and off. Synaptic strength is encoded by the number of discrete channels which are activated at a time. The signals required to turn these channels on or off have to be digital. Consequently, a transition from analog signals to digital signals is inevitable, and therefore an A/D converter is needed. Since it is a biologically inspired system with the necessity to operate at low power levels, clocks can not be used because they draw too much power and do not reflect the biological environment.

Another characteristic of the system is its operation in subthreshold domain. For this reason, the analog-to-digital converter used within the system has to operate in subthreshold regime. A problem with subthreshold circuits is that systems operating in this mode are both low power and slow. Consequently, the need for a subthreshold current-mode A/D converter is due to the specifications which postulate energy efficiency. However, they have to deal with the drawback of being slower than other solutions.

### 3.2

#### Nairn's and Salama's Current-Mode Algorithmic Analog-to-Digital Converter

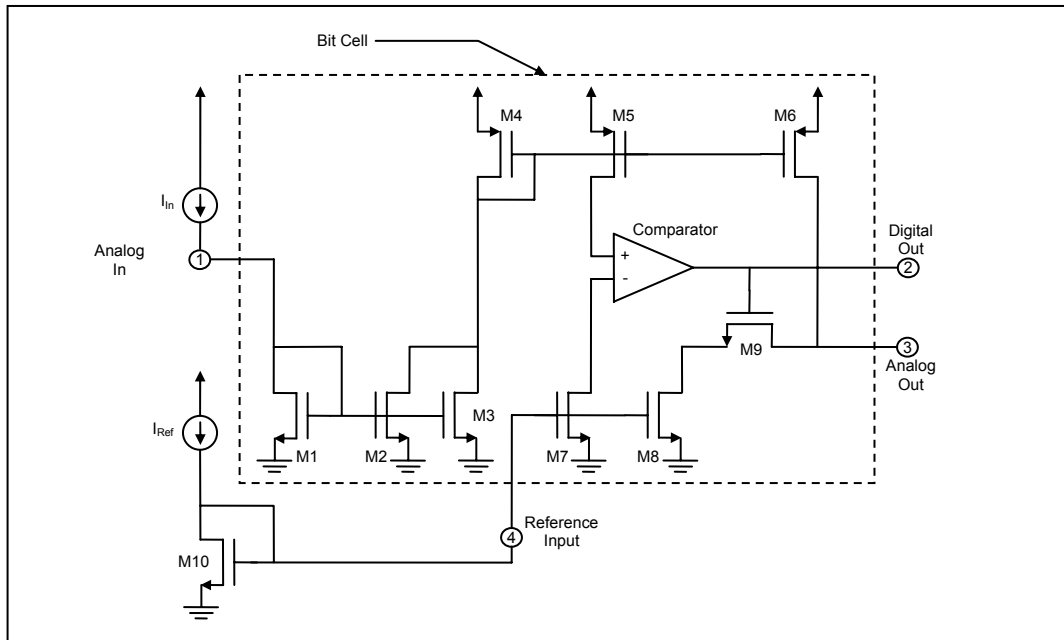
In this subchapter the principle of operation of a current-mode algorithmic ADC will be described. First the focus lies on the principle of operation for only one single bit cell, and then we will move on to a cascade of these bit cells, making up a whole ADC system like the one which was first introduced by Nairn and Salama, 1990<sup>39</sup>.

#### 3.2.1

##### 1-Bit Algorithmic Conversion

The circuit shown in Figure 16 performs a 1-bit algorithmic analog-to-digital conversion in the following manner. The input current  $I_{in}$  is first multiplied by two using the current mirror composed of  $M1$ ,  $M2$ , and  $M3$ . Following the multiplication, the signal  $2I_{in}$  is mirrored from  $M4$  through  $M5$  to the comparator, COMP1, and through  $M6$  to the output. COMP1 is used to compare  $2I_{in}$  (from  $M5$ ) with  $I_{Ref}$ , the reference current (from  $M7$ ). If  $2I_{in}$  is less than  $I_{Ref}$ , the digital output goes low and  $M9$  remains off, resulting in an output current of  $2I_{in}$  (from  $M6$ ). In contrast, if  $2I_{in}$  exceeds  $I_{Ref}$ , the digital output will be high causing  $M9$  to

be on. With  $M9$  on,  $I_{Ref}$  (from  $M8$ ) will be subtracted from  $2I_{in}$  (from  $M6$ ) resulting in an output current of  $2I_{in} - I_{Ref}$ . This completes the 1-bit algorithmic conversion<sup>39</sup>.



**Figure 16:** A bit cell implements a 1-bit algorithmic conversion.

### 3.2.2

#### ***N*-Bit Converter**

To produce an  $N$ -bit converter,  $N$  bit cells are cascaded with the analog output of one cell connected to the analog input of the following cell. The arrangement is illustrated in Figure 17. Transistor  $M10$  is shared by all bit cells. The resulting linear sequence of bit cells does not require control signals. Therefore, this configuration will result in a very compact circuit that can be easily modified for different resolutions<sup>39</sup>.

<sup>39</sup> D. G. Nairn and C. A. Salama. Current-Mode Algorithmic Analog-to-Digital Converters. IEEE Journal of Solid-State Circuits, Vol. 25, No. 4, August 1990.

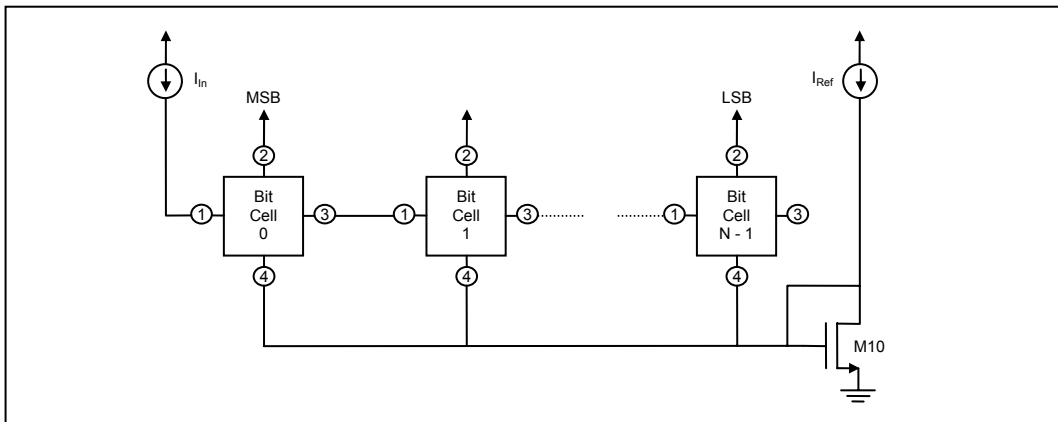


Figure 17: Cascade of bit cells for an  $N$ -bit converter.

### 3.2.3

#### Current Comparator

The algorithmic current-mode ADC is composed of current comparators and current mirrors. Due to the need for  $N$  comparators, and  $2N$  current mirrors for an  $N$ -bit ADC, these components should be made as small as possible without sacrificing the accuracy of the overall converter.

An appropriate current comparator can be implemented using the inverter cascade shown in Figure 18. Although a converter of this type will display a poor power supply rejection ratio (PSRR) when used as a voltage comparator, this problem is not significant when the circuit is used as a current comparator. The first inverter in this circuit operates as an integrating current-to-voltage converter, hence effectively filters out the power supply noise. At the same time the integrating nature of the comparator ensures that there is no inherent DC offset in the comparator. Consequently, the inverter cascade provides a simple, small, and effective current-to-voltage converter / comparator<sup>39</sup>.

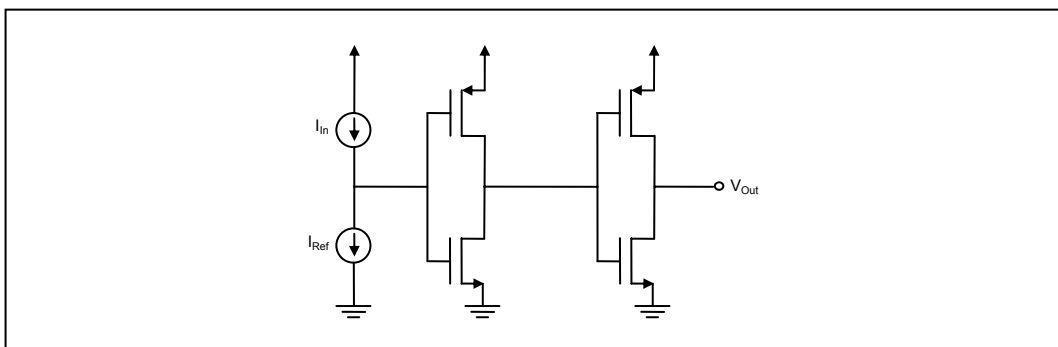
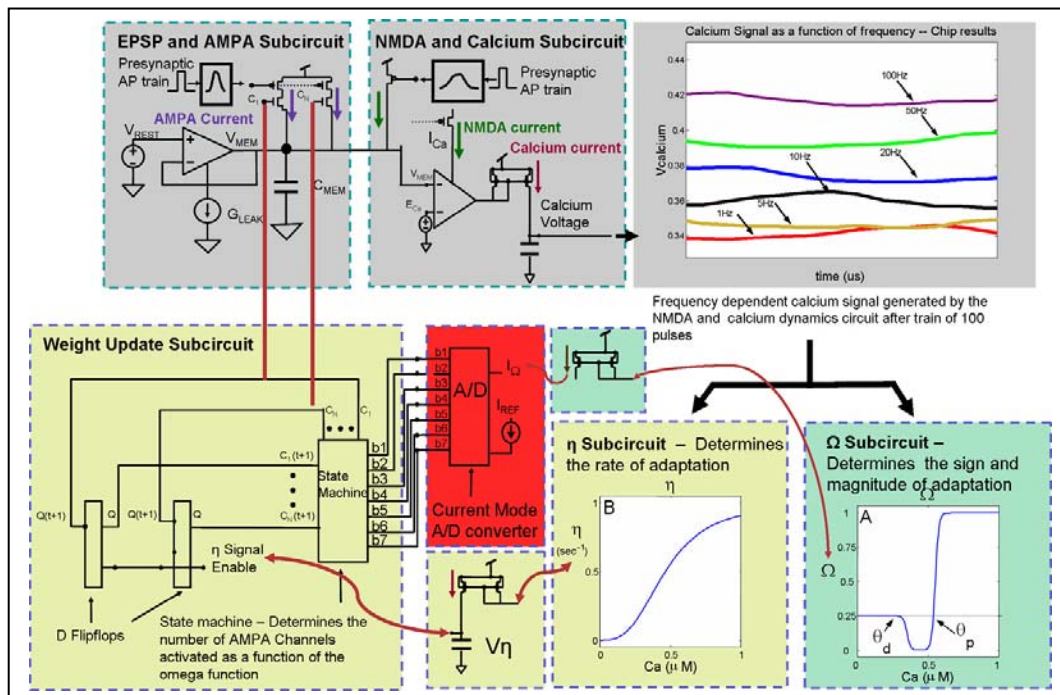


Figure 18: Basic current comparator.

### 3.3 Previous A/D Converter

The previous A/D converter used in the *Artificial Synapse* was based on the circuit introduced in chapter 3.2. It was adjusted for usage in subthreshold regime by the doctoral student G. Rachmuth, as shown in section 3.3.1. He developed this first approach of an analog current-mode VLSI subthreshold analog-to-digital converter as part of his doctoral thesis at the Harvard-MIT Division of Health Sciences & Technology (HST). A pictograph of the artificial synapse chip design is shown in Figure 19.



**Figure 19:** A/D converter in its context, an in-silico model of *N*-methyl-*D*-aspartate (NMDA) and non-NMDA receptor activities using analog VLSI circuits. The converter is highlighted in red color.

During the initial stages of this project, the A/D converter which was used behaved abnormally. The voltage levels of the output bits were oscillating when they should have remained at one constant DC level, the input sensitivity was rather exponential than linear. In addition, the linearity of the converter itself was nonlinear in theory as well as in SPICE simulations. Another issue was the form of the output code produced by the converter, which led to a thermometer code. All these faults were corrected during the research for this Diploma Degree thesis. In section 3.4 the research will be presented which was carried out analyzing and testing the previous A/D design, whereas in chapters 4, 5, and 6, the A/D designs and an encoder design which are subject of this thesis will be shown.

#### 3.3.1 Adjustment for Subthreshold Operation

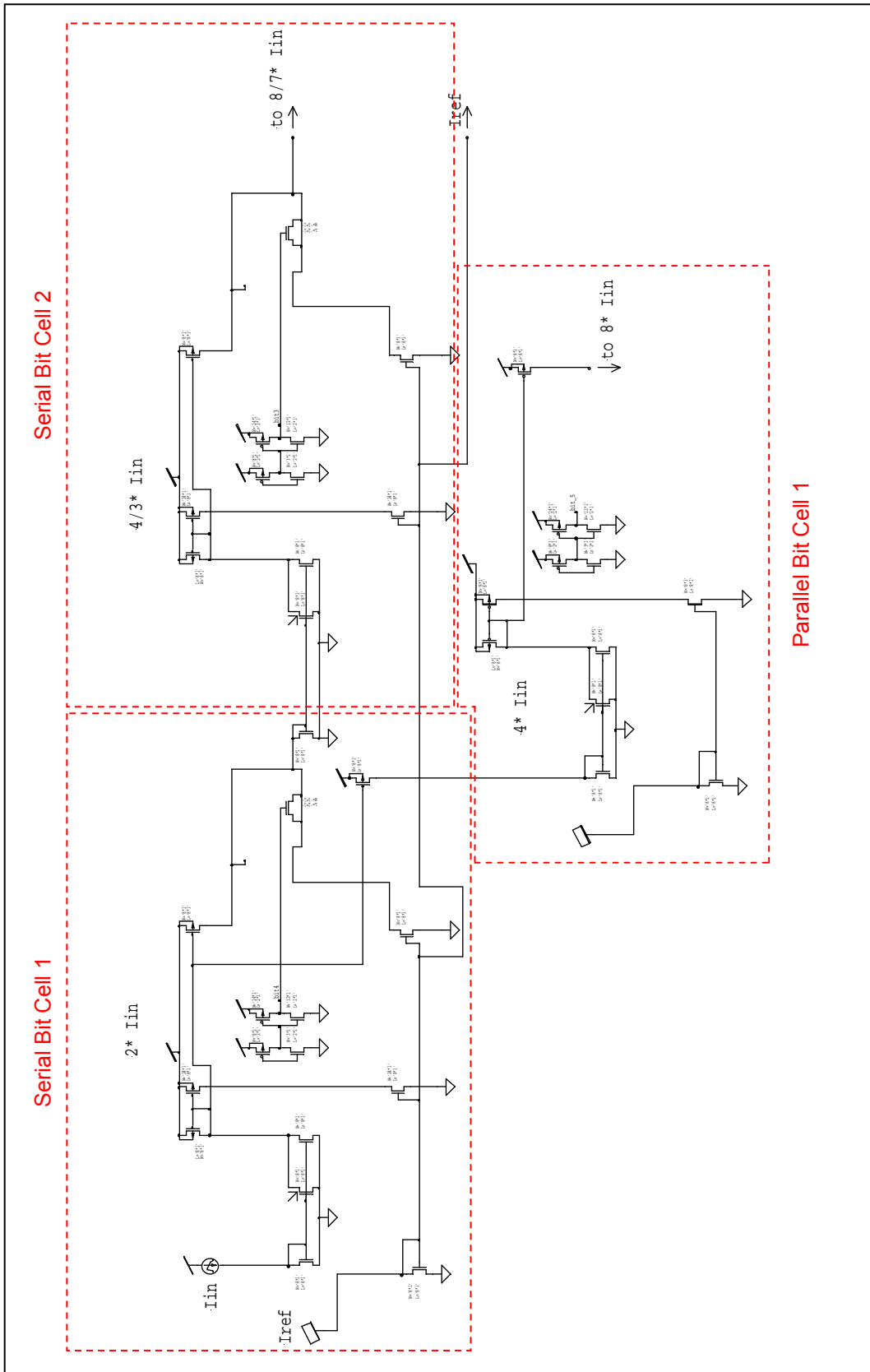
The original design of the current-mode ADC bit cell (Nairn and Salama, 1990) shown in Figure 16 uses the digital state of the digital out signal (which is output Nr. (2) in the sche-

matic of Figure 16) to turn the pass transistor  $M_9$  either on or off. This results in  $I_{in} - I_{Ref}$  either being transferred to the next bit cell or not. For retrospection: if the output of the comparator is a 0, the next bit cell will only receive  $I_{in}$ . G. Rachmuth encountered the following problem when trying to transcribe the design into subthreshold regime and operating it at a power supply voltage of less than 1.5V: pass transistor  $M_9$  proved to create transients which could not be suppressed. By eliminating the pass transistor, the transients could be removed. This is due to the fact that  $M_9$  caused a third diode drop in the chain of transistors in the  $V_{DD}$  to ground (GND) path. However, eliminating  $M_9$  led to new problems. Firstly, it changes the whole principle of operation of the algorithmic conversion principle, which means that the modified converter will need  $N$  bit cells to achieve  $N$  bit of thermometer code. Secondly, it decreases the number of bit cells which can be realized in the cascade of bit cells used to form the current-mode ADC. Section 3.3.2 discusses how the mentioned problems were treated.

### 3.3.2

#### Serial-Parallel Design

The system was expanded to include bit cells which were in parallel with the cascade of bit cells arranged in a serial pattern. This effectively increased the number of digital output bits that could be obtained. Figure 20 shows a schematic drawing of the final design which was implemented on a chip and subsequently analyzed and tested for this thesis research. Note that pass transistor  $M_9$  was omitted in the design.



**Figure 20:** Schematic of the serial-parallel A/D design, showing two serial bit cells and one parallel bit cell.



### 3.3.3

#### Function Principle

Firstly, it was investigated how the conversion of this A/D converter approach works in theory. The converter is, as shown in section 3.3.2, made up of a serial stage and a parallel stage. In the serial processing stage, the input of the bit cell  $I_{in}$  is multiplied by two and then the reference current  $I_{Ref}$  is subtracted. Is the result of this calculation bigger than zero, the corresponding bit cell will go on high level (true). Accordingly, when the result is less than zero, it will remain on the low level (false). For a seven bit thermometer code A/D converter (complies with three bit binary code), the truth table looks like this:

#### Serial Processing

<b>Bit 4:</b>	If $(2^* I_{in} - I_{Ref}) > 0$	→ true
	Else	→ false
<b>Bit 3:</b>	If $(2^* (2^* I_{in} - I_{Ref}) - I_{Ref}) > 0$	→ true
	Else	→ false
<b>Bit 2:</b>	If $(2^* (2^* (2^* I_{in} - I_{Ref}) - I_{Ref}) - I_{Ref}) > 0$	→ true
	Else	→ false
<b>Bit 1:</b>	If $(2^* (2^* (2^* (2^* I_{in} - I_{Ref}) - I_{Ref}) - I_{Ref}) - I_{Ref}) > 0$	→ true
	Else	→ false

With algebraic transformation this can be simplified to:

<b>Bit 4:</b>	If $I_{in} > \frac{1}{2} I_{Ref}$	→ true
	Else	→ false
<b>Bit 3:</b>	If $I_{in} > \frac{3}{4} I_{Ref}$	→ true
	Else	→ false
<b>Bit 2:</b>	If $I_{in} > \frac{7}{8} I_{Ref}$	→ true
	Else	→ false
<b>Bit 1:</b>	If $I_{in} > \frac{15}{16} I_{Ref}$	→ true
	Else	→ false

In the parallel stage of the converter, the input current  $I_{in}$  is doubled from one bit cell to the next cell, followed by the subtraction of  $I_{Ref}$ . For the seven bit converter from the previous example, this can be described as follows:

#### Parallel Processing

<b>Bit 5:</b>	If $(4^* I_{in} - I_{Ref}) > 0$	→ true
	Else	→ false
<b>Bit 6:</b>	If $(8^* I_{in} - I_{Ref}) > 0$	→ true
	Else	→ false

**Bit 7:** If  $(16 \cdot I_{\text{In}} - I_{\text{Ref}}) > 0$  → true  
 Else → false

Again, this can be simplified through algebraic transformation:

**Bit 5:** If  $I_{\text{In}} > \frac{1}{4} I_{\text{Ref}}$  → true  
 Else → false

**Bit 6:** If  $I_{\text{In}} > \frac{1}{8} I_{\text{Ref}}$  → true  
 Else → false

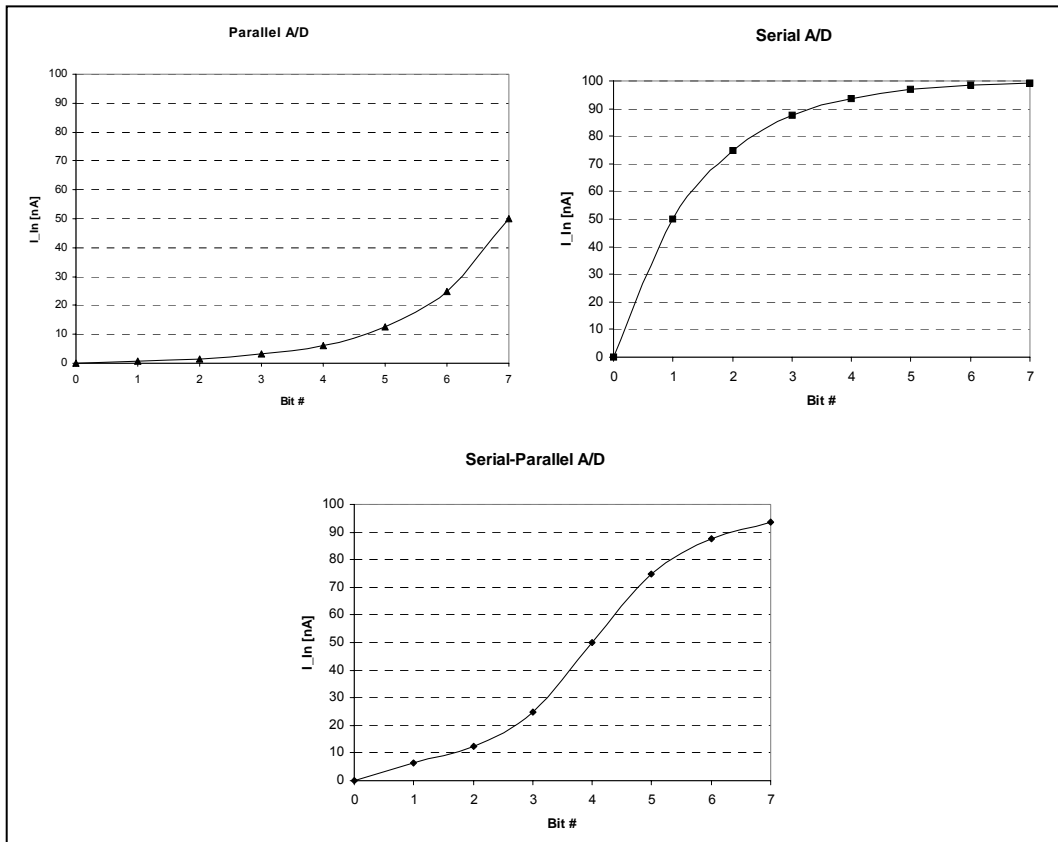
**Bit 7:** If  $I_{\text{In}} > \frac{1}{16} I_{\text{Ref}}$  → true  
 Else → false

### 3.3.4

#### Nonlinearity Issues

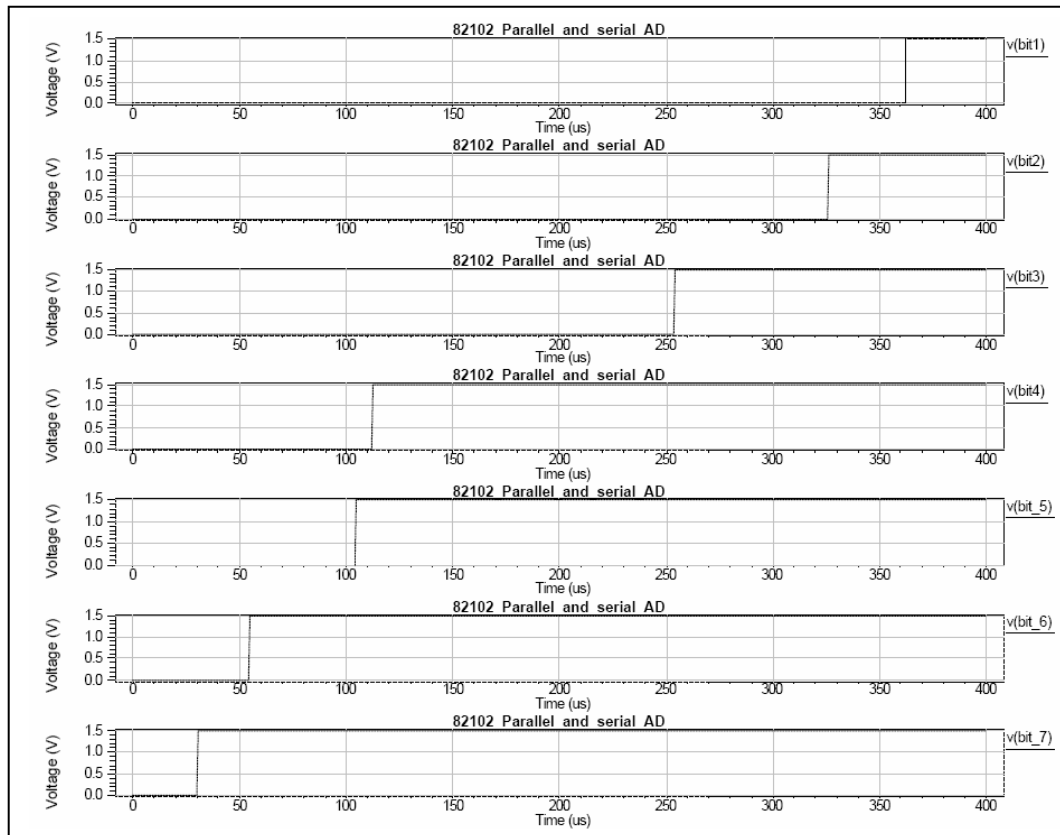
In Figure 21, you can see a visual representation of the above conversion scheme. Note that the points on the graphs represent the current levels at which the corresponding bit changes its signal level from low to high. While the parallel stage shows an exponential pattern, the serial stage produces a more logarithmic shaped curve. Given that the converter is composed from a serial and a parallel stage (bit 1 – bit 4 are serial, bit 5 – bit 7 are realized with parallel bit cells), the two curves are amalgamated together at the junction of Bit 4 and 5. This leads to an S-shaped conversion character, shown in Figure 21 in the lower graph.

In the background chapter describing the ideal analog-to-digital converter and its ideal conversion characteristic (see 2.8.1.1.3), we have seen that this S-shaped line, called the transfer curve, should be shaped straight (see Figure 10). This would allow a linear transformation of analog current levels into a binary encoded digital output word.



**Figure 21:** Visualized conversion schemes of the serial-parallel A/D converter. Top left: Parallel alignment theoretical conversion scheme; Top right: Serial alignment theoretical conversion scheme; Bottom: Combined parallel-serial converter conversion scheme.

Figure 22 is extracted from the program *W-Edit* which is part of the Tanner SPICE development suite. It shows the simulation results of the circuit shown in Figure 20. The simulation was run for 520 $\mu$ s using 100nA as a reference current ( $I_{Ref}$ ) and by rising the input current ( $I_{in}$ ) from 0 to 100nA. Consequently, if it was about an ideal A/D converter, the positions at which bit 1 – bit 7 change their signal levels from 1V to 1.5V (which is equivalent to low and high or true and false respectively) should be equidistant, forming a linear transfer curve. Instead we see, as already predicted by calculation, the bit switch positions grouping around the beginning and the end of the current input range. This verifies the S-shaped transfer curve in terms of simulation aspects of the circuit.



**Figure 22:** Simulation results of the parallel-serial design using T-SPICE. The graph shows bit 1 – bit 7,  $I_{in}$  was a continuously increasing current (from 0 to 100nA).

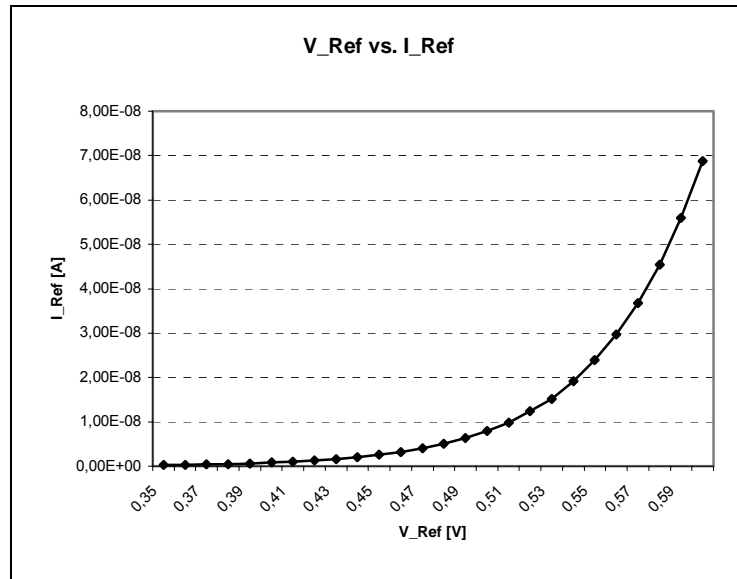
### 3.3.5

#### Exponential Input Sensitivity

After analysis of the existing circuit of the previous A/D design, attention was focused on the behavior of the input sensitivity of the  $I_{Ref}$  port. It was conspicuous that small changes of the input voltage, which gets converted into a current using a special voltage-current converter circuit, led to huge changes of the  $I_{Ref}$ . On closer inspection of the A/D circuit schematic, it became apparent that the reference current wasn't mirrored to the comparator of each bit cell – it was simply connected in parallel.

Tests on the original converter determined that there was an exponential coherence between the input voltage and the reference current which is connected to the comparator input in each cell. This is because a transistor in subthreshold regime has an exponential dependence of the drain-source current compared to the gate voltage respectively the gate potential. In Figure 23 the exponential dependence is shown in a graph. To its left, you find a table which was used for adjustments of the desired current level by looking it up in the table. This is a convenient and easy way to manipulate the current level indirectly.

$V_{Ref}$ [V]	$I_{Ref}$ [A]
0,35	2,48E-10
0,36	3,08E-10
0,37	3,95E-10
0,38	4,99E-10
0,39	6,30E-10
0,4	7,97E-10
0,41	1,00E-09
0,42	1,27E-09
0,43	1,60E-09
0,44	2,02E-09
0,45	2,54E-09
0,46	3,20E-09
0,47	4,03E-09
0,48	5,05E-09
0,49	6,28E-09
0,5	7,88E-09
0,51	9,87E-09
0,52	1,23E-08
0,53	1,52E-08
0,54	1,92E-08
0,55	2,39E-08
0,56	2,97E-08
0,57	3,68E-08
0,58	4,54E-08
0,59	5,59E-08
0,6	6,88E-08



**Figure 23:**  $I_{Ref}$  versus  $V_{Ref}$ . To apply a certain input current to the previous A/D converter, it is necessary to adjust the input voltage according to this current-voltage conversion. It follows an exponential function and was generated by using the dataset shown in the table to the left.

### 3.4

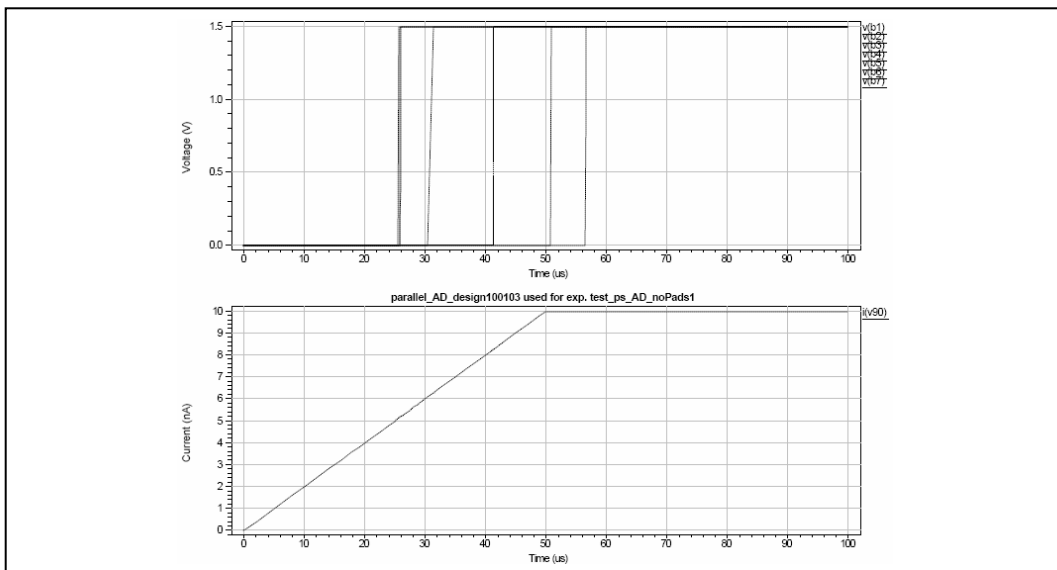
#### Experiments with the Previous A/D Converter

In this section, the experiments which were carried out prior to investigating the novel A/D design approaches will be explained and discussed. It turned out to be help understanding the problems behind the project and gave the opportunity to learn how measurements can be made at current levels of only a few nano amperes (nA).

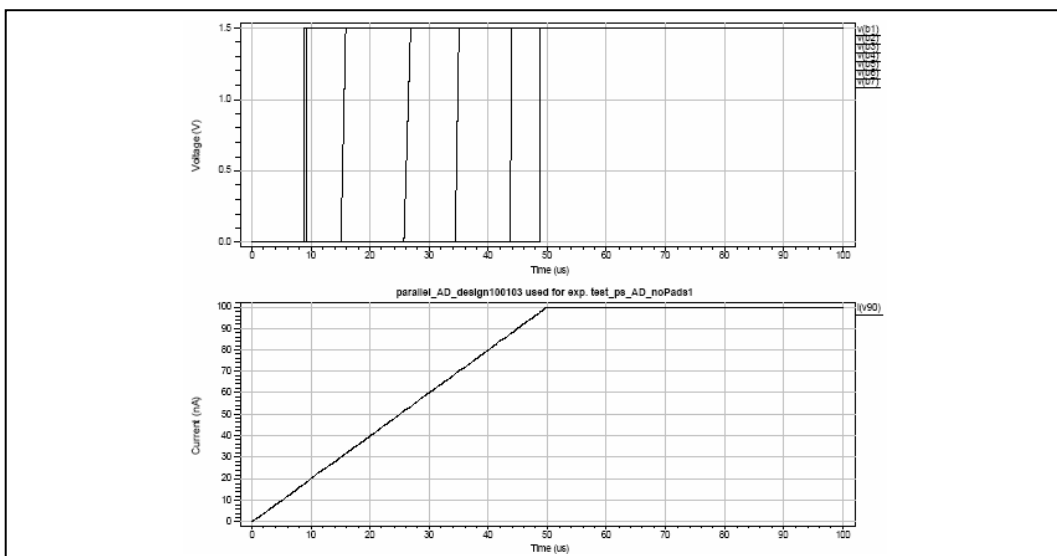
### 3.4.1

#### SPICE Simulation Results

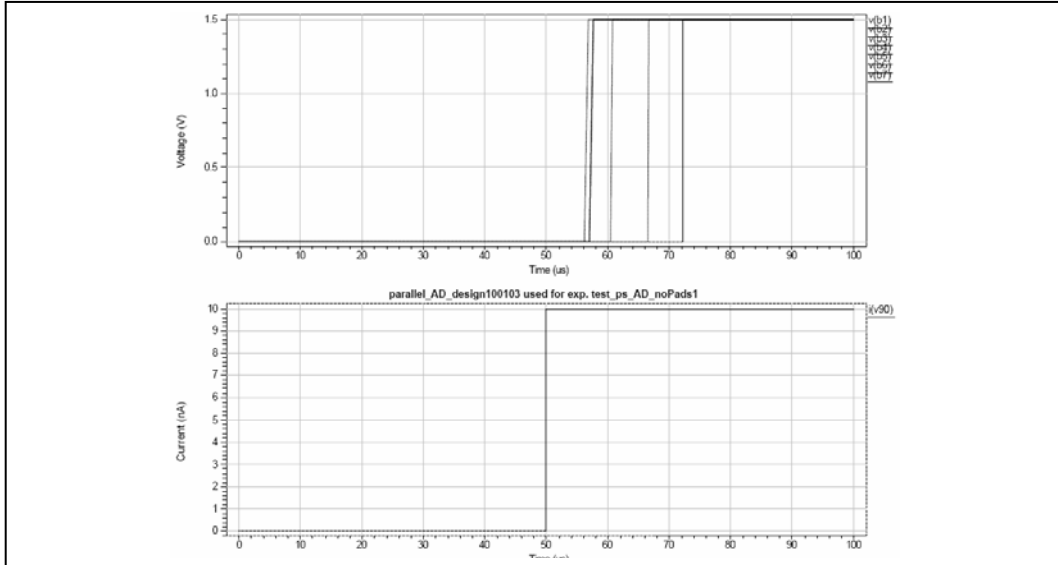
Figure 24 – Figure 27 show the simulation results of the serial-parallel design. All SPICE simulations were performed using Tanner Reasearch’s *SPICE Development Kit (T-SPICE Pro v9.02, S-Edit v8.1 and W-Edit v9.02)*. BSIM3 transistor models, provided by the MOSIS manufacturing service, were used to emulate the transistor properties for the technology which was used for the chip fabrication. While Figure 24 and Figure 26 show the behavior of the circuit using an input range of 0 – 10nA, Figure 25 and Figure 27 were taken using an input range of 0 – 100nA. As you can see, the higher currents result in a faster response of the converter. This is especially apparent in the simulations which use a square wave.



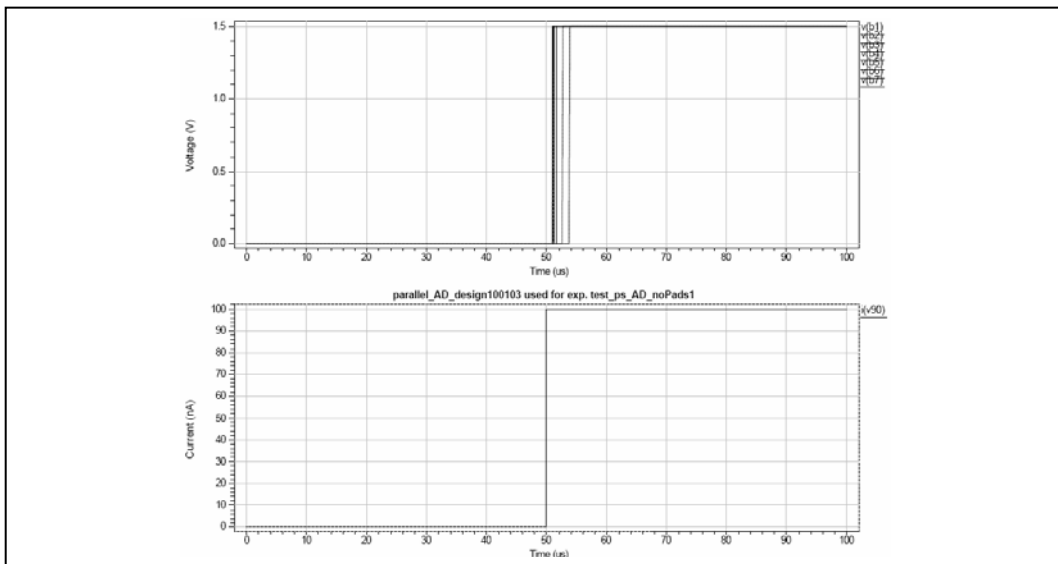
**Figure 24:** T-SPICE simulation of serial-parallel converter with constant  $I_{Ref} = 10\text{nA}$  and  $I_{in}$  rising from 0 to 10nA. The simulation period displayed is  $100\mu\text{s}$  long.



**Figure 25:** T-SPICE simulation of serial-parallel converter with constant  $I_{Ref} = 100\text{nA}$  and  $I_{in}$  rising from 0 to 100nA. The simulation period displayed is  $100\mu\text{s}$  long.



**Figure 26:** T-SPICE simulation of serial-parallel converter with constant  $I_{Ref} = 10\text{nA}$  and a pulse of  $I_{In} = 10\text{nA}$  at  $t = 50\mu\text{s}$ . The conversion time with these parameters is  $\Delta x = 22.35 \mu\text{s}$ . The simulation period displayed is  $100\mu\text{s}$  long.



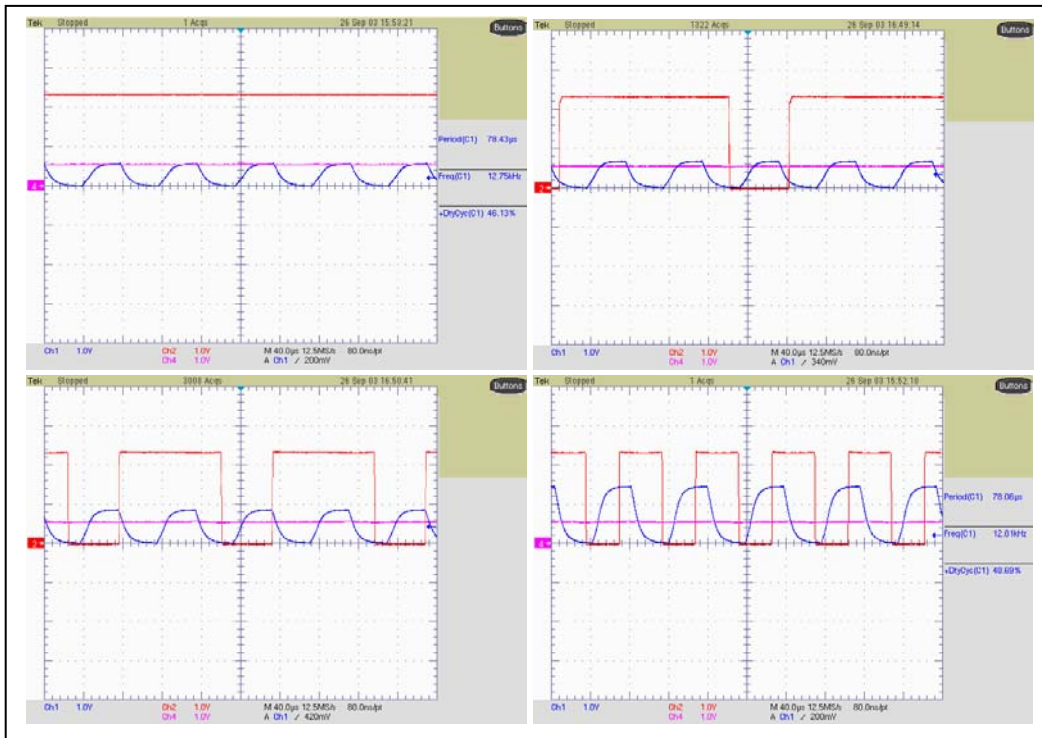
**Figure 27:** T-SPICE simulation of serial-parallel converter with constant  $I_{Ref} = 100\text{nA}$  and a pulse of  $I_{In} = 100\text{nA}$  at  $t = 50\mu\text{s}$ . The conversion time with these parameters is  $\Delta x = 3.92 \mu\text{s}$ . The simulation period displayed is  $100\mu\text{s}$  long.

In Figure 24 and Figure 25, which use a rising current as  $I_{In}$ , a conceptual problem of the previous design emerges: some bits are switching at the same time. This means that

the simulation results confirm the experimental findings. The parallel part of the converter expels an exponential behavior which causes the bits to switch nearly at the same time.

### 3.4.2

#### Experimental Results



**Figure 28:** Frequency measurement of bit 1 of the previous A/D design with  $V_{in}$  at 12.81 KHz (channel 1). By increasing the input voltage  $V_{in}$ , which is converted to  $I_{in}$ , the bit starts to oscillate. Measurements were made with a Tektronix TDS 5034 4-channel digital phosphor oscilloscope.

- Top left image:  $I_{in} = I_{ref}$  Bit doesn't oscillate → **FAIL!**
- Top right image:  $I_{in} > I_{ref}$  Bit oscillates, but only with every 3<sup>rd</sup> edge → **FAIL!**
- Bottom left image:  $I_{in} > I_{ref}$  Bit oscillates, but only with every 2<sup>nd</sup> edge → **FAIL!**
- Bottom right image:  $I_{in} \gg I_{ref}$  Bit oscillates as it should → **OK**

**Table 4:** Voltages used for measurements taken in Figure 28.

	Description	Top Left	Top Right	Bottom Left	Bottom Right
Ch1	$V_{in}$	580mV	610mV	810mV	1.4V
Ch2	Bit 1	2.3V	2.3V	2.3V	2.3V
Ch3	-	-	-	-	-
Ch4	$V_{Ref}$	580mV	580mV	580mV	580mV



## 3.5

### Conclusions

In this chapter the original design for the A/D converter, based on the design by Nairn and Salama, 1990, but converted for subthreshold operation, has been discussed. The serial-parallel design leads to an S-shaped conversion curve which was confirmed by both, simulations and experiments. The exponential input sensitivity of the system was demonstrated in a series of experimental tests. Finally, a series of DC and dynamic experiments were performed.

Although the idea of the converter works in theory, the system had problems when examined under experimental conditions. Due to the heavy bit oscillations and the exponential input sensitivity, it has proven to be unsuitable for its target application, the *Artificial Synapse*. Therefore, a new approach to find a converter that works has to be designed.

## 4 Subthreshold Current-Mode ADC based on Current Multiplication

### 4.1

#### Requirements and Goals

After having introduced the algorithmic A/D converter and the previous attempt to construct a current mode A/D converter which is capable of a resolution of only few nano amperes in chapter 3, this chapter introduces the designs which are subject of this thesis. To overcome the problems which were encountered with G. Rachmuth's design, several new designs were tried out using Tanner's SPICE development kit. The two most successful circuits found during the research will be discussed in this and in the following chapter.

### 4.2

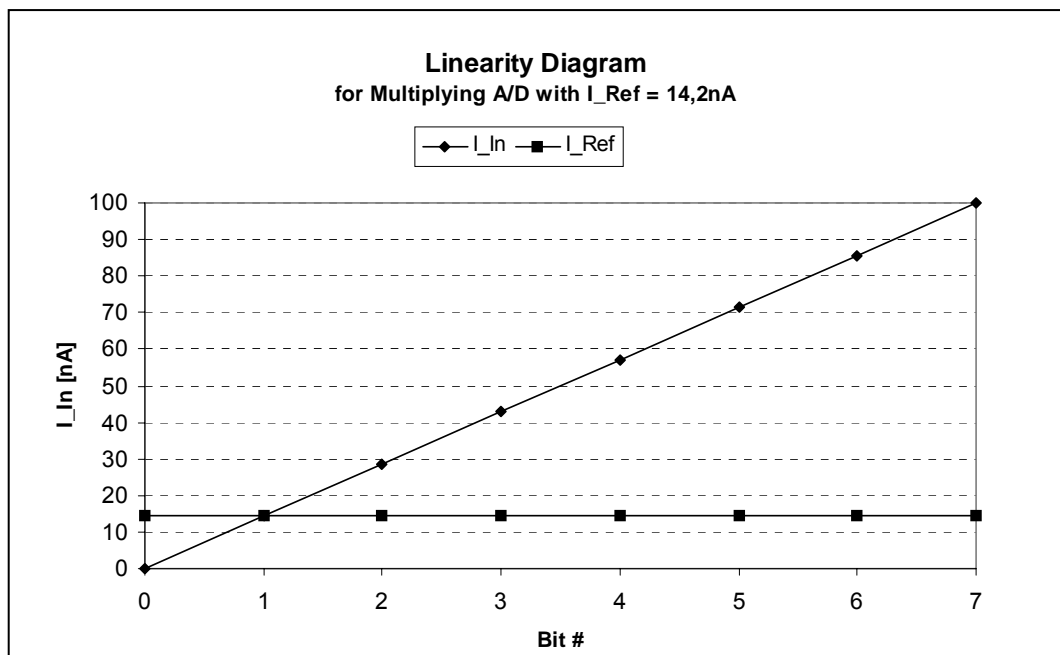
#### Principle of Operation

As the name of this approach suggests, its principle of operation is based on the technique of multiplying a reference current and afterwards comparing the product with the actual input current. Since the input current is directly compared to a stage of various products of reference currents, it leads to a linear conversion characteristic for the A/D converter. The principle is similar to a flash converter for voltage operation (see section 2.8.2.3), which directly compares a given input voltage to a stage of voltages. This stage of voltages is obtained by dividing the reference voltage into equal fractions through using a simple chain of resistors in which each resistor ideally should have exactly the same resistance.

Unlike in the voltage type flash converter, whose full scale input is  $V_{Ref}$ , this current mode converter has a full scale input of  $N * I_{Ref}$  where  $N$  is the number of bits in thermometer code representation. In the case of the converter which was built as the subject of this thesis, seven bit of thermometer code was required. Consequently, the least significant bit (LSB) of the converter is  $I_{Ref}$ , and the most significant bit (MSB) of it is  $7 * I_{Ref}$ . The principle of operation for all seven bits can be summarized as follows:

<b>Bit 1:</b>	If $(1 * I_{Ref}) > I_{In}$	→	high
	Else	→	low
<b>Bit 2:</b>	If $(2 * I_{Ref}) > I_{In}$	→	high
	Else	→	low
<b>Bit 3:</b>	If $(3 * I_{Ref}) > I_{In}$	→	high
	Else	→	low
<b>Bit 4:</b>	If $(4 * I_{Ref}) > I_{In}$	→	high
	Else	→	low
<b>Bit 5:</b>	If $(5 * I_{Ref}) > I_{In}$	→	high
	Else	→	low
<b>Bit 6:</b>	If $(6 * I_{Ref}) > I_{In}$	→	high
	Else	→	low
<b>Bit 7:</b>	If $(7 * I_{Ref}) > I_{In}$	→	high
	Else	→	low

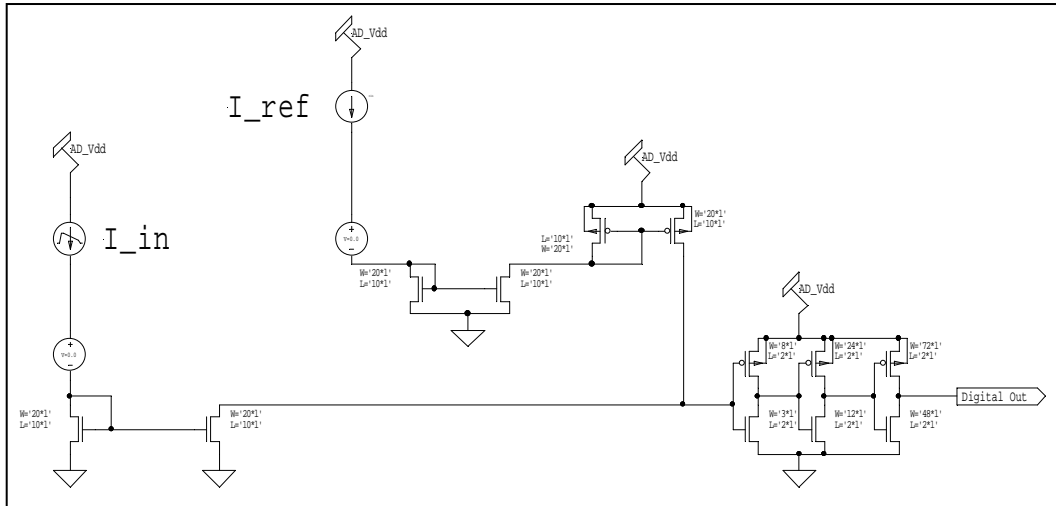
This new approach not only has the benefit of being linear, it also ensures a higher conversion rate. This is due to the fact that the current which is meant to be converted into a digital signal does not have to be transformed by multiplication cells. It rather is compared instantly after entering the converter by a comparator cell to the static  $I_{Ref}$  current.



**Figure 29:** In this figure, bit 1- 7 are supposed to switch at the positions marked with rhombus shaped markers. For an input current  $I_{In} = 14,2nA$ , bit one would switch at  $1 * 14,2nA$ , bit 2 at  $2 * 14,2nA$ , ... and bit 7 at  $7 * 14,2nA$ .

Figure 29 shows the ideal switching points of the comparators when a steadily increasing input current (ramp) is applied to the circuit. Note that the bit switching positions plotted on the X-axis of the diagram are equidistant to each other.

### 4.3 Schematics



**Figure 30:** Schematic of a single bit cell of the A/D converter based on current multiplication.

Figure 30 shows the first bit cell of the multiplying converter.  $I_{Ref}$  is mirrored by an  $n$ -mirror to isolate the converter from the outside world. To transform the current sink into a current source, the current gets mirrored again but this time a  $p$ -mirror is used. Neglecting the current mirror error, due to device variances caused by production tolerances, the current should still have the exact same value as the reference current had before it was mirrored twice.

The other input to the cell,  $I_{in}$ , also passes through an  $N$ -mirror first, transforming it into a current sink. It has the same value as  $I_{in}$  had, but the sign changes. This node is connected to the drain of the  $p$ -type transistor of the mirror which provides the isolated  $I_{Ref}$  in the form of a current source. In addition, the input of a CMOS current comparator, whose design is similar to the one introduced in section 3.2.3, is connected to this node as well. It is supposed to switch from low to high when the input current (the current sink) becomes bigger than the reference current (the current source). To meet these requirements, the existing comparator design had to be extended by adding a third inverter stage to the two existing ones. It inverts the signal after the second stage a third time, so that the comparator output switches when the absolute value ( $I_{in}$ ) of the current sink becomes bigger than the absolute value ( $I_{Ref}$ ) of the current source. SPICE experiments showed the usage of only a single inverter stage in the comparator would principally work as well but suffers from an extreme comparison speed loss by at least ten magnitudes. Since this is not acceptable for the target application, it was decided to choose the three inverter design for this project.

Figure 31 shows the entire circuitry which is necessary for the seven bit thermometer code current mode A/D converter. It is composed of seven of the bit cells from Figure 30. Since every stage of the comparator requires its own copy of  $I_{in}$ , it has to be copied seven times. The copies are obtained by connecting the gates of  $n$ -MOS transistors to the node which drives the gate of the second transistor in the  $n$ -mirror for  $I_{in}$ . They form the  $I_{in}$  input

network which can be identified on the left hand side of the schematic in Figure 31. Since they are all part of an  $n$ -type current mirror, their drains are in a second connection line connected to the ground node. The source of each  $I_{in}$  copy transistor directly connects to the comparator input of the corresponding bit cell.

For the input of the second bit cell,  $I_{Ref}$  times two is required. It is obtained by taking a copy of  $I_{Ref}$  from the first cell and then doubling it in the  $n$ -mirror of bit cell number two. The current doubles because the gates of two transistors of the same dimensions are connected in parallel.

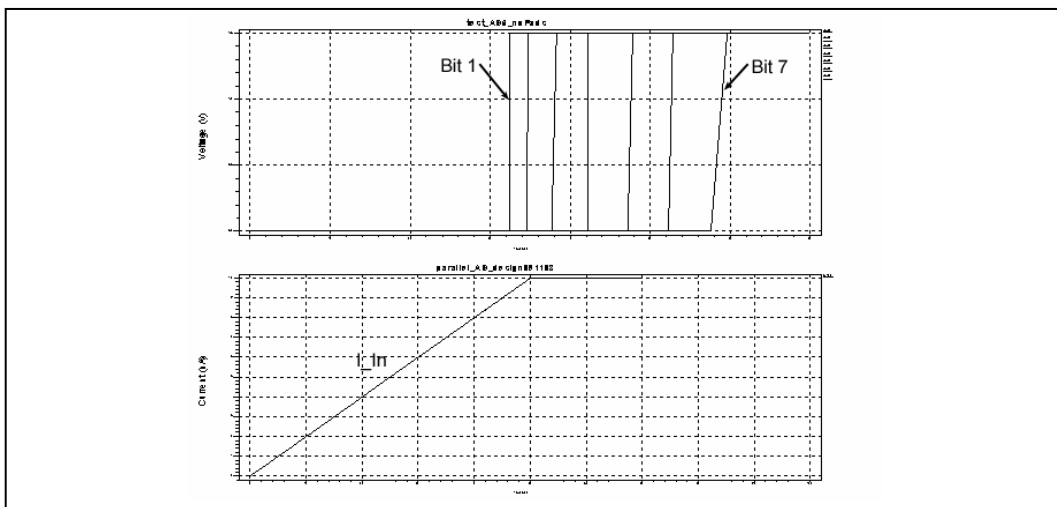
For the input of bit cell number three,  $I_{Ref}$  times three is required. Since two can not be divided by three, doubling again does not work. But, according to Kirchhoff's current law, making one copy of  $2 * I_{Ref}$  and one copy of  $I_{Ref}$  itself and adding them together results in  $3 * I_{Ref}$ . Four times  $I_{Ref}$  can be obtained by making a copy of  $2 * I_{Ref}$  and doubling it as done in bit cell number two. Five times  $I_{Ref}$  can be obtained by making one copy of  $2 * I_{Ref}$  and one copy of  $3 * I_{Ref}$  and adding them together. Six times  $I_{Ref}$  again is obtained by doubling a copy of  $3 * I_{Ref}$  as done before in the case of bit cell number two and four. Finally, seven times  $I_{Ref}$  is obtained by adding a copy of  $6 * I_{Ref}$  to a copy of  $I_{Ref}$ .



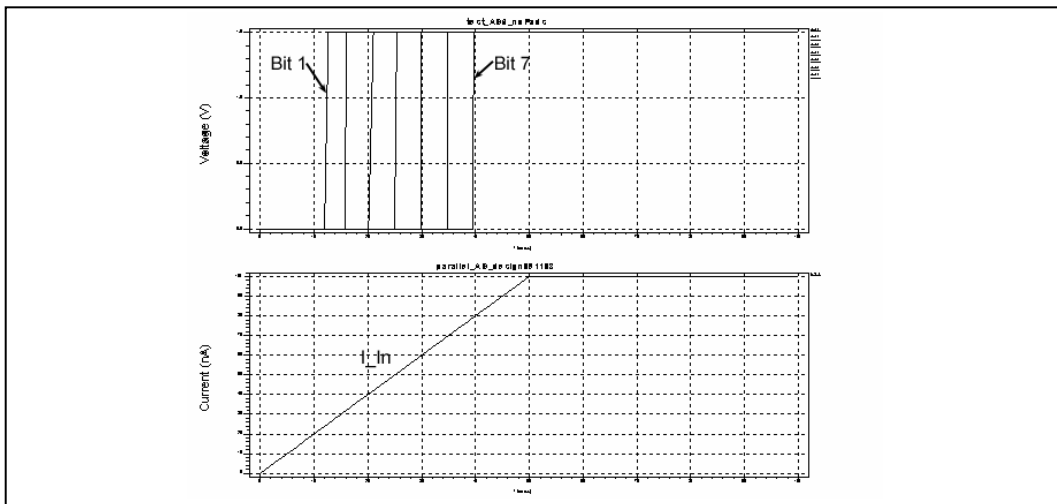
## 4.4

### SPICE Simulation

The next step in the design verification process is to test the circuit with SPICE simulation. The Tanner SPICE simulator accepts either written ASCII description text files or schematic files generated by *S-SPICE*. Again, all SPICE simulations were performed using Tanner Research's *SPICE Development Kit* (*T-SPICE Pro* v9.02, *S-Edit* v8.1 and *W-Edit* v9.02). Once more, BSIM3 transistor models were employed to emulate the transistor. In Figure 32 and Figure 33 you can see the results of simulations in which the input current was increased from zero to full scale. In Figure 34 and Figure 35 a square wave shaped input current was applied to the circuit to see its dynamic response. The simulation length in all four diagrams is 100 $\mu$ s.

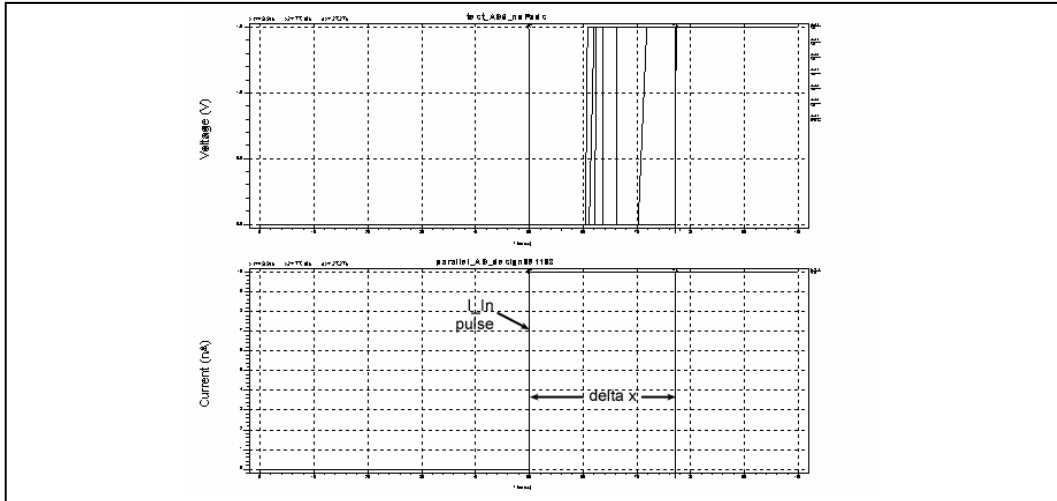


**Figure 32:** Simulation with  $I_{Ref}=1nA=LSB$ . Thus, full scale input is  $7*LSB=7nA$ . Lower diagram:  $I_{in}$  rises from 0 to 10nA. Upper diagram: bit 1 to bit 7 switches from 0 to 5V.

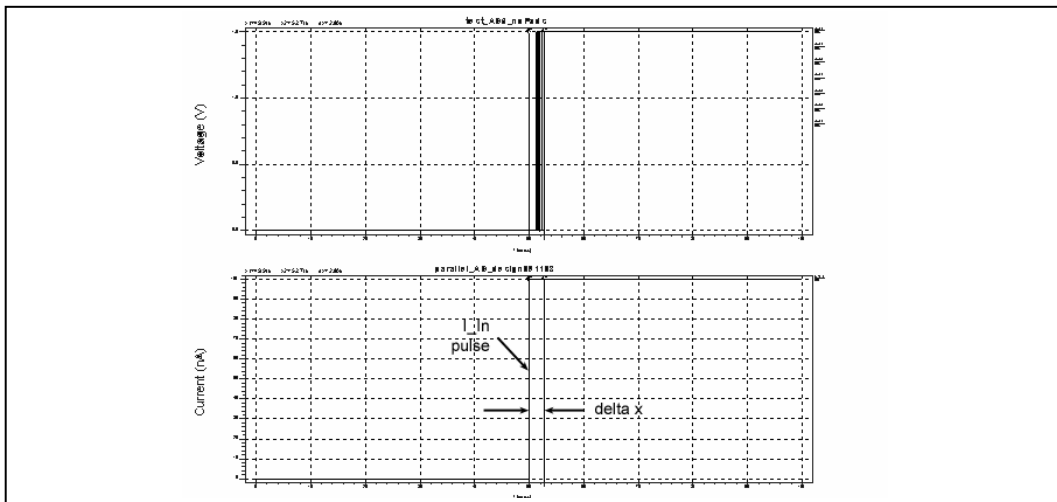


**Figure 33:** Simulation with  $I_{Ref}=10nA$ . Consequently, full scale input is  $7*LSB=70nA$ . Lower diagram:  $I_{in}$  ramp (it rises from 0 to 100nA).

The response of the converter from Figure 32 shows that it is easily capable to resolve current differences as small as 1nA. The most significant difference when comparing the simulation in which  $I_{Ref}$  is 1nA to the simulation in which it is 10nA is the response time. The higher currents lead to more current flowing between the current source and the current sink to which the comparator is attached to. Consequently, the capacitances which have to be reloaded get charged more quickly, resulting in a quicker response time of the system.



**Figure 34:** Dynamic response to a square wave input of  $I_{in}=10n$ .  $I_{Ref}$  was as 1nA, total simulation time 100 $\mu$ s,  $\Delta x$  has been measured with 27,27 $\mu$ s.



**Figure 35:** Square wave input of  $I_{in}=100nA$ . Reference current  $I_{Ref}=10nA$ , simulation time 100 $\mu$ s,  $\Delta x$  is 2.8 $\mu$ s.

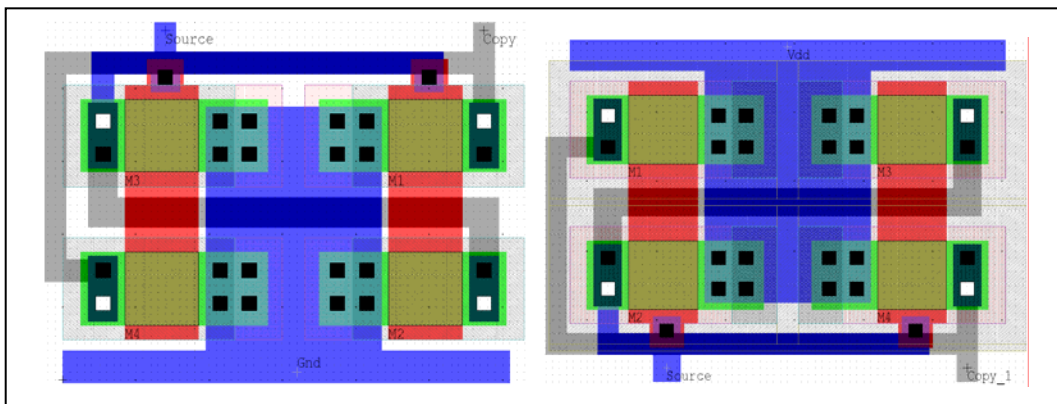
Figure 34 and Figure 35 show that there is a linear coherence between the response time and the input current value. The input current in the second simulation is exactly one magnitude bigger than in the input current in the first simulation. The response time  $\Delta x$  which was measured in each attempt shows the same correlation: In the simulation



where  $I_{\text{Ref}} = 1\text{nA}$  the delay until the last bit (bit 7) has switched is  $\Delta x = 27.27\mu\text{s}$ , while in the simulation where  $I_{\text{Ref}} = 10\text{nA}$  the delay is only  $\Delta x = 2.8\mu\text{s}$ . This is nearly exactly one magnitude faster.

When the same measurements are carried out with the real chip, shown in section 4.6, it will be possible to determine whether SPICE simulations are a good estimate for the accomplishable conversion speed or if it will have a maximum conversion rate which is much lower or even higher than the rate measured here.

## 4.5 Layout



**Figure 36:** Layout of two current mirror cells. Left hand side:  $n$ -mirror cell; Right hand side:  $p$ -mirror cell. Both use two pairs of cross connected transistors (each  $w/l=10/10$  lambdas in size).

In this step of the chip development process, the schematic had to be converted into a drawn representation on transistor level. By using Tanner's *L-Edit* software (v10.12), it was possible to develop the circuit layout from scratch. Mirrors and inverters are the only required building blocks in the converter. They are both made up of either  $p$ - or  $n$ -MOS transistors, which are the basic elements to be used over and over again. To achieve the best matching properties in current mirrors, cross connected pairs of transistors were used to form a mirror with the dimensions of  $w/l = 20/10$  lambdas. Cross connected mirrors can compensate substrate variations which cause mirror mismatching and lead to a lack of conversion accuracy and a less efficient resolution.

Figure 36 shows the  $p$ - and the  $n$ -mirror cell which was used for all the different layout purposes. It makes use of two layers of metal, *metal1* and *metal2*, which can be interconnected by vias. This layout was chosen so that several  $n$ -mirror cells can be easily aligned along the ground line to which all their drains are connect to.

In Figure 37, the whole on current multiplication based A/D converter is shown. It consists of 23  $p$ -mirrors, 25  $n$ -mirrors, 7 current comparators and 12 shielded mirrors (9  $p$ - and 3  $n$ -mirrors). The shielded mirrors are used to make copies of currents which are required to be measured outside the chip. In order to protect the rest of the circuit from outside interference, the copy mirrors are protected by a guard ring consisting of substrate contacts and layers of *metal1* and *metal2*. The current comparators are made up of three stages of CMOS inverters. To maximize the comparator speed, the transistor dimensions become bigger in each inverter stage.

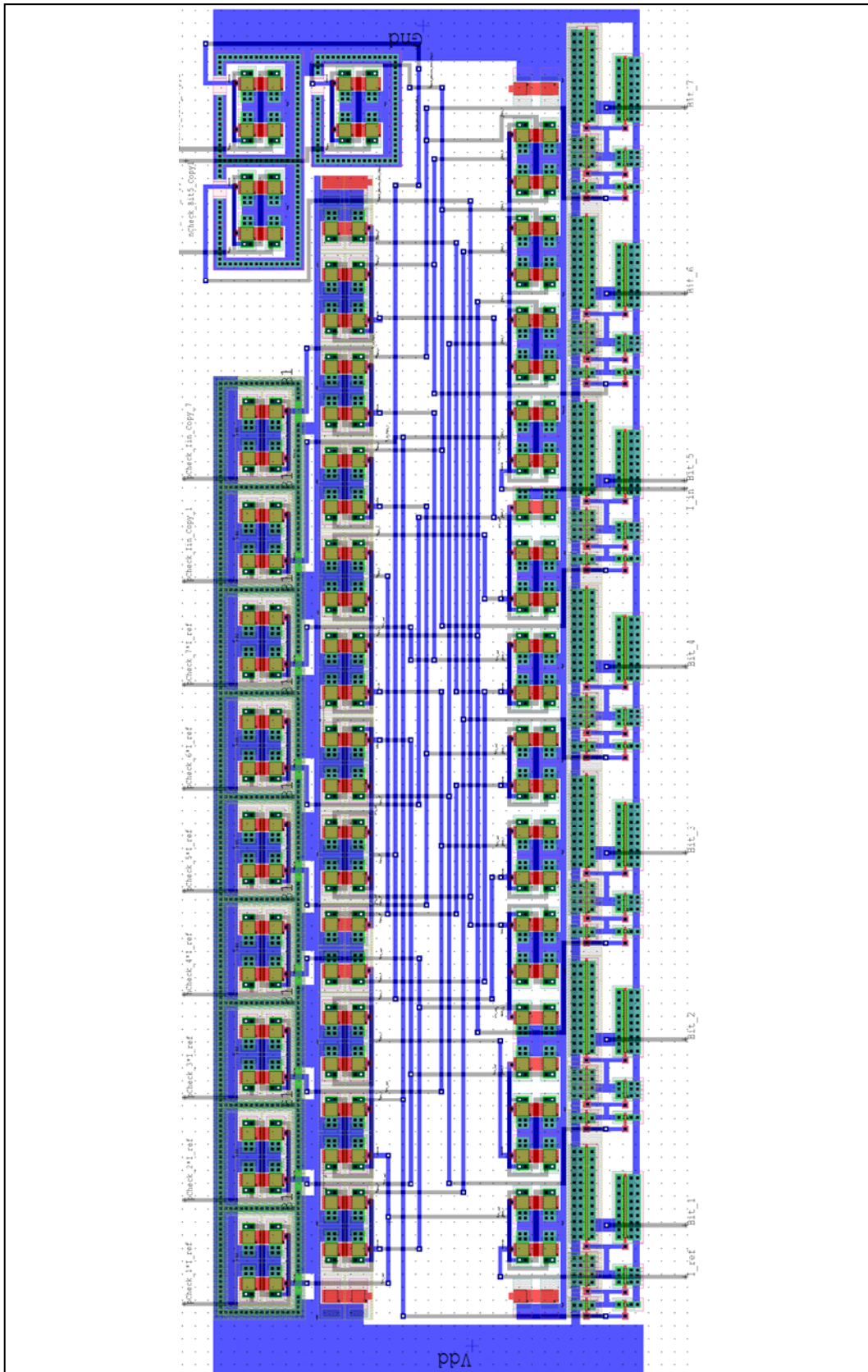
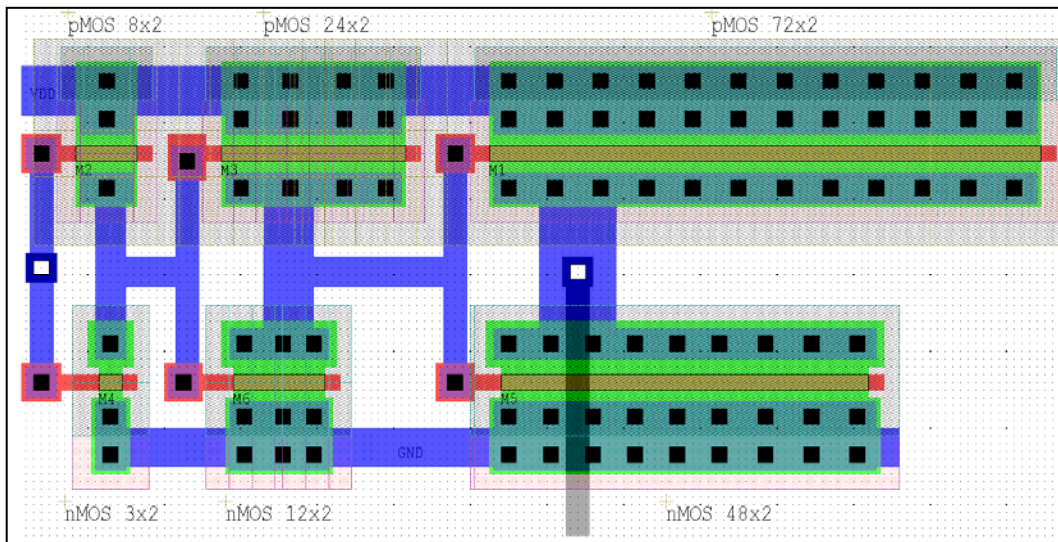


Figure 37: Layout of the A/D design based on current multiplication.



**Figure 38:** CMOS comparator consisting of three inverter stages with differently sized transistor dimensions.

Figure 38 clarifies the design: Inverter stage one has an  $n$ -MOS transistor with a width of three lambdas and a length of two lambdas. The  $p$ -MOS has the dimensions  $w/l = 8/2$  lambdas. In the second inverter stage, the  $n$ -type transistor is  $w/l = 12/2$  lambdas in size, the  $p$ -type measures  $w/l = 24/2$  lambdas. This is a multiplication factor of four for the  $n$ -type and a factor of three for the  $p$ -type. Multiplying in the same way again gives the dimensions of the transistors used in the third stage, amounting to  $w/l = 48/2$  lambdas for the  $n$ -type and  $w/l = 72/2$  lambdas for the  $p$ -type transistor. In this setup, delay times are minimized and the capacitive load is kept constant over the inverter

As all the connecting work has to be done by hand and frequent design rule checks are mandatory, it is necessary to stick to a strictly orthogonal layout which only positions *metal1* in the horizontal direction and *metal2* in the vertical direction (or the other way round). Apart from design rule checks (DRCs) it is possible to perform layout versus schematic tests (LVS). This helps to verify the layout of new building blocks on different levels in the building block hierarchy. Once a block has successfully been verified as 100% equal to its schematic counterpart, it is safe to use it in a more complex surrounding circuitry. Another measurement to obtain best current mirror matching results is to surround the current mirrors which are at the ends of the mirror chain by dummy mirrors which are not actually used. It helps to embed the mirrors into a preferably equal surrounding which is known to have an influence on the matching characteristics of current mirrors.

When holding Figure 37 in landscape format, you can identify the seven comparator cells on the bottom of the image. In the next row above them are the 25  $n$ -mirrors with two dummy mirrors on each side of them. Above this row the wiring begins, which is followed by a row of  $p$ -type current mirrors. The top row of building blocks in this image consists of the copy mirrors which are protected by guard rings.

## 4.6

### Experimental Results

This section includes results obtained by measurements on the real chip after it was received back from the manufacturer, MOSIS, in January 2004. For its operation and to carry out experiments with it, a self developed printed circuit prototype test bed was used. It will be described in detail in chapter 8.

#### 4.6.1

##### Test Overview

Table 5 gives an overview on all the tests which were performed with the multiplying A/D converter as well as with the dividing A/D converter. Test results for the dividing A/D converter can be found in Chapter 5 “Subthreshold Current-Mode ADC based on Current Division”. The table is split into two main test categories: DC tests and dynamic tests. The DC tests were carried out to test the conversion quality, such as accuracy, linearity, offset and quantization errors. Dynamic tests were performed to measure signal-to-noise ratio, noise, bit error rate, maximum sampling frequency and settling time.

**Table 5:** Test matrix showing the different combinations of input values for the two A/D converters.

		Multiplying Converter	Dividing Converter
DC Tests ( $I_{in}$ constant at 1Hz)	$I_{Ref}$ variation; $V_{DD}$ fixed	$I_{in}$ 0-12nA 0-120nA 0-500nA $I_{Ref}$ 1nA 10nA 30nA $V_{DD}$ 5V	$I_{in}$ 0-15nA 0-150nA 0-300nA $I_{Ref}$ 10nA 100nA 250nA $V_{DD}$ 5V
	$V_{DD}$ variation; $I_{Ref}$ fixed	$I_{in}$ 0-120nA $I_{Ref}$ 10nA $V_{DD}$ 1.0V 1.5V 3.0V	$I_{in}$ 0-150nA $I_{Ref}$ 100nA $V_{DD}$ 1.0V 1.5V 3.0V
AC Tests ( $I_{in}$ at max. frequency)	$I_{Ref}$ variation; $V_{DD}$ fixed;	$I_{in}$ 0-12nA 0-120nA 0-500nA $I_{Ref}$ 1nA 10nA 25nA $V_{DD}$ 5V	$I_{in}$ 0-15nA 0-150nA 0-500nA $I_{Ref}$ 10nA 100nA 250nA $V_{DD}$ 5V
	$V_{DD}$ variation; $I_{Ref}$ fixed	$I_{in}$ 0-120nA $I_{Ref}$ 10nA $V_{DD}$ 1.0V 1.5V 3.0V	$I_{in}$ 0-150nA $I_{Ref}$ 100nA $V_{DD}$ 1.0V 1.5V 3.0V

Note that a saw tooth shaped input was chosen for the DC tests for  $I_{in}$  (resulting in an input range so that each bit switches independently), while the AC tests were performed using a square wave shaped input for  $I_{in}$  (here only the edges are interesting, all bits switch at a time).

According to the test matrix shown in Table 5, the results are split into the categories *DC Tests* and *Dynamic Tests*. A third category of tests performed measures the internal multiplication accuracy of the converter (multiplication factor).

#### 4.6.2

##### Test Equipment

The test equipment which was used for the experiments consists of:

- 1 x A.M.P.I. Master-8 Stimulator
- 1 x HP E3631A Programmable Power Supply
- 1 x Tektronix 4 Channel Digital Phosphor Oscilloscope
- 1 x National Instruments BNC-2090 Data Acquisition Board and Interface Card
- 1 x Prototype test-bed with analog chip

The HP power supply supplies the test-bed with +5V and -5V power rails and a bias voltage of +3.9V for the OP-amps. The Master-8 provides the voltage which is used to generate  $I_{Ref}$  and also deliver  $V_{DD}$  for the chip. The National Instruments DAB is controlled by a personal computer (PC) on which the LabView software runs a data acquisition module. It is capable to simultaneously record 15 channels while generating two independent voltages (square wave, saw tooth, triangle, etc.). In the following experiments, one of the output channels to control the voltage which generates  $I_{Ref}$  was used, and one of the recording channels to monitor this voltage. In addition, seven more recording channels to record bit one to bit seven were used. The Tektronix four channel oscilloscope measures the two voltages generated by the Master-8 stimulator, due to the absence of a voltmeter on the stimulator. This was used to visualize the voltage which gets converted into  $I_{in}$ , provided by the DAB. Its fourth channel was finally used to analyze the frequency response of single bits when performing high frequency tests which are difficult to record with the DAB.

#### 4.6.3

##### Multiplication Factor Tests

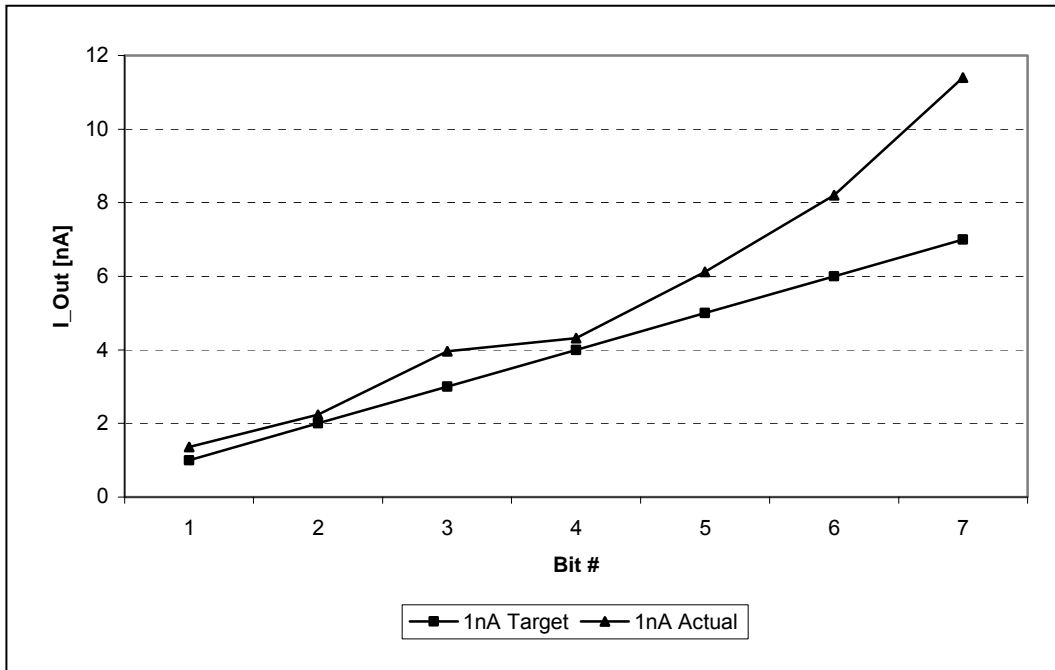
This experiment shows the accuracy of the current multiplication within the seven bit cells of the converter. The output current of each of these cells is mirrored with separate current mirrors using guard rings to an output pin of the chip. By using a multiplexer (thumb-nail switch) on the prototype test board, it is possible to connect these pins to a current measurement circuit which is shared by all of them. In Table 6, the result of these experiments is shown. Ideally, there should be no difference between  $I_{Ref}$  multiplied by the factors between one and seven and the outputs of the cells for bit one to bit seven. All measurements were taken using a supply voltage of  $V_{DD} = 5.0V$ .

**Table 6:** Measured multiplication factors from the real chip.

	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
$I_{Ref} = 1nA$	Target: 1nA Actual: 1.36nA Error: +36%	Target: 2nA Actual: 2.24nA Error: +12%	Target: 3nA Actual: 3.96nA Error: +32%	Target: 4nA Actual: 4.32nA Error: +8%	Target: 5nA Actual: 6.12nA Error: +22.4%	Target: 6nA Actual: 8.20nA Error: +36.6%	Target: 7nA Actual: 11.4nA Error: +62.8%
$I_{Ref} = 10nA$	Target: 10nA Actual: 9.7nA Error: -3%	Target: 20nA Actual: 19.8nA Error: -1%	Target: 30nA Actual: 38.8nA Error: +29.3%	Target: 40nA Actual: 42.8nA Error: +7%	Target: 50nA Actual: 63.8nA Error: +26.7%	Target: 60nA Actual: 86.2nA Error: +43.6%	Target: 70nA Actual: 114.0nA Error: +62.9%
$I_{Ref} = 50nA$	Target: 50nA Actual: 48.4nA Error: -3.2%	Target: 100nA Actual: 100.4nA Error: +0.4%	Target: 150nA Actual: 187.4nA Error: +24.9%	Target: 200nA Actual: 215.5nA Error: +7.75%	Target: 250nA Actual: 322.1nA Error: +28.84%	Target: 300nA Actual: 419.5nA Error: +39.8%	Target: 350nA Actual: 533.1nA Error: +52.3%

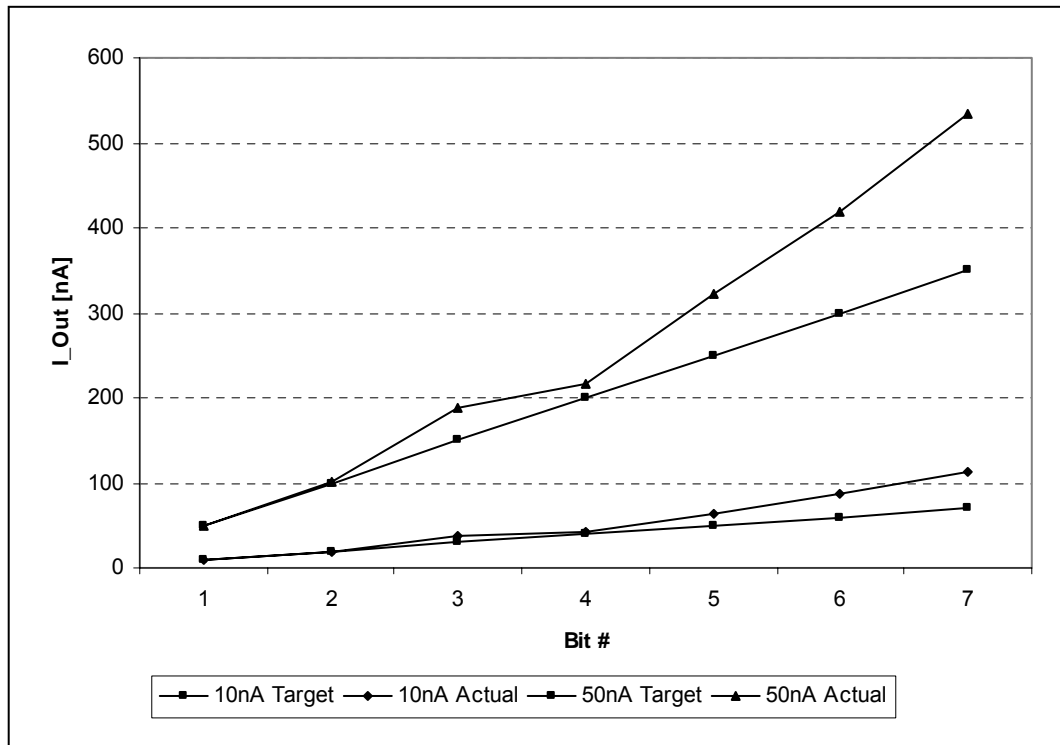
In Figure 39 and Figure 40 the ideal and the actual currents at which bit 1 – 7 switch are visualized in a chart graph. As seen, the error of the multiplication increases the higher the bit number. This is due to errors in the multiplications and additions which are made for the lower bits. By reusing the results of these calculations, the error gets multiplied again. Also, there will be a new error in the second multiplication which has to be taken into account. Consider that the reference current for bit seven for example was obtained by calculating  $((I_{Ref} + 2 * I_{Ref}) * 2) + I_{Ref}$ . This means there are four calculations involved, leading to an error rate of approximately 50-60% for bit seven. The exact numbers can be found in Table 6.

Comparing Figure 39 and Figure 40 shows that the multiplication accuracy is about the same for all the reference currents used. However, a closer look at bit one and two reveals some differences. In the case of  $I_{Ref} = 1nA$  the errors seem to be much bigger than the errors of bit one and two when  $I_{Ref} = 10nA$  or  $I_{Ref} = 50nA$ . This is probably due to the inaccuracy of measurements when such small voltages are measured.



**Figure 39:** Deviance of the actual measured multiplication factors from the target factors for  $I_{Ref} = 1nA$ .

Figure 39 and Figure 40 show multiplication factors in a range between 1nA and 50nA. Bit three is particularly apparent because of its greater deviation from the ideal curve (target).



**Figure 40:** Deviance of the actual measured multiplication factors from the target factors for  $I_{Ref} = 10nA$  and  $I_{Ref} = 50nA$ .

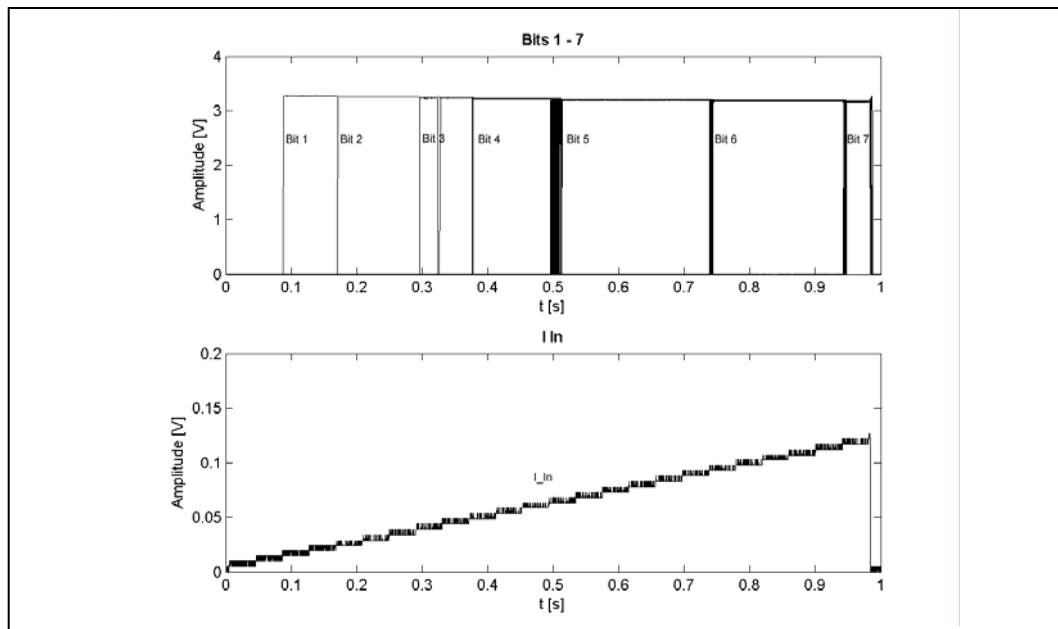
#### 4.6.4

##### DC Tests with $I_{Ref}$ Variation

DC tests are all done by applying a slowly increasing voltage to the voltage/current converter, which is a discrete circuit located on the prototype test bed. This voltage was generated by the National Instruments DAB by using one of its two data output channels. To record, eight DAB channels were used. Seven of them recorded the voltage levels of bits 1 to 7 of the converter, the eighth channel served to record the stimulation voltage generated on the data out channel (self monitoring). The stimulation signal is saw tooth shaped with a frequency of 1Hz. The amplitude of the saw tooth depends on the test which is done, since the full scale input has to match the reference current. In all experiments where  $I_{Ref}$  is varied,  $V_{DD}$  is kept at a constant level of 5V.

##### 4.6.4.1

##### $I_{Ref} = 1nA$



**Figure 41:** Bits 1- 7 triggered by a saw tooth shaped input current providing the full scale input for the converter with a reference current of  $I_{Ref} = 1nA$ .

Figure 41 shows the converter's response to a stimulation current between 1 – 12nA when operating with a reference current of 1nA. Although bit three and five oscillate a few times before they remain in a stable condition, the system works as predicted in earlier SPICE simulations. When looking at the linearity of the converter with these parameters in Figure 42, it shows that the error it makes is fairly constant for bits one to five. For bit six and seven, the gap between ideal linear conversion curve and the actual conversion curve becomes bigger.



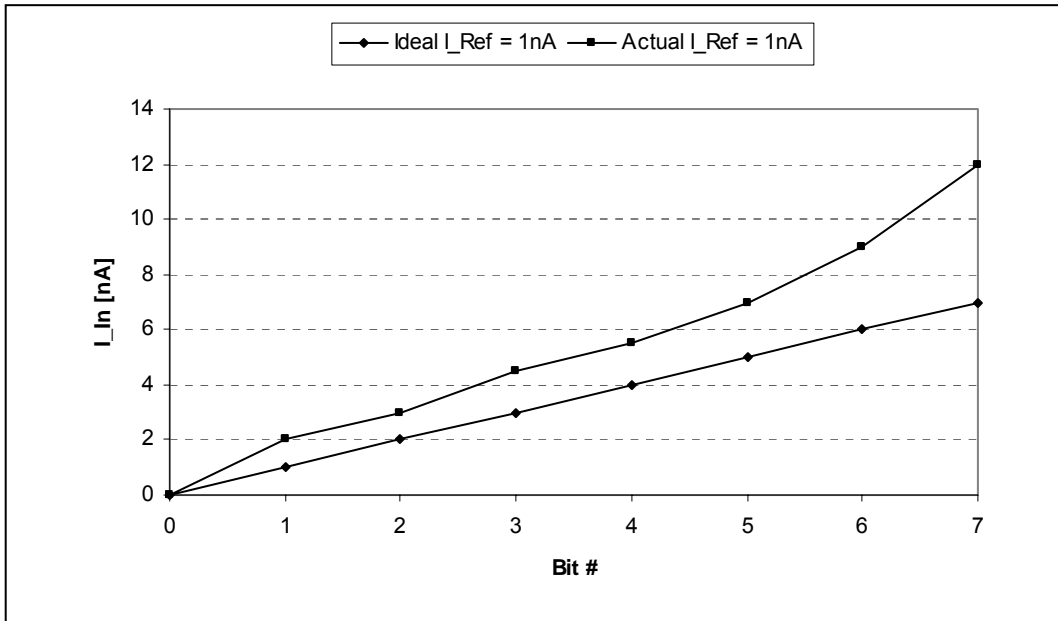


Figure 42: Variance of the actual conversion curve from the ideal conversion curve for  $I_{Ref} = 1\text{nA}$ .

4.6.4.2

$I_{Ref} = 10\text{nA}$

Test conditions were the same as in the previous experiment, only the reference current is 10nA and the full scale input (amplitude of the of the saw tooth shaped stimulation voltage) is 1.2V which translates to 120nA.

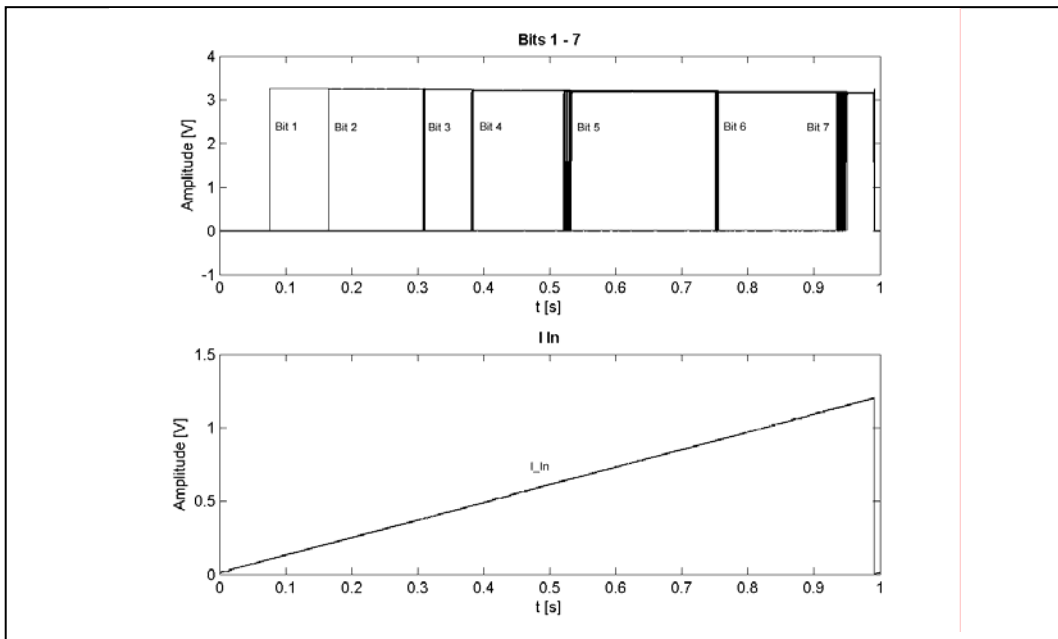


Figure 43: Measurement of bits 1- 7 for  $I_{Ref} = 10\text{nA}$ , saw tooth shaped input.

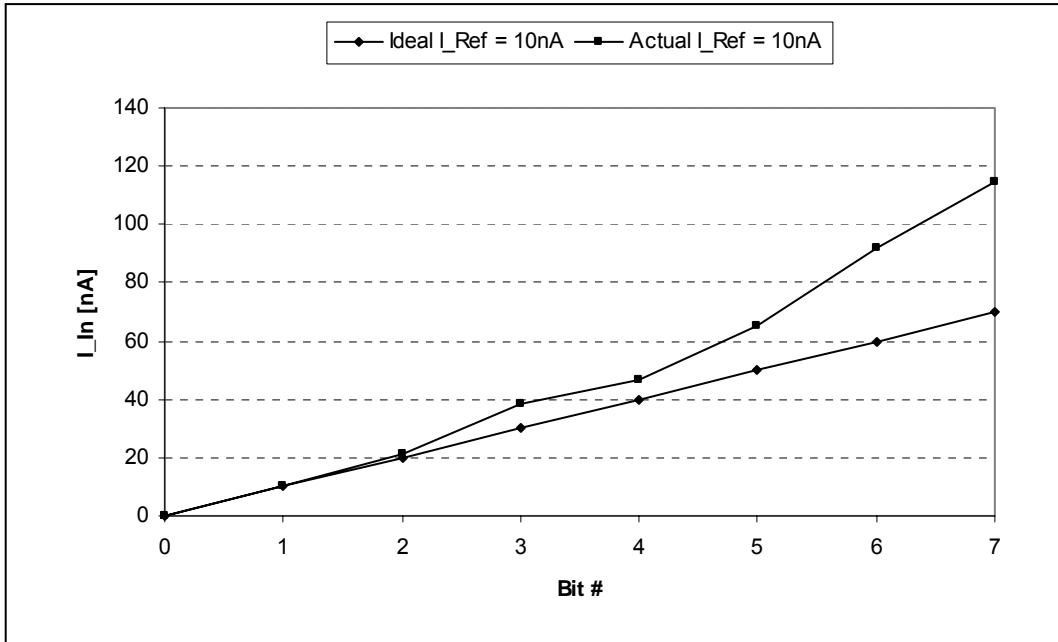


Figure 44: Variance of the actual conversion curve from the ideal conversion curve for  $I_{Ref} = 10nA$ .

4.6.4.3

$I_{Ref} = 30nA$

In this example a reference current of 30nA is used, changing the required full scale input current to 500nA which equals 5V.

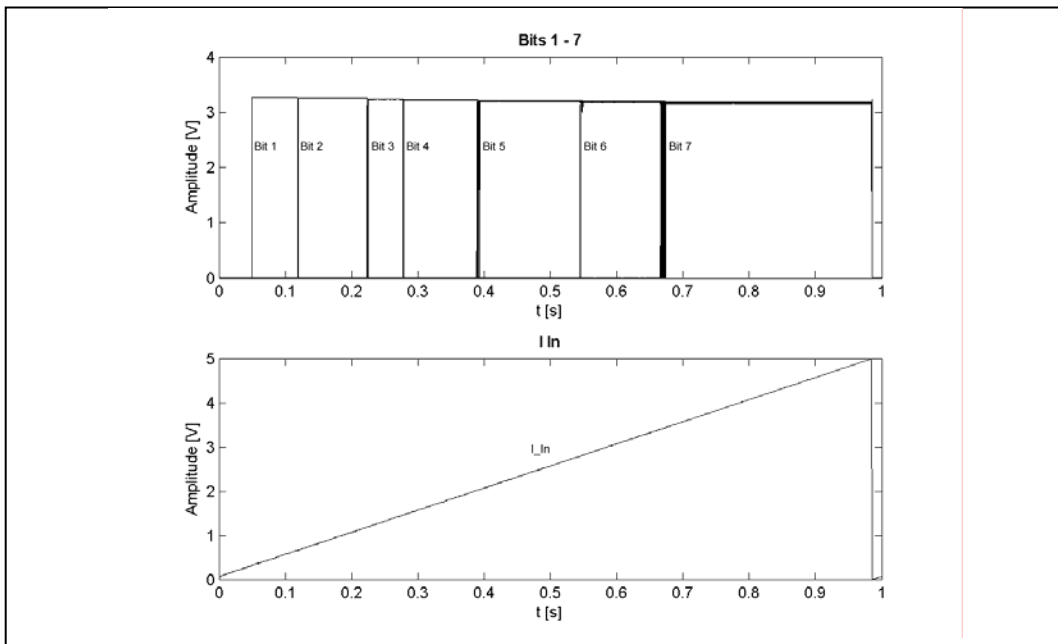
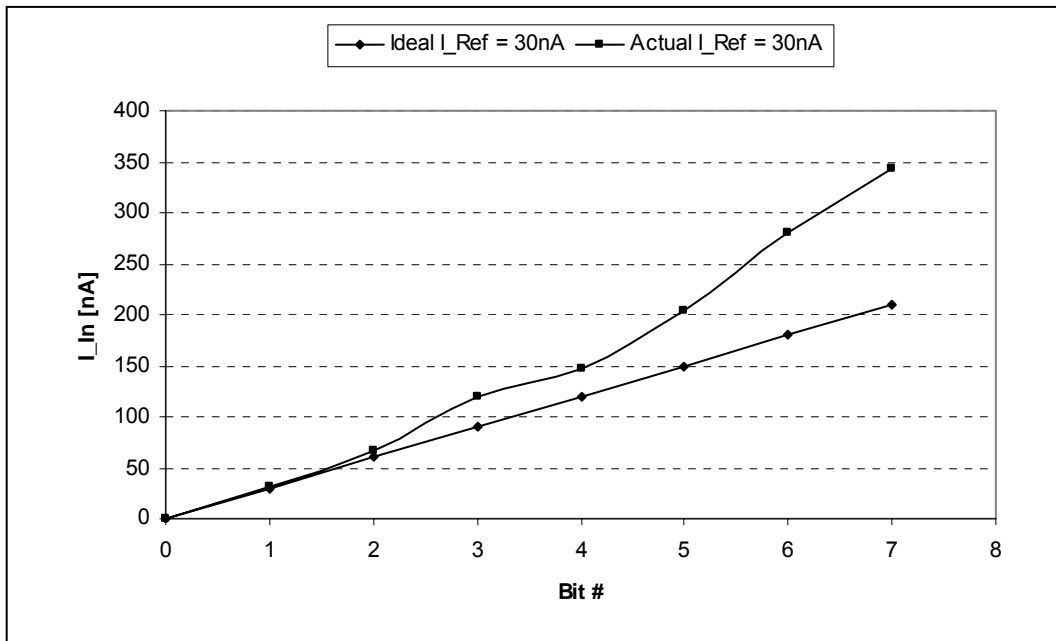


Figure 45: Measurement of bits 1- 7 for  $I_{Ref} = 30nA$ , saw tooth shaped input.



**Figure 46:** Variance of the actual conversion curve from the ideal conversion curve for  $I_{Ref} = 30\text{nA}$ .

#### 4.6.5

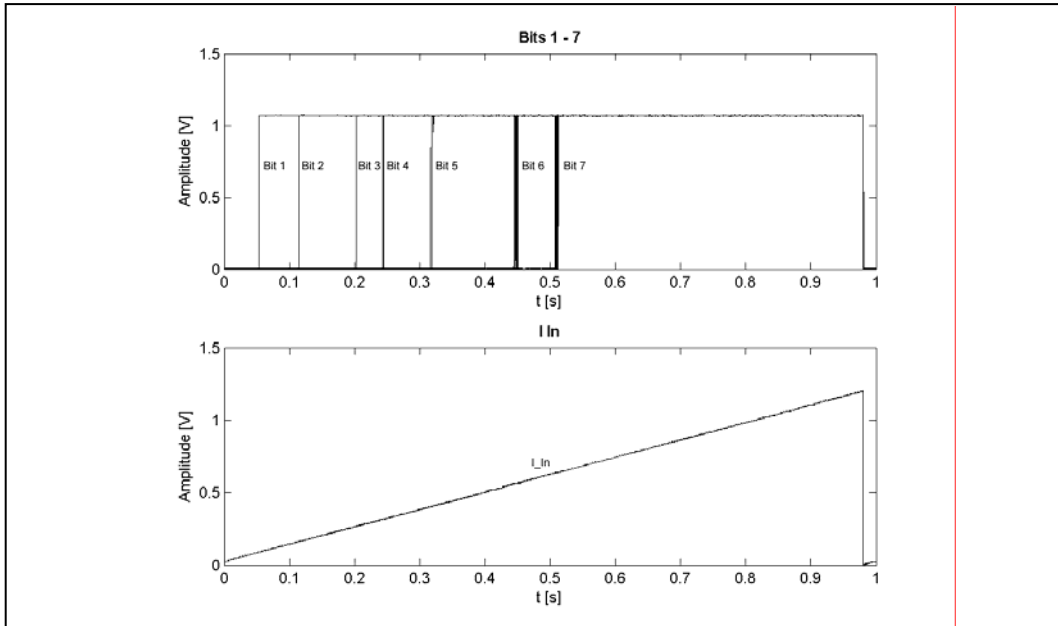
##### DC Tests with $V_{DD}$ Variation

Unlike the experiments when the input current  $I_{Ref}$  was varied, it is kept at a fixed value of  $10\text{nA}$  and the power supply voltage of the converter is varied instead. The goal of these experiments is to find out if the circuit still works at low operating voltages. Also, the linearity at these low operating voltages can be analyzed and compared to the experiments which were carried out using  $V_{DD} = 5\text{V}$  as a power supply to the chip.

##### 4.6.5.1

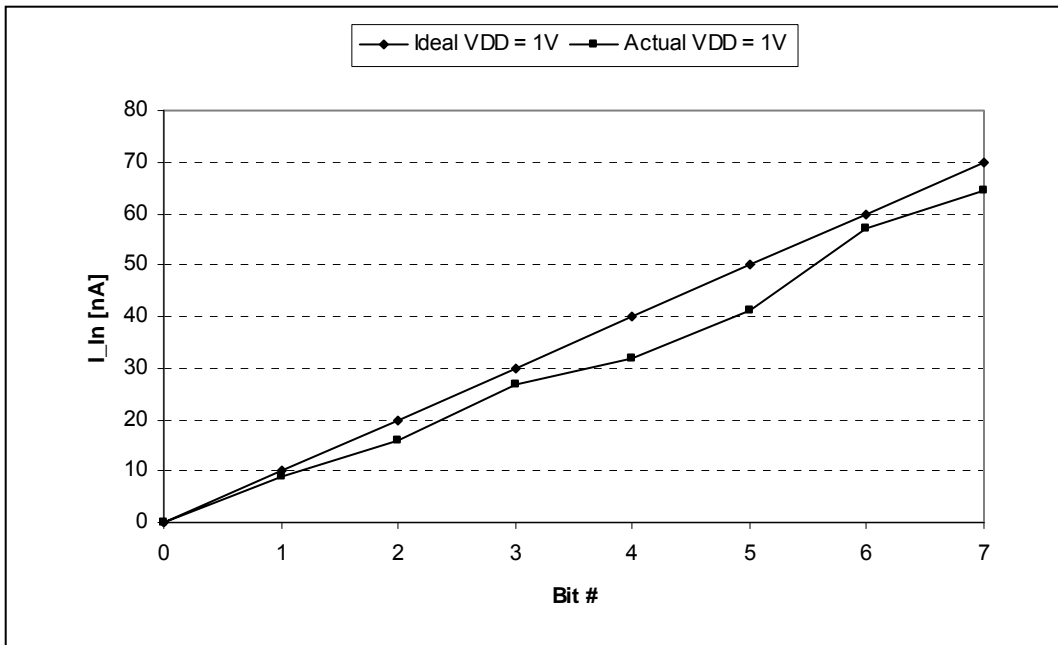
###### $V_{DD} = 1.0\text{V}$

$1\text{V}$  is the lowest supply voltage at which the converter was tested. By looking at the linearity diagram in Figure 48 you will notice that the accuracy is much better than seen in the same test using  $V_{DD} = 5\text{V}$  (Figure 41).



**Figure 47:** Measurement of bits 1- 7 for  $V_{DD} = 1V$ , saw tooth shaped input of 10nA.

It is clearly apparent in Figure 48 that the actual measured data points are situated below the target data points. Bit four and five form a “belly” in the curve indicating that these two bits seem to be less accurate than the rest.



**Figure 48:** Variance of the actual conversion curve from the ideal conversion curve for  $V_{DD} = 1V$  and  $I_{Ref} = 10nA$ .

4.6.5.2

$V_{DD} = 1.5V$

By raising the supply voltage to 1.5V, it is noticeable that the converter's switching points for bit six and bit seven jump from less than the ideal value to more then the ideal value.

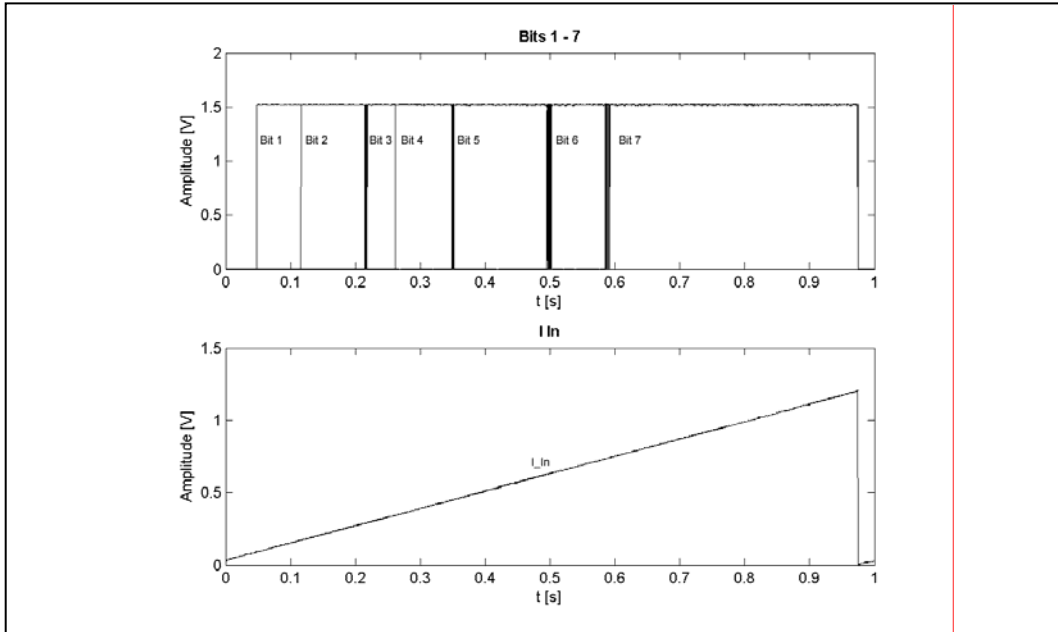


Figure 49: Measurement of bits 1-7 for  $V_{DD} = 1.5V$ , saw tooth shaped input of 10nA.

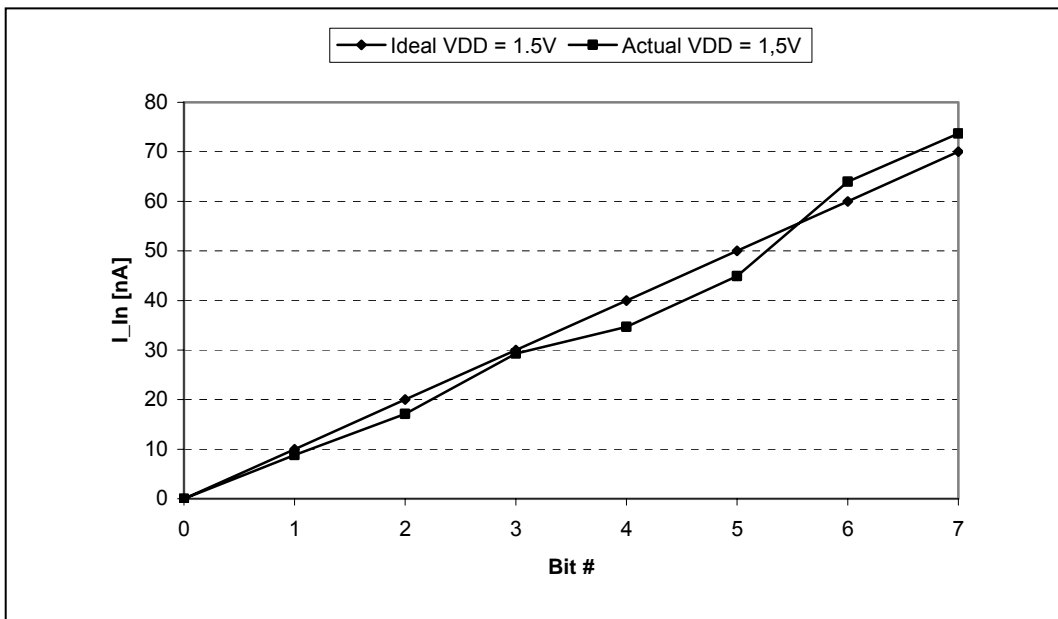


Figure 50: Variance of the actual conversion curve from the ideal conversion curve for  $V_{DD} = 1.5V$  and  $I_{Ref} = 10nA$ .

4.6.5.3

$V_{DD} = 3.0V$

In the experiment with  $V_{DD} = 3V$  you can see how the linearity error suddenly becomes much bigger then in the last two experiments with 1.5V. Figure 52 shows a clear deviation of the switching points of bit six and seven from the ideal linear curve.

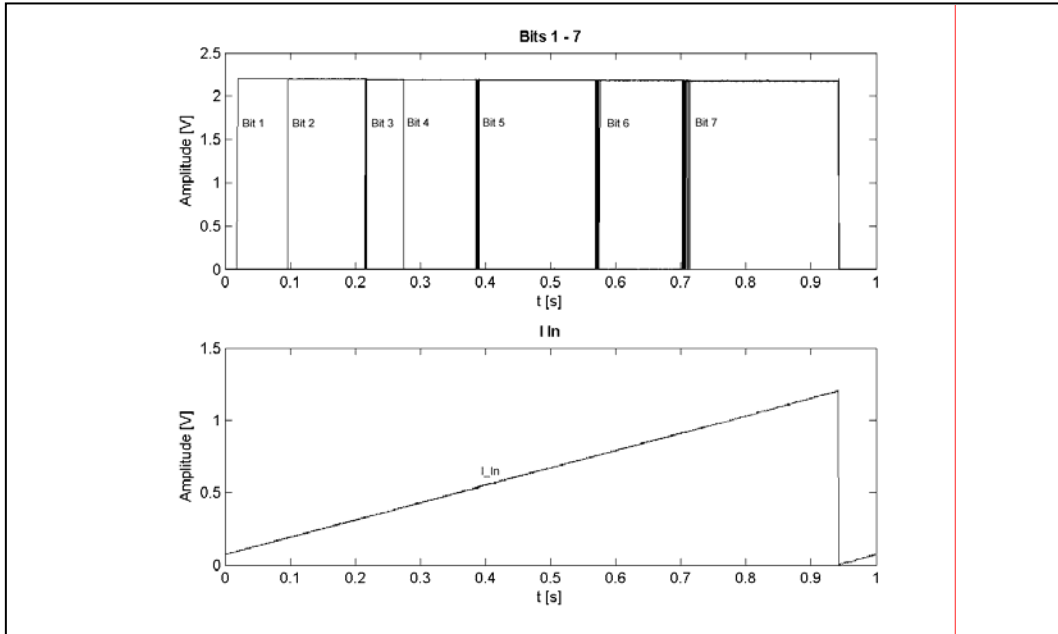


Figure 51: Measurement of bits 1-7 for  $V_{DD} = 3V$ , saw tooth shaped input of 10nA.

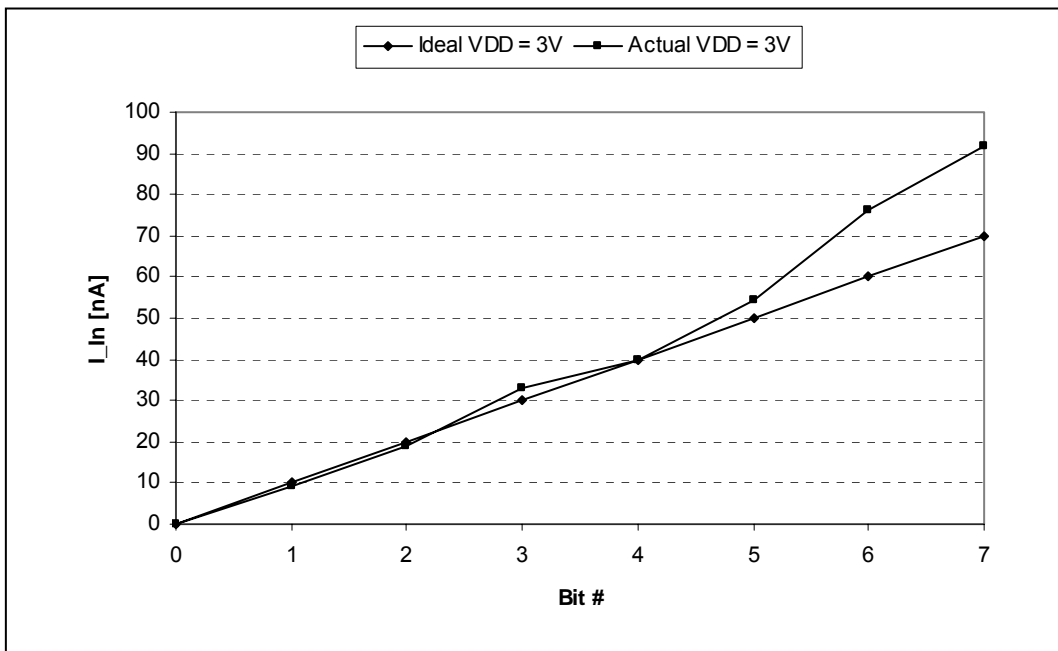


Figure 52: Variance of the actual conversion curve from the ideal conversion curve for  $V_{DD} = 3V$  and  $I_{Ref} = 10nA$ .

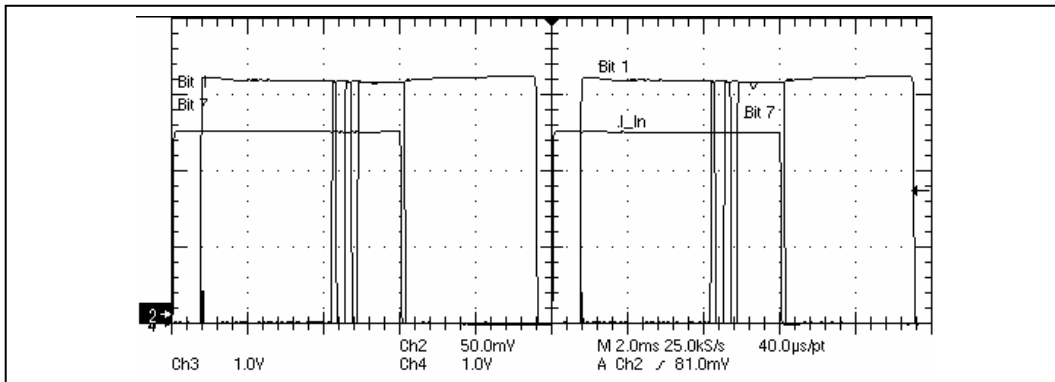
#### 4.6.6

##### Dynamic Tests with $I_{Ref}$ Variation

In this series of experiments the Master-8 Stimulator was used to generate a square wave at the  $I_{in}$  input. Since the DAB couldn't keep up with the amount of channels and the sampling rate/frequency which were used, the Tektronic oscilloscope was used to record and measure the converter's response. The oscilloscope does not have enough channels to measure all seven bits at a time, therefore measurements were limited to bit one and bit seven. In each experiment, five different parameters were measured: (1+2) the delay of bit one and seven after the pulse until they change to high, (3+4) the bit high time of bit one and bit seven, and (5) the maximum possible operating frequency of the converter.

##### 4.6.6.1

$I_{Ref} = 1nA$



**Figure 53:** Test results showing bit 1 and bit 7 for  $I_{Ref} = 1nA$  at  $f = 100Hz$ .

With  $I_{Ref} = 1nA$ , the maximum achievable conversion rate was 100Hz. It is conspicuous that the delay of bit seven is seven times longer than the delay of bit one. Conversely, bit one has a seven times longer bit high time than bit seven. The exact times which were measured on the oscilloscope can be found below in Table 7.

**Table 7:** Measurements at maximum frequency for  $I_{Ref} = 1nA$ .

Delay Bit 1	728 $\mu s$
Delay Bit 7	476 ms
High time Bit 1	8.72 ms
High time Bit 7	1.18 ms
Frequency	100 Hz (Interval = 10ms, Duration = 6ms)

4.6.6.2

$I_{Ref} = 10nA$

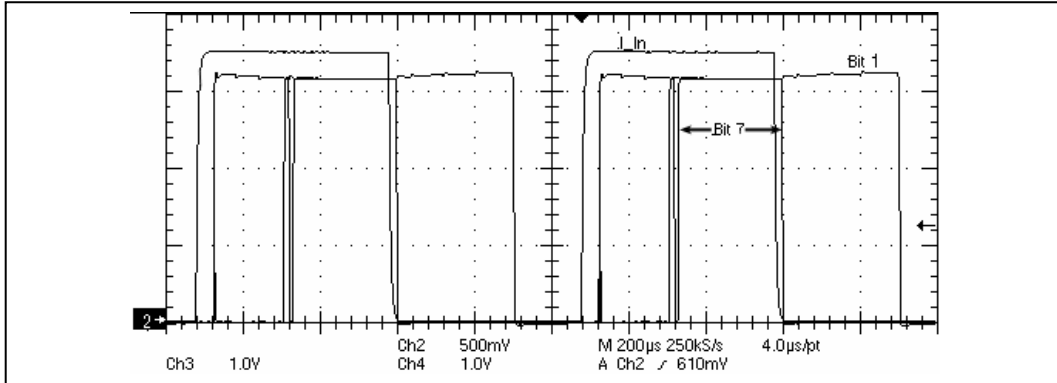


Figure 54: Test results showing bit 1 and bit 7 for  $I_{Ref} = 10nA$  at  $f = 1kHz$ .

After raising the reference current by a factor of ten from 1nA to 10nA, the maximum possible conversion frequency also raises by a factor of ten. Figure 54 shows the converter’s response to the square wave pulse applied to the input  $I_{In}$ .

Table 8: Measurements at maximum frequency for  $I_{Ref} = 10nA$ .

Delay Bit 1	40 $\mu s$
Delay Bit 7	242 $\mu s$
High time Bit 1	770 $\mu s$
High time Bit 7	266 $\mu s$
Frequency	1 kHz (Interval = 1 ms, Duration = 500 $\mu s$ )

4.6.6.3

$I_{Ref} = 25nA$

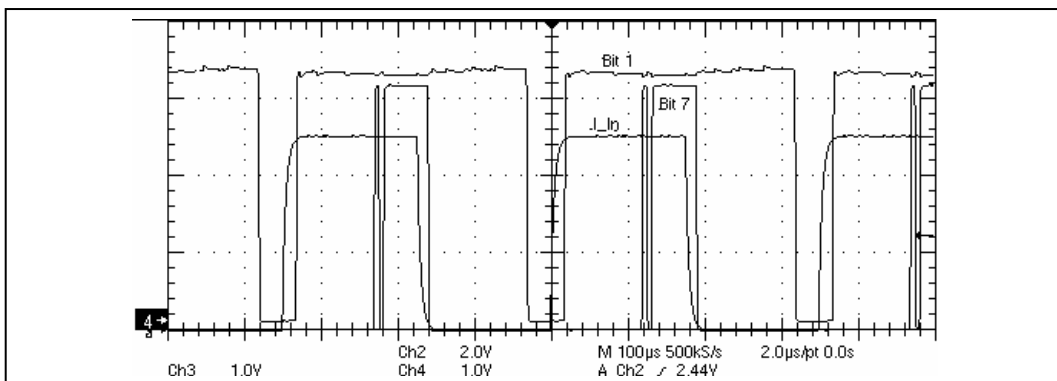


Figure 55: Test results showing bit 1 and bit 7 for  $I_{Ref} = 25nA$  at  $f = 2.86 kHz$ .



In the experiment with a reference current of 25nA, the maximum possible conversion frequency turns out to be 2.86kHz. However, bit seven now has a delay which is about 12 times longer than the delay of bit one. The bit high times are different by a factor of six between bit one and bit seven.

**Table 9:** Measurements at maximum frequency for  $I_{Ref} = 25\text{nA}$ .

Delay Bit 1	10 $\mu\text{s}$
Delay Bit 7	122 $\mu\text{s}$
High time Bit 1	301.6 $\mu\text{s}$
High time Bit 7	57.6 $\mu\text{s}$
Frequency	2.86 kHz (Interval = 350 $\mu\text{s}$ , Duration = 175 $\mu\text{s}$ )

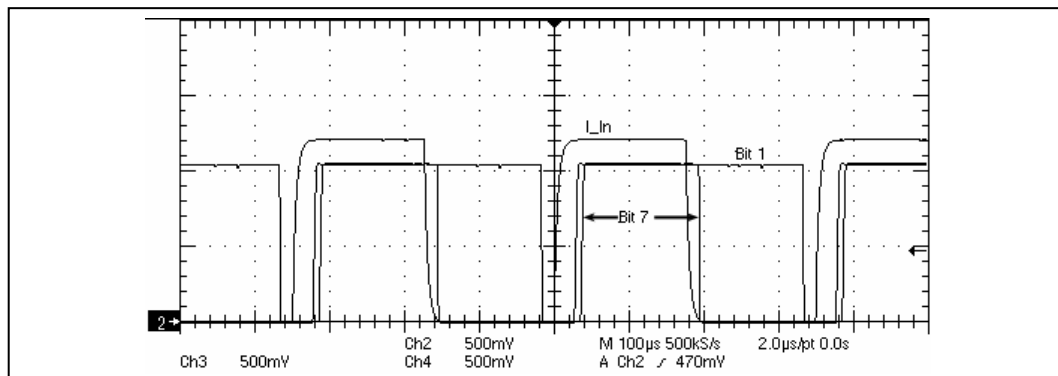
#### 4.6.7

##### Dynamic Tests with $V_{DD}$ Variation

As shown in the DC tests previously, in this series of experiments  $V_{DD}$  was varied and  $I_{Ref}$  kept at a constant value of 120nA.

##### 4.6.7.1

$V_{DD} = 1.0\text{V}$



**Figure 56:** Test results showing bit 1 and bit 7 for  $V_{DD} = 1\text{V}$  at  $f = 2.86\text{ kHz}$  and  $I_{Ref} = 10\text{nA}$ .

This experiment shows some astonishing reactions of the converter. By comparing Figure 54 with Figure 56, it becomes clear that the converter actually works better and faster when the supply voltage is very low. It reaches 2.86kHz with  $V_{DD} = 1\text{V}$ , whereas it was only capable of 1kHz when  $V_{DD}$  was 5V. Also, the delay time difference between bit one and bit seven is now only 8.8 $\mu\text{s}$ , which is less than a factor of 1.5 (in the experiment shown in Figure 54 the factor was 6).

**Table 10:** Measurements at maximum frequency for  $V_{DD} = 1\text{V}$ .

Delay Bit 1	20.8 $\mu\text{s}$
Delay Bit 7	28.8 $\mu\text{s}$
High time Bit 1	300.8 $\mu\text{s}$
High time Bit 7	155.2 $\mu\text{s}$
Frequency	2.86 kHz (Interval = 350 $\mu\text{s}$ , Duration = 175 $\mu\text{s}$ )

4.6.7.2

$V_{DD} = 1.5V$

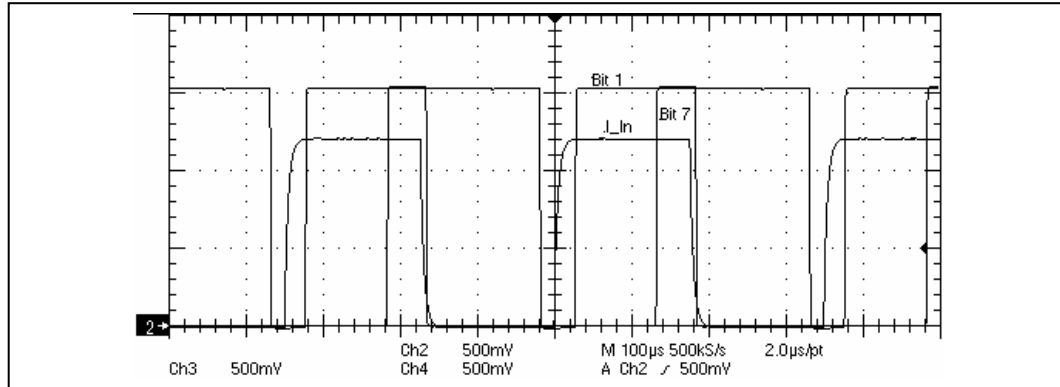


Figure 57: Test results showing bit 1 and bit 7 for  $V_{DD} = 1.5V$  at  $f = 2.86$  kHz and  $I_{Ref} = 10nA$ .

Data in Table 11 shows that there is no difference in the maximum conversion frequency if  $V_{DD}$  is 1V or if it is 1.5V. But the 0.5V difference in power supply amplitude can be seen in the delay and high times of the two measured bits. There is a difference of a factor six between the delay times of bit one and seven (the factor was 1.5 at  $V_{DD} = 1V$ ), and there is a factor of six in the difference between the high times of bit one and seven (the factor was 2 at  $V_{DD} = 1V$ ).

Table 11: Measurements at maximum frequency for  $V_{DD} = 1.5V$ .

Delay Bit 1	19.8 µs
Delay Bit 7	125.6 µs
High time Bit 1	300.8 µs
High time Bit 7	48.8 µs
Frequency	2.86 kHz (Interval = 350 µs, Duration = 175 µs)

4.6.7.3

$V_{DD} = 3.0V$

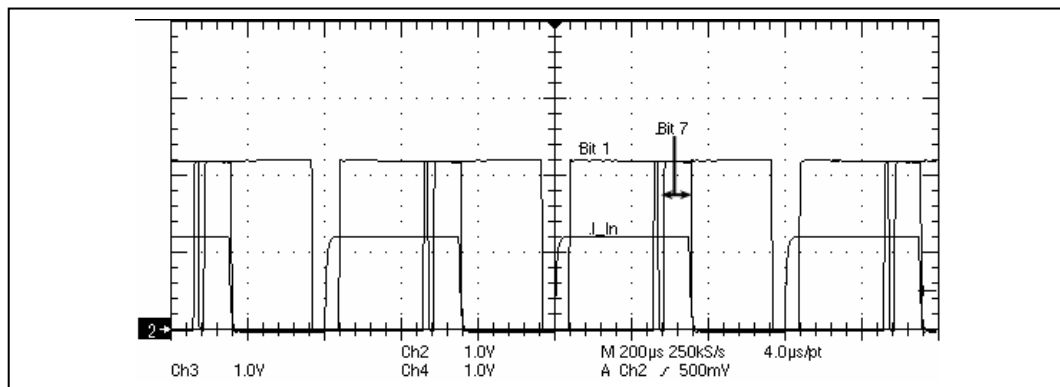


Figure 58: Test results showing bit 1 and bit 7 for  $V_{DD} = 3V$  at  $f = 1.67$  kHz and  $I_{Ref} = 10nA$ .

Finally, as the last of the dynamic experiments,  $V_{DD}$  is raised to 3V. This leads to a decreased maximum conversion frequency of 1.67kHz compared to a power supply voltage of 1.5V.

**Table 12:** Measurements at maximum frequency for  $V_{DD} = 3V$ .

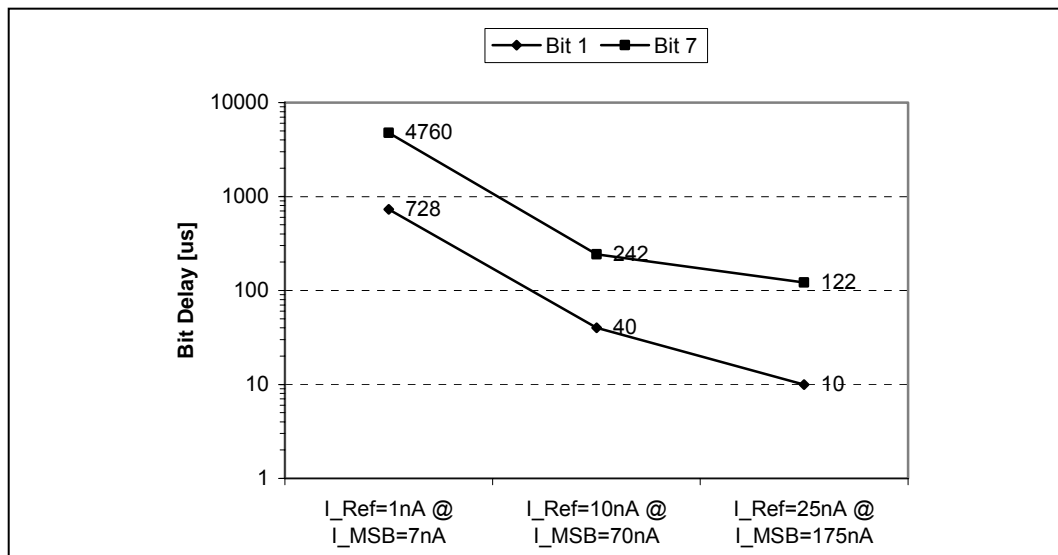
Delay Bit 1	28.6 $\mu s$
Delay Bit 7	277.6 $\mu s$
High time Bit 1	524.3 $\mu s$
High time Bit 7	70.1 $\mu s$
Frequency	1.67 kHz (Interval = 600 $\mu s$ , Duration = 350 $\mu s$ )

## 4.7

### Dynamic Performance Analysis

The dynamic performance analysis visualizes the data gained from experiments with the converter in sections 4.6.6 and 4.6.7. It compares the measured properties *delay time*, *bit high time* and *frequency* as they were measured during the different dynamic experiments which were performed.

Figure 59 compares the bit delay times of the three experimental series in which  $I_{Ref}$  was 1nA, 10nA and 25nA, respectively. In order to make them more comparable, a logarithmic scale was chosen for the X-axis of the graph which represents the bit delay in  $\mu s$ .



**Figure 59:** Delay comparison for different input currents.

In Figure 60, the bit high times are being compared. The differences in high time length were so big that a logarithmic scale for the X-axis was also used.

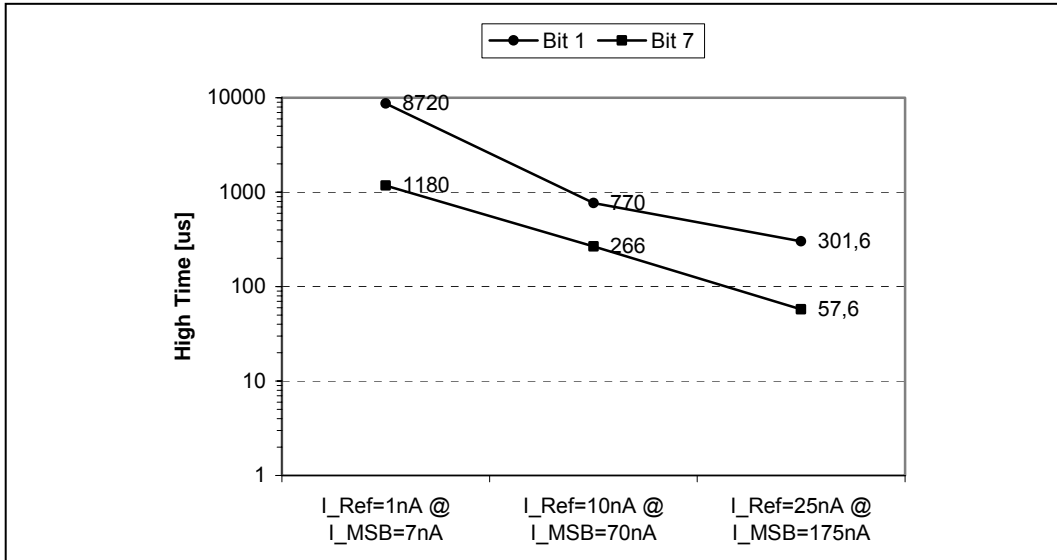


Figure 60: Comparison of bit high times for different input currents.

Figure 61 compares the maximum possible conversion frequencies which are possible for a certain reference current. Although the frequency difference between the experiment with  $I_{Ref} = 1nA$  and the experiment with  $I_{Ref} = 25nA$  is considerable, they still were plotted on a graph with a linear scaled X-axis. The range of frequencies shown is between 0.1kHz and 2.86kHz. Obviously, there is a linear dependence between the used reference voltage and the maximum obtainable conversion speed.

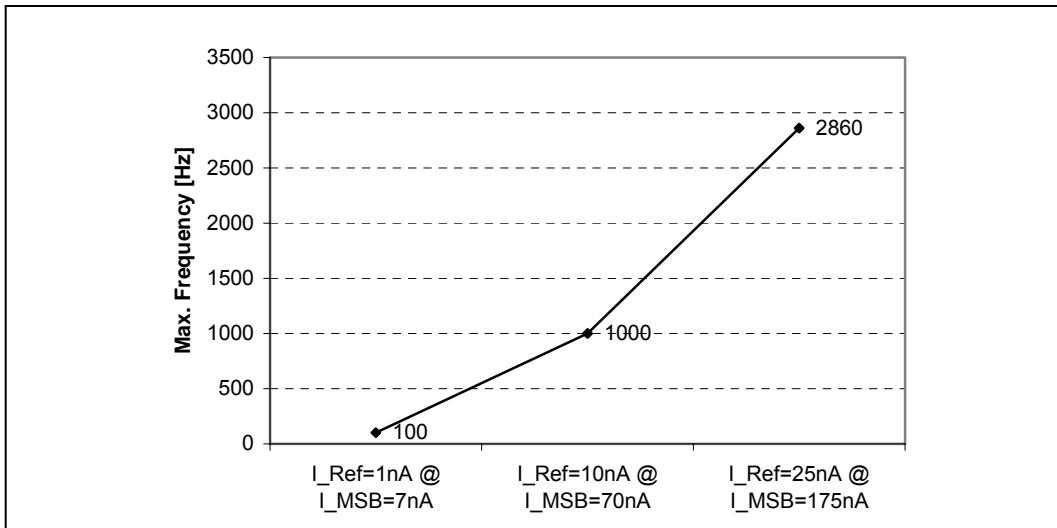


Figure 61: Maximum possible conversion frequency for different current input levels.

## 4.8

### Conclusions

The development of the multiplying A/D converter was shown beginning with early theoretical considerations, to the simulation phase and the production step. Finally, experiments with the real circuit were performed and measurements were taken. The experiments covered DC as well dynamic tests. All experimental results were discussed using figures and data tables.

The results of the multiplication factor tests show that with an increasing number of bits, the multiplication errors increase. As a result, the linearity of the converter is affected.

DC tests showed that the design is capable of working accurately for reference currents ranging from 1 to 30 nano amperes. The power supply voltage for the chip was varied between one and five volts, for all voltages the results were good.

In dynamic tests with reference currents between 1 and 25 nano amperes, the maximum possible frequency was measured together with various other parameters. These results have been compared with each other. The converter proved to allow conversion rates up to 2.86kHz.

## 5 Subthreshold Current-Mode ADC based on Current Division

### 5.1

#### Requirements and Goals

This chapter describes the second A/D converter, which was designed, laid out and fabricated in parallel with the on current multiplication based A/D converter approach from the previous chapter. Similarly to the current multiplication based approach, this A/D converter must also be capable of operating at extremely low voltages whilst having a resolution in the single nano amperes range. Another requirement is to have seven bits thermometer code as output of the converter cell. This second approach of an analog current mode A/D converter improves on the first approach in regards of speed, resolution, linearity, size and power consumption.

### 5.2

#### Principle of Operation

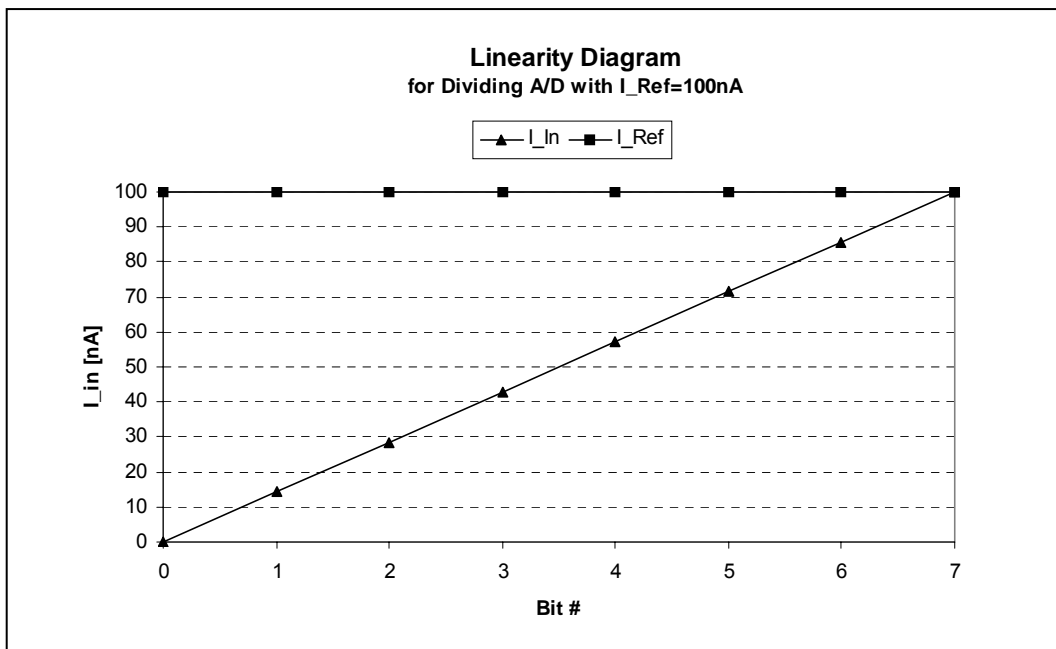
The idea behind this converter is to divide a reference current by a number of different divisors to obtain a linear increasing set of currents to which the input current can be compared. While  $I_{Ref}$  represents the full scale input of the converter, the LSB is, in this case, is always  $1/7 * I_{Ref}$ . This brings us back to the principle of operation of the voltage mode flash converter, where a chain of equal resistors divides a reference voltage into  $N$  voltages which increase by the value of the LSB from stage to stage. The design is also about a flash architecture, in which a copy of the current which we want to convert is fed directly to a comparator. Therefore, for each bit of the thermometer code a separate comparator is required.

Improvements over its on multiplication based competitor are primarily expected with regard to its operation speed and linearity. In contrast to the multiplication technique, current division can be accomplished using Ohm's law. To do so, the reference current simply has to be copied several times with current mirrors and then split up again into fractions by using current mirrors. The algorithm which follows this principle looks like this for bit one to bit seven:

<b>Bit 1:</b>	If $\frac{1}{7} I_{Ref} > I_{In}$	→ high
	Else	→ low
<b>Bit 2:</b>	If $\frac{2}{7} I_{Ref} > I_{In}$	→ high
	Else	→ low

<b>Bit 3:</b>	If $\frac{3}{7} I_{\text{Ref}} > I_{\text{In}}$	→ high
	Else	→ low
<b>Bit 4:</b>	If $\frac{4}{7} I_{\text{Ref}} > I_{\text{In}}$	→ high
	Else	→ low
<b>Bit 5:</b>	If $\frac{5}{7} I_{\text{Ref}} > I_{\text{In}}$	→ high
	Else	→ low
<b>Bit 6:</b>	If $\frac{6}{7} I_{\text{Ref}} > I_{\text{In}}$	→ high
	Else	→ low
<b>Bit 7:</b>	If $\frac{7}{7} I_{\text{Ref}} > I_{\text{In}}$	→ high
	Else	→ low

For clarification of the operation principle, refer to the diagram shown in Figure 62. The data series labeled with square shaped boxes represents the statically present reference current of 100nA. The other data series, identified by triangle shaped markers, represents the switching positions of the bits. Each triangle corresponds to a current at which the corresponding bit will switch from low to high (or from high to low if the current is lowered instead of raised).

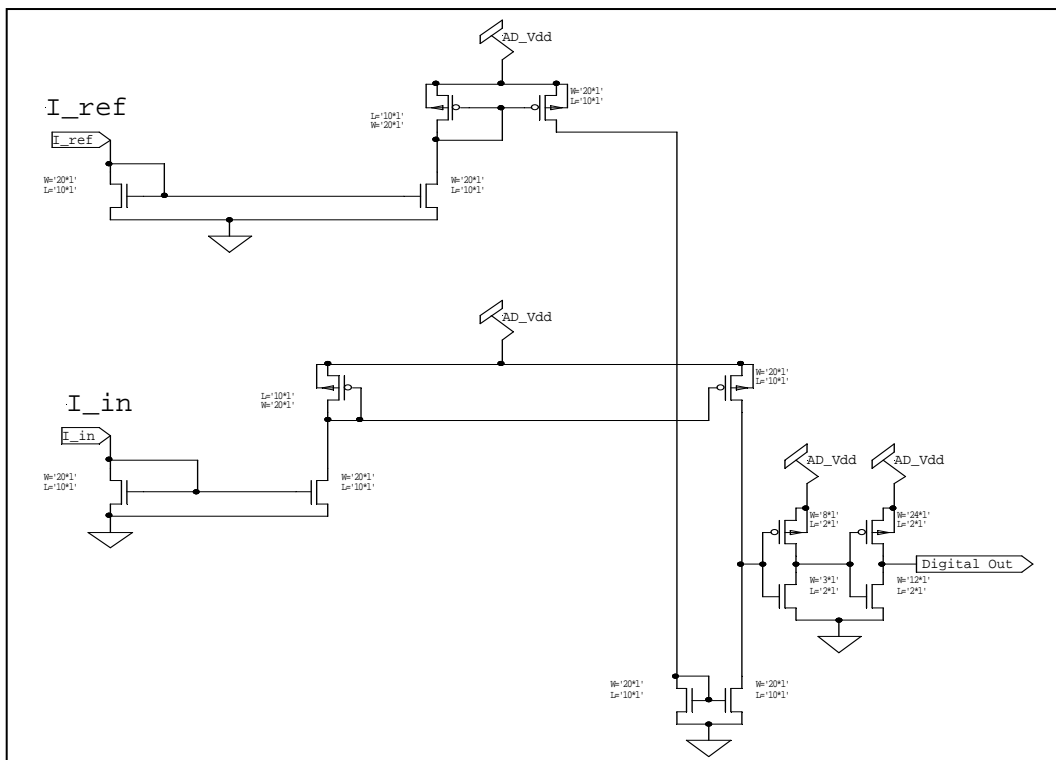


**Figure 62:** In this figure, bits 1- 7 are shown to switch at the positions marked with triangle shaped markers. For an input current  $I_{\text{In}} = 100\text{nA}$ , bit one would switch at  $1 \cdot 14,2\text{nA}$ , bit 2 at  $2 \cdot 14,2\text{nA}$ , ... and bit 7 at  $7 \cdot 14,2\text{nA}$ .

### 5.3 Schematics

Figure 63 shows one bit cell of the design. It is made up of three  $n$ -mirrors, two  $p$ -mirrors and one comparator.  $I_{Ref}$  is mirrored by an  $n$ -mirror first, followed by a  $p$ -mirror. Thus its value is unchanged at this point (despite the inaccuracies of the mirrors) and can be compared directly to the reference current to determine the logical state of bit seven. The comparator used here only consists of two inverter stages unlike the comparator which was used in the multiplying A/D converter's design. This leads to the same switching behavior as seen in the other converter. When  $I_{in}$  is raised from zero to full scale, one bit after another will go from *low* to *high*. If a comparator with three inverters had been used, their logic values would have changed from *high* to *low* for the same stimulation.

Given that the converter has to deliver seven bits of thermometer code, seven bit cells are needed. They all look different, but the way they work is the same for all of them. The design as a whole, as shown in Figure 64, performs a series of static current divisions to generate seven different currents to which the input current can be compared to. This can be explained using the  $I_{in}$  current copy chain which is made up of one  $n$ - and one  $p$ -mirror. The  $p$ -mirror has seven transistors connected in parallel, so that it provides seven identical copies of the input current in the form of a current source. These current sources are each connected to a separate comparator.



**Figure 63:** Schematic of a single bit cell of the A/D converter based on current division.



The division of  $I_{\text{Ref}}$  is slightly more complicated. Consider a copy of  $I_{\text{Ref}}$ , as seen in the single bit cell in Figure 63, this current is then split into seven equal parts by connecting it to seven parallel connected  $n$ -mirrors, functioning as current sinks. Assuming that these seven parallel  $n$ -mirrors all have exactly the same electrical properties, the current will inevitably split up into seven identical portions, following Kirchhoff's current law. For bit number one (the LSB), it is sufficient to compare this current directly to  $I_{\text{Ref}}$ . For the second bit, two of the LSB currents have to be added together and then be compared to  $I_{\text{Ref}}$ . The very same rules apply to the currents which are formed to determine the logical state of bit three, four, five and six. For the seventh bit,  $I_{\text{in}}$  is directly compared to  $I_{\text{Ref}}$ . This comes from the fact that seven LSB currents added together sum up to  $I_{\text{Ref}}$ . Due to the fact that it is more accurate, size, and power efficient to use just one  $n$ -mirror instead adding together the current output of seven of them, this appears to be the best solution.

Finally, the whole converter consists of 27  $n$ -MOS and 62  $p$ -MOS transistors. With a total of 89 transistors, it seems to be a very promising design concerning size requirement and expected power dissipation.

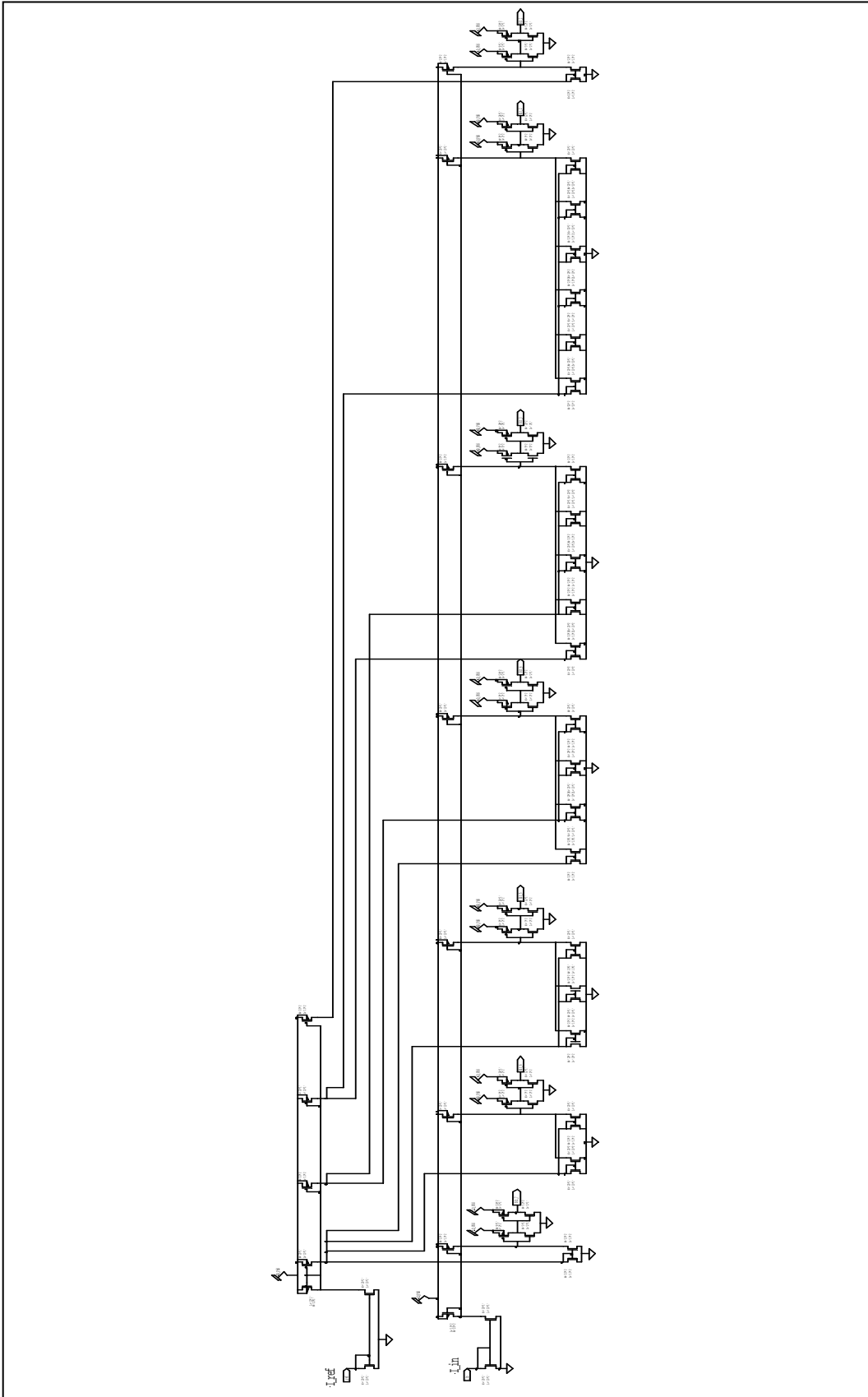
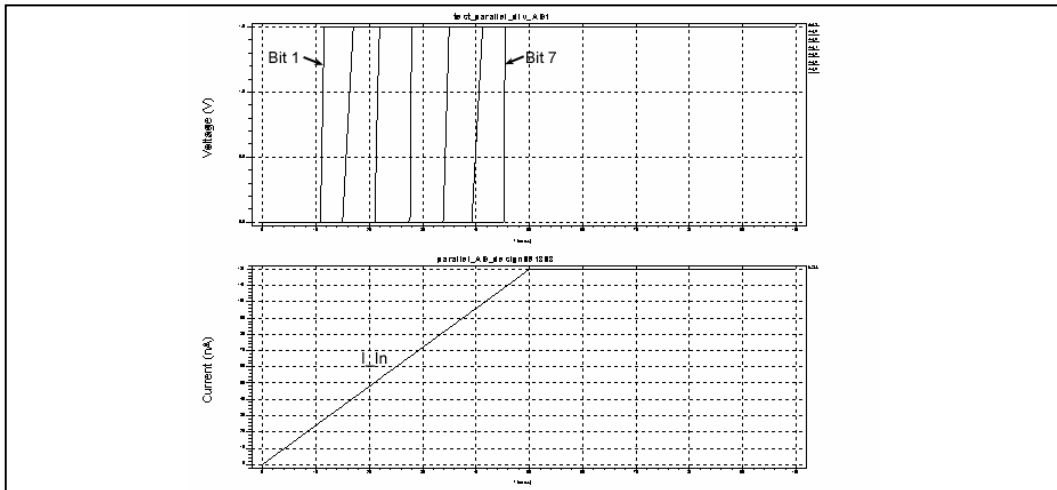


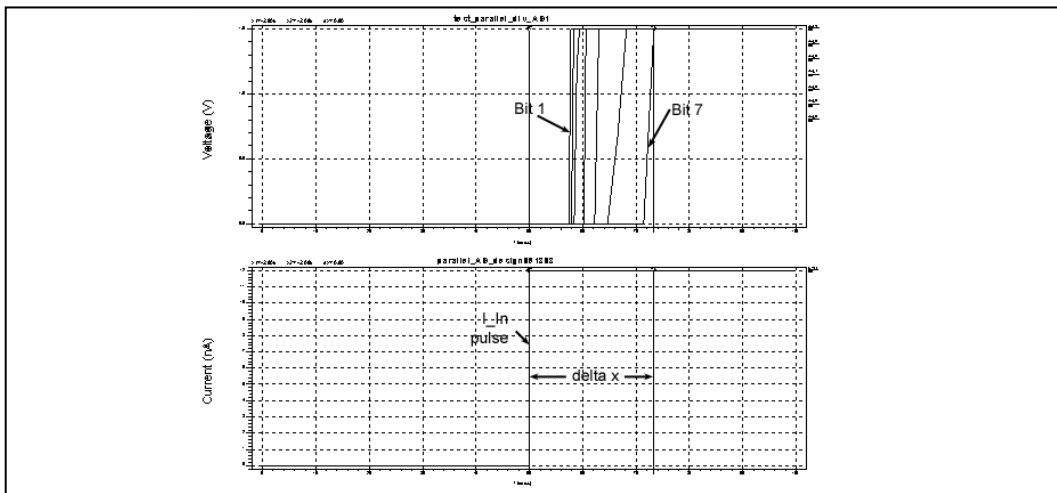
Figure 64: Schematic of the A/D converter based on current division.

### 5.4 SPICE Simulation

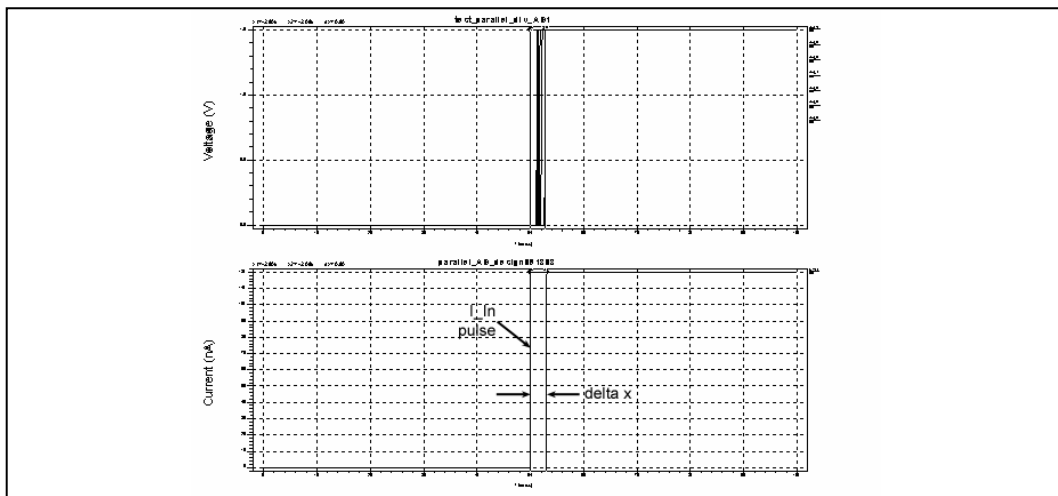
The SPICE simulation results show that the operation principle works in theory. For the simulations shown in this section, exactly the same software tools were used as in the previous SPICE simulations (*T-SPICE Pro v9.02*, *S-Edit v8.1* and *W-Edit v9.02*). Furthermore, the BSIM3 transistor model was utilized to emulate the transistor's physical properties. In Figure 65, the input current  $I_{in}$  raises from 0 to 120nA, while the reference current  $I_{Ref}$  stays at a constant level of 100nA. As expected, bits 1 to 7 are all switching from *low* to *high* one after another. The linearity of the system can be seen by looking at the distances at which the switching takes place. They all seem to be fairly equidistant from each other, thus the converter has good overall conversion linearity. Detailed measurements with the circuit are performed and analyzed in the *Experimental Results* section of this chapter.



**Figure 65:** SPICE simulation of the dividing A/D converter. The input current  $I_{in}$  climbs from 0-120nA, the reference current is  $I_{Ref} = 100nA$ .



**Figure 66:** Response of the dividing A/D converter to a simulated current pulse of 12nA.  $I_{Ref} = 10n$ ,  $\Delta x = 23ns$ .



**Figure 67:** Response of the dividing A/D converter to a simulated current pulse of 120nA.  $I_{Ref} = 100n$ ,  $\Delta x = 2,8ns$ .

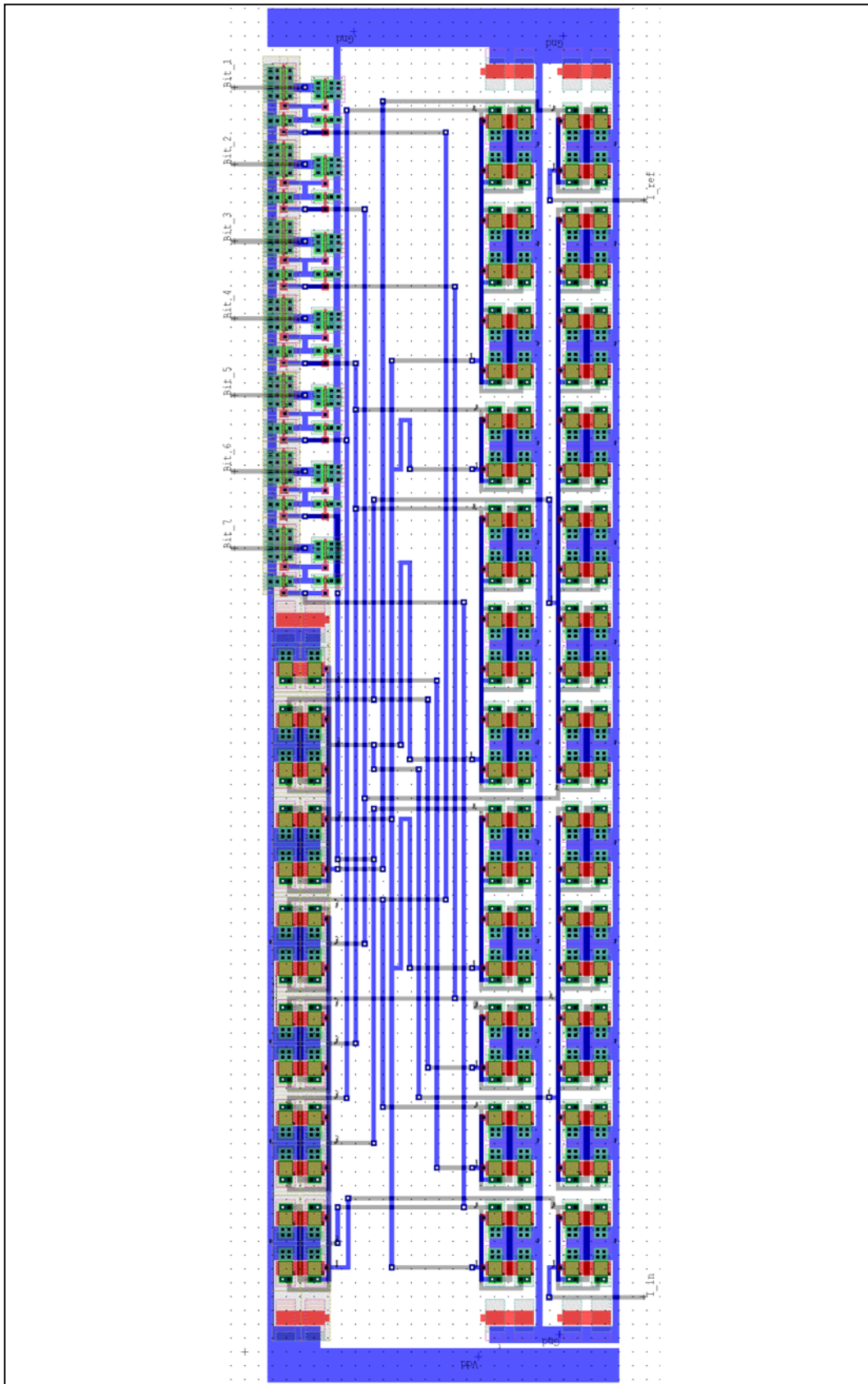
## 5.5

### Layout

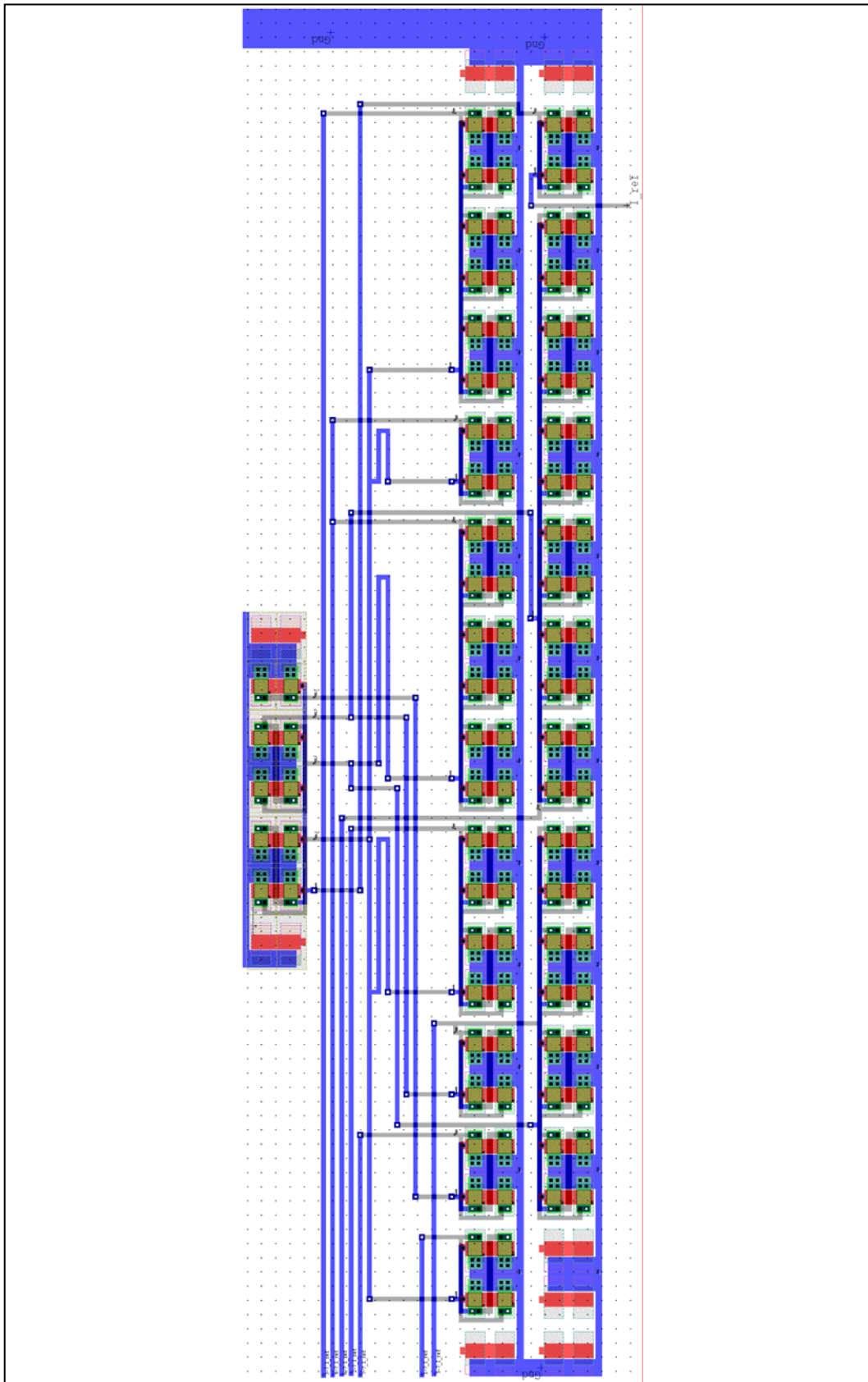
In the layout for this converter current mirror cells and current comparator cells were used in repetition. Most of these cells have already been used in the on current multiplication based approach, so they did not have to be drawn again. For the layout development on the PC, *L-Edit* (v10.12) has been used. It is hard to believe that the most challenging layout step is the wiring of the basic building blocks. However, it takes up most of the time and requires full concentration. In the case of this dividing converter, wiring has to be done extremely carefully. This is because the actual division accuracy is influenced by the length of the wires which connect the current source, a copy of  $I_{\text{Ref}}$ , with the current comparator. This drawback of the circuitry can be compensated by measuring the resistance of the wires. Additional complexity arises from the fact that *metal1* and *metal2* have a different specific resistance, so that the wires formed by the different layers have to be measured independently from each other. Layout goal is that all these wires have the same total resistance, including additional resistances caused by vias. To achieve that, it is possible to form additional loops in the wires. This approach is demonstrated in Figure 68. When viewed in landscape format, the additional wire loops, used to balance the wire resistances, can be found in the middle of the schematic in a horizontal row.

Theoretically, the layout prohibits the making of copies of the currents which are generated by division. If another current mirror would be added to access and measure the current from outside the chip, the whole operation principle would be disrupted. This is because an additional current mirror would mean that the reference current would not be divided by seven any more, but by eight. To overcome these problems, the converter design was first modified slightly and then implemented on the chip, only serving to measure the division accuracy which is realized. The layout for this modified converter (it is not a real converter because it lacks an input current network or any comparator) is shown in Figure 69.

The layout of this division accuracy test circuit consists of only 5  $p$ -mirror cells and 46  $n$ -mirror cells. Its only input is the input for the reference current, which gets divided as described for the real converter. The seven fractions of the reference current which are generated by it are then forwarded to a pin of the chip so that they can be measured by using the current-to-voltage converter which is located on the prototype test bed. Of course, this extra circuit will not be needed for any future applications of the A/D converter, but will help in determining the division accuracy and find possible design errors or problems. Results of the so-called *division factor tests* can be found in section 5.6.1.



**Figure 68:** Layout of the A/D design based on current division.



**Figure 69:** Layout of the division test circuit, enabling testing of the actual division accuracy of the design.

## 5.6

### Experimental Results

To test the performance of the dividing A/D converter, all experiments which were carried out with the multiplying A/D converter before were repeated. Thus, there are the two categories *DC Tests* and *Dynamic Tests*. Furthermore a series of tests was performed to determine the accuracy of the division of currents which are used in the different stages of the converter.

#### 5.6.1

##### Division Factor Tests

As already mentioned, a second circuit was used for the purpose of measuring the division accuracy. It is a modified version of the dividing A/D converter circuit. Assuming that local variations on the chip surface do not significantly alter the accuracy of the current dividers, it is possible to determine how well current division based on parallel current mirrors works in practice.

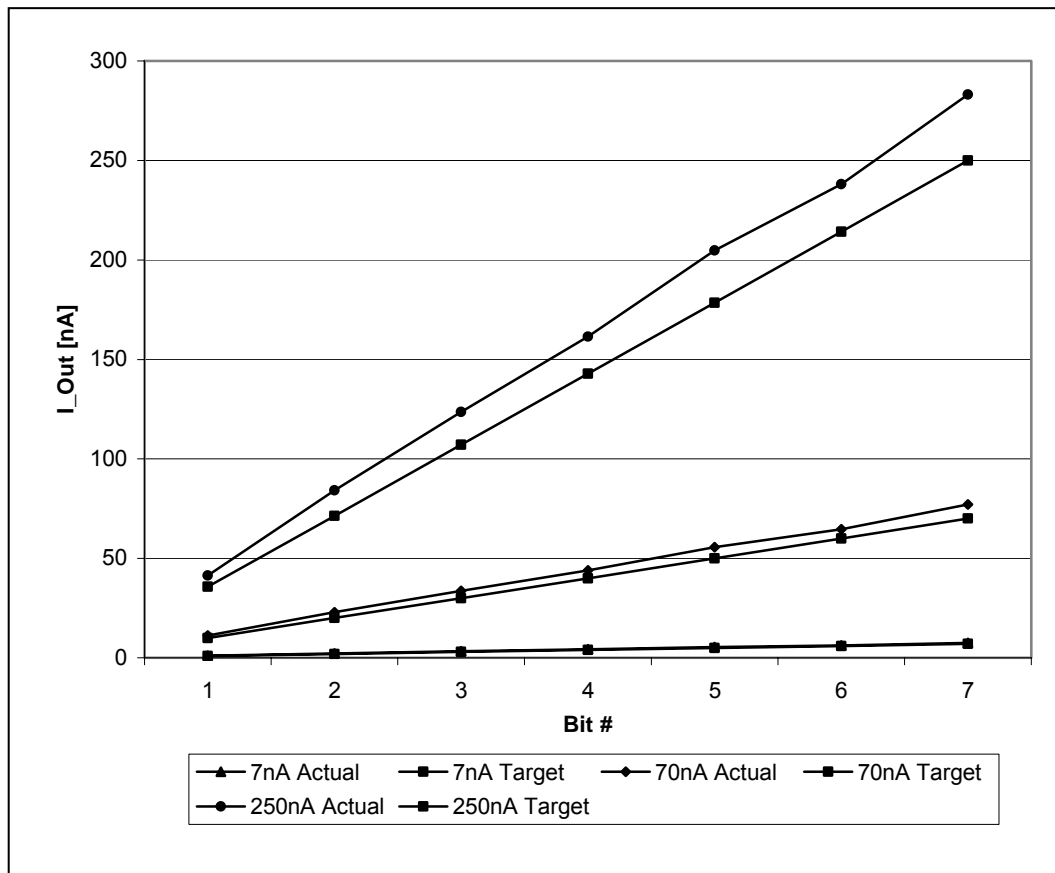
Naturally the currents which are to be measured are in the range of nano amperes, so it will be necessary to use the off-chip circuit, a current-voltage converter and amplifier which also was used previously in the *Multiplication Factor Tests* in section 4.6.3. To be able to conveniently measure these seven currents and avoid the need of seven discrete measurement circuits, a ten way thumbnail switch was integrated on the prototype board, acting like a multiplexer for the currents.

Table 13 shows the measured currents of all seven bits of the converter for three different test series. The first series uses a reference current of 7nA, in the second one  $I_{\text{Ref}}$  is 70nA and in the third one it was raised to 250nA. For each bit of the converter the target and the actual  $I_{\text{in}}$  current level is given at the corresponding bit which is supposed to switch to its logic state. Beyond that the absolute error of the deviation from the target current level is given. The diagram shown in the Figure 70 indicates how big these deviations are based on looking at the whole data series. While the ideal conversion data points are identified by a square shaped marker, the actually measured data points of the different data series are labeled according to the legend which can be found below the diagram. At first view it seems obvious that the division errors become larger the higher the reference current (and with it the input current). This is not entirely true if you consider the absolute numbers of the error rates shown in Table 13. According to this, there is an average error rate of 10.27% for  $I_{\text{Ref}} = 7\text{nA}$ , 11.34% for  $I_{\text{Ref}} = 70\text{nA}$  and 14.43% for  $I_{\text{Ref}} = 250\text{nA}$ .



**Table 13:** Measured division factors from the real chip.

	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
$I_{Ref} = 7nA$	Target: 1nA Actual: 1.1nA Error: +10%	Target: 2nA Actual: 2.3nA Error: +15%	Target: 3nA Actual: 3.4nA Error: +13.3%	Target: 4nA Actual: 4.4nA Error: 10%	Target: 5nA Actual: 5.5nA Error: 10%	Target: 6nA Actual: 6.3nA Error: 5%	Target: 7nA Actual: 7.6nA Error: 8.6%
$I_{Ref} = 70nA$	Target: 10nA Actual: 11.3nA Error: +13%	Target: 20nA Actual: 23.0nA Error: +15%	Target: 30nA Actual: 33.7nA Error: +12.3%	Target: 40nA Actual: 44.0nA Error: +10%	Target: 50nA Actual: 55.7nA Error: +11.4%	Target: 60nA Actual: 64.6nA Error: +7.6%	Target: 70nA Actual: 77.1nA Error: 10.1%
$I_{Ref} = 250nA$	Target: 35.7nA Actual: 41.3nA Error: +15.7%	Target: 71.4nA Actual: 84.1nA Error: +17.8%	Target: 107.1nA Actual: 123.6nA Error: +15.4%	Target: 142.8nA Actual: 161.4nA Error: +13%	Target: 178.5nA Actual: 204.8nA Error: +14.7%	Target: 214.2nA Actual: 238.1nA Error: +11.1%	Target: 250nA Actual: 283.2nA Error: 13.3%



**Figure 70:** Visual representation of the measured division factors.

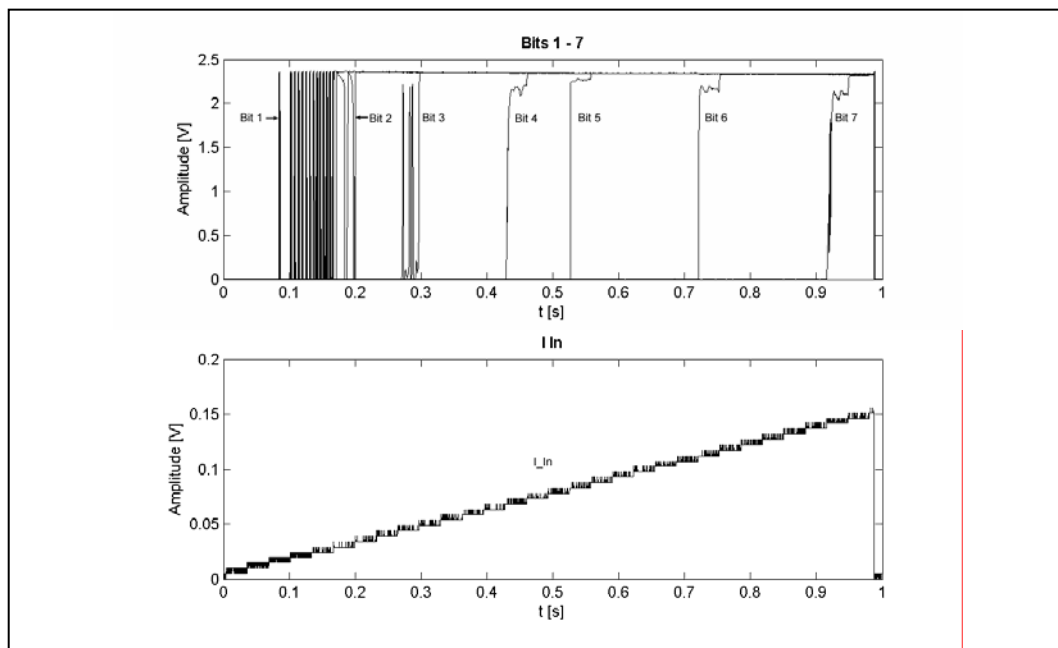
## 5.6.2

### DC Tests with $I_{Ref}$ Variation

Similarly to earlier experiments, the measurements were carried out using the National Instruments DAB. Controlled by a DAB module for *LabView*, it produces a 1Hz saw tooth voltage available to the voltage controlled current generator. This voltage is measured for reference together with the output signals of bits one to seven of the converter.

#### 5.6.2.1

$I_{Ref} = 10nA$



**Figure 71:** Bits 1- 7 triggered by a saw tooth shaped input current providing the full scale input for the converter with a reference current of  $I_{Ref} = 10nA$ .

Figure 71 shows the response of the dividing current converter which was implemented on the chip. It is driven by an input current ranging between zero and 15nA. The reference current in this experiment was 10nA. Due to the extreme small currents, we see bit one oscillating for about 80ms. This could be a consequence of the input voltage which gets converted into an input current. The problem here is that the source of this voltage is the DAB which is limited in its minimal voltage step size resolution. Also, the accuracy of the voltage supplied is not ideal. In the lower panel of Figure 71 you can see that the voltage driving  $I_{in}$  increases in discrete steps of 5mV. It is also apparent that the voltage swing of the DAB is 5mV. Since this almost represents  $\frac{1}{2} * LSB$  of the converter, it is unsurprising that bit one oscillates for a while.

Figure 72 visualizes the deviation in linearity from the ideal 100% linear conversion line. It is especially demonstrative that bits six and seven in this experiment deviate more from the ideal line than the other bits.

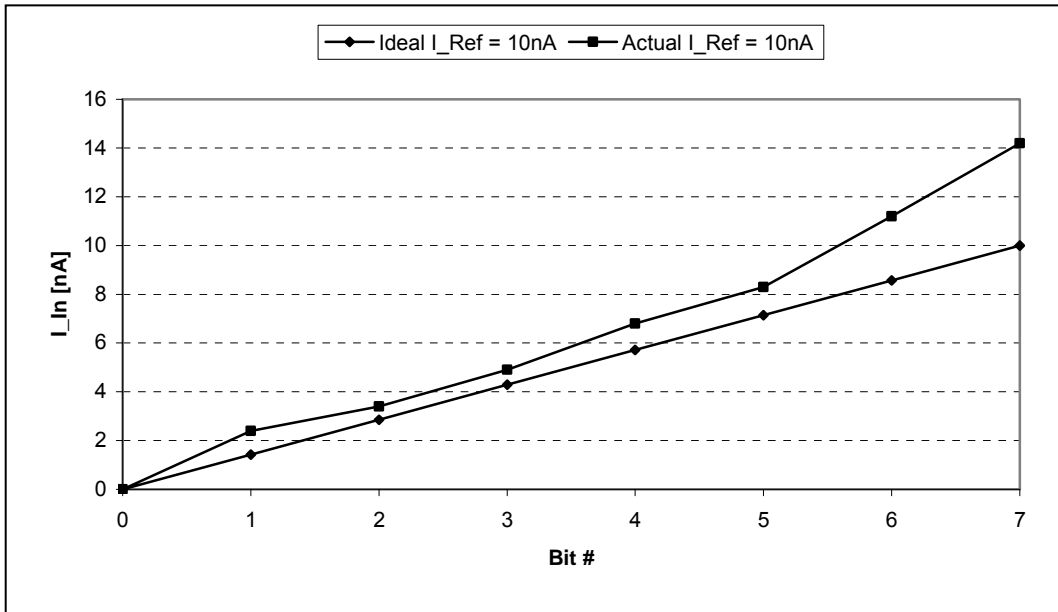


Figure 72: Variance of the actual conversion curve from the ideal conversion curve for  $I_{Ref} = 10nA$ .

5.6.2.2

$I_{Ref} = 100nA$

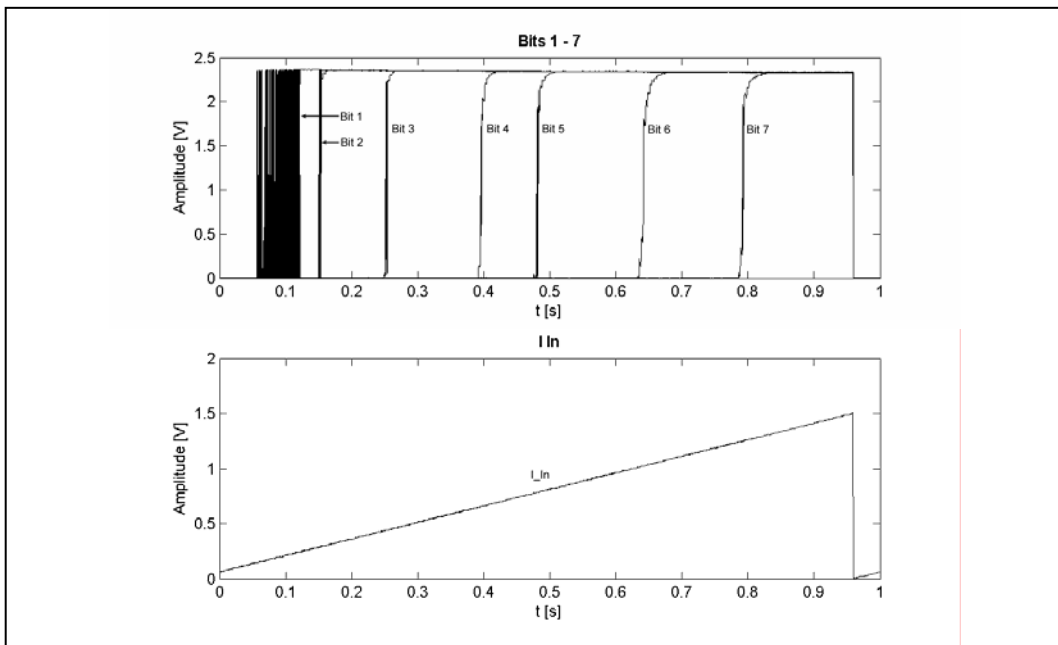
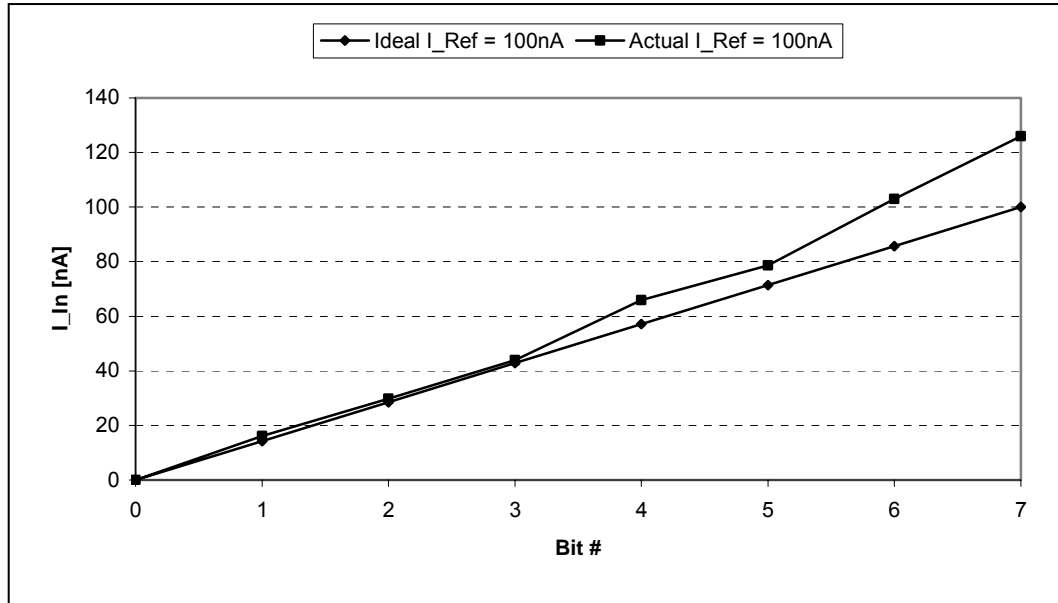


Figure 73: Bits 1- 7 triggered by a saw tooth shaped input current providing the full scale input for the converter with a reference current of  $I_{Ref} = 100nA$ .

In this experiment a reference current of  $I_{Ref} = 100nA$  and an input current ranging between 0 – 150nA was used. As 150nA translate to 1.5V, the DAB’s inability to deliver

voltage steps smaller than 5mV does not have such a big impact on the converter's switching behavior any more.



**Figure 74:** Variance of the actual conversion curve from the ideal conversion curve for  $I_{Ref} = 100\text{nA}$ .

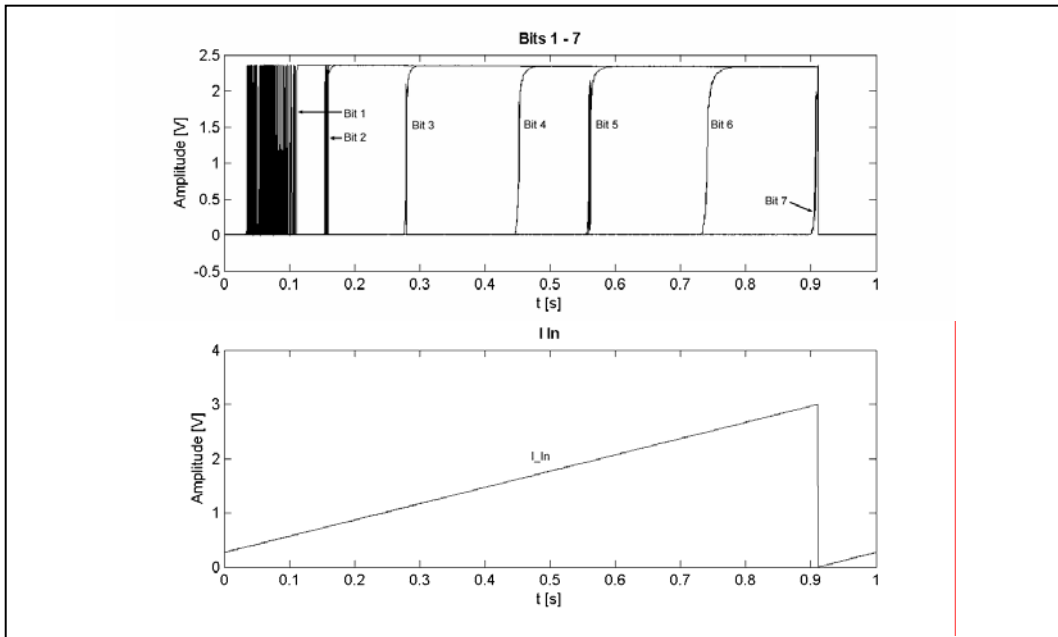
In Figure 73, bit one is still oscillating before it stabilizes in the logical state high. However, there is less oscillation occurring compared to the previous experiment. In Figure 74, bits one to three show an almost linear switching behavior. While bits four and five slightly deviate from the ideal line, bit six and seven show more error.

### 5.6.2.3

#### $I_{Ref} = 250\text{nA}$

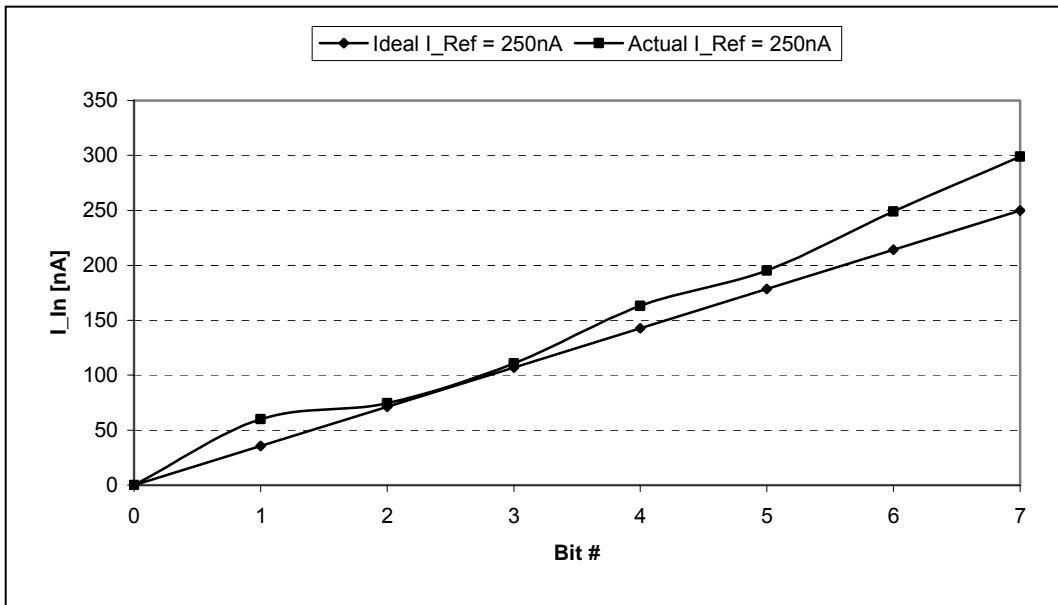
The results of the experiment with  $I_{Ref} = 250\text{nA}$  are shown in Figure 75 and Figure 76. The input current  $I_{in}$  ranges between 0 – 300nA which translates to a stimulation voltage supplied by the DAB between 0 – 3V. Bit one also oscillates in this experiment for about 70ms. Apart from that, all other bits pass the transition between low and high trouble-free. The linearity graph in Figure 76 shows that the deviation of the converter from the ideal conversion curve is minimal between bit two and three and maximal for bit six and seven.

Even though the full scale input of the converter theoretically should be the same as the reference current, this is not exactly true here. As you can see in the upper diagram of Figure 75, bit seven hardly reaches the *high* level. Although the input current has a maximum of 300nA while the reference current is only 250nA, this seems to be insufficiently high enough.



**Figure 75:** Bits 1- 7 triggered by a saw tooth shaped input current providing the full scale input for the converter with a reference current of  $I_{Ref} = 250\text{nA}$ .

This and the previous two experiments have been performed with a power supply voltage of the chip which was  $V_{DD} = 5\text{V}$ . In the next set of experiments,  $I_{Ref}$  is kept constant and  $V_{DD}$  is varied.



**Figure 76:** Variance of the actual conversion curve from the ideal conversion curve for  $I_{Ref} = 250\text{nA}$ .

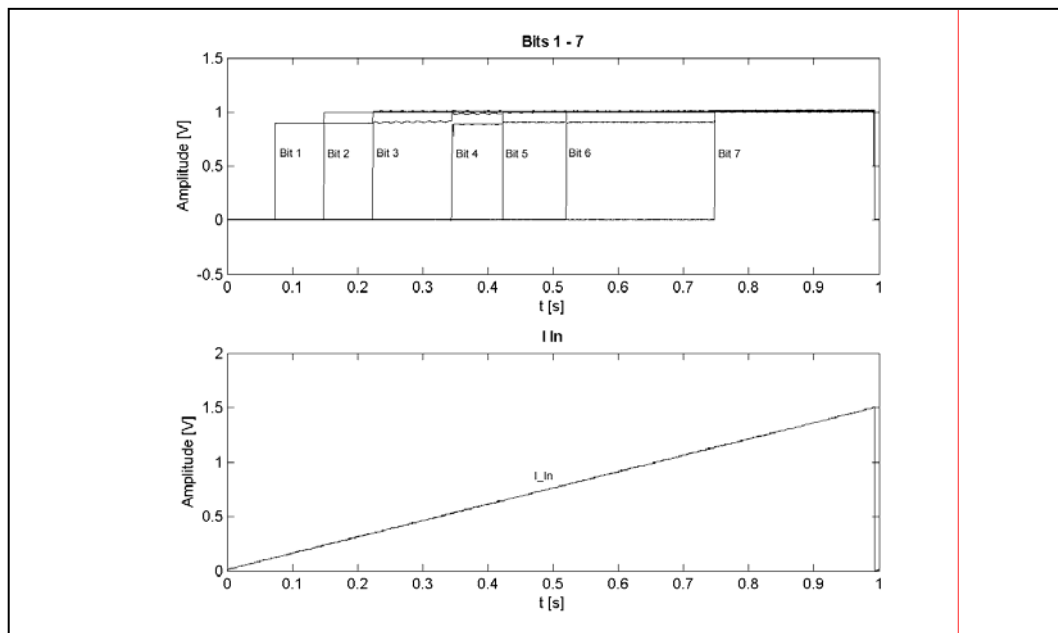
### 5.6.3

#### DC Tests with $V_{DD}$ Variation

As shown previously in the experiments with the multiplying A/D converter,  $V_{DD}$  is varied in this test series. The reference current is a constant current of 100nA, the input current raises from 0 – 150nA within one second.

##### 5.6.3.1

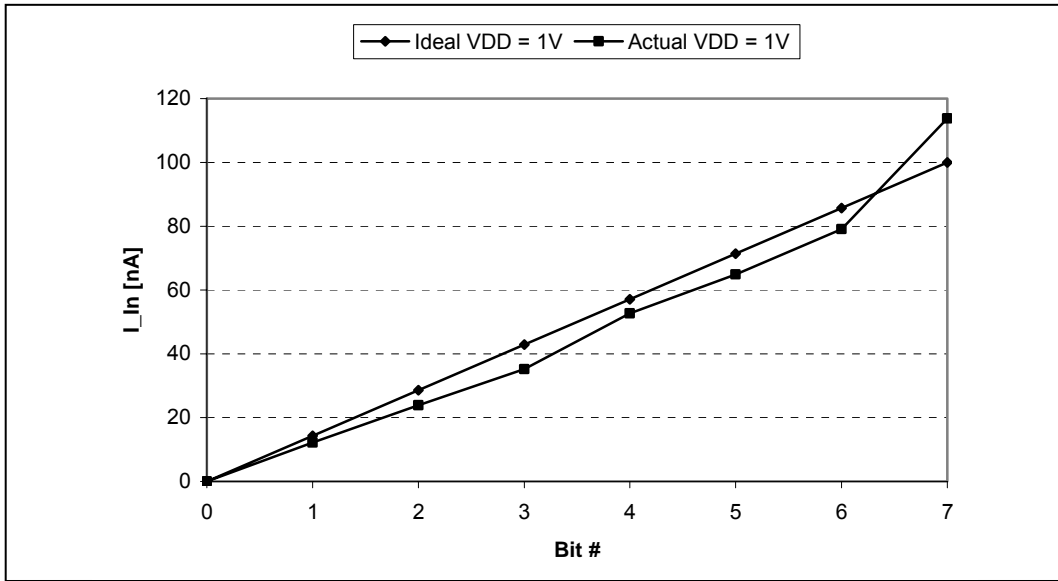
$V_{DD} = 1V$



**Figure 77:** Measurement of bits 1- 7 for  $V_{DD} = 1V$ , saw tooth shaped input of 100nA.

For the lowest possible supply voltage of 1V, the converter shows excellent results. Neither bit one is oscillating, nor has bit six or seven an extraordinary large deviation from the ideal curve. Figure 77 attests a clean and flicker free switching of all seven bits.

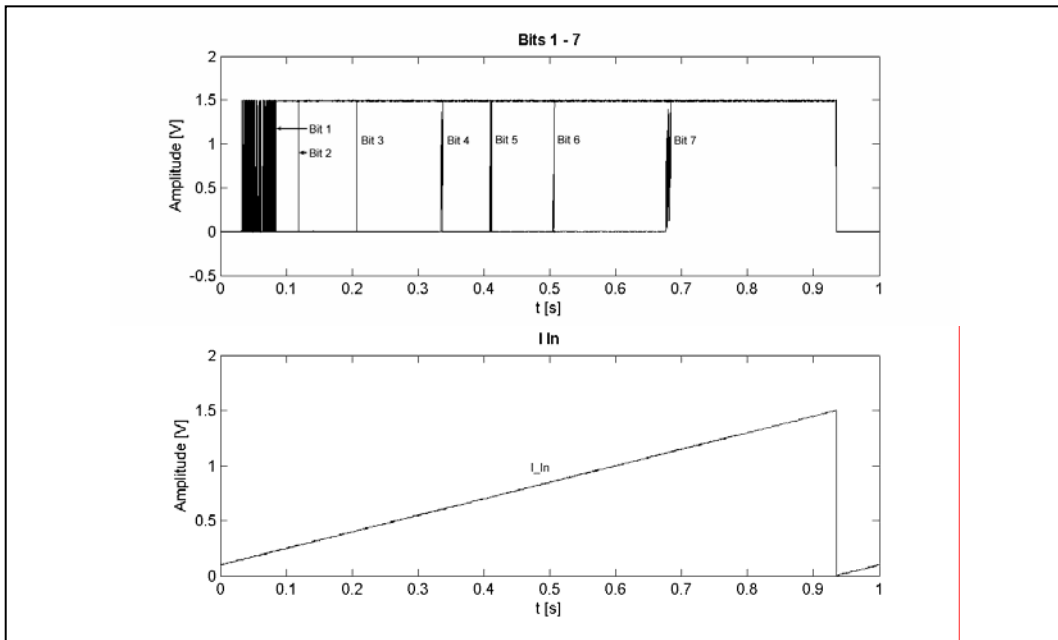
Figure 78 shows the best linearity of this converter seen so far in all the experiments. Between bit one and bit six, the curve of actual measurements remains below the curve of ideal linearity. Just bit seven seems to differ from this behaviour, since it indicates that the current necessary to switch bit seven is slightly higher than the ideal curve.



**Figure 78:** Variance of the actual conversion curve from the ideal conversion curve for  $V_{DD} = 1V$  and  $I_{Ref} = 100nA$ .

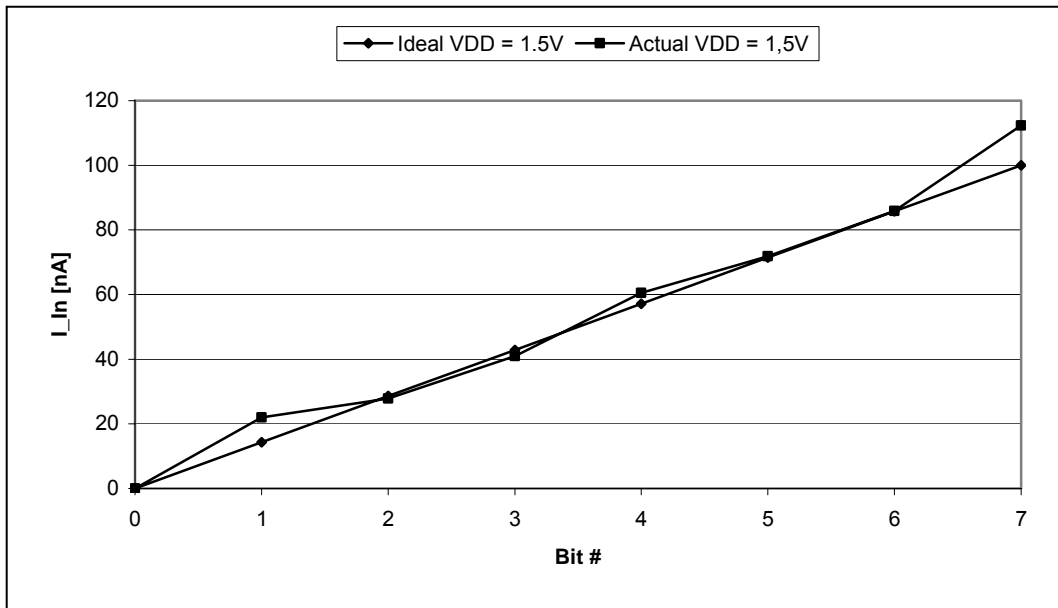
**5.6.3.2**

$V_{DD} = 1.5V$



**Figure 79:** Measurement of bits 1- 7 for  $V_{DD} = 1.5V$ , saw tooth shaped input of 100nA.

This experiment shows, that the power supply voltage is responsible for the oscillations of bit one seen in earlier experiments. The slight increase in  $V_{DD}$  from 1V to 1.5V triggers the oscillations before bit one settles.



**Figure 80:** Variance of the actual conversion curve from the ideal conversion curve for  $V_{DD} = 1V$  and  $I_{Ref} = 100nA$ .

Figure 80 shows that the increase in power supply voltage by 0.5V made the curve of actual measurements shift upwards compared to the one seen in Figure 78. The greatest differences were seen with bit one and seven, which deviate more from the ideal curve than the other bits.



5.6.3  $3V_{DD} = 3.0V$

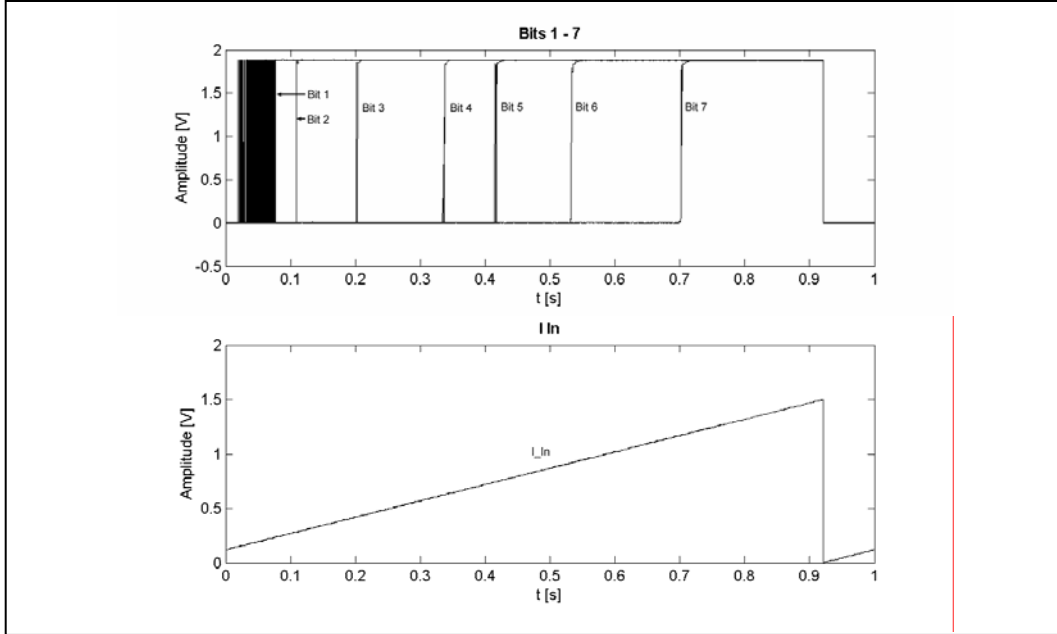


Figure 81: Measurement of bits 1- 7 for  $V_{DD} = 3V$ , saw tooth shaped input of 100nA.

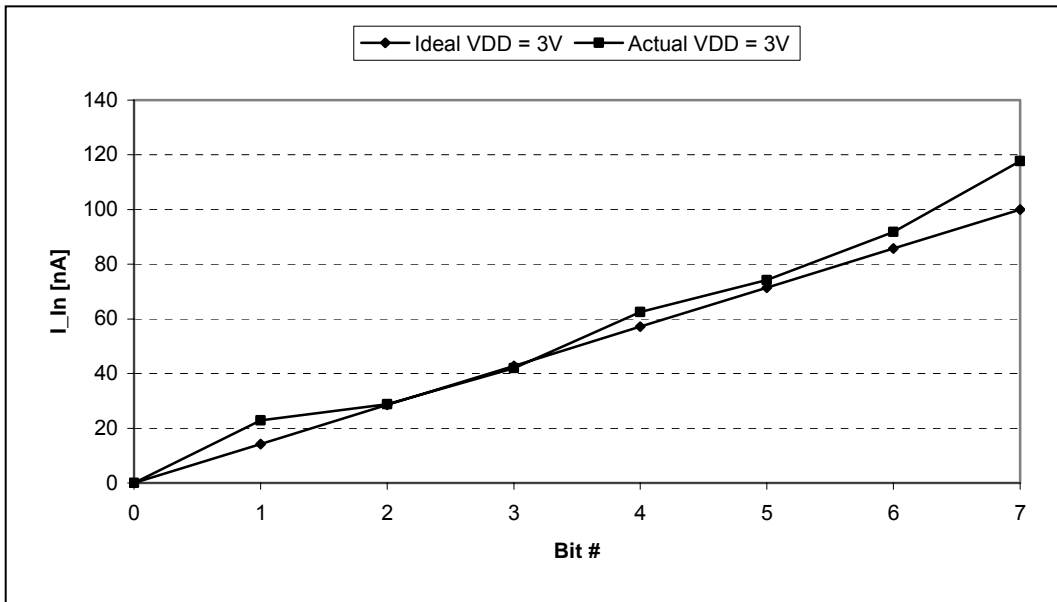


Figure 82: Variance of the actual conversion curve from the ideal conversion curve for  $V_{DD} = 3V$  and  $I_{Ref} = 100nA$ .

With a supply voltage of 3V, the measurement diagrams do not change a lot compared to the experiment with  $V_{DD} = 1.5V$ . The bit switching characteristic of Figure 81 shows quite large oscillations of bit one again, lasting for about 75ms. All other bits change their signal

level without oscillations. In the second diagram, Figure 82, the only suspicious behavior is seen for bit one and seven. Obviously, the current division error affects these two conversion stages more than the other stages.

## 5.6.4

### Dynamic Tests with $I_{Ref}$ Variation

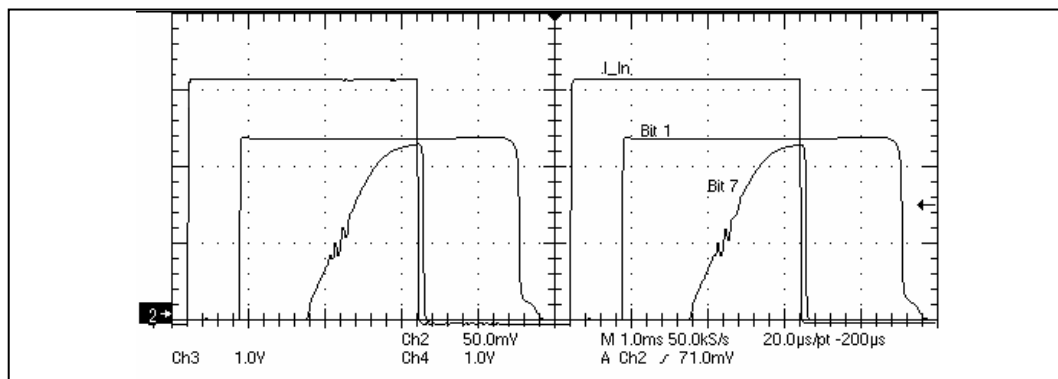
The dynamic test program determines the maximum conversion rate of the converter and measures the delay- and high-times of bit one and bit seven. Just like in the other dynamic experiments, the *Master-8 Stimulator* and the *Tektronic* oscilloscope are used to generate the stimulation signal and record the converter response. The power supply voltage is fixed in this set of experiments to a value of  $V_{DD} = 5V$ .

#### 5.6.4.1

##### $I_{Ref} = 10nA$

The first experiment employs a reference current of 10nA. The current level of the input channel ranges between 0 and 15nA. The exact test matrix with all parameters, voltages and currents can be seen in Table 5 in section 4.6.1.

In Figure 83, the dividing A/D converter reaches a conversion rate of 200Hz. The stimulation square wave  $I_{in}$  and bit one form a fairly square shaped signal. Bit seven, which should not look different in shape, has a rounded positive edge. This could be corrected by using a higher full scale input than 150nA, causing more current to flow and making the CMOS converter switch more quickly.



**Figure 83:** Test results showing bit 1 and bit 7 for  $I_{Ref} = 10nA$  at  $f = 200Hz$ .

The table below shows the exact measurements for the delay- and high-time parameters of the converter. Of course, the maximum conversion frequency is only determined by the value of the interval. The duration is separately modified to see where exactly the limits of the circuit are with regard to dynamic experiments.

**Table 14:** Measurements at maximum frequency for  $I_{Ref} = 10nA$ .

Delay Bit 1	680 $\mu s$
Delay Bit 7	2.42 ms
High time Bit 1	3.6 ms
High time Bit 7	616 $\mu s$
Frequency	200 Hz (Interval = 5 ms, Duration = 3 ms)

### 5.6.4.2

#### $I_{Ref} = 100nA$

The results of the experiment using a reference current of 100nA can be found in Figure 84 and Table 15. Compared to the experiment with  $I_{Ref} = 10nA$ , the maximum possible conversion frequency has also increased by one magnitude. This supports the idea that there is a linear dependence between the reference current and the maximum possible conversion frequency. However, that is not the only parameter which has changed by approximately one magnitude: The Delay time of bit one has changed from 680 $\mu$ s to 60.8 $\mu$ s. This corresponds to a division by ten.

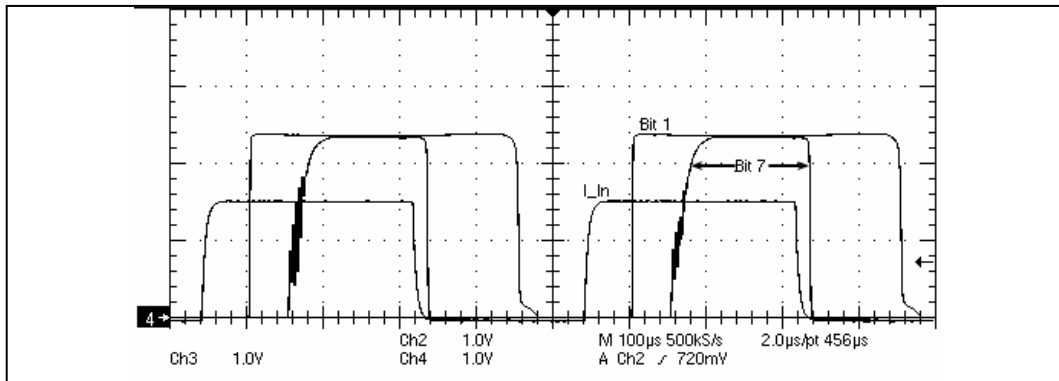


Figure 84: Test results showing bit 1 and bit 7 for  $I_{Ref} = 100nA$  at  $f = 2kHz$ .

Figure 84 shows that the shape of the positive edge of bit seven has become a lot steeper than seen in the  $I_{Ref} = 10nA$  experiment.

Table 15: Measurements at maximum frequency for  $I_{Ref} = 100nA$ .

Delay Bit 1	60.8 $\mu$ s
Delay Bit 7	134.8 $\mu$ s
High time Bit 1	337.6 $\mu$ s
High time Bit 7	153.6 $\mu$ s
Frequency	2 kHz (Interval = 500 $\mu$ s, Duration = 275 $\mu$ s)

### 5.6.4.3

#### $I_{Ref} = 250nA$

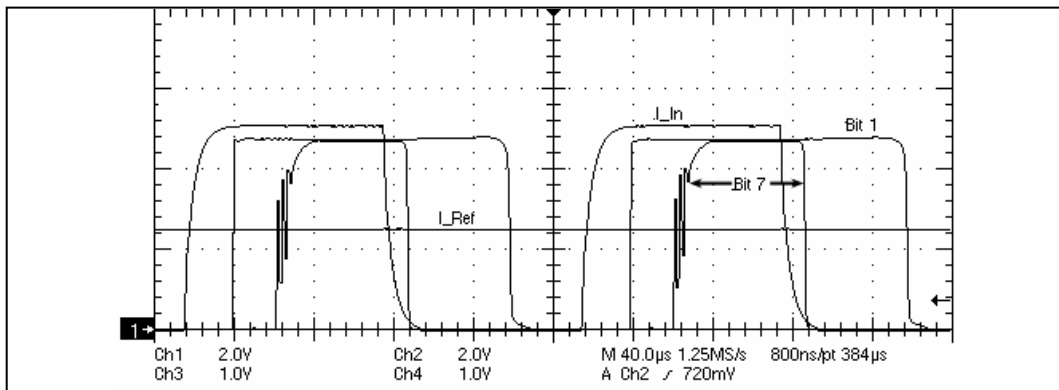


Figure 85: Test results showing bit 1 and bit 7 for  $I_{Ref} = 250nA$  at  $f = 5kHz$ .

Here, the input current ranges from 0 – 500nA. This makes a conversion rate of 5kHz possible, as shown in Table 16. Nevertheless, the switching behavior is not significantly affected by this. Bit seven has an even steeper rising edge than the one in the experiment with  $I_{Ref} = 100\text{nA}$ .

**Table 16:** Measurements at maximum frequency for  $I_{Ref} = 250\text{nA}$ .

Delay Bit 1	19.4 $\mu\text{s}$
Delay Bit 7	57.8 $\mu\text{s}$
High time Bit 1	128.1 $\mu\text{s}$
High time Bit 7	44.2 $\mu\text{s}$
Frequency	5 kHz (Interval = 200 $\mu\text{s}$ , Duration = 100 $\mu\text{s}$ )

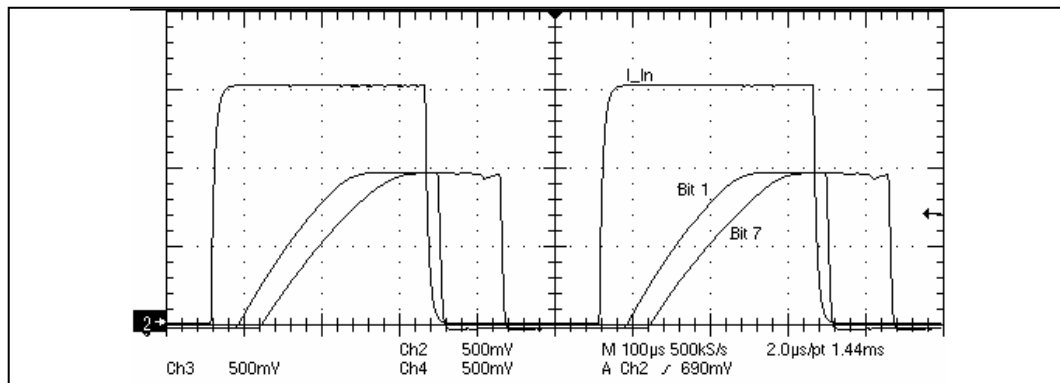
### 5.6.5

#### Dynamic Tests with $V_{DD}$ Variation

In this second series of dynamic tests,  $V_{DD}$  is varied instead of  $I_{Ref}$ . The goal of these experiments is to find out how the maximum possible conversion speed together with the other parameters which are measured changes when the power supply voltage of the transistors is reduced. The reference current used in the next three experiments is thus constant, its value is  $I_{Ref} = 150\text{nA}$ .

##### 5.6.5.1

$V_{DD} = 1\text{V}$



**Figure 86:** Test results showing bit 1 and bit 7 for  $V_{DD} = 1\text{V}$  at  $f = 2\text{kHz}$  and  $I_{Ref} = 100\text{nA}$ .

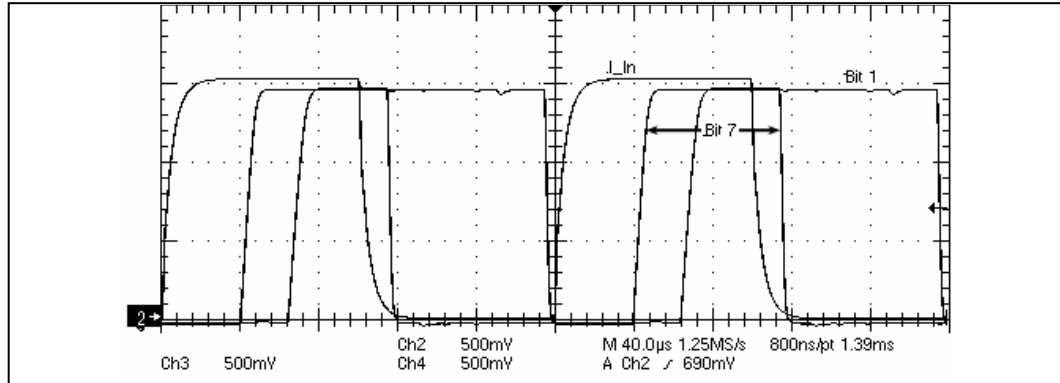
The extremely low voltage test performed here shows interesting results. Although the supply voltage is only one fifth of the voltage used in the experiment from section 5.6.4.2, it leads to the same maximum conversion speed of 2000Hz.

**Table 17:** Measurements at maximum frequency for  $V_{DD} = 1\text{V}$ .

Delay Bit 1	128.0 $\mu\text{s}$
Delay Bit 7	198.0 $\mu\text{s}$
High time Bit 1	226.0 $\mu\text{s}$
High time Bit 7	104.8 $\mu\text{s}$
Frequency	2 kHz (Interval = 500 $\mu\text{s}$ , Duration = 275 $\mu\text{s}$ )

### 5.6.5.2

$V_{DD} = 1.5V$



**Figure 87:** Test results showing bit 1 and bit 7 for  $V_{DD} = 1.5V$  at  $f = 5kHz$  and  $I_{Ref} = 100nA$ .

Although  $V_{DD}$  was only raised from 1V to 1.5V in this experiment, the maximum possible conversion frequency more than doubled to 5000Hz. By comparing the two graphs from Figure 86 and Figure 87, it is noticed that the response signal of bit one and bit seven has significantly changed in shape. While it still was a fairly flat positive edge in the 1V experiment, they both changed their shape to nearly perfectly square shaped signals, or square waves.

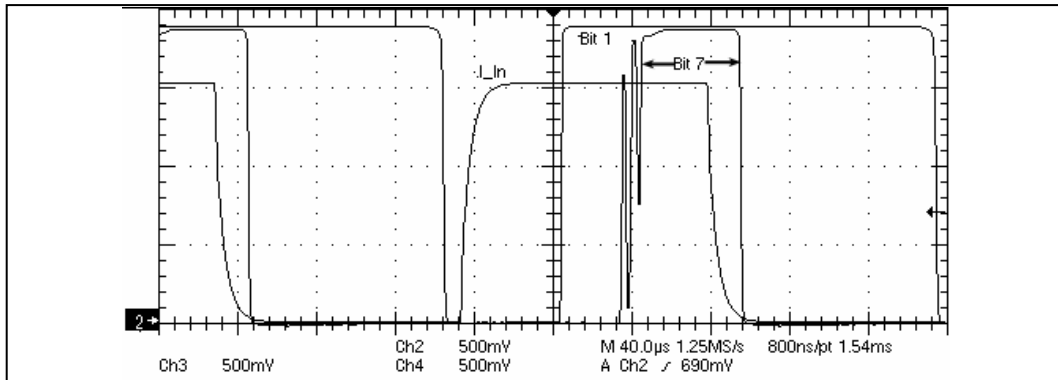
**Table 18:** Measurements at maximum frequency for  $V_{DD} = 1.5V$ .

Delay Bit 1	39.2 $\mu s$
Delay Bit 7	65.2 $\mu s$
High time Bit 1	146.8 $\mu s$
High time Bit 7	41.6 $\mu s$
Frequency	5 kHz (Interval = 200 $\mu s$ , Duration = 100 $\mu s$ )

### 5.6.5.3

$V_{DD} = 3.0V$

In this last experiment, the converter's behavior will be recorded and analyzed for a power supply voltage of 3V. Table 19 reveals that the maximum possible conversion frequency decreased by 1kHz since the last experiment which was carried out. This consequently means that lower supply voltages can lead to a higher conversion rate. This is also confirmed by the similar experiment in section 5.6.4.2. It has exactly the same parameters, just the supply voltage  $V_{DD}$  is 5V instead of 3V. Unsurprisingly, the maximum possible conversion rate comes down to only 2kHz.



**Figure 88:** Test results showing bit 1 and bit 7 for  $V_{DD} = 3V$  at  $f = 4kHz$  and  $I_{Ref} = 100nA$ .

In Figure 88, bit seven is oscillating a couple of times up and down before stabilizing on the *high* signal level. One drawback of this converter might be that the bit high-time of bit one and bit seven are quite different. While bit seven only is up for roughly  $50\mu s$ , bit one remains up nearly four times as long.

**Table 19:** Measurements at maximum frequency for  $V_{DD} = 3V$ .

Delay Bit 1	42.2 $\mu s$
Delay Bit 7	84.8 $\mu s$
High time Bit 1	187.2 $\mu s$
High time Bit 7	48.6 $\mu s$
Frequency	4 kHz (Interval = 250 $\mu s$ , Duration = 125 $\mu s$ )

## 5.7

### Dynamic Performance Analysis

The dynamic performance analysis compares the results of the previous test series with each other. Each of the measured parameters is visually illustrated, making it easy to identify trends for certain assumptions.

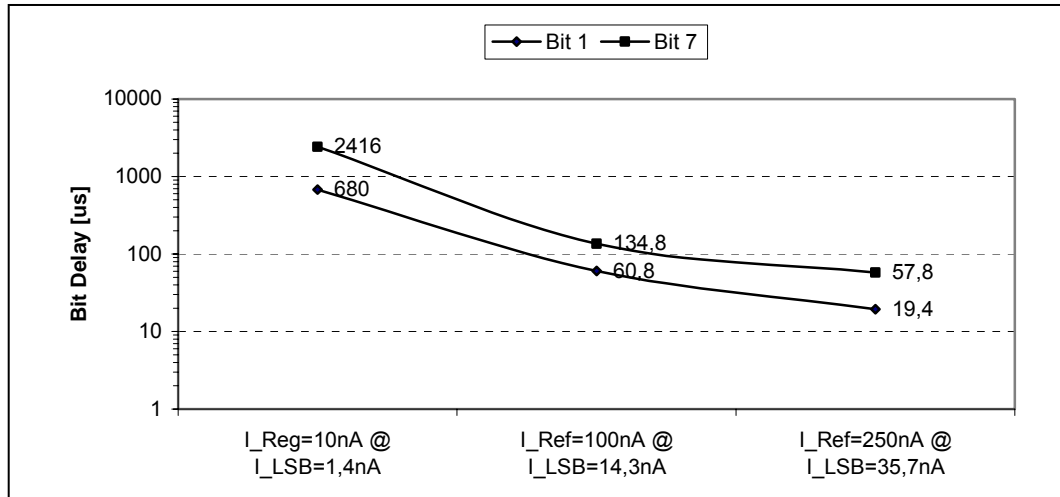


Figure 89: Delay comparison for different reference currents.

The bit delay comparison for the experiments in which the reference currents shown in Figure 89 were used is only sensible when the data is plotted on a logarithmic scale. As a general rule, this can be summarized as: “The higher the reference current, the quicker the converter becomes.”

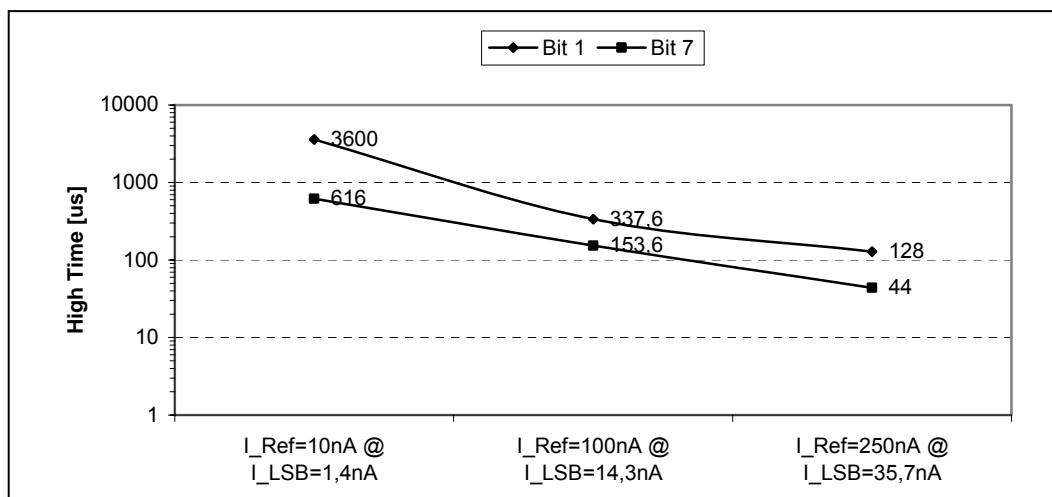
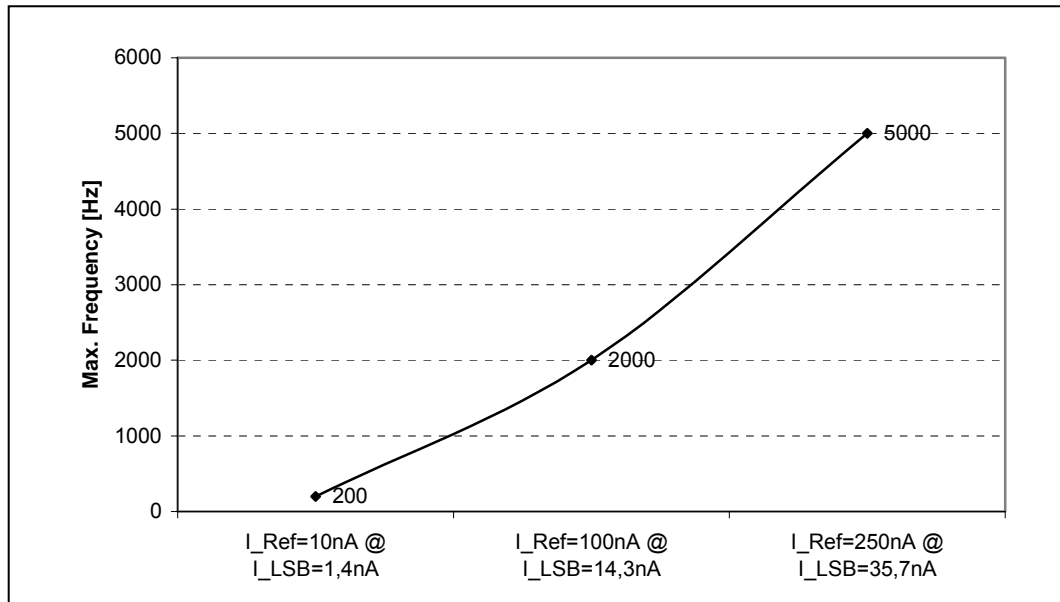


Figure 90: Comparison of bit high times for different input currents.

Comparing the bit high-times of bit one and bit seven for different reference currents in Figure 90 shows us that a low reference current automatically leads to long bit high-times. Notice that the Y-axis, on which the bit high-time is measured, has a logarithmic scale in this graph.



**Figure 91:** Maximum possible conversion frequency for different current input levels.

The frequency comparison from Figure 91 shows a very close and clear linear correlation between the used reference current and the maximum possible conversion frequency. In this figure, which has a normal (linear) scaled Y-axis, the frequency increase is of particular interest.

## 5.8

### Conclusions

The second novel A/D converter approach, which is based on current division, was introduced in theory as well as in practice. The same series of experiments were performed as for the multiplying A/D converter. Likewise, the analysis and performance results can be compared between each other.

While SPICE simulations ratified the principle of the schematic, including expected DC and dynamic properties, real live tests with the chip principally supported this assumption. The converter successfully showed that it is capable to distinguish between currents in the order of one nano ampere. The dynamic aspects are also promising: Within the used parameter value range, a conversion rate of up to 5kHz was achieved.

As seen in the previously tested circuit, this circuit also adduced good results for power supply voltages smaller than 1.5V. The division accuracy experiments showed that more accuracy is obtained for smaller reference currents.



## 6 Seven-to-Three-Encoder

### 6.1

#### Principle of Operation

Digital Encoders are used to encode a number of bits into a smaller number of bits. In the case of the *Artificial Synapse*, an encoder is required which is capable of encoding the seven bits of thermometer code into three bits of dual logic or binary code. Consequently, the encoder will have seven inputs and three outputs. Due to the fact that the outputs of the comparators used in the two proposed A/D converters provide signals in the form of digital voltages, it is evident that a CMOS digital circuit would be the most effective technology. Below is a truth table showing the input and output variables of the system.

**Table 20:** Truth table for the 7-to-3 encoder. Bits 1 – 7 are the input variables, D0 – D2 are the output variables.

Decimal	Thermometer Code							Digital Output		
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0	1
2	0	0	0	0	0	1	1	0	1	0
3	0	0	0	0	1	1	1	0	1	1
4	0	0	0	1	1	1	1	1	0	0
5	0	0	1	1	1	1	1	1	0	1
6	0	1	1	1	1	1	1	1	1	0
7	1	1	1	1	1	1	1	1	1	1

This can be transformed into a logic equation in the form of:

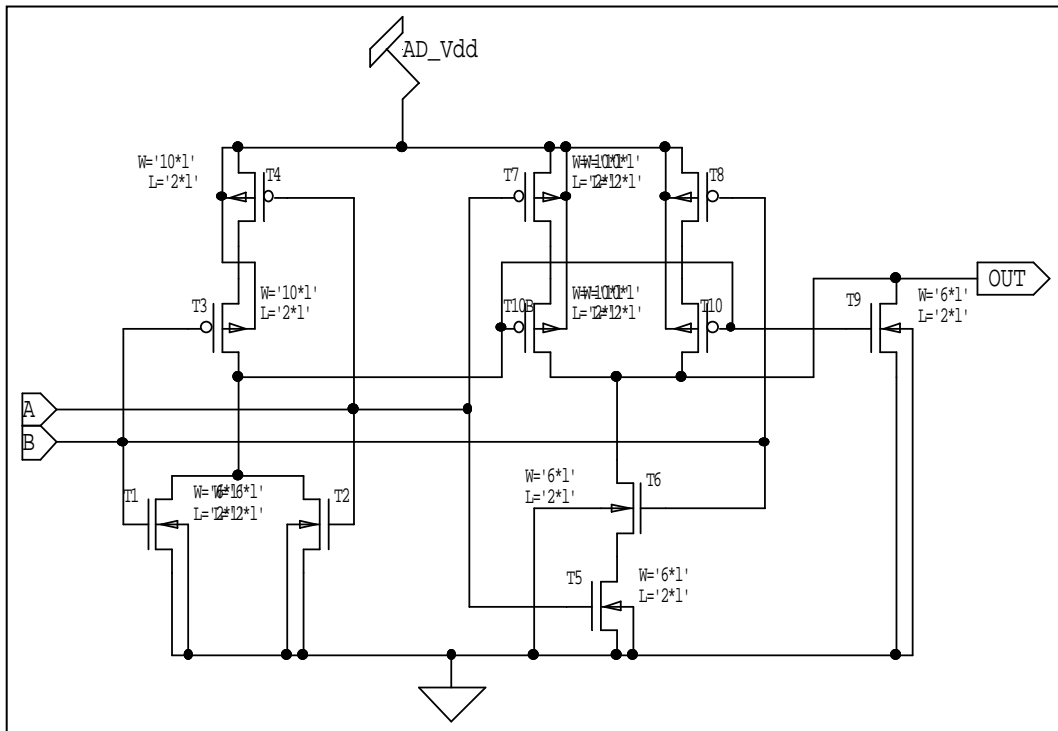
$$D_0 = (\text{Bit1} \wedge \overline{\text{Bit2}} \wedge \overline{\text{Bit3}} \wedge \overline{\text{Bit4}} \wedge \overline{\text{Bit5}} \wedge \overline{\text{Bit6}} \wedge \overline{\text{Bit7}}) \vee (\text{Bit1} \wedge \text{Bit2} \wedge \overline{\text{Bit3}} \wedge \overline{\text{Bit4}} \wedge \overline{\text{Bit5}} \wedge \overline{\text{Bit6}} \wedge \overline{\text{Bit7}}) \vee (\text{Bit1} \wedge \text{Bit2} \wedge \overline{\text{Bit3}} \wedge \text{Bit4} \wedge \overline{\text{Bit5}} \wedge \overline{\text{Bit6}} \wedge \overline{\text{Bit7}}) \vee (\text{Bit1} \wedge \text{Bit2} \wedge \text{Bit3} \wedge \overline{\text{Bit4}} \wedge \overline{\text{Bit5}} \wedge \overline{\text{Bit6}} \wedge \overline{\text{Bit7}})$$

**Equation 28:** Logic equation for the output D0 of the 7-to-3 encoder.

The logic equation for output  $D_0$  from Equation 28 can be set up for  $D_1$  and  $D_2$ . These three equations can be combined into one logic equation which describes all possible states of the encoder. In the next step the equation is minimized using the *Karnaugh Veitch* (KV) algorithm. This leads to an efficient logic circuit with no unessential gates. Of course, in most cases there are several implementations possible. One possible solution for the task given requires six *exclusive or* (XOR) gates to realize the logic function. Each XOR gate consists of eleven transistors. With a total of 66 transistors, the circuit is acceptable in size and complexity.

## 6.2 Schematics

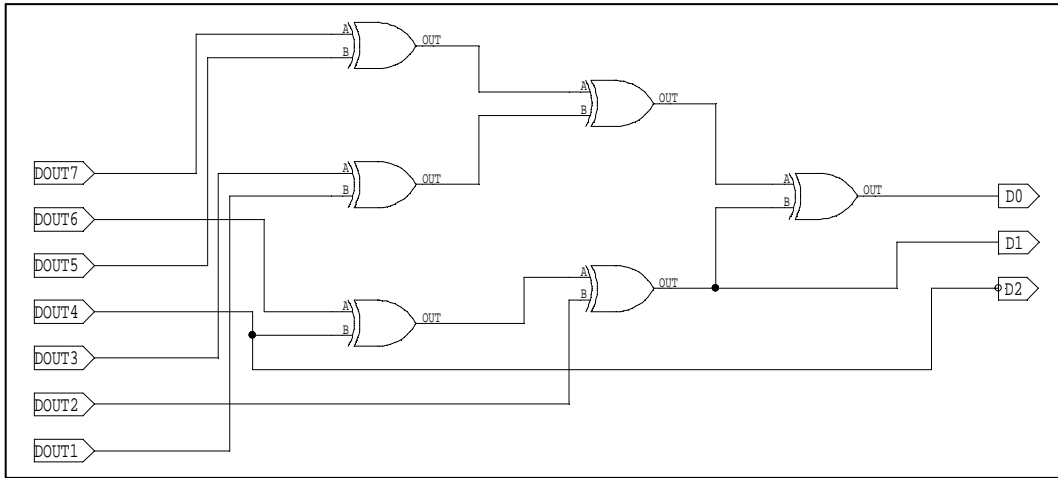
Figure 92 shows the schematic of the XOR cell which was used for the implementation of the encoder. Since a XOR cell is a standard CMOS logic gate, Tanner provides a ready designed and laid out XOR cell as part of a cell library which can be used in research projects. This cell was used in the belief that this already tested XOR cell layout should definitely work well in the encoder. Theoretically a XOR cell can be composed of only six transistors: three  $n$ -MOS and three  $p$ -MOS transistors.



**Figure 92:** Schematic of the XOR cell used in the 7-to-3 encoder shown in Figure 93.

The output “OUT” of the XOR cell will show logic “1” if one of the two inputs “A” and “B” is showing logic “1”, regardless of the other input. Therefore, gates performing this function are commonly called *exclusive or* or simply XOR gates.

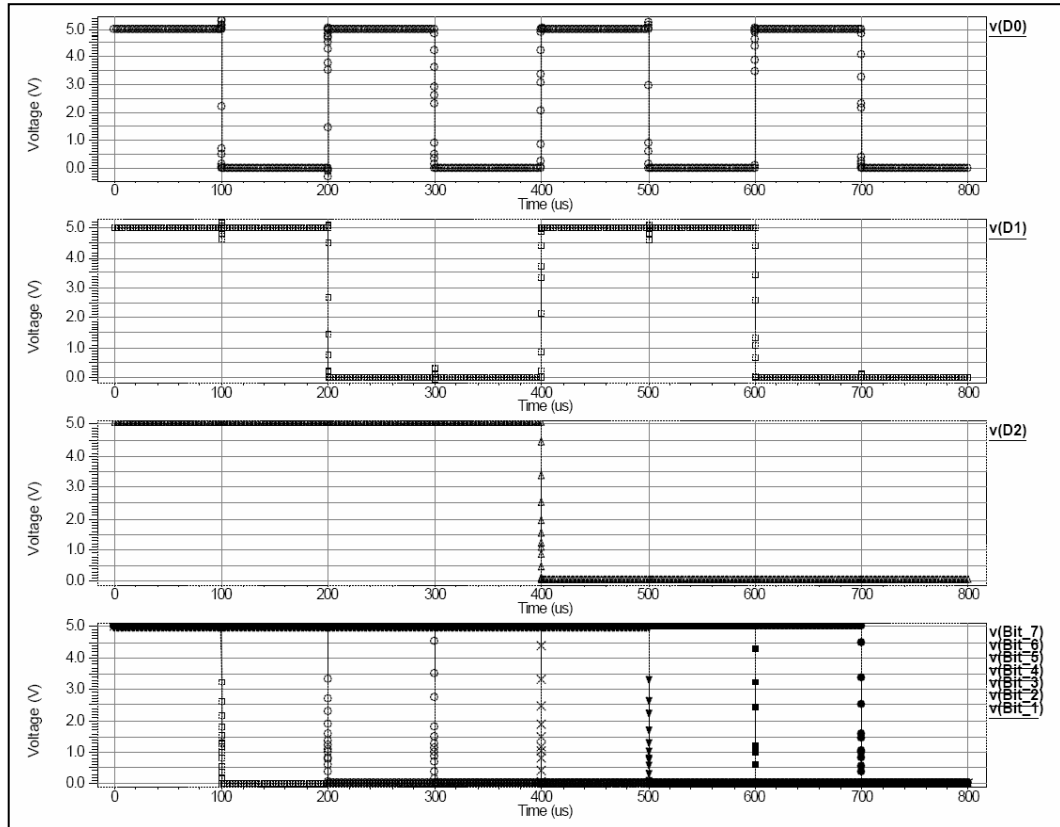
As previously mentioned, the entire 7-to-3 encoder consists of six XOR cells. Figure 93 shows the schematic of the encoder. On the left hand side, you can see the seven input ports labeled “DOUT1” to “DOUT7”. The right hand side of the schematic shows the three outputs “D0”, “D1” and “D2”.



**Figure 93:** Schematic of the 7-to-3 encoder, based on voltage operation and digital signal levels.

This simple circuit does not use clocks or reference voltages and in addition it does not require oversized transistors to be resistant against device mismatches or noise. Hence, it is very well suited as an additional process step of the converters' thermometer output.

### 6.3 SPICE Simulation



**Figure 94:** SPICE simulation of the 7-to-3 encoder. This figure shows the response output signals for the stimulation of inputs 1 – 7 with all signals on *high* at the beginning. Then the bits switch to *low* in progressive stages every 100 $\mu$ s.

The simulation shown in Figure 94 was performed using *T-SPICE Pro* v9.02 and *W-Edit* v9.02 in conjunction with a BSIM3 transistor model for the 1.5 $\mu$ m AMI target process. In this 800 $\mu$ s long simulation, the seven input bits of the encoder are deactivated one after another, with a time delay of 100 $\mu$ s per bit. Thus, you can see the encoder switching through all its eight states. The top chart shows output “D0”, the second chart shows “D1” and the third is “D2”. The chart on the bottom panel shows the stimulation of inputs 1 – 7 together. As predicted in Table 20, the output of the encoder displays the correct value.

### 6.4 Layout

In the layout step of the design process, the Tanner reference XOR cell design was exclusively used. The encoder layout development on the PC was done with *L-Edit* v10.12. For the wiring of the cells, horizontal and vertical layers of *metal1* and *metal2* were used. Figure 95 shows the layout of the whole encoder. In landscape orientation, the six XOR cells are located in the upper half. They are aligned along a  $V_{DD}$  and a ground line. The

seven input lines are positioned at the bottom left hand side. The three output lines are positioned on the bottom right hand side. The whole circuit measures  $300\mu\text{m} \times 85\mu\text{m}$ .

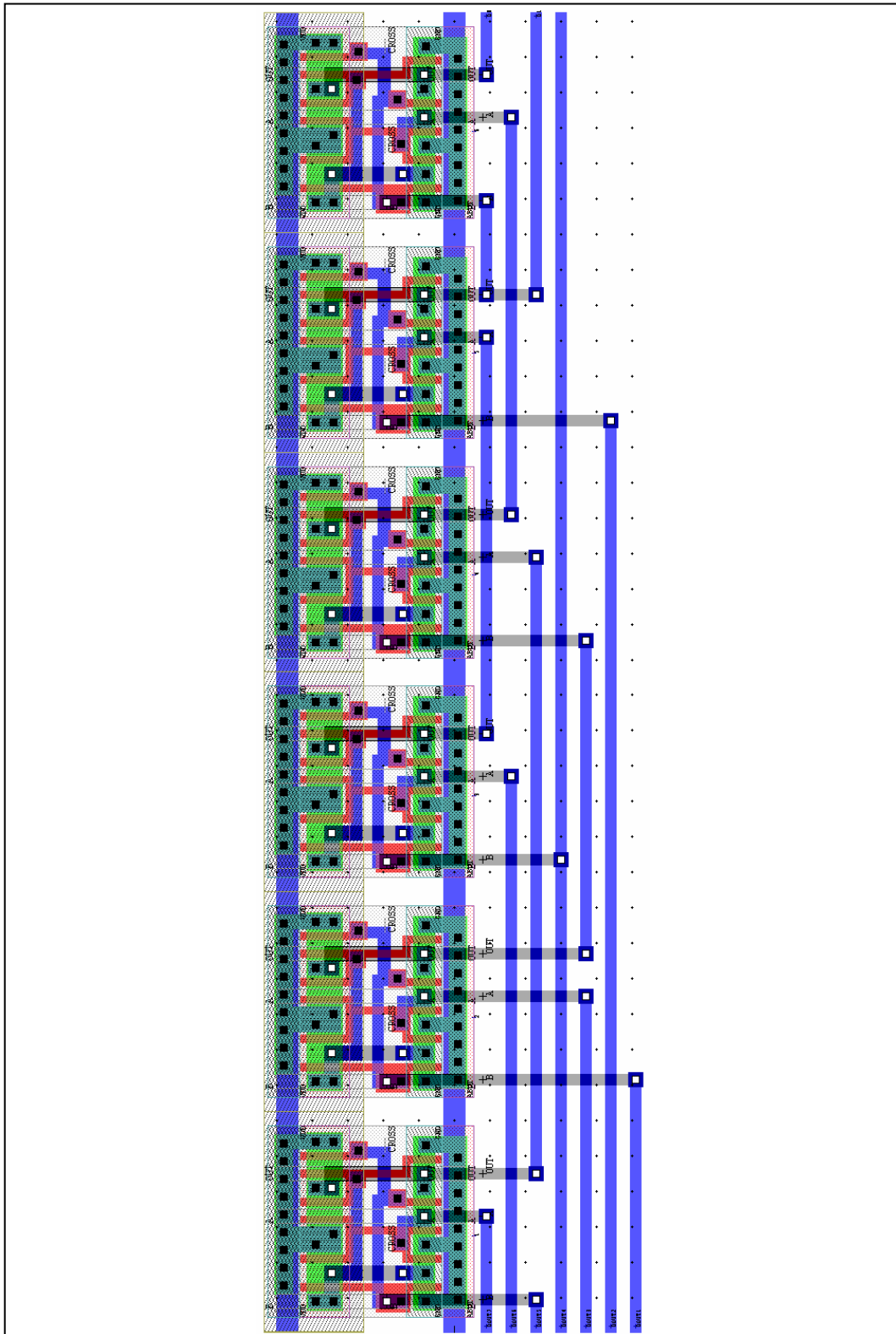
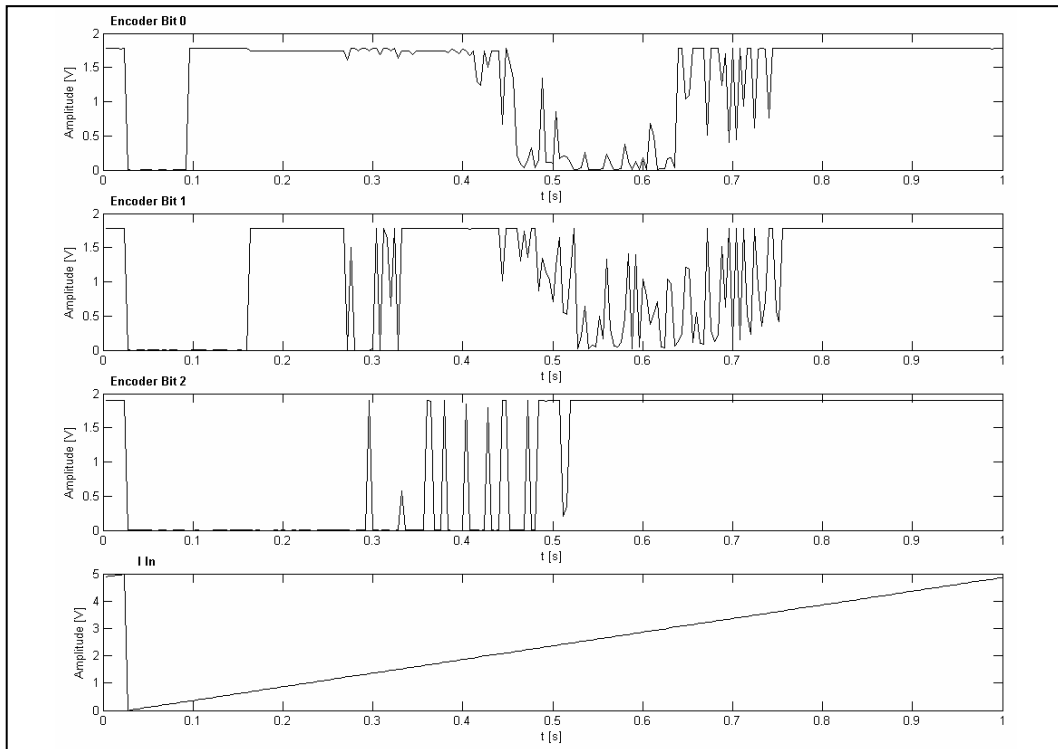


Figure 95: Layout of the 7-to-3 encoder.

## 6.5 Experimental Results

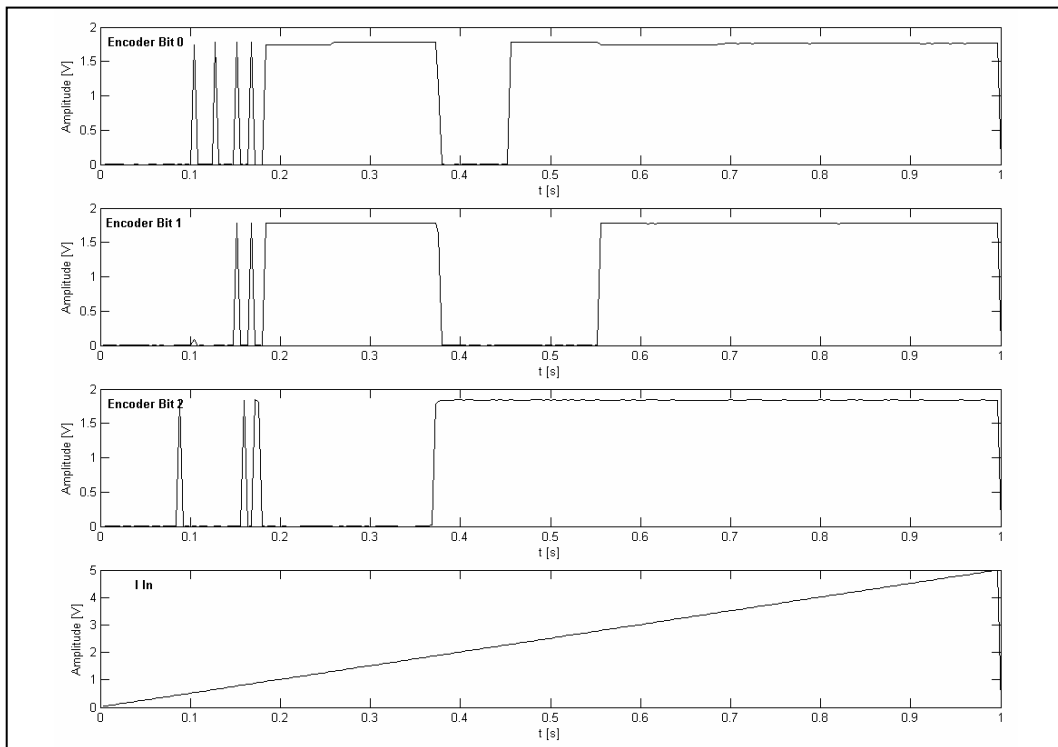


**Figure 96:** 7-to-3 Encoder cycling through all its input combinations which are provided by the output bits of the multiplying A/D converter.

To test the functionality of the encoder, a seven bit thermometer code is needed. In the experiment shown in Figure 96, the seven output bits of the multiplying A/D converter were used. They were connected to the encoder inputs through switches and wires on the printed circuit board. By applying a current which increases from zero to full scale input of the converter, the seven output bits cycle through all possible thermometer code states. The graph on the bottom panel of Figure 96 shows the input voltage which was fed into the current generation circuit for the converter. Thus, the encoder should pass all its transitions exactly once, just like seen in the SPICE simulation graph in Figure 94. The experiment lasted one second.

Unfortunately, the functionality is very restricted. When looking at the top graph of the figure, it should be possible to see the output signal of the LSB output code of the encoder, namely “DOUT0”. It should be switching between *low* and *high* at a continuous interval and duration. However, it goes to *high* for about 400 $\mu$ s, switches back to *low* for about 200 $\mu$ s, and returns to *high* where it remains for the rest of the cycle. The second bit, “DOUT1”, also shows an unwanted switching behavior. Nevertheless, the third bit does perform better. It is supposed to be in the *low* state for the first half of the experiment and in the *high* state for the second half of the experiment. Apart from some oscillations at the transition between *low* and *high*, “DOUT2” works as specified in the design.

In a second experiment, the input stimulation of the encoder was done by the output bits of the dividing A/D converter. Similarly to the previous experiment shown in Figure 96, an increasing current was provided to the converter input. It covers the full scale input, ensuring that all seven output bits of the converter would be at least activated once in each cycle (the saw tooth voltage used to generate the current had a frequency of 1Hz).



**Figure 97:** 7-to-3 encoder cycling through all its input combinations which are provided by the output bits of the dividing A/D converter. The figure on the bottom panel shows the input voltage which is fed into the current generation circuit for the converter. This translates to an input current between 0 and 500nA.

Figure 97 shows that the encoder has a number of problems in its functionality. As seen before in Figure 96, the encoder output bits “DOUT0” and “DOUT1” have a faulty switching behavior and only the signal of “DOUT2” works correctly. However, even this bit has problems, since it oscillates even when it is supposed to remain on *low*. In both experiments, several data series were recorded while the power supply voltage was varied between one and five volts. None of these variations improved the results more than those shown in Figure 96 and Figure 97.

It would appear that something went wrong with the encoder design or layout. Even though SPICE simulations showed correct results for the design and the layout which was used, the circuit does not work as expected in practice. It is currently unclear as to why this malfunction occurs. However, the 7-to-3 encoder should have optimized the result of the current-mode A/D converter but is not mandatory for its operation. If an encoder will be needed it also can be created by using regular discrete logic gates or FPGA chip technology.

## 6.6

### Conclusions

With regard to the theoretical considerations concerning the principle of operation, all aspects of the encoder development process were shown. Design, layout and experiments with the circuit were explained and analyzed.

Although simulation results for this circuit were promising, the performance in actual experiments needs to be improved. The cause for this is not completely understood. Nevertheless, the technique the circuit is based on uses normal CMOS logic gates. Thus, automated software tools for logic synthesis can construct these more easily than the manual layout techniques.



## 7 LVS and Die Layout

### 7.1

#### Layout versus Schematic

Before the chip layout can be sent to the manufacturer, it has to be compared with the schematics. To do this job, the program *LVS* (Layout Vs. Schematic) in version 10.12 has been used. It is part of the Tanner development kit and allows comparing schematic and a layout files which were created with *S-Edit* or *L-Edit*. When the files are being compared, they are not only checked if they are identical in matters of the circuit itself, but also the transistor dimensions are checked. It is therefore possible to exclude errors in the layout and make sure that there are no shorted signal lines or grounded power rails. When LVS outputs the success message circuits are equal at the end of the merging, eliminating and morphing process, it does not necessarily mean that the circuits are automatically working in practice as the SPICE simulations predict. Although the average chip production parameters which are provided by the manufacturer are considered by the T-SPICE simulation, there are too many unpredictable parameters in analog chip design which may vary and change the result into the negative direction.

Debugging a complex analog design layout can be a time consuming affair. Even though LVS displays error messages saying where the error occurred when the files were parsed, it can still be very hard to locate the layout error which is responsible for the inequality between the circuit descriptions.

### 7.2

#### Die Layout

Figure 98 shows the entire die layout. The complete chip measures 4.6 x 4.7mm, the area shown in the picture measures 4.6 x 1.9mm. In addition to the four circuits, it is also possible to identify the five bypass capacitors in the middle of the image as well as numerous areas which contain grounded *substrate contacts*. Bypass capacitors help to minimize high frequency noise and are placed in-between ground and  $V_{DD}$ . Substrate contacts are important in analog design to ground unused chip area.

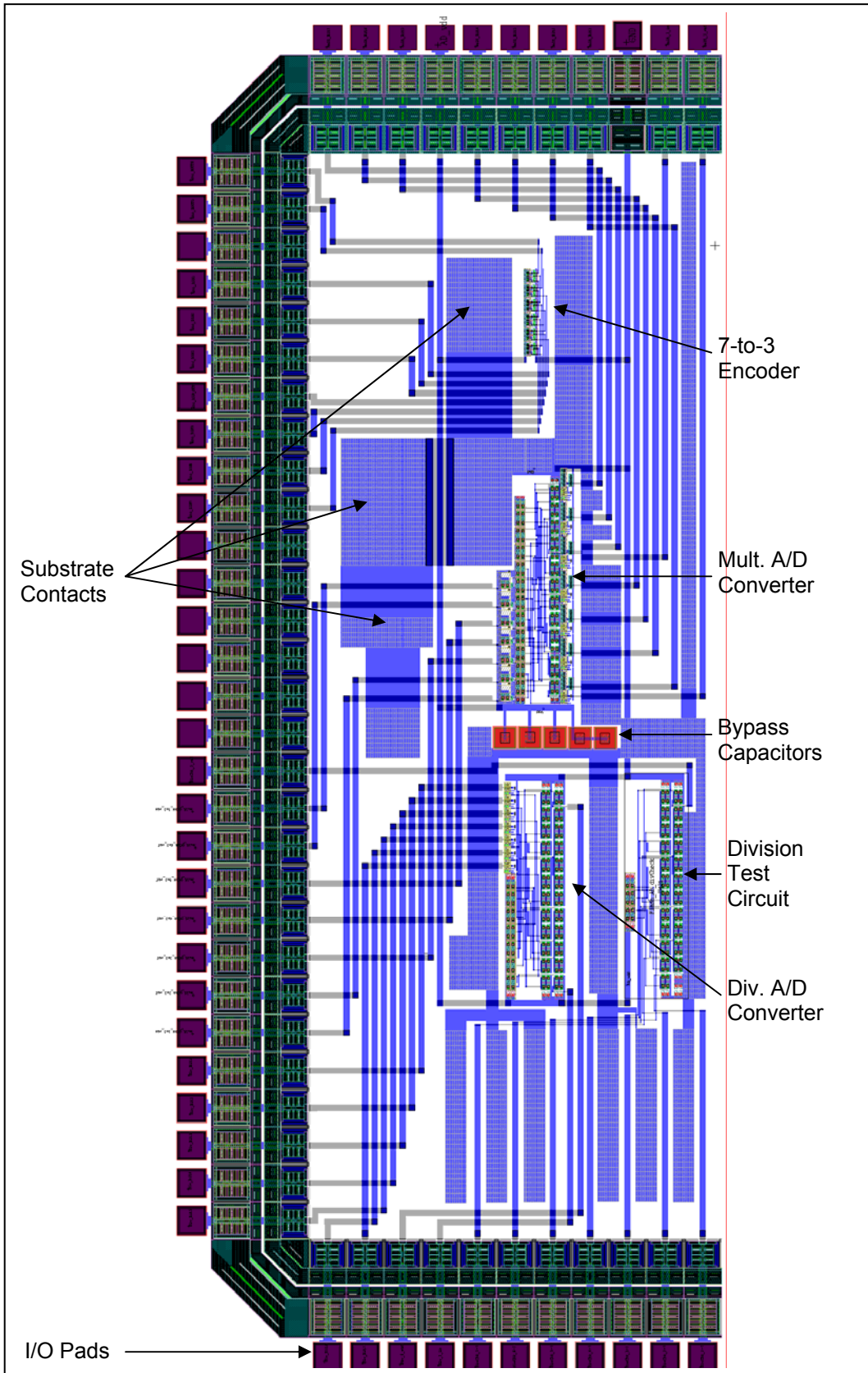


Figure 98: Layout of the whole die including I/O pads, bypass capacitors and substrate contacts.

## 8 Prototype Test-Bed

### 8.1

#### Functionality

The prototype board is essential to operate the chip. It not only provides the supply voltages which are necessary for the transistors on the chip to operate, it also represents the input and output (I/O) interface to the real world. One of the main aspects when designing the printed circuit board (PCB) was to maximize the ease of use when carrying out experiments with the integrated circuits. The following list provides the major things which had to be considered when designing the PCB:

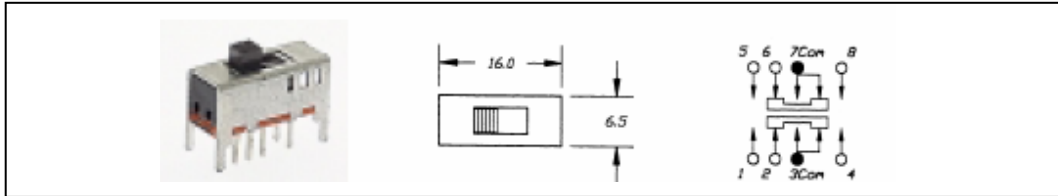
- Generation of the reference and input current, driven by an externally applied voltage in the range between 0 – 5V.
- Current measurement circuits which transform a current in the nano ampere range into a voltage between 0 – 5V. The following 14 currents have to be measured; each of them appears on a different pin of the chip: multiplication factor test bit 1 – 7 and division factor test bit 1 – 7.
- Visual display of the seven output bits of the two A/D converters, appearing on 14 pins.
- Visual display of the three bits of the 7-to-3 encoder, which allocate three pins.
- Interfaces for the different I/O voltages of the board. Oscilloscope probes, DAB probes and the connectors of the power supply and the stimulator need to be connectable.
- The PCB layout should be as packed as possible in view of the fact that the production price follows the dimensions of the PCB.
- The chip comes in a 121 position *pin grid array* (PGA) socket package and will be located on a prototyping adaptor which converts the PGA into a *type A base prototyping panel base terminal*. This adaptor has to be soldered onto the PCB.

Using different kinds of switches on the PCB makes the wiring between the different function blocks of the system “variable”. Components can be shared and testing of the integrated circuits becomes more convenient. Thus, measurements have been taken. To keep the required space and the costs for parts minimal, current measurement and generation circuits are shared between the integrated circuits. Instead of placing 14 separate current measurement circuits onto the board, only two were used. Instead of having current generation circuits for the reference and the input current for each one of the A/D converters plus the third circuit which needs a current, the division test circuit, only two were used. Instead of using 14 LEDs to show the result of the digitalization of the applied currents, seven were shared among the two converters.

## 8.2

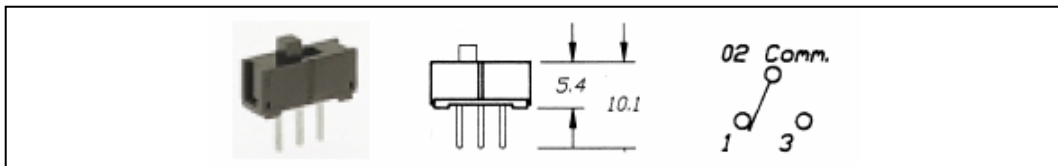
### Part list

The following parts and components are used on the PCB:



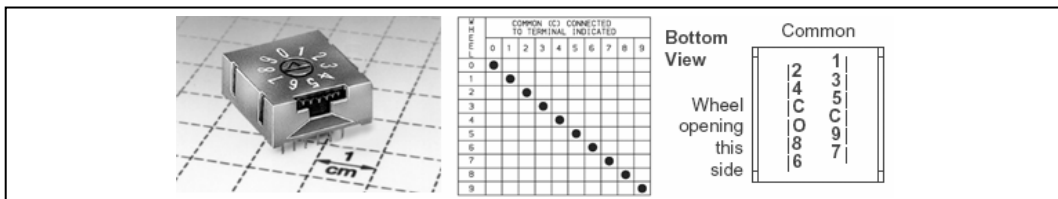
**Figure 99:** EG-2301 three way slide switch.

One EG 2301 three way slide switch is used to connect the reference current either to the multiplying, the dividing or the division test circuit.



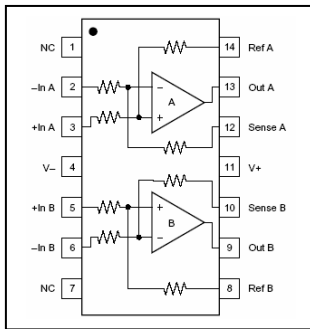
**Figure 100:** EG-1218 two way slide switch.

Two position switches are used in numerous forms. Where exactly they are located can be seen in the schematic of the test board in section 8.4. In total, 21 pieces of this sort of switch is being used on the PCB.



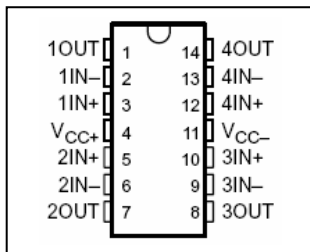
**Figure 101:** C&K 3M series miniature thumbnail switch.

As previously discussed, two so called *thumbnail switches* are used to connect the two current measurement circuits with one current each which can be measured at a time. Thus the thumbnail switches represent seven-to-one multiplexers (MUXs), the switches used are 10:1 multiplexers, but merely seven are used. Figure 101 shows an image, the truth table and the pin layout of the C&K 3M series miniature thumbnail switch.



**Figure 102:** Schematic of the INA 133 precision difference amplifier.

The INA133 is a high speed precision difference amplifier. It has a high slew rate, unity gain difference amplifier which consists of a precision op-amp with a precision resistor network. On the PCB, a dual version, the INA2133 with a SO-14 package and surface mount possibility was used. Detailed information how the current generation and measurement circuit works in which INA133 IC is used can be found in section 8.3.

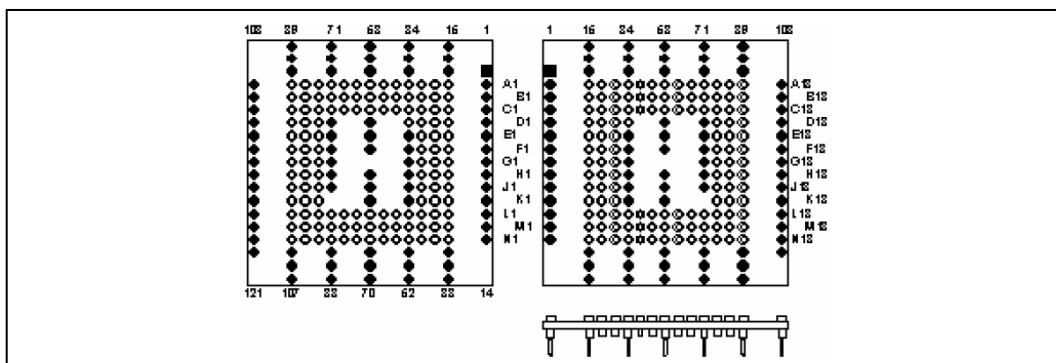


**Figure 103:** Schematic of the TL034 low-power low-offset operational amplifier.

The TL034 is an enhanced *junction field effect transistor* (JFET) low-power low-offset operational amplifier (OP-amp). The version used on the PCB is a quad IC, thus it contains four separated OP-amps together in one package. The on-chip zener trimming of offset voltage yields precision grades as low as 1.5 mV (TL031A) for improved accuracy. It is used in conjunction with the INA133 in the current generation/measurement circuit which is discussed in section 8.3.

The pin map in Figure 104 shows the top, bottom and side view of the PA-PGA121-02 prototyping adaptor. It converts the tight PGA-packing to a less tight packed *type A base prototyping panel base terminal*. Also, it is necessary to use a prototyping adaptor in order to change the chip in case this should become necessary.

Apart from the components shown in the figures above, 10 LEDs were used to visualize the output bits of the two A/D converters and the output of the encoder circuit. Also, four 1% 10MΩ resistors are part of the current generation and measurement circuits.

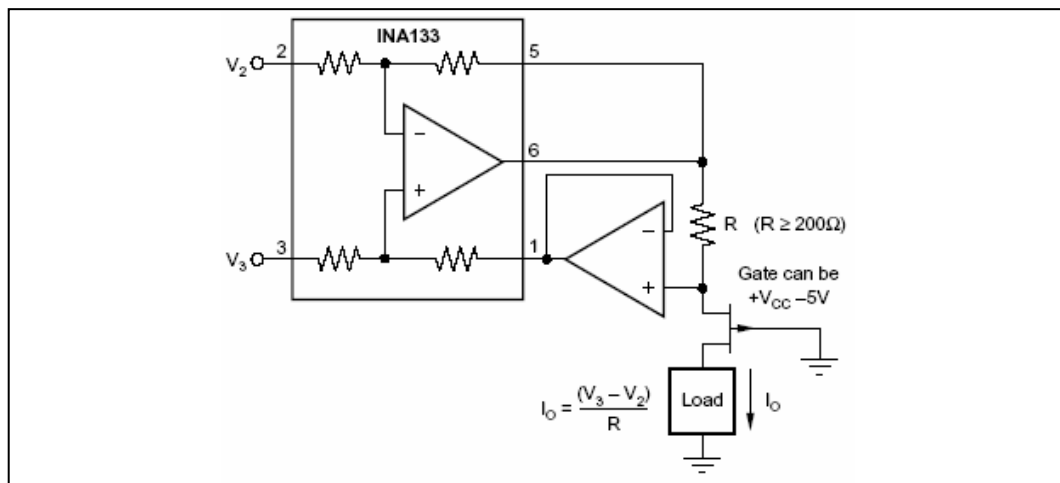


**Figure 104:** Map of the PA-PGA121-02 prototyping adaptor. Left: Bottom view panel base terminal; Right: Top view PGA.

### 8.3

#### Current Measurement and Generation

The combination of an OP-amp and a differential amplifier solves on the PCB as a high-precision current source. Figure 105 shows the schematic with the three components INA133 differential amplifier, TL034 operational amplifier and 10M $\Omega$  resistor R.  $V_2$  is connected to ground;  $V_3$  is driven by an external voltage source to control either the reference or the input current of the converters. The additional transistor in Figure 105 is omitted since it is not essential. "Load" refers to the input of the converter fed from the generated current.



**Figure 105:** Schematic of the current measurement and generation circuit composed of one INA133 IC, one TL034 IC, and one resistor R.

The 10M $\Omega$  resistor causes a voltage to current conversion factor of 1.000.000 resulting in the output current formula:

$$I_{\text{Output}} = U_{\text{Input}} / 1.000.000\Omega$$

**Equation 29:** Voltage to current translation factor of the current generation circuit.

If a current is actually applied to the circuit from Figure 105 instead of being generated driven by a stimulating external voltage source, it turns into a high-precision current measurement circuit. Based on the assumption that we are using a 10M $\Omega$  resistor, the formula to compute the voltage caused by a current applied to the circuit is:

$$U_{\text{Output}} = I_{\text{Input}} * 1.000.000\Omega$$

**Equation 30:** Current to voltage translation factor of the current measurement circuit.

## 8.4

### PCB Schematics

Figure 106 shows the schematic of the PCB circuit how it was planned in the first step. Starting with abstract function blocks, a practical solution for their flexible wiring was sought. Each of the function blocks represents an isolated integrated circuit being implemented on the chip. The I/O ports, which really are pins, are stylized by short lines going into and coming out of the four function blocks. The function blocks are:

- The multiplying A/D converter with two in and fourteen outputs
- The dividing A/D converter with two in and seven outputs
- The test circuit for testing the division accuracy (one in and seven outputs)
- The 7-to-3 encoder with seven in and three outputs.

The schematic neither shows the actual chip with its pins nor the ICs used for current generation and measurement. It also omits the power rails needed to supply the transistors with energy. It rather is an abstract view showing the interconnections between the function blocks including switches and I/O ports of the PCB to communicate with the rest of the world.

After the two input currents  $I_{in}$  and  $I_{Ref}$  are distributed to the A/D converters using one two way and one three way slide switch, a row of seven switches selects which of the seven output bits are connected to the next stage of switches. This second stage of seven parallel switches selects whether the bit signals shall be connected to the LEDs respectively I/O ports or to the encoder inputs. Seven more parallel switches which make up the third stage finally select if the input lines of the 7-to-3 encoder are connected to I/O ports for external stimulation and testing purposes, or if the converter signal drives the encoder. In Figure 106 you can see one more row consisting of seven and one row consisting of three more switches which were not included in the final design of the PCB. The reason for this is that it is not necessary to have switches selecting between the signals being connected to the LEDs respectively its series resistance (not shown in Figure 106) or an I/O port. Since I/O ports are merely pieces of wire soldered onto the PCB, the node will not be affected whether a LED is connected to it or not.

In Figure 107 a second schematic shows all connecting wires, the chip, slide switches, thumbnail switches, LEDs, ICs, resistors and I/O ports. It was created using the software *ExpressSCH 4.1.1* by *ExpressPCB*. This development tool allows designing schematics by using switches, resistors and other electrical circuit components. It also aids the design of custom components, which has been used to model the *Artificial Synapse* chip in the schematic. In addition, it has a feature to assign unique identification (UID) names to each component and each port of each component so that this information can be linked into the PCB modeling part of the software, called *ExpressPCB*. UIDs are a convenient and powerful tool which helps to develop an error free PCB layout more accurately and faster. Section 8.5 focuses on how the layout for the PCB was done using *ExpressPCB*.

Since manufacturing the chip is costly, the die (which has 116 pins in total) was shared with G. Rachmuth, a doctoral student in Professor Poon's laboratory. As you can see in the schematic in Figure 107, 42 pins were used for the project related to this thesis. The remaining pins are left unconnected since they are not required here. The 42 pins also include a separate power supply rail which allows controlling the converters'  $V_{DD}$  voltage independently from the  $V_{DD}$  required to power the current generation/measurement ICs mounted on the PCB.

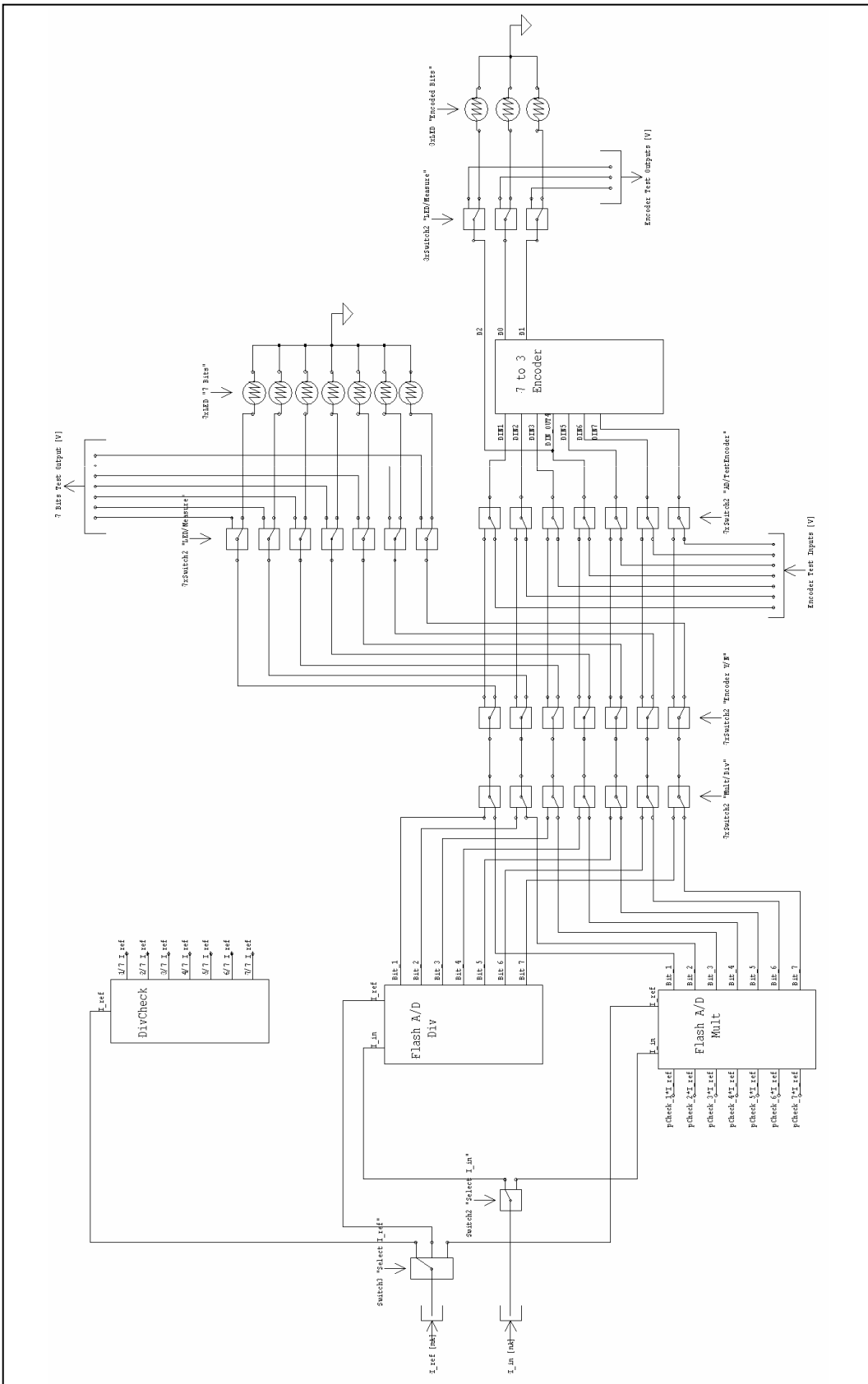
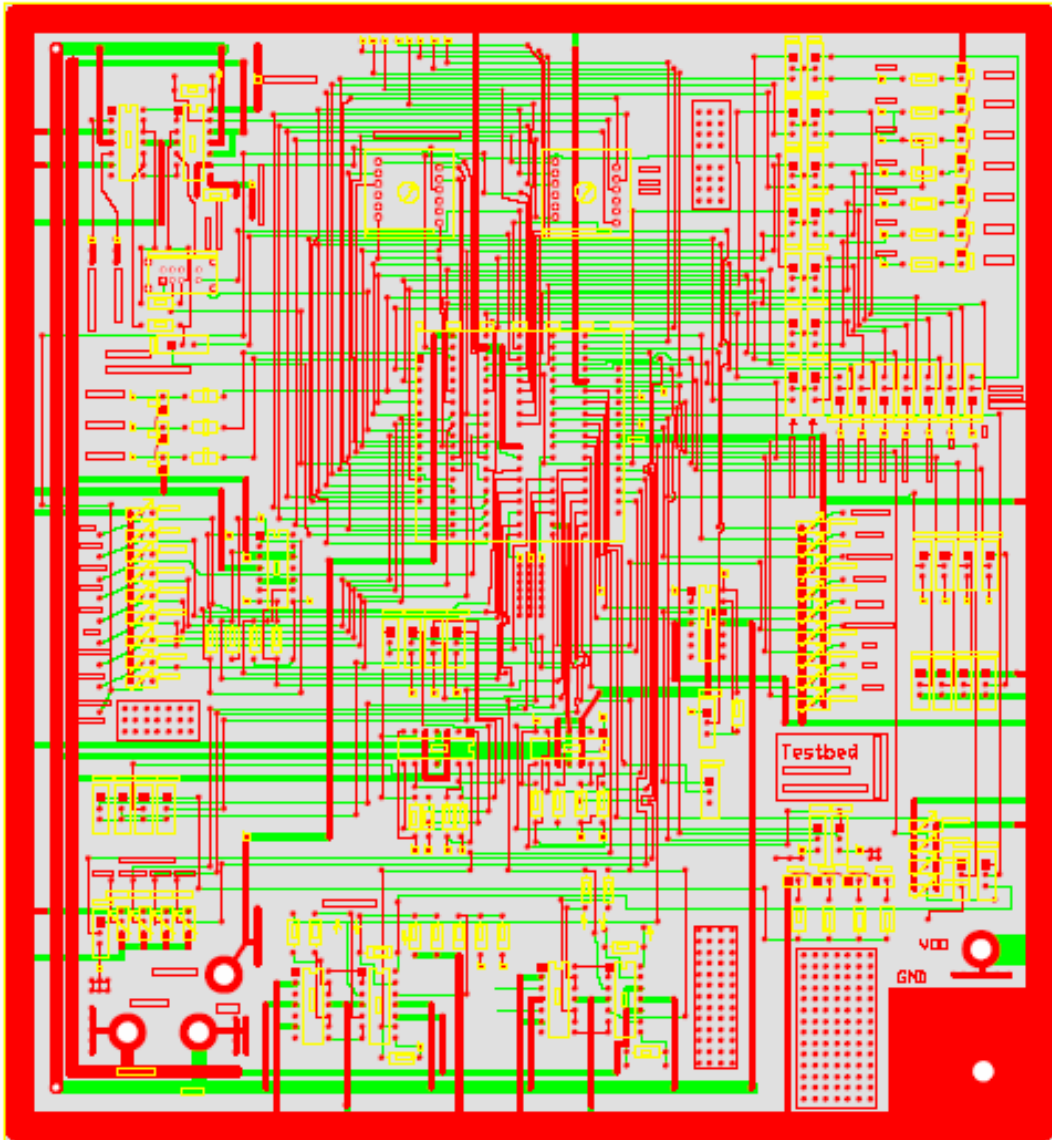


Figure 106: Schematic of the circuit used for the PCB. It shows the wiring of the different functional units which were implemented on the chip.





## 8.5 PCB Layout



**Figure 108:** Layout of the prototype printed circuit board. An overlay of both metal layers is shown in this view.

Although the *ExpressPCB* software supports the PCB designer, the actual layout of the circuit has to be done manually. Thereby the designer has to route the power, ground and signal wires from source node to target node making sure not to short any of the wires. The components on the PCB are represented through pre-designed or custom made symbols. They contain the exact dimensions, positions and hole diameters of the mounting pins of the components. Components have unique identification numbers. When these UIDs match the UIDs assigned to the components in *ExpressSCH*, the software is able to highlight nodes which belong together and thus make the wiring a lot easier. By

changing to the *network mode* in ExpressPCB, it is possible to actually step through all connection networks which form the circuit by clicking on forwards and backwards buttons.

Figure 108 shows the top view of the PCB layout. It is an overlay of the bottom copper layer, the top copper layer and the silkscreen layer (which only adds annotations and names to the digital representation of the circuit, it does not appear on the real board). A ground wire with a width of 0.25" surrounds the PCB on the top side. On the bottom side, the same arrangement makes the  $V_{DD}$  supply available on the whole board. Furthermore, three 0.1" wires spread  $V_{SS}$ ,  $V_{Bias}$  and the alternate power supply  $AD-V_{DD}$  on the PCB. They are the medium thickest wires on the left and lower side of the layout in Figure 108.

After layout and layout verification is complete, *ExpressPCB* offers to directly submit the information to the PCB manufacturer. After a production and shipping time of four days, two exemplars of the PCB were received back in the laboratory. The assembly and soldering took two days. On the third day, the board and its ICs proved to work correctly, and thus far no problem has occurred with the PCB.

## 8.6

### Conclusions

Using a custom PCB design to test the chip has been a convenient and successful method. Instead of using a breadboard solution which is complex to handle and fault-prone, the PCB allows accurate interconnects between the chip the components surrounding it.

For the actual layout of the circuitry it reduced the time to design the circuit with a schematic counterpart of the PCB layout software. Thus, layout errors could be completely avoided. Since the PCB production technique which was chosen only uses two layers of metal, the most complicated part of the layout was to route the wires which actually connect to the prototype adaptor without causing any electrical shorts.

Soldering all the resistors, switches, IC mounts and wires into place requires great care. It is important to produce 100% faultless electrical connections; otherwise it maybe hard to determine where an error originates. In addition, using too much solder or soldering for a too long time can either cause shorts with other solder joints or can damage the component itself.

## 9 Summary and Future Work

The goal of this thesis was to optimize or develop a novel design for an analog current-mode subthreshold analog-to-digital converter. This goal has successfully been achieved. The two new A/D converters outperformed the previous A/D converter in all tests performed. Experimental results of both approaches tested the ability to distinguish between input currents in the order of nano amperes accurately. All initial requirements were met by the two new converters, including key criteria such as input current range between 0 – 100nA, conversion frequencies of up to 5kHz, and power supply voltages of less than 1.5V. Temperature range, space occupation and power dissipation aspects were not defined in detail by the *Artificial Synapse* project.

The analog-to-digital converter based on current division convinced with a very good linearity and high conversion rates. Performance differences between the two current conversion circuits are due to the fact that the design based on current division is much more consistent and uniform than circuit design of the multiplying A/D. The mixture of current multiplication and current addition leads to less accurate partial currents. In addition, the multiplying analog-to-digital converter reuses intermediate results which already contain errors again.

Although analog integrated circuit design based on CMOS technology is awkward and time consuming, it has been possible to design a layout which has been submitted to the MOSIS chip foundry, functioning as required. The *Tanner Research SPICE development kit* has been essential for the development process, especially considering that sub-threshold simulation on SPICE systems is known to be imprecise.

The results included in this thesis will be submitted for publication in an international scientific magazine for analog integrated circuits (e.g. the IEEE magazine *Analog Integrated Circuits and Signal Processing*).

A research assistantship, at MIT, has been offered to the author of this work, giving him the opportunity to write and publish a paper about this work. Furthermore, he plans to conduct another project in the area of analog integrated circuits in Prof. Poon's laboratory.

## 10 Appendix

### 10.1

#### PCB and Chip Images



**Figure 109:** One out of 15 chip exemplars which were received from the MOSIS chip manufacturing service. It is located on an Ironwood-121 prototyping adaptor.

Figure 109 shows the chip which contains the ICs discussed in this thesis. In Figure 110, the whole PCB is shown as it was used for the experiments performed with the chip. On the right hand side, the two thumbnail switches are located. In the bottom right hand corner, an array of 21 switches controls the interconnections which allow variable test setups for the converters. In the same corner, a row of seven LEDs is responsible to visualize the bit outputs of the A/D converters. The top right corner holds the INA133 and the TL034 chips.

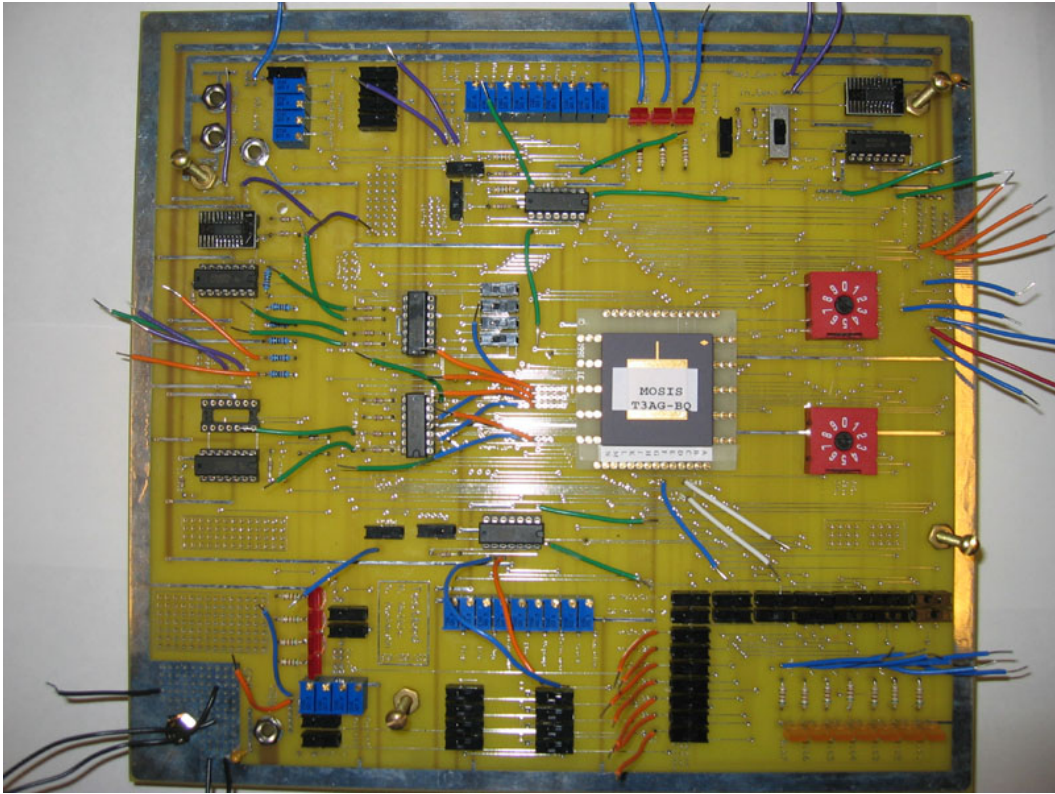


Figure 110: The PCB prototype test-bed loaded with all components.

## 10.2 Test Equipment

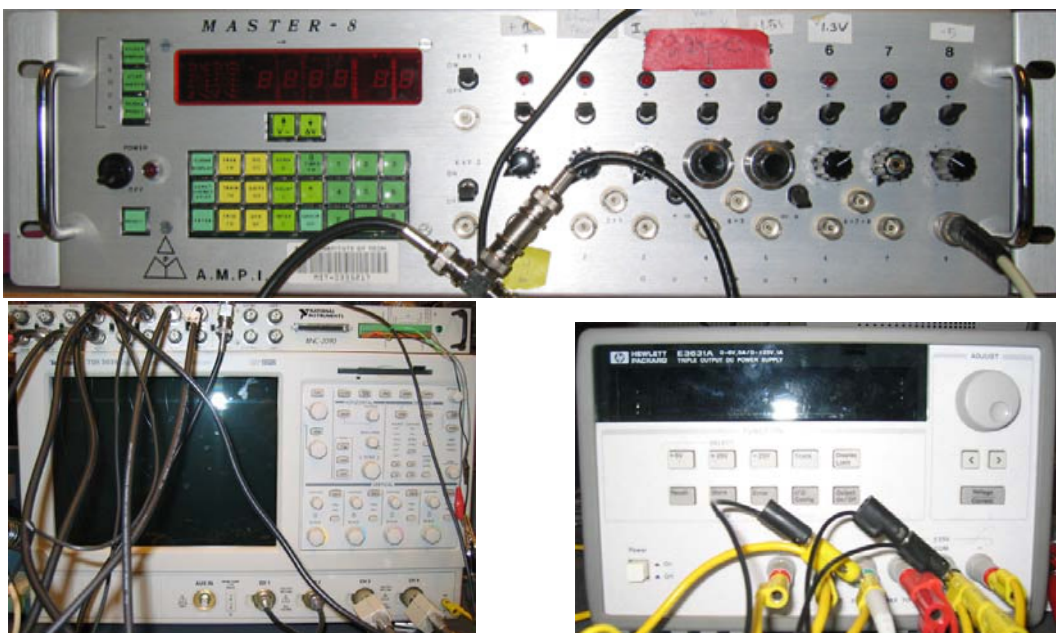


Figure 111: Top: Master-8 Stimulator; Bottom left: Tektronic Digital Phosphor Oscilloscope and National Instruments DAB; Bottom right: HP E3631A Programmable Power Supply.

## 11 Bibliography

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