01 Jan 2023

Averaged Behavior Model of Current-Mode Buck Converters for Transient Power Noise Analysis

Anfeng Huang

Jingdong Sun

Hongseok Kim
Missouri University of Science and Technology, kimhong@mst.edu

Zhenxue Xu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/4802

Recommended Citation

A. Huang and J. Sun and H. Kim and Z. Xu and S. Jin and S. Wu and Z. Yang and K. Qiu and J. Fan and C. Hwang, "Averaged Behavior Model of Current-Mode Buck Converters for Transient Power Noise Analysis," *IEEE Transactions on Electromagnetic Compatibility*, Institute of Electrical and Electronics Engineers, Jan 2023.
The definitive version is available at https://doi.org/10.1109/TEMC.2023.3253546

Averaged Behavior Model of Current-Mode Buck Converters for Transient Power Noise Analysis

Anfeng Huang, *Member, IEEE*, Jingdong Sun, *Member, IEEE*, Hongseok Kim, *Member, IEEE*, Zhenxue Xu, *Senior Member, IEEE*, Shuai Jin, *Member, IEEE*, Songping Wu, *Senior Member, IEEE*, Zhiping Yang, *Fellow, IEEE*, Kelvin Qiu, Jun Fan, *Fellow, IEEE*, and Chulsoon Hwang, *Senior Member, IEEE*

***Abstract*—Accurate evaluation and simulation of power noise is critical in the development of modern electronic devices. However, the widely used target impedance fails to predict the low-frequency noise generated in a device due to the existence of the dc–dc converter, whose output impedance can change under different loading conditions. A physical circuit model is then desired to replicate the behavior of a voltage regulator module, and the average technique is an efficient method to estimate the noise of a pulsewidth-modulated (PWM) converter. With the emergence of converters with adaptive on-time (AOT) controllers, more complex averaging methods are required, but none of them supports transient simulation. A general, efficient, and accurate modeling technique is presented in this article, whose framework supports both current-mode PWM and AOT controllers. In addition, a novel two-step parameter extraction method is proposed, which can be used to evaluate the equivalent values of internal feedback parameters of an encrypted simulation model or from measurement. The modeling method is validated by both simulation and measurement.**

***Index Terms*—Average model, buck converter, power distribution network (PDN), transient power noise.**

I. Introduction

DESIGN and optimization for power distribution networks (PDNs) are critical for the state-of-the-art applications, such as laptops and smartphones. The PDN is designed to maintain a constant supply voltage for the chips and keep it within a narrow tolerance band [1], [2], [3]. The demand for low-voltage operation of a high-speed digital interface is increasing due to the faster logic transition [4], [5]; however, the noise margin is also compromised. Evaluating the fluctuation of the power rail voltage under different loading conditions is increasingly important.

Manuscript received 17 September 2022; revised 13 January 2023; accepted 8 February 2023. This work was supported by the National Science Foundation under Grant IIP-1916535. *(Corresponding author: Chulsoon Hwang.)*

Anfeng Huang, Jingdong Sun, Hongseok Kim, Jun Fan, and Chulsoon Hwang are with the EMC Laboratory, Missouri University of Science and Technology, Rolla, MO 65409 USA (e-mail: huanganfeng@detooltech.com; sunjing@mst.edu; kimhong@mst.edu; jfan@mst.edu; hwangc@mst.edu).

Zhenxue Xu, Shuai Jin, Songping Wu, Zhiping Yang, and Kelvin Qiu are with the Google Inc., Mountain View, CA 94043 USA (e-mail: zhenxue@google.com; shuanjin@google.com; songpingwu@google.com; zhipingyang@google.com; kqiu@google.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TEMC.2023.3253546.

Digital Object Identifier 10.1109/TEMC.2023.3253546

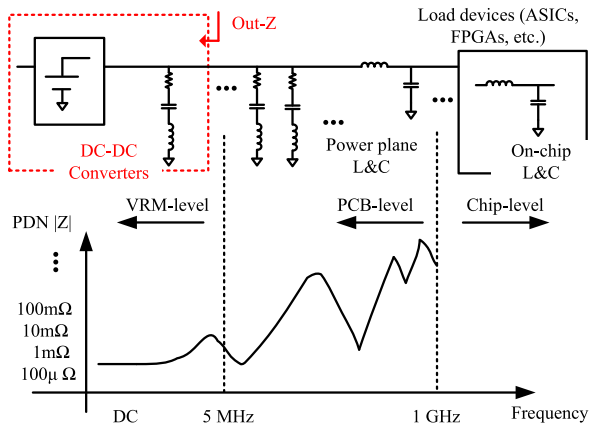


Fig. 1. Impedance curve of a typical end-to-end PDN platform. The PDN impedance is dominated by the dc–dc converter below 5 MHz [6].

The time-domain noise of the PDN is closely coupled with its frequency-domain impedance. To ensure limited voltage fluctuations, the target impedance has been developed as a common criterion for engineers [8]. A typical system-level PDN is consisted of three parts: voltage regulator module (VRM)-level, printed circuit board (PCB)-level, and chip level [9], as demonstrated in Fig. 1. The target impedance method works well for PCB and chip-level PDNs [10]; however, the output impedance can change drastically with different output currents I_{out}, as depicted in Fig. 2(a). The linearized output impedance fails to replicate the transient behaviors of a dc–dc converter. Thus, significant error can be observed if a linearized impedance is used to predict the transient output noise of the buck converter, as shown in Fig. 2(b). To accurately evaluate the transient noise of a converter, the behavior of its feedback controller needs to be modeled [11], [12]. The SPICE models are most widely used, which contains all components in the power converter and parasitic components in the PCB and the chip. Nevertheless, the model of a switching converter is typically provided in the encrypted format and is locked to a certain simulation tool. In addition, tremendous efforts are required to link the PDNs of a PCB and a chip to that of the converter, as S-parameter blocks are the most widely used format to describe the PCB and chip-level PDNs. It is worth noting that many power electronics-oriented SPICE solvers cannot properly handle the cosimulation with S-parameters [13]. The long elapsed time of the simulation is

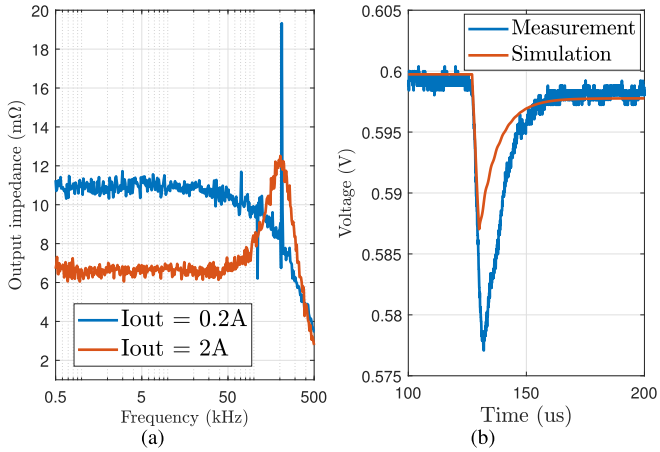


Fig. 2. (a) Measured output impedance of a buck converter under different current sinking levels. (b) Comparison of measured and simulated transient power noise. The linearized simulation model is created based on measured output impedance and the traditional four-element fitting method [7].

another concern when a detailed SPICE model is provided. A simplified yet accurate model is required for efficient evaluation and optimization of an end-to-end PDN.

Average-value technique [14], [15], [16], [17], [18] has been developed as a solution to reveal the complicated physics behind the circuit. In particular, the modeling method is preferred due to its simplicity and has been successfully applied in the modeling of buck converters with constant switching frequency. Even though the ripples in current and voltage waveforms are not explicitly represented, the response due to the feedback controller can be well reproduced by the per-cycle average technique. In addition, the absence of ON/OFF switching provides a better convergence capability and a faster simulation speed. The time-domain behaviors, e.g., dc load regulation and over/undershoot of output voltage, can be accurately predicted [15], [17], [19], [20].

Recently, adaptive on-time (AOT) controllers have been increasingly used due to their feasibility of high-bandwidth design capability and high efficiency [21], [22]. The AOT controller has a smaller switching delay than an ordinary pulsewidth-modulated (PWM) controller and is suitable for CPU applications due to its fast response [23]. We note that the AOT control technique is developed based on the pulse–frequency-modulation method, which has a nonconstant switching frequency. Thus, traditional averaging techniques are hard to directly apply due to the frequency variant nature of the controller. The describing function (DF) is one of the solutions to model the nonconstant frequency operation in the converter, and several small-signal models [16], [24], [25], [26] have been successfully implemented based on this idea. However, to the best of our knowledge, none of the averaged model supports time-domain simulation for the AOT controllers.

With the higher integration level in VRM design, complicated feedback circuits, including current and voltage feedback loops and slope compensation, are integrated into a chip and not disclosed to users due to intellectual property (IP) concerns. The SPICE model of a converter is not always available. Thus, developing a parameter extraction technique that can be used to determine the equivalent parameters of internal feedback loops is also desired.

This article provides an average modeling method for transient simulation of current-mode buck converters. Compared with the existing models, the contributions of this article are highlighted as follows.

1) The utilization of time domain waveforms and cycle-by-cycle averaging technique enable a generalized modeling framework for buck converters with constant and nonconstant switching frequencies.
2) An efficient two-step parameter extraction flow is developed with the help of the proposed modeling technique. An accurate equivalent model can be efficiently implemented based on simulation (from an encrypted model) or measurement results.

This article is an extension of the original conference paper [27] and has more emphasis on the parameter extraction aspects. The rest of this article is organized as follows. Section II gives an overview of the characteristics and operation of current-mode buck converters. The time-domain waveform-based modeling strategy is presented in Section III. Validation in the simulation is demonstrated in Section IV, and a novel two-step parameter extraction method is presented in Section V. The model is then validated by the experimental results in Section VI. Finally, Section VII concludes this article.

II. Buck Converters With Current-Mode Control

Current-mode controllers are currently very popular and widely adopted in buck converters due to its simple structure and fast response. The current feedback loop reduces the feedback delay in the voltage as the inductor current responds immediately to load changes [28]. In addition, the control-to-output transfer function of the current-mode buck converter is with one pole. Therefore, it can be stabilized by a simple type II compensator [16], [22], [28], [29]. In this section, the topologies of current-mode buck converter with the AOT and PWM controllers are introduced and compared.

The schematics of buck converters with the AOT and PWM controllers are shown in Fig. 3(a) and (b), respectively. Each converter consists of a synchronized step-down power stage and a dual-loop controller. The feedback controller is primarily implemented by a comparator, a ramp generator for the elimination of subharmonics oscillation [15], [16], [17], an inductor current sensor, a voltage loop error amplifier, a voltage feedback loop compensator, and an internal voltage reference. Depending on whether the inductor current i_{L} reaches zero during each switching cycle, the converter may operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM).

In the AOT buck converter, the input voltage V_{in} is regulated by a half-bridge inverter consisting of two metal oxide semiconductor field effect transistors (MOSFETs). The output voltage V_{out} is filtered by the inductor L, the equivalent series resistance (ESR) of the inductor r_{L}, and the output capacitor tank C_{out}.

We note that the on-timer is controlled by the output signals of the voltage and current loops, as the current loop feedback

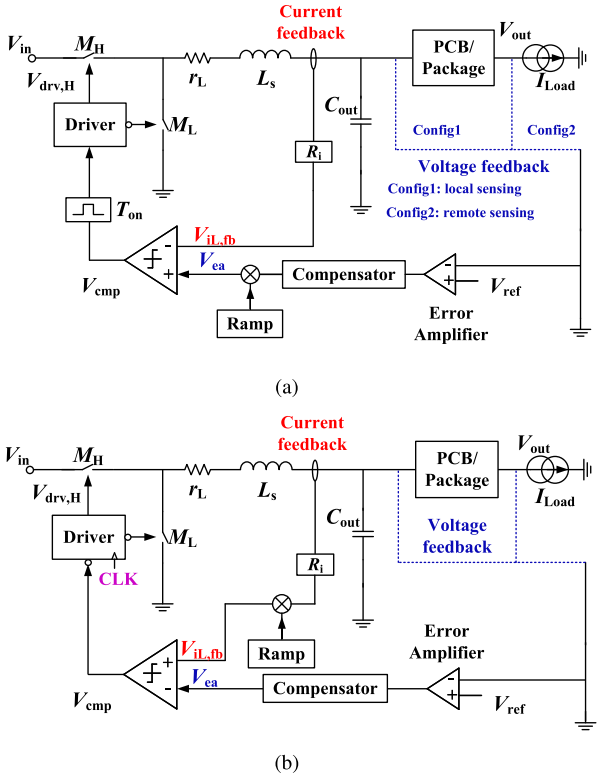


Fig. 3. Circuit diagram of the current-mode converter with (a) an AOT controller and (b) a PWM controller. The main difference is the reversely connected current loop and voltage loop feedback signals.

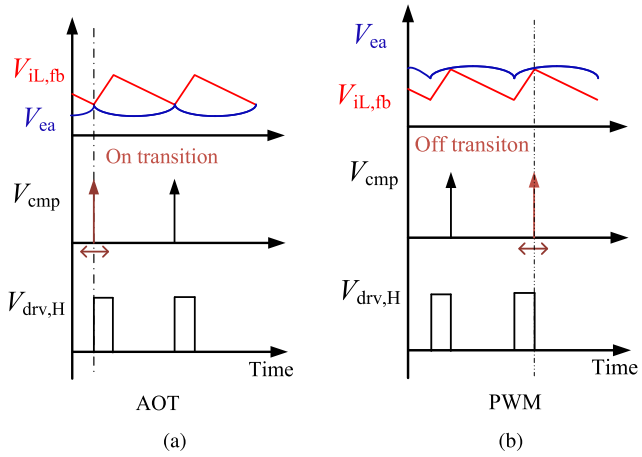


Fig. 4. Critical waveforms (in CCM operation) in the feedback circuits of the (a) AOT feedback controller and (b) PWM feedback controller.

signal $V_{\mathrm{iL,fb}}$ and the voltage loop feedback signal V_{ea} are connected to the inverting and noninverting pins of the comparator, respectively. A short pulse V_{cmp} will be generated when V_{ea} is larger than $V_{\mathrm{iL,fb}}$. The on-timer is activated by the V_{cmp}, and the high-side MOSFET M_{H} is turned ON during T_{on}. Meanwhile, the inductor current i_{L} ramps up as the inductor L is energized by input voltage V_{in}. The low-side MOSFET M_{L} is turned ON, and the inductor current decreases once T_{on} is expired. The off-time ends when V_{cmp} triggers the next on-time cycle. The overall system is stabilized when the sensed voltage is same as the reference voltage V_{ref}.

The on-time of the AOT controller is typically determined by the nominal switching frequency, input, and output voltage of the converter [30]

$$T_{\mathrm{on}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}} f_{\mathrm{nom}}} \tag{1}$$

where V_{out} is the output voltage and f_{nom} is the nominal switching frequency of the buck converter.

The circuit diagram of the PWM controller is very similar to that of the AOT controller, except for the comparator and gate driver, as shown in Fig. 3(b). The gate driver is activated by a fixed clock signal, and the output voltage is regulated by adjusting the duty cycle D of the gate driving signal. Similarly, the duty cycle is determined by the feedback loops.

As we have mentioned, accurate modeling of the feedback loop is essential to replicate the transient behaviors of a buck converter. The voltage V_{ea} and current feedback $V_{\mathrm{iL,fb}}$ signals are then critical for power noise estimation. The corresponding waveforms in the feedback circuit are shown in Fig. 4.

In the AOT controller, an adaptive on-timer is deployed and the gate driving signal will expire automatically. The output voltage is regulated by adjusting the turn-ON timing of the gate driver, as illustrated in Fig. 4(a). Fig. 4(b) plots the waveforms of the PWM controller. The gate driver is activated by a fixed clocks signal, and the output voltage is adjusted by controlling the duty cycle D or the turn-OFF timing of the PWM signal.

Even though the difference in the topology of the two controllers is relatively trivial, the nonconstant switching frequency in the AOT controller invalidates the traditional modeling method developed based on Laplace domain analysis [14], [15], [17]. In those methods, the comparator in the feedback loop is modeled as a sample-and-hold block, which is only accurate under a constant operation frequency.

III. Proposed Waveform-Based Modeling Approach for a Current-Mode Buck Converter

In this section, a topology and time-domain waveform-based modeling method is proposed for current-mode mode buck converters. The idea from the DF method is adopted to model a system with a nonconstant fundamental frequency. A similar modeling approach was developed and applied to a PWM controller in [20] and [28]. The equations are formulated in a time-domain representation, which makes the model naturally suitable for transient simulation. As an add-on feature, the same framework can be applied for both of the AOT and PWM controllers by only changing the equations which describe the current feedback loop. In this article, we assume that the buck converter is operating in the CCM, where the inductor current is always larger than zero.

The circuit depicted in Fig. 3(a) can be divided into three subcircuit blocks: the voltage feedback loop, the current feedback loop, and the power stage, which are discussed separately in the rest of the section. We note the nonideal performances of circuits, e.g., the hysteresis in the comparator and dead time in the gate driver, are not considered in the model.

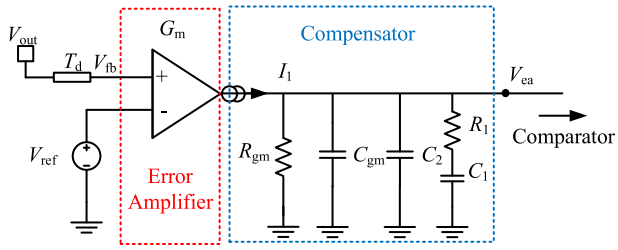


Fig. 5. Simplified circuit diagram of an error amplifier.

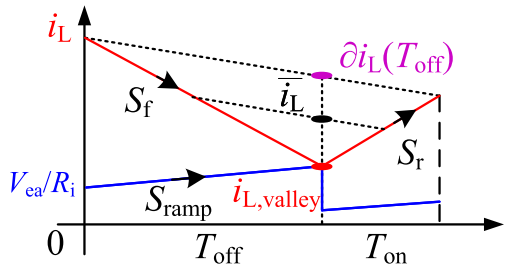


Fig. 6. Waveforms of the current feedback loop in the CCM state. [We note that the units of S_r and S_f are A/s, while the unit of S_{ramp} is V/s.]

A. Voltage Feedback Loop

Fig. 5 shows the circuit diagram of a typical type II compensator. The output voltage V_{out} is fed back to the error amplifier and compared with the internal reference voltage V_{ref}. An operational transconductance amplifier (OTA) is typically used due to its high open-loop gain and bandwidth. Another parameter in this loop is the feedback delay T_d from the instant when V_{out} is sensed to the instant when V_{fb} is updated. The output voltage V_{ea} of the OTA is analyzed in the Laplace domain and formulated as follows:

$$V_{ea} = G_m(V_{out} - V_{ref}) \times \left(R_1 + \frac{1}{sC_1}\right) // \frac{1}{sC_2} // R_{gm} // \frac{1}{sC_{gm}} \times e^{-sT_d} \quad (2)$$

where G_m is the open-loop gain of the OTA. R_1, C_1, and C_2 are compensation components in the error amplifier. R_{gm} and C_{gm} are the internal parasitics of the OTA. As C_1 is much larger than C_2 in the real implementation, its behavior can be represented by a transfer function with one zero and two poles [31]

$$V_{ea} \approx K_{dc}(V_{out} - V_{ref}) \times \frac{s - f_{z1}}{(s - f_{p0})(s - f_{p1})} \times e^{-sT_d}. \quad (3)$$

The locations of the zero and the poles are $f_{z1} = \frac{1}{2\pi} R_1 C_1$, $f_{p0} = \frac{1}{2\pi} R_{gm}(C_{gm} + C_1 + C_2)$, and $f_{p1} = \frac{1}{2\pi} R_1 C_1 (C_{gm} + C_2)/(C_{gm} + C_1 + C_2)$, respectively. K_{dc} is the dc gain of the error amplifier circuit.

B. Current Feedback Loop

In the buck converter, the voltage feedback loop is typically configured with a narrow bandwidth to achieve accurate dc regulation while the transient recovery speed is sacrificed. Therefore, the current feedback loop is important to speed up the transient response of the converter. R_i represents the total sensing gain of the current feedback loop, and the output signal $V_{iL,fb}$ can be formulated as

$$V_{iL,fb} = i_L \cdot R_i. \quad (4)$$

It is worth noting that the switching period of the AOT controller is directly determined by $V_{iL,fb}$ and V_{ea}. The derivation of average inductor current $\overline{i_L}$ is important to calculate the switching period T_{sw} in the converter. Due to the off-time modulating nature of the controller, the switching cycle start time is defined as the turn-OFF transition of high-side switching.

The inductor current is always larger than zero, and the switching period T_{sw} of the AOT controller can be separated into T_{on} and T_{off} periods

$$T_{sw} = T_{on} + T_{off}. \quad (5)$$

The inductor used in the circuit is typical with a high-quality factor, and the current flows through it can be simplified as a triangular wave. The charging and discharging slopes S_r and S_f are calculated as

$$S_r = \frac{V_{in} - \overline{i_L}(r_{on,H} + r_L) - V_{out}}{L_s} \quad (6)$$

$$S_f = \frac{-\overline{i_L}(r_{on,L} + r_L) - V_{out}}{L_s} \quad (7)$$

where r_L and L_s are the ESR and inductance of the output inductor. In this model, we assume that a linear slope compensation circuit is deployed whose rising slope is S_{ramp}. In addition, the ramp generator is reset at the crossing moment of V_{ea} and $V_{iL,fb}$, i.e., turn-ON transition of the high-side switch, as depicted in Fig. 6.

The minimum value of the inductor current in one cycle $i_{L,Valley}$ can be expressed as

$$i_{L,Valley} = i_L(T_{off}) = \frac{1}{R_i}(V_{ea} + T_{off} S_{ramp}). \quad (8)$$

Linear interpolation is then applied to the inductor current regarding $i_L(0)$ and $i_L(T_{sw})$

$$\partial i_L(t) = (i_L(T_{sw}) - i_L(0)) \times \frac{t}{T_{sw}} = (S_r T_{on} + S_f T_{off}) \times \frac{t}{T_{sw}}. \quad (9)$$

The average inductor current $\overline{i_L}$ is defined as

$$\overline{i_L} = i_{L,Valley} + 0.5 \cdot (\partial i_L(T_{off}) - i_{L,Valley}). \quad (10)$$

An equation with the independent variable T_{sw} can be constructed by substituting (5), (8), and (9) into (10)

$$\overline{i_L} = -0.5\, S_f T_{off} + 0.5\, (i_L(0) - \partial i_L(T_{off})) + i_{L,Valley}. \quad (11)$$

The switching period of the AOT controller in the CCM state can be solved by

$$T_{sw} = \frac{-2R_i i_L + 2R_i S_f T_{on} - R_i S_r T_{on} - 2S_{ramp} T_{on} + V_{ea}}{2R_i S_f - R_i S_r - 2S_{ramp}}. \quad (12)$$

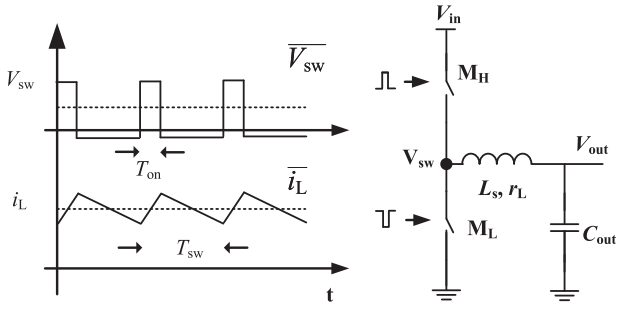


Fig. 7. Power stage waveforms, including the *LC* filter and the half-bridge inverter.

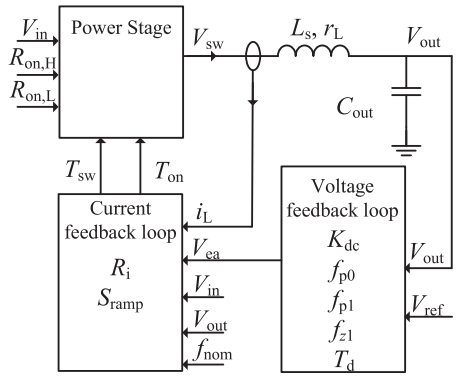


Fig. 8. Diagram of the proposed model with three subcircuits.

TABLE I
KEY PARAMETERS OF THE PROPOSED MODEL

Category	Parameter	Description
System Parameters	V_{in}	Input voltage.
	f_{nom}	Nominal switching frequency.
	C_{out}	Capacitance of output capacitor.
	L_s,r_L	Inductance and its ESR.
Device Parameters (Accessible)	$r_{on,H}$, $r_{on,L}$	On resistances of high and low side MOSFETs
	V_{ref}	Reference voltage.
Device Parameters (Integrated)	K_{dc}	DC gain of EA.
	f_{p0}, f_{p1}, f_{z1}	Zero and poles of EA.
	T_d	Remote sensing delay.
	S_{ramp}	Slope of ramp compensation.
	R_i	Current sensing gain.

C. Power Stage

The power stage includes the half-bridge inverter and the *LC* filter of the buck converter. The switching node voltage V_{sw} and the inductor current i_L are shown in Fig. 7.

In the CCM state, the conduction current is always larger than zero, and a pair of complementary pulse signals are generated to drive the two MOSFETs M_H and M_L. A triangle shape inductor current is thereby generated. Within each switching cycle, the average inductor current is denoted as $\overline{i_L}$. The average voltage of the switching node is calculated as

$$\overline{V_{sw}} = \frac{T_{on}}{T_{sw}}\left(V_{in} - \overline{i_L} r_{on,H}\right) - \left(1 - \frac{T_{on}}{T_{sw}}\right)\overline{i_L} r_{on,L} \qquad (13)$$

where $r_{on,H}$ and $r_{on,L}$ are the resistances of M_H and M_L, respectively. T_{sw} denotes the switching period of the buck converter, which is determined by both voltage and current feedback loops.

A droop voltage is induced between the inductor due to its ESR r_L, and the output voltage for the next cycle can be directly calculated as

$$V_{out} = \overline{V_{sw}} - \overline{i_L} r_L. \qquad (14)$$

D. Key Parameters and Model Implementation

Table I lists all the key parameters that are required to implement the average model, which can be divided into two groups: system parameters and device parameters. The system parameters are related to the off-chip components and circuits, and they are typically configurable and accessible to the users. The device parameters are defined as the internal parameters of the chip, and many of those parameters are not accessible due to IP protection and the integration of circuits.

The proposed average buck converter model can be fully described when the values of all parameters are provided. Fig. 8 shows the testbench for the buck converter. The testbench contains the following parts:

1) the power stage, in which the switching part is replaced by the average model;
2) the voltage feedback loop for calculating the output signal V_{ea} of the voltage loop compensator;
3) the current feedback loop for calculating the switching period T_{sw} and on-time T_{on} of the gate driving signal.

The behavior of the buck converter is described by analytical equations, and thus, the model is implemented by the combination of *RLC* components and dependent sources. In addition, it is currently built in the Keysight Advanced Design System (ADS) [32] and can be translated to different circuit simulators, e.g., Pspice and Hspice.

IV. SIMULATION VALIDATION

In this section, the simulated results are presented to validate the proposed average model. A circuit model is implemented in Simplis [33] for comparison. The parameters used in the simulations are $V_{in} = 5\,\text{V}$, $f_{nom} = 600\,\text{kHz}$, $C_{out} = 142\,\mu\text{F}$, $L_s = 500\,\text{nH}$, $r_L = 1\,\text{m}\Omega$, $r_{on,H} = 10\,\text{m}\Omega$, $r_{on,L} = 3\,\text{m}\Omega$, $V_{ref} = 0.9\,\text{V}$, $K_{dc} = 200$, $f_{p0} = 400\,\text{Hz}$, $f_{p1} = 1\,\text{MHz}$, $f_{z1} = 16.7\,\text{kHz}$, $T_d = 20\,\text{ns}$, $S_{ramp} = 240\,\text{V/ms}$, and $R_i = 0.2\,\Omega$.

Fig. 9 compares the mean values of output voltage generated by two models under different load conditions (1A–9A). The difference between the two curves is controlled within the submilivolt range, which validates the dc simulation capability of the proposed model.

Fig. 10 illustrates the load transient responses of the two models from 0.5 to 5 A and vice versa. Both rise and fall time is configured as 1μs. The recovery time and voltage drop simulated by the two models are well matched. Due to the cycle-by-cycle averaging of the model, on-off switching is not generated in the model. The difference between the two models is brought by the missing ripple, which is limited to 2 mV in the test case.

As discussed previously, the frequency variant nature of the AOT controller is the main challenge in Laplace transformation-based modeling. With the time-domain modeling technique, the

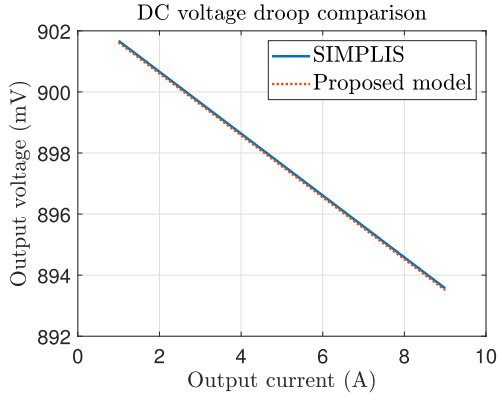


Fig. 9. Comparison of output voltages.

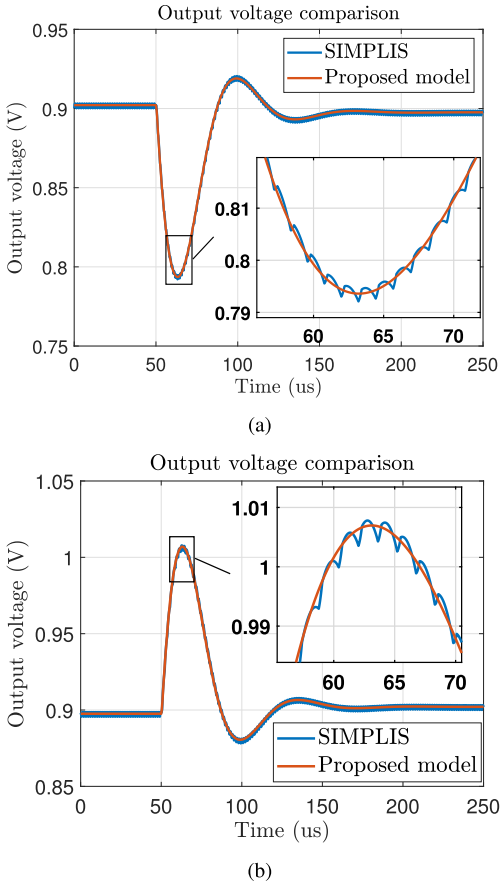


Fig. 10. Transient response of the output voltage with (a) ramp-up load, from 0.5A to 5A (rise time: 1μs); (b) ramp-down load, from 5A to 0.5A (fall time: 1μs).

change in switching period and on-time can be captured, as shown in Fig. 11. The T_{sw} and T_{on} during the transient state can be well predicted by the proposed model, and the errors are limited to 0.5%. The well-matched results further validate the proposed modeling methodology.

Finally, the comparison of output voltage when the parasitic components of PCB are demonstrated in Fig. 12. The configuration of the output capacitor in the simulation models is replaced by that of a real product, and the parasitics of a remote sensing

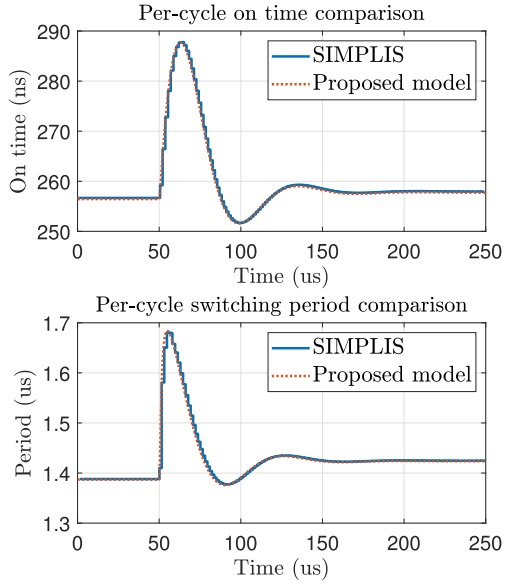


Fig. 11. Comparison of T_{sw} and T_{on} under ramp-down loading conditions, where the load current drops from 5 A to 0.5 A in 1μs.

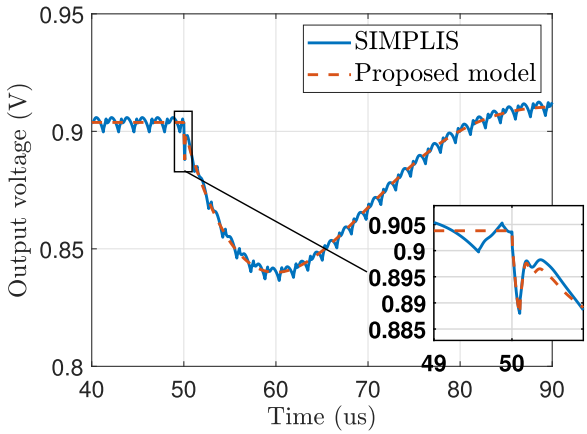


Fig. 12. Comparison of output voltages simulated by two models. The influences of PCBs and real capacitors are considered.

trace are included in the model. The extra spike due to those parasitic inductances can also be captured by the model. This indicates that the model can be used to predict power noise in a realistic application. In addition, the influence of different internal feedback parameters, e.g., the rising slope of ramp compensation and zeros and poles of the error amplifier, can be simulated by the proposed model.

V. Two-Step Parameter Extraction Method

As a modern VRM reaches higher integration levels, its internal circuits are becoming increasingly complicated. The exact feedback configurations and slope compensation circuits are not accessible to users. With the help of the time-domain modeling methodology, the trial-and-error approach is used to determine all the unknown parameters [20], [28]. However, the tuning process is extremely tedious and time-consuming, as seven or more parameters are coupled together.

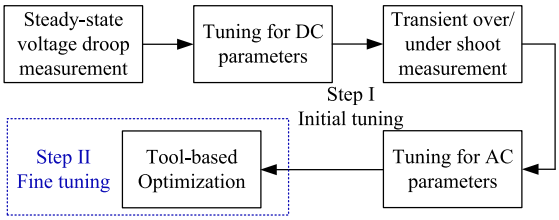


Fig. 13. Flow of the two-step parameter extraction.

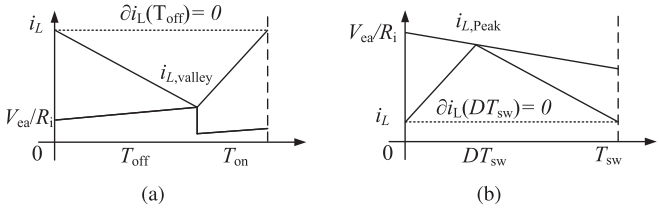


Fig. 14. Waveforms of the current feedback loop under steady-state conditions in (a) the AOT controller and (b) the PWM controller.

A novel two-step method is proposed to extract the parameters of internal circuits and replicate the time-domain behavior of a current-mode buck converter. The tuning process for the AOT controller is exemplified in this section, as shown in Fig. 13. The seven unknowns are separated into dc (K_{dc}, S_{ramp}, and R_i) and ac parameters (f_{p0}, f_{p1}, f_{p1}, and T_d). The initial values of all seven variables can be efficiently extracted from measurement or simulation, and fine-tuning can be applied to further optimize the parameters.

A. Initial Tuning

1) DC Parameters: The modeling technique demonstrated in Section III provides the simulation capability for both transient and steady-state operation of a buck converter, and the model can be greatly simplified when it is used to describe behaviors in the steady state. The output voltage of the error amplifier V_{ea} can be simplified, as only its dc gain needs to be considered. Eliminating the ac terms in (3), the V_{ea} can be formulated as

$$V_{ea} = K_{dc}(V_{out} - V_{ref}). \tag{15}$$

The per-cycle derivative of the inductor current is zero in the steady state, as shown in Fig. 14(a) and (b). The ∂i_L can be simplified as

$$\partial i_L = i_L(T_{sw}) - i_L(0) = 0. \tag{16}$$

The per-cycle average inductor current can then be formulated as

$$\overline{i_L} = i_{L,Valley} - 0.5 S_f T_{off}. \tag{17}$$

The equation can be expanded as

$$\overline{i_L} R_i - (V_{ea} + S_{ramp} T_{off}) + 0.5 R_i S_f T_{off} = 0. \tag{18}$$

The steady-state V_{out} can be obtained by substituting (15) into (18)

$$V_{out} = \frac{\overline{i_L} R_i + 0.5 T_{off} R_i S_f - S_{ramp} T_{off}}{K_{dc}} + V_{ref}. \tag{19}$$

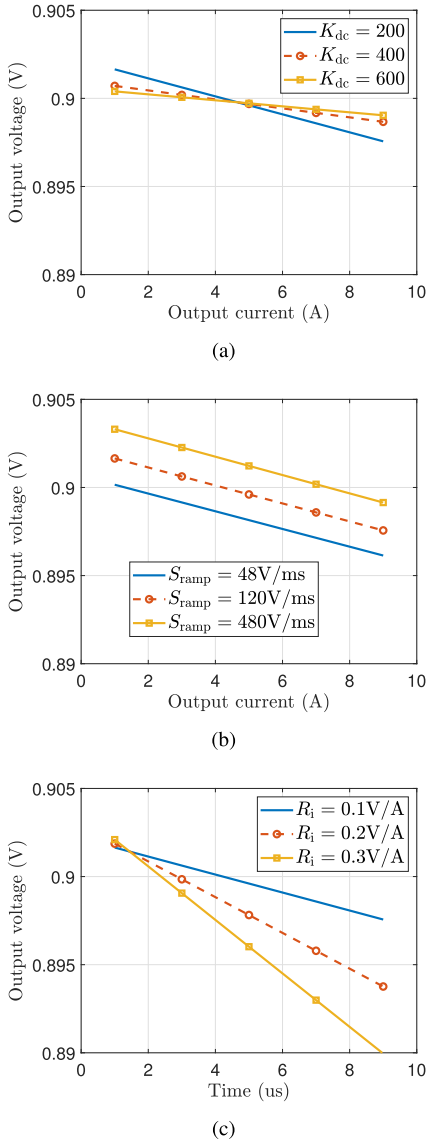


Fig. 15. Impacts of dc parameters (a) K_{dc}, (b) S_{ramp}, and (c) R_i. Default parameters are $K_{dc} = 200$, $S_{ramp} = 120$ V/ms, and $R_i = 0.1$ V/A.

TABLE II
INFLUENCE OF DC PARAMETERS

Parameter	Trend	offset	Slope
K_{dc}	↑	N/A	↓
	↓	N/A	↑
S_{ramp}	↑	↑	-
	↓	↓	-
R_i	↑	N/A	↑
	↓	N/A	↓

It can be seen that the steady-state output voltage of a current-mode buck with an AOT controller is only determined by dc parameters (K_{dc}, S_{ramp}, and R_i), and the influences of them are illustrated in Fig. 15 and Table II. It is worth noting that the same parameter tuning strategy can be applied to a current-mode buck converter with a PWM controller. The critical waveform of the current feedback loop is shown in Fig. 14(b). The steady-state per-cycle inductor current can be simplified, according to (24)

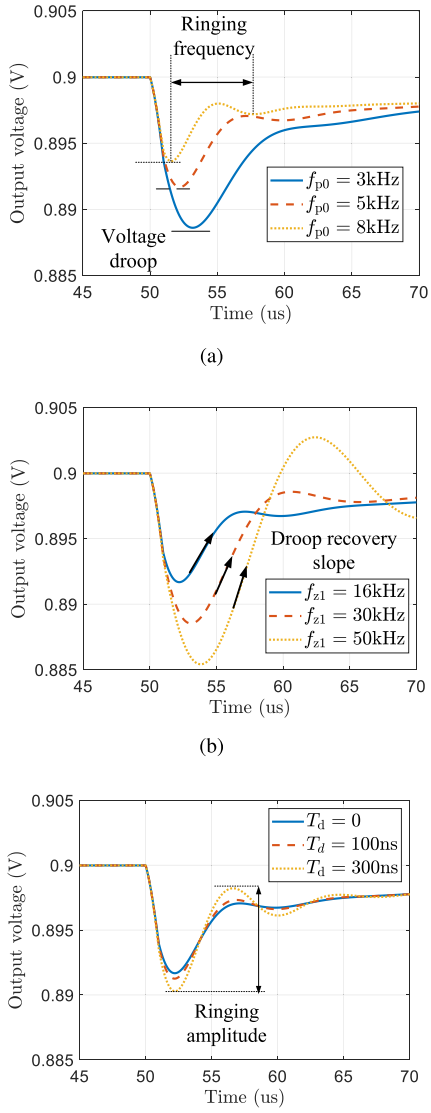


Fig. 16. Impacts of ac parameters (a) f_{p0}, (b) f_{z1}, and (c) T_d. Default parameters are $K_{dc} = 200$, $f_{p0} = 400\,\text{Hz}$, $f_{p2} = 1\,\text{MHz}$, $f_{z1} = 16.7\,\text{kHz}$, $T_d = 0\,\text{ns}$, $S_{ramp} = 240\,\text{V/ms}$, and $R_i = 0.1\,\Omega$.

in Appendix A.

$$\overline{i_L} = i_{L,Peak} - 0.5 S_r D T_{sw} \tag{20}$$

where D is the duty cycle of the PWM signal. Similarly, the V_{out} can be expressed as

$$V_{out} = \frac{\overline{i_L} R_i - 0.5 R_i D S_r T_{sw} + D S_{ramp} T_{sw}}{K_{dc}} + V_{ref}. \tag{21}$$

2) AC Parameters: The rest of the unknown parameters are treated as ac parameters that can be characterized by the transient response. The voltage droop and overshoot recovery are mainly affected by these ac parameters, and the influence of ac parameters is illustrated in Fig. 16 under ramp-up loading conditions.

The first voltage droop and the ringing frequency during recovery are mainly dominated by f_{p0}; see Fig. 16(a). The f_{z1} can be further determined by fitting the recovery slope [see Fig. 16(b)]. It is worth noting that f_{p1} only has minor impacts on the voltage droop, and the simulation result is not attached. It is suggested to set f_{p1} to twice the switching frequency according to general design guidelines. The tuning for control delay T_d by observing the ringing amplitude is depicted in Fig. 16(c).

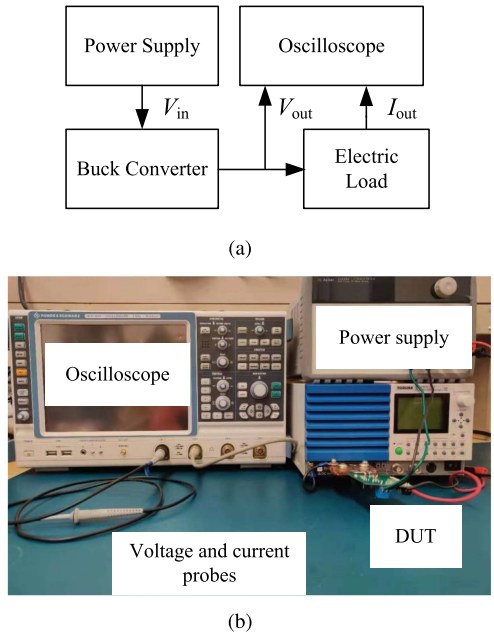


Fig. 17. (a) Configuration of characterization setup for a buck converter with the AOT controller. (b) Photograph of the measurement setup.

B. Fine-Tuning

The simulated voltage waveform based on the initial values can achieve a relatively good correlation with the measured result. The fine-tuning step only works as an optional process to further improve the accuracy. The ADS built-in optimization tool is used here to further adjust the parameters simultaneously based on the initial values obtained from the previous step.

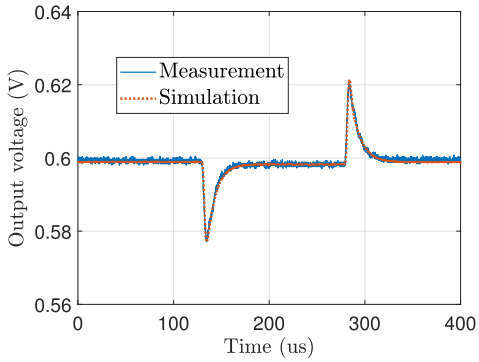
VI. Measurement Validation on a Practical Buck Converter

To further validate the proposed modeling method, the proposed modeling, and parameter extraction techniques are performed on another buck converter. We note the converter is different from the one used in the Section IV.

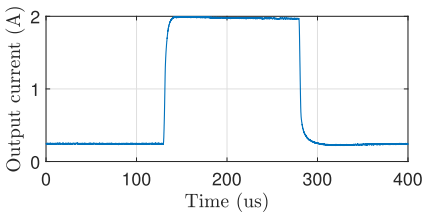
A. Measurement Validation

The configuration and photograph of the measurement setup are plotted in Fig. 17. The input voltage is configured as 3 V by a dc power supply (Agilent E3648 A). An electric load (Kikusui PLZ164WA) is used to control the current extracted from the converter. Both the output voltage and current are monitored by an oscilloscope (R&S RTO1024).

The voltage reference is configured as 0.6 V, and the switching frequency is configured as 600 kHz. The output inductor is



(a)



(b)

Fig. 18. (a) Comparison of simulated and measured output voltages. (b) Output current extracted by the slammer board. the high and low levels of current are 0.25 A and 2 A, respectively.

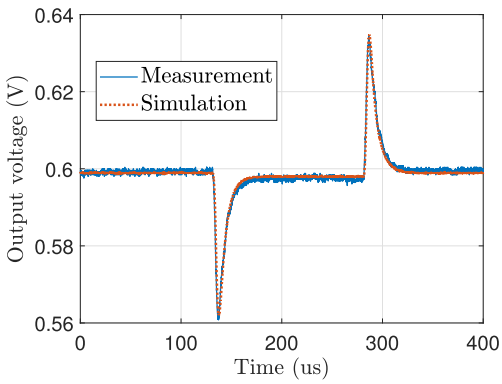


Fig. 19. Comparison of simulated and measured output voltages. The output voltage is measured under changing load current between 0.25 and 3 A.

250 nH with a 2.2 m Ω ESR, and the total output capacitance of the X7R ceramic capacitors is 118 μF considering the derate effect. In addition, the converter is configured in forced CCM mode.

Figs. 18 and 19 compare the measured and simulated output voltages under different transient loads. The load amplitudes are from 0.25 to 2 and 3 A, respectively. In addition, both rise and fall times are configured as 2μs. The simulated and measured results have good correlations for both of the conditions. The maximum differences in the output voltage are limited to 1.8 mV. This validates both the time-domain modeling approach and the parameter extraction flow. We note that the model demonstrated in Section VI was implemented within 30 min.

B. Discussion

From the comparisons between simulation and experiment, an accurate buck converter model for transient power noise is demonstrated. However, the proposed model is topology based. Larger errors may be observed when the method is applying to a buck converter with an unknown controller. Fortunately, the modeling approach can be extended to different controllers with extra efforts, e.g., voltage mode and V^2 controllers. Besides, the DCM operation is not considered in the model. The model is not applicable to the DCM mode as the waveforms in feedback controllers are different in DCM and CCM. Nevertheless, it should be emphasized that the transient power noise is more server under a heavy loading, where the buck converters are working in CCM condition. In summary, the model can predict the worst case of transient power noise, which is useful for the system-level PDN optimization.

TABLE III
COMPARISON OF SIMULATION TIME FOR DIFFERENT MODELS

Simulator	Type of Model	Stop Time	Elasped Time
ADS	SPICE	1 ms	$\sim$ 12 ms
Simplis	SPICE	1 ms	$\sim$ 2 ms
ADS	Proposed	1 ms	$\sim$ 2 ms

Benefits from the averaging technique, the proposed model has a faster simulation speed comparing with an ordinary SPICE model. The simulation speed of different models are compared in Table III. For the test case discussed in Section V, the proposed model is 5 times faster than the ordinary SPICE model. Besides, the simulation is comparable with Simplis, which is a specialized SPICE solver with piecewise linear modeling technique.

VII. CONCLUSION

An averaged model is proposed for transient power noise prediction of current-mode buck converters. Thanks to the averaging technique, the simulation speed of the proposed model is 4 times faster than traditional SPICE solver and is comparable with the state-of-art Simplis solver.

The main contribution of this article is providing a framework that can model controllers with constant and nonconstant switching frequencies. The proposed model is verified by both simulation and measurement. In addition to the modeling methodology, the model can also serve as a platform to extract the internal parameters of a current-mode buck converter. With the proposed two-step parameter extraction method, the parameter tuning procedure is greatly simplified. In the test case demonstrated in this article, the parameters are extracted within 30 min. The optimization of a system-level PDN is possible with the proposed model when the vendor's model is not provided in the early design stage.

However, the proposed model is topology based, and extra efforts are required to extend the model to different controllers.

APPENDIX A
EQUATIONS FOR PWM CONTROLLER

As discussed in Fig. 4, the PWM and AOT controllers have reversed connections regarding the inputs of the comparator. The waveforms in the current feedback loop are plotted in Fig. 20. The rest of the circuits remain the same, and all variables are defined the same as in Section III.

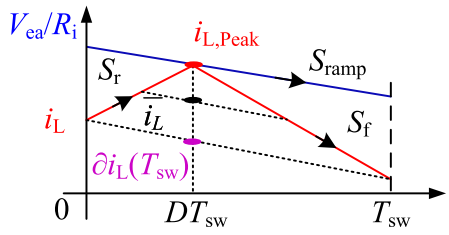


Fig. 20. Waveforms of the current feedback loop in the CCM state for a PWM controller. The clock period is defined as T_{sw}.

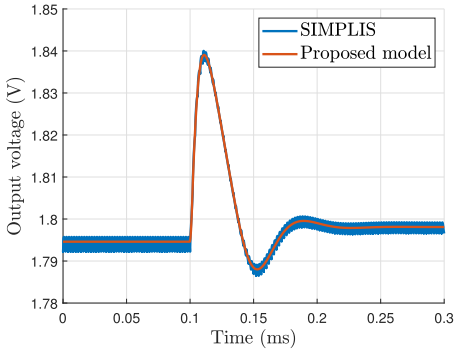


Fig. 21. Comparison of the output voltage of a current-mode buck converter with the PWM controller.

The peak value of the inductor current within one cycle $i_{L,Peak}$ is calculated as

$$i_{L,Peak} = i_L(DT_{sw}) = \frac{1}{R_i}(V_{ea} - DT_{sw}S_{ramp}). \quad (22)$$

Similarly, the per-cycle average inductor current $\overline{i_L}$ is calculated as

$$\overline{i_L} = i_{L,Peak} - 0.5 \cdot (i_{L,Peak} - i_L(0) + \partial i_L(DT_{sw})). \quad (23)$$

The duty cycle of can then be solved as

$$D = 0.5 + \frac{S_{ramp}}{D_s R_i} - \sqrt{\left(0.5 + \frac{S_{ramp}}{D_s R_i}\right)^2 - \frac{2}{T_{sw} D_s}\left(\frac{V_{ea}}{R_i} - \overline{i_L}\right)}. \quad (24)$$

V_{out} can be derived by rewriting (13) with respect to D

$$\overline{V_{sw}} = D(V_{in} - \overline{i_L} r_{on,H}) - (1 - D)\overline{i_L} r_{on,L}. \quad (25)$$

The model is validated by a model implemented in the SIMPLIS, as shown in Fig. 21.

REFERENCES

[1] J. Sun, H. Wang, K. Wu, and J. Fan, "A pattern-based analytical method for impedance calculation of the power distribution network in mobile platforms," *IEEE Trans. Electromagn. Compat.*, vol. 63, no. 3, pp. 912–921, Jun. 2021.

[2] Y. Sun, J. Lee, and C. Hwang, "A generalized power supply induced jitter model based on power supply rejection ratio response," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 29, no. 6, pp. 1052–1060, Jun. 2021.

[3] J. Chen and M. Hashimoto, "A frequency-dependent target impedance method fulfilling voltage drop constraints in multiple frequency ranges," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 10, no. 11, pp. 1769–1781, Nov. 2020.

[4] D. Prasad et al., "Buried power rails and back-side power grids: Arm CPU power delivery network design beyond 5 nm," in *Proc. IEEE Int. Electron Devices Meeting*, 2019, pp. 19.1.1–19.1.4.

[5] P. K. D. Pramanik et al., "Power consumption analysis, measurement, management, and issues: A state-of-the-art review of smartphone battery and energy usage," *IEEE Access*, vol. 7, pp. 182113–182172, 2019.

[6] "Evaluating DC-DC converters and passive PDN components," Accessed: Oct. 19, 2022. [Online]. Available: https://www.keysight.com/us/en/assets/7018-02564/application-notes/5990-5902.pdf

[7] E. H.-K. Hsiung, Y.-L. Li, R.-B. Wu, T. Su, Y.-S. Cheng, and K.-B. Wu, "A linear 4-element model of VRM –characteristics, practical uses and limitations," in *Proc. IEEE Elect. Des. Adv. Packag. Syst. Symp.*, 2012, pp. 13–16.

[8] J. Kim, Y. Takita, K. Araki, and J. Fan, "Improved target impedance for power distribution network design with power traces based on rigorous transient analysis in a handheld device," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 3, no. 9, pp. 1554–1563, Sep. 2013.

[9] T.-L. Wu, H.-H. Chuang, and T.-K. Wang, "Overview of power integrity solutions on package and PCB: Decoupling and EBG isolation," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 2, pp. 346–356, May 2010.

[10] K. Shringarpure et al., "Sensitivity analysis of a circuit model for power distribution network in a multilayered printed circuit board," *IEEE Trans. Electromagn. Compat.*, vol. 59, no. 6, pp. 1993–2001, Dec. 2017.

[11] S. Baek, P. Pun, and A. Agrawal, "Behavioral model of switching DC-DC converter for improving power delivery network design," in *Proc. IEEE 62nd Electron. Compon. Technol. Conf.*, 2012, pp. 926–929.

[12] S. B. Nasir, Y. Lee, and A. Raychowdhury, "Modeling and analysis of system stability in a distributed power delivery network with embedded digital linear regulators," in *Proc. 15th Int. Symp. Qual. Electron. Des.*, 2014, pp. 68–75.

[13] B. Gustavsen and H. J. De Silva, "Inclusion of rational models in an electromagnetic transients program: Y-parameters, Z-parameters, S-parameters, transfer functions," *IEEE Trans. Power Del.*, vol. 28, no. 2, pp. 1164–1174, Apr. 2013.

[14] J. Sun, D. M. Mitchell, M. F. Greuel, P. T. Krein, and R. M. Bass, "Averaged modeling of PWM converters operating in discontinuous conduction mode," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 482–492, Jul. 2001.

[15] R. B. Ridley, "A new, continuous-time model for current-mode control (power convertors)," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, Apr. 1991.

[16] J. Li and F. C. Lee, "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1218–1230, May 2010.

[17] A. Davoudi, J. Jatskevich, and T. De Rybel, "Numerical state-space average-value modeling of PWM DC-DC converters operating in DCM and CCM," *IEEE Trans. power Electron.*, vol. 21, no. 4, pp. 1003–1012, Jul. 2006.

[18] A. C. Schittler, D. Pappis, C. Rech, A. Campos, and M. A. Dalla Costa, "Generalized state-space model for the interleaved buck converter," in *Proc. 11th Braz. Power Electron. Conf.*, 2011, pp. 451–457.

[19] G. Migoni, M. E. Romero, F. Bergero, and E. Kofman, "A mixed modeling approach for efficient simulation of PWM switching mode power supplies," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9758–9767, Oct. 2019.

[20] J. Sun, *Accurate Modeling Techniques for Power Delivery*, Ph.D. dissertation, Missouri Univ. Sci. Technol., Rolla, MO, USA, 2020.

[21] S. Bari, Q. Li, and F. C. Lee, "A new fast adaptive on-time control for transient response improvement in constant on-time control," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2680–2689, Mar. 2018.

[22] C.-F. Nien et al., "A novel adaptive quasi-constant on-time current-mode buck converter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 8124–8133, Oct. 2017.

[23] P.-L. Wong and F. C. Lee, "Switching action delays in voltage regulator modules," in *Proc. APEC. 17th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2002, vol. 2, pp. 675–678.

[24] J. Sun, "Small-signal modeling of variable-frequency pulsewidth modulators," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 38, no. 3, pp. 1104–1108, Jul. 2002.

[25] J. Li and F. C. Lee, "Modeling of V2 current-mode control," *IEEE Trans. Circuits Syst. I, Reg, Papers*, vol. 57, no. 9, pp. 2552–2563, Sep. 2010.

[26] S. Tian, F. C. Lee, Q. Li, and Y. Yan, "Unified equivalent circuit model and optimal design of V2 controlled buck converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1734–1744, Feb. 2016.

[27] A. Huang et al., "Time domain continuous-time model of current mode buck converter for power delivery network design," in *Proc. IEEE Int. Joint EMC/SI/PI EMC Europe Symp.*, 2021, pp. 1133–1138.
[28] J. Sun, Y. Yan, H. Wang, E. Chen, K. Wu, and J. Fan, "Topology-based accurate modeling of current-mode voltage regulator modules for power distribution network design," *IEEE Trans. Electromagn. Compat.*, vol. 64, no. 2, pp. 524–535, Apr. 2022.
[29] X. Li, X. Ruan, Q. Jin, M. Sha, and K. T. Chi, "Small-signal models with extended frequency range for DC–DC converters with large modulation ripple amplitude," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8151–8163, Sep. 2018.
[30] C.-H. Tsai, B.-M. Chen, and H.-L. Li, "Switching frequency stabilization techniques for adaptive on-time controlled buck converter with adaptive voltage positioning mechanism," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 443–451, Jan. 2016.
[31] A. Ghosh and S. Banerjee, "Design and implementation of type-II compensator in DC-DC switch-mode step-up power supply," in *Proc. Third Int. Conf. Comput., Commun., Control Inf. Technol.*, 2015, pp. 1–5.
[32] "Pathwave advanced design system," Accessed: Oct. 19, 2022. [Online]. Available: https://www.keysight.com.cn/cn/zh/products/software/pathwave-design-software/pathwave-advanced-design-system.html
[33] "Simplis reference manual," Accessed: Oct. 19, 2022. [Online]. Available: https://simplis.com/support/documentation/learning-simplis

Anfeng Huang (Member, IEEE) was born in Guangxi, China, in July 1992. He received the B.E. and M.S. degrees in electrical engineering from Xidian University, Shaanxi, China, in 2014 and 2017, respectively, and the Ph.D. degree in electrical engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in 2022.

He is currently with Detooltech, Ningbo, China. His current research interests include EMI in power electronics, magnetic material characterization, and advanced measurement techniques.

Jingdong Sun (Member, IEEE) received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2014, and the M.S. and Ph.D. degrees in electrical engineering from the Missouri University of Science and Technology, Rolla, MO, USA, in 2016 and 2020, respectively.

He is currently with Tesla, Palo Alto, CA, USA, as a Staff Electronic Design Engineer. His research interests include device modeling for electromagnetic interference and power distribution network applications, signal/power integrity, and wireless power transfer systems.

Hongseok Kim (Member, IEEE) received the Ph.D. degree in electrical engineering (division of future vehicle) from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2017.

He was a Visiting Assistant Research Professor from June 2019 to December 2019 and an Assistant Research Professor from January 2020 to August 2021 with EMC Laboratory, Missouri University of Science and Technology, Rolla, MO, USA. He is currently a President of CPS Tech, Inc., Seoul, South Korea, and EMC Design Partners LLC, Las Vegas, NV, USA. He has provided electromagnetic compatibility (EMC) analysis and design consulting services for automotive companies including Hyundai Motor Company, Hyundai Mobis, and LG Electronics. His research interests include EMC modeling and design for power electronics, such as dc–dc resonant converter, PFC boost converter, wireless charging system, and motor drive system.

Zhenxue Xu (Senior Member, IEEE) received the B.S. and M.S. degrees from Tsinghua University, Beijing, China, in 1991 and 1996, respectively, and the Ph.D. degree from Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA, USA, in 2003, all in electrical engineering.

Since 2018, he has been with Google, Inc., Mountain View, CA, USA, as a Senior Power Engineer for consumer hardware. His research interest includes the modeling, control and design of the high performance dc/dc and ac/dc power converters, and wireless charging systems.

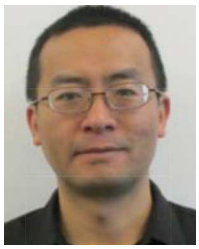
Shuai Jin (Member, IEEE) received the B.S. degree in biomedical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2011, and the M.S. and Ph.D. degrees in electrical engineering from the Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla, MO, USA, in 2013 and 2017, respectively.

He is currently a Signal Integrity Engineer with Google Platform. His research interests include signal integrity in high-speed digital systems, power distribution network modeling, RF interference, and high-speed package modeling.

Songping Wu (Senior Member, IEEE) received the B.S. and M.S. degrees from Huazhong University of Science and Technology, Wuhan, China in 2003 and 2006, respectively, and the Ph.D. degree from the Missouri University of Science and Technology, Rolla, MO, USA, in 2011.

He is currently with Rivos, Inc., as SI/PI lead. From 2011 to 2012, he was with Cisco as a Senior SI/PI Engineer. From 2012 to 2016, he with Apple Computer, Cupertino, CA, USA, as a Principal Engineer. From 2016 to 2021, he was with Google LLC, Mountain View, CA, USA, as a Staff Engineer. He has authored or coauthored more than 55 research papers and five patents. His research and patents have been applied in Google Chromebook, Apple iPhone 5S/6/6S, etc. His research interests include signal integrity and power integrity methodology development for die/package/board co-design, Chiplet/2.5-D/3-D packaging, high-speed serial signaling technology, and RF interference.

Dr. Wu was the Chair of TC10 Signal Integrity and Power Integrity Committee and has been with SI/PI and EMC Society since 2007. He was the recipient of the 2011 IEEE President's Memorial Award.

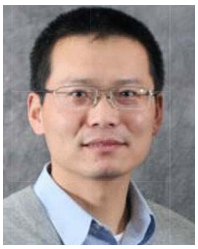


Zhiping Yang (Fellow, IEEE) received the B.S. and M.S. degrees from Tsinghua University, Beijing, China, in 1994 and 1997, respectively, and the Ph.D. degree from the University of Missouri-Rolla, Rolla, MO, USA, in 2000, all in electrical engineering.

He is currently a Senior Hardware Manager with Google Consumer Hardware Group. From 2000 to 2005, he was with Cisco Systems, San Jose, CA, USA, as a Technical Leader. From 2005 to 2006, he was with Apple Computer, Cupertino, CA, USA, as a Principal Engineer. From 2006 to 2012, he was with Nuova Systems (which was acquired by Cisco in 2008) and Cisco Systems as a Principal Engineer. From 2012 to 2015, he was with Apple as a Senior Manager. He has authored or coauthored more than 70 research papers and 20 patents. His research and patents have been applied in Google Chromebook, Apple iPhone 5S/6/6S, Cisco UCS, Cisco Nexus 6K/4K/3K, and Cisco Cat6K products. His research interests include signal integrity and power integrity methodology development for die/package/board co-design, high-speed optical module, various high-speed cabling solutions, high-speed DRAM/storage technology, high-speed serial signaling technology, and RF interference.

Kelvin Qiu received the B.S. and M.S. degrees in information physics from Nanjing University, Nanjing, China, and the M.S.E.E. degree from Clemson University, Clemson, SC, USA.

In 2003, he joined Cisco and specializes in ASIC package SI/PI, and PCB Board signal integrity design. His research interests include high-speed serial links signaling design, backplane and optical module interconnect optimization and measurement, and also Serdes (PAM4/NRZ) technology. He is a Technical Member of OIF and involves in 112G Ethernet standard. In 2021, he joined Google and specialized in PCB PDN design and optimization. He has authored or coauthored multiple papers in the IEEE conferences and Journals.



Jun Fan (Fellow, IEEE) received the B.S. and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively, and the Ph.D. degree in electrical engineering from the University of Missouri-Rolla, Rolla, MO, USA, in 2000.

From 2000 to 2007, he was with NCR Corporation, San Diego, CA, USA, as a Consultant Engineer. In July 2007, he joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), and is currently the Cynthia Tang Missouri Distinguished Professor in computer engineering and the Director of the Missouri S&T EMC Laboratory. He is also the Director of the National Science Foundation (NSF) Industry/University Cooperative Research Center (I/UCRC) for Electromagnetic Compatibility and Senior Investigator of Missouri S&T Material Research Center. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, intrasystem EMI and RF interference, PCB noise reduction, differential signaling, and cable/connector designs.

Dr. Fan was the Chair of the TC-9 Computational Electromagnetics Committee from 2006 to 2008, Chair of the Technical Advisory Committee from 2014 to 2016, and a Distinguished Lecturer in 2007 and 2008. He is an Associate Editor for IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY and IEEE EMC magazine. He was the recipient of the IEEE EMC Society Technical Achievement Award in August 2009.

Chulsoon Hwang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2007, 2009, and 2012, respectively.

From 2012 to 2015, he was with Samsung Electronics, Suwon, South Korea, as a Senior Engineer. In July 2015, he joined the Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla, MO, USA, where he is currently an Assistant Professor. His research interests include RF desense, signal/power integrity in high-speed digital systems, EMI/EMC, hardware security, and machine learning.

Dr. Hwang was the recipient of the AP-EMC Young Scientist Award, Google Faculty Research Award, and Missouri S&T's Faculty Research Award. He was the corecipient of the IEEE EMC Best Paper Award, AP-EMC Best Paper Award, and two-time DesignCon Best Paper Award.