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AN ACCURATE DIGITAL INSTRUMENT TO MEASURE REACTOR PERIOD

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ABSTRACT

At facilities having a research-training reactor, such as the University of Missouri-Rolla Reactor (UMRR), one finds it necessary to perform a large number of rod calibrations during the course of the year. In practice rod worths are determined by measuring the reactor period created by an incremental withdrawal of the rod under calibration. Period is then related to reactivity thru the use of a publication such as the AEC publication, IDO16485.

This frequent measurement of period makes it desirable to have a simple, automatic and accurate method to make such measurements. At UMRR we have designed, constructed and installed such an instrument. The instrument measures doubling time rather than period but, thru the use of an internal time base conversion, displays a four bit decimal number that is the reactor period in seconds. The instrument is simple in concept and utilizes the 7400 Series integrated circuits in the largest portion of the unit. The instrument is easy to operate and once initiated, will automatically complete the measurement of the period displaying the results. Error in the instrument can be shown to be less than 1.5%. Thus the unit meets the three requirements of simplicity, accuracy and ease of operation and in addition is moderately inexpensive, less than $120.

I. INTRODUCTION

The Atomic Energy Commission's licensing requirements make it necessary to determine rod worth curves at intervals not to exceed six months as well as recalibration following changes in core configuration. At research-training facilities like the University of Missouri-Rolla Reactor (UMRR), a 200 $Kw_{thermal}$ swimming-pool reactor, such rod calibrations occur quite frequently. At UMRR rod worth curves are performed by staff at six months intervals and following interim changes of core configuration. They are also performed as laboratory experiments by students in Nuclear Engineering.

Rod worth determinations are made by experimentally determining the reactor period generated by the incremental withdrawals of the rod under calibration, then relating the period to reactivity thru AEC publication, IDO16485. Since period is defined as the amount of time required for reactor power to increase by a factor of the exponential constant "e", the measurement to be made is time as a function of power. The method of making this measurement is to withdraw the rod a specific distance and after the initial transients have died away a manual measurement is made of the time for reactor power to increase from 30 to 81% as observed on the Linear Power Recorder. The 30 to 81% change is approximately a factor of "e" increase. This method of measurement requires interpolation of the signal observed, since the minor divisions on the recorder in question are 2% increments. It is difficult to calculate the accuracy of measurements made in this manner since the operator is an integral part of the measurement. One may assume that, on the average, the operator is able to resolve reactor power to within ± 1% with an occasional operator induced error. In addition to the resolving error the recorder has a quoted figure of ± 0.3% for linearity.

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The purpose to this paper is to detail a digital system that is capable of measuring and displaying period. The system is automatic, except for an initiation signal from the operator. The instrument has an eight stage Analog to Digital Convertor with a resolving accuracy of plus or minus the least significant digit (± LSD). This is a resolving accuracy of ±0.4%. The linearity figure for the convertor is ±½ LSD or ± 0.2% if expressed as a percentage. The two sources of error create an uncertainty in the period measurement that is inversely proportional to the initial power level. (Refer to Topic IV) If one uses the optimum range of the instrument, initial power equal to one-half the full scale power, the maximum possible instrument error can be shown to be less than 1.5%. The device has been installed at the UMRR and fulfills its intended function during the rod calibration procedures.

II. THEORY OF OPERATION

Reactor period is defined as the time necessary for the reactor power to increase by the exponential constant "e" and is normally expressed in seconds. It may be measured by determining the elapsed time for such an increase or by measuring the time for power to increase by a factor of two, "Doubling Time", and then converting to period by dividing by the natural logarithm of two. This can be shown in the following manner:

$P(t) = P_0 \cdot e^{t/T}$ where, t = time from $P(0) = P_0$

T = Reactor Period

P_0 = Initial power level

When $P(t) = 2 \cdot P_0$ the power is twice the initial value and the variable, time, is defined to be t_2.

$$2 \cdot P_0 = P_0 \cdot e^{t_{2/T}}$$

$$2 = e^{t_{2/T}}$$

$$\ln 2 = t_{2/T}$$

$$T = t_{2/\ln 2} \simeq t_{2/0.69}$$

The instrument installed at the UMRR measures the elapsed doubling time and internally converts real time seconds to equivalent

period seconds. The instrument can be divided into three sections for discussion purposes, shown in Figure 1.

A. Analog to Digital Convertor

The section contains a tracking Analog to Digital Convertor whose input is a zero to -5 volt analog signal that is proportional to the present reactor power and whose output is an unsigned 8 bit binary number which is sent to the Decision Logic board.

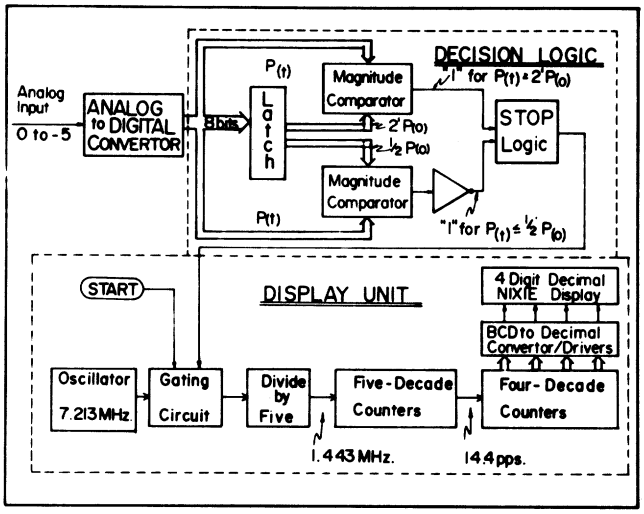

Figure 1. Block Diagram of the System

B. Decision Logic

This unit inputs the 8 bit number and upon initiation of a measurement locks the initial value of P_0 into a register. The board then begins to compare the present value received from the Analog to Digital Convertor against the initial value. This comparison continues until the present value is either twice or one-half the initial value. At this time the Decision Logic unit outputs a termination signal to the Display Logic board.

C. Display Logic

The unit is basically a four stage counter with an input gating circuit. The gate is opened when the START push button is pushed and is closed by the STOP signal from the Decision Logic board. Since the interval between initiation and termination is the doubling time, one must convert to reactor period by dividing by the natural logarithm of two. This is accomplished internally in the Display Unit by dividing the real time, time base by the natural logarithm of two and using the equivalent period time base as the input to the four digit display register.

III. CIRCUIT OPERATION

This section is intended to give a complete detailed description of the sub-sections of the device and to describe the interactions of the sub-sections in the complete system.

A. Analog to Digital Convertor

The heart of the Analog to Digital Convertor is a solid state Digital to Analog Convertor (DAC) module that converts an eight bit binary number to a proportional current. Referring to Figure 2 we examine the operation of the circuit. For an illustrative example we assume that the input to J1 is a -1 volt signal and the 8 bit counter is initially reset, zero current output, so the voltage at the test point (TP) will be negative. This negative signal is converted to a logic "1" by the μ710 comparator circuit. The direction Flip-Flop is set when the CLOCK1 timing pulse is generated. This will partially enable the upper NAND gate. The gate will be completely enabled when the CLOCK2 pulse is generated, however, the Up pulse doesn't enter the 74193 reversible counter until the trailing edge of CLOCK2, due to the triggering characteristics of the counter. With a count of 1 in the counter the current out of the DAC is about 7.8 microamperes which developes about +4.4 millivolts at pin 15 of the convertor, thus reducing the negative voltage at the TP by a small amount. The process is continued until the 8 bit counter reaches a count of 52_{10} or 110100_2. The current out of the DAC will be about 406 micro-amps, while the current removed from the TP node by the -1 volt input signal is about 400 micro-amps. Thus the voltage at the TP is now a small positive voltage which is converted to a logic "0" by the μ710 comparator. The direction Flip-Flop is reset by the CLOCK1 pulse and the register is counted down one bit by the CLOCK2 pulse. At a count of 51_{10} or 110011_2 the voltage at the TP is negative which generates an Up pulse during the next clock cycle. The convertor continues to oscillate back and forth between a count of 51_{10} and 52_{10} until one changes the input voltage. The Analog to Digital Convertor will continually track the input signal until one depresses the START push button, at which time the timing circuit is momentarily frozen at CLOCK4 time. This allows the transfer of the 8 bit word from the convertor to the Decision Logic board to be free from switching transients.

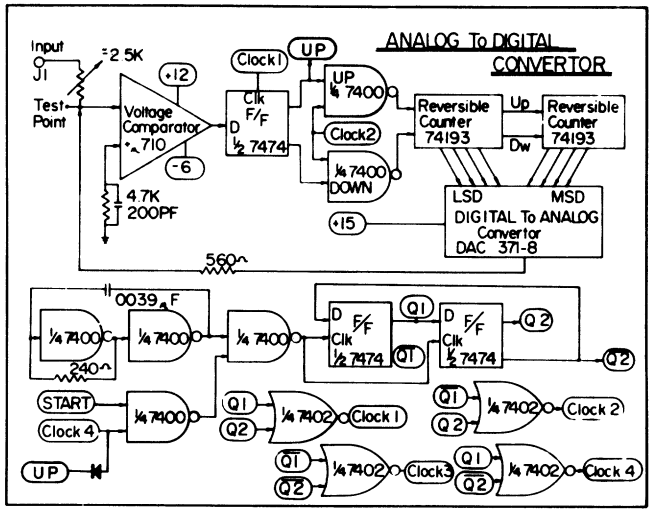

Figure 2. Analog to Digital Convertor

The remaining circuit on the Analog to Digital board is the clock and timing circuit which consists of an astable multivibrator and a two stage binary counter. The two stage counter is decoded by four NOR gates into four distinct timing pulses, CLOCK1 thru CLOCK4. The astable runs at approximately 100 kHz and thus the timing pulse frequency is about 25 kHz. This gives the convertor a resolution time for a full scale step input of about 0.01 seconds, which would give a tracking rate of 500 volts/sec. Comparing this to the maximum expected input rate of change of 0.182 volts/sec. we see that the convertor's tracking ability is well in excess of that required to follow input variations.

B. Decision Logic Board

The Decision Logic board, Figure 3, takes as an input the 8 bit binary number from the Analog to Digital Convertor. When the STROBE signal from the START push button is received, the present digital value of the reactor power is stored in the two 7475 latches. The inverted output of the latches is fed into two 8 bit adder chains. In the first adder chain the latch output is shifted one position left with the LSD and the input carry both hard-wired at a logic "1" level. This means that when the 8 bit number from the convertor has doubled from its' initial value the first adder chain will generate a carry out signal. As an illustrative example assume the initial digital value is a count of 100_{10} or 01100100_2.

$P(0) = 01100100$

$\overline{L} = 10011011$

Thus $\overline{L}$ left shifted one position and with a hard-wired logic "1" LSD, the first input to the adder is:

$\overline{L}^* = 00110111$

The second input is the 8 bit digital input from the Analog to Digital Convertor, which at the region of interest will be twice P(0) or $200_{10} = 11001000_2$. The third input is a hard-wired "1" carry-in. Thus the adder chain sums:

$2 \cdot P(0) = 11001000$

$\overline{L}^* = 00110111$

Carry-in = 1

00000000 plus a "1" carry-out signal.

Thus the first adder chain generates a logic "1" carry-out signal when P(t) is greater than or equal to twice P(0).

The second adder chain works in a similar fashion, except the carry-out signal becomes a zero when P(t) is less than or equal to one-half P(0). For example:

$P(0) = 100_{10} = 01100100$

$\overline{L} = 10011011$

Creating the modified signal, $\overline{L}^{**}$ by right shifting the binary number one position and making the MSD a "1".

$\overline{L}^{**} = 11001101$

Plus $\frac{1}{2} \cdot P(0) = 00110010$

11111111 with a "0" carry-out.

The logic "0" carry-out signal from the second adder chain is fed thru a NAND gate used as a simple invertor. This signal and the output of the first adder chain are gated with the CLOCK4 pulse from the Digital to Analog Convertor, creating a "0" $\overline{STOP}$ signal when the power level has either doubled or been reduced to one-half the original value frozen in the 7475 latches when the START push button was depressed.

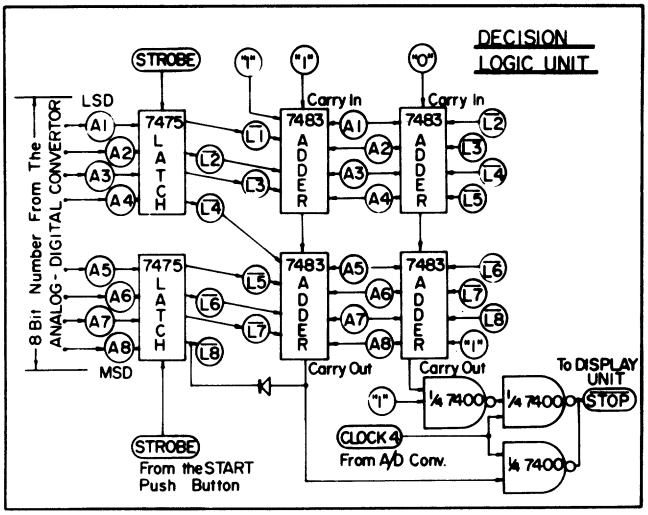

Figure 3. Decision Logic Unit

One item in the circuit that is not self-explanatory is the purpose of the diode from the carry-out of the first adder chain to the $\overline{L}_8$ output. The diode inhibits an erroneous $\overline{STOP}$ signal that would be generated when one would attempt to measure negative periods and the initial count in the register would contain a logic "1" in the MSD. Rather than belabor the point it is suggested that the reader examine the behavior of the first adder chain, as was done in a previous example, assuming an initial value of 128_{10}. If this is done one will find that carry-out "1's" are generated immediately after the initiation of the measurement unless inhibited by the diode.

C. Display Logic Board

The Display Board, Figure 4, is simply a gated decade counter that counts clock pulses from a crystal controlled oscillator. The gate is opened in the following manner, by depressing the START push button the NAND-NAND

flip-flop is set, which partially enables the NOR gate. When the push button is released the NOR gate is fully enabled and clock pulses are then gated into the display counter via the NAND gate.

The oscillator frequency was determined as much by economics as by reactor theory. The desired display was to be a four digit decimal number including one decimal place. The time base counted into the display unit is to be tenths of reactor period equivalent seconds rather than real time tenths of seconds. Real time is converted to equivalent period seconds by dividing by the natural logarithm of 2.0 which is 0.69315. This requires an input pulse rate of 14.427 pps into the four stage decimal display register. For crystal stability one is restricted to values above 100 kHz using divider circuits to achieve the lower frequencies. Crystals of 144.270 kHz and 1.442 695 MHz were found to be unrealistically priced. By multiplying 1.442 695 by 5 we find that 7.213 475 MHz lies in the middle of the 40 meter amateur radio band where crystals can be ordered at a reasonable cost. The additional cost of adding two more 7490 decade counters to the display unit is minimal when compared to the cost of the special purpose crystal. Thus the display unit consists of a 7.213 MHz oscillator, a divide by five section of a 7490 decade counter, five divide by ten decade counters (7490's) followed by four more decade counters (7490's) those outputs are tied to BCD drivers (7441's) for the Nixie tube display units. The counter is enabled as previously discussed and counting is terminated by the $\overline{\text{STOP}}$ signal from the Decision Logic board. The display is reset by depressing the START push button.

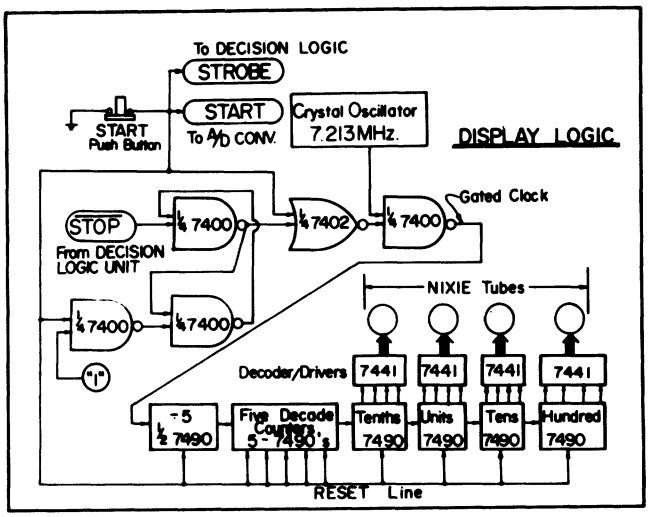

Figure 4. Diplay Logic

The oscillator used in the system is an untuned Pierce with a common emitter follower stage for isolation. The output of the CE stage is clipped at a five volt level by a zener diode to make the oscillator output compatible with TTL logic circuits.

IV. CALIBRATION AND ACCURACY

The pico-ammeter at UMRR provides a 0 to -5 volt signal proportional to 0 to 120% of the instrument's range, with nine usable ranges from 2 watts to 200 kilowatts. The period measuring device should be calibrated so that a -5 volt input yields a count oscillating between 254_{10} and 255_{10}. This is accomplished by first shorting the input and observing that the 8 bit number from the A/D Convertor is oscillating between a count of zero and one, then one inputs a -5 volt signal and adjusts the potentiometer until the count from the convertor varies between 254_{10} and 255_{10}. The preceding item is the only adjustment required on the unit and following that, the unit may be installed and connected to the pico-ammeter.

Accuracy of the unit is determined by the four factors listed below:

1. Voltage resolution in the A/D Convertor.
2. Linearity of the A/D Convertor.
3. Resolution time of the A/D Convertor.
4. Time base inaccuracy.

The last two factors are disregarded as sources of error since the resolving time of the unit is much faster than the maximum rate of change of the input and the time base will have less than 0.01% deviation due to the use of the crystal oscillator. Thus the accuracy is determined by the two factors generated in the A/D Convertor.

The first source of error is related to the one bit variation in the LSD of the A/D Convertor. This variation in count is an uncertainty in power since the signal we are performing the conversion on is proportional to power. We may relate uncertainty in power to uncertainty in time in the following manner:

1. Solve the power equation for time.
2. Differentiate with respect to power.
3. Replace dt and dP with Δt and ΔP, the respective uncertainties in time and power, then solve for Δt.

At the beginning of a measurement there will not be any uncertainty in time because the counter is started by the START push button, however, there will be an uncertainty at the end of the measurement because of the power uncertainty created by the resolving error of the system. In the normal A/D Convertor the uncertainty is $\pm\frac{1}{2}$ LSD. In tracking convertors the uncertainty is $\pm$ LSD because the count varies above and below the true value, thus at any instant the true value could lie as much as one count above or below the indicated value. This $\pm$ one count variation is doubled in the instrument creating a four count error band in the termination of the measurement. This error band has been reduced by half by gating the START signal with the CLOCK4 and the Up signals, refer to Figure 2. The process is to simply force the A/D Convertor to take on the upper value of the one bit variation so that the uncertainty at the beginning is -LSD rather than $\pm$ LSD, thus reducing the uncertainty at the termination value to $\pm$ LSD.

The steps involved in calculating the error are:

1. Define error created by the power uncertainty as;

$$\text{Error}_1 = \frac{\Delta t\big|_{P=2\cdot P_0}}{t_2} \times 100\%$$

2. Replace T in the expression for Δt by $T = {}^{t_2}/_{0.69}$.
3. The power per bit resolution of the convertor, defined as ΔP, is expressed as the full scale power ($P_{F.S.}$) divided by 255_{10}.
4. Evaluated the error expression at the termination value of $P = 2\cdot P_0$ replacing P_0 with $K\cdot P_{f.s.}$. Where K is the fractional part of full scale power, i.e. $K = {}^{P_0}/_{P_{F.S.}}$.

The culmination of these three steps is:

$$\text{Error}_1 = \frac{1}{0.69\cdot 2\cdot 255\cdot K} \times 100\% = \frac{0.28}{K}\ \%$$

Thus, as one might expect, the accuracy of a measurement depends on the initial starting point of the measurement.

The second error term can be calculated in a similar manner using the figure of ±½ LSD for linearity quoted by the manufacturer of the DAC module used in the A/D unit. The only difference in the calculation is brought about by the fact that the nonlinearity does not have to have the same sign at the termination and initiation points, therefore, one will have to consider the effect of the uncertainty at both locations. The ±½ LSD uncertainty at the initiation point will be multiplied by two at the termination point and the termination nonlinearity will add another ±½ LSD so the effective uncertainty due to nonlinearity will be one and one-half counts. Thus the error due to nonlinearity is expressed by:

$$\text{Error}_2 = \frac{\Delta t\big|_{\text{start.}} + \Delta t\big|_{\text{stop.}}}{t_2} \times 100\%$$

$$= \pm\frac{\Delta t\big|_{P=2P_0} + \tfrac{1}{2}\Delta t\big|_{P=2P_0}}{t_2} \times 100\%$$

$$\text{Error} = \pm\frac{0.43}{K}\ \%$$

The maximum error possible would be the simple sum of the error sources so that:

$$\text{Error}_{\text{Total}} = \text{Error}_1 + \text{Error}_2 = \pm\frac{0.71}{K}\ \%$$

The possible error ranges from a low of ± 1.5% for K = 0.5, initial power equal to one-half the full scale value, thru 7.1% at K = 0.1, initial power one-tenth the full scale value. As can be seen, one must utilize the upper half of the instrument's range to achieve maximum accuracy when making period measurements.

V. CONCLUSIONS

A basic digital instrument has been designed, constructed and installed on the UMRR. Although not particularly sophisticated the instrument has the advantages of modest cost, improved convenience and improved accuracy. The instrument automatically completes the measurement of reactor period, positive or negative, by physically measuring the doubling time and displaying the equivalent reactor period on a four digit decimal readout. The instrument can measure stable periods up to 999.9 sec. with a possible error of less than 1.5%, if one uses the entire measurement range. It is difficult to compare the 1.5% figure to the manual method of measurement because the operator was an integral part of the system, but we can show a two-to-one improvement in the power resolving ability of the digital device and an improvement of three-to-two in the linearity of the A/D Convertor when compared to the recorder. Thus we can simply say that there is an increase in the accuracy of the system.

There are three considerations to be observed when using the instrument to measure positive period:

1. The power must double from the initial value, therefore, the pico-ammeter must be less than half scale prior to the initiation of a measurement.
2. Accuracy is inversely proportional to the initial power, therefore, one would like to start as near to half scale as possible.
3. Switching the pico-ammeter during a measurement will cause an erroneous reading.

When measuring negative periods one must observe two considerations to insure maximum accuracy.

1. The initial value should be near full scale.
2. Switching the pico-ammeter during a measurement invalidates the reading.

As long as the preceding considerations are followed the measured period will have an error of less than one and one-half percent.

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